# SUN 3 MBit Ethernet Board

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# SUN 3 MBit Ethernet Board

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### Features

- Implements Xerox 3 MBit/sec Ethernet Specifications
- Performs Ethernet Data Link Layer Functions data encapsulation, framing, addressing, CRC generation/checking, CSMA/CD data link management and contention resolution
- Performs Ethernet Physical Layer Functions data encoding and decoding channel access
- High Station Performance back-to-back packet capability full-duplex operation
   4K byte packet buffers for receiver and transmitter bit-vector address recognition allowing any multicast groups
   4 MByte/sec bus transfer rate
   0-access time device
- Exception Reporting and Diagnostics timeout on transmit error status on receive loopback capability
- single board compatible with IEEE-796 Bus (Intel Multibus)
  6.75 by 12 inch board
  796-compatibility: D16 I16 VOL
  16-bit parallel port host interface
  readily compatible with most micro and minicomputers
- 5V-only operation onboard 15V voltage converter for transceiver

### **Overview**

The SUN 3 MBit/sec Ethernet board provides a high-performance interface between the "experimental" 3-MBit/sec Xerox Ethernet and the IEEE-796 Bus (Intel Multibus). It supports a full implementation of the 3 MBit/sec Ethernet data link layer and physical layer in hardware/firmware.

On-board packet buffering avoids real-time demands on host computer system. Parallel port type host interface is compatible with most micro or minicomputers and has data transfer throughput up to 4 MByte/sec.

### SUN Ethernet Board Architecture

The SUN Ethernet board was designed as a high-performance 3 MBit/sec Ethernet interface capable of supporting workstations, gateways, TIPs, and other busy servers. The board performs all specified data link layer and physical layer functions and provides packet buffering. As shown in Figure 1, the SUN Ethernet board in conjunction with a transceiver unit provides a microprocessor host system with a complete connection to the 3 MBit/sec Ethernet local area network.



### Figure 1: The SUN Ethernet Interface

Figure 2 shows a 3 Mbit/sec Ethernet packet. The packet contains a single startbit, followed by eight bit fields for destination address and source address, a variable-length data field, and a 16-bit CRC code.

StartBit	Destination Address	Source Address	DATA	CRC
1-Bit	8-Bit	8-Bit	16 TO 2048 Bytes	16 Bit

### Figure 2: A 3 MBit/sec Ethernet Packet

The destination address field specifies the station(s) on a local Ethernet for which this packet is intended. Since it is a 8-bit quantity, at most 256 stations can be connected to a local Ethernet. A destination address of 0 means the packet is a broadcast packet addressed to all receiving stations. Multicast addresses can be established at will within the addressing range. The source address field identifies uniquely the station transmitting the packet within a local Ethernet. Each station connected

to an Ethernet has a "native" address to identify it. Since this address is relative to a particular Ethernet, the native address is usually switch selectable.

The data field allows arbitrary information of variable length to be transmitted. Although the original Xerox 3 MBit/sec Ethernet does not specify size constraints for the data field, it is recommended that the minimum data field is 8 16-bit words or 16 Bytes and the maximum is 1024 16-bit words or 2048 bytes. The rational for the minimum length is to avoid "invisible" collisions. The maximum packet length assures that no single station can monopolize the network.



### Figure 3: SUN Ethernet Block Diagram

As shown in Figure 3, the SUN Ethernet interface consists of a receiver/transmitter frontend that converts between Ethernet bit-serial data and word-parallel data. Also, the frontend handles the other physical layer functions such as channel access and collision detection. Incoming packets are put into a queue from which they can be read by the host computer. An interrupt is generated whenever the queue is non-empty. On the transmitter side, a packet buffer holds one packet at a time that is to be transmitted. An interrupt is generated when the packet has been sent or when the transmit attempt has been aborted.

### **SUN Ethernet Board Functions**

The SUN Ethernet board performs all the Data Link Layer and Physical Layer functions for the 3 Mbit/sec Ethernet. These functions include transmit data encapsulation, transmit data encoding, transmit link management, receive data decoding, receive data decapsulation, and receive link management. The functions are implemented in such a way to allow maximum station performance and to provide a simple host computer interface.

### Transmit Data Encapsulation and Encoding

The packet to be sent, including address and data fields, is prepared by the host computer and loaded into the on-board packet buffer. During transmission, the SUN Ethernet interface generates the startbit preamble for all receivers on the network to synchronize on, converts the packet from word-parallel to bit-serial, computes the 16-bit CRC value and appends it at the end of the packet. The serial bit-stream to the Ethernet transceiver is Manchester-encoded to be self-synchronizing.

### **Transmit Link Management**

The SUN Ethernet board incorporates all functions necessary to successfully deliver a packet onto the network. These functions include:

**Carrier Deference:** The SUN Ethernet interface defers any transmission until the channel is idle and there are no other ongoing transmissions.

Collision Detection: After starting with its own transmission, a collision may occur with other stations simultaneously starting their transmissions. Upon detecting a collision, the SUN Ethernet interface will abort its own transmission and jam the channel to enforce collision consensus.

**Randomized Retransmission:** When a transmission has been aborted due to a collision, the SUN Ethernet interface attempts its transmission again after waiting a randomized time period, which is computed according to a binary exponential backoff algorithm.

The SUN Ethernet interface automatically performs the exponential backoff retransmission algorithm using a slot time of 42 microseconds. The mean value of the retransmission time interval is thus MIN(number of retries, 8) \* 42 microseconds)/2. When retransmission attempts have been unsuccessful for more than 160 milliseconds, a timeout aborts the retransmission attempts. The interface has no preset upper limit on the number of retry attempts, except for the timeout interval. Thus the minimum number of retry attempts is 16 and the expected number of retry attempts is 32.

### **Receive Data Decoding and Decapsulation**

Manchester-encoded data from the Ethernet is decoded on the SUN Ethernet interface with a digital phase-locked loop and then converted from bit-serial into word-parallel.

The SUN Ethernet interface removes the startbit from the packet and checks the destination address of all incoming packets against an address filter, only accepting packets with matching addresses. An accepted packet is placed into the receiver FIFO buffer together with its status.

The SUN Ethernet interface supports completely general multicast address recognition with a "bitvector" address filter. This address filter is implemented as a 256-Bit RAM. For each of the possible 256 Ethernet addresses, the filter contains either a "1" bit, to accept packets with that address, or a "0" bit to reject packets. The address filter is setup during initialization in software. A hardware address switch register is also provided to provide a "native" address on the local Ethernet. The SUN Ethernet interface validates the integrity of a received packet by generating a CRC on the received bit stream and checking it against the CRC found in the packet, by checking that the packet consists of an integral number of words and that no phase distortion or collision was associated with reception of the packet.

### **Receive Link Management**

Collision detection and carrier deference cause most collisions on the Ethernet to result in fragemented packets only a few bits long. The SUN Ethernet board rejects packets fragments that are shorter than 17 bit times or 5 microseconds. Longer packets that pass through the address filter and collide at a later point appear in the receiver FIFO with error status.

### IEEE-796 Bus Interface

The host processor bus interface is a 16-bit parallel port compatible with the IEEE-796 Microcomputer Bus standard (Intel Multibus). This interface is also compatible with virtually any host computer that offer parallel port interfaces.

The host computer communicates with the Ethernet interface through three read registers, three write registers, and an interrupt line. The registers are accessible as 4 consecutive word addresses that can be located on a 256-byte boundary anywhere in the 16-bit 796-Bus I/O address space.

#### High Station Performance

The SUN Ethernet board has been designed to offer maximum network performance and maximum data-bus through-put while minimizing the service load placed on the host computer.

The SUN Ethernet interface includes a 4K Bytes receiver FIFO that buffers the host computer system from the unpredictable arrival times of network traffic. A 4K Byte buffer size offers a latency of 5 milliseconds, assuming 2048 byte maximum packets.

The SUN Ethernet interface can handle any number of back-to-back packets (multiple packets immediately following each other) and allows full-duplex transmission and reception. Thus it can receive packets sent to itself (loopback packets), allowing self-testing.

Using a look-ahead port, the host processor interface features a zero access time and supports high-speed data transfers at rates of up to 4 Mbyte/sec. The SUN Ethernet interface can simultaneously transmit packets, receive packets, and transfer packets on the bus interface without degrading any of its performance specifications.

### Comparision between 3 and 10 MBit/sec Ethernets

The 3 Mbit/sec Ethernet is the "original" Ethernet developed at Xerox Corporation from which the "standard" 10 MBit/sec DEC/Intel/Xerox Ethernet evolved. 3 MBit/sec Ethernets are in use inside Xerox Corporation and at several Universities and research institutions, including Stanford University, MIT, Cal-Tech, Rochester, and Carnegie-Mellon. The SUN Ethernet board addresses primarily the market of existing 3 MBit/sec network installatios and applications for which the 3 MBit/sec specifications are advantageous. It is also suitable for implementing gateways between 3 MBit/sec and 10 MBit/sec Ethernets.

The main differences between 3 and 10 MBit/sec Ethernet are in packet format, timing, and transceiver signal levels.

Packet format: A 3 MBit/sec Ethernet packet has a single start bit, 8-bit destination and source addresses, an integral number of 16-bit data words, and a 16-bit CRC code. A standard 10 MBit/sec Ethernet frame uses a 64-bit preample, 48-bit addressing, and a 32-bit CRC code. The minimum recommended packet length for 3 MBit/sec is 20 bytes, for 10 MBit/sec the minimum is 72 bytes. Maximum recommended packet length for 3 MBit/sec is 2052 bytes, for 10 Mbit/sec the maximum is 1526 bytes.

Timing: Besides the obvious difference is the bit rate, the two networks differ in interpacket spacing time and slot time. The 3 MBit/sec Ethernet places no restrictions on interpacket spacing, whereas at 10 MBit the interframe spacing is 9.6 microseconds. 3 MBit/sec slot time has varied from 28 to 42 microseconds, on 10 MBit/sec the slot time is specified as 50 microseconds.

Transceiver: 3 MBit/sec Ethernet uses a "TTL" transceiver with unipolar drive, wheras the 10 MBit/sec Ethernet uses an "ECL" transceiver with bipolar drive. It is possible to adapt the SUN Ethernet board to standard 10 MBit/sec ECL transceivers that can operate at a 3 MBit/sec frequency. In this case, it appears that 3 MBit/sec Ethernets can be intermixed with 10 MBit/sec networks on the same coaxial cable. It is also possible to embed maximum-size 10 MBit/sec frames in 3 MBit/sec packets.

### References

R.M.Metcalfe and D.R.Boggs, "Ethernet: Distributed Packet Switching for Local Computer Networks", Communications of the ACM, 19, 7, July 1976.

Digital Equipment Corporation, Intel Corporation, and Xerox Corporation, The Ethernet, A Local Area Network, Data Link Layer and Physical Layer Specifications, September 1980.

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### Using the SUN Ethernet Interface

### Sending a Packet

After preparing the packet to be sent, including addresses but excluding CRC, the host computer loads the packet into the on-board transmit packet buffer. To load a packet, the host first writes a control word specifying the total number of words in the packet (the wordcount) and then the specified number of data words to the TRANSMITTER DATA PORT. Upon completing this transfer, the Ethernet interface automatically attempts to acquire the Ethernet and to send the message.

The Ethernet interface returns to the host with a TRANSMITTER interrupt either when the message has been successfully sent or when the timeout interval of 160 milliseconds has expired without having sent the message successfully. The TIMEOUT bit in the READ STATUS register is set when the message was not sent successfully.

### **Receiving Packets**

When a incoming packet passed the address filter and has been completely received, it is put into the receiver FIFO buffer, prefixed with a control word that specifies its length (word count) and its status. The packet status indicates whether there was a CRC-Error, a collision, or a FIFO overflow associated with the packet. Another status bit, the QEMPTY bit, is set whenever the FIFO is empty and is cleared when a complete packet is waiting in the receiver queue. Repeated read attempts beyond a QEMPTY control word will always return the same control word, thus the receiver FIFO cannot underflow.

When the FIFO is non-empty, the RECEIVER interrupt is set to inform the host that a valid control word can be read from the interface. In response, the host computer will read the control word and the specified number of words from the RECEIVER DATA PORT. Packets with error status can be analysed to collect network diagnostics or they can be simply discarded. In any case, all packets must be removed from the receiver queue by reading the specified number of words.

A slight complication is caused the fact that the RECEIVER DATA PORT is a look-ahead port. This implies that the first word read after a RECEIVER interrupt is invalid and needs to discarded. The second word read contains the actual status and the wordcount of the packet. Only the first packet read after the queue was previously empty is an invalid lookahead word, the lookahead is transparent for any other packet waiting.

### Interrupt Handling

The SUN Ethernet interface uses a single interrupt line to signal transmitter or receiver interrupts to the host-computer. Transmitter and receiver interrupts can be separately enabled by setting the corresponding bits in the WRITE STATUS register. The interrupt level can be selected under software control via the INTERRUPT LEVEL bits in the WRITE STATUS register.

Upon receiving an interrupt, the source can be distinguished by reading the READ STATUS register. A transmit interrupt can be cleared in software by accessing the CLEAR TX INTERRUPT location. A receiver interrupt is cleared automatically whenever the receiver FIFO is empty.

The maximum latency to deal with RECEIVER interrupts is 5 milliseconds, which is the shortest time in which the receiver buffer could fill up assuming a maximum packet length of 2048 bytes. TRANSMITTER interrupts do not require any immediate service.

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### Initialization

Before the Ethernet interface can be used, it must be initialized from the local host computer. This involves loading a valid address map into the receiver, enabling of the transmitter and the receiver, and enabling interrupts.

Initializing is done via the WRITE STATUS REGISTER. Upon hardware reset, all bits in the WRITE STATUS REGISTER are set to ones. Thus INIT and LOOPBACK are asserted (enabled) whereas RECEIVER and TRANSMITTER INTERRUPT ENABLE is negated, disabling interrupts to the host computer. The INIT flag has two effects: First, it disables the Ethernet receiver and enables loading of the address filter. Second it causes the controller to initialize the buffer pointers. The LOOPBACK bit isolates the transmitter and the receiver from the Ethernet transceiver and connectes the transmitter directly to the receiver.

The address filter is loaded address by address under host control. First, INIT must be set to enable address loading. Then for each address the desired data bit is set up in the FILTER DATA Bit in the WRITE STATUS register and the address is written to the WRITE ADDRESS register.

The Ethernet interface also has a switchable hardware address that can be accessed as the READ ADDRESS. This is a read-only hardwired switch that does not affect the address filtering in the receiver. Its purpose is to establish an initial Ethernet address after booting.

To connect to the Ethernet, the INIT and LOOPBACK bit need to be cleared. Also, for interrupt driven software, the desired interrupt level on the bus is programmed into the WRITE STATUS REGISTER and RECEIVER and TRANSMITTER INTERRUPT need to be enabled.

## Interface Registers

R/W	Adrs	Data
Read	0	<015> Receiver Data Port
		Format for control word:
		<0:11> Word Count
		<12> CRC-Error
		<13> Collision/Abort
		<14> Receiver queue overflow
		<15> Qempty
Read	4	<12:15> Read Status Register
		<12> Interrupt Flag
		<13> Receiver Interrupt (before enable)
		<14> Transmitter Timeout
		<15> Transmitter Interrupt (before enable)
Read	6	<07> Read Hardwired Switch Address / Clear Tx Interrupt
Write	0	<015> Transmitter Data Port
		Format for control word:
		<0:11> Word Count
		<12:15> 0
Write	4	<815> Write Status Register
		(all bits set to 1 on hardware reset)
		<810> Interrupt Level (inverted)
		<11> Receiver Interrupt Enable (inverted)
		<12> Transmitter Interrupt Enable (inverted)
		<13> Filter Data Bit (inverted)
		<14> Loopback (non-inverted)
		<15> Init (non-inverted)
Write	6	<07> Write Receiver Address Filter

### **Specifications**

### Network

"experimental" 3 MBit/sec Xerox Ethernet 8-bit addressing, 16-bit CRC, up to 2048 Bytes Data. coaxial cable up to 1 kilometer up to 256 transceivers per cable

### Transceiver

Compatible with Xerox TTL transceiver, Part # 209926. Mating Connector: 26-pin flat cable. Transceiver Signals: TxData\, RxData\, Collision, +5V, +15V

### **Functions**

Implements 3 MBit/sec Data Link Layer Functions 4K Byte F⊮o buffer for receiver 4K Byte Buffer for transmitter handles back-to-back packets loopback capability for self-test bit-vector address filtering local address switches

### 796-Bus Compatibility

D16 I16 VOL, 16-bit data only.

### **Electrical Characteristics**

VCC = +5V + -5%, ICC = 6A max. 15V Voltage Converter for Xerox transceiver included on board.

### Physical Characteristics

Width:	12.00	in.	(30.48	Cm)
Height:	6.75	in.	(17.15	cm)
Depth:	0.50	in.	(1.27	cm)
Weight:	16 02	2.	(447 g	)

### **Environmental Characteristics**

Operating Temparature: 0-50 C

# SUN 3MBit/sec Ethernet Board

#### Installation Manual

SUN Microsystems Inc. May 1982

### **General Description**

The SUN 3 MBit/sec Ethernet Board provides the connection of the SUN Workstation and other machines using the Intel Multibus (TM) backplane to Ethernet-1, the experimental 3 MBit/sec Ethernet developed by Xerox PARC.

The SUN 3 MBit/sec Ethernet Board interfaces with the CPU via programmed I/O and interrupt. In Multibus notation, the board is a I/O slave with 16-bit addressing and 16-bit data paths. Note that the board is not readily compatible with 8-bit Multibus I/O.

### **Unpacking Instructions**

Inspect the shipping carton immediately upon receipt for evidence of damage. If the shipping carton is severely damaged, request that the carrier's agent be present when the carton is opened. If the carrier's agent is not present when the carton is opened and the contents are damaged, keep the content and carton for the agent's inspection.

It is suggested that salvageable shipping cartons and packing material be saved for future use in the event the product must be reshipped.

### Installation Considerations

The board is designed for installation into a Intel Multibus compatible backplane or cardcage.

**POWER:** The Board requires a 5V power supply and draws a maximum current of 6 Amp. The board includes an on-board voltage converter that generates the 15V power for the Xerox transceiver.

COOLING: The board dissipates 30 Watts. When installing the board in an enclosed environment or under restricted airflow conditions, ensure that the internal operating temperature does not exceed 130 degree F or 55 degree C.

CAUTION: To prevent possible equipment damage, do not install board in a cardcage while power is on. Also, to prevent damage due to static voltages, avoid exposing the board to plastic materials.

#### Ethernet Tranceiver and Cable

The SUN 3-Mbit Ethernet Board is designed to interface directly to the Xerox 3-Mbit Transceiver part # 209926. This transceiver is also available as TLC Part # 2000. The cables described below apply to this particular transceiver. The assembly is shown in Figure 1.

The 3 MBit/sec Ethernet transceiver is designed for RG-8/U Type Foam Coax with a solid center

conductor and a characteristic impedance of 75 Ohm. The Ethernet cable must be terminated at both ends with a 75 Ohm terminator.

### **Cable between Transceiver and Board**

The cable that connects the transceiver to computing equipment is Xerox Part # 216411D. The cable contains six twisted pairs of wire and features a female 15-pin D-connector on the transceiver side and a male 25-pin D-connector on the receiver side. The cable can be up to 15 meter long.

The SUN Ethernet board is designed to interface directly to the above Transceiver cable via a flatcable assembly. The flat cable consists of a 26-pin header and a 25-pin D-type female connector, with wire-1 connecting to pin-1 of both sides and wire-26 ommitted for the 25-pin connector. It is recommended that the flat cable not exceeds 1 meter in length.

### Switches on SUN Ethernet Board

The SUN Ethernet Board has two octal dip-switches: one to select the Multibus base address and one to select the local Ethernet host address. The location of these switches is shown in Figure 1.

### Switch Setting for Multibus Base Address

The SUN 3 Mbit/sec Ethernet interface communicates with the host CPU via 4 read and 4 write registers located in Multibus I/O space. The registers are located on successive word (16-bit) boundaries starting on a 256-byte boundary within the 64k Multibus I/O space. Only the eight high-order address bits are decoded for the selection of the board; thus the interface will respond to 256 consecutive byte addresses even if only 4 word addresses are decoded.

To select the Multibus base address, take address bits A8..A15 of the desired address and encode them into dip-switch S505. Switch #1 is the least significant bit, and "1" bits correspond to "ON" switches.

By convention, 0x100 is the normal address for the first Ethernet board, and subsequent boards if any are placed at successively higher addresses.

#### Switch Setting for Ethernet Host Address

After obtaining an Ethernet host number from your local Ethernet administrator, express it in binary and set it into dip-switch S507. Switch #1 is the least significant bit, and "0" bits correspond to "ON" switches, unlike the correspondance used for the Multibus base address.

Note: Ethernet addresses "0" and "0377" (octal) are reserved for special Ethernet functions and should not be used as a host address.



## Figure 1: SUN 3 MBit/sec Ethernet Installation

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RX.ABORT\ GND RX.END RX.PU RX.CRCERR 12D S 09 1174LS74 UB128 RX.CRCERR 12D S 09 1174LS74 UB128 B C.READ 'n



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D8 D9 D10 D11 D4 D5 D6 D7 D0 D1 D2 D3 24232426 D3D2D1D0 2222222 222 2426 D3D2D1D0 D3D2D1D0  $\begin{array}{c} C.10\\ \hline C.11\\ \hline C.12\\ \hline C.13\\ \hline C.14\\ \hline C.16\\ \hline C.16\\ \hline C.16\\ \hline C.17\\ \hline C.18\\ \hline C.18\\ \hline \end{array}$ 12 13 14 12 13 10 10 10 11 11 I 1 14 12 12 12 13 13 13 28 14 15 16 17 14 14 15 15 16 16 17 18 18 18 C.A0 C.A1 C.A2 C.A3 A0 A1 A2 A3 40 AO A1 AI 142 A2 AM2901 AN2901 AM2901 C.80 C.81 C.82 C.83 80 80 U102 U103 U105 81 82 R 2 R 2 83 83 83 <u>C170.85-0 16</u> 16 CР 00 21 C.PU 50 9 C.PU 16 Q3 32 G 35 G 34 C4 34 OVR 31 F3 40 C5 03 Q3 sol So ŝз 32 G 35 G 35 G 35 C4 34 OVR 31 F3 11 F0 10 OC \$3 C.CYE G C0 29 C.19 C0 29 C0 29 64 DVR F 3 C.NEG C.ZERO GND FO 40 0573Y2Y1Y0 Po 05/3Y2Y1Y0 0573727170 34343736 30303136 31313136 C. Y8 C. Y9 C. Y10 C. Y11 C.Y0 C.Y1 C.Y2 C.Y3 C. Y4 C.Y6 C.Y7 6 0 9 1411 12 13 4 13 6393C36292C261PiC 160P0C0 9 6 M2002 9 6 U201



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DS 2 U408 18 8.) C.PU 41A11Y 16	ACK
6 1A217 14 8 1A3173 12 INT 11 1A4174 9 8	D12\
R. INTERRUPT 32A12Y 7 B. TX. TINEOUT 152A22Y27 B.	D13\ D14\
T. INTERRUPT 72A32Y 3 B.	0151
BUSSELN T1 19	

D1

INTO INTI INTZ INT\

8.08\ 3 8.09\ 4 8.010\ 7 8.011\ 6 8.012\ 13 8.013\ 14 8.014\ 17 8.016\ 18	4LS2 U510 D1 Q1 D2 Q2 D3 Q3 D4 Q4 D5 Q8 D8 Q8 D7 Q7 D8 Q8 CK CF	3 2 5 6 9 12 16 16 19	INTO INTI INTZ R.INTEN T.INTEN R.FOIN LOOPBACKY INITY
STATUS.WE\ B.INIT\			

8.00\ 8.01\ 8.02\ 8.03\ 8.04\ 8.04\ 8.06\ 8.06\ 8.07\

ADRS.WEL

14L<u>55</u>3

D2 0.

7 D2 Q2 06 8 D3 Q3 09 13 D4 Q4 012 14 D5 Q5 016 17 D6 Q6 016 17 D6 Q6 016 18 D7 Q7 019 18 D8 Q9 0

EN OE

RX . A0 RX . A1 RX . A2 RX . A3 RX . A4 RX . A5 RX . A5 RX . A5

R.FWE\

	745240	
P.WRITEACK\2	USCZ	18 P.WRITEACK
P.WRITEREQ 4	141111	16P.WRITEREQ
B.IORC\ 6	142112	14 BUSREAD
B.IOWC\ 8	143113	12 BUSWRITE
C.ZERO 11	DA12V	9 C.ZEROV
C.NEG 13	5A22V2	7 C.NEGV
INT 15	5A32V	5 INT
RX.ENABLE 17	DAA274	3 RX.ENABLE
	1626	
GND	راليك_	)

BUSREAD 4 71504 6 <u>P.READREOG</u> 71504 6 <u>BUSWRITE10</u> 12 74501 11 DS 13 74501 051 <u>P.WRITEREG</u> 71507 0 <u>P.WRITEREG</u> 71507 0 <u>WRITEN</u>

8. INTO 8. INTI 8. INTZ 8. INTZ 8. INTZ 8. INTZ 8. INTZ 8. INTE 8. INTE 8. INTE 8. INTE

