Sun-2 Ethernet Interface Spec

W. M. Bradley

ABSTRACT

This specification describes the architecture of the Sun-2 Ethernet Interface.

Overview

The Sun-2 Ethernet interface consists of an Ethernet Data Link Controller (EDLC), an Encoder-Decoder, and 256 Kbytes of dual-ported memory on a single Multibus card. One of the memory ports is dedicated to the EDLC, the other to the Multibus. Memory may be expanded up to 3.25 MBytes using Sun 1 MByte expansion memory cards. The board will support 256 kbit RAMs, for 1 MByte of on-board memory.

Ethernet Interface

The Ethernet interface is implemented using an Intel 82586 EDLC chip. The 82586 provides command and buffer chaining facilities so that back-to-back Ethernet packets may be received. All commands to the 82586 are sent via memory-resident parameter blocks.

The EDLC interrupts the processor to signal various events. Interrupts are not vectored.

The encoder-decoder function is performed on-board. The card connects directly to an external Ethernet transceiver.

Memory

Local dual-ported memory is used to transfer all commands and data. The dual-ported memory consists of 256 Kbytes of on-board memory, and up to 3 MBytes of external expansion memory. The on-board memory consists of 256 KBytes of RAM, organized as 128 K 16-bit words, with byte parity. When 256 Kbit dynamic RAMs become available, they may be substituted for the 64 K RAMs memory, giving up to 1 MByte of on-board memory. Expansion memory consists of from 0 to 3 Sun 1 MByte expansion memory boards on a P2 bus private to the Ethernet board. If expansion memory is not used, the board may be jumpered so that it does not use the P2 bus, so the board may be plugged into a slot where the P2 bus is used for some other purpose.

The memory is locally mappable in 1 Kbyte pages. The EDLC chip has a logical address space of 1 K pages, each of 1 Kbyte, for a total of 1 MByte. The Multibus port has a logical address space of up to 256 pages, for a total of 256 Kbytes. Each page may be mapped to any page boundary in the 4 MByte physical address space of the local memory. The Multibus port may be either 64K, 128K, or 256K bytes, configurable with switches. The address space of the Multibus port may be assigned via jumpers to any (64,128,256)K boundary within the 1 MByte Multibus address space. The base address must be a multiple of the port size.

Any page may be configured so that the bytes within a word are swapped when a word within that page is accessed from the Multibus. This may be used to rearrange the bytes so that both the 68000 and other peripherals (which tend to use Intel byte order) see data in their natural byte order. This feature is controlled via a bit in each page map entry. The byte swap bit has no effect on EDLC memory accesses.

The proper usage is to arrange for all data written to the local memory to be in the proper order for the EDLC chip, i.e. Intel byte order. The processor may then access this data in its natural byte order by setting the swap bit in the page map entry that it uses to address the data. If there are Multibus devices that DMA transfer into the local memory, the page map should be set up so that the resulting byte order in the memory is Intel byte order.

Page Map

The page map is organized as 1 K words of 16 bits each. The address to the page map is the logical page number. The lower 12 data bits are the physical page number. The most-significant-bit, bit 15, is the byte swap control bit - 1 for 68000 byte order, 0 for Intel byte order. Intel byte order puts the least significant or lower byte at the lower address (A0 = 0), while 68000 byte order has the least significant byte at the higher address (A0 = 1). Bit 13 selects on-board memory if 0 and P2 memory if 1.

The page map may be read and written via the Multibus. It occupies a 2K bank of Multibus memory space and is accessed just like memory. The base address for accessing the Page Map is separately selectable from the base address of the Multibus memory port.

Parity

Byte parity on the local memory is implemented. If a parity error occurs, the logical address of the offending memory location is stored in a register. A flag is set in the register, telling which port was accessing the memory when the error occurred. The register also has a separate bit for the high byte and the low byte, showing which of the bytes had an error. If parity error interrupts are enabled, a parity error will cause an interrupt at the same priority as all of the other types of interrupts that the board generates. Bits in the status register identify the reason for the interrupt.

After a parity error occurs, the EDLC is disabled and cannot access memory until the parity error interrupt request is cleared. This prevents the EDLC from going into a strange state and doing something random. The EDLC should be completely reinitialized in this case.

The error address register is 32 bits wide, appearing in Multibus memory space as two consequetive 16 bit words. Once an error occurs, the error address register is "locked", so that it may not be written again until it has been acknowledged. Acknowledging the parity error is done by writing anything to the error address register.

Bit 7 of the first word reads as 1 if the error occurred during an EDLC access, and 0 if it occurred during a Multibus access. Bit 6 of the first word is 0 if the high byte was being accessed. Bits 3-0 of the first word are the high order bits of the error address, and bits 15-1 of the second word are the low order bits of the error address. Bit 0 of the second word is 0 if the low byte was being accessed. All other bits read as 0.

A bit in the Status Register (described below) indicates the presence of a parity interrupt request. The physical address of the bad memory location may be determined by consulting the page map.

External Memory

Local memory may be expanded by connecting Sun 1 MByte memory expansion cards to a local bus accessed via the P2 connector. This P2 bus is electrically separate from the P2 bus that the Sun 68000 processor card uses. If no external memory is used, the signals to and from the P2 bus may be disabled by a jumper, so that the placement of the Ethernet card in a card cage will not be constrained by the P2 bus.

ID PROM

A 32 byte PROM is provided on the board. This may be used to contain the Ethernet address or any other information that may be desired. The EDLC cannot access the ID PROM; the CPU may use it or ignore it as it wishes. The ID PROM may be read over the Multibus. Only one byte of the PROM may be read at a time. The data appears on the low-order byte. The high-order byte's value is undefined.

Status Register

The status register tells how much on-board memory is present, which base address has been selected for the Multibus memory port, whether or not P2 memory expansion is enabled, and which types of interrupts are currently pending.

Bit 15 Reset Read/Write

Writing a 1 to this bit causes the whole board to be reset to its initial state. After this has been set, the board will be held in the reset state until a 0 is written to this bit. Asserting the Multibus INIT line will also cause a board reset.

Bit 14 Loopback Enable Read/Write

0 for normal mode. 1 for loopback mode. Loopback mode is a testing function whereby Ethernet packets that are transmitted are immediately received by the transmitting Ethernet node.

Bit 13 Channel Attention Read/Write

Writing a 1 to this bit causes the Channel Attention line of the EDLC to be asserted. This is the way that the CPU gets the attention of the EDLC. After asserting this, you have to explicitly negate it.

Bit 12 EDLC Interrupt Enable Read/Write

0 to diasble interrupts, 1 to enable interrupts. If interrupts are disabled, bit 8 will still display the status of the EDLC interrupt request.

Bit 11 Parity Error Interrupt Enable Read/Write

0 to diasble interrupts, 1 to enable interrupts. If interrupts are disabled, bit 8 will still display the status of the parity error flag.

Bit 10 Reserved

Bit 9 Parity Error Read Only

1 if a parity error has occurred. An interrupt request will be generated if this bit is 1 and Parity Error interrupts are enabled.

Bit 8 EDLC Interrupt Read Only

1 if the EDLC chip wants to interrupt. An interrupt request will be generated if this bit is 1 and EDLC interrupts are enabled.

Bit 7 Reserved

Bit 6 Reserved

Bit 5 Expansion Enabled Read Only

1 if the P2 expansion memory bus is enabled.

Bit 4 On Board Memory Size Read Only

0 if On-board memory is 256 KBytes. 1 if On-board memory is 1 MByte.

Bits 0-3 Multibus Base Address Read Only

These bits show the high order address bits which must be sent to write into the on-board memory from the Multibus Bit 0 corresponds to A16, Bit 1 - A17, Bit 2 - A18, Bit 3 - A19.

Register Map

All registers are 16 bits wide, and may be accessed as either bytes or words. The byte order is 68000 byte order -- the most-significant-byte is at the lower address. Reg Base is the base address of the registers. It is jumper selectable to any 4 Kbyte boundary within Multibus memory space. In the table below, xxx means that the register is not writeable. Attempts to write it will not cause a bus error, but nothing will happen to the Ethernet board.

Address	Read	Write
Reg Base + 0x000	Page Map 0	Page Map 0
...	...	...
Reg Base + 0x7FE	Page Map 1023	Page Map 1023
Reg Base + 0x800	ID PROM 0	xxx
...	...	...
Reg Base + 0x83E	ID PROM 31	xxx
Reg Base + 0x840	Status Register	Status Register
Reg Base + 0x842	undefined	xxx
Reg Base + 0x844	Error Address High	Error Acknowledge
Reg Base + 0x846	Error Address Low	xxx

Power Requirements

5.2 A (max) @ 5 Volts.

Cost

$360, including 256 Kbytes of RAM.

Parts Count

150 16-pin equivalents, including 36 Dynamic RAMs and 116 decoupling capacitors. There are 3 large parts: an 8207 Dual-Ported RAM controller in a 68-pin leadless chip carrier package, an 82586 Ethernet Data Link Controller in a 48-pin DIP package, and an MB502 Ethernet Encoder/Decoder in a 24-pin 600 mil DIP package.