TEK SERVICE MANUAL
VOLUME 1

Part No. 070-3817-00
Product Group 16

4112
COMPUTER DISPLAY TERMINAL

Please Check for
CHANGE INFORMATION
at the Rear of this Manual

First Printing SEP 1982

Tektronix®
COMMITTED TO EXCELLENCE

WARNING

THE FOLLOWING SERVICING INSTRUCTIONS ARE FOR USE BY QUALIFIED PERSONNEL ONLY. TO AVOID PERSONAL INJURY, DO NOT PERFORM ANY SERVICING OTHER THAN THAT CONTAINED IN OPERATING INSTRUCTIONS UNLESS YOU ARE QUALIFIED TO DO SO.

MANUAL REVISION STATUS

PRODUCT: 4112 COMPUTER DISPLAY TERMINAL

This manual supports the following versions of this product: Serial Numbers B010100 and up.

REV DATE	DESCRIPTION
SEPT 1982	Original Issue; replaces 061-2490-00.

CONTENTS

Section 4 **THEORY OVERVIEW**

Section 5 **PROCESSOR BUS THEORY**

Section 5 (cont)

Section 5 (cont)

Section 6 **DISPLAY BUS THEORY**

Section 6 (cont)

Section 10 TROUBLESHOOTING AND SELF-TEST DIAGNOSTIC

Appendix C EXTERNAL VIDEO OPTION

ILLUSTRATIONS

TABLES

OPERATORS SAFETY SUMMARY

This general safety information is for both operating and servicing personnel. Specific warnings and cautions will be found throughout the manual where they apply, but may not appear in this summary.

TERMS

IN THIS MANUAL

CAUTION statements identify conditions or practices that can result in damage to the equipment or other property.

WARNING statements identify conditions or practices that can result in personal injury or loss of life.

AS MARKED ON EQUIPMENT

CAUTION indicates a personal injury hazard not immediately accessible as one reads the marking, or a hazard to property including the equipment itself.

DANGER indicates a personal injury hazard immediately accessible as one reads the marking.

SYMBOLS

IN THIS MANUAL


This symbol indicates where applicable cautionary or other information is to be found.

AS MARKED ON EQUIPMENT


DANGER high voltage.


Protective ground (earth) terminal.


ATTENTION—refer to manual.


Refer to manual.

POWER SOURCE

This product is designed to operate from a power source that does not apply more than 250 volts rms between the supply conductors or between either supply conductor and ground. A protective ground connection by way of the grounding conductor in the power cord is essential for safe operation.

GROUNDING THE PRODUCT

This product is grounded through the grounding conductor of the power cord. To avoid electrical shock, plug the power cord into a properly wired receptacle before connecting to the power input or output terminals. A protective ground connection by way of the grounding conductor in the power cord is essential for safe operation.

DANGER ARISING FROM LOSS OF GROUND

Upon loss of the protective-ground connection, all accessible conductive parts (including knobs and controls that may appear to be insulating) can render an electric shock.

USE THE PROPER POWER CORD

Use only the power cord and connector specified for your product.

Use only a power cord that is in good condition.

Refer cord and connector changes to qualified service personnel.

USE THE PROPER FUSE

To avoid fire hazard, use only the fuse specified in the parts list for your product, and which is identical in type, voltage rating, and current rating.

Refer fuse replacement to qualified service personnel.

DO NOT OPERATE IN EXPLOSIVE ATMOSPHERES

To avoid explosion, do not operate this product in an atmosphere of explosive gases unless it has been specifically certified for such operation.

DO NOT REMOVE COVERS OR PANELS

To avoid personal injury, do not remove the product covers or panels. Do not operate the product without the covers and panels properly installed.

DO NOT OPERATE PLUG-IN UNIT WITHOUT COVERS

To avoid personal injury, do not operate this product without covers or panels installed. Do not apply power to the plug-in via a plug-in extender.

SERVICE SAFETY SUMMARY

FOR QUALIFIED SERVICE PERSONNEL ONLY

Refer also to the preceding Operators Safety Summary.

DO NOT SERVICE ALONE

Do not perform internal service or adjustment of this product unless another person capable of rendering first aid and resuscitation is present.

USE CARE WHEN SERVICING WITH POWER ON

Dangerous voltages may exist at several points in this product. To avoid personal injury, do not touch exposed connections and components while power is on.

Disconnect power before removing the power supply shield, soldering, or replacing components.

DO NOT WEAR JEWELRY

Remove jewelry prior to servicing. Rings, necklaces, and other metallic objects could come into contact with dangerous voltages and currents.

X-RADIATION

X-ray emission generated within this instrument has been sufficiently shielded. Do not modify or otherwise alter the high voltage circuitry or the CRT enclosure.

POWER SOURCE

This product is intended to operate from a power source that will not apply more than 250 volts rms between the supply conductors or between either supply conductor and ground. A protective ground connection by way of the grounding conductor in the power cord is essential for safe operation.

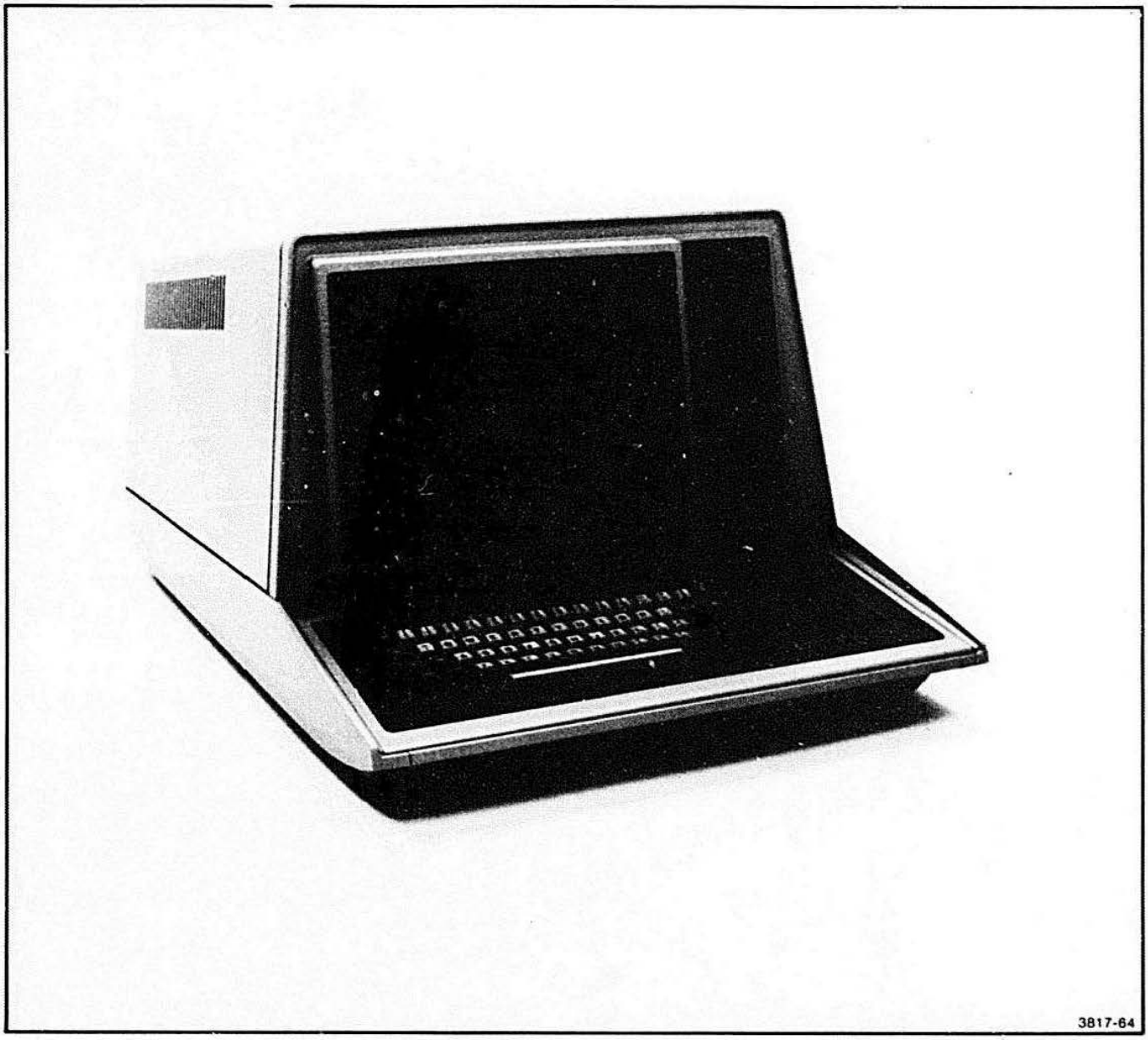


Figure 1-1. The 4112 Computer Display Terminal.

Section 1

INTRODUCTION

ABOUT THIS MANUAL

This is the first volume of a two-volume service manual for the TEKTRONIX 4112 Computer Display Terminal. Volume 1 contains introductory information, characteristics, operator information, detailed theory, maintenance and adjustment procedures, and appendices (signal list, strap options, and theory of operation for the memory and External Video options).

Volume 2 contains a short-form adjustment procedure, schematics, electrical and mechanical parts lists, and appendices (installation, error messages, and logic tables). Volume 2 is intended as an on-site service tool, while Volume 1 is likely to be used in service centers for detailed component-level repair.

This manual is arranged like most Tektronix computer terminal service manuals. However, since the terminal contains several distinct functional parts, this manual divides the operating theory into the following separate sections:

- Overview
- Processor Bus Theory of Operation
- Display Bus Theory of Operation
- Display Module Theory of Operation

Power Supply theory is contained in the *620-0295-00 Low Voltage Power Supply Service Manual*. Refer to that manual for Power Supply theory, troubleshooting, parts lists, etc.

This section includes a list of options available for the 4112 terminal (see *Options*, later in this section). Some options are used in both the 4112 and 4114 terminals, in which case these options have their own separate service manuals. Options with separate service manuals are:

- Disk Drive options (Options 42/43)
- Graphic Tablet options (Options 13/14)
- Three Port Peripheral Interface option (Option 10)

Because the External Video option (Option 11) is only available on the 4112, that option is described in this manual (Appendix D).

RELATED DOCUMENTS

The following documents contain detailed information on the use of the 4112 terminal:

- *Introducing Your 4112*
- *4112 Computer Display Terminal Operator's Manual*
- *4112 Host Programmer's Reference Manual*
- *4110 Series Command Reference Manual*
- Service manuals for any options that are included in the 4112; see *Optional Accessories* (later in this section)

INSTALLATION INFORMATION

Appendix A (Volume 1) provides complete instructions for installing the 4112 terminal. Immediately after receiving the 4112, unpack and inspect it for possible shipping damage. Do not throw away the shipping container until the terminal passes the damage inspection and is fully operational. Run the Self-Test program to verify its functional condition (see Section 8, *Functional Check and Performance Check Procedures*). Also verify that all accessories checked on the Accessories Packing Slip are included and are operational.

GENERAL DESCRIPTION

The 4112 is a raster-scan, intelligent graphics computer terminal. The display is a 15-inch raster-scan crt (cathode ray tube). There are 640 by 480 points on the display surface that are individually addressable. The display uses these points to build line segments and curve segments, which combine to produce complex graphic images.

The 4112's microprocessor-based circuitry responds to inputs of some sixty different graphics-related commands. The terminal responds to these commands by executing the appropriate firmware routines so that graphic images may be created, modified, displayed, and then sent to (or received from) the host computer. The 4112 carries most of the graphics processing time burden when its local graphics commands are used.

MAJOR PARTS OF THE 4112

The 4112 consists of several major functional modules. See Figure 1-2. These modules are:

- The card cage (including its circuit boards)
- The keyboard
- The Display Module
- The Low Voltage Power Supply (and Distribution board)
- The optional flexible disk drive unit

The card cage (and circuit boards) contains the intelligence and control circuitry for the terminal. The keyboard is the primary input device; it contains a standard ASCII keyset, a pair of thumbwheels, and specialized function keys. The Display Module's crt is the primary output device. The Low Voltage Power Supply provides the main power for the other modules in the 4112. The flexible disk drive unit provides mass storage for local programming applications.

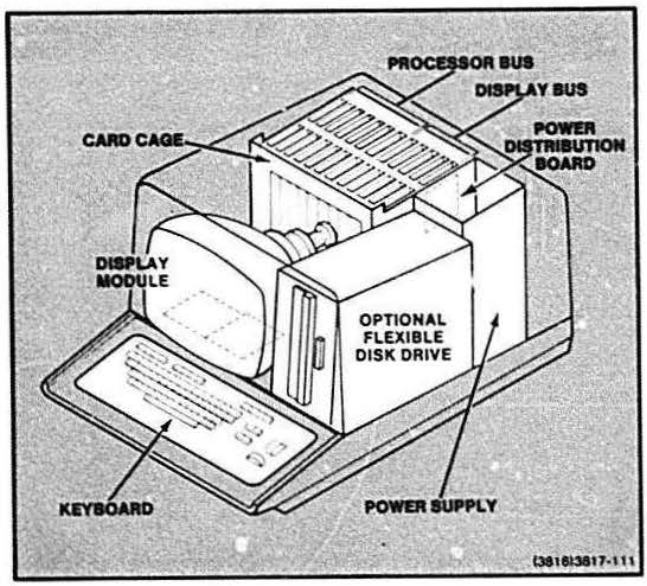


Figure 1-2. 4112 Functional Modules.

FRONT-PANEL CONTROLS AND INDICATORS

The 4112 terminal has the following controls and indicators on the front of the terminal (see Figure 1-3):

- POWER. The POWER switch is a pushbutton located next to the lower-left corner of the display.
- SCREEN INTENSITY. This potentiometer controls the intensity of the images on the display tube. This control is located above the optional disk drive unit, next to its WRITE-PROTECT switch.
- Keyboard. The keyboard consists of these groups of keys, controls, and indicators:
  - Alphanumeric keyset
  - Programmable user-defined function keys
  - LED indicators
  - Predefined function keys
  - Display control keys
  - Thumbwheels

Section 2 describes the front-panel keys, controls and indicators in more detail.

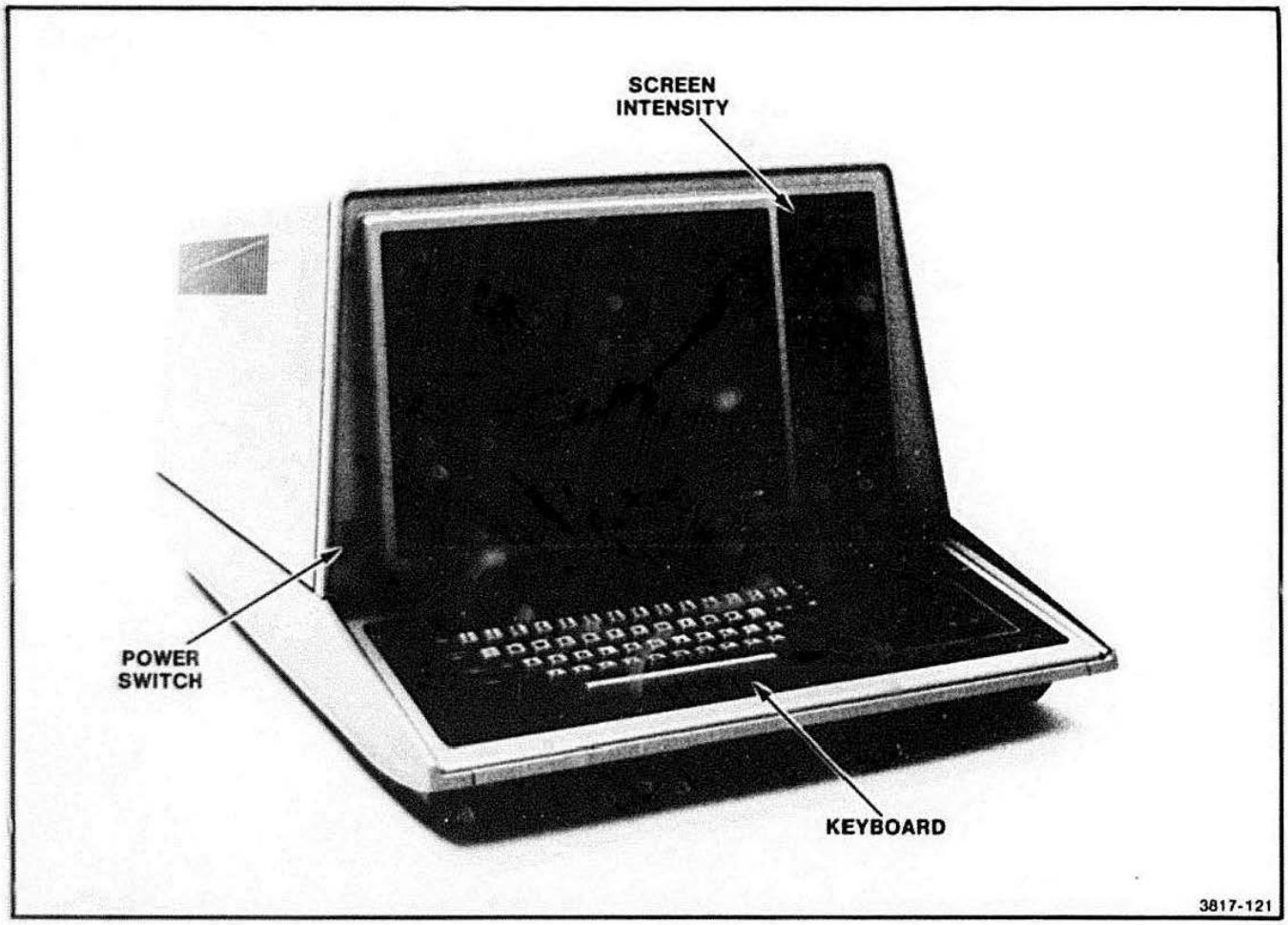


Figure 1-3. Front-Panel Features.

REAR-PANEL CONTROLS AND CONNECTORS

The following controls and connectors are located on the rear panel (see Figure 1-4):

- MASTER RESET switch. This control resets the terminal's user-definable operating parameters and thus returns the terminal to a known state. This pushbutton is mounted on the rear panel above the power-supply cooling fins.

- SELF TEST switch. This pushbutton, when pressed with the MASTER RESET switch, runs a diagnostic program that resides in the terminal's firmware. The Self Test program systematically checks each major piece of circuitry in the terminal and reports any problems, via error messages, on either the display screen or the eight LED indicators. The SELF TEST switch is located next to the MASTER RESET button on the rear panel.

- Power connector. This connector accepts the female end of a standard 110 V/220 V AC, 60 Hz power cord.

- Line voltage selector switches. These switches select between 110 V and 220 V AC power.

- "To MODEM RS-232" connector. Standard connection via modem or RS-232 line to the host computer.

Your 4112 may also contain connectors associated with certain options. These are described in Section 2, *Operating Information*.

BELL INDICATOR

The terminal is equipped with a bell that ser. , several purposes. It rings upon host command, thus alerting you to a screen message from the host, etc. The Power-Up and Self-Test routines also use the bell to communicate information as follows:

- Power-Up Test. The bell rings once if a major malfunction is detected when the 4112 is turned on. For example, an optional ROM that is out of position will fail the Power-Up test. This causes the bell to ring once (also, an error message is printed on the screen).

  A "fatal error" causes the bell to ring three times. (Also, a coded error message appears on blinking keyboard lights.) Such a fatal error might be a bad RAM on the RAM/ROM board.

- Self-Test. The bell rings once during the key check. This requests the operator:

  — To type a character (to continue Self-Test), or
  — To press the CTRL (control) and C keys, which call the adjustment routine.

If the bell rings twice, press the RETURN key for additional error-reporting information.

If the bell rings three times, this indicates a fatal error.

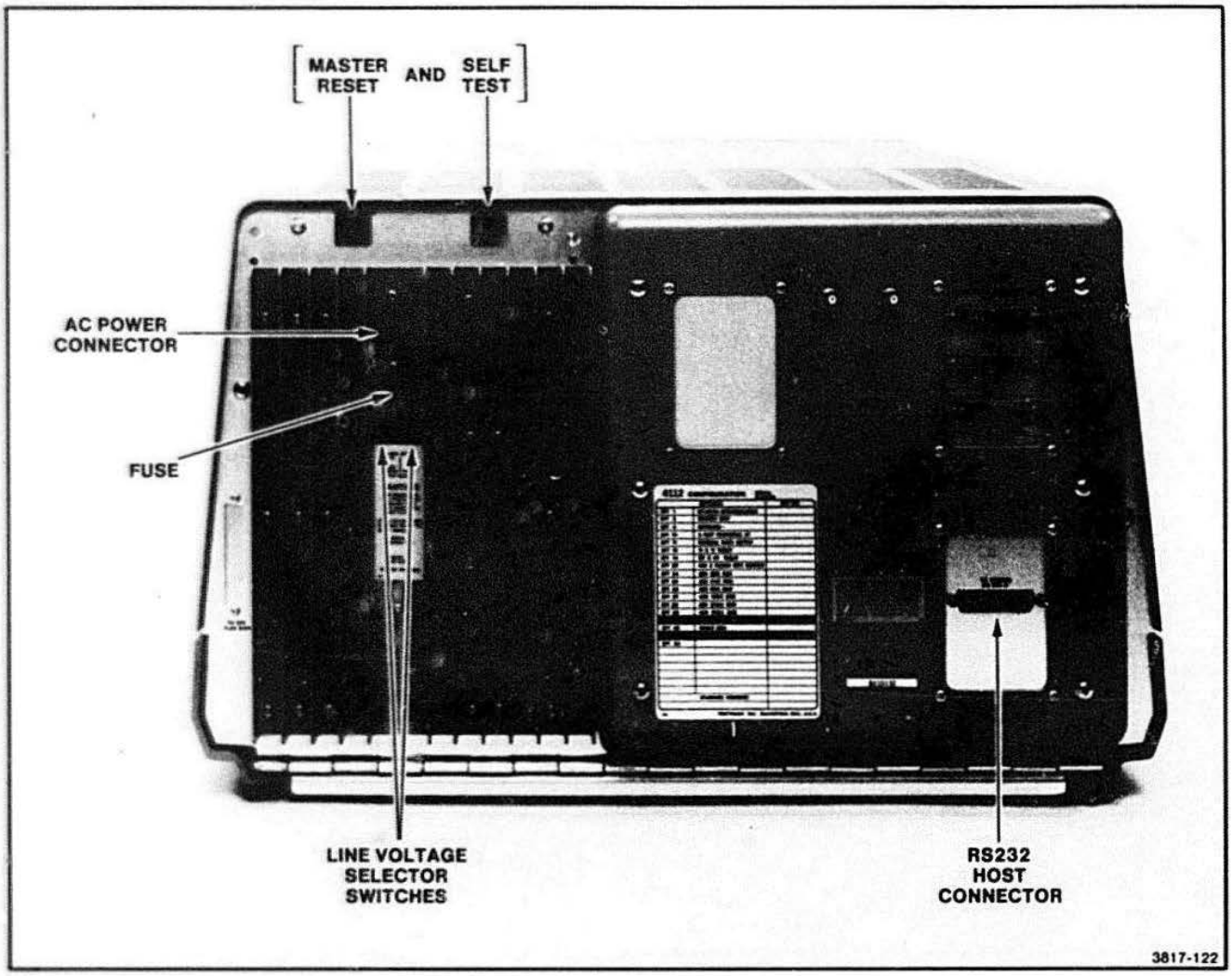


Figure 1-4. Rear-Panel Features.

ERROR MESSAGES

The 4112 has the following error detecting and reporting systems:

1. The 4112 performs a general set of hardware tests automatically each time the terminal is turned on. This series of tests is called the Power-Up Test.

2. A Self-Test sequence (also in firmware) runs a comprehensive test of all the hardware in the terminal. The Self-Test routine is manually started via buttons on the back of the terminal. Self-Test and its error messages are explained in Section 10 (*Troubleshooting and Self-Test*) of this volume, and in Section 5 of Volume 2.

3. Sections of the system firmware are designed to report any problem encountered during ordinary use of the terminal. If the user makes an operating error, or if an operation uncovers a hardware malfunction, an error message is printed on the screen. This third group of system-level error messages is described fully in Appendix C, *Error Codes*, in the *4110 Series Command Reference Manual*.

OPTIONS

Table 1-1 lists the 4112 options in numerical order. Option numbers beginning with an alpha designation are grouped at the end of the table.

Table 1-1

4112 OPTIONS

Option #	Description
Option 01	Extended Communications (includes half-duplex, block mode, and downloader).
Option 02	Current Loop Interface. (See the *Option 02 Current Loop Interface Service Manual* for detailed hardware information.)
Option 4A	United Kingdom Keyboard.[a]
Option 4C	Swedish Keyboard.[a]
Option 4E	APL Keyboard.[a]
Option 4F	Danish and Norwegian Keyboard.[a]
Option 10	Three Port Peripheral Interface (3PPI). This option supports peripherals such as: • 4662 and 4663 Plotters, • 4641 and 4642 Printers, • and other RS-232 devices such as the 4923 Tape Recorder (with Option 01 installed). See the 3PPI service manual for details.
Option 13	Graphic Tablet. Size: 11 x 11-inch. Option hardware includes: graphic tablet (and pen), 4110 Series Tablet Controller board, and Tablet Interconnect board (housed in a separate enclosure). (See the service manual for Options 13/14.)
Option 14	Graphic Tablet. Size: 30 x 40-inch. Option hardware includes: graphic tablet (and pen), 4110 Series Tablet Controller board, and Tablet Interconnect board (housed in separate enclosure). (See the service manual for Options 13/14.)
Option 24	One RAM Controller Board. Includes 32K bytes of RAM on one RAM Array board. (Service information is in this manual.)
Option 25	One RAM Controller Board. Includes 64K bytes of RAM on two RAM Array boards. (Service information is in this manual.)
Option 26	One RAM Controller Board. Includes 96K bytes of RAM on three RAM Array boards. (Service information is in this manual.)
Option 27	One RAM Controller Board. Includes 128K bytes of RAM on four RAM Array boards. (Service information is in this manual.)
Option 28	Two RAM Controller Boards. Includes 256K bytes of RAM on eight RAM Array boards. (Service information is in this manual.)
Option 29	Four RAM Controller Boards. Includes 512K bytes of RAM on sixteen RAM Array boards. (Service information is in this manual.)
Option 42	Single Flexible Disk Drive, and one Disk Controller Board. (Service information is included in the *4110 Series F42/43 Disk Options Service Manual* and the *119-0977-01/03 Flexible Disk Drive Instruction Manual*.)
Option 52	Customer-specified line voltage and frequency option.[b]
Option A1	Universal European line voltage and frequency: 220 Volt, 50 Hz.[b]
Option A2	United Kingdom line voltage and frequency: 240 Volt, 50 Hz.[b]
Option A3	Australian line voltage and frequency: 240 Volt, 50 Hz.[b]
Option A4	North American line voltage and frequency: 240 Volt, 60 Hz.[b]

[a] **Hardware is identical to standard keyboard, except for different keyboard ROMs and keycaps (labels).**

[b] **See *Replaceable Mechanical Parts* (Volume 2) for illustrations of the plugs/connectors that correspond to each of these power options.**

ACCESSORIES

These accessories are also listed in the mechanical parts list in Volume 2, where part numbers are given for each item. Standard accessories are supplied with each 4112, and optional accessories may be ordered separately, and in addition to, standard accessories.

STANDARD ACCESSORIES

- *4112 Introduction Brochure*
- *4112 Computer Display Terminal Operator's Manual*
- Power cord set
- Host port RS-232 cable
- Eight relegendable keycaps
- Six function key overlays

OPTIONAL ACCESSORIES

- Logic extender board
- Relegendable keycaps
- Function key overlays
- *4112 Host Programmer's Reference Manual*
- *4110 Series Command Reference Manual*
- *4112 Computer Display Terminal Service Manual*, Volume 1
- *4112 Computer Display Terminal Service Manual*, Volume 2
- *620-0295-00 Low Voltage Power Supply Service Manual*
- *4110 Series Option 10 (Three Port Peripheral Interface) Service Manual*
- *4110 Series Option 13/14 (Graphics Tablet) Service Manual*
- *4110 Series Option 42/43 (Flexible Disk Drives) Service Manual*
- *119-0977-01/03 Flexible Disk Drive Instruction Manual*
- Package of ten diskettes
- Loop-back connector for host-port test

Section 2

OPERATING INFORMATION

Section 2 includes a concise summary of operating information that will quickly familiarize you with the 4112's operation; for more detailed operating instructions, refer to the *4112 Operator's Manual*. Understanding the 4112's operation allows you:

- To recognize that a reported problem is actually a lack of understanding on the part of the operator.
- To use the terminal after completing repairs and adjustments to verify that it is operating properly.

This section first reviews the 4112's controls, indicators, and connectors; then it describes each of the major types of operations and commands, giving examples for each category.

CONTROLS AND INDICATORS

The 4112 has the following operator controls (see Figure 2-1):

- POWER switch. Located on the front of the 4112 by the lower left-hand corner of the screen.[1] To turn on power to the terminal, push in the switch and release. You will hear a click and a green indicator appears in the switch.
- Disk drive UNIT BUSY indicator. The disk drive unit is positioned vertically on the right side of the screen. The "unit busy" light, an LED in the center of the drive unit door, is on whenever the unit is energized. Push the button on the drive door to open it; this provides access for inserting or removing the diskette (also called "disk").

CAUTION

Do NOT attempt to remove or insert a disk while the unit busy light is on. To do so may cause:

- *Irreparable damage to the read/write head*
- *Irreparable damage to the disk*
- *Loss of the program on the disk*
- *Or all three*

- WRITE-PROTECT switch. A rocker switch above the disk drive unit, next to the write-protect LED indicator and the REFRESH INTENSITY knob. The write-protect LED indicator is on when write-protect is enabled.
- REFRESH INTENSITY knob. A potentiometer located near the upper-right corner of the display and next to the write-protect indicator. Turning it CW (clockwise) increases the screen image intensity, and turning it CCW decreases the intensity.

[1] "Screen" refers to the display crt.

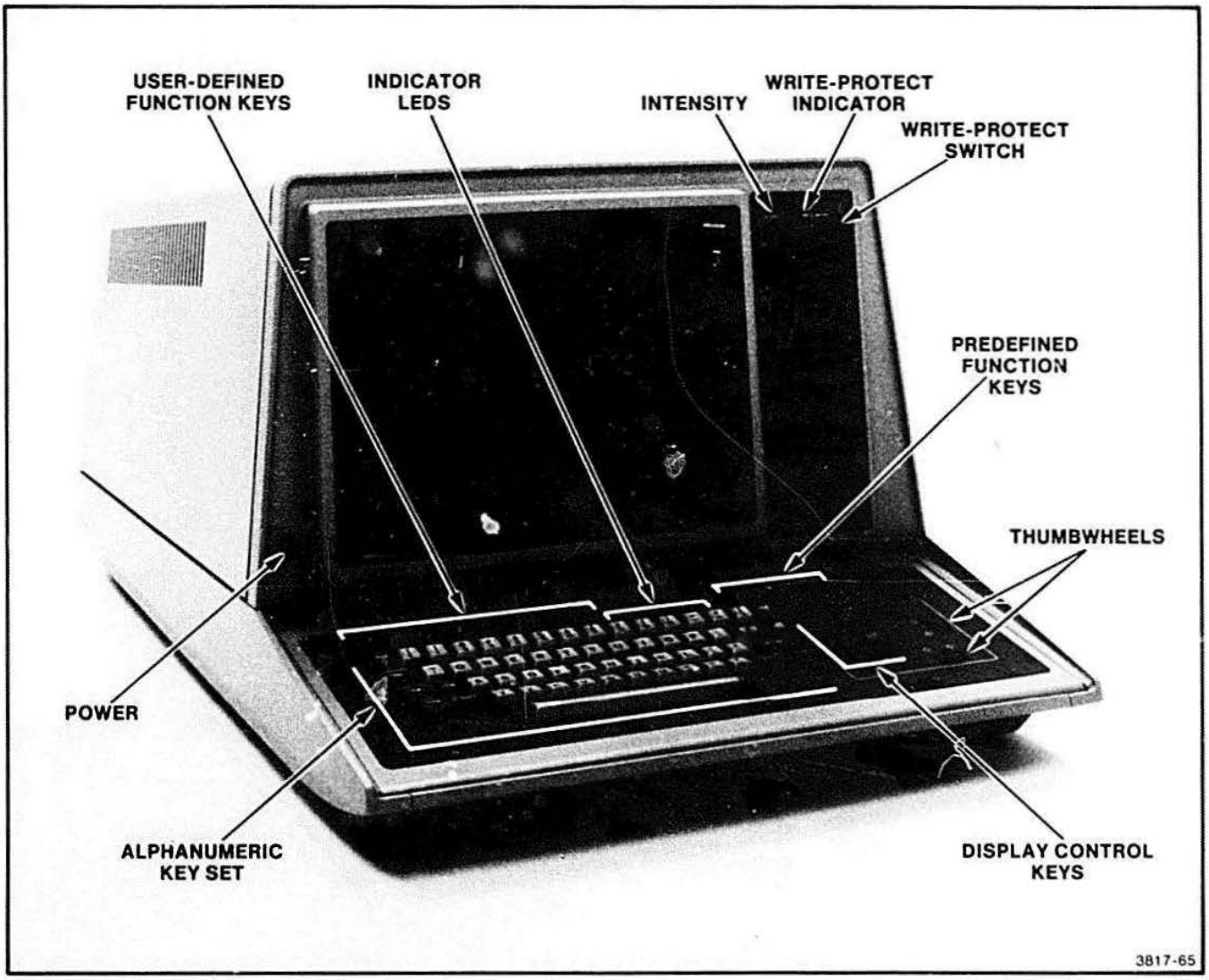


Figure 2-1. Controls, Indicators, and Keys.

INDICATOR LIGHTS

The keyboard contains four LED indicator lights and six keys with indicator lights. The locations of these indicators are shown in Figure 2-2. The four lights are:

- The KYBD LOCK indicator light is on when the terminal's keyboard is locked; this keeps you from entering any data from the keyboard.
- The PAGE FULL indicator light is on when the screen is filled with alphanumeric data.
- The XMT light is on when the terminal is transmitting data to the host.
- The RCV light is on when the terminal is receiving data from the host.

The DIALOG, SET UP, LOCAL, HARD COPY, NORMAL/ ZOOM, and CAPS LOCK keys contain lights. Each key light is lit when the function that the key controls is active. These keys are described in greater detail in the following text.

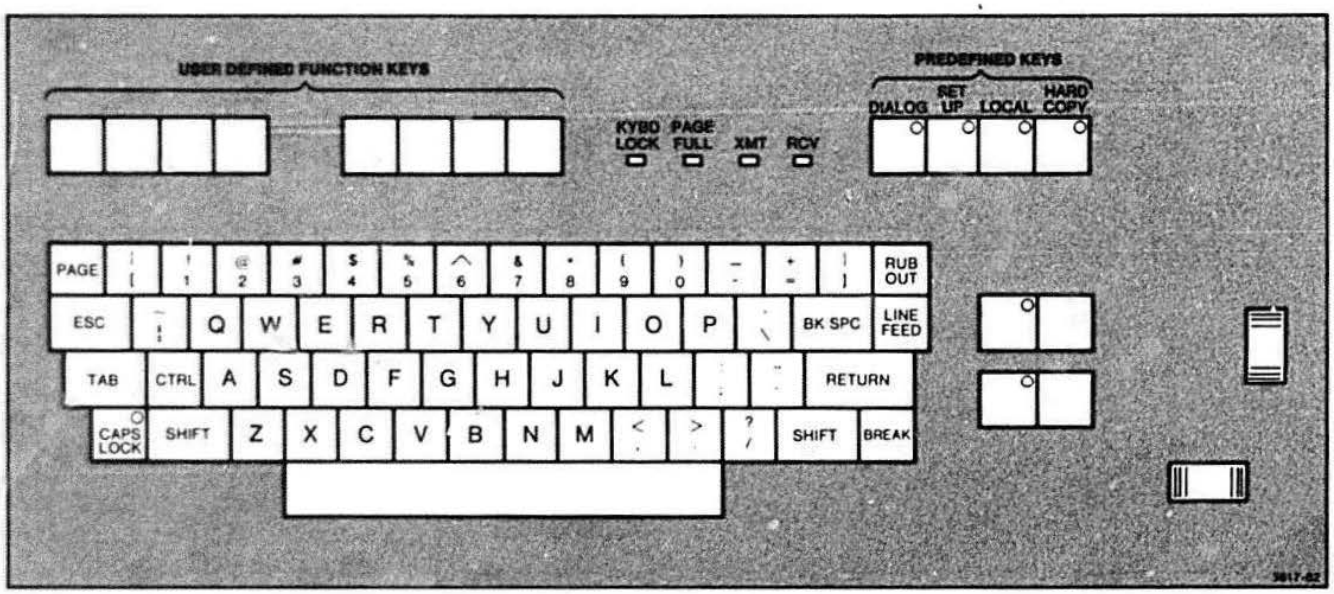


Figure 2-2. Keyboard Layout.

KEYBOARD

In addition to showing the 4112 controls and indicators, Figure 2-1 shows the locations of:

- The alphanumeric key set
- The user-defined function keys
- The predefined function keys
- The display control keys
- The thumbwheels

Most of the keys on the keyboard are the same as a typewriter; Figure 2-2 shows the alphanumeric key set. The operator programs the user-defined keys to perform certain functions, while other keys (the predefined function keys) have default functions upon power-up.

The predefined keys have the following functions:

- DIALOG/CLEAR. DIALOG causes the dialog area to be displayed. It is in use when the LED on the key is lit. CLEAR is the shifted function of the DIALOG key. It erases the dialog area.
- SET UP. Pressing this key places the terminal in "Setup mode." In Setup mode the terminal can perform many functions locally by executing "setup" and "escape sequence" commands. Setup mode has priority over local mode. The LED is lit when in Setup mode. For more detailed information see *Setup Mode* and Table 2-1.
- LOCAL/CANCEL. LOCAL places the terminal under local control. When Local mode is selected, the host has no effect and local echo is employed. CANCEL is the shifted version of the local key. It cancels anything that the terminal is presently doing except for spooling. The LED is lit while in Cancel mode.
- HARD COPY. When you press this key, the contents of the screen are sent to a hard copy unit if one is connected. Pressing SHIFT and HARD COPY simultaneously gives a "reverse video" of the display (see Figure 2-3).
- CAPS LOCK. Caps lock causes alphabetic characters to be uppercase, but does not affect numeric or special symbol keys.

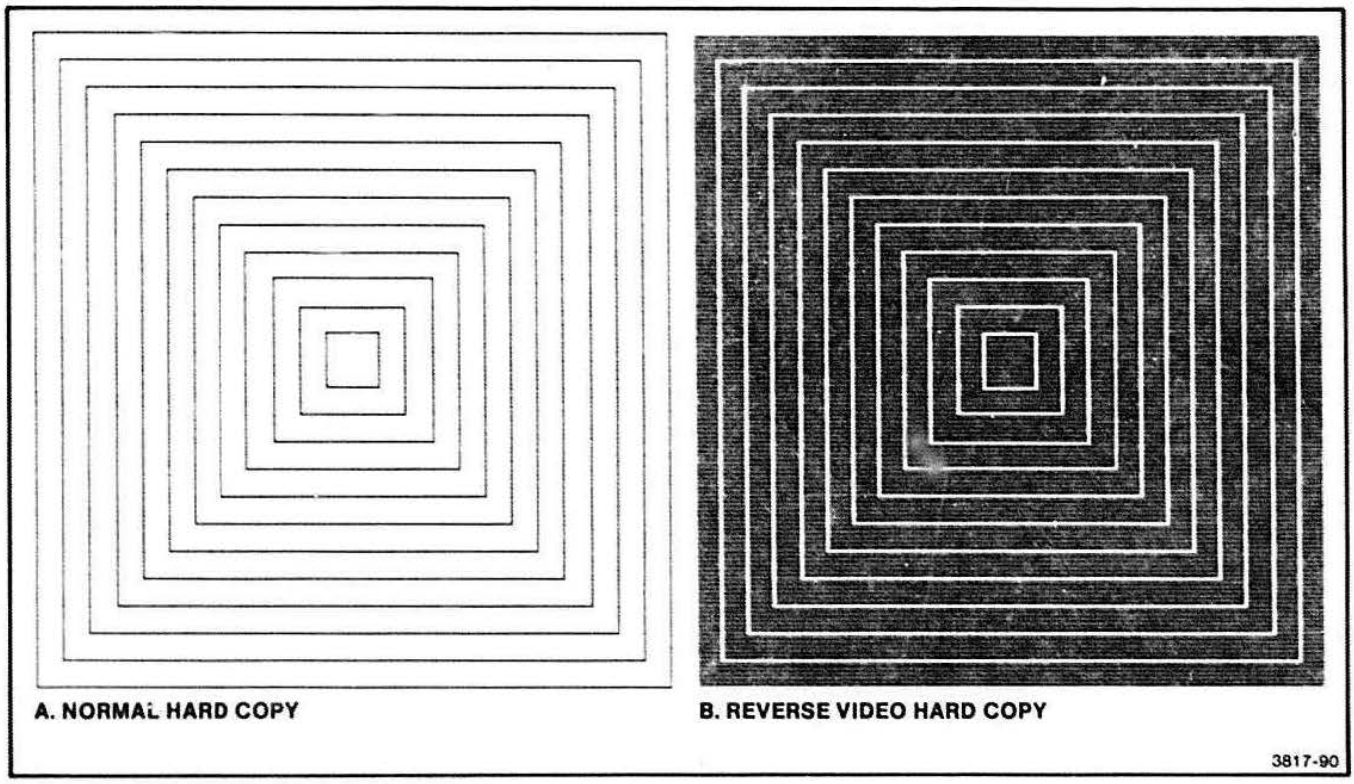


Figure 2-3. Samples of Hard Copy.

DISPLAY CONTROL KEYS AND THE THUMBWHEELS

The four keys adjacent to the thumbwheels, Figure 2-4, are the display control keys, and, with the thumbwheels, are used to manipulate graphic segments. The following list describes these keys and the thumbwheels (more detailed explanations are given in the operator's manual).

- ZOOM/NORMAL. ZOOM allows you to focus on a particular area of the total image. NORMAL, which is the shifted version of this key, restores the normal aspect ratio; this corrects distortion caused by zooming and panning operations. To change the aspect ratio, press ZOOM and CTRL while moving the thumbwheels.

- PAN/OVERVIEW. Panning permits changing the point of view. OVERVIEW, the shifted version of PAN, permits viewing the entire image. A "framing box" shows the area being panned or zoomed.

- NEXT VIEW/BORDER. NEXT VIEW activates the viewport. If more than one viewport is enabled, NEXT VIEW looks at the next viewport. Simultaneously pressing CTRL and NEXT VIEW causes the previous viewport to be displayed. BORDER (shifted NEXT VIEW) causes a border to appear or to disappear around the current viewport.

- VIEW/RESTORE. VIEW updates the view to what is in the current framing box. RESTORE (shifted VIEW) restores the original view of the current viewport.

- THUMBWHEELS. Either vertical or horizontal thumbwheels are used to move a cursor or to change dimensions of a framing box.

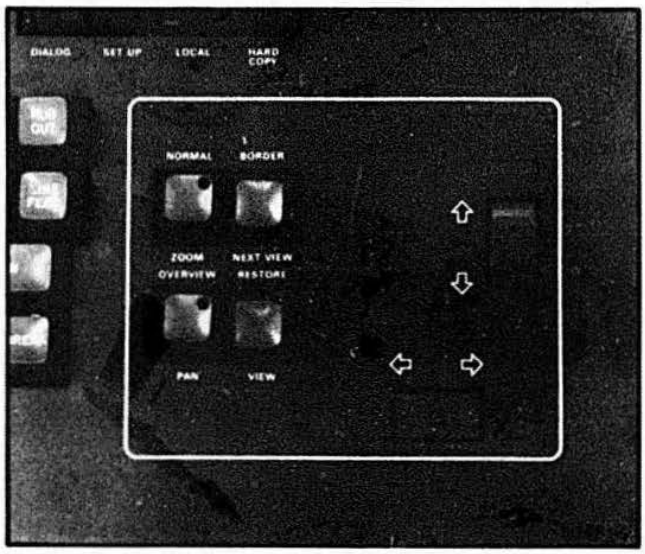


Figure 2-4. Display Control Keys and Thumbwheels.

REAR-PANEL CONTROLS AND CONNECTORS

These controls are on the rear panel of the terminal (see Figure 2-5):

- MASTER RESET switch. This control resets the terminal's user-definable operating parameters and thus returns the terminal to a known state. This pushbutton is mounted on the rear panel above the power-supply cooling fins.
- SELF TEST switch. This pushbutton, when pressed with the MASTER RESET button, runs the diagnostic Self-Test program that resides in the terminal's firmware. The Self-Test program systematically exercises each major piece of circuitry in the terminal and reports any problems via error messages on either the display screen or the keyboard indicator LEDs. This switch is located next to the MASTER RESET button on the rear panel.
- AC Power connector. This connector accepts the female end of a standard 110 V/220 V AC, 60 Hz power cord.
- Line voltage selector switches. These switches select between 110 V and 220 V AC power.
- To MODEM RS-232 (connector). This connector provides a standard connection via modem or RS-232 line to a host computer.
- To HARD COPY (connector). This connector accepts a cable from Tektronix hard copy units.
- To GRAPHIC TABLET (connector). This connector accepts a cable to Tektronix graphic tablets. The 4112 must have Option 13/14 installed to connect it to a graphic tablet.
- VIDEO OUT. This connector supplies a video signal to an external monitor.
- EXT SYNC. This connector supplies sync pulses to an external monitor.
- 3PPI interface. These three connectors provide signals to peripherals.
- Fuse. The fuse is a 6.25A SB, size 3AG, located on the back of the terminal on the power supply heatsink (for 110V AC operation).

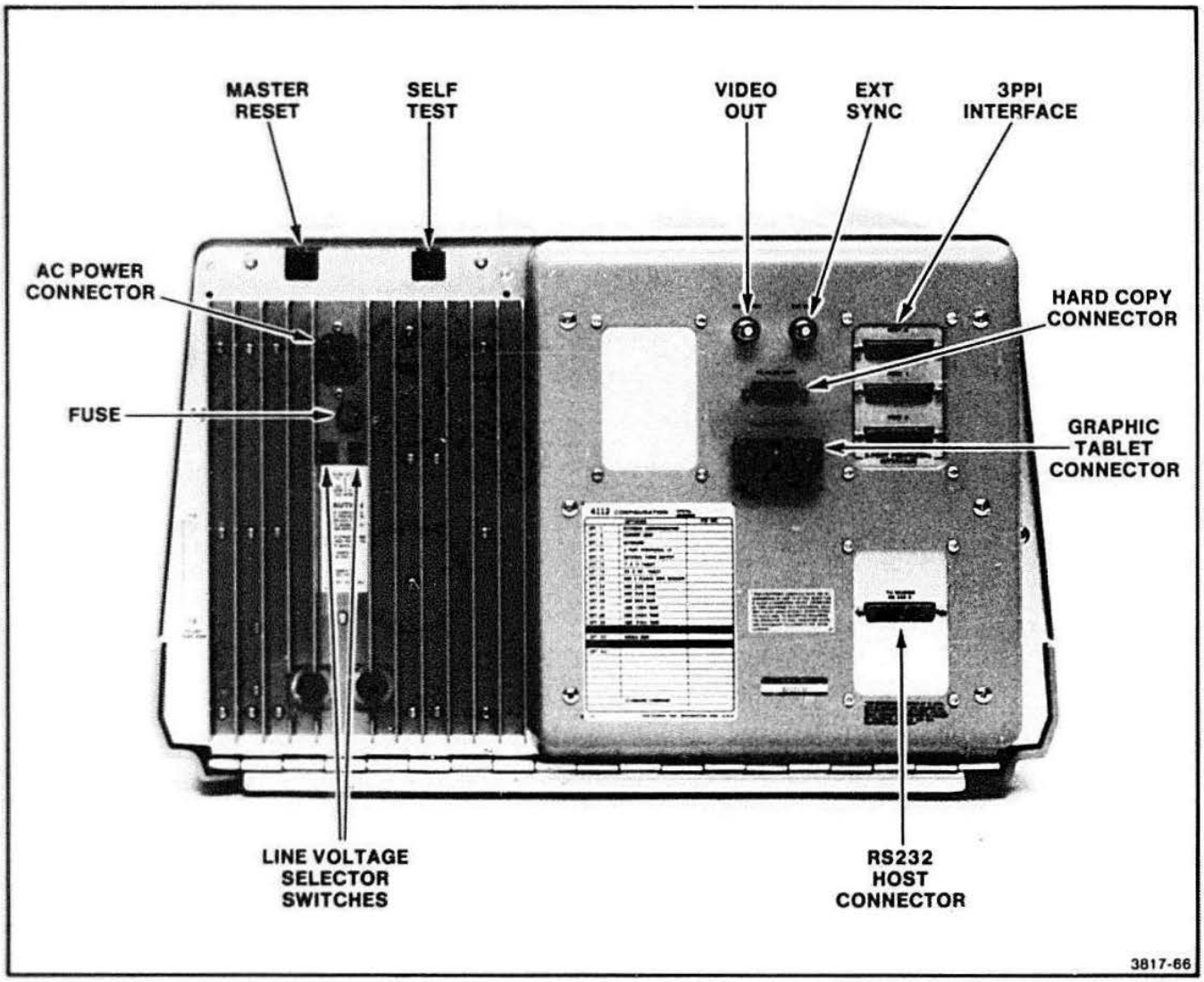


Figure 2-5. Rear View Showing the Fuse, Controls, and Connectors.

OPERATING CHECK

The following information is intended to give the service technician a quick hands-on check of basic terminal operation. This is not a detailed operational analysis; instead, this check allows you to use the terminal briefly in its fundamental modes. This information will familiarize new technicians with the 4112 and provide a refresher for persons who have worked with the 4112 before. The introduction brochure, *Introducing Your 4112 Computer Display Terminal*, provides similar procedures that may also be helpful when operating the 4112 terminal.

The following pages contain a tutorial exercise based on several examples. Each example is shown in a table. The tables may be read or may be followed step-by-step.

A host program normally controls the 4112. The operator's task is to set up the terminal for use, and to respond to the directions given by the host-resident program.

The examples in Tables 2-1 through 2-4 illustrate these tasks that are likely to be performed by an operator:

- Getting ready and turning on the 4112
- Creating a segment
- Manipulating a graphics segment
- Using GIN (Graphics Input) mode

The examples in Tables 2-1 through 2-4 require the use of Setup commands with the terminal in Setup mode. The following pages provide background information so you can easily use these commands.

SETUP MODE

English-like commands (called "Setup commands") can be executed to define the terminal's operating environment when the terminal is in Setup mode.

Setup mode suspends communications to the terminal's host computer. The host is unaware of this and may send messages to the 4112. These messages are stored in the terminal's memory and are displayed upon leaving Setup mode.

If you make a programming mistake while in Setup mode, the terminal displays an error message immediately below the incorrect command. In most cases these messages are self-explanatory. The *4110 Command Reference Manual* lists Setup mode error messages and their meanings.

SETUP COMMANDS

Setup commands are used primarily by an operator, but knowledge of these commands may also be useful to the service technician. Setup mode allows execution of the 4112 commands for which there are no English-like commands. These commands are called "escape sequences" because the first character in each of these commands is the "Escape" character. Escape is also sometimes called ALT mode, depicted by a $, or by some other convention. For the purposes of this manual, Escape is indicated by (ESC), which means you should press the ESC key. These commands are terminated by pressing the RETURN key, depicted in each command line by (RETURN).

Table 2-1 uses one escape sequence command and Tables 2-2 through 2-4 illustrate the use of other escape sequence commands. See the *4112 Operator's Manual* for a complete description of Setup commands.

USING THE STATUS MESSAGE

The terminal displays a status report that contains such things as:

- Communications conditions
- The size and position of the dialog area
- The kinds of errors the terminal displays
- Control of peripherals, etc.

The terminal remembers the new values for status as you enter them. The 4112 retains these values after it is turned off. The word in the left column of the status report is the name of the command. The right column lists the current parameter of the command. Only those commands that have parameters are remembered when the terminal is turned off. These are stored in battery-powered RAM (CMOS) and may be listed when the 4112 is turned on again. Table 2-1 contains examples of the status report.

CONVENTIONS

The following conventions are used in the tables:

- The terminal is installed and ready for operation. (See Section 2 in Volume 2 for installation procedures.)
- Setup commands in the examples are shown in UPPERCASE. Any English-like Setup command can be entered in either upper or lower case. If you want to enter all uppercase characters as shown, press the CAPS LOCK key. An "escape sequence" entered in Setup mode must be all uppercase.
- (ESC) means press the ESCAPE key.
- Individual keys are enclosed in parentheses: (E)(X)(A)(M)(P)(L)(E).
- Text strings are enclosed by angle brackets: <Example>.
- The space character is a field separator and must be included as shown in the examples.
- The commands are initiated (and executed) by pressing the RETURN key. (RETURN) means press the RETURN key.

NOTE

If you have any problems working through the examples, refer to the corresponding information in the 4112 Operator's Manual. The operator's manual contains similar examples and provides more detailed background and helpful information.

4112 STARTUP

Table 2-1 contains the 4112 startup procedure; do this example first. The startup procedure sets up the terminal so the other examples will work as specified. The examples in Table 2-2 must be done before the examples in Tables 2-3 and 2-4.

Before attempting to isolate a fault, reset the terminal to its default status. This will eliminate any fault caused by improperly programming the 4112. Appendix E provides a procedure for returning the terminal to the factory default status.

This section does not explain the commands used in Table 2-1 in detail. For more information on these commands, see the *4112 Operator's Manual* or the *4110 Series Command Reference Manual*.

The terminal tests certain parts of its memory and circuitry every time it is turned on. On a properly functioning terminal:

- The four indicator lights and the lights in other keys all turn on.
- The light in the CAPS LOCK key blinks and then stays off.
- All lights turn off.

NOTE

If the DIALOG key was on when the the terminal was last used, the Dialog light will remain on. Press the DIALOG key once to turn it off.

- The XMT and RCV indicator lights flash once each.
- The cursor appears in the upper left corner of the screen, and the terminal is then ready for operation.

If the test fails, the terminal bell may ring and some of the lights may remain on. If this happens, see Section 10 (*Troubleshooting and Self-Test*), or the *4112 Operator's Manual* for details.

Table 2-1

GETTING READY AND TURNING ON THE 4112

Step	Comment
1. Press the power button. If the terminal is on, skip to Step 2. The POWER button is shown in Figure 2-1.	When you release the POWER button the green indicator appears. You can hear the terminal's ventilation fans start up. If some of the indicator lights remain on and the terminal bell rings, it has failed the Power-Up test sequence. See Section 10, *Troubleshooting and Self-Test*, for details.
2. If the terminal is already on, press the RESET button.	This resets the terminal to its power-up default status.
3. Press the LOCAL key (Figure 2-2).	The red light in the key turns on and the terminal enters Local mode.
4. Press the following keys: (ESC) (8) (RETURN)	This command sets text size of the terminal. If the text was already set to this size, there is no change. The size of the cursor changes to reflect the new text size.
5. Press the LOCAL key.	The light in the key turns off and the terminal exits from Local mode.
6. Press the key labeled SET UP (Figure 2-2).	The red light in the key turns on.
7. Enter the following command: DAENABLE NO	This command causes the terminal to turn the dialog area off.
8. Enter the following command: PAGEFULL STOP	This command causes the terminal not to take any special action when the screen is filled with text. Other commands for Pagefull are: NONE, BREAK, and AUTOCOPY.
9. Enter the following command: STATUS	A report of the status of the terminal is displayed. Not all of the report is displayed at once.
10. Press RETURN (or any key except SHIFT).	This displays the remainder of the report on the screen. The PAGEFULL light comes on.
11. Press any key (except SHIFT) again, and press PAGE key.	This clears the PAGEFULL light and erases the screen (returning the cursor to the upper left corner).
12. Enter the following command: STATUS COMMUNICATIONS	This displays a report of only the current 4112 communications parameters.
13. Press the PAGE key.	The screen is erased.
14. Press the SET UP key.	The terminal exits from Setup mode. The red light in the key turns off.

CREATING A GRAPHICS SEGMENT

A graphics segment is a picture, or a part of a picture, that can be manipulated by 4112 commands. By manipulating a segment, you can manipulate all or part of a picture without continually compiling and executing an entire program.

A software program usually creates a segment. Table 2-2 is an example of how a graphics segment may be created at the terminal instead. The example tells you to call a host program that uses segments. Then, after creating a segment in Local mode, you send this to the host to become part of the picture in your graphics program.

NOTE

This graphics program should not include text. If no non-text program is available, refer to the 4112 Operator's Manual; it tells how to use the dialog area to display such text.

The example in Table 2-2 also illustrates the use of "escape sequence" commands with the 4112 in Setup mode. Refer to the previous subsection, *Conventions*.

At the end of Table 2-2, the segment remains on the screen. The same segment is used in the examples of Tables 2-3 and 2-4. The segment is deleted from the terminal's memory at the end of the example in Table 2-4.

Table 2-2
CREATING A SEGMENT

Step	Comment
1. If the DIALOG light is on, press the key; this turns the light off.	The light in the key turns off. If the dialog area is enabled, the cursor disappears.
2. Press the SET UP key.	The lights in both the SET UP and DIALOG keys turn on if the dialog area is enabled. If the dialog area is not enabled, do Step 3a and continue; otherwise, skip to Step 4.
3a. Enter the following command: DAENABLE YES	This command enables the dialog area, causing subsequent dialog to appear in it. When you press RETURN, the cursor disappears; this is because the cursor is now in the dialog area, even though the dialog area is not yet visible.
b. Clear the dialog area if necessary (press CLEAR key).[a]	If there was any text in the dialog area it is erased, and the dialog area is placed on the display screen.
4. Press the SET UP key again.	The light in the SET UP key turns off (the light in the DIALOG key stays lit only if Step 3a was done). The terminal exits from Setup mode.
5. If Step 3 was omitted, press the DIALOG key.	The light in the key turns on and the dialog area becomes visible.
6. Log on the host computer.	
7. Press the SET UP and the CAPS LOCK key.	The lights in the SET UP and DIALOG keys are now both on, the CAPS LOCK light is on, and the terminal enters Setup mode.
8. Enter the following command:[b] (ESC) < SO 1> (RETURN)	The terminal "opens" segment one. This means that subsequent graphics data is captured into segment 1.
9. Press the SET UP key.	The terminal exits from Setup mode and is now able to communicate with the host computer. The light in the SET UP key turns off. The light in the DIALOG key remains lit because the key was explicitly pressed in Step 3 or in Step 5.
10. Enter the necessary commands to run a graphics program on the host.	As the picture is displayed, it is captured in segment 1.
11. When the program is finished running, press the SET UP key.	The light in the SET UP key turns on and the terminal enters Setup mode.
12. Enter the following command:[b] (ESC) < SC> (RETURN)	The terminal "closes" the open segment. Incoming data is no longer captured.
13. Press the SET UP key.	The light in the SET UP key key turns off.
15. Log off the host computer.	
16. Clear the dialog area (CLEAR key) and press the DIALOG key.	The dialog area is erased and the DIALOG light turns off.
17. Press the PAGE key.	Graphics that are not part of a segment are erased. The segment is erased momentarily and redrawn.

[a] CLEAR key is the shifted version of the DIALOG key.

[b] Use UPPERCASE for all escape sequence commands.

MANIPULATING A GRAPHICS SEGMENT

Table 2-2 illustrates how to create a graphics segment. Table 2-3 goes a little further by showing some of the ways to manipulate a segment.

Table 2-3 assumes that the segment created by Table 2-2 is still on the screen. Table 2-3 illustrates the use of the viewing keys, except for RESTORE and NEXT VIEW, and escape sequence commands that make the segment:

- Invisible
- Visible
- Appear in refresh
- Appear in storage
- Highlighted
- Unhighlighted

The escape sequence command format is described prior to Table 2-2.

The manipulation of a segment is normally accomplished under program control. The simple examples in Table 2-3 illustrate just a few of the ways a segment can be used. See the *4112 Host Programmer's Manual* and the *4110 Command Reference Manual* for details.

Table 2-3

MANIPULATING A GRAPHICS SEGMENT

Step	Comment
1. If the DIALOG light is on, press the DIALOG key to turn the light off.	The light in the key turns off. If the dialog area is enabled, the cursor disappears.
2. Press the SET UP key.	If the dialog area is enabled, the lights in the SET UP and DIALOG keys both turn on. If the dialog area is not enabled, do Step 3 and continue; otherwise, skip to Step 4.
3. Enter the following command: DAENABLE YES	This command enables the dialog area, causing subsequent dialog to appear in it. When RETURN is pressed, the cursor disappears. This is because the cursor is now in the dialog area, even though the dialog area is not yet visible.
4. Enter the following command to make the segment invisible:[a] (ESC) < SV 1 0> (RETURN)	There is no immediate effect on the segment; the asterisk appears on the next line as a prompt. Erasing the screen causes the segment to disappear.
5. Enter the following command to make the segment visible again:[a] (ESC) < SV 1 1> (RETURN)	The segment becomes visible when RETURN is pressed.

[a]Use UPPERCASE for all escape sequence commands.

(continued)

Table 2-3 (cont)

MANIPULATING A GRAPHICS SEGMENT

Step	Comment
6. The following parts of this step exercise the viewing keys.	
a. Press the ZOOM key.	The light in the ZOOM key comes on as the terminal enters Zoom mode and the framing box becomes visible.
b. Rotate the thumbwheels. Make the framing box about half as large as the screen.	Observe the action of the framing box. Either thumbwheel has the same effect.
c. Press the PAN key.	The light in the ZOOM key turns off as the terminal exits Zoom mode and the crosshair cursor appears in the framing box.
d. Rotate the thumbwheels. Move the crosshair about halfway to the left of center on the screen.	Observe the action of the framing box as the thumbwheels are turned. The vertical thumbwheel moves the cursor up and down; the horizontal thumbwheel moves the cursor left and right.
e. Press the VIEW key.	The screen now shows only a part of the original picture. This is determined by the position of the framing box from the previous steps.
f. Enter Zoom mode and press CTRL while manipulating the thumbwheels.	Notice that the aspect ratio of the framing box changes in a horizontal and vertical direction as the respective thumbwheels are turned.
g. Press VIEW.	The distorted panned and zoomed portion of the picture in the framing box is displayed.
h. Press NORMAL (SHIFT-ZOOM).	The picture returns to the default aspect ratio (4:3).
i. Press OVERVIEW (SHIFT-PAN).	The original picture with the default aspect ratio and the framing box are displayed.
j. Press BORDER (SHIFT-NEXT VIEW). Pressing BORDER a second time erases the border.	A border is displayed around the graphics segment.
k. Continue to experiment with the controls using all modes of operation and the viewing keys until you are completely familiar with their function.	
7. Enter the following command to draw the segment in refresh:[a] (ESC) < SM 1 2> (RETURN)	The segment is erased and redrawn with no apparent change in the segment. The asterisk appears on the next line as a prompt.
8. Turn the REFRESH INTENSITY knob to the left.	The displayed segment dims as the knob is turned. If you turn the knob all the way to the left the segment disappears. If you turn it all the way to the right the segment becomes bright.
9. Enter the following command to draw the segment in storage:[a] (ESC) < SM 1 1> (RETURN)	The segment may appear somewhat brighter again.
10. Enter the following command to "highlight" the segment:[a] (ESC) < SH 1 1> (RETURN)	The segment "blinks" slowly. Turn the REFRESH INTENSITY knob to the right to make the blinking more noticeable.
11. Enter the following command to discontinue highlighting of the segment:[a] (ESC) < SH 1 0> (RETURN)	The segment stops blinking.
12. Press the SET UP key.	The light in the key turns off and the terminal exits from Setup mode.
13. Press the DIALOG key.	The dialog area becomes visible.

[a] Use UPPERCASE for all escape sequence commands.

GRAPHICS INPUT

Graphics input (GIN) mode allows graphics information to be sent to a program.

In a typical use of GIN mode, the operator logs on a host and executes a program. The program displays some graphics or text. It prompts for positioning of the graphics cursor to send data to the program or to indicate a choice of action. The program continues sending prompts until all of the necessary information has been sent; it then terminates GIN mode.

Table 2-4 illustrates the use of escape sequence commands to enter GIN mode and use some of its features.

The example in Table 2-4 assumes that a graphics segment is displayed (from Table 2-2 or 2-3).

Table 2-4

USING GIN (GRAPHICS INPUT) MODE

Step	Comment
1. If the DIALOG light is on, press the DIALOG key to turn the light off.	The light in the key turns off.
2. Press the PAGE key.	The screen is erased. The segment on the screen is redrawn.
3. Press the SET UP key.	If the dialog area is enabled, the lights in the SET UP and DIALOG keys both turn on. If the dialog area is not enabled, do Step 3 in Table 2-3 and then continue with Step 4 of this example.
4. Clear the dialog area (press CLEAR key).	If there is any text in the dialog area, it is erased.
5. Enter the following command:[a] (ESC) < IE 0 1> (RETURN)	The crosshair cursor becomes visible as the terminal enters GIN mode.
6. Press the SET UP key.	The light in the SET UP key turns off as the terminal exits from Setup mode.
7. Rotate each thumbwheel.	The horizontal line of the crosshair cursor moves up and down as the right thumbwheel is rotated. The vertical line of the crosshair moves left and right as the bottom thumbwheel is rotated.
8. Press an alphanumeric key.	In an actual GIN situation, this "locates" the point at which the crosshair cursor is positioned. The coordinates of that point are sent to the graphics program. In this case, the crosshair cursor disappears and the terminal exits from GIN mode because only one GIN event was asked for.
9. Press the SET UP key.	The red light in the key turns on and the terminal enters Setup mode.
10. Enter the following commands:[a] (ESC) < II 0 1> (RETURN) (ESC) < IR 0 1> (RETURN) (ESC) < IE 0 5> (RETURN)	The terminal enters GIN mode again, with "rubberbanding" and "inking" in effect. II is inking, IR is rubberbanding, and IE means enter GIN. The "0" means use the thumbwheels for the locator function, and the "5" means perform five GIN events.
11. Press the SET UP key.	The lights in the SET UP key turns off. The terminal exits from Setup mode.

[a]Use UPPERCASE for all escape sequence commands.

Table 2-4 (cont)

USING GIN (GRAPHICS INPUT) MODE

Step	Comment
12. Press an alphanumeric key.	The crosshair cursor blinks momentarily and then reappears.
13. Rotate the thumbwheels to move the crosshair cursor to another point.	Notice that a line follows the cursor as you move it. This is the "rubberbanding" feature.
14. Press an alphanumeric key.	A line is drawn from the last point located to the current point. This is the "inking" feature of GIN mode.
15. Continue to move the thumbwheels and press three more alphanumeric keys.	A line is drawn as you press each key. When the third key is pressed, the crosshair cursor disappears.
16. Press the PAGE key.	The screen is erased. The lines drawn while the inking feature was on are erased, since they are not part of a segment. Segment 1 is erased momentarily and redrawn.
17. Press the SET UP key.	The light in the SET UP key turns on.
18. Enter the following commands:[a] (ESC) < IC 0 1> (RETURN) (ESC) < IE 0 1> (RETURN)	The first command specifies that the next time the terminal enters GIN mode, segment 1 is to be the graphics cursor. The second command puts the terminal into GIN mode.
19. Press the SET UP key.	The light in the SET UP key turns off.
20. Rotate each of the thumbwheels.	Segment 1 is now the graphics cursor. Rotating the top thumbwheel moves the cursor left and right; rotating the bottom thumbwheel moves it up and down.
21. Press an alphanumeric key.	The terminal exits from GIN mode.
22. Press the SET UP key.	The light in the SET UP key turns on.
23. Enter the following command:[a] (ESC) < SK 1> (RETURN)	This command deletes segment 1 from the terminal's memory.
24. Press the SET UP key.	The light in the SET UP key turns off.
25. Press the DIALOG key.	The light in the DIALOG key turns off.

[a] **Use UPPERCASE for all escape sequence commands.**

Section 3

CHARACTERISTICS

This characteristic/specifications section lists two different types of specifications: those that are classified as environmental, physical, or "static" specifications (specifications that cannot be verified by a user); and those that can be verified as actual operational parameters of the 4112. The user-verifiable specifications can be verified through the 4112 adjustment procedures located in Section 9.(User-verifiable specifications are listed only in Tables 3-3 and 3-4.)

CHARACTERISTICS/SPECIFICATIONS

The remainder of this section summarizes characteristics and performance specifications of the 4112. In order for these specifications to be achieved and to ensure proper performance, the following conditions must be met:

1. The 4112 must be adjusted at an ambient temperature of 68 to 86° F (20 to 30° C).

2. The 4112 must be operating in an environment as specified in Section 2 (Volume 2), *Installation*.

3. A warm-up time of at least 20 minutes must precede operation.

4. The 4112 must meet specified power requirements. See Section 9, *Adjustment Procedures*, and refer to Table 3-3, under Power Supply Requirements. (The separate *620-0295-00 Low Voltage Power Supply Service Manual* lists its own set of characteristics.) The 4112 terminal is intended to be operated from a power source with its neutral line at or near ground potential. It is not intended for operation from two phases of a multiphase system.

The following tables contain specifications and characteristics for the 4112.

Table	Description
3-1	Physical Characteristics
3-2	Environmental Characteristics
3-3	Electrical Characteristics
3-4	Display Module Electrical Characteristics
3-5	Installation Requirements
3-6	Graphics Characteristics
3-7	Alphanumeric Characters

Table 3-1

PHYSICAL CHARACTERISTICS[a]

Characteristic	Specification
Weight	102 lbs (46.27 kg) with all options
Length	32.48 in (824.9 mm)
Width	21.50 in (546.1 mm)
Height	15.91 in (404.1 mm)
Display Area	See Table 3-4.

[a]See Figure 3-1.

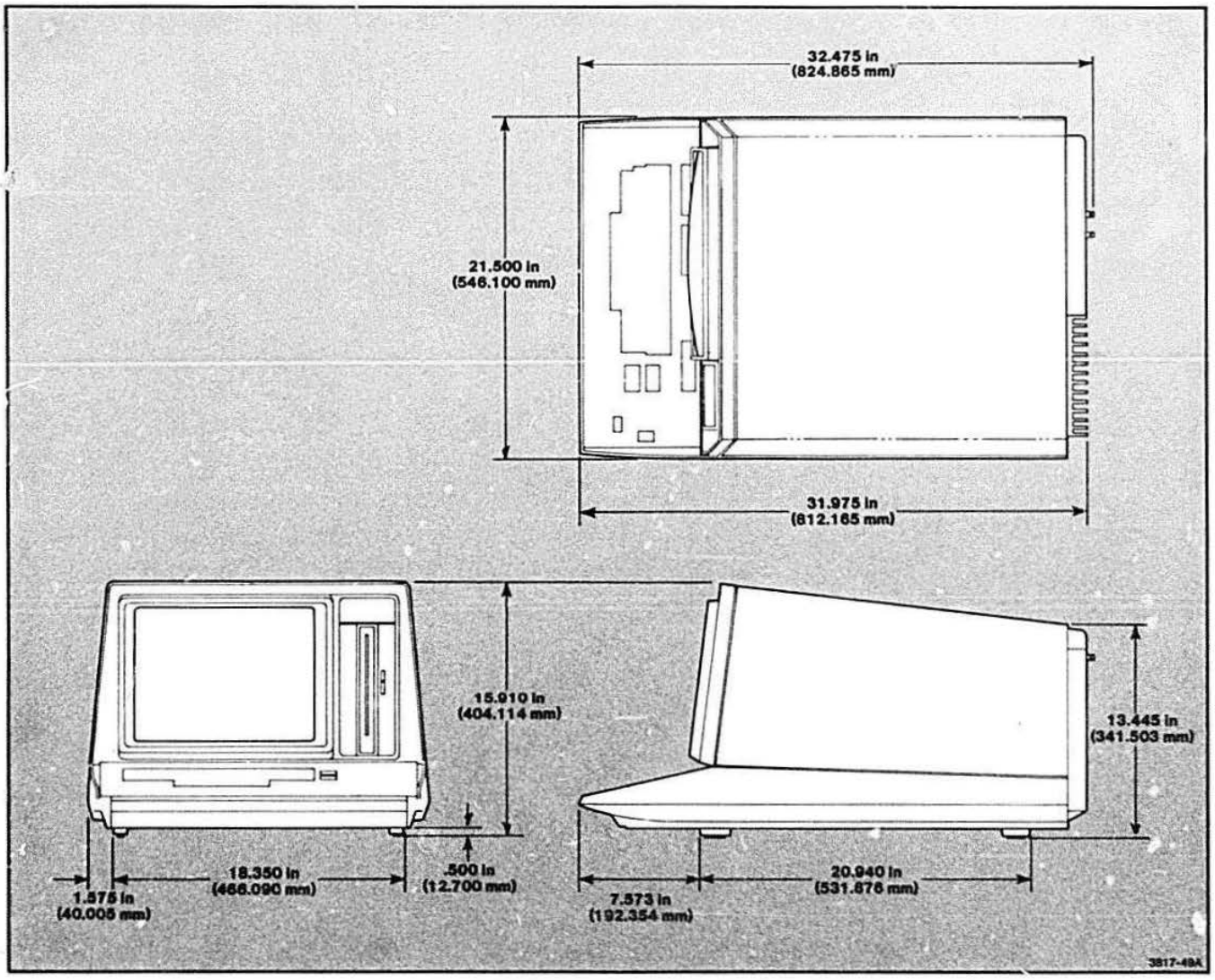


Figure 3-1. 4112 Physical Dimensions.

Table 3-2
ENVIRONMENTAL CHARACTERISTICS[a]

Characteristic	Specification
Temperature[a]	
Without Option 42	
Operating	32 to 104°F (0 to + 40°C)
Nonoperating	−67 to + 167°F (−55 to + 75°C)
With Option 42	
Operating	43 to 100°F (+ 10 to + 38°C)
Nonoperating	−40 to + 122°F (−40 to + 50°C)
Altitude[a]	
Operating	To 15,000 ft (4572 m)
Nonoperating	To 50,000 ft (15240 m)
Humidity	
Without Option 42	
Operating	70-75% maximum relative humidity
Nonoperating	90-95% maximum relative humidity
With Option 42	
Operating	20% to 80% noncondensing
Nonoperating	8% to 80% noncondensing

[a] Maximum operating temperature decreases 1°C for every 1,000 feet above 5,000 feet in altitude.

Table 3-3
ELECTRICAL CHARACTERISTICS[a]

Characteristic	Specification
Fuse	6.25 A medium (110V AC) 3.0 A fast (220V AC)
Low Voltage Power Supply Requirements	55 V DC ± 2%; 1.25 A max. Ripple at 60 Hz and 20 Hz is less than or equal to 50 mV.
High Voltage Power Supply[b] Requirements	16 kv ± 5% nominal value with ripple 40 V p-p or less.
Test Pattern	All white raster (not synchronized).[c]

[a] See Table 3-4, Display Module Characteristics, for additional electrical characteristics.

[b] The High Voltage Power Supply is part of the Display Module.

[c] Initiated by TTL Logic Low ("0") command.

Table 3-4

DISPLAY MODULE CHARACTERISTICS

Characteristic	Specification	Supplemental Information
Physical Characteristics		
Weight	17 pounds (7.65 kg)	
Length	13.49 in (342.6 mm)	
Width	11.87 in (301.5 mm)	
Height	10.76 in (273.3 mm)	
Display Area	10.5 in (266.7 mm) x 7.875 in (200.025 mm) nominal	
Electrical Characteristics		
VIDEO	High = 1.0 V max beam on	Connector Pin 2 of P586. 75 Ω nominal.
HORIZ SYNC	31.500 kHz, ±300 Hz, or 31.250 kHz, ±300 Hz	Connector Pin 7 of P586. TTL logic level.
VERT SYNC	57 Hz min to 63 Hz max for 60 Hz frame rate. 47 Hz min to 53 Hz max for 50 Hz frame rate.	Connector Pin 5 of P586. TTL Logic level.

Table 3-5

INSTALLATION REQUIREMENTS

Characteristic	Specification
Heat dissipation	1066 BTU/hr typical
Heat dissipation, with following circuitry installed: 1. Processor Board with 8 2732s 2. Flexible disk option. 3. 2 RAM controller boards each with 128K bytes of RAM 4. RAM/ROM board with 32K bytes of RAM and 16 2732s 5. External Video 6. Dual Raster Memory 7. 3PPI option 8. Tablet Interface option	1740 BTU/hr maximum allowable
Surge Current[a]	±25 A peak (typical) ±30 A peak (maximum)

[a] Surge current values are mainly determined by the power supply filter capacitors in the inverter.

Table 3-6

GRAPHICS CHARACTERISTICS

Characteristic	Description
Resolution	640 by 480 vertical resolvable dots
Addressability	4096 x 4096 points (in the 4112's world space coordinate system)
Zooming	An image filling a 4096 x 4096-point space can be condensed for viewing in 640 x 480 points by zooming out. Fine detail can be resolved by zooming into the area of interest; it is identified by panning a rectangle over the image and adjusting the rectangle's size. The zoom range is adjustable via 4112 commands. See the *4110 Series Command Reference Manual* for additional information.
Graphics Command Syntax	PLOT 10-compatible
Line Types	Solid, Dashed, Erase, XOR
Drawing Speed	9.6 K baud for moves and draws, from host communications line The Vector Generator draws vectors at a rate of 200 to 600 ns/pixel, depending on slope. This produces the following display drawing speeds. For short vectors: 2000 vectors/second from memory. For vectors longer than 1/2 inch: 3000 inches/second. (The last two values assume a 15-inch display size.)
Graphics Primitives	Vectors, Polygon, and Text
Graphics Options	Gray Scale: Eight shades from white to black. Up to three memory planes can be directly loaded through the I/O port and displayed as gray scale. Overlays

Table 3-7

ALPHANUMERIC CHARACTER SETS

Character Set	Description
Standard Character Set	Full ASCII character set 95 displayable characters (counting "space" as a displayable character) In "Snoopy mode" all 128 characters are displayable.
Optional Character Sets	United Kingdom (Option 4A) Swedish (Option 4C) APL (Option 4E) Danish/Norwegian (Option 4F)
Character Format	80 columns, 34 rows 7 x 9 dot matrix in an 8 x 14 area

Section 4

THEORY OVERVIEW

This section introduces the theory of operation. Because the 4112's theory of operation is modular, the theory discussion is divided into four logical groupings. These groups correspond to divisions in the terminal's architecture:

- Processor Bus and keyboard theory
- Display Bus theory
- Display Module theory
- Low Voltage Power Supply theory (contained in separate manual)

Each grouping is covered in a separate section, thus keeping the theory discussion from being one large and unwieldy section. This makes it easier to find and retrieve the desired information.

This section contains introductory theory and comments that pertain to the remaining theory sections.

This section first reviews terminology used in this manual and display concepts that describe the general operating nature of this raster-scan terminal. Next, this section gives an overview of the operating theory of the terminal; this overview includes very general and macroscopic views of the various 4112 circuit modules and boards.

DEFINING TERMS

Before reading detailed circuit descriptions you should be familiar with the terminology used to describe graphics operations. These terms and concepts are essentially the same for any raster-scan graphic terminal. A graphic terminal uses the Cartesian coordinate system as its base.[1] Unless otherwise noted, all of the following definitions are based on the Cartesian coordinate system.

WORLD COORDINATE SPACE

This is used by IGL (Interactive Graphics Library) and is not viewed directly by the operator or service technician. This space encompasses the world of real numbers from minus infinity to plus infinity on both the X and the Y axes.

TERMINAL COORDINATE SPACE

This is the space of valid <XY> coordinates that can be sent to the terminal. This space is 4096 points wide (X = 0 to X = 4095) by 4096 points high (Y = 0 to Y = 4095) for the 4112 terminal. This can also be called the device coordinate space.

RASTER MEMORY SPACE

Raster memory space is always 640 pixels per line by 480 lines. (A pixel is defined elsewhere in this section.) For the 4112, each line is divided into 32 words of 20 bits each. Each pixel is assigned to one bit in the word and this is the address of that pixel. In this way, only those pixels that need to be modified are altered, allowing for much faster time to change the picture. The term "screen" refers to raster memory space and the viewing screen. The screen may be divided into numerous viewports for multiple views of an object and to separate dialog from the picture.

[1] The Cartesian coordinate system is based on X, Y coordinates, compared to the Polar coordinate system, which is based on R, θ coordinates.

THE WINDOW-VIEWPORT TRANSFORM

The explanation that follows and Figure 4-1 best describe the concept of the window-viewport transform for the 4112 terminal.

The terminal's firmware converts coordinates in 4096-by-4096 terminal space to 640 pixels by 480 lines in raster memory space. The window-viewport transform is the mathematical computation used for this conversion.

The left portion of Figure 4-1 shows a part of a house (with a door) in the terminal coordinate space of the 4112. The area of the terminal coordinate space that is to be displayed on the screen is the box labeled WINDOW 1. This is the "window." The right portion of the figure shows the terminal's screen, or raster memory space. Only a part of the screen is designated for displaying the house with a door. This area is called the viewport and the display of the window in the viewport is the window-viewport transform (represented by the two arrows in the illustration).

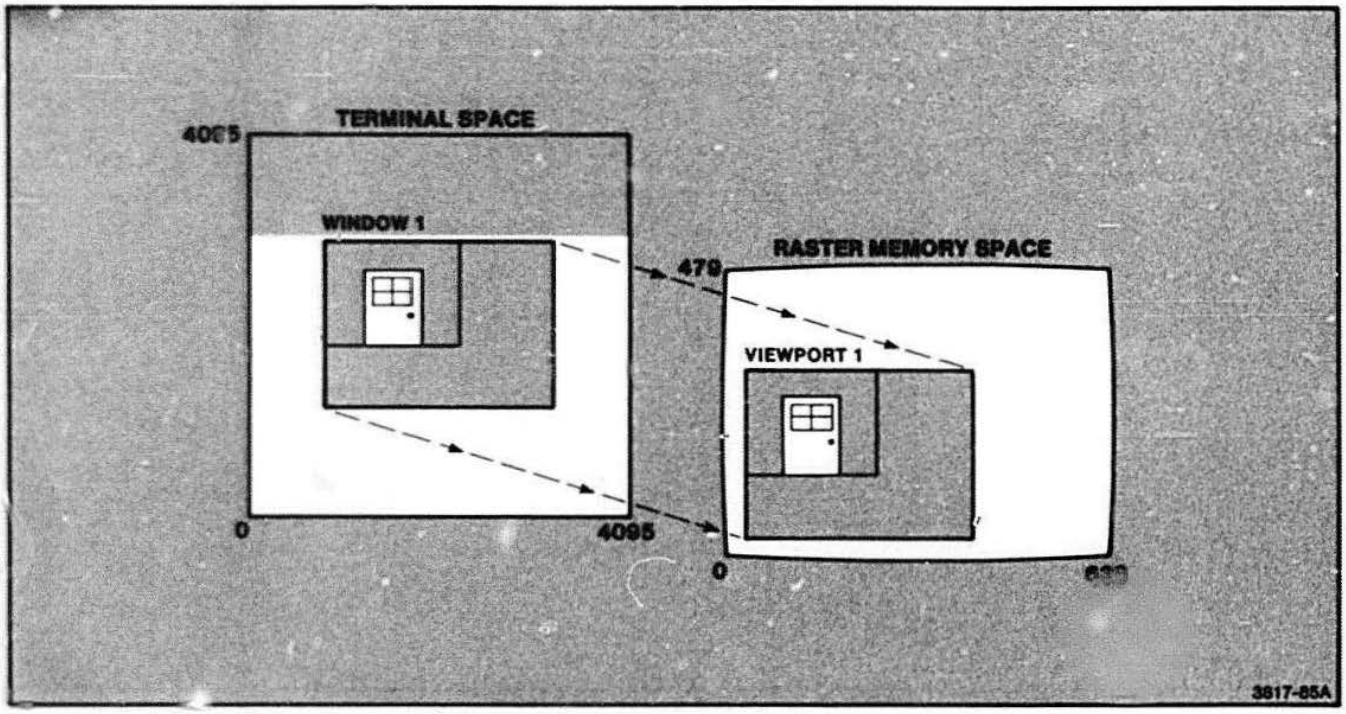


Figure 4-1. Window-Viewport Transform.

WINDOW

The window is that portion of the coordinate space that is to be looked at by the terminal (in the case of terminal coordinate space), or by IGL (in the case of world coordinate space). There is no relation between the window for world coordinate space and the window for terminal coordinate space.

VIEWPORT

The viewport is that portion of the window that is to be displayed in the designated area of the device coordinate space (IGL), or in the designated area of the terminal's display when talking about the terminal only. More than one viewport may be designated and displayed on the 4112. An example that may be easily seen is the screen split into a graphics area and a dialog area (Figure 4-2). A technician will not normally be concerned with the viewport, except to realize that it is based on software rather than hardware in the 4112. The viewport will be the same as the window (default) in all instances requiring hardware maintenance.

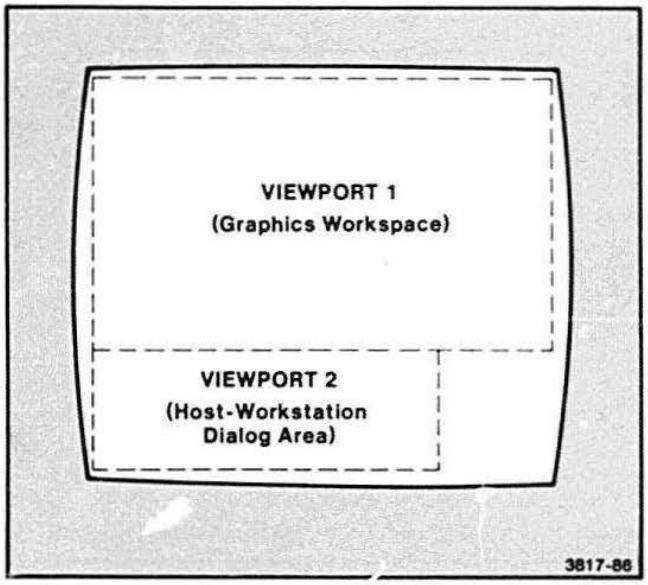


Figure 4-2. Screen with Two Viewports.

GENERAL DISPLAY CONCEPTS

The 4112 display (unlike most video monitors) does not have interlaced scanning. The scanning frequency is 31,500 Hz in the horizontal direction. The frame rate is the same as the field refresh rate in the case of non-interlaced scan, which is 60 Hz. The full 525 lines of scan are covered 60 times a second; however only 480 lines are visible. All display information is conveyed by turning the electron beam on and off as it scans the screen.

PIXELS

The smallest unit of information that can be displayed is the "pixel." (Pixel is a coined word meaning picture element.) A pixel is produced by turning on the electron beam for approximately 39.6 ns during a raster line. This produces a dot on the face of the crt. In the 4112, a pixel can be one of 16 different gray shades, including black. The means of producing these shades is discussed in a later section.

Figure 4-3 depicts how a display can be made from pixels. Raster line 1 contains one pixel; raster line 2 contains three adjacent pixels. Notice that in order to produce three adjacent pixels, the electron beam is turned on for 118.2 ns.

Information about which pixels in the display are on or off is stored as binary data within the raster memory. This data is recalled from the raster memory and used to turn the electron beam on and off as it scans the screen.

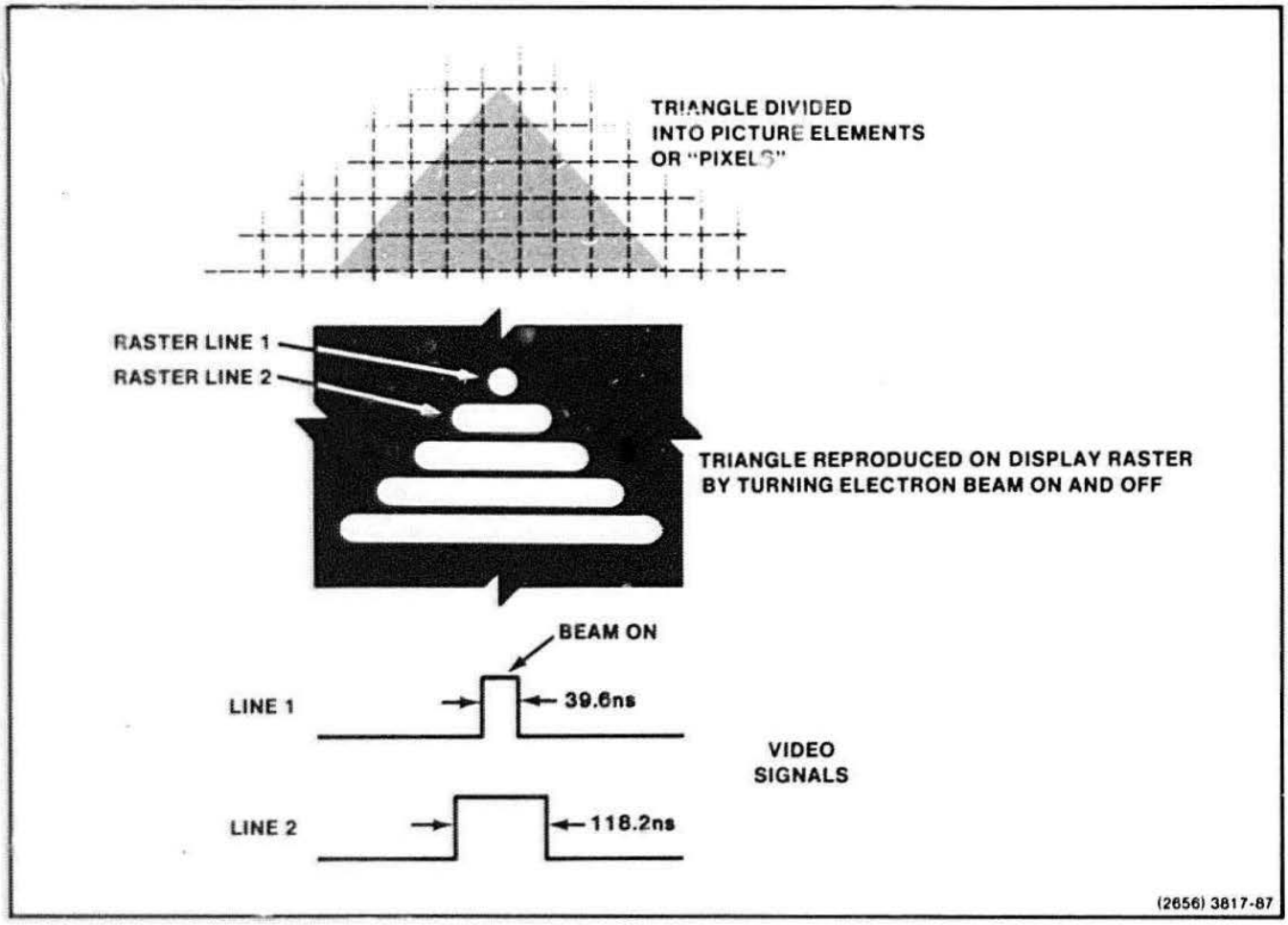


Figure 4-3. Constructing a Display From Pixels.

CHARACTERS

Characters are 8 X 14 arrays of pixels which may be positioned anywhere. There are no "physical cells" in the 4112, only arrays of characters arranged much the same as a typewriter. The illusion of physical cells is created by the firmware, which spaces the character arrays in a regular pattern. The characters all occupy the same amount of space on the line, whether they are wide or narrow characters (i.e., an "i" uses as much space as an "M").

There are two types of text used in the 4112, alphatext and graphtext. Graphtext is used by the operator and can be manipulated in many ways. Alphatext is the default text and is the text used in the dialog area. The character size of alphatext is a 7 x 9 dot matrix in an 8 x 14 block of pixels. See Figure 4-4.

BIT MAP AND DISPLAY CONCEPTS

A bit map is picture information stored as a collection of binary digits in a memory device. For a simple black and white display, there is one memory bit for each pixel on the display screen. If the bit contains a "1," the pixel is on; if the bit is a "0," the pixel is off. This type of memory scheme is called a "real" memory map (as opposed to a "virtual" memory map, which is used in other Tektronix terminals such as the 4027). A virtual memory array requires less memory, but more graphics manipulation hardware, than the real memory array. Because the 4112 has an abundance of graphics memory, it uses a real array, thus storing every pixel whether it is on or off. The result is greater speed and versatility in graphics manipulation.

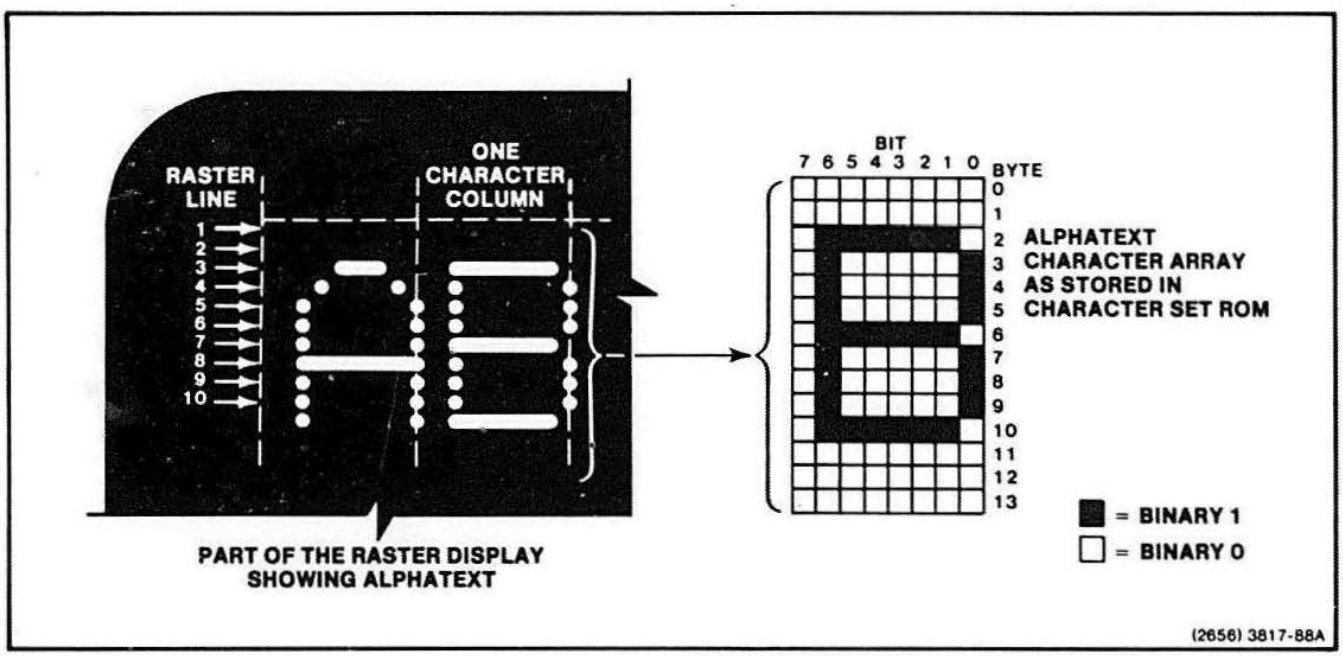


Figure 4-4. 4112 Alphatext Character Array.

4112 OVERVIEW

The 4112 circuitry is divided into two parts:

- Circuit boards that plug into the card cage
- Circuit boards and modules located outside the card cage

The card cage contains circuit boards on two busses: the Processor Bus and the Display Bus. Many of the Processor Bus lines continue into the Display Bus. Physically, the two busses are joined as one bus — the system bus. This allows the processor to send and receive data and control signals over the entire bus to any of the circuit boards.

The Power Supply/Distribution board, the keyboard, and the Display Module are not located in the card cage. The keyboard communicates directly with the Processor board via a separate ribbon cable. The Display Module receives video data from the Video Controller board via a ribbon cable also.

Figure 4-5 is a system block diagram of the 4112. This illustration shows the terminal's major circuit boards and modules and shows how they are connected together in the instrument. Figure 4-5 also shows the host computer's relationship with respect to the 4112. This diagram shows which boards are included in the card cage and also gives their address locations in the 4112's firmware; these addresses begin at F000 (Video Memory Map) and go through F7FF (Memory Plan 0). The flexible disk option and graphics tablet option each consist of an I/F circuit board in the 4112 card cage and the external disk unit or tablet.

BUS MASTERS AND SLAVES

The Processor/Display Bus design allows control of the system bus to be gained and relinquished by "bus masters" and "bus slaves." At any one time, there is only one bus master. After the current bus master is through with its operations on the bus, it gives up control of the bus to the highest priority bus slave, which then becomes the bus master. The current bus master is the only device that can drive address lines and perform reads and writes. The Processor, Display Controller, and Vector Generator boards are the only potential bus masters in the standard 4112. However, the optional Disk Controller board may also be a bus master.

A bus slave is a device that obeys the bus master by sending data to the bus master (during read operations), and by accepting data from the bus master (during write operations). The RAM/ROM board and optional 3PPI board are examples of bus slaves. When a bus master device (such as the Disk Controller board) does not have control of the bus, it functions as a bus slave. For instance, the Processor board, while functioning as bus master, may read from or write to I/O registers on the Disk Controller board; these registers function as a bus slave during this operation.

The position of the boards in the card cage determines bus master priority, which is explained next.

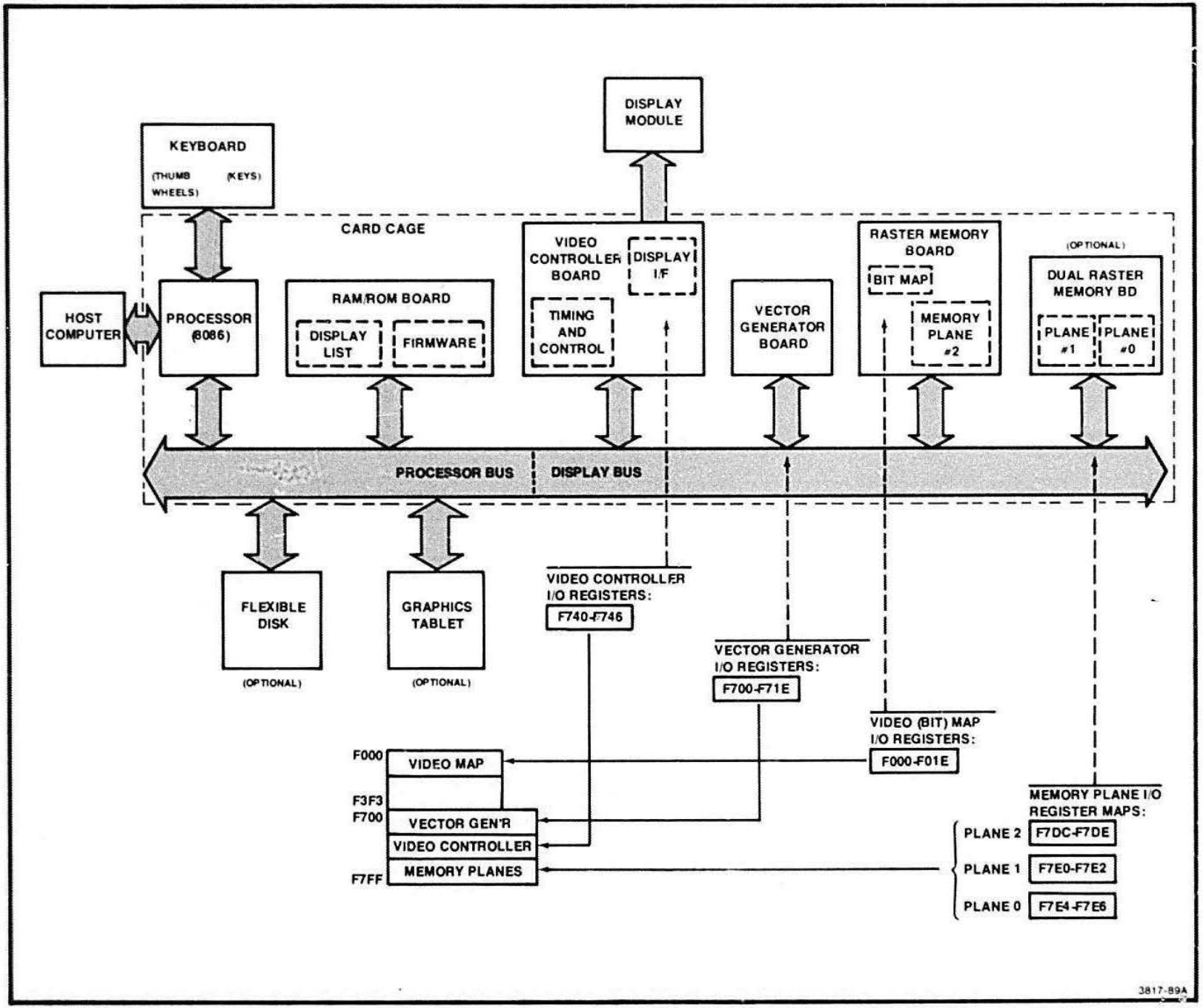


Figure 4-5. 4112 Overall Block Diagram.

PROCESSOR BUS

The Processor Bus includes the left-most seven slots in the card cage and the boards that are plugged into them. See Figure 4-6. Bus masters and bus slaves may occupy any of the seven Processor Bus slots. Priority among bus masters is determined by their relative positions on the bus: if bus master "A" is installed in a slot to the right of bus master "B," then "A" has a higher priority than "B."

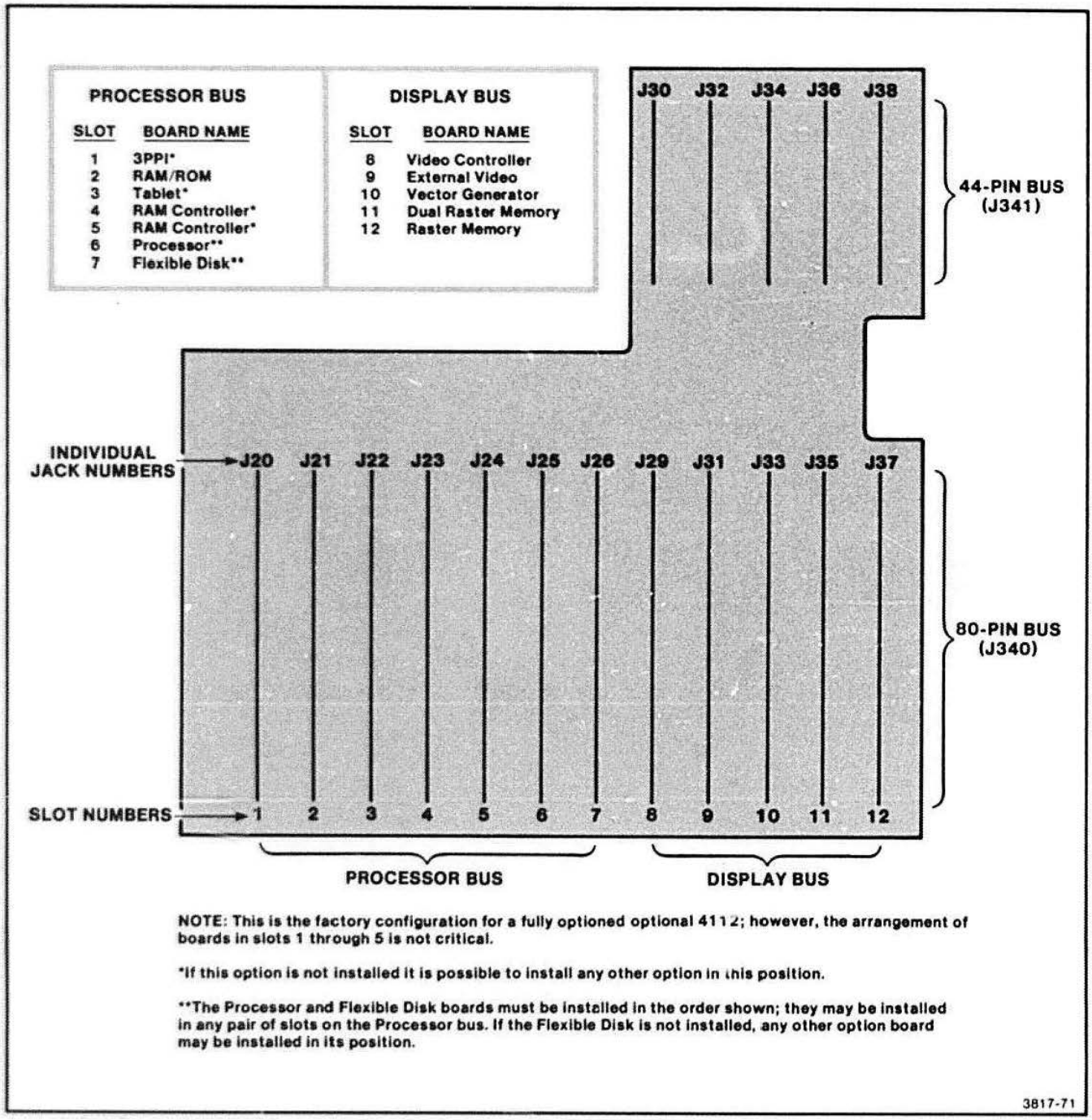


Figure 4-6. Physical Layout of Processor/Display Busses.

Table 4-1 lists the signals and associated connector numbers on the Processor Bus slots.

The Processor board is the chief board on the Processor Bus. The MPU[2] on the Processor board accepts keyboard data and commands through the "keyboard port," or interface. The processor communicates with the host in a similar manner; the processor sends and receives data to and from the host through the RS-232 data link and the "host communications port." The MPU acts upon commands received from the keyboard or host computer and accesses the proper firmware routine on the appropriate board. The MPU then sends instructions to the Video Controller, Vector Generator, or Raster Memory boards initiating the requested operation; these boards are connected to the Display Bus (an extension of the Processor Bus).

[2]MPU represents the 8086 microprocessor unit.

Table 4-1

80-PIN CONNECTOR SIGNALS
(PROCESSOR BUS ONLY)

Pin	Signal	Description	Pin	Signal	Description
1	-12V		23	ADR12-1	Address Bus
2	-12V		24	ADR13-1	Address Bus
3	GND	Ground	25	ADR14-1	Address Bus
4	GND	Ground	26	ADR15-1	Address Bus
5	-5.2V		27	ADR16-1	Address Bus
6	-5.2V		28	ADR17-1	Address Bus
7	PFAIL-0	Power Fail Warning	29	ADR18-1	Address Bus
8	AGND	Analog Ground	30	ADR19-1	Address Bus
9	INIT-0	Initialize	31	INTA-0	Interrupt Acknowledge
10	BHEN-0	Byte High Enable	32	INH-0	Read Inhibit
11	ADR0-0	Address Bus	33	AMWC-0	Adv. Memory Write Cmd.
12	ADR1-1	Address Bus	34	MWTX-0	Memory Write Command
13	ADR2-1	Address Bus	35	MRDC-0	Memory Read Command
14	ADR3-1	Address Bus	36	IORC-0	I/O Read Command
15	ADR4-1	Address Bus	37	AIOWC-0	Adv. I/O Write Command
16	ADR5-1	Address Bus	38	IOWC-0	I/O Write Command
17	ADR6-1	Address Bus	39	ACK1-0	Command Acknowledge 1
18	ADR7-1	Address Bus	40	ACK2-0	Command Acknowledge 2
19	ADR8-1	Address Bus	41	BUSY-0	Bus Busy
20	ADR9-1	Address Bus	42	CBRQ-0	Common Bus Request
21	ADR10-1	Address Bus	43	STEST-0	Self-Test Switch
22	ADR11-1	Address Bus	44		(not used)

(continued)

Table 4-1 (cont)

80-PIN CONNECTOR SIGNALS
(PROCESSOR BUS ONLY)

Pin	Signal	Description	Pin	Signal	Description
45	BCLK-0	Bus Clock	63	DAT6-1	Data Bus
46	GND	Ground	64	DAT7-1	Data Bus
47	GND	Ground	65	DAT8-1	Data Bus
48		(not used)	66	DAT9-1	Data Bus
49	INT0-0	Interrupt Request	67	DAT10-1	Data Bus
50	INT1-0	Interrupt Request	68	DAT11-1	Data Bus
51	INT2-0	Interrupt Request	69	DAT12-1	Data Bus
52	INT3-0	Interrupt Request	70	DAT13-1	Data Bus
53	INT4-0	Interrupt Request	71	DAT14-1	Data Bus
54	INT5-0	Interrupt Request	72	DAT15-1	Data Bus
55	INT6-0	Interrupt Request	73	BREQ-0	Bus Request
56	INT7-0	Interrupt Request	74	BPRN-0	Bus Grant
57	DAT0-1	Data Bus	75	+ 5 V	
58	DAT1-1	Data Bus	76	+ 5 V	
59	DAT2-1	Data Bus	77	GND	Ground
60	DAT3-1	Data Bus	78	GND	Ground
61	DAT4-1	Data Bus	79	+ 12 V	
62	DAT5-1	Data Bus	80	+ 12 V	

DISPLAY BUS

The terminal's Display Bus includes the right-most five slots in the card cage (refer to Figure 4-6).

The left-most slot on the Display Bus is unique. It is reserved for the Video Controller board. Table 4-2 lists the signals on this slot's 80-pin connector. Many of these signals are the same signals that are on the Processor Bus. Those signals that do not appear on the Processor Bus are listed in Table 4-3.

The next slot on the Display Bus is also unique. This slot is reserved for the optional External Video board.

All of the remaining slots on the Display Bus are identical. The right-most slot on the Display Bus, however, should hold the standard Raster Memory board. This board contains terminating resistors for several of the lines on the Display Bus. To terminate these lines properly, the termination resistors should be at the ends of the lines (the right-most Display Bus slot). This right-most slot is the twelfth slot on the 4112 Motherboard.

Table 4-2

80-PIN CONNECTOR SIGNALS
(VIDEO CONTROLLER ONLY)

Pin	Signal	Description	Pin	Signal	Description
1	-12V		21	ADR10-1	Address Bus
2	-12V		22	ADR11-1	Address Bus
3	GND	Ground	23	ADR12-1	Address Bus
4	GND	Ground	24	ADR13-1	Address Bus
5	-5.2V		25	ADR14-1	Address Bus
6	-5.2V		26	ADR15-1	Address Bus
7	PSYNC-0	Power Supply Sync Pulse	27	IORC-0	I/O Read Command
8	NRFND-0	Not Rdy For New Data	28	AIOWC-1	Adv. I/O Write Command
9	INIT-0	Initialize	29	IOWC-0	I/C Write Command
10	VGADR-0	Vect. Gen. Address	30	ACK1-0	Command Acknowledge 1
11	VBUSY-0	Vect. Gen. Busy	31	ACK2-0	Command Acknowledge 2
12	ADR1-1	Address Bus	32	STEST-0	Self-Test Switch
13	ADR2-1	Address Bus	33	GND	Ground
14	ADR3-1	Address Bus	34	GND	Ground
15	ADR4-1	Address Bus	35	MX0-1	Map X Address Bus
16	ADR5-1	Address Bus	36	MX1-1	Map X Address Bus
17	ADR6-1	Address Bus	37	MX2-1	Map X Address Bus
18	ADR7-1	Address Bus	38	MX3-1	Map X Address Bus
19	ADR8-1	Address Bus	39	MX4-1	Map X Address Bus
20	ADR9-1	Address Bus	40	MY1-1	Map Y Address Bus

(continued)

Table 4-2 (cont)

80-PIN CONNECTOR SIGNALS
(VIDEO CONTROLLER ONLY)

Pin	Signal	Description	Pin	Signal	Description
41	MY1-1	Map Y Address Bus	61	DAT4-1	Data Bus
42	MY2-1	Map Y Address Bus	62	DAT5-1	Data Bus
43	MY3-1	Map Y Address Bus	63	DAT6-1	Data Bus
44	MY4-1	Map Y Address Bus	64	DAT7-1	Data Bus
45	MY5-1	Map Y Address Bus	65	DAT8-1	Data Bus
46	MY6-1	Map Y Address Bus	66	DAT9-1	Data Bus
47	MY7-1	Map Y Address Bus	67	DAT10-1	Data Bus
48	MY8-1	Map Y Address Bus	68	DAT11-1	Data Bus
49		(not used)	69	DAT12-1	Data Bus
50	INT6-0	Level 6 Interrupt	70	DAT13-1	Data Bus
51		(not used)	71	DAT14-1	Data Bus
52		(not used)	72	DAT15-1	Data Bus
53		(not used)	73	SACK-0	System Acknowledge
54		(not used)	74	EQUAL-0	Memory Test Equal Deleted
55	GND	Ground	75	+ 5 V	
56	GND	Ground	76	+ 5 V	
57	DAT0-1	Data Bus	77	GND	Ground
58	DAT1-1	Data Bus	78	GND	Ground
59	DAT2-1	Data Bus	79	+ 12 V	
60	DAT3-1	Data Bus	80	+ 12 V	

Table 4-3

80-PIN CONNECTOR SIGNALS
(DISPLAY BUS, EXCEPT VIDEO CONTROLLER)

Pin	Signal	Description	Pin	Signal	Description
1	-12V		8	NRFND-0	Not Ready For New Data
2	-12V		9	INIT-0	Initialize
3	GND	Ground	10	VGADR-0	Vect. Gen. Address
4	GND	Ground	11	VBUSY-0	Vect. Gen. Busy
5	-5.2V		12	ADR1-1	Address Bus
6	-5.2V		13	ADR2-1	Address Bus
7	PSYNC-0	Power Supply Sync Pulse	14	ADR3-1	Address Bus

Table 4-3 (cont)

80-PIN CONNECTOR SIGNALS
(DISPLAY BUS, EXCEPT VIDEO CONTROLLER)

Pin	Signal	Description	Pin	Signal	Description
15	ADR4-1	Address Bus	48	MY8-1	Map Y Address Bus
16	ADR5-1	Address Bus	49	MP0-0	Pixel Address/Raster Mask
17	ADR6-1	Address Bus	50	MP1-0	Pixel Address/Raster Mask
18	ADR7-1	Address Bus	51	MP2-0	Pixel Address/Raster Mask
19	ADR8-1	Address Bus	52	MP3-0	Pixel Address/Raster Mask
20	ADR9-1	Address Bus	53	MP4-0	Pixel Address/Raster Mask
21	ADR10-1	Address Bus	54	PWRT-0	Pixel Address Write Pulse
22	ADR11-1	Address Bus	55	GND	Ground
23	ADR12-1	Address Bus	56	GND	Ground
24	ADR13-1	Address Bus	57	DAT0-1	Data Bus
25	ADR14-1	Address Bus	58	DAT1-1	Data Bus
26	ADR15-1	Address Bus	59	DAT2-1	Data Bus
27	IORC-0	I/O Read Command	60	DAT3-1	Data Bus
28	AIOWC-1	Adv. I/O Write Command	61	DAT4-1	Data Bus
29	IOWC-0	I/O Write Command	62	DAT5-1	Data Bus
30	ACK1-0	Command Acknowledge 1	63	DAT6-1	Data Bus
31	ACK2-0	Command Acknowledge 2	64	DAT7-1	Data Bus
32	STEST-0	Self-Test Switch	65	DAT8-1	Data Bus
33	GND	Ground	66	DAT9-1	Data Bus
34	GND	Ground	67	DAT10-1	Data Bus
35	MX0-1	Map X Address Bus	68	DAT11-1	Data Bus
36	MX1-1	Map X Address Bus	69	DAT12-1	Data Bus
37	MX2-1	Map X Address Bus	70	DAT13-1	Data Bus
38	MX3-1	Map X Address Bus	71	DAT14-1	Data Bus
39	MX4-1	Map X Address Bus	72	DAT15-1	Data Bus
40	MY0-1	Map Y Address Bus	73	SACK-0	System Acknowledge
41	MY1-1	Map Y Address Bus	74	EQUAL-0	Memory Test Equal Deleted
42	MY2-1	Map Y Address Bus	75	+ 5 V	
43	MY3-1	Map Y Address Bus	76	+ 5 V	
44	MY4-1	Map Y Address Bus	77	GND	Ground
45	MY5-1	Map Y Address Bus	78	GND	Ground
46	MY6-1	Map Y Address Bus	79	+ 12 V	
47	MY7-1	Map Y Address Bus	80	+ 12 V	

Video Controller

The Video Controller board contains timing and decoding circuits that synchronize the various interrelated operations on the Vector Generator, Raster Memory, and Display Interface circuits. The write cycle timing of the Raster Memory RAMs comes from this board. The vertical and horizontal sweep and sync signals for the display module are also generated on this board. The Video Controller board's clocks are independent of the processor's clocks; consequentially the timing functions do not depend on the processor. The Video Controller board acts as a link between the Processor and Display Busses. The Video Controller board resides in its own dedicated slot on the 4112 Motherboard. The Display Interface block located on the Video Controller board is discussed in Section 6.

Vector Generator

The Vector Generator board receives instructions from the main processor. It then creates the bit patterns corresponding to various slopes generated by moves and draws. This amounts to writing only certain pixels in a word (20 bits long) and skipping the remaining bits. Certain bits are then written into a word in adjacent lines (above or below it) thus creating a sloped line vector. The Vector Generator receives input over the Display Bus. Its output is sent to the Raster Memory board, via the Display Bus.

Display Memories

The Raster Memory board has two separate functions:

- It contains the primary "bit plane" which holds the X-Y pixel data for the current display
- It contains the video interpreter or "map"

The 4112 may contain two additional memory planes on an optional Dual Raster Memory board, providing a total of three planes. Each plane contains one bit per pixel over the entire display. The memory is arranged to correspond with the set of 480 raster scan lines appearing on the display. Each line is 640 bits long and is divided into 32 words of 20 bits each. The Raster Memory board receives its timing and control information from the Video Controller board. It is set up to dump its contents sequentially out to a shift register synchronized with the 60 Hz scan cycle. When the display reads from its memory, data leaves the output shift register and enters the Display Bus. From there it goes to the Raster Memory Video Map and then to the DACs (digital-to-analog converters) on the Video Controller board. It then goes to the Display Module (Analog Video).

The Video Map is a means of taking 4 bits of data (8 shades plus cursor video) and allowing these to choose from a much larger list of possible shades (16). The Video Map is programmed via commands entered at the keyboard; these commands are interpreted by the processor and sent to this map circuit. The output of the map is a four-bit signal that represents a video mixture determined by the four input bits.

The write cycle timing on the Raster Memory board is independent of the read cycle (and sweep rate) and therefore may be much faster. The Vector Generator can write data into memory (via the ALUs) without interfering with the read cycles. In order to achieve this, the Video Controller board keeps track of the two processes (read and write). When the Video Controller board sends a refresh signal, the Raster Memory board inhibits the write pulse. This prevents a write cycle, which would cause undefined memory modification during screen refresh.

Interfacing

The Video Controller board also contains a Display Interface module. This module is connected to the Video Map on the standard Raster Memory board (via a 44-pin connector). The interface's main function is to take the four-bit output from the Raster Memory Board and to perform a digital-to-analog conversion on the picture data. This interface also amplifies this graphic signal so it will drive the Display Module's video input. A secondary function of the Display Interface is to pass and/or modify the timing signals from those Video Controller board's circuits that provide the Display Module's vertical and horizontal sweep, sync., etc.

CONNECTORS

Tables 4-1 through 4-5 describe the main connectors. Figure 4-6 shows the locations of the busses and their jack numbers.

Table 4-4

44-PIN CONNECTOR SIGNALS (DISPLAY BUS)

Pin	Signal	Description	Pin	Signal	Description
1	GND	Ground	23	VACK-0	Vector Acknowledge
2	GND	Ground	24	VENB-0	Vector Enable
3	-5.2 V	Power	25	VRQST-0	Vector Request
4	-5.2 V	Power	26	REF-0	Refresh
5	-2.0 V	Power	27	PDAT0-1	Pixel Data Bus
6	-2.0 V	Power	28	PDAT1-1	Pixel Data Bus
7	COL-1	Column	29	PDAT2-1	Pixel Data Bus
8	RAS-1	Row Address Strobe	30	XLOAD-0	Video Controller Reboot
9	CAS-0	Column Address Strobe	31	VCLK-0	Vector Clock
10	WR-1	Write	32	50 Hz-0	50/60 Hz Strap
11	DCLK-1	Dot Clock	33	VDRIVE-0	Vertical Drive
12	LOAD-1	Load	34	XEN-0	External Video Opt. Present
13	VID0-1	Video Data Bus	35	XVSYNC-0	Extenal Vertical Sync.
14	VID1-1	Video Data Bus	36	XHSYNC-0	External Horiz. Sync.
15	VID2-1	Video Data Bus	37	MODE0-0	Mode 0
16	VID3-1	Video Data Bus	38	MODE1-0	Mode 1
17	DAC0-1	D/A Converter Bus	39	TEST-0	Test
18	DAC1-1	D/A Converter Bus	40	MAP-0	Map Write Select
19	DAC2-1	D/A Converter Bus	41	-5.2 V	Power
20	DAC3-1	D/A Converter Bus	42	-5.2 V	Power
21	SCANSYNC-1	Scan Sync Pulse	43	GND	Ground
22		(not used)	44	GND	Ground

Table 4-5

50-PIN FRONT-EDGE CONNECTOR SIGNALS

Pin	Signal	Description	Pin	Signal	Description
1	YNEXT-0	Y Axis Increment Next	2	XNEXT-0	X Axis Increment Next
3	YSIGN-0	Y Sign Bit	4	XSIGN-0	X Sign Bit
5		Reserved	6		Reserved
7		Reserved	8		Reserved
9		Reserved	10	EXT-0	External Data Input Select

Single Plane Raster Memory Board

Pin	Signal	Description	Pin	Signal	Description
11		Reserved	12	X19-0	Ext Vid Bit 19, Plane 2
13		Reserved	14	X18-0	Ext Vid Bit 18, Plane 2
15		Reserved	16	X17-0	Ext Vid Bit 17, Plane 2
17		Reserved	18	X16-0	Ext Vid Bit 16, Plane 2
19		Reserved	20	X15-0	Ext Vid Bit 15, Plane 2
21		Reserved	22	X14-0	Ext Vid Bit 14, Plane 2
23		Reserved	24	X13-0	Ext Vid Bit 13, Plane 2
25		Reserved	26	X12-0	Ext Vid Bit 12, Plane 2
27		Reserved	28	X11-0	Ext Vid Bit 11, Plane 2
29		Reserved	30	X10-0	Ext Vid Bit 10, Plane 2
31		Reserved	32	X9-0	Ext Vid Bit 9, Plane 2
33		Reserved	34	X8-0	Ext Vid Bit 8, Plane 2
35		Reserved	36	X7-0	Ext Vid Bit 7, Plane 2
37		Reserved	38	X6-0	Ext Vid Bit 6, Plane 2
39		Reserved	40	X5-0	Ext Vid Bit 5, Plane 2
41		Reserved	42	X4-0	Ext Vid Bit 4, Plane 2
43		Reserved	44	X3-0	Ext Vid Bit 3, Plane 2
45		Reserved	46	X2-0	Ext Vid Bit 2, Plane 2
47		Reserved	48	X1-0	Ext Vid Bit 1, Plane 2
49		Reserved	50	X0-0	Ext Vid Bit 0, Plane 2

Table 4-5 (cont)

50-PIN FRONT-EDGE CONNECTOR SIGNALS

Dual Plane Raster Memory Board

Pin	Signal	Description	Pin	Signal	Description
11	X19-0	Ext Vid Bit 19, Plane 0	12	Y19-0	Ext Vid Bit 19, Plane 1
13	X18-0	Ext Vid Bit 18, Plane 0	14	Y18-0	Ext Vid Bit 18, Plane 1
15	X17-0	Ext Vid Bit 17, Plane 0	16	Y17-0	Ext Vid Bit 17, Plane 1
17	X16-0	Ext Vid Bit 16, Plane 0	18	Y16-0	Ext Vid Bit 16, Plane 1
19	X15-0	Ext Vid Bit 15, Plane 0	20	Y15-0	Ext Vid Bit 15, Plane 1
21	X14-0	Ext Vid Bit 14, Plane 0	22	Y14-0	Ext Vid Bit 14, Plane 1
23	X13-0	Ext Vid Bit 13, Plane 0	24	Y13-0	Ext Vid Bit 13, Plane 1
25	X12-0	Ext Vid Bit 12, Plane 0	26	Y12-0	Ext Vid Bit 12, Plane 1
27	X11-0	Ext Vid Bit 11, Plane 0	28	Y11-0	Ext Vid Bit 11, Plane 1
29	X10-0	Ext Vid Bit 10, Plane 0	30	Y10-0	Ext Vid Bit 10, Plane 1
31	X9-0	Ext Vid Bit 9, Plane 0	31	Y9-0	Ext Vid Bit 9, Plane 1
33	X8-0	Ext Vid Bit 8, Plane 0	32	Y8-0	Ext Vid Bit 8, Plane 1
35	X7-0	Ext Vid Bit 7, Plane 0	33	Y7-0	Ext Vid Bit 7, Plane 1
37	X6-0	Ext Vid Bit 6, Plane 0	34	Y6-0	Ext Vid Bit 6, Plane 1
39	X5-0	Ext Vid Bit 5, Plane 0	35	Y5-0	Ext Vid Bit 5, Plane 1
41	X4-0	Ext Vid Bit 4, Plane 0	36	Y4-0	Ext Vid Bit 4, Plane 1
43	X3-0	Ext Vid Bit 3, Plane 0	37	Y3-0	Ext Vid Bit 3, Plane 1
45	X2-0	Ext Vid Bit 2, Plane 0	38	Y2-0	Ext Vid Bit 2, Plane 1
47	X1-0	Ext Vid Bit 1, Plane 0	39	Y1-0	Ext Vid Bit 1, Plane 1
49	X0-0	Ext Vid Bit 0, Plane 0	40	Y0-0	Ext Vid Bit 0, Plane 1

Section 5

PROCESSOR BUS THEORY

INTRODUCTION TO PROCESSOR BUS

The Processor board and the RAM/ROM board, together with their respective parts of the Motherboard, comprise the Processor Bus. The Processor Bus, joined with the Display Bus, forms the total system bus (refer back to Figure 4-5 in Section 4, *Theory Overview*).

The first part of this theory section explains the operation of the "heart" of the 4112, the Processor board. The next major part of this section deals with the system memories, located on the RAM/ROM and optional RAM Controller boards.

PROCESSOR BOARD THEORY

PROCESSOR THEORY OVERVIEW

The Processor board consists of circuitry that performs the following functions:

- Processes system firmware commands and data along with interrupt data from on and off the board
- Accepts interrupt signals from the host computer communications port, the keyboard, peripheral devices and other circuitry connected to the Processor Bus, and from other circuitry on the Processor board itself
- Transmits and receives data from the Processor Bus
- Stores part of the system firmware and the terminal initialization information
- Provides control and status signals primarily for the microprocessor unit (MPU)
- Communicates with the host computer using the RS-232 communication standard
- Communicates with the keyboard

These functions are performed by the blocks shown in the simplified block diagram of the Processor board (Figure 5-1). The following pages discuss each of these blocks; detailed circuit descriptions for the Processor board's circuitry are located later in this section.

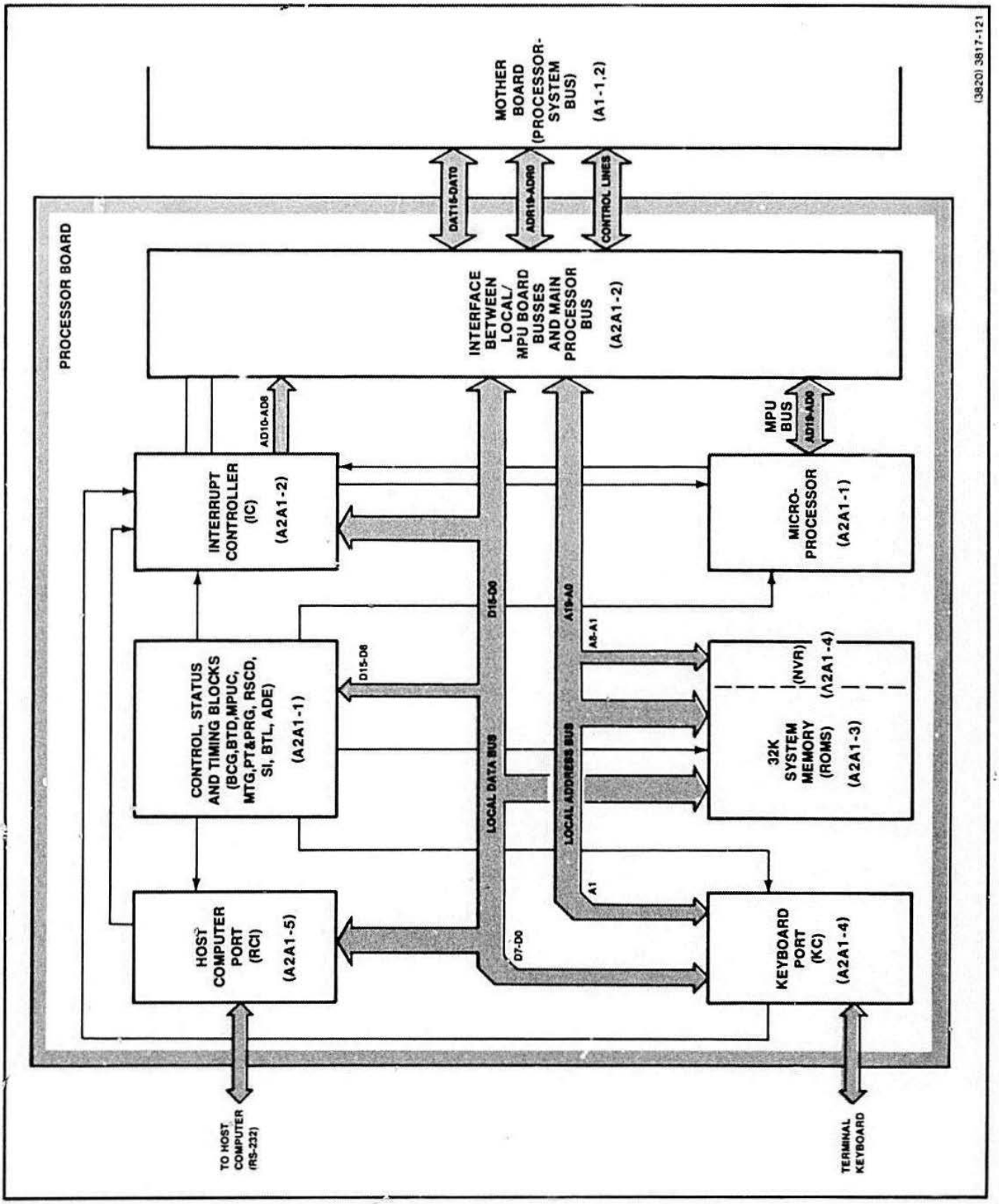


Figure 5-1. Simplified Block Diagram of Processor Board.

Microprocessor (MPU)

This block consists of the microprocessor unit. This 16-bit processor time-multiplexes its AD0-AD19 (MPU Bus) lines: that is, at one point in time address information is on these lines; then later data information is on these lines. The MPU outputs three internal state identifiers (S0-S2), which are used by the board's circuit blocks to synchronize their operations with the MPU. Inputs to the block are primarily a clock, a reset, and an interrupt signal.

Interrupt Controller

The Interrupt Controller circuitry consists primarily of the Peripheral Interrupt Controller (PIC). This integrated circuit determines which one of eight interrupting sources is to be serviced if more than one source requests servicing simultaneously. The interrupting sources can be other boards in the terminal, such as the Three Port Peripheral Interface (3PPI) board, or Processor board circuitry, such as the keyboard port or host computer port. The MPU communicates with the Interrupt Controller block through the Local (Processor board) Data Bus, D0-D15. The PIC is programmed by the MPU shortly after the terminal is turned on. The MPU can also read the current status of the PIC and change its mode of operation by reprogramming its internal registers.

Processor Board to Processor/System Bus Interface

The primary inputs to the Processor Board to Processor /System Bus Interface circuitry are the lines on the multiplexed (address/data) MPU Bus; these lines are AD0-AD19, which are output directly from the MPU. The AD0-AD19 signal lines carry, at different times, data and address information. This interface separates the data and address information into four distinct buses:

- D0-D15 is the Local Data Bus
- A0-A19 is the Local Address Bus
- DAT0-DAT15 is the Processor/System Data Bus
- ADR0-ADR19 is the Processor/System Address Bus

This block also outputs control and status signals onto the Processor/System Bus (hereafter called the "Processor Bus").

System Memory

There are approximately 32-thousand bytes of ROM in the System Memory circuitry that contain most of the basic system firmware. The Local Data and Address Busses connect to this block. Memory is addressed using the Local Address Bus, and the selected data is placed on the Local Data Bus. The System Memory also includes non-volatile RAM where setup parameters are retained when the terminal power switch is off.

Control, Status, and Timing

This circuitry performs MPU control, status detection, and timing functions for the Processor board itself. The following related blocks of circuitry are labeled on the Processor board schematics.

- The MPU Control Logic — generates the 4.9152-MHz clock signal for the MPU. The block also synchronizes the reset and ready inputs of the MPU.
- The Bus Transfer Logic — provides signals that inform bus masters and slaves whether or not they can use the Processor Bus. There is priority-determining logic on the Motherboard that works in conjunction with this circuitry.
- The Address Decoding circuitry — creates signals from high-order address bits that indicate what area of I/O or memory address space that data is to be sent to or received from.
- The Bus Timeout Detector — detects when a slave device fails to respond with an acknowledge signal (ACK1 or ACK2) to a command from any master device. If the circuitry does detect this failure to respond, it drives its own acknowledge signal (ACK1 or ACK2) onto the bus and sets an error status bit. This action prevents the bus from "hanging"; that is, it prevents the bus from remaining in a state that cannot be responded to by any master or slave device.

- The Status Input circuitry — allows the MPU to read two Processor board status signals. This circuitry also outputs STATEN, which is input to the Bus Timeout Detector.

- The Bus Clock Generator — produces a clock signal (BCLK) for the Processor and Display Busses.

- The Microprocessor Timing Generator — receives three signals (S0-S2) from the MPU that indicate whether the MPU is acknowledging an interrupt, reading or writing to I/O or memory space, fetching an instruction, in a halt state, or in a no-bus-cycle state. This information synchronizes operations both on and off the Processor board.

The Programmable Timer and Baud Rate Generator consist of a Programmable Interval Timer that primarily provides variable timing functions. This circuitry provides the transmit baud rate, a firmware interval timer, the bus timeout interval, and the RS-232 intercharacter delay.

Host Computer Port

The Host Computer Port circuitry communicates with the host computer by means of RS-232 signals. A programmable UART-type integrated circuit accepts RS-232 control and data signals from the host computer and then converts this information to parallel data and interrupts for the MPU. In addition to various control and status signals, the block outputs data on the Local Data Bus, D0-D15.

Circuitry related to the host computer port is the RS-232 State Change Detector. This detects state changes on the incoming RS-232 status lines and generates interrupts if changes occur.

Keyboard Port

The Keyboard Port circuitry accepts data from the keyboard. The Peripheral Interface Microprocessor (PI MPU), dedicated to servicing the keyboard, processes this data and outputs it to part of the Local Data Bus, D0-D7. The PI MPU also outputs various control signals, including an interrupt (KBINT) that reaches the MPU after being processed by the Interrupt Controller circuitry.

PROCESSOR BOARD CIRCUIT BLOCK DESCRIPTIONS

Every block of circuitry that appears on the Processor board schematics is described here. Refer to Figure 5-2 for an overall view of how the circuit blocks communicate. Some individual block descriptions are further supported with detailed block diagrams. Those descriptions without more detailed illustrations (e.g., Address Drivers, Data Drivers/Receivers, etc.) are shown on the Processor Board Block Diagram, Figure 5-2. Note that the Address Drivers and Data Drivers/Receivers perform analogous tasks for the address and and data information that the MPU emits. They either output this information to the main Processor Bus or the MPU Bus, depending on the state of control signals from the MPU.

In the description of some blocks of circuitry, abbreviated signal names are used instead of detailed 4112 signal names. These names are usually the input or output pin name of an LSI circuit as shown on the manufacturer's data sheet. Such names are enclosed in parentheses. Some examples are (CLK), (OSC), and (RDY) in the Microprocessor Control block. These obviously stand for clock, oscillator, and ready.

Often signal names are an abbreviation of the more lengthy functional name. Most signal names are followed by the full functional name in parentheses. Sometimes the signal name in parentheses also contains descriptive terms in brackets. These inner brackets enclose additional explanatory words about the signal name, for example, in the Bus Transfer Logic circuitry, there is "BUSY ([System Bus] Busy)". This means the System Bus is busy.

Seven of the eighteen blocks have an LSI circuit as a main component. Many of these are programmable and all are multipurpose. The LSI circuits are used in a definite configuration (and in some cases in a definite "mode") in the design of the Processor board. The block descriptions do not give complete accounts of the unused "modes" and configurations of these LSI circuits. However, Table 5-1 gives references to further information, along with the abbreviations used for these LSI circuits.

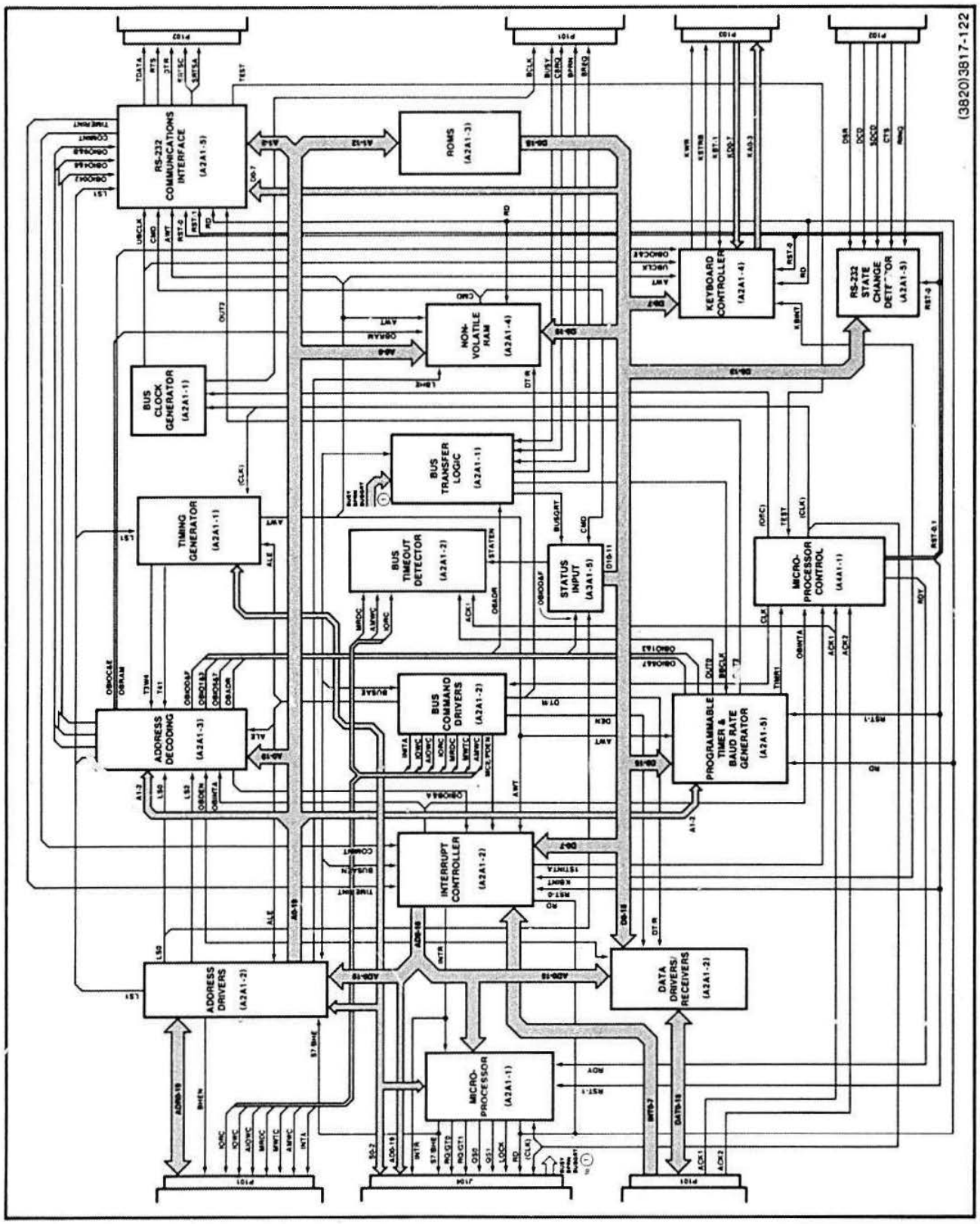


Figure 5-2. Processor Board Block Diagram.

Table 5-1

MANUFACTURERS' NOMENCLATURE FOR LSI CIRCUITS

LSI Circuit	Abbreviation	Manufacturer's Number
Programmable Interrupt Controller	PIC	8259A[a]
Microprocessor	MPU	8086[a]
Clock Generator and Driver	CGD	8284[a]
Bus Controller	BC	8288[a]
Keyboard Controller MPU	KC MPU	8041A[a]
Programmable Interval Timer	PIT	8253[a]
Programmable Communications Interface	PCI	2661[b]

[a]Description in Intel Component Data Catalog, 1980.
[b]Description in Signetics Data Manual, 1980.

MPU

The MPU controls the general-purpose reading and writing of data and address information for the entire terminal system. Sometimes the MPU gives up control of the Processor Bus in favor of other bus masters.

The MPU is a general-purpose microprocessor that has an address space of one megabyte. It operates at 4.9152 MHz and manipulates data in 8-bit or 16-bit word sizes. See Figure 5-3.

The Bus Cycle. The MPU operations and related bus cycles require use of the MPU bus for definite time intervals. These time intervals are named T1 through T4, Tw, and Ti. Clock states T1 through T4 each have a duration of 200 ns.

Some operations require that one or more clock states are inserted between T3 and T4. These states are Tw — "wait" states. Also, sometimes states are inserted between bus cycles. These are Ti — "idle" states. The MPU uses idle states for internal housekeeping operations.

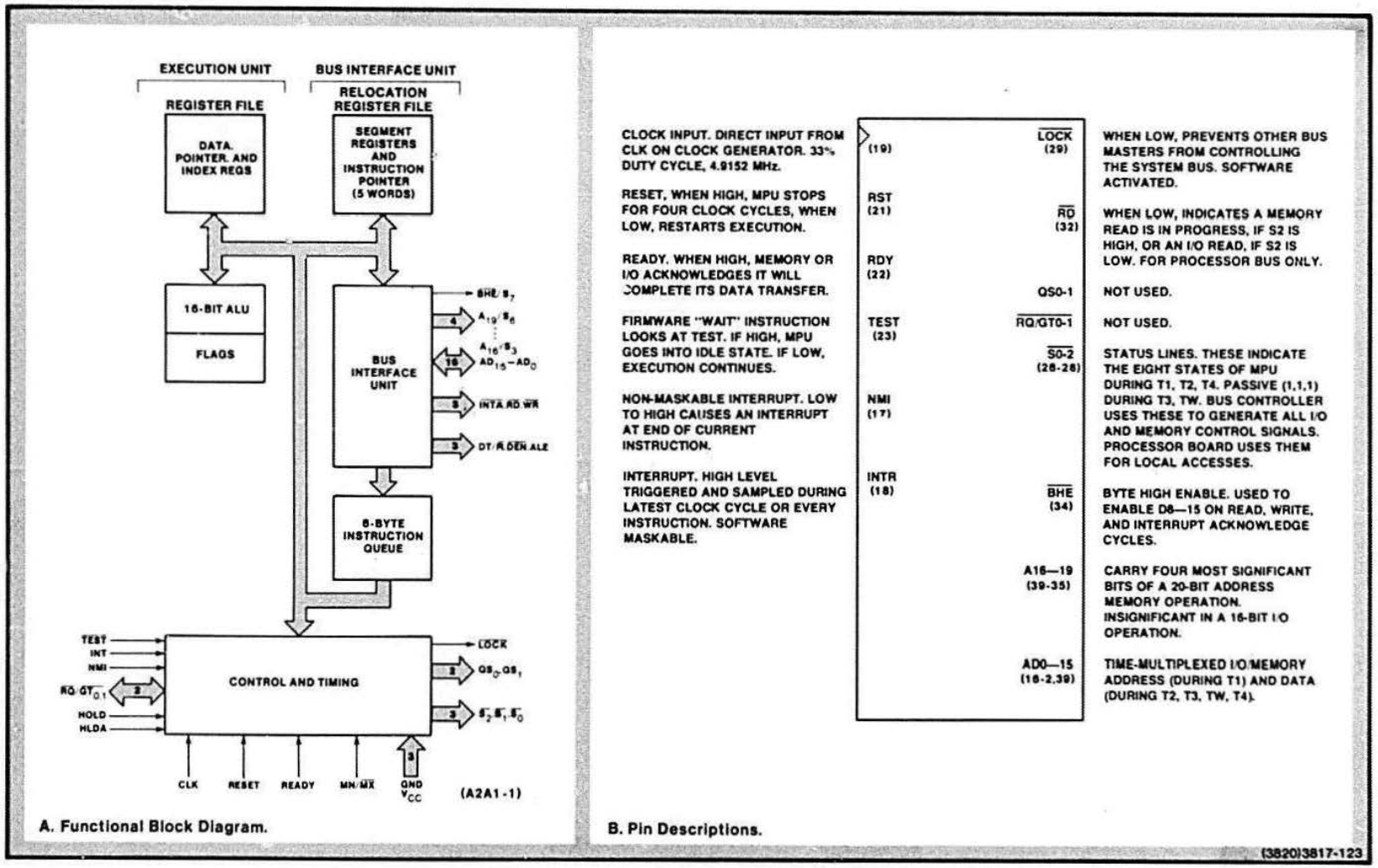
MPU Internal States. The major operations of the MPU are reading and writing to memory or I/O address space, reset and initialization, and interrupt operations.

During normal operation, the MPU performs one of eight types of bus cycles:

- Interrupt Acknowledge
- Read I/O Port
- Write I/O Port
- Halt
- Code Access
- Read from Memory
- Write to Memory
- Inactive

These cycles are encoded in MPU outputs SO-S2. Table 5-2, Status Word and Bus Controller Commands, shows the cycle that corresponds with each of the eight bit patterns of S0-S2. The cycle status information is available during states T2, T3, and Tw. S0-S2 become binary 111 (inactive) during T4, which lasts through any Ti states.

Memory and I/O Address Space Access. During T1, the MPU outputs an address on the data bus. The MPU state information on SO-S2 becomes available and the address is latched during T2. Also, during T2, the data path direction on the bus is switched if the operation is a read instead of a write. Data is then read from or written to memory or I/O locations during T2, T3, and Tw. The information on S0-S2 is used by different functional blocks of circuitry on the Processor board if the read or write access is local. Otherwise the S0-S2 information is converted directly into I/O and memory access commands for the Processor Bus by the Command Driver.



A. Functional Block Diagram.

CLOCK INPUT. DIRECT INPUT FROM CLK ON CLOCK GENERATOR. 33% DUTY CYCLE, 4.9152 MHz.	(19)	LOCK (29)	WHEN LOW, PREVENTS OTHER BUS MASTERS FROM CONTROLLING THE SYSTEM BUS. SOFTWARE ACTIVATED.
RESET, WHEN HIGH, MPU STOPS FOR FOUR CLOCK CYCLES, WHEN LOW, RESTARTS EXECUTION.	RST (21)	RD (32)	WHEN LOW, INDICATES A MEMORY READ IS IN PROGRESS, IF S2 IS HIGH, OR AN I/O READ, IF S2 IS LOW. FOR PROCESSOR BUS ONLY.
READY. WHEN HIGH, MEMORY OR I/O ACKNOWLEDGES IT WILL COMPLETE ITS DATA TRANSFER.	RDY (22)	QS0-1	NOT USED.
FIRMWARE "WAIT" INSTRUCTION LOOKS AT TEST. IF HIGH, MPU GOES INTO IDLE STATE. IF LOW, EXECUTION CONTINUES.	TEST (23)	RQ/GT0-1	NOT USED.
		S0-2 (26-28)	STATUS LINES. THESE INDICATE THE EIGHT STATES OF MPU DURING T1, T2, T4. PASSIVE (1,1,1) DURING T3, TW. BUS CONTROLLER USES THESE TO GENERATE ALL I/O AND MEMORY CONTROL SIGNALS. PROCESSOR BOARD USES THEM FOR LOCAL ACCESSES.
NON-MASKABLE INTERRUPT. LOW TO HIGH CAUSES AN INTERRUPT AT END OF CURRENT INSTRUCTION.	NMI (17)		
INTERRUPT. HIGH LEVEL TRIGGERED AND SAMPLED DURING LATEST CLOCK CYCLE OR EVERY INSTRUCTION. SOFTWARE MASKABLE.	INTR (18)	BHE (34)	BYTE HIGH ENABLE. USED TO ENABLE D8—15 ON READ, WRITE, AND INTERRUPT ACKNOWLEDGE CYCLES.
		A16—19 (39-35)	CARRY FOUR MOST SIGNIFICANT BITS OF A 20-BIT ADDRESS MEMORY OPERATION. INSIGNIFICANT IN A 16-BIT I/O OPERATION.
		AD0—15 (16-2,39)	TIME-MULTIPLEXED I/O/MEMORY ADDRESS (DURING T1) AND DATA (DURING T2, T3, TW, T4).

B. Pin Descriptions.

(3820)3817-123

Figure 5-3. MPU Functional Block Diagram.

Reset and Initialization. MPU reset occurs when (RST) from the Microprocessor Control circuitry goes high. (RST) must stay high for at least four clock cycles. The MPU executes no operations as long as (RST) is high. When (RST) goes low, an internal reset sequence is triggered that lasts about ten clock cycles. After this, the MPU fetches the instruction in location X'FFFF0'. There must be at least 50 μs between power-up and the high-to-low transition of (RST).

Interrupt Operations. There are two hardware interrupts to the MPU: NMI and INTR. NMI is the non-maskable interrupt, and INTR is the maskable interrupt request input.

The non-maskable interrupt stays high for more than two clock cycles; NMI is latched by the MPU and is serviced immediately after the current instruction is completed. NMI is only available on the Processor Board Test Fixture Connector and is not part of the Processor Bus.

The maskable interrupt is a cycle that may precede the end of the current instruction; the MPU is then triggered into a response sequence. The MPU executes two consecutive interrupt acknowledge cycles (same as two bus cycles). (See the Interrupt Controller description that follows.) LOCK is held low from T2 of the first cycle to T2 of the second cycle. During the second bus cycle, a byte is fetched from the PIC. This byte specifies the source that requires the interrupt. The byte also addresses a location in ROM that determines the appropriate interrupt service for this condition.

INTR can be disabled by resetting a status bit in the MPU (via software instructions).

Interrupt Controller

The Interrupt Controller handles a maximum of eight Processor Bus and Processor board interrupt signals (INT0-INT7) and determines the priority of each interrupt signal in relation to the others. This controller also has the capability of addressing eight other Programmable Interrupt Controllers.

The heart of the Interrupt Controller is the Programmable Interrupt Controller (PIC) integrated circuit. The PIC receives interrupt signals (INT0-INT7) and INTA from the Processor Bus and control signals from other circuits on the board. It receives and transmits data from the Local Data Bus, and it outputs INTR, OBINTA, and AD8-AD10 (which can carry addresses for eight other PICs). The other circuitry in the Interrupt Controller inverts and buffers INT0-INT7, provides enabling for the AD8-AD10 drivers, and produces 1STINTA. Also, BUSAEN and INTA are NANDed for the INTA input of the PIC.

This integrated circuit consists of five main blocks of circuitry:

- The Local Data Bus Buffer
- The Interrupt Priority Logic and Registers
- The Control Logic
- The Read and Write Logic
- The cascade buffers and comparator

See Figure 5-4, Programmable Interrupt Controller Block Diagram.

Local Data Bus Buffer. Eight bits, D0-D7, are transmitted and received by this tri-state buffer. The system firmware supplies control words and status information to the PIC through this buffer. An internal bus connects the data bus buffer to the interrupt registers and logic circuitry.

Interrupt Priority Logic and Registers. This circuitry determines the priority of interrupts that are sent to the processor. This circuit block contains the priority logic and three associated registers:

- Interrupts Requesting Service
- Interrupts In-Service
- Interrupts priority mask

The priority logic decides which interrupt bit (INT0-INT7 in Requesting Service register) has the highest priority. This bit is strobed into the corresponding bit position in the In-Service register. Firmware uses the third register to mask the INT0-INT7 bits in the Requesting Service register. This masking changes the priority of the INT0-INT7 interrupt signals.

Control Logic. When the system signal INTA goes active low, it causes the control logic to transmit a service routine address to the Processor Bus via the Local Data Bus buffer. The control logic, also, issues INT if it receives a signal from the Interrupt Priority Logic.

Read and Write Logic. OBIO8&A goes active low to enable reading or writing access to the PIC. If RD goes active low, any of the three registers and the interrupt level of the Interrupt Priority Logic circuitry can be output to the Processor Board Data Bus. If AWT goes active low, firmware can write PIC control words to registers in the read and write logic circuitry. A0 selects, in conjunction with RD and AWT, whether the interrupt registers or the command word registers are read from or written to.

Cascade Buffers and Comparator. If other PICs are added to the system, this circuitry addresses them. These "slave" PICs are controlled by the "master" PIC on the Processor board. AD8-AD10 carries the address of any one of eight additional PICs.

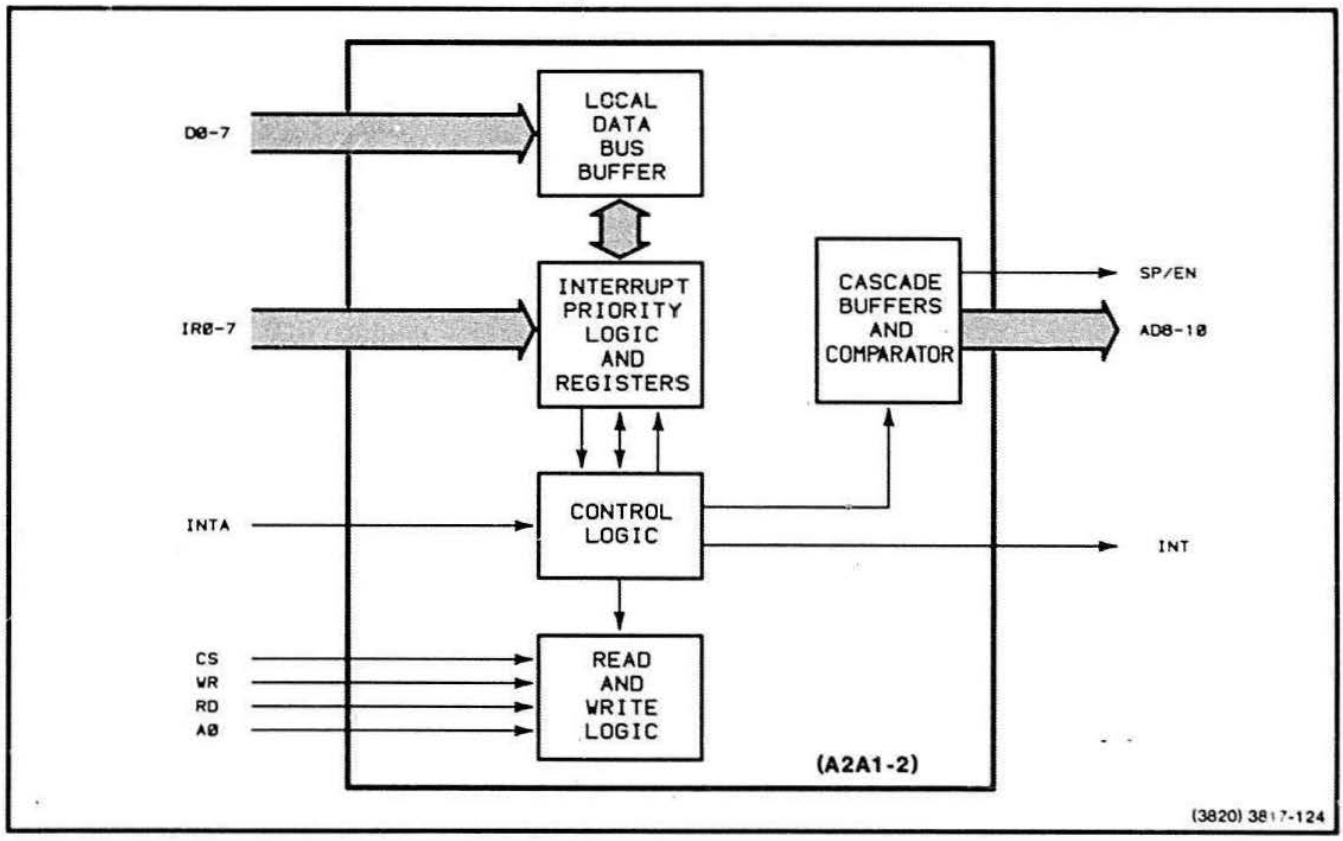


Figure 5-4. Programmable Interrupt Controller Block Diagram.

PIC Operations

There are two phases of operation in the PIC: initialization and normal operation. During initialization, soon after the terminal is turned on, the system firmware sends PIC setup data and control words to the PIC. After initialization, the PIC is ready to receive and prioritize the interrupt request signals on INT0-INT7.

The Interrupt Operating Sequence. The following sequence of events occurs in the normal operation of the Interrupt Controller circuitry.

1. One or more of the INT0-INT7 bits goes active low. This sets (because of the inverter) the corresponding bit(s) in the "interrupt request" register in the Interrupt Priority Logic circuitry in the PIC.

2. The PIC determines the priority of these INT0-INT7 bits, and sends INT to the MPU if a higher priority interrupt request is present than any currently being processed.

3. The MPU receives the INT signal and responds with a low on its INTA line.

4. The PIC now sets the highest priority bit in its in-service register and the corresponding interrupt request register bit is reset. No signals are sent from the PIC at this time.

5. Now the MPU sends a second low on INTA. This causes the PIC to place an eight-bit interrupt service routine ("vectoring") address on the Local Data Bus, D0-D7.

6. The MPU reads this vectoring address on the processor data bus and begins the service routine. The Interrupt Controller is now done with this interrupt cycle.

If the duration of an interrupt request on INT0-INT7 is not long enough to be active low at Step 4, the PIC automatically issues a vectoring address as if INT7 were active low.

1STINTA and Cascade Addresses for Slave PICs. During the interrupt sequence the MPU sends two INTA signals. At the time of the first INTA, 1STINTA is generated by a toggling JK flip-flop and a negative logic NAND gate. At the time of the second INTA, the toggling JK flip-flop and another NAND gate drive the cascade addresses of the PIC onto the Local Address and Data Busses.

Address Drivers

The address drivers first latch 20 bits of address and BEHN. The drivers then place these 21 bits onto the Local Address Bus (during a *local* read or write), or onto the Processor Bus (during a *system* read or write).

The Address Drivers consist of six packages of D-type latches. These form two sets of latches. One set outputs LS0-2, LBHE, and the Local Bus address bits; the other set outputs BHEN and the Processor Bus address bits.

When the MPU outputs address information on AD0-AD19 and ALE makes a high-to-low transition, the Local Bus latches latch this data. They also latch S0-S2 and BHE. Since this set of latches is permanently enabled for output, the latched data appears immediately as A0-A19, LS0-LS2, and LBHE.

The Processor Bus set of latches operates like the Local Bus set except that the Processor Bus latches are not permanently enabled for output. BUSAEN provides this enabling function.

Data Drivers/Receivers

This block latches 16 bits of data information from AD0-AD15 (the MPU Bus) and converts this data to D0-D15 (the Local Data Bus), or DAT0-DAT15 (the Processor Data Bus).

Four bus transceivers and one NAND gate make up the Data Drivers/Receivers circuitry. The bus transceivers are divided into two sets. One set handles D0-D15, the Local Data Bus, and the other set handles DAT0-DAT15, the Processor Bus. Data bits are transmitted and received in each set.

If OBDEN goes active low and DT/R-0 is high, the data bits on AD0-AD15 are transmitted to D0-D15. But if OBDEN is low and DT/R-0 goes low, data on D0-D15 is transmitted back through the transceivers and becomes AD0-AD15, which is received directly by the MPU.

Data is transmitted to the Processor Data Bus, DAT0-DAT15, when DT/R-0 goes high and both DEN and SP-0/EN-0 are high. If DT/R-0 is low during data transmission, the Processor Bus bits become AD0-AD15.

Bus Command Driver

The Bus Command Driver decodes MPU status signals to generate system bus read, write, and interrupt commands. Also, this driver generates control signals for the Processor board address and data drivers and latches.

The Bus Command Driver circuitry consists solely of the Bus Controller. This device combines control logic, MPU status decoder, control signal generator, and command generator circuitry. Figure 5-5, Bus Controller Block Diagram, shows the signal paths among these blocks of circuitry.

Control Logic. IOB is permanently tied low. This sets up the control logic so that it enables the command generator to output command signals (AIOWC, MWTC, MRDC, etc.) no sooner than 105 ns after BUSAEN goes active low. When BUSAEN is high, the control logic tri-states the command signal outputs (places them in a high impedance condition).

OBADR also affects command signal output. When OBADR is active low all command signal outputs (in addition to the DEN and MCE outputs) are inactive. If OBADR goes inactive high, these same outputs are enabled.

CLK synchronizes the operations within the Bus Controller.

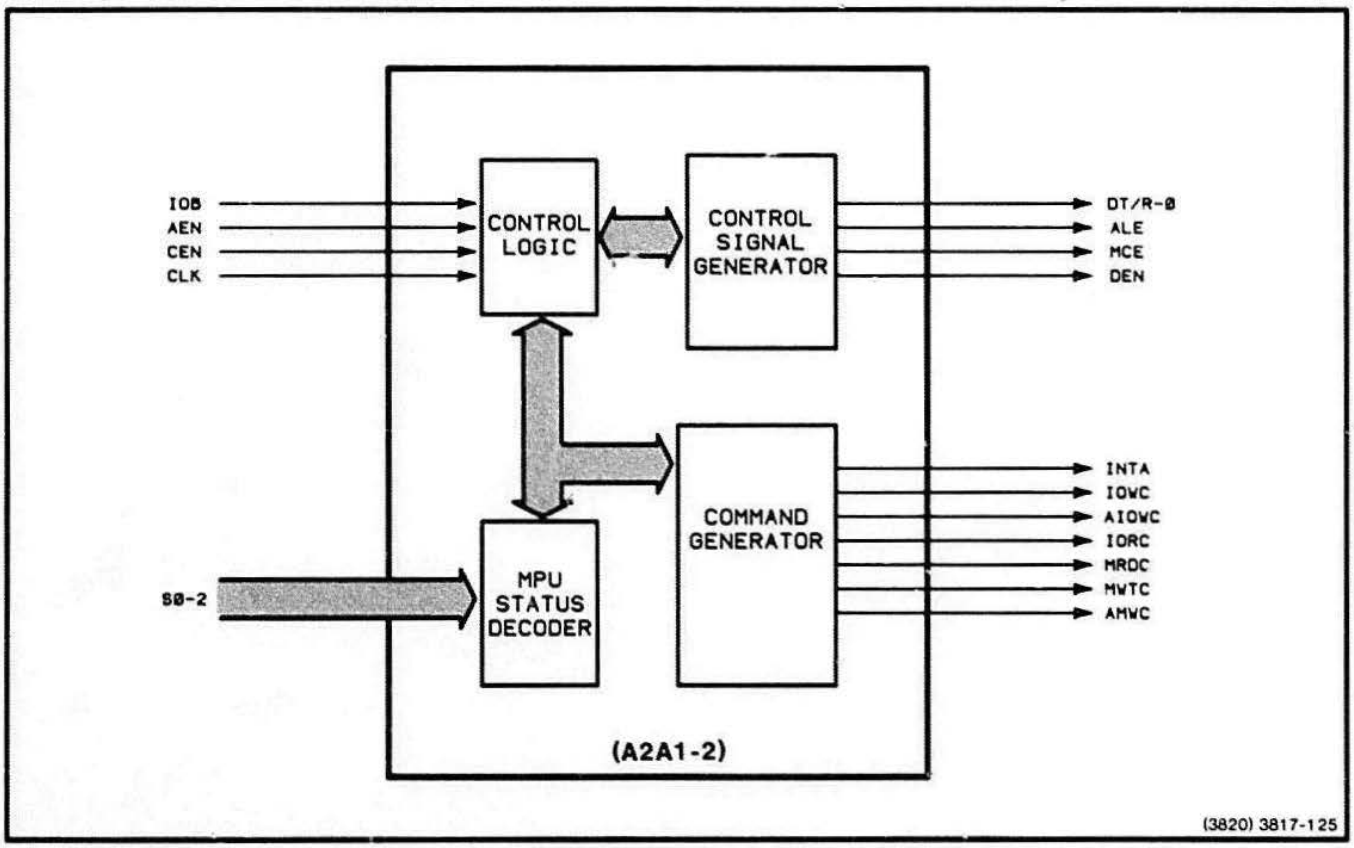


Figure 5-5. Bus Controller Block Diagram.

MPU Status Decoder. This circuitry decodes the S0-S2 signals from the MPU. These lines indicate the eight different states that the MPU can be in. Table 5-2 shows the MPU state and the command signal for each bit combination. The command signals are output only when the corresponding S0-S2 bit combination is present.

Table 5-2

STATUS WORD AND BUS CONTROLLER COMMANDS

S0	S1	S2	Processor State	Bus Controller Command
0	0	0	Interrupt Acknowledge	INTA
1	0	0	Read I/O Port	IORC
0	1	0	Write I/O Port	IOWC, AIOWC
1	1	0	Halt	none
0	0	1	Code Access	MRDC
1	0	1	Read Memory	MRDC
0	1	1	Write Memory	MWTC, AMWC
1	1	1	Inactive	none

Control Signal Generator. This part of the Bus Controller outputs DT/R, ALE, MCE, and DEN. These signals control, respectively, direction of data transmission, enabling of the address latches, enabling of AD8-AD10 (additional Interrupt Controller addresses), and enabling of Processor Bus Data Drivers if OBINTA is high.

When BUSAEN is low (MPU is bus master) and OBADR is high (MPU is not accessing a device on the Processor board), the Control Signal Generator activates its control outputs according to whether lines SO-S2 indicate a read, write, or interrupt cycle. See Figure 5-6, Bus Controller Timing, for the sequencing of these signals.

Command Generator. This circuitry outputs the command signals — MRDC, MWTC, IORC, IOWC, AMWC, AIOWC, and INTA. When BUSAEN is active low and OBADR is inactive high, the Command Generator outputs the command signals corresponding to the three bits of S0-S2. See Table 5-2, Status Words and Bus Controller Commands, for this relationship.

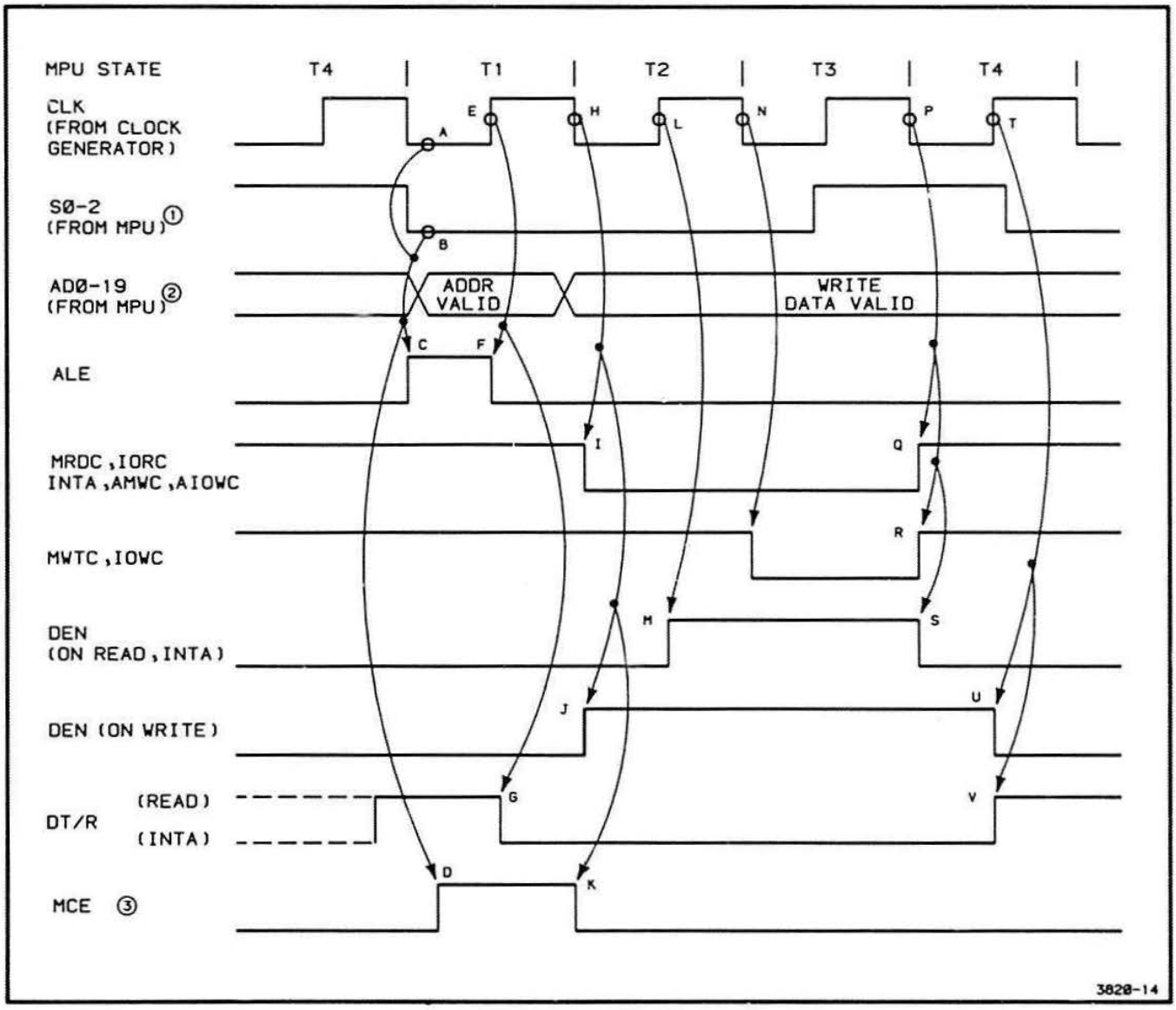


Figure 5-6. Bus Controller Timing.

ROM

The ROMs circuit block holds a maximum of 32K bytes of system firmware; the ROMs output this coding to the Processor Bus when they are addressed.

ROM Configuration. The ROM circuitry is made up of eight ROM integrated circuits, arranged in four banks of two ROMs each. The four banks supply a total of 32K bytes. Each bank contains 4K by 16 bits of I/O address space. The bottom half of each bank outputs D0-D7 and the top half outputs D8-D15.

Firmware. Starting from the left-most bank on the schematic, the first three banks contain system firmware in masked ROMs. The fourth bank contains a firmware "jump table" and the "patch code" in erasable/programmable ROMs (EPROMs).

Straps. There are three kinds of straps that affect the operation of the ROM circuitry:

- ROM-type selection straps
- ROM wait-states strap
- Two ROM address-decoding straps

The ROM circuitry is designed to accept a variety of different ROM integrated circuit packages. A chart specifying these different ROMs is located on the schematic itself (Schematic A5A1-3). The chart also specifies the positions required for each kind of ROM.

Cut strap W475 selects the number of ROM wait states that the MPU inserts between states T3 and T4. If the strap is not altered, the MPU inserts one wait state. This allows the use of ROMs with chip select access times of up to 580 ns. However, if all the ROMs on the Processor board have an access time of 380 ns or less, strap W475 may be altered so that the MPU inserts no wait states between T3 and T4. This latter position, of course, increases the speed of ROM accesses.

The straps at W126 in effect allow some or all of the ROMs' memory to be diverted from local use on the Processor board for use by the system. There are three positions for the straps. See Appendix B, *Strap Information*, to determine the positions for each of the three straps. If the straps are not altered, all 32K bytes of the ROMs are addressed in the range X'F8000' to X'FFFFF'. However, the straps may be altered to two positions. In one position, only ROMs addressed in the range X'FC000' to X'FFFFF' output data to the MPU Bus (AD0-AD19). In the other position, there is no Processor board ROM space — all memory space is accessed via the main Processor Bus.

The ROM circuitry receives an address from the MPU and puts the data for that address on the MPU Bus. When the MPU reads from a ROM bank, this sequence of events takes place:

1. An address from the MPU is latched by the Address Driver circuitry.
2. The Address Decoding circuitry determines whether it is a Processor board ROM address, which is any address in the range X'F8000' to X'FFFFF'. If the address is in this range, Address Decoding drives OBROM active low.
3. The bank decoder selects one ROM bank in response to A13 and A14 in addition to ALE, LS1, LS2, and A15-19. See Figure 5-7, ROM Bank Decoder Logic and Table 5-3, Selection Bits for ROM Banks, for an exact description of how the bank decoder works.
4. The two ROMs in the selected ROM bank place their data on the Local Data Bus lines, D0-D15.
5. The Data Drivers/Receivers pass this data on to the MPU.

Table 5-3

SELECTION BITS FOR ROM BANKS

Banks	Address Bits							
	A19	A18	A17	A16	A15	A14	A13	A12
F8000	1	1	1	1	1	0	0	X[a]
FA000	1	1	1	1	1	0	1	X
FC000	1	1	1	1	1	1	0	X
FE000	1	1	1	1	1	1	1	X

[a] "X" is the "don't care" condition.

Non-Volatile RAM

Non-volatile RAM stores various initialization and system parameters in 512 bytes of CMOS RAM.

Four 256 X 4 CMOS RAMs combine to give a total memory capacity of 512 bytes. Also included in this circuitry are six logic gates that decode various input signals that control reading and writing access.

When power to the terminal is shut off, this CMOS RAM retains its contents. A 2.4 V battery provides the trickle current to sustain CMOS memory.

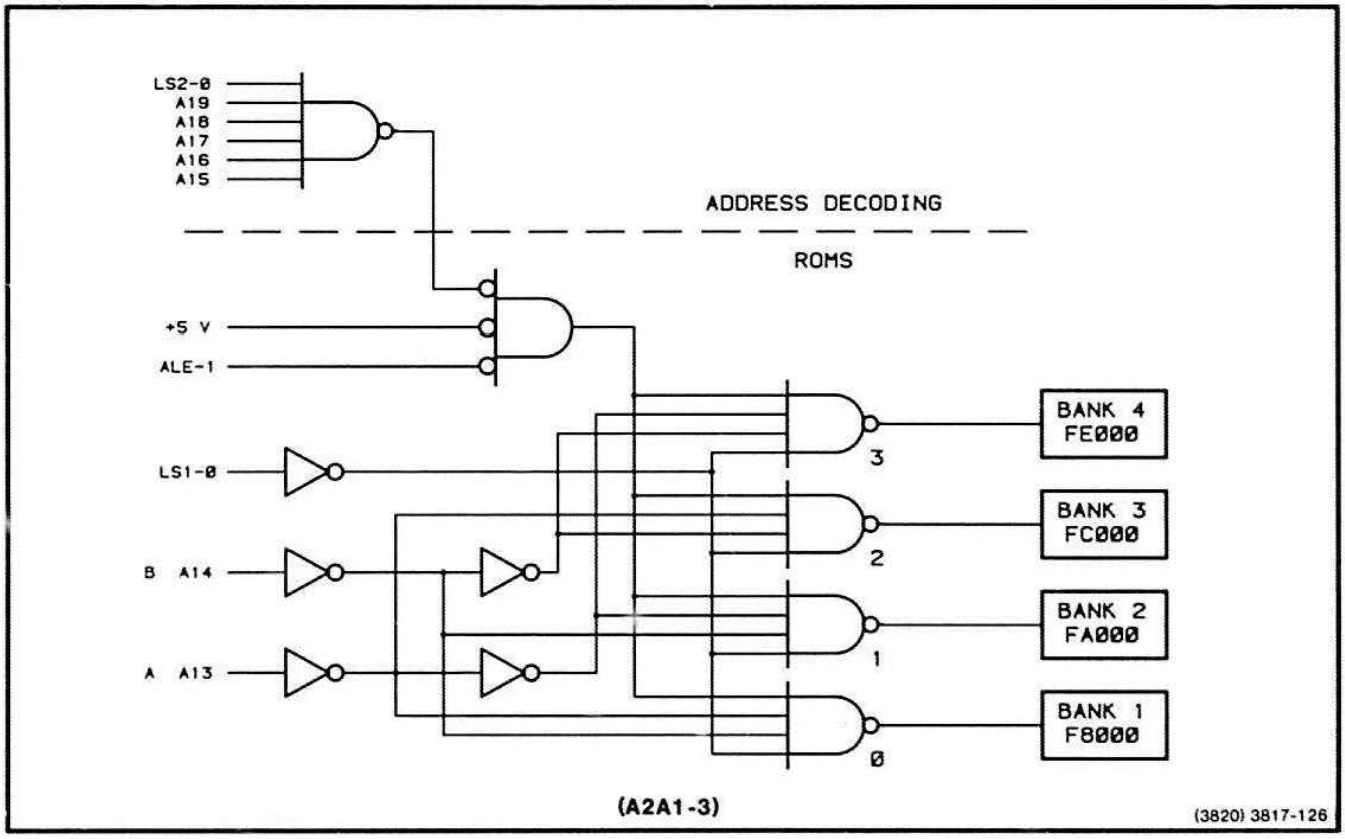


Figure 5-7. ROMs Bank Decoder Logic.

For the MPU to receive a RDY input from the Processor Bus, the AEN2-1 input must be low. This occurs under the following conditions:

- RDYAND is high
- BUSAEN is low
- At least one of the following is active low — INTA, AIOWC, IORC, MRDC, or ANWC

Once AEN2-1 is active low, an ACK1 going low triggers an RDY input to the MPU. Or, if the device sends ACK2 signals instead, the MPU receives an RDY input on the next positive edge of the CLK signal after ACK2 goes low.

Bus Transfer Logic

The Bus Transfer Logic allows the Processor board to gain control of the Processor Bus:

- To perform data transfers
- To relinquish bus mastership to other bus masters.

The Bus Transfer Logic enables the Processor board to respond to the bus transfer protocol that all users of the Processor/Display Bus must obey. (See *Control Transfer of Processor/Display Bus* in Section 4.) The Processor board is just one system device that can control the Processor Bus. The Processor board, along with the Display Controller and Disk Controller boards, are the "bus masters" of the Processor/Display Bus.

There are three JK flip-flops whose Q or Q-not outputs are the main output signals of this circuitry. (For the purpose of description, these flip-flops are called the BRQ, BUSAEN, and BUSY flip-flops from their Q or Q-not outputs.)

Note that three signals, CBRQ, BUSGRT, and BUSY, are both inputs and outputs of this circuitry The bus transfer protocol makes this necessary.

End-of-Data-Transfer Strap. Cutstrap W455 in the Microprocessor Timing Generator selects one of two signals that indicate the end of a current MPU data transfer. W455 should be strapped to Pins 2 and 3 only in a customized multiple processor-board system, where the MPU is not the microprocessor supplying the bus clock signal. (Note that cutstrap W456 should be open if the MPU is not supplying the bus clock signal.)

When the MPU begins a memory, I/O, or interrupt cycle, the Address Decoding circuitry drives OBADR low if the cycle is transferring data on the Processor board's Local Data Bus.

Since the MPU is not accessing the Processor Bus, BRQ goes or stays inactive high.

However, if OBADR is driven high, BRQ goes active low and the bus transfer logic is activated. At this point the MPU is in one of two states; it either controls or does not control the Processor Bus.

If it controls the bus, then, according to the protocol, the MPU has already caused BUSY to go active low and the MPU proceeds with its data transfer immediately, since it is currently bus master.

However, if the MPU does not currently control the bus, the following sequence of events occurs:

1. The BRQ flip-flop toggles high and drives BRQ and CBRQ both active low onto the bus.
2. When BUSY goes inactive high (bus is available) and BPRN goes active low (bus is granted to Processor board), the Bus Transfer Logic makes BUSGRT-0 active high, and BUSY active low (bus is busy and unavailable).
3. At the same time the BUSAEN flip-flop is preset by BUSY. This enables the Bus Controller to begin driving control signals onto the Processor Bus.
4. BUSY remains active low until the MPU is finished transferring data. Then BUSY goes inactive high if BPRN is inactive high. There are two ways to cause BPRN to go inactive high:
   - A higher priority bus master requests bus control by driving its BRQ signal active low. If this happens, the bus priority logic on the Motherboard causes the BPRN of the Processor board to go inactive high.

- A lower priority bus master requests bus control by making its CBRQ go active high. This causes the BRQ flip-flop to be reset to 0, which makes BRQ go inactive high due to the inverter. Thus, the Processor board no longer requests use of the Processor Bus.

If no other bus master needs the bus, the Processor board maintains control. This eliminates the time delay that would be caused by having to get control of the bus for every data transfer.

Address Decoding

The Address Decoding circuit decodes an MPU (or Local Bus) address, consisting of A4-A19, to determine what Processor Bus circuitry is currently being addressed.

The Address Decoding circuitry consists of a number of logic gates arranged in a combinational logic circuit that decodes the ranges of addresses shown in Table 5-4, Processor Board Address Enabling Signals. A 3-to-8 line decoder also forms part of the circuitry, and outputs the eight OBIOX&X signals.

Note that two sets of two multiple-input AND gates are marked off by dashed lines on the schematic. Address Decoding is designed to work with one or the other set present, but not both. Both sets of gates feed a three-input NAND gate which directly produces OBRAM. Ordinarily, the set with the four-input AND gates is present. This set decodes addresses in the range X'FE00' to X'FFFF' in I/O address space. CMOS RAM is located in this range. On the other hand, if another MPU is added to the system, the set with five-input AND gates is present. This set decodes addresses in the range X'00000' to X'001FF' in memory address space. This gives a secondary MPU access to local RAM.

Table 5-4

PROCESSOR BOARD ADDRESS ENABLING SIGNALS[a]

Addressed Circuit	Signal	Address Range (Hexadecimal)	
32K ROM	OBROM-0	MEMORY	F8000-FFFFF
CMOS RAM	OBRAM-0	I/O	FE00 & FFFF
Programmable Interrupt Controller	OBIO0&2-0	I/O	00E0 & 00E2
PCI	OBIO4&6-0	I/O	00E4 & 00E6
PCI	OBIO8&A-0	I/O	00E8 & 00EA
Keyboard Controller MPU	OBIOC&E-0	I/O	00EC & 00EE
Programmable Interval Timer	OBIO1&3-0	I/O	00E1 & 00E3
Programmable Interval Timer	OBIO5&7-0	I/O	00E5 & 00E7
RS-232 Interrupt Enable and Status A	OBIO9&B-0	I/O	00E9 & 00EB
Bus Timeout Reset and Status B	OBIOD&F-0	I/O	00ED & 00EF
Processor Bus	OBADR(-1)	MEMORY	00000-F7FFF
Processor Bus	OBADR-0	I/O	0000-00DF
Processor Bus	OBADR-0	I/O	8000-FDFF[b]

[a]With all straps set to their normal positions.

[b]The I/O address space range X'0100' to X'7FFF' is defined as "not accessible" in the 4112 address space configuration.

The MPU enters bus cycle T1; during this time it outputs an address (on lines AD0-AD19) and the MPU status (on S0-S2). The Address Drivers latch these signals on the trailing edge of ALE. If the address falls in one of the ranges of Processor board circuitry, the Address Decoding circuitry generates one and only one of the output signals in Table 5-4, in addition to OBADR active low. Once OBADR goes active low, it generates OBDEN in conjunction with the timing signals T3W4 and T4I. T3W4 essentially turns OBDEN on and T4I turns it off. Note that a Processor board interrupt by means of OBINTA can also cause OBDEN to go active low.

All of the OBIOX&X signals are generated by the 3-to-8 decoder. Since all of the addresses for these signals fall in the range X'00E0' to X'00EF', the decoding gates examine bits A4-A7 (which carry the binary 1110, or hexadecimal E). The 3-to-8 decoder has bits A0, A2, and A3 as inputs, but NOT bit A1. Thus, the decoder cannot distinguish between, for example, X'00E0' and X'00E2', so it outputs the same OBIOX&X signal for both addresses. For example, for X'00E0' and X'00E2', the decoder outputs OBIO0&2.

If MDEN goes active high, it disables both OBDEN and OBADR. This implies that the MPU cannot address either the Processor board or the main Processor Bus accessible locations. The 4110 Series Bus Test Fixture uses MDEN as an MPU disable feature.

Bus Timeout Detector

The Bus Timeout Detector detects when a Processor Bus slave device fails to respond with an acknowledge signal (ACK1) to a command from any master device. It drives ACK1 onto the Processor Bus and sets an error status bit (D8), which the MPU can read.

This circuitry consists of a 4-bit binary counter, a D-type flip-flop, and some logic gates. The QD output of the binary counter drives ACK1 through an open-collector driver. The Q output of the error flip-flop becomes D8 after it passes through an output-controlled line driver.

During a normal data transfer between any bus master and any slave device, one of the bus command lines goes low, enabling the 4-bit counter to begin counting. Because the programmable clock input signal, OUT0, is normally about 20 ms, the bus command is held low continuously for 160 ms before QD of the counter goes high. If this bus timeout condition occurs, QD sets the error flip-flop and drives ACK1 by means of an open-collector driver. This completes the handshake sequence for the non-responding or non-existent slave device.

If the bus commands are all less than 160 ms, the counter is always reset before it can drive QD high; thus, no bus timeout occurs.

Note that this circuit detects timeouts even when some other bus master is controlling the bus. In a multiple-processor board system, it may be desirable to disable the timeout function on one or more of the Processor Bus boards by cutting cutstrap W561.

Status Input

Status Input allows the MPU to read these Processor board status signals: BUSGRT, STEST, TIMR1, and bus timeout error.

The Status Input circuitry outputs STATEN active high if CMD is active high, LSO is inactive high, and OBIOD&F is active low. STATEN going active high enables two buffers, which place the following information on the indicated Local Data Bus lines:

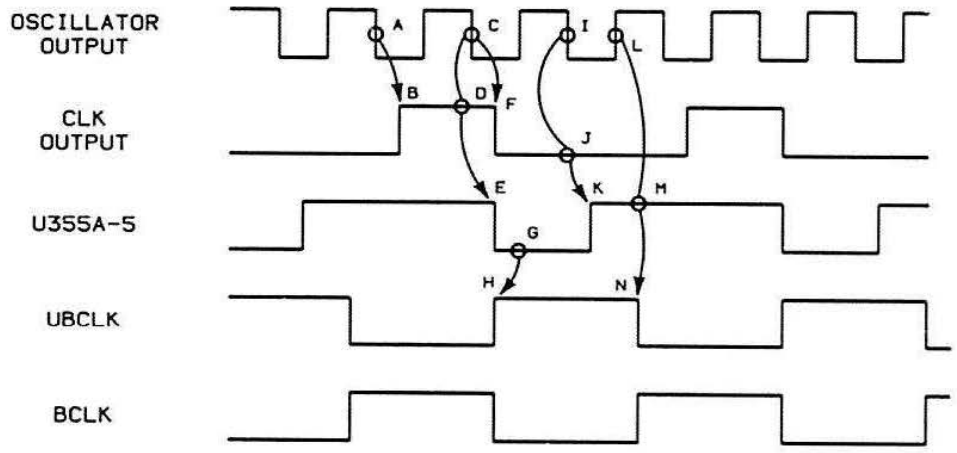
- D11 — BUSGRT
- D10 — STEST
- D9 — output of the Programmable Interrupt Timer
- D8 — bus timeout error

Bus Clock Generator

The Bus Clock Generator generates the 4.9152-MHz, 50% duty-cycle bus clock signal, BCLK, for the Processor board and Processor Bus.

The Bus Clock Generator consists of two JK flip-flops and two logic gates. A four-input NAND gate is used as a 50 Ω TTL driver to give extra drive to BCLK for the Processor Bus. The NOR gate is simply an inverter for the clock input to one of the JK flip-flops. (Cutstrap W456 can be cut to enable only one Processor board to generate BCLK in a multiple processor-board system.)

The Bus Clock Generator circuitry transforms a 50% duty cycle, 14.7456-MHz signal (OSC output) and a 33% duty cycle, 4.9152-MHz signal (CLK output) into two 50% duty cycle, 4.9152-MHz signals, UBCLK and BCLK. Figure 5-8, Bus Clock Generator Timing, shows the timing relationships among the signals in the circuitry.



NOTES:

A,B The trailing edge of OSC causes CLK to go high.

C,D,E The trailing edge of OSC and a high on CLK cause Pin 5 of the U355A JK flip-flop to go low.

C,F The trailing edge of OSC causes CLK to go low.

G,H A low level on U355A-5 causes UBCLK to go high.

I,J,K The trailing edge of OSC and a low level on CLK causes U355A-5 to go high.

L,M,N The leading edge of OSC and a high level on U355A-5 causes UBCLK to go low.

3820-17

Figure 5-8. Bus Clock Generator Timing.

MPU Timing Generator

The MPU Timing Generator provides MPU timing information for other circuitry on the Processor board.

The MPU performs memory and I/O transfers by going through bus cycles. Each bus cycle consists of at least four clock states, which are called T1, T2, T3, and T4. Sometimes, Tw or wait states, are inserted between T3 and T4. Also, Ti, or idle states, are sometimes inserted between bus cycles. The MPU Timing Generator makes this information available to other circuitry on the Processor board.

The MPU Timing Generator comprises four logic gates and an IC composed of four D-type flip-flops. The interconnections among the four D-type flip-flops are shown in Figure 5-9.

The circuit is basically a shift register. At the end of a bus cycle, the D input of flip-flop #1 is a logical one. When the next bus cycle begins, ALE resets all four flip-flops during T1. Next, T2 is entered and the Q output of flip-flop #1 becomes a logical one. This condition turns AWT active low. During T3, the Q output of flip-flop #2, which is T3W4, goes active high, because it is connected directly to the Q output of flip-flop #1. After T3, it enters the Tw state unless or until MPU status bits S0-S2 become all logical ones. Then, in state T4, the Q-not output of flip-flop #3, which is T4I, goes active low. The MPU Timing Generator stays in state Ti until the MPU issues another ALE during T1.

Table 5-5

MPU STATE AND MPU TIMING GENERATOR SIGNALS

Signal Name	MPU Clock State					
	T1	T2	T3	Tw[a]	T4	Ti[a]
(T123W)	True	True	True	True	False	False
(T23W)	False	True	True	True	False	False
T3W4	False	False	True	True	True	False
T4I	False	False	False	False	True	True

[a]Note that there may be multiple Tw and Ti states.

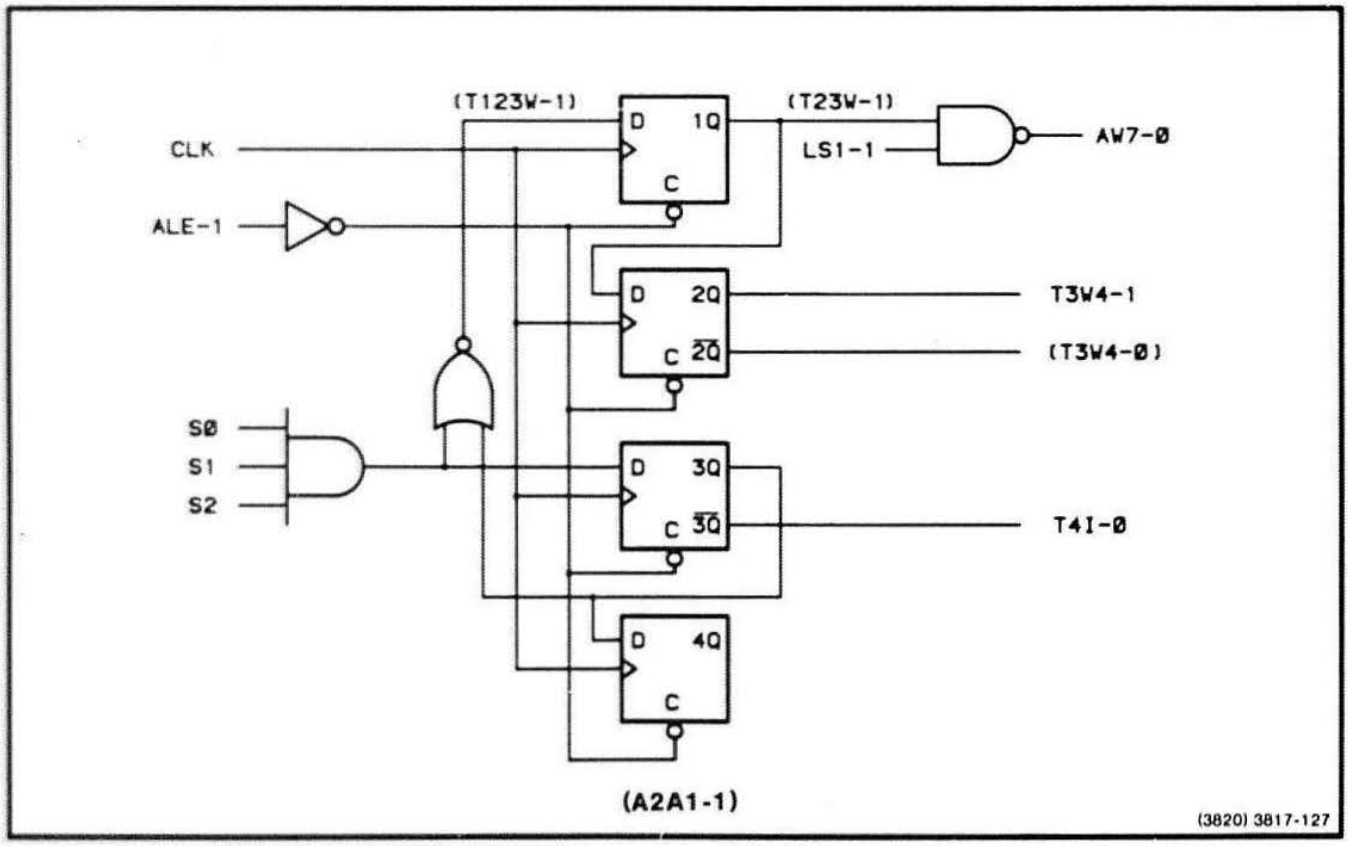


Figure 5-9. MPU Timing Generator Circuitry.

Programmable Timer and Baud Rate Generator

The Programmable Timer and Baud Rate Generator have three programmable counters, inside a Programmable Interval Timer (PIT), that generate timing signals to produce:

- The transmit baud rate in the RS-232 Communications Interface logic
- TIMR1, which can generate an interrupt signal to the MPU
- OUT0, the primary firmware interrupting timer and timing source for the bus timeout detector

These timing signals prevent the bus from "hanging."

The Programmable Timer and Baud Rate Generator consist primarily of the Programmable Interval Timer (PIT). The PIT has three internal 16-bit counters numbered 0, 1, and 2. It also has a has a data buffer and read/write circuitry.

The Programmable Timer and Baud Rate Generator also have one positive AND gate and one 4-bit binary counter. The AND gate combines OBIO5&7 and OBIO1&3 to operate the chip select input of the PIT. The counter produces two signals by dividing the buffered bus clock signal (BBCLK) by two and eight. BBCLK-divided-by-two is input to the Number 2 counter of the PIT and BBCLK-divided-by-eight is input to the Number 0 and 1 counters of the PIT.

Programmable Interval Timer. There are three main blocks of circuitry in the PIT: three 16-bit down counters, an 8-bit data bus buffer, and read/write logic.

The three counters operate independently and each has its own output (O0, O1, O2). Commands from the system (or possibly other) firmware completely control the operation of these counters. The firmware loads each counter with an initial value. Firmware commands can also read the counter value at any time during its down count.

The data bus buffer is connected to D8-D15, part of the Local Data Bus. Firmware commands, initial counter values, and read-out counter values pass through this buffer.

The read/write logic is turned on by the chip select input to the PIT. The local Processor Bus signals, RD and AWT, control the direction of data flow in the data bus buffer. A1 and A2, which are part of the Local Address Bus, select which of the three counters that commands and counter values are directed to.

The PIT has two phases of operation: initialization and normal operation. Initialization occurs shortly after the 4112 is turned on (though initialization commands may be given after this time).

After power-up, the MPU initializes the PIT as follows: either OBIO1&3 or OBIO5&7 goes active low to enable the PIT, and A1 and A2 select counter 0, 1, or 2. AWT goes active low, which enables firmware commands and counter values to program the selected counter via D8-D15. After all three counters are programmed, initialization is complete.

Note that there is no reset pin on the PIT, and that after the Processor Bus INIT signal goes high inactive and before the MPU initializes the PIT, outputs O1, O2, and O3 are undefined and may be stable high, low, or clocking.

In normal operation, a count value may be read from one of the counters. In this case RD goes active low after the PIT and the appropriate counter are selected. The counter value then appears on D8-D15.

Also in normal operation, output 2 (O2) produces the baud rate signal for the RS-232 Communications Interface, output 1 (O1) produces TIMR1 (which is used by the MPU Control circuitry in combination with a number of other interrupt-type signals), and output 0 (O0) produces OUT0 (which serves as both the primary interrupting firmware timer and as the clock source for the bus timeout detector).

RS-232 State Change Detector

The RS-232 State Change Detector detects state changes on the incoming RS-232 status lines (DSR, DCD, SDCD, CTS, and RING) and generates an interrupt (TIMERINT) when any of these change state.

This circuitry consists of a 4-input line receiver, a 6-input D-type flip-flop (latch), a bus driver, a 6-bit comparator, and part of another 4-input line receiver. (The five capacitors connected to the line receivers prevent voltage spikes on the RS-232 status lines from being transmitted to the RS-232 State Change Detector circuitry.)

The MPU interacts with the RS-232 State Change Detector in two ways. It first receives an interrupt and then determines what caused the interrupt.

The RS-232 status signals (DSR, DCD, SDCD, CTS, and RING) are input to the last state latch and to the comparator. (Note also that the O0 out of the Programmable Interval Timer in the Programmable Timer and Baud Rate Generator block makes up the sixth input to the comparator and latch.) The six outputs of the latch are routed to the bus driver and to the other half of the magnitude comparator. Thus the comparator compares these outputs of the latch with its inputs.

Suppose any one of the RS-232 status lines (or the O0 output of the PIT) changes state. The comparator then outputs an active low on (Y), which activates a NAND gate in the RS-232 Communications Interface. This causes TIMERINT to go active low. After TIMERINT is processed by the Interrupt Controller, the MPU eventually receives an interrupt.

At this point the MPU needs to determine which RS-232 status line (or O0 from the PIT) caused the interrupt. The MPU now reads either the "old" status lines or the "new" ones. To read the "old" status lines that exist at the outputs of the latch, it addresses the RS-232 State Change Detector, which causes OBIO9&B to go active low. Also, A1 must be active high. Now RD strobes, causing the Bus Command Driver to drive the status line data onto the Processor Bus. To read the "new" status lines, OBIO9&B goes active low again, but this time A1 goes low. Now, the latch is clocked, and the Bus Command Driver drives the inputs ("new" status lines) of the latch onto the data lines of the Processor Bus. From here, firmware determines which status line caused the TIMERINT interrupt.

RS-232 Communications Interface

The RS-232 Communications Interface transmits and receives RS-232 characters and control ("handshake") signals. The RS-232 interface contains the receive Baud Rate Generator, which is different than the transmit Baud Rate Generator discussed earlier.

This circuitry consists of a line driver, a line receiver, a number of logic gates, and a fancy USART, the Programmable Communications Interface (PCI). The PCI is the heart of the interface circuitry and is described next.

Programmable Communications Interface. This integrated circuit performs the parallel-to-serial data conversion for data sent to the host computer and also the serial-to-parallel conversion for data sent to the terminal. The PCI also has a programmable baud rate generator. In order to perform these functions, the PCI has the following circuitry (see Figure 5-10 for the PCI block diagram):

- Local Data Bus Buffer. D0-D7 are input and output via this 8-bit data bus buffer. Firmware commands, status information, and data are transferred through the buffer.

- Modem Control. Two "handshaking" signals, DTR and RTS, are sent directly to the host computer or modem from this block. TXEMT-0/DSCHG-0 also originates here, and when low, indicates that the transmitter has completed the parallel-to-serial conversion of the last character loaded by the MPU. Note that DSR-0, CTS-0, and DCD-0, which are generated in this circuitry, are permanently tied low.

- Control Functions. By responding to A1-2, LSI, OBIO0&2, OBIO4&6, and CMD, this circuitry controls when the PCI is written to and read from. Also, this circuitry controls the overall PCI internal operation. In addition, there are internal registers whose contents are manipulated by firmware commands.

- Baud Rate Generator and Clock Control. UBCLK provides the source frequency for the internal baud rate generator. Usually, the transmit baud rate is generated by output O2 from the PIT and the receive baud rate is generated from the internal baud rate generator and a software-selectable register value. However, 1X baud rate clocks from the modem may be selected for either the receive rate, transmit rate, or both. For external transmit clocks, TCLK is converted to TTL levels, multiplexed with the PIT O2, and input to (TXC-0). For external receive clocks, RCLK is converted to TTL levels, and input directly to (RXC-0), since the signal is multiplexed internally with the internal baud rate generator.

- Transmitter. The holding register receives data from the MPU and passes it to the shift register. Start, stop, and parity bits are added to the data according to the current communication parameters. The data is then output serially and becomes TDATA.

- Receiver. The shift register receives serial data on RDATA. This passes to the holding register and bits or characters are checked according to the current communication parameters. The data is then output to the MPU during a read of the data register.

Before the RS-232 Communications Interface can send and receive data, its operating parameters must be set by a combination of firmware and software commands and values. Communications parameters like synchronous or asynchronous mode, receive baud rate, parity, number of bits per character, etc., are sent to the PCI shortly after the terminal is powered up. Once this programming of values is done, normal data communication begins.

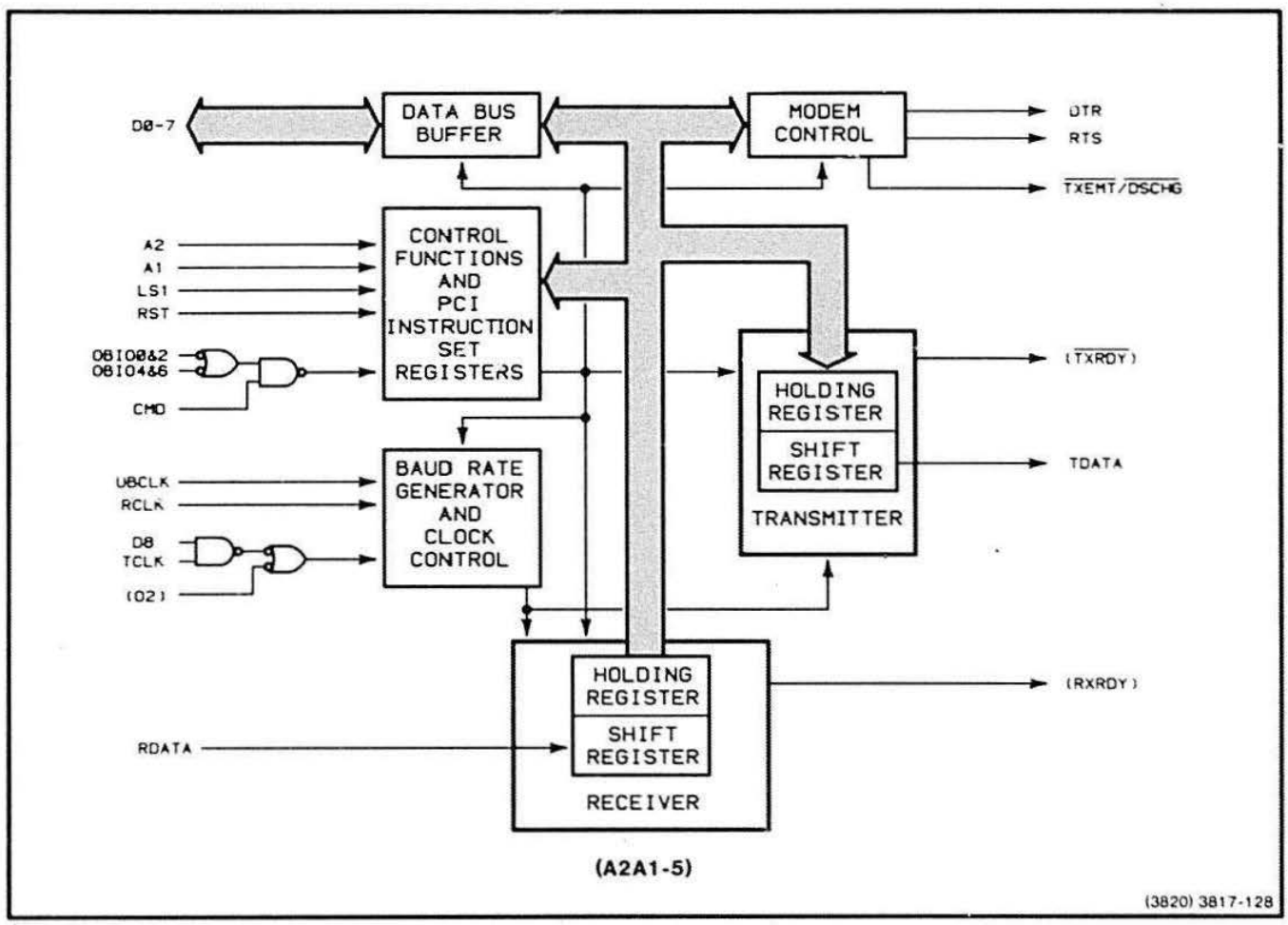


Figure 5-10. Programmable Communications Interface Block Diagram.

MPU Control. The MPU controls the PCI by activating A1-2, LS1, OBIO0&2, OBIO4&6, and CMD. The bit pattern of A1 and A2 together determine which of four registers in the control function circuitry is selected to be read from or written to. The MPU first selects the PCI by causing OBIO0&2 or OBIO4&6 to go active low, and CMD to go active high. LS1 is low for a read operation and high for a write operation.

Data Communication. Serial data on RDATA is input on the RS-232 cable (via P102). The data is then converted to TTL levels by the line receiver and fed to the (RXD) input of the PIC. Serial data is output to the line driver and becomes TDATA on the RS-232 cable (via P102). The PIC determines when to output DTR and RTS for modem control also on P102. Note that SRTS is controlled by the MPU directly and is latched, inverted, and level-converted before it reaches P102. (SRTSC — the usual strap setting — may be strapped to produce SRTSA if the modem requires it.)

Interrupts. The signals (TXEMT-O), (TXRDY-O), and (RXRDY-O) are status signals from the PCI that can generate interrupts to the MPU. All three signals are inverted and ANDed with interrupt enable-type signals from the latch. This allows the MPU to disable the PCI interrupts.

Keyboard Controller

The Keyboard Controller scans the keyboard port for key and thumbwheel change data and informs the MPU if there is any activity. The Keyboard Controller also handles the LED and bell signals.

The main component in this circuitry is an 8-bit Keyboard Controller Microprocessor (KC-MPU). Firmware written in the instruction set of the KC-MPU enables it to transmit key change and thumbwheel data from the Keyboard and Thumbwheel boards to the MPU Data Bus. Also, keyboard LED and bell signals are transmitted from the Local Data Bus to the Keyboard circuit board.

Other Keyboard Controller components are: an 8-bit buffer, three inverters, and seven open-collector buffer gates. The 8-bit buffer is always enabled and buffers KD0-KD7 for the KC-MPU. Two of the inverters are placed between UBCLK and the clock inputs, X1 and X2, to provide extra drive for the inputs. The seven buffer gates drive KWR, KSTRB, KBDINT, and KA0-KA3 onto the Keyboard and Thumbwheel boards.

Keyboard Controller Microprocessor. The KC-MPU consists of these blocks of circuitry: control logic, timing, test logic, I/O ports 1 and 2, status register, data-out buffer, data-in buffer, and one large block that consists of all blocks that do not have direct inputs from or outputs to the Keyboard Controller. (See Figure 5-11.) Descriptions of the KC-MPU Circuit blocks follow:

- Control Logic. This logic produces internal instructions that accomplish a variety of internal control functions. The signals that determine these internal control functions are A1, AWT, RD, OBIOC&E, and RST. A1 enables the MPU to indicate to the KC-MPU whether the information on D0-D7 is data or a command. AWT, when low, allows the MPU to write data to the data-in buffer. RD, when low, allows the MPU to read data from the status buffer or data-out buffer. OBIOC&E enables the KC-MPU. RST resets various internal counters and status flip-flops. (Note that the (SS-0) and (EA) inputs, although they are inputs to the control logic, control functions that are effectively disabled since they are tied high and grounded, respectively.)

- Timing. UBCLK provides the 4.9152-MHz clock for an internal oscillator.

- Test Logic. (Test 0) has been "disabled" by tying it high, but (Test 1) is controlled by KBT1. A high on KBT1 can be read by firmware in the KC-MPU during testing. This testing is done at the time of manufacture of the 4112 terminal.

- I/O Ports 1 and 2. Although these ports can function as input and output ports, I/O Port 1 functions only as the input port for KD0-KD7 and I/O Port 2 functions only as the output port for KWR, KSTRB, KBDINT, and KA0-KA3.

- Status Register. This register is accessed by the MPU through D0-D7. This register stores status information that tells the MPU the type of information in the data buffers and whether it can (or should) read/write to or from the KC-MPU. The MPU reads the status register at I/O address X'00EE'.
- Data-Out Buffer. The MPU reads all data (key codes and thumbwheel position data) from the KC-MPU from this buffer. The data-out buffer I/O address is X'00EC'.
- Data-In Buffer. The MPU writes data and commands to the KC-MPU through this buffer. The data-in buffer I/O address is X'00EC'.

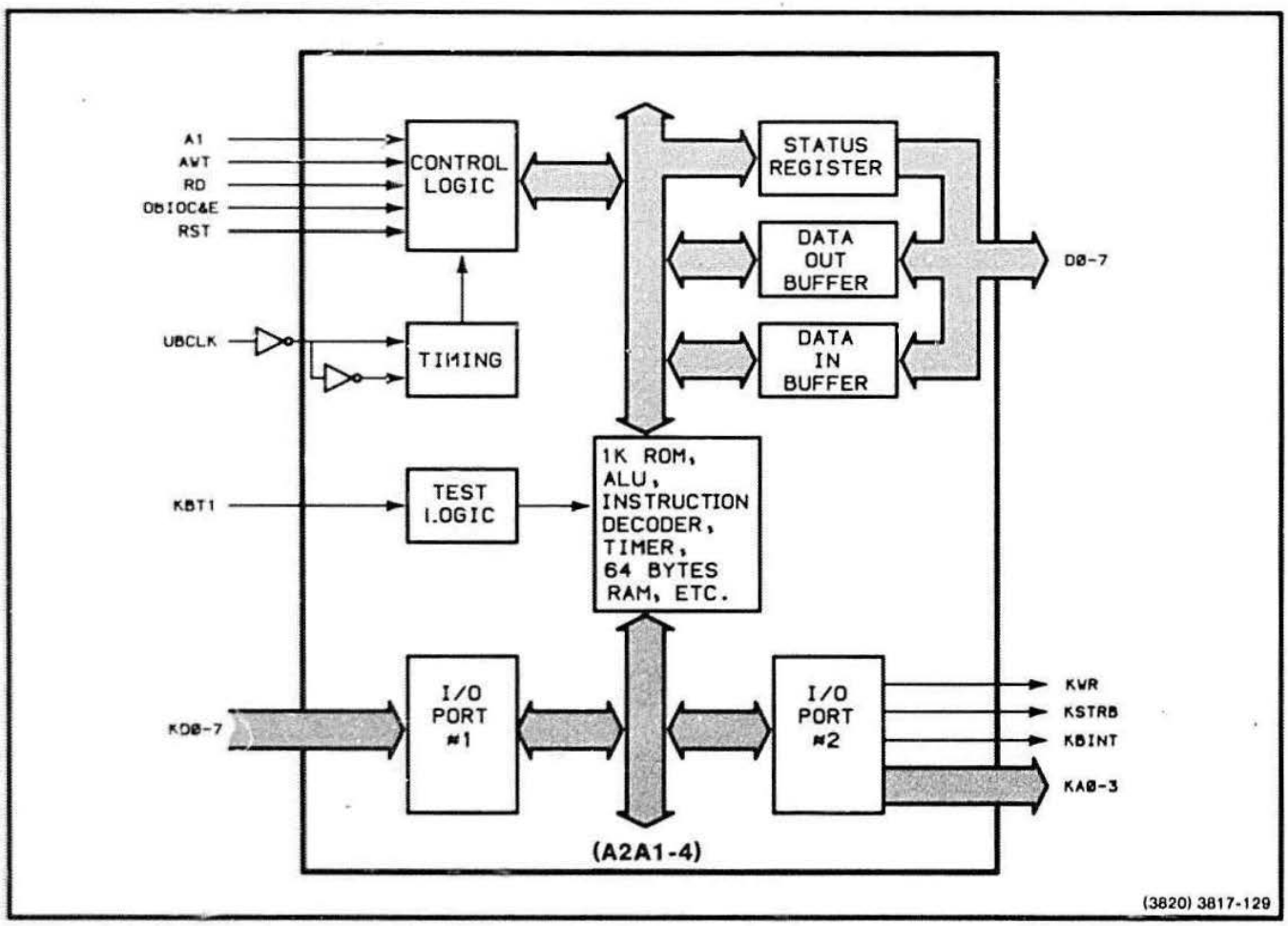


Figure 5-11. Keyboard Controller Microprocessor Block Diagram.

The KC-MPU has firmware routines masked into its 1K of ROM. These routines cause the KC-MPU to operate independently of the MPU. In addition to carrying out these routines, the KC-MPU responds to a set of commands that the MPU issues to it. These commands cause operations such as ringing the terminal bell, turning LEDs on and off, enabling keyboard interrupts, enabling and disabling the timer interrupt, resetting the KC-MPU, and inquiring about the installed keyboard language.

The KC-MPU passes three kinds of data to the MPU: keycodes, thumbwheel count values, and keyboard language identification data. The interactions between the MPU and KC-MPU are somewhat different for each kind of data.

Keycode Data. The KC-MPU has internal firmware that causes KA0-KA3 to scan the character decoder on the Keyboard. (See the Keyboard Thumbwheel circuitry description.) If the MPU has enabled the KC-MPU interrupt and if a key is pressed or released, the KC-MPU reads a keycode from KD0-KD7. The keycode is placed in the data-out buffer and the KC-MPU issues an interrupt on KBINT. Now, the MPU reads the status register to determine which of the three kinds of data the KC-MPU has for it. At this point, the MPU initiates a routine that reads the 8-bit keycode from the data-out buffer.

Suppose a key is held down. The MPU recognizes whether this is a valid repeating key and if it is, the MPU sends the command to enable the timer. The KC-MPU starts a 500-ms delay. If the MPU, within this delay, has not sent the command to disable the timer, the KC-MPU interrupts the MPU every 100 ms until the MPU sends the disable command (because the key was released).

Thumbwheel Count Values. Firmware routines in the KC-MPU scan the thumbwheel count values from the Thumbwheel board. When these routines detect a change in a thumbwheel count value (one counter each for the horizontal and vertical thumbwheels), the counter is adjusted and a KBINT is issued if 45 ms has passed since the previous KBINT. The MPU finds out from the status register that there is thumbwheel count data in the data-out buffer and reads it. Note that the MPU is interrupted only if the thumbwheels move, because the KC-MPU routines issue an interrupt only if there is a change in the counter value associated with either thumbwheel.

Keyboard Identification. When the terminal is turned on or reset, the KC-MPU places the keyboard status in the status register and the keyboard identification code in the data-out buffer. Also, the MPU itself can determine the keyboard identity at any time by sending a keyboard identification command to the KC-MPU.

LED and Bell. The LED on-off state and bell are controlled by sending commands to the KC-MPU. To turn a LED on or off, the MPU sends the address of the LED and the "on" or "off" command to the KC-MPU. The KC-MPU controls the timing once it gets the address and "on" or "off" command. The bell sounds when its address and the bell command is sent. The bell rings once for every bell command that is sent to the KC-MPU.

Introduction to the Keyboard

The previous discussion described the Keyboard Controller (located on the Processor board). The following theory section describes the operation of the keyboard's circuitry.

The keyboard consists of four blocks of circuitry that drive the LEDs (LED & Bell Logic), ring the terminal bell (Bell circuit), interface the thumbwheels to the character decoder (Thumbwheel Interface), and output character codes when keys are pressed or released (Character Decoder). See Figure 5-12.

LED & Bell Logic

The LED & Bell Logic lights the LEDs and rings the bell on command.

This circuitry turns on or off the terminal bell and any of eleven LEDs located on the terminal keyboard surface.

How a LED Changes State. The Keyboard Controller MPU (in the Keyboard Controller circuitry on the Processor board) sends a binary address from 000 to 111 on lines KA0-KA2. (Note that only seven addresses are needed on one 8-bit addressable latch and only five on the other.) This binary address is latched by the D-type flip-flops.

Now the KC-MPU sends the "on" or "off" information on lines KA0 and KA1. KA0 controls the state of any of the seven LEDs output from one of the 8-bit latches, and KA1 changes the state of the bell or other four outputs from the other 8-bit latch.

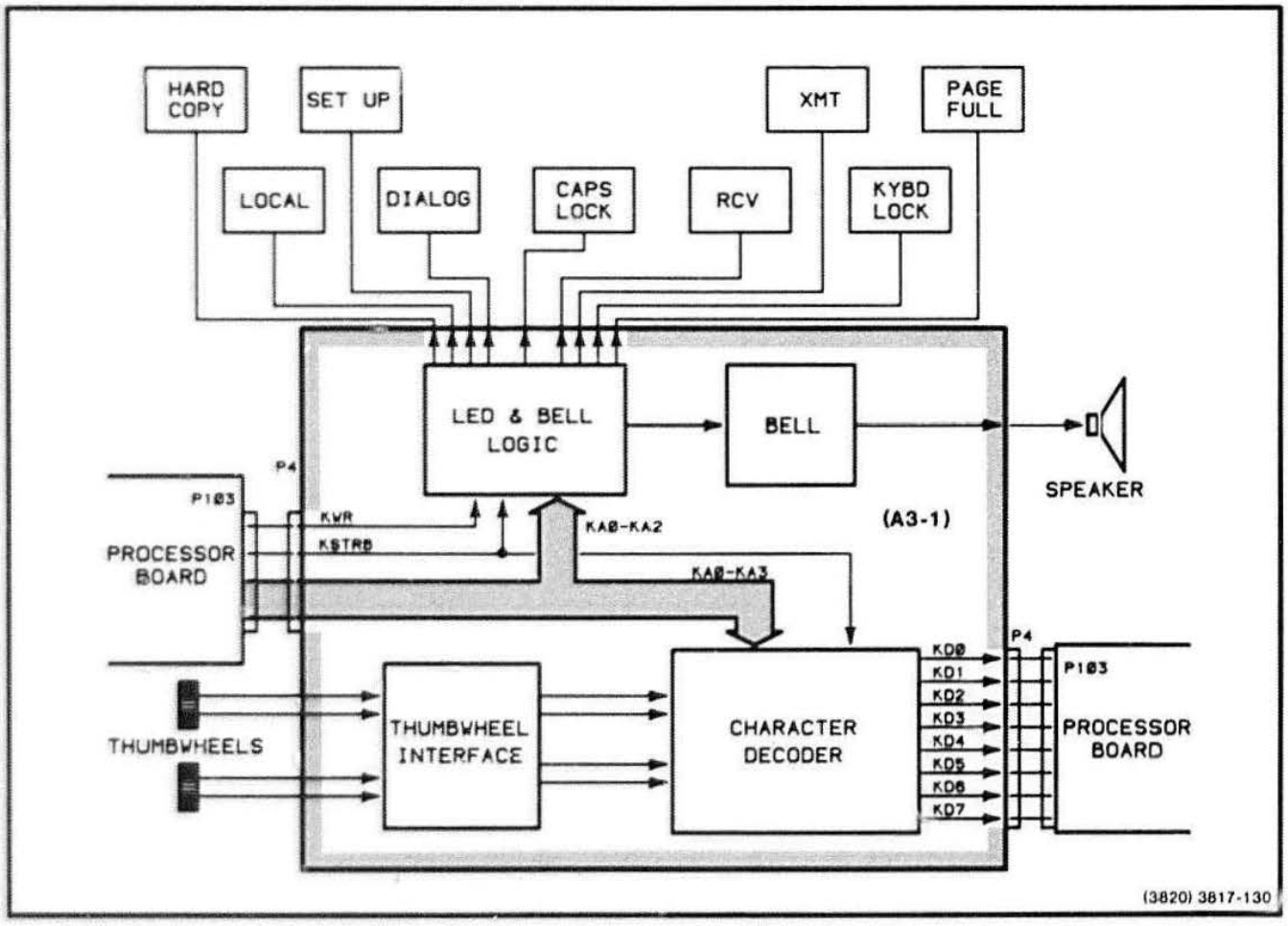


Figure 5-12. Keyboard Block Diagram.

KWR enables the KA0 or KA1 information to be latched by whichever latch is addressed.

Thumbwheel Interface

The Thumbwheel Interface changes the voltage of the thumbwheel output to TTL levels and gates the output to KD4-KD7 (keyboard data lines).

The inputs to this block are two sets of 2-bit Grey code. One set is output by the vertical thumbwheel, the other by the horizontal thumbwheel. The outputs of the block are the two sets of Grey code changed to TTL voltage levels.

Thumbwheels and 2-bit Grey Code. The thumbwheels operate identically so only one thumbwheel is described.

Rigidly attached to the shaft of the thumbwheel is a disk perforated with equally spaced slots. As the wheel is turned, a light (stationary with respect to the slotted disk) activates two phototransistors in this sequence:

- Both phototransistors on (00)
- One off, the other on (01)
- Both off (11)
- One on, the other off (10)

This sequence is the 2-bit Grey code. Each of the thumbwheels may output only these four states.

Interfacing of Thumbwheels to the KD4-KD7 Lines. The 2-bit Grey code signals from the thumbwheels have voltage levels outside TTL levels. Therefore, these signals are changed to TTL levels by four CMOS NAND gates. The outputs of these NAND gates connect to four TTL NAND gates. The outputs of the TTL NAND gates are passed to the row detector only when the X11 line of the column interrogator goes high. At this time, KD4-KD7 have valid thumbwheel 2-bit Grey code data on them.

Creating Key Change Data. The Keyboard Controller MPU on the Processor board needs two kinds of information to recognize that a key has been pressed or released. These two kinds of information correspond to the columns and rows of the key "matrix." Each key has a unique position at the intersection of a column and row in the matrix. So, when the KC-MPU receives both column data (KA0-KA3) and row data (KD0-KD7), it can determine which key has changed state.

The firmware driving the KC-MPU repeats the following sequence of operations for each column of the key matrix.

The KC-MPU outputs a low on KSTRB, which disables the outputs (KD0-KD7) of the row detector. Four bits of information representing a column of the key matrix are loaded onto lines KA0-KA3. (Note that only ten columns are used for the keys, one is not used, and the remaining column line is used in the Thumbwheel Interface logic.)

The column represented by the KA0-KA3 address data is interrogated. If a key in that column is pressed or released during the interrogation, the row detector IC senses this change. KSTRB then goes high and a low appears on a combination of the row signals (KD0-KD7) corresponding to the key position.

Bell

The Bell circuitry provides an audible tone that the programmer can use to alert the user.

This block has one input and one output. The input is from an output of an 8-bit addressable latch in the LED and Bell Logic circuitry. The output turns on or off a speaker mounted inside the terminal.

How the Bell Rings. To ring the bell, the Keyboard Controller MPU first sends a binary address (100) over KA0-KA2. Next a binary 1 (high) is sent on KA1. (See the previous discussion of *How a LED Changes State.*) This sequence activates the bell circuitry.

A 555 timer circuit is connected to form a free-running oscillator that generates a square wave signal of about 760 Hz. This 760-Hz signal feeds the base of a transistor connected in series with a Darlington amplifier. After the input to the Bell Logic (KA1) switches on the Darlington amplifier, current charges and discharges a capacitor connected across the speaker. The bell tone dies out because an RC network, connected to the base of the Darlington pair, times out after about one-half second.

Character Decoder

The Character Decoder detects whether a key has been pressed or released. It also detects the positions of both thumbwheels.

Each key of the keyboard changes capacitance when it is pressed or released, and each thumbwheel sends a 2-bit Grey code (described earlier in this section).

RAM/ROM BOARD THEORY

The following pages describe the general architecture and operation of the RAM/ROM board and then describe each block of RAM/ROM circuitry. The order of the block descriptions follows the basic information flow, from left to right, of the block diagram in Figure 5-13.

GENERAL DESCRIPTION

The RAM/ROM board supplies 32K bytes of RAM in addition to a maximum of 64K bytes (32K 16-bit words) of ROM-type memory.

The circuitry of the board consists of a dynamic RAM controller IC with support circuitry, one socket where the RAM Array board plugs in, and 16 ROMs with support circuitry. (The RAM Array board is a small circuit board that holds 32K bytes of dynamic RAM.)

GENERAL OPERATION

The RAM/ROM board performs these three basic operations:

- Reading the contents of a location in RAM
- Writing over the contents of a location in RAM
- Reading the contents of a location in ROM

To read the contents of a location in RAM, the bus master first drives the location address onto the Processor Bus, and then it issues a memory read command (MRDC). When the RAM Controller board receives an active MRDC signal, it responds by driving ACK2 onto the bus, and then the data from the address location.

To write over the contents of a location in RAM, the same sequence of events occurs except that AMWC replaces MRDC and the bus master drives the data onto the bus.

To read the contents of a location in ROM, the bus master follows a similar sequence of events as for a read from RAM. However, when the signals reach the board, they are routed through different circuitry. The RAM Controller, which is involved when a read from RAM takes place, is not involved in a read access from ROM.

RAM/ROM BOARD CIRCUIT BLOCK DESCRIPTIONS

Bus Receivers

The Bus Receivers receive signals from the Processor Bus and buffer them for the board.

The three bus receivers in this block are permanently enabled. This means that the outputs constantly follow whatever is on the Processor Bus. The board responds when the correct range of addresses and active read (MRDC-0) or active write (AMWC-0) signals appear on the Processor Bus.

RAM Control

The RAM Control circuitry performs these functions:

- Generates all control signals for the RAMs on the RAM Array board

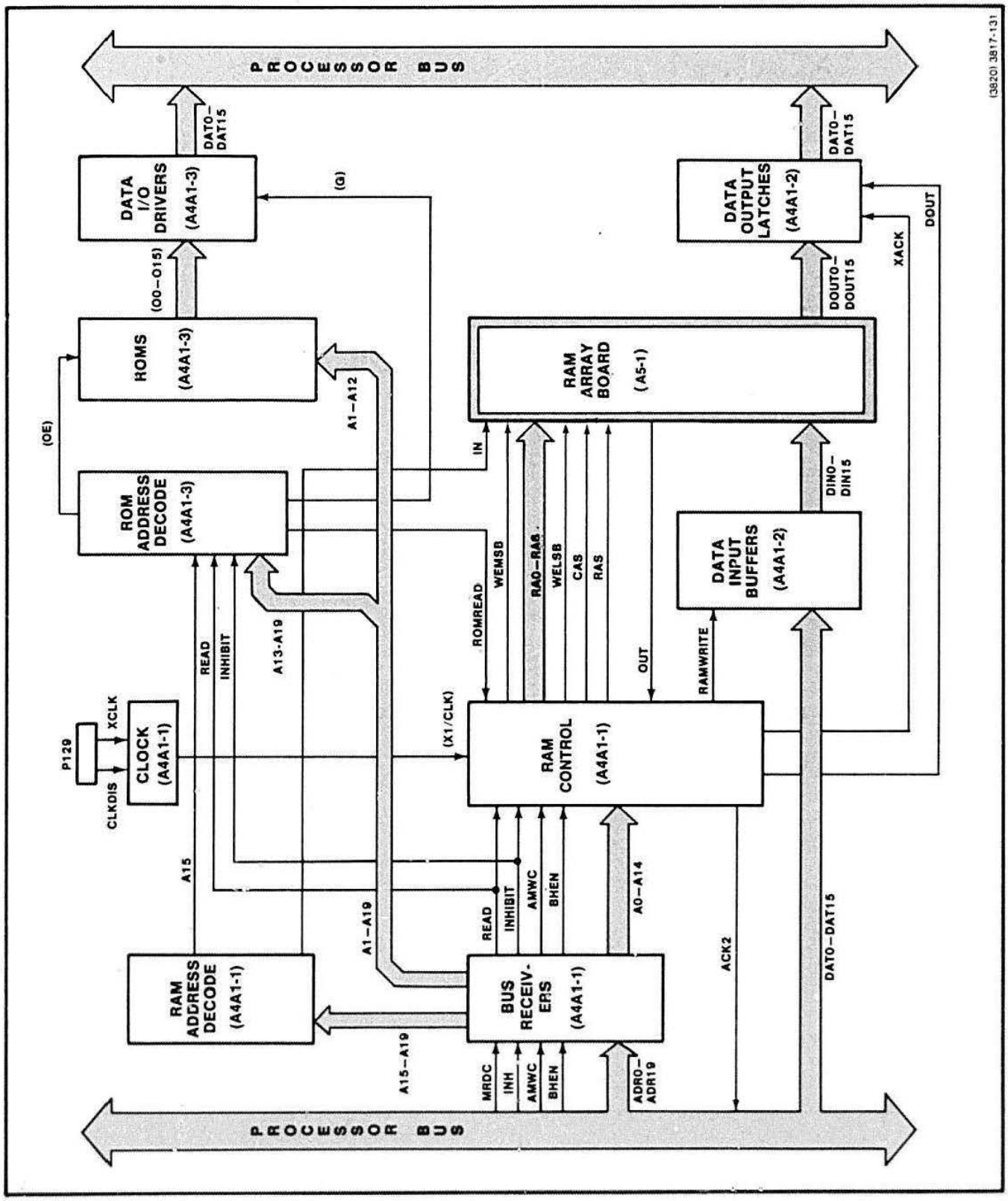


Figure 5-13. RAM/ROM Block Diagram.

- Provides address multiplexing and address strobes for the RAM on the RAM Array board
- Decides whether the RAM on the RAM Array board will be in a read, write, or refresh cycle
- Provides signals to latch data from the RAM Array board and to drive data onto the Processor Bus

This block consists primarily of the Dynamic RAM Controller. (Figure 5-14 is a block diagram for this controller.) In addition to this, the RAM Control circuitry includes some logic gates that combine related signals into new signals needed by the board. There are also two flip-flops that synchronize the timing of the read and write signals to the Dynamic RAM Controller clock signal (CLK). The Dynamic RAM Controller combines into one all of the functions that are needed to operate dynamic RAM. These functions are:

- Multiplexing 14 address bits into two 7-bit parts
- Arbitrating among selecting a read, write, or refresh cycle
- Generating various timing and control signals

The Dynamic RAM Controller also has circuitry for the internal generation of refresh signals for the dynamic RAM on the RAM Array board.

Multiplexing of RAM Addresses. A1-A14 are input to the multiplexer in the Dynamic RAM Controller. Because of the requirements of the 16K RAMs on the RAM Array board, A1-A14 is split into a low- and a high-order word. A1-A7 is output as a 7-bit row address and then A8-A14 is output as a 7-bit column address. The low and high words of A1-A14 appear one after the other on the RA0-6 lines of the RAM Control block.

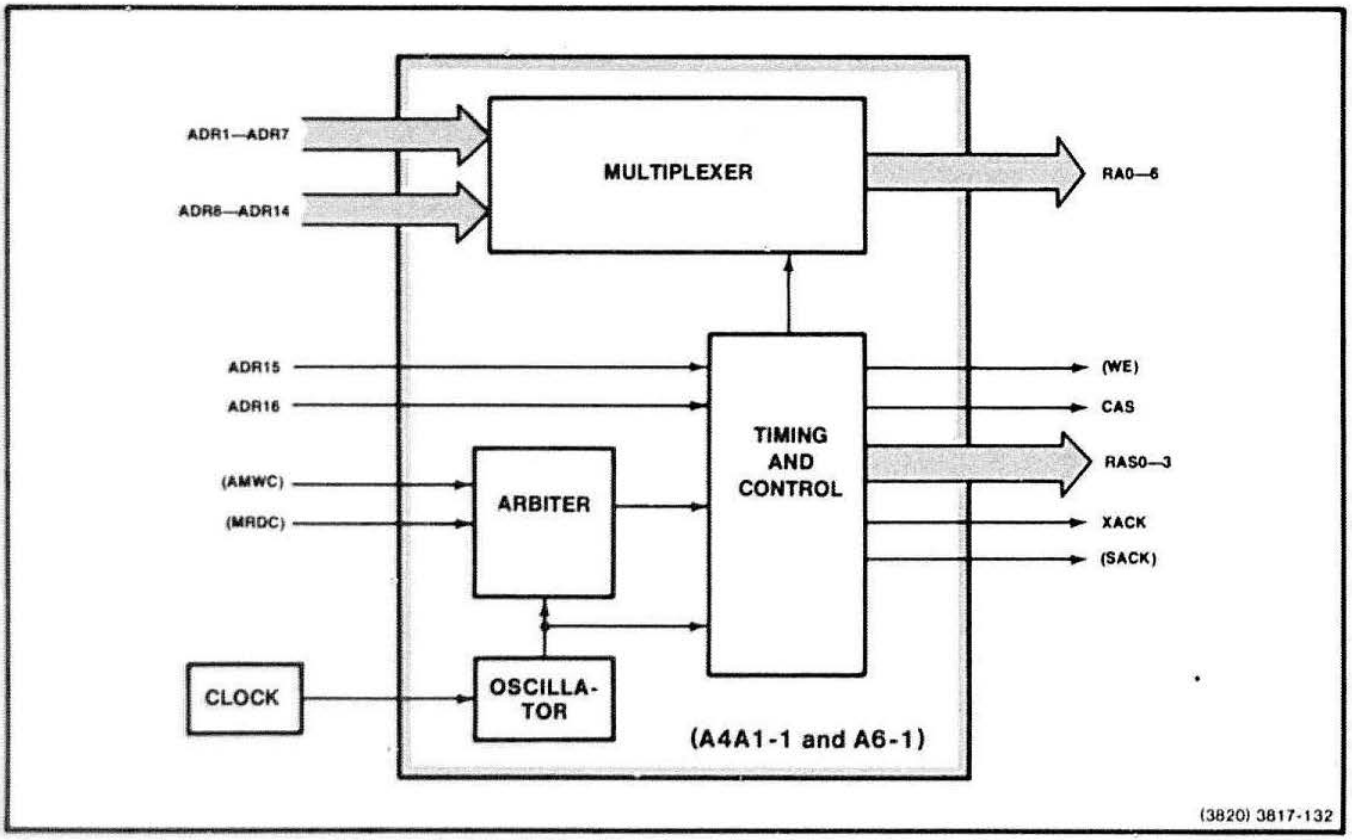


Figure 5-14. Dynamic RAM Controller Block Diagram.

Arbiter Circuitry. The Arbiter circuitry in the Dynamic RAM Controller arbitrates the read, write and refresh cycles. This sub-block prevents requests for read or write cycles from interrupting read, write, or refresh cycles in current operation. Refresh cycles are generated internally in the Dynamic RAM Controller.

Timing and Control. The Timing and Control sub-block generates the timing and control signals. This block of circuitry has five functions.

- It executes a read, write, or refresh cycle at the request of the Arbiter block
- It generates the column address strobe (CAS), the write enable (WE), and the row address strobe (RAS)
- It generates the transfer (XACK) and system (SACK) acknowledge signals
- It sends internal control signals to the multiplexer block in the Dynamic RAM Controller
- It resets an internal refresh timer and increments an internal refresh counter

Clock. The Clock circuitry on the board feeds a 22.008-MHz square wave to the Dynamic RAM Controller. This square wave provides the timing for the Multiplexer, Arbiter, and Timing and Control circuitry inside the Dynamic RAM Controller.

Dynamic RAM Controller Operations

The Dynamic RAM Controller performs these operations:

- Idling
- Write cycle
- Read cycle
- Refresh cycle

Idling. The Arbiter block in the Dynamic RAM Controller monitors requests for read, write, and refresh cycles. Read and write requests originate outside the Dynamic RAM Controller, but refresh requests all originate internally to the Dynamic RAM Controller.

The Dynamic RAM Controller is idling when requests are not currently being processed and cycles are not in progress. Read cycles are initiated if MRDC is active low when requests are sampled. Write cycles are initiated if AMWC is active low when requests are sampled. If a read or write cycle is requested simultaneously with a refresh cycle, the read or write cycle is executed before the refresh cycle.

Write Cycle. The steps of a write cycle occur in the following order:

1. The Multiplexer drives RA0-RA6 with the low-order address.
2. (SACK) is activated.
3. The RAS strobes the low-order row address into the RAM.
4. The Multiplexer drives RA0-RA6 with the high-order address.
5. (WE) is activated.
6. CAS strobes the high-order column address into the RAM.
7. XACK is activated.
8. All signals are deactivated and the Dynamic RAM Controller begins idling.

Read Cycle. The read and write cycles are nearly the same except that (WE) is not activated during a read cycle.

Refresh Cycle. When a refresh cycle is internally requested, the Multiplexer drives RA0-RA6 with a refresh address contained in an internal refresh counter. Then RAS is activated, causing a refresh cycle to occur on the RAM Array board. After some internal operations, the Dynamic RAM Controller begins idling again.

Data Input Buffers

The Data Input Buffers receive data signals from the Processor Bus and buffers them for the RAM Array board.

Whenever AMWC and OUT are active low, the RAM Control block generates RAMWRITE. This enables DAT0-DAT15 to be driven on to the RAM Array board.

RAM ARRAY BOARD

NOTE

The RAM Array board is a board that plugs into the RAM/ROM board and is NOT physically a block of circuitry on the RAM/ROM board. However, it is treated here functionally as a block of circuitry.

The RAM Array board is a small circuit board that contains 32K bytes of dynamic RAMs. The RAM Array board plugs into a socket on the RAM/ROM board.

The 32K bytes of RAM are arranged in two banks on the board. One bank handles the least-significant byte of a 16-bit word, and the other bank handles the most-significant byte of a 16-bit word. The RAMs are 16K-by-one bit wide, so there are eight RAMs in each bank.

The RAM address lines RA0-RA6 connect to both the LSB and MSB banks. RAS and CAS connect to both banks, but there are separate write enable signals (WELSB and WEMSB) that allow the accessing of the high and low bytes of the 16-bit word.

The RAM Array board responds to the signals generated by the RAM Controller block. Refer to the heading *RAM Control* (earlier in this section) for a description of accessing data on the RAM Array board.

RAM Array Board Circuit Blocks

Data Output Latches. Data Output Latches accept data from the RAM Array board and buffer it for the Processor Bus.

When XACK goes active low, data on DOUT0-DOUT15 is latched into the flip-flops in each of two D-type latches. When DOUT goes active low, the data is driven onto the Processor Data Bus lines, DAT0-DAT15.

RAM Address Decode. The RAM Address Decode informs the RAM Control block that the RAM on this board has been addressed. The RAM Address Decode block consists of a NAND gate and some inverters that detect when 00000 binary is on A15-A19. IN then becomes active low.

Clock. Clock generates a 22.008-MHz square wave that directly feeds the X1/CLK input of the 8202 Dynamic RAM Controller in the RAM Control block.

Two NAND gates are biased into their linear region of operation by 820 Ω feedback resistors. In this mode of operation, the NAND gates act as linear inverting amplifiers. A series tank circuit and a 22.008-MHz crystal are connected in a loop with the two gate amplifiers. This causes the circuit to oscillate at 22.008 MHz. The output is connected to the X1/CLK input of the 8202 Dynamic RAM Controller. The output also clocks two flip-flops in the RAM Control block.

ROM Address Decode. The ROM Address Decode circuitry produces one of eight ROM select signals, depending on which of the eight banks of ROM is addressed.

This block consists of a 3-to-8 line decoder and various logic gates.

Whenever both the G2B and G2A inputs to the decoder are low, the address on A13-A15 selects one of eight outputs. Each of the eight outputs enables one of the eight banks of ROM in the ROM block. READ is connected directly to the G2B input and A15-A19 are gated through some logic before they are connected to G2A. If READ is active low and A15-A19 is 11101 binary or 11110 binary, the decoder is enabled. (The ROMs in the ROM block respond to addresses X'E8000' through X'F7FFF'.)

If the bus master initiates a read operation from ROM, the ROMREAD signal becomes active low and the RAM/ROM board drives ACK2 active low on the system bus. If INHIBIT goes active low, it prevents the Data I/O Drivers block from outputting data to the Processor Bus.

ROM. The ROM block stores up to 64K bytes (32K of 16-bit words) of system firmware.

In the ROM block are eight banks of two ROMs each. The banks hold 4K of 16-bit words. A set of straps is associated with each bank of ROMs. The straps allow the board to use various kinds of ROM/PROM/EPROMs that have different pin function assignments.

This block outputs 16-bit words of data to the Data I/O Drivers block if MRDC goes active low and an address in the range of X'E8000' through X'F7FFF' is presented on A1-A19.

Data Output Drivers. Data Output Drivers drive data from the ROMS block onto the Processor Bus.

Two data drivers in this block handle DAT0-DAT7 and DAT8-DAT15 separately. Whenever (G) is low active, whatever is present on the inputs of the two drivers is output to the Processor Bus as DAT0-DAT15.

RAM CONTROLLER BOARD THEORY

The optional RAM Controller board is very similar to the RAM/ROM board. Both contain many of the same circuit blocks and the RAM Array board(s). For this reason, much of the following theory appears to be a repeat of earlier information. Because minor differences exist between the RAM/ROM board and the RAM Controller board theory, the following pages present a separate description for the RAM Controller board theory.

The RAM Controller circuit theory first describes the general architecture and operation of the RAM Controller board and then describes each block of RAM Controller circuitry. The order of the block descriptions follows the basic information flow, from left to right, of the block diagram in Figure 5-15.

GENERAL DESCRIPTION

The RAM Controller board supplies the optional system RAM memory that the Processor board and other bus masters use. It consists of a dynamic RAM controller chip (with support circuitry), in addition to four sockets where up to four RAM Array boards plug in. (RAM Array boards are small circuit boards that hold 32K bytes of dynamic RAM.) See Figure 5-16, RAM Controller boards and Memory Address Space.

GENERAL OPERATION

Two basic operations are performed by the RAM Controller: reading the contents of a location in RAM, and writing over the contents of a location in RAM.

To read the contents of a location in RAM, the bus master first places the location address on the Processor Bus; then it issues an MRDC. When the RAM Controller board receives an active MRDC signal, it responds by driving ACK2 onto the bus, and then the data from the addressed location.

To write to a location in RAM, the same sequence of events occurs except that AMWC is enabled (instead of MRDC) and the bus master drives the data onto the bus.

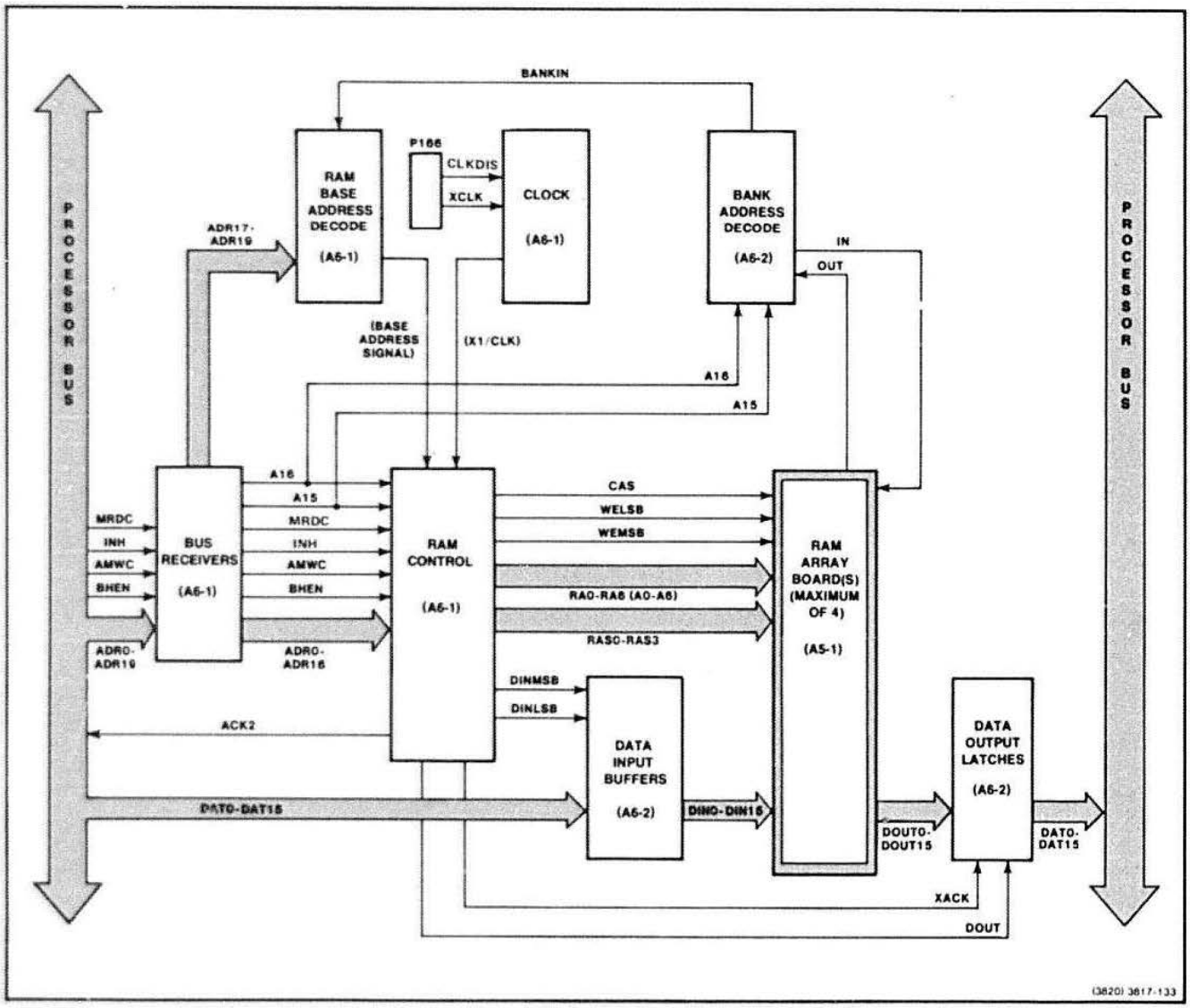


Figure 5-15. RAM Controller Board Block Diagram.

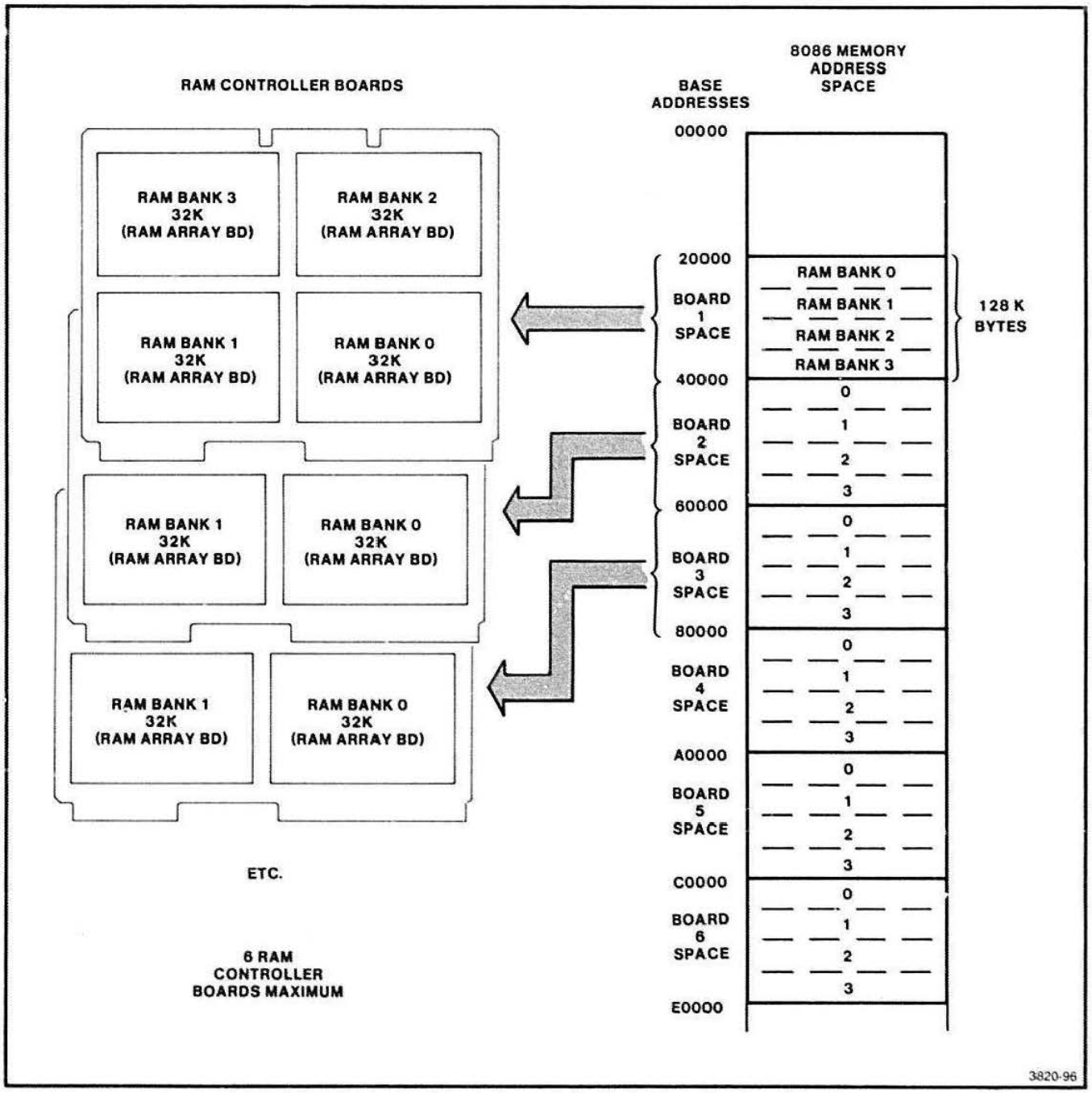


Figure 5-16. RAM Controller Boards and Memory Address Space.

RAM CONTROLLER CIRCUIT BLOCK DESCRIPTIONS

Bus Receivers

This block receives signals from the Processor Bus and buffers them for the board.

The three bus receivers are permanently enabled. This means that the outputs constantly follow whatever is on the system bus. The board responds when MRDC or AMWC is enabled and a valid address is on the Processor Bus.

RAM Control

The RAM Control circuitry:

- Generates all control signals for the RAMs on the RAM Array board(s)
- Provides address multiplexing and address strobes for the RAM on the RAM Array board(s)
- Determines whether the RAM on the RAM Array board(s) will be in a read, write, or refresh cycle
- Provides signals to latch data from RAM Array board(s) and place the data on the Processor Bus

This circuitry consists primarily of the DRC (Dynamic RAM Controller chip). See Figure 5-14, Dynamic RAM Controller Block Diagram. In addition to the DRC, there are some logic gates that combine related signals into new signals needed by the board. There are also two flip-flops that synchronize the timing of the read and write signals to the DRC clock signal (CLK).

The DRC combines all of the functions that are needed to operate dynamic RAM. These functions are:

- Multiplexing 14 address bits into two 7-bit parts
- Arbitrating for selection of read, write, or refresh cycles
- Generating various timing and control signals

The DRC also has circuitry for the internal generation of refresh signals for the dynamic RAM on the RAM Array board.

Multiplexing of RAM Addresses. ADR1-ADR14 are input to the multiplexer in the Dynamic RAM Controller. Because of the requirements of the 16K RAMs on the RAM Array board(s), ADR1-ADR14 is split into a low- and a high-order word. ADR1-ADR7 is output as a 7-bit row address and then ADR8-ADR14 is output as a 7-bit column address. The low- and high-order words of ADR1-ADR14 appear one after the other on the RA0-RA6 lines of the RAM Control circuitry.

Arbiter Circuitry. The Arbiter circuitry in the DRC arbitrates the read, write, and refresh cycles. This block prevents requests for read or write cycles from interrupting read, write, or refresh cycles in current operation. Refresh cycles are generated internally in the Dynamic RAM Controller.

Timing and Control. The Timing and Control sub-blocks generate timing and control signals. This block of circuitry has five functions:

- It executes a read, write, or refresh cycle at the request of the Arbiter circuitry
- It generates CAS (Column Address Strobe), WE (Write Enable), and RAS0-RAS3 (Row Address Strobes)
- It generates XACK and SACK, the transfer and system acknowledge signals
- It sends internal control signals to the multiplexer circuitry in the DRC
- It resets an internal refresh timer and increments an internal refresh counter

Dynamic RAM Controller Operations

The Dynamic RAM Controller performs these operations:

- Idling
- Write cycle
- Read cycle
- Refresh cycle

Idling. The Arbiter logic in the DRC monitors requests for read, write, and refresh cycles. Read and write requests originate from the Processor Bus, but refresh requests all originate internally to the DRC.

The DRC is in the idle state when no requests are currently being processed and no cycles are in progress. Read cycles are initiated if MRDC is active low when requests are sampled. Write cycles are initiated if AMWC is active low when requests are sampled. If a read or write cycle is requested simultaneously with a refresh cycle, the read or write cycle is executed before the refresh cycle.

Write Cycle. The steps of a write cycle occur in the following order:

1. The Multiplexer drives RA0-RA6 with the low-order address.
2. SACK is activated.
3. The appropriate RAS0-RAS3 signal strobes the low-order row address into the RAM.
4. The Multiplexer drives RA0-RA6 with the high-order address.
5. WE is activated.
6. CAS strobes the high-order column address into the RAM.
7. XACK is activated.
8. All signals are deactivated and the DRC enters the idling state.

Read Cycle. The read and write cycles are identical except that WE is not activated during a read cycle.

Refresh Cycle. When a refresh cycle is internally requested, the Multiplexer drives RA0-RA6 with a refresh address contained in an internal refresh counter. RAS0-RAS3 are all simultaneously activated causing a refresh cycle to occur on all RAM Array boards. After some internal operations, the DRC enters the idling state again.

Data Input Buffers

This circuit block receives data signals from the Processor Bus and buffers these signals for the RAM Array board(s).

Whenever a write operation is requested and ADR0 is active low on the Processor Bus, the RAM Control logic generates DINLSB. This enables the least-significant byte (DAT0-DAT7) of data to be transmitted to the RAM Array board(s). Whenever a write operation is requested and BHEN is active low on the Processor Bus, the RAM Control circuitry generates DINMSB. This enables the most-significant byte (DAT8-DAT15) of data to be transmitted to the RAM Array board(s).

Data Output Latches

These latches accept data from the RAM Array board(s) and buffer it for the Processor Bus.

When XACK goes active low, data on DOUT0-DOUT15 is latched into the flip-flops in each of two D-type latches. When DOUT goes active low, the data is driven onto the Processor Data Bus lines, DAT0-DAT15.

RAM Base Address Decode

This decoder circuit informs the RAM Control logic that a particular RAM Controller board has been addressed.

This circuitry consists of one 3-to-8 decoder. ADR17-ADR19 carry one of eight possible addresses. Only six of these are used, corresponding to the six ranges of addresses in system RAM. If BANKIN is active low and ADR17-ADR19 carry a valid address, the decoder pulls one of its six strappable pins low. If the correct decoder output pin is strapped, this circuitry asserts BDSELECT.

Clock

This clock circuit generates a 22.008-MHz square wave that directly feeds the X1/CLK input of the Dynamic RAM Controller Chip in the RAM Control circuitry. This square wave provides the timing for the Multiplexer, Arbiter, and Timing and Control circuitry in the DRC.

Two NAND gates are biased into their linear region of operation by 820 Ω feedback resistors. In this mode of operation, the NAND gates act as linear inverting amplifiers. A series tank circuit and a 22.008-MHz crystal are connected in a loop with the two gate amplifiers. This causes the circuit to oscillate at 22.008 MHz. The output is connected to the X1/CLK input of the DRC. The output also clocks two flip-flops in the RAM Control circuitry.

Bank Address Decode

This block sends a signal that indicates whether the addressed RAM Array board is installed in the RAM Controller board.

A15 and A16 can address any one of four RAM Array boards. The Bank Address Decode logic contains a 2-to-4 line decoder that responds to the address placed on its inputs by A15 and A16. If the RAM Array board corresponding to a received address is installed, IN is connected to OUT through the board, and BANKIN goes active low.

Section 6

DISPLAY BUS THEORY OF OPERATION

INTRODUCTION TO DISPLAY BUS

The three principal boards on the 4112 Display Bus are:

- The Video Controller board
- The Vector Generator board
- The Raster Memory board

This section describes these boards in the order (from left to right) that they are inserted in the card cage.

The Video Controller board acts as an interface between the Display Bus, the Processor Bus, and the Raster Display Module. The Video Controller accesses pixel data stored in the Raster Memory planes, and then sends it to the Raster Display Module for display.

The Vector Generator board accepts commands from the processor, converts them into vector data, and then sends that data to the Raster Memories.

VIDEO CONTROLLER BOARD THEORY

GENERAL DESCRIPTION AND OVERVIEW

The Video Controller board is the interface between the Processor Bus and the Display Bus, and occupies a specially wired slot next to the Processor Bus. The Video Controller board contains two main circuit modules:

- The Timing and Control section
- Display Module Interface

The Timing and Control section does the following:

- Decodes I/O addresses F000 through F7FF for the other boards on the Display Bus.
- Provides timing/control for RAMs on the Raster Memory board.
- Provides video timing for the Video Interface and Display Module.
- Supplies −2 Volts to the Display Bus for ECL termination.

The four-bit Display Module Interface performs these functions:

- Receives four bits of digital video data from the Video Map.
- Receives blanking pulses and sync pulses from elsewhere on the Video Controller.
- Then generates and sends to the Raster Display Module composite video and separate vertical and horizontal synchronization (hereafter called sync) pulses.

The display screen cursor is also created and controlled by a special circuit on the Video Controller board. This circuit uses a set of counters to remember locations of the vertical and horizontal lines that comprise the graphics crosshair cursor. See Figure 6-1 for a block diagram of the entire Video Controller board.

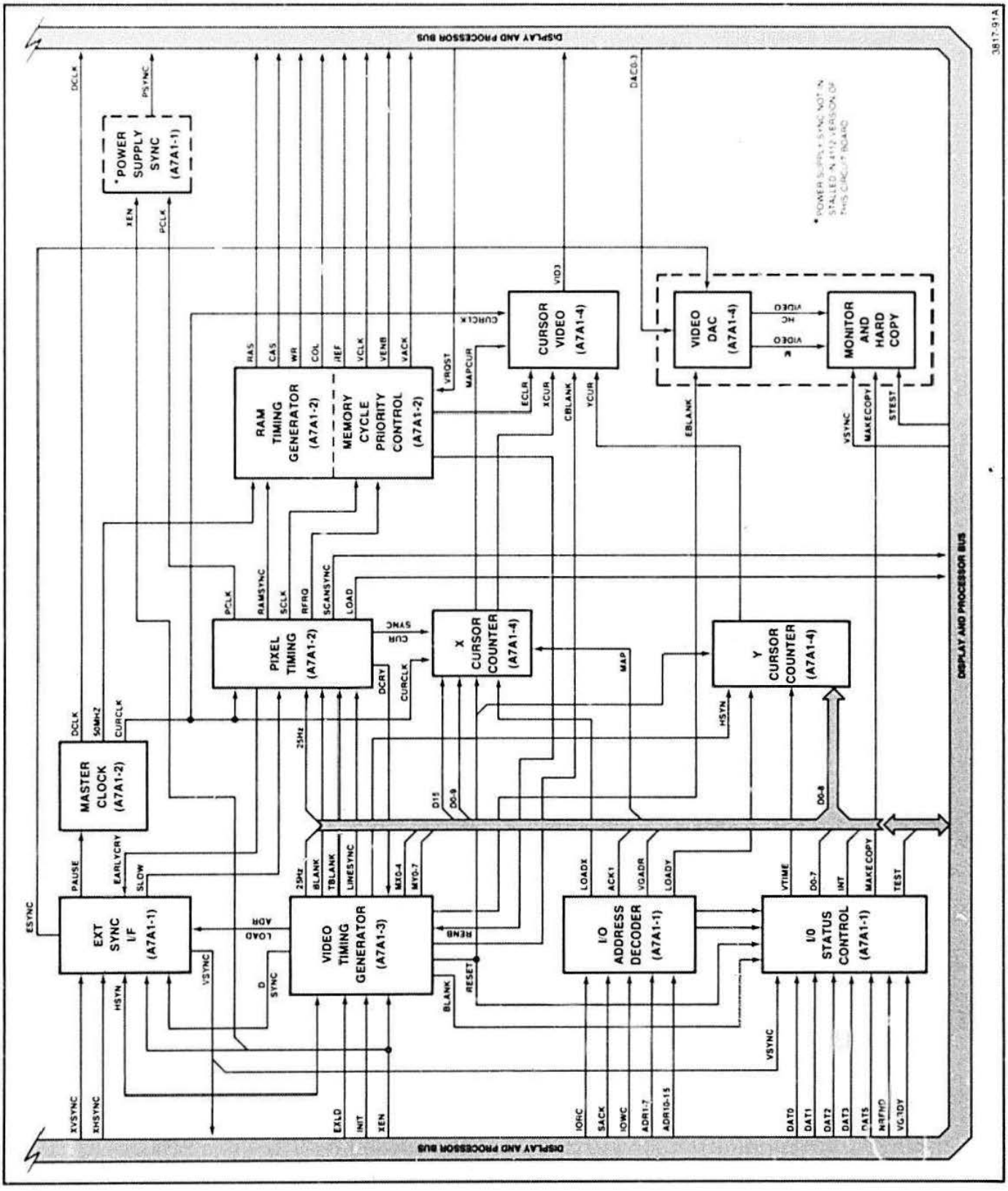


Figure 6-1. Video Controller Board Block Diagram.

VIDEO CONTROLLER CIRCUIT BLOCK DESCRIPTIONS

Master Clock

The Master Clock uses a free running 100-MHz crystal oscillator. A tuned circuit consisting of a resistor, a capacitor, a coil, and a crystal determines the oscillator frequency.

A divide-by-two circuit changes the oscillator signal to a 50-MHz signal. The 50-MHz signal, after going through another divide-by-two circuit, results in a 25-MHz signal.

All of the video circuitry in the 4112 terminal uses the 50-MHz clock and 25-MHz clock signals for a master clock. The Video Controller uses the 50-MHz signal to generate other timing signals. The Video Controller (hereafter called V.C.) uses the 25-MHz clock signal internally. This signal is also sent to the Raster Memory Planes as the DCLK-1 (dot clock) signal.

PAUSE-1 controls the 25-MHz and 50-MHz outputs of the master clock. This signal, when high, disables the first divide-by-two circuit; this stops the 50-MHz and 25-MHz clock outputs (see Figure 6-2). The PAUSE-1 signal thus switches the V.C. sync/timing from its internal clocks to a sync signal from an external device.

When the 4112 terminal is strapped to run at 60 Hz, a 100.8-MHz crystal replaces the 100-MHz crystal. This allows the video timing to run as close as possible to its correct line rate for 60 Hz. For simplicity all the description assumes a 100-MHz oscillator.

Strap J201 is a manufacturing board test strap and should always be installed for the board to work in the terminal.

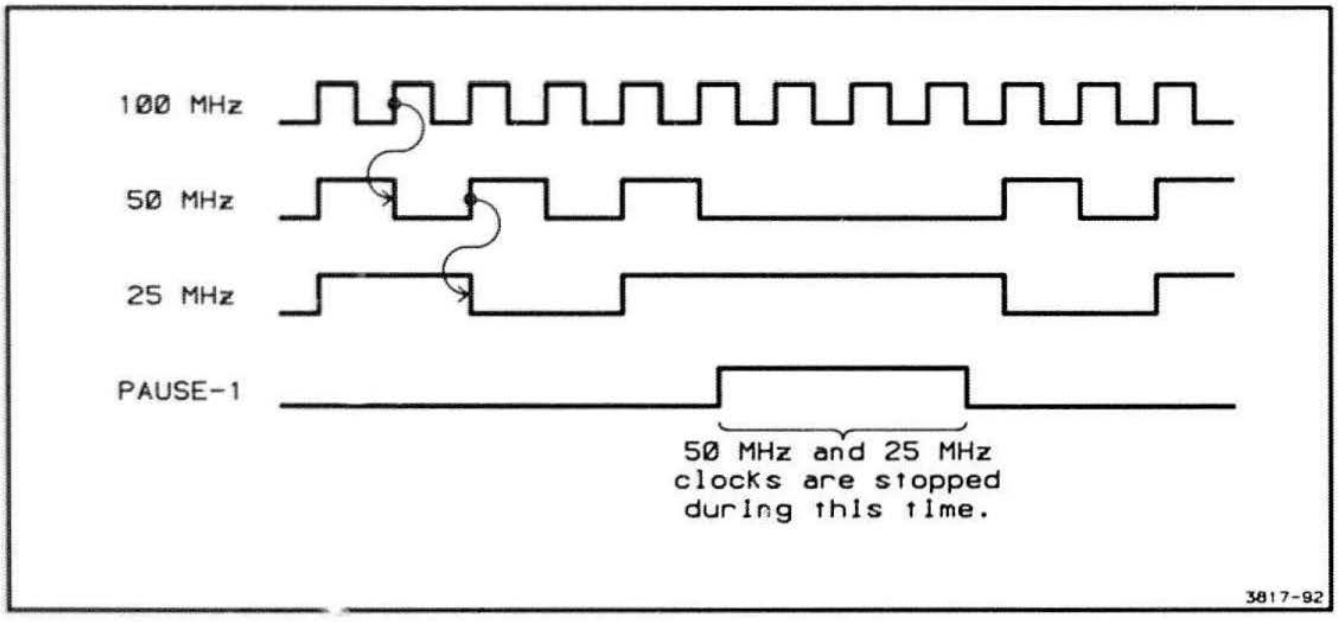


Figure 6-2. Master Clock Timing Diagram.

Video Timing Generator

This block generates:

- The horizontal and vertical sync signals which drive the video monitor (in the Display Module)
- The video blanking signal
- An additional sync signal (LINESYNC-0), which keeps the pixel timing blocks in sync with the Display Module timing
- The memory addresses used during the screen refresh memory cycles (MY 0-8 and MX 0-4)

The programmable CRT Controller chip plays an important part in the video timing. DCRY-1 (Dot Carry), from the pixel timing section, is the controller's only input while running. DCRY-1 is divided down by the various programmable counters in the CRT Controller. The outputs of these counters become the output of this controller chip.

Either an INIT-0 (initialize) or an EXLD-0 (external load) causes the CRT Controller to go through its "self-booting" sequence. Either input causes the 9-ms one-shot to fire, pulling the address and chip select lines high on the CRT Controller. Meanwhile, the 3-μs one-shot fires, causing the CRT Controller chip to load in eight bytes from the boot-strap PROM.

Details of this boot-strap loading process are contained in the 5027 CRT Controller Guide (manufacturers data book for SMC 5027 or TI 9927). The boot ROM contains four different modes of operation that are selected by the states of XEN-0 and 50 Hz-0. The appropriate mode is then loaded.

RENB-0 (enable for screen refresh) from the Memory Cycle Priority Control enables the tristate address drivers so the refresh address is sent to the Raster Memories.

LINESYNC-0 (syncs pixel timing to scan line) is generated at the beginning of HSYNC-1 and lasts for one DCRY-1 period.

The DCRY-1 flip-flop samples the vertical sync signal from the CRT Controller and sends VSYN to the External Sync block.

BLANK-0 (video blanking signal), EBLANK-0 (ECL composite video sync), and TBLANK-0 (TTL level composite blank) are all derived from the blanking signal coming from the CRT Controller.

Jumpers J56, J55, J650, J563, and J361 are manufacturing test jumpers and must always be in place for operation of this block. J551 is the jumper that selects either 50-Hz or 60-Hz terminal video operation. Refer to Section 8, *Functional Check and Performance Check Procedures*, for waveforms appearing at testpoints J283-4,5,8,9,10.

Pixel Timing Control

This block generates the timing for placing the pixels on the screen. The main input to this block is the 25-MHz clock. From this, Pixel Timing Control generates:

- The clock that goes to the video timing chip (DCRY-1)
- The load enable for the video shift registers (LOAD-1)
- A signal that syncs the RAM Timing circuit with the pixel timing circuit (RAMSYNC)
- The memory cycle request that initiates the screen refresh memory cycle

The 25-MHz clock that is used for DCLK-1 (dot clock) and CURCLK-1 (cursor clock) goes to a divide-by-10 counter. The output state of this counter (Q0 thru Q3) is sent to the A, B, and C inputs of a decoder.

Since each scan line on the display consists of 32 20-bit words, the timing signals from this block must repeat every 20 pixels instead of ten. A pixel state decoder performs this additional divide-by-two function and generates a signal called PHASE.

PHASE changes state at the beginning of "count 8" from the pixel state counter. PHASE is gated with the decoded timing states and is sent to a D-type flip-flop. Their relationship with each other as well as with some of the RAM timing is shown in the pixel timing diagram (Figure 6-3).

The main feedback signal from the Video Timing block is LINESYNC-0. This signal is sent during horizontal sync and assures that the PHASE is correct and that the pixel timing is synchronized with the video timing TBLANK-0. TBLANK-0 is used to force CURSYNC-0 (cursor sync) to occur only during blanking.

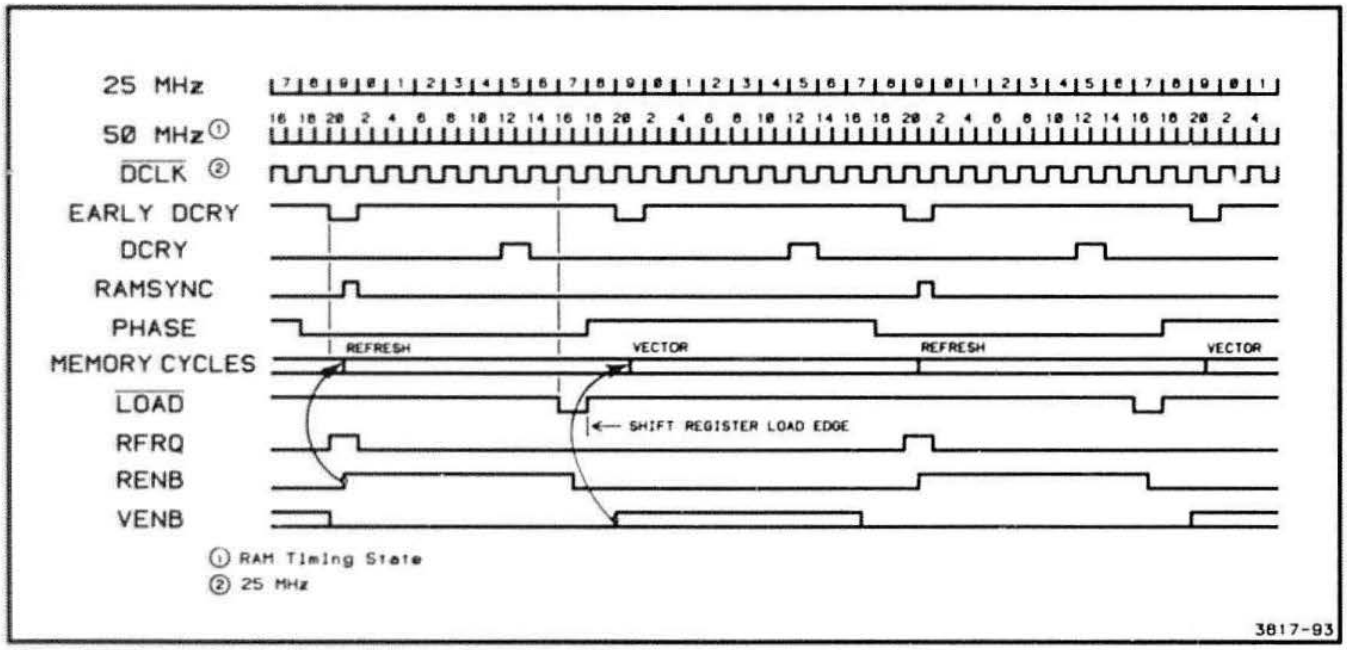


Figure 6-3. Pixel Timing Diagram.

The LOAD-1 signal loads pixel data into the video shift registers on the Raster Memory board. LOAD-1 comes from the decoder's Q6 output and is gated with BLANK-0. This means that no data may be loaded from the Raster Memories during either a vertical or horizontal blanking period. This prevents pixels from being sent to the display during an invisible part of the raster pattern.

The BLANK-0 signal also inhibits RFRQ-1 (raster memory refresh request) during blanking. An exception is when the 50-Hz option is installed. Because the 50-Hz video is slower than standard 60-Hz video, the less frequent memory refresh causes unsatisfactory retention of data. Therefore, BLANK-0 (with the 50-Hz option) does NOT prevent RFRQ-1; this allows memory refresh during blanking.

The CRT Controller generates timing for 524 line video; however, the Video Controller must send 525 line video to the display. To correct for this, the Video Controller effectively adds one scan line; it runs one scan line at half the normal frequency, so that its time equals two scans. Because DCRY-1 is the signal that synchronizes the pixel writes with the sweep rate, this signal's frequency must be halved during this particular scan line. The SLOW-0 signal accomplishes this by eliminating every other DCRY-1 pulse. (DCRY-1 is gated with the decoder's Q4 output.) SLOW-0 occurs during the vertical sync pulse so it halves DCRY-1 for only the one corresponding scan line. Thereafter SLOW-0 is removed and the remainder of the frame scans at the normal rate. Figure 6-3 shows the relative timing of these logic pulses.

RAM Timing Generator

The RAM Timing Generator generates the basic memory timing for the video memory. These four RAM timing signals are RAS, CAS, WR, and COL.

The RAM Timing Generator consists of a ring counter running at 50 MHz; the 50-MHz clock and RAMSYNC from the pixel timing blocks are inputs. The ring counter goes to state T2 when RAMSYNC comes from the pixel timing. This keeps the RAM timing in sync with the pixel timing. The ring counter outputs are logically combined to produce the RAM Timing Generator signals: RAS, CAS, WR, and COL. See Figure 6-4.

The RAS and CAS signals are gated with the output of the RAS and CAS enable flip-flop and put on the bus only when a memory cycle is supposed to take place. Memory cycle request pulses (RFRQ) enter the Preset of this enable flip-flop. This type of RFRQ control allows the completion of the current RAS and CAS, while blocking all subsequent cycles. The RAM timing diagram, Figure 6-5, shows the relationship of these signals to the RAM timing states of the Ring Counter.

Jumper strap J310 changes the timing of WR-1 slightly to be compatible with different types of RAMs (see Figure 6-5). Position 1 is for 4116-type RAMs and position 3 is for 2118-type RAMs.

Memory Cycle Priority Control

The Memory Cycle Priority Control circuitry decides between simultaneous requests for a vector cycle and a refresh cycle. Whenever an RFRQ comes from the pixel timing, REF and RENB are generated so a screen refresh cycle takes place. If a RFRQ and a VRQST (vector cycle) occur at the same time, a refresh cycle occurs first and then a vector cycle takes place on the next memory cycle.

During the time between a VRQST and the end of the vector memory cycle, VCLK-0 is stopped. Otherwise, VCLK is running all the time. If VRQST is continuously true (low), then every memory cycle that is not needed to refresh the screen is given to the Vector Generator. There is one VCLK at the end of each of these memory cycles. VENB-0 is generated during each Vector Generator memory cycle. Figure 6-5 shows these relationships.

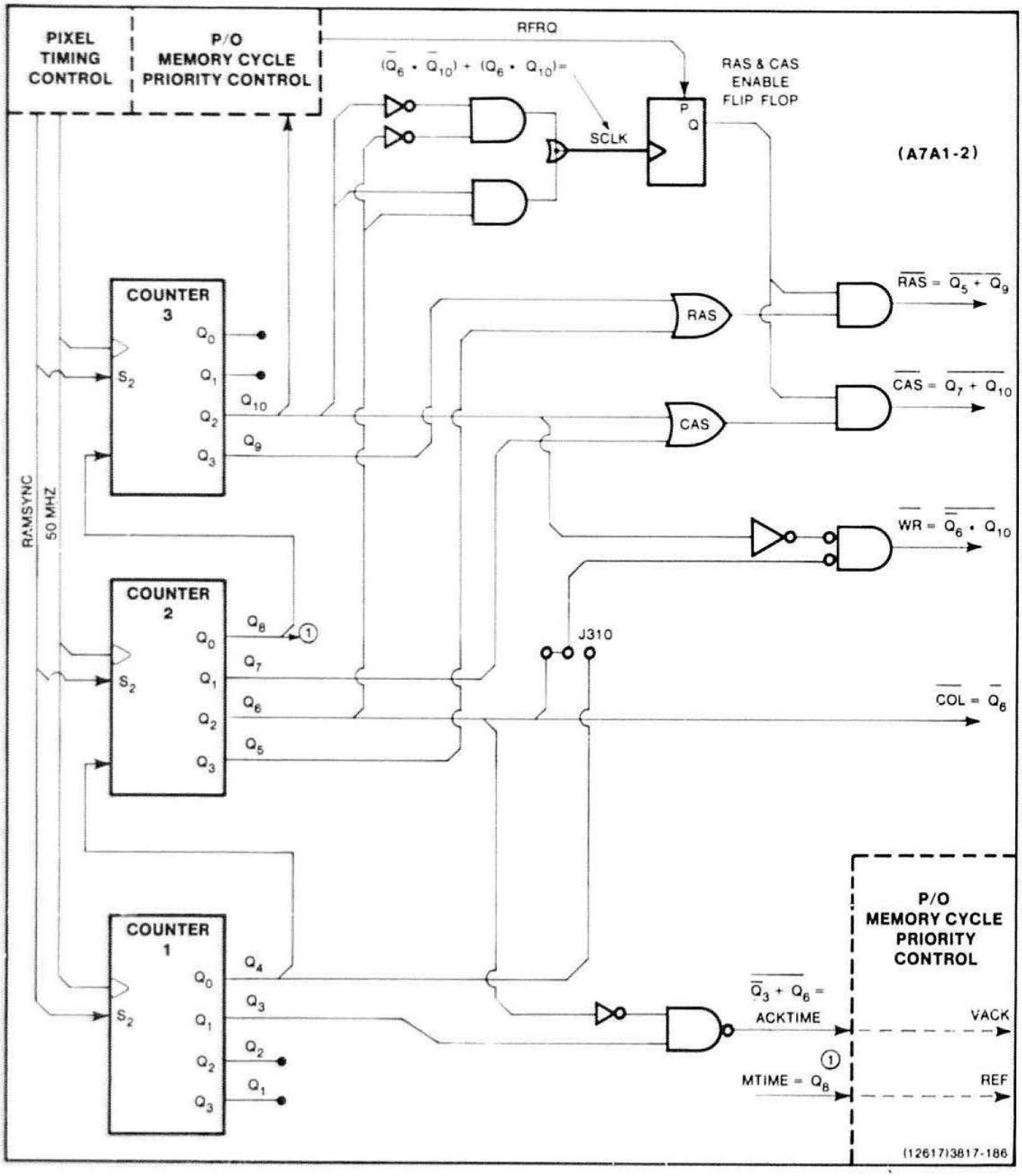


Figure 6-4. RAM Timing Generator Circuitry.

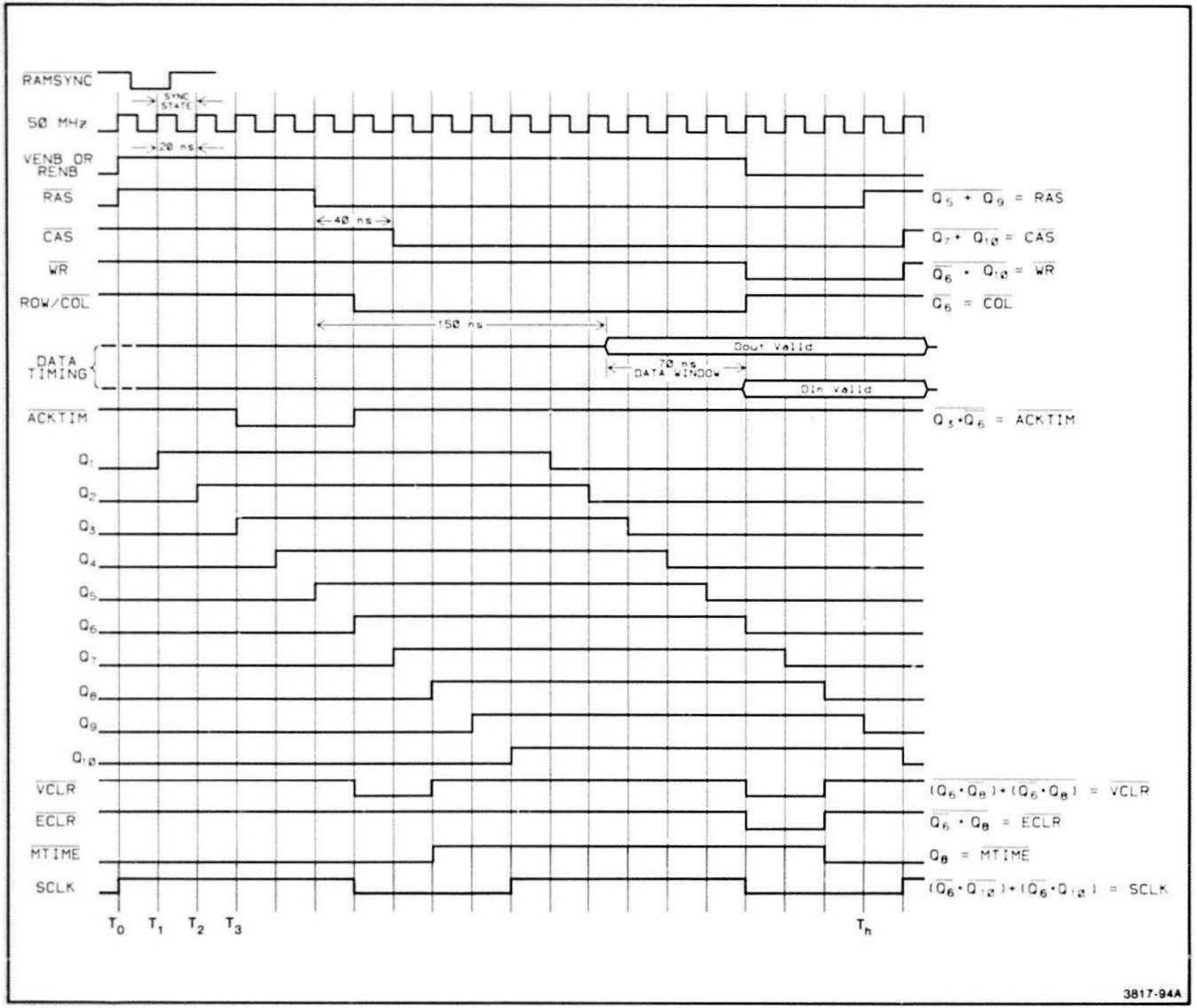


Figure 6-5. RAM Timing for Raster Memory System.

The Memory Cycle Priority Control generates:

- The clock for the Vector Generator (VCLK-0)
- The enables for the Vector Generator
- The enable for the Video Controller address drivers to the video memory

The Memory Cycle Priority Control also sends:

- VACK-0 to the Vector Generator to acknowledge that a memory cycle has been granted. VACK is a version of ACKTIME, generated by the RAM Timing block.
- REF-0 to indicate that a screen refresh memory cycle is taking place.

See Figure 6-6, Memory Cycle Priority Control Gates.

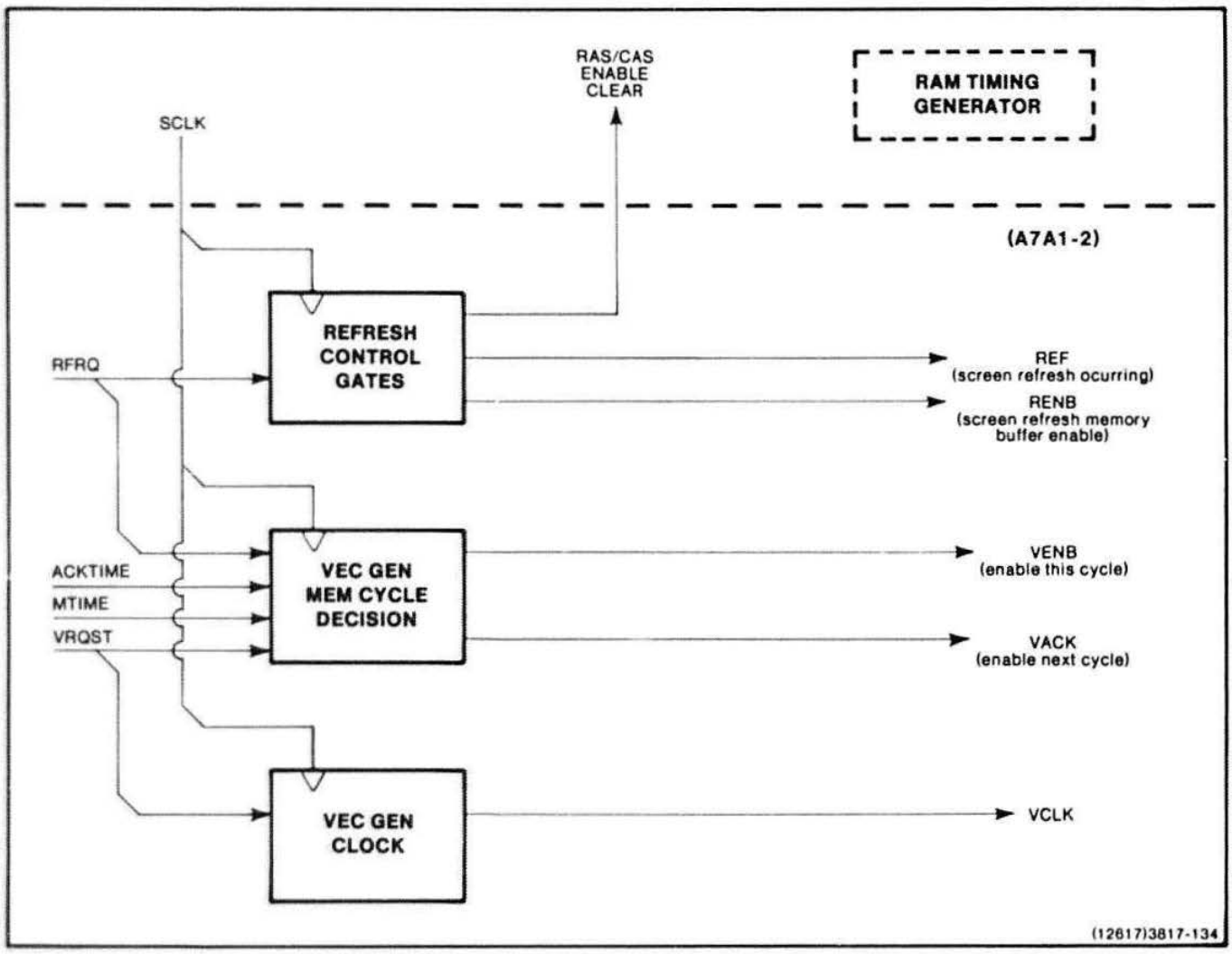


Figure 6-6. Memory Cycle Priority Control Gates.

Jumper strap J501 is a test jumper and, when installed, disables RFRQ so that the Vector Generator may have every memory cycle. This strap is used for testing the Vector Generator and should not be installed for normal operation.

Test connector J282 is set up for use with a logic analyzer (such as a TEKTRONIX 7D01 Logic Analyzer). This test connector is useful for verifying that memory timing is operating correctly.

The logic analyzer threshold must be set to −1.3 volts since all the signals are ECL logic. A typical logic analyzer display is shown in the J282 timing diagram. Because the requests from the Vector Generator and the blanking circuit will change the timing, there can be some variation in this output.

I/O Address Decoder

The I/O Address Decoder block decodes the I/O address on the bus, IORC-0 (I/O READ command), and IOWC-0 (I/O Write Command). It also generates the appropriate control signals.

This block:

- Decodes the most-significant five bits of the I/O address.
- Generates VGADR-0 (which goes to all the devices on the Display Bus, making decoding of these five bits by the rest of the boards unnecessary).
- Decodes the addresses of the status word and the control and cursor registers.
- Generates the appropriate load or enable control signals for the I/O Status Control.
- Generates an acknowledge (ACK-0) to the bus when VGADR-0 is true and either IORC-0 or SACK-0 is true.

Table 6-1

I/O ADDRESS SIGNALS

	Signals Generated	
Bus Address	**Read**	**Write**
F000-F700	VGADR-0	–
	IORC-0	IOWC-0
F740	I/O status (IORC ANDed with Decoder's Y4)	I/O status (Decoder's Y0)
F742	–	I/O control (Decoder's Y1)
F744	–	LOADX-0
F746	–	LOADY-0

I/O Interrupts and Status

This block acts as an interface between the system bus and the Video Controller. Figure 6-7 represents this circuit block.

This block:

- Contains status registers that the processor can read.
- Generates interrupts to the processor when certain functions have occurred.
- Contains control registers that enable or disable the interrupt function.
- Generates a MAKECOPY-0 pulse to initiate a hard copy when given the correct command by the processor.

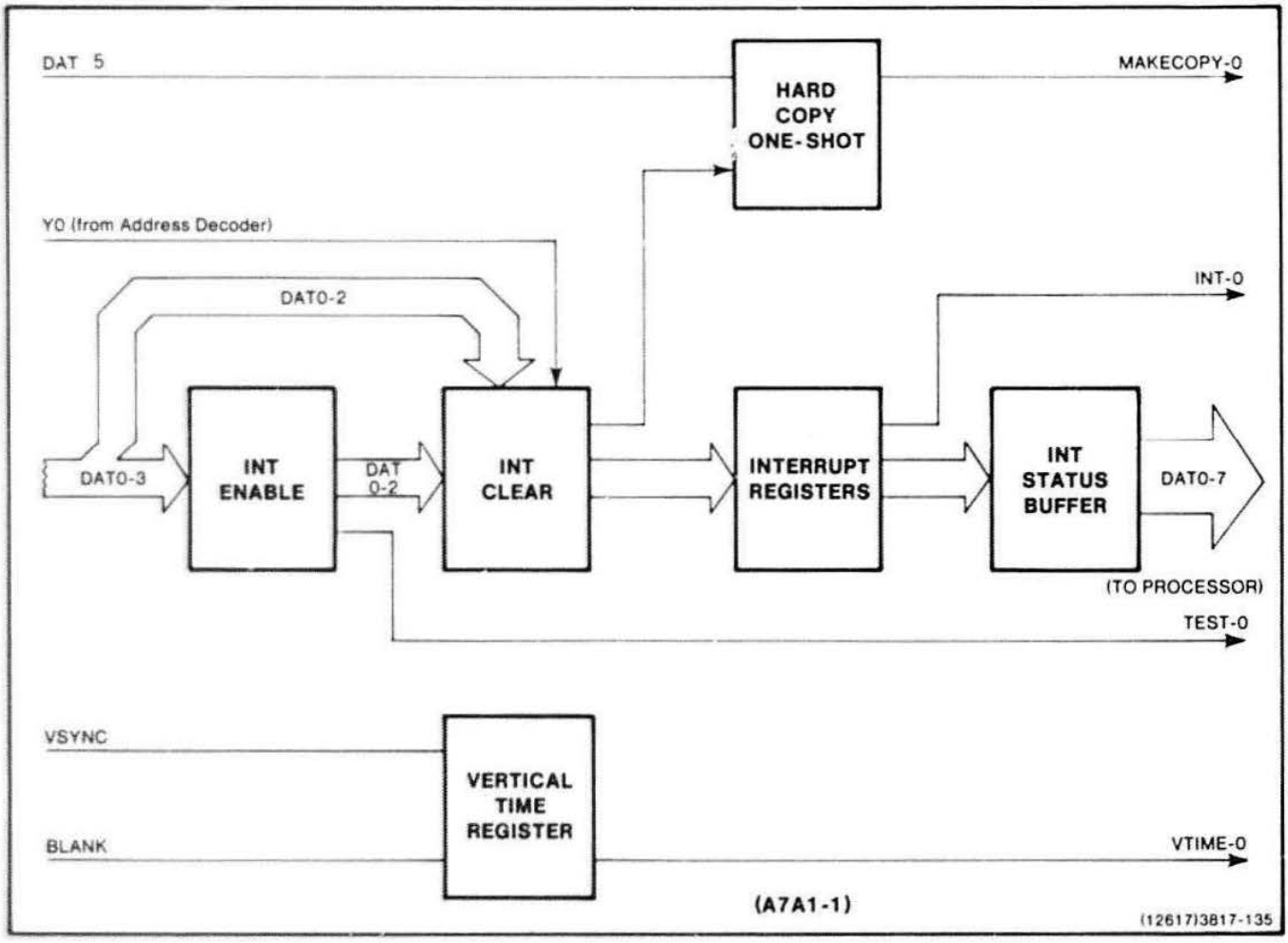


Figure 6-7. Interrupts and Status Registers.

The status word is read by gating IORC-0 with the proper decoded address. This enables the tri-state driver, which then places the status word on the data bus.

Interrupts are enabled or disabled by writing to the Interrupt Enable Register. If they are enabled, the following things cause their appropriate interrupt register to be set:

- When VGRDY-1 goes high, it sets the Vector Generator Ready register.
- When CBUSY-0 goes high, it sets the Hard Copy "Done Interrupt" register (flip-flop).
- When VSYNC occurs, it sets the Vertical Time Register.
- When any of these interrupt registers are set, INT-0 is sent to the processor.

When the Address Decoder's Y0 output generates an I/O Status Write, this signal is ANDed with the data bits. It either generates pulses to clear the interrupt registers or generates a pulse that triggers the 6-ms one-shot. This one-shot activates the MAKECOPY-0 drive circuit that sends a MAKECOPY-0 pulse to the hard copy unit. The generation of the MAKECOPY-0 pulse:

- Signals the hard copy unit to start a copy.
- Holds down the CBUSY-0 (copier busy) line.
- Gives the hard copy unit time to respond before it can pull down on the CBUSY-0 signal line.

Power Supply Synchronizer

This block synchronizes a switching power supply with the video display. This circuit is not needed in the 4112 terminal, and therefore is not installed.

X Cursor Counter

The crosshair cursor is a vertical and a horizontal line displayed on the screen. Unlike other vectors that are made by the Vector Generator board and written to the screen from the Raster Memory Planes, the cursor is written (via CUR-0) directly from the Video Controller to the screen.

The X Cursor Counter block consists of a register and a counter that generate the X component (vertical line) of the cursor. (See Figure 6-8.) The processor sends the address of the cursor's X location onto the data bus. It then sends a LOADX-0 (via the I/O Address Decoder) that causes the register to load this address. The data in this register is then loaded into the X counter during each horizontal retrace, signified by CURSYN-0 true.

The X counter is decremented by the clock, CURCLK-0, and counts down from the loaded address value until it reaches zero. At this point its RCO (ripple carry out) is sent as XCUR-0 to the Cursor Video block. XCUR-0 is converted into CUR-0 as a one-pixel wide pulse, which is sent to the display. This pixel is written on each scan, thus making a vertical line on the display.

The most-significant bit of the X register (DAT 15) is gated with MAP-0 and is used as a cursor enable bit. When the cursor is loaded with a 1, the cursor is enabled; otherwise it is disabled.

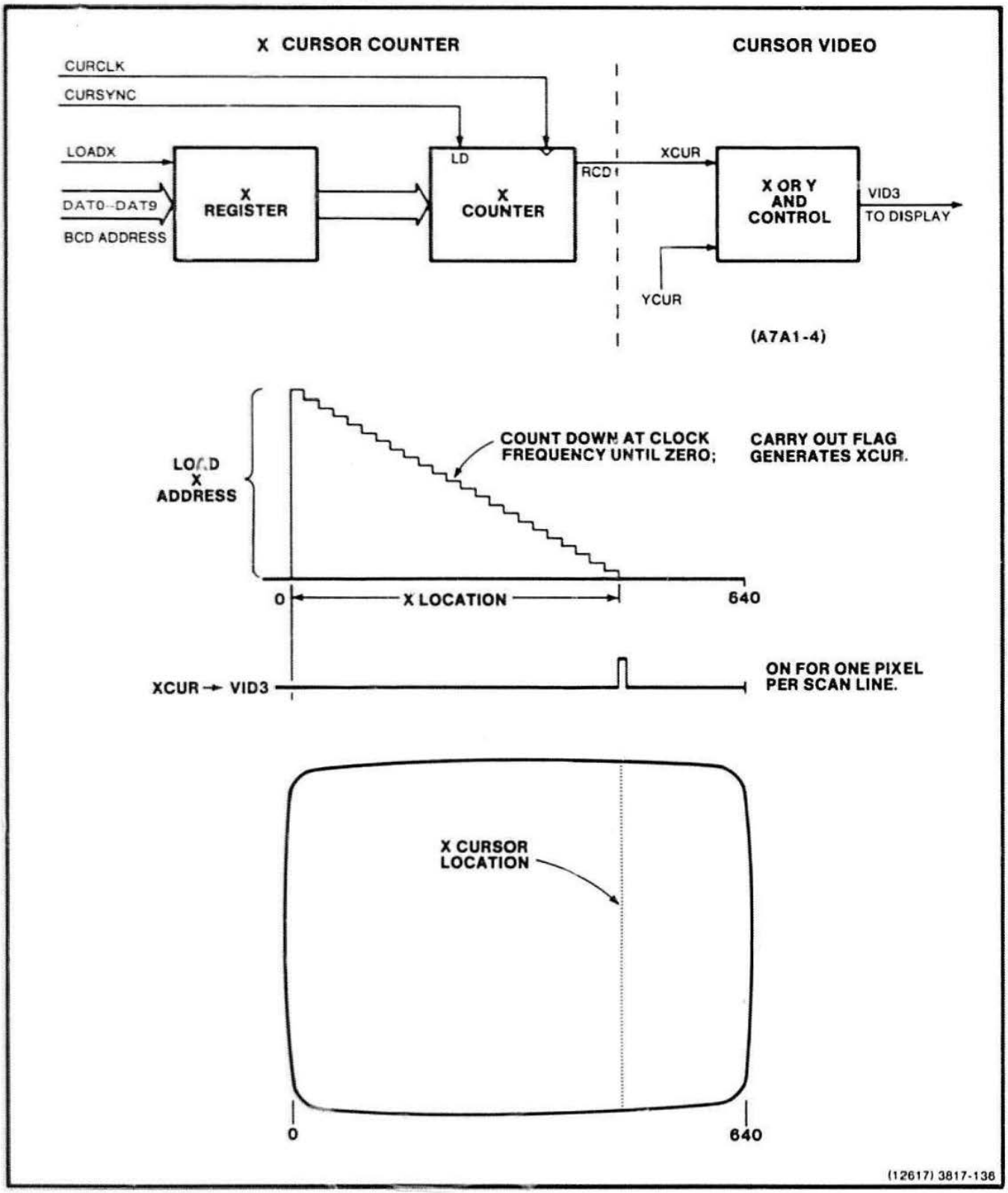


Figure 6-8. X Cursor Operation.

Y Cursor Counter

This block generates the cursor's Y component and functions similarly to the X Cursor Counter block. The Y Cursor Counter uses a register and a counter to make the horizontal line of the crosshair cursor. The register accepts a Y address from the data bus when the I/O address decoder sends the YLOAD-0 signal. This data is then loaded into the Y counter during vertical retrace (when VTIME-0 is true).

The Y counter decrements on every HSYNC (clock), except when VTIME-0 (vertical retrace) is true. It counts down until it reaches zero, which causes the carry-out condition. The carry signal, YCUR-0, is sent to the Cursor Video block along with the XCUR-0 signal from the X Cursor Counter. The YCUR-0 overrides the XCUR-0, and this causes the writing beam to turn on for one complete scan line corresponding to the Y cursor address. (See Figure 6-9.)

Cursor Video

This block generates the most-significant video bit (CUR-1, which is the same as VID3-0) that is used to control the cursor. This block combines:

- XCUR-0
- YCUR-0
- CBLANK-0 (cursor blanking)
- ECLR-0 (ECL clear pulse from the RAM timing)
- the enable signal from the X-Register

to make the CUR-0 cursor control signal.

The cursor latch is constantly sampling XCUR-0 on every CURCLK-1. When XCUR-0 is true, the output of the cursor latch goes low and CUR-1 is true. Likewise, when YCUR and the output of the Border Blanking Latch are both high, the cursor latch is cleared and CUR-1 is true. When either MAP-0 (map write select) or the cursor enable bit are low, the cursor latch is preset; this forces CUR-1 to be low.

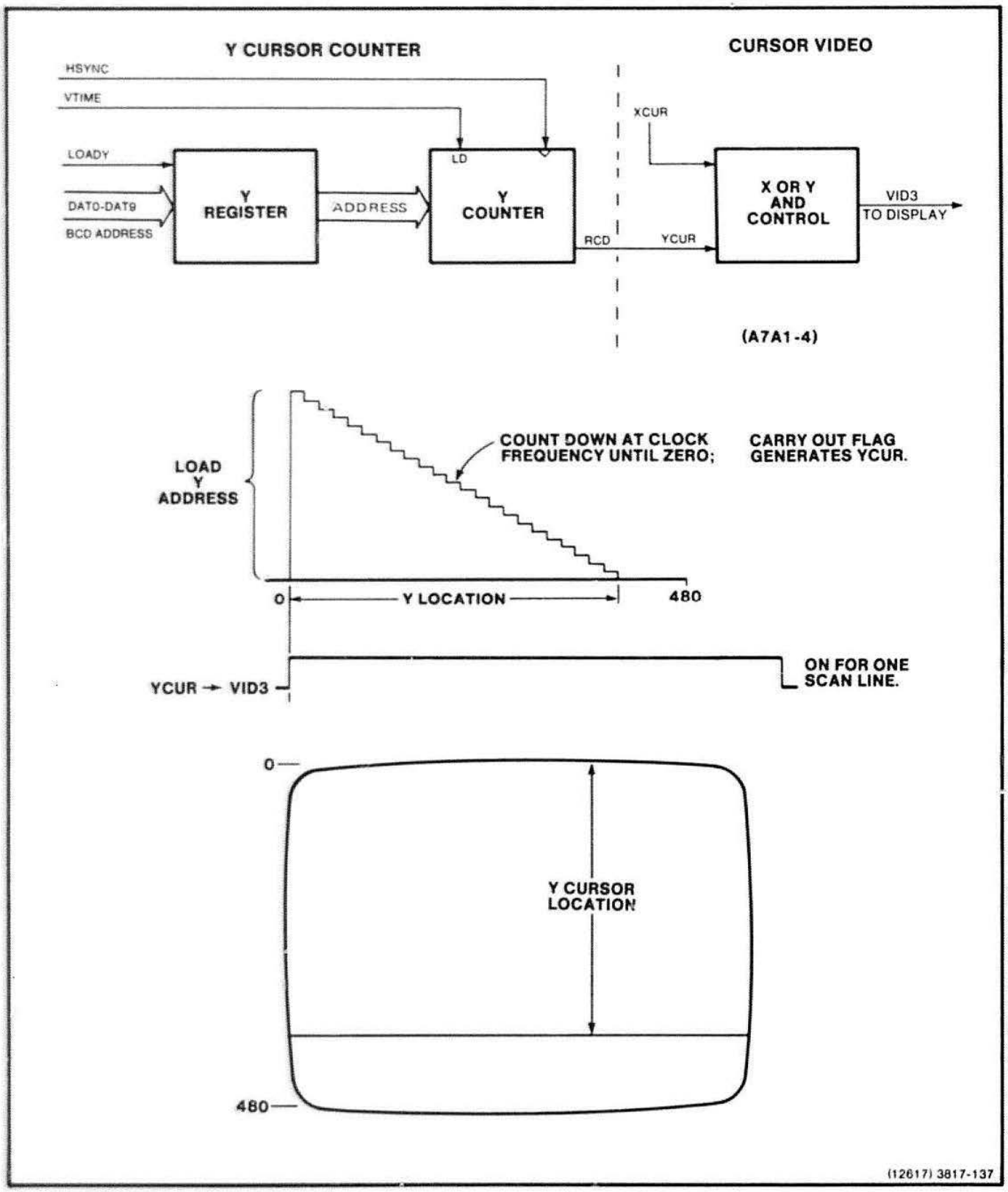


Figure 6-9. Y Cursor Operation.

Video DAC

The Video DAC (Digital-to-Analog Converter) block generates the analog video output for the Display Module and the hard copy unit. The block takes the four DAC bits (DACO-1 through DAC3-1), EBLANK-0, and ESYNC-0 and converts them to two identical analog signals.

The input signals all go to ECL gates, which have outputs that are connected to current source resistors and transistors. The collectors of all the transistors are tied together at the current summing node. The bias voltage is determined by the two DAC collector resistors.

These current source transistors are biased so that their emitters are at the ECL transition level. When one of the gates is high, the associated transistor is "off" and is not conducting. When the output of the gate is low, the transistor is turned on and the amount of current it is drawing is determined by the current source resistor.

The current source resistors, driven by the DAC0-DAC3 signals, are given binary values. This value causes 0 to 15 on these lines to generate linear steps from 0 to 2 volts at the current summing node (see Figure 6-10).

The voltage generated at the current summing node is the input to the Output Driver Amplifier. This is a two-output amplifier with a gain of 0.5 when driving a load of 75 Ω. The two outputs of this amplifier go to the Display Module and the video hard copy connector.

50-Hz Operation

To operate at 50 Hz, which adds 50 extra blanked scan lines before and after vertical sync:

- Move strap J551 from the 60-Hz position to the 50-Hz position.
- Change crystal from a 100.8-MHz crystal to a 100-MHz crystal.

External Sync

The External Sync Interface allows the 4112 video timing to synchronize with an external video sync system, such as a closed circuit TV system.

The optional External Video board, if present, applies XVSYNC (external vertical sync) and XHSYNC (external horizontal sync) to the inputs of this block. From these signals, this block generates VSYNC-0 (vertical sync) and HSYNC-0 (horizontal sync) for the Display Module, ESYNC-0 (ECL level composite video sync) for the video DAC, SLOW (DCRY at half the normal rate) for pixel timing, and PAUSE (stops 50-MHz clock) for the Master Clock.

VSYNC-0 is generated by combining VSYNC and VSYNCDELAYED, making two horizontal periods. Because each signal lasts 3 x 31 μs or three "H times," VSYNC-0 lasts for six "H times" (i.e., 6 x 31 μs).

The CRT Controller generates SLOW, which lasts for one horizontal count, during the end of VSYNC. This horizontal count is actually two horizontal periods because the DCRY-1 (dot carry clock) clock period is halved during this time. The DCRY-1 clock period is halved when DCRY-1 goes to the pixel timing blocks.

ESYNC-0 is the combination of HSYNC-0 and a shortened version of VSYNC-0. ESYNC-0 goes to the Video DAC as a composite SYNC signal.

The PAUSE-0 signal inhibits the internal sync signal, thus allowing the Video Controller to sync to an external monitor. If XEN-0 (external sync mode enable) is true (low) and HSYNC or VSYNC occur, PAUSE occurs. PAUSE goes to the master clock and causes it to stop. The board stays in this state until XHSYNC-0 or XVSYNC (if VSYNC has caused the PAUSE) occurs. This immediately takes away PAUSE-1 and allows the Master Clock to run again. PAUSE-0 allows the board to sync to any external sync source.

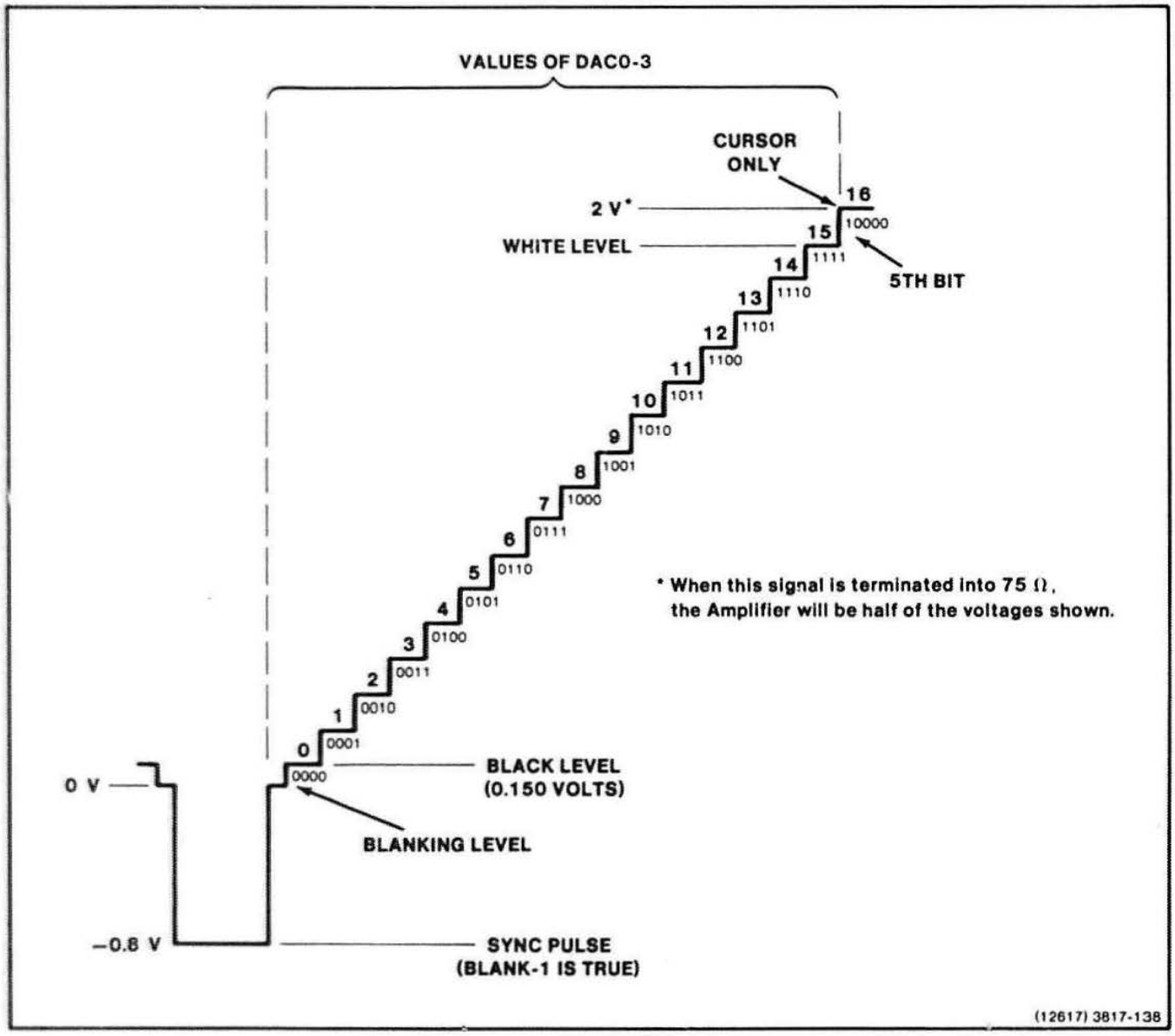


Figure 6-10. Analog Output of the DAC.

VECTOR GENERATOR BOARD THEORY

GENERAL DESCRIPTION AND OVERVIEW

The Vector Generator board writes vector data into the Raster Memories. The 4112 and 4114 Vector Generator boards (though they have similar names) are not interchangeable. The 4112 Vector Generator board makes vectors for a raster-type display, while the 4114 uses a DVST-type display. The way a vector is created on these two terminals is considerably different, and consequently the circuitry is much different.

The Vector Generator board contains I/O registers that receive instructions from the processor via certain I/O address and data lines on the Display Bus. These instructions are decoded by a state machine type of processor. This state machine takes firmware "op-codes" and generates dots in various display pixels that make up zig-zag lines. From a distance the eye perceives these zig-zag lines as a straight line or a smooth curve.

Figure 6-11 is a simplified block diagram of this circuit board, while Figure 6-12 is a detailed block diagram of the same board.

The Vector Generator performs the following functions upon command from the terminal's main processor:

- Generates vectors
- Erases
- Performs vertical block moves (scrolls)
- Reads bit maps
- Generates dot matrix characters

The Vector Generator is an intelligent board and performs the requested operation without intervention from the main processor.

A microcoded state machine that operates on a 200-ns cycle (5-MHz clock) controls the Vector Generator circuits (which are mostly counters and registers). The state machine, which exercises the proper combinations of registers and counters to achieve the desired draw, scroll, or erase, interprets the complex array of firmware intructions from the processor. All Vector Generator operations are transparent, so no visible effects appear on the display screen. However, certain operations may result in transitory visible effects due to the nature of the refresh cycles.

The following pages describe each circuit block on the schematic diagrams for this board.

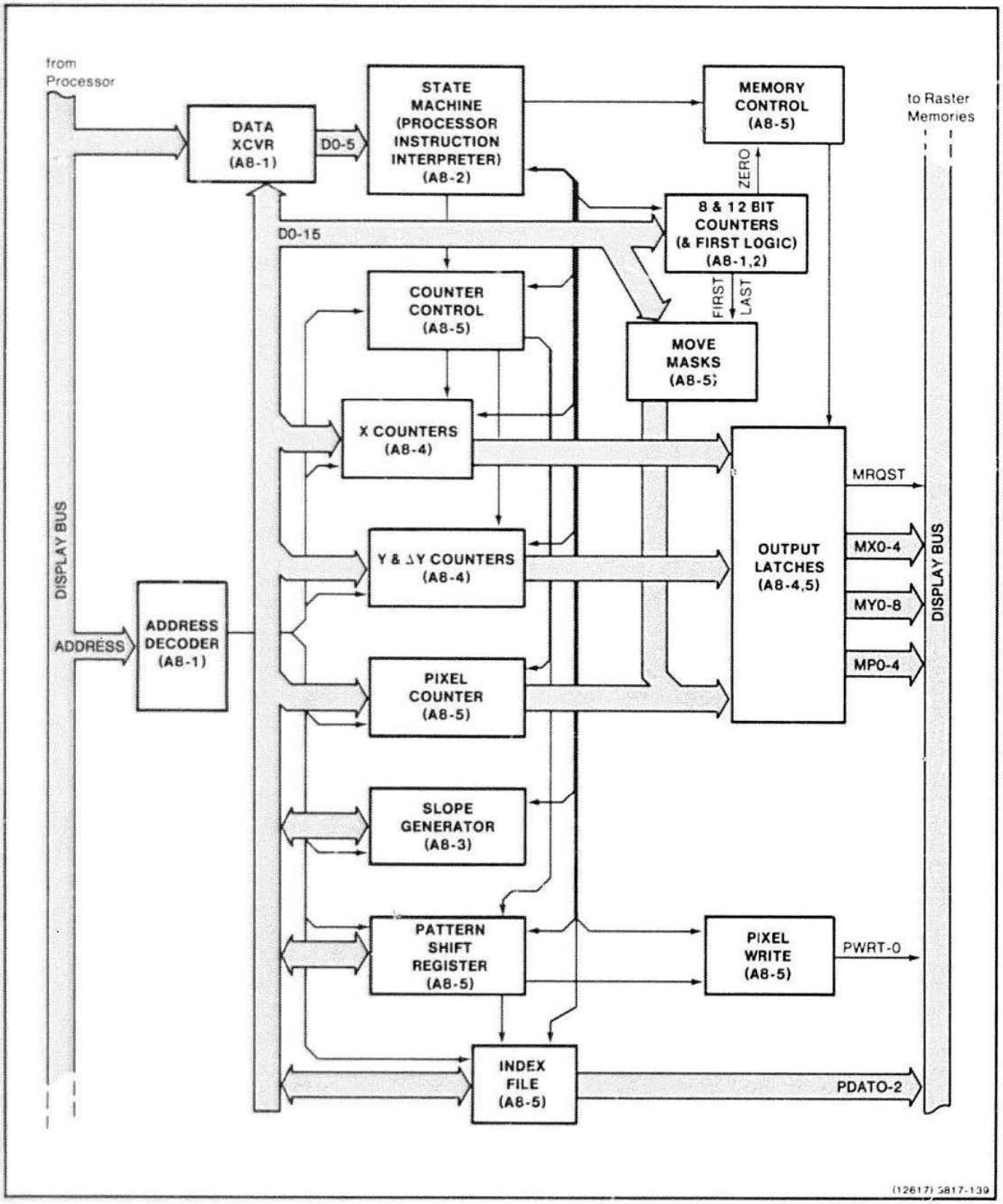


Figure 6-11. Vector Generator Board Simplified Block Diagram.

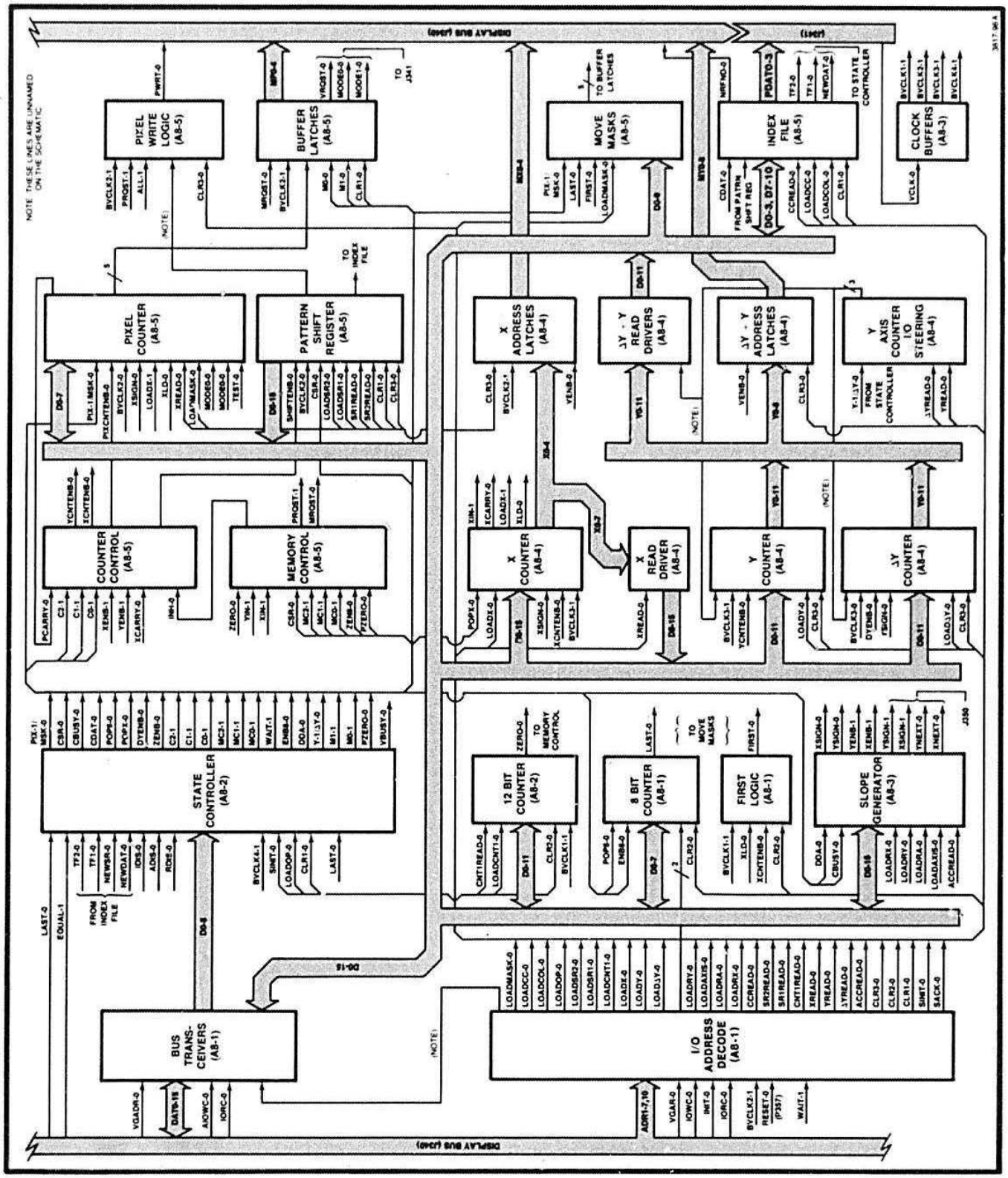


Figure 6-12. Vector Generator Board Block Diagram.

VECTOR GENERATOR CIRCUIT BLOCK DESCRIPTIONS

Bus Transceiver

The Bus Transceiver block isolates the data portion of the Display Bus (Motherboard) from the Internal Data Bus, which is used by the various registers within the Vector Generator to receive and transmit data. A pair of tristate bus transceivers isolates the two busses. A buffered IOWC-0 (I/O write control) signal from the bus produces bus direction control. The transceivers assume that a write cycle is taking place unless Read is present. Tristate driver enable is achieved on write cycles by ANDing together AIOWC-0 (advanced I/O write control), and VGADR-0 (Vector Generator address), which is generated by the Video Controller.

Read cycle tristate enable is achieved by ANDing together a buffered version of IORC-0 (I/O read control) and a board select signal (from the I/O Decode block). The read and write control signals are then NORed together to create a common gate signal for the two transceivers.

I/O Decode

The I/O Decode block provides four functions:

- Decodes board address
- Decodes individual READ and WRITE strobes
- Synchronizes WRITE strobes to the board clock and generates write acknowledges for the complete display system, and
- Synchronizes and buffers board reset signals from both the bus and test square pins.

Signals ADR5-1 through ADR7-1, ADR10-1, and VGADR-0 are ANDed together to generate the board select signals. VGADR-0 is a signal that originates on the Video Controller board; it represents the decode of the "missing" address bits that are common to all devices on the Display Bus.

There are three sources of "reset" signals on the board. INIT-0 (from the bus) and RESET-0 (from the test connector) are ORed together and synchronized to the clock. This reset signal is then ORed with a decoded write signal that provides a software reset capability and is distributed to the other circuit blocks as CLR1-0, CLR2-0 and CLR3-0. The bus and test connector resets are also available as SINIT-0 (system INIT signal), which is used only by the State Controller block.

Four decoders decode the individual READ and WRITE strobes: two are for writes and the other two are for reads. All four decoders have their select inputs connected to the three least-significant address bits from the bus (ADR1, ADR2, and ADR3). ADR4 and its complement select between either the low eight or high eight decoders. The "board select" signal strobes all four decoders (enabling them when the board is addressed). The remaining G2B pin receives the buffered IORC-0 signal (on the read decoders) and the synchronized write signal on the write decoders. The outputs of the decoder chips are the decoded read and write signals. Write strobes are named LOADxxx-0 while read strobes are named xxxREAD-0 (where xxx denotes the different signal names).

The write synchronization logic consists of the remaining three sections of a flip-flop chip and the gate network connected to the inputs of these flip-flops. Another flip-flop generates the SACK (system acknowledge) signal. Writes to the board must be synchronized with the clock to guarantee that counters will load correctly. The WAIT-1 input allows the Vector Generator to cause the processor to wait for completion of an operation before receiving its acknowledge signal. This has the effect of synchronizing the processor to the Vector Generator and is used in such time-critical operations as outputting characters. SACK becomes the processor acknowledge signal, after passing through the Video Controller. The Write Synchronizer sequences on all I/O writes occurring in the complete system, but the Video Controller passes the SACK signal to the processor only on writes to the display section of the 4112. (The Vector Generator acknowledges all display system writes, not just its own).

Figure 6-13 is a block diagram of this circuitry.

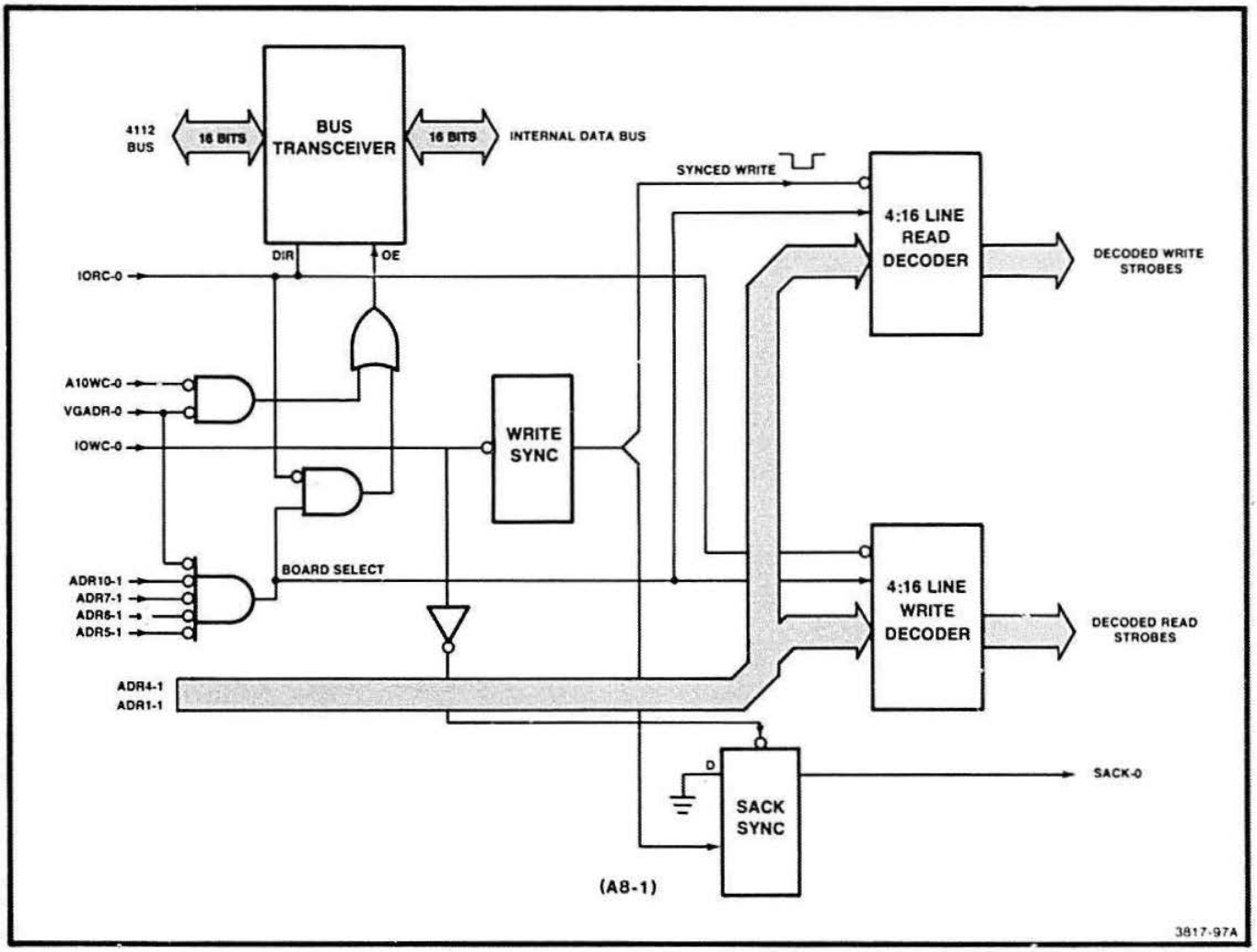


Figure 6-13. Data Bus Transceiver, I/O Decode, Write Sync, and SACK Logic.

Figure 6-14 shows the timing of this synchronization circuit. Assuming the circuit is at rest with its clock running (no IOWC signal has occurred), the outputs of the Write Sync chip are: 2Q-1 = 0, 1Q-0 = 1, 4Q-0 = 1, and SACK-0 = 1. Then if IOWC-0 goes low and WAIT-1 = 0 sometime between two clock edges, 2Q-1 goes to one (note the possible glitch); 2Q-1 = 1 starts the first clock pulse, T1. At the start of T2, outputs 2Q-1, 1Q-0, and 4Q-0 (the synchronized write pulse) all go low. One clock pulse later (at the start of T3) 4Q-0 goes high. This ends the write pulse and clocks the SACK-0 signal to go low. Sometime later, the processor receives its acknowledge signal (SACK is passed through the Video Controller) and terminates its write pulse (IOWC-0 = 1). This causes the SACK flip-flop to be set back to one. At the next available positive clock edge (shown in Figure 6-14 as the end of T4), 1Q-0 clocks back to a one, and the cycle is finished. Note that the WAIT-1 signal acts to block the IOWC-0 signal, thereby extending the cycle until both signals are zero.

Eight-Bit Counter

This counter has different uses for the different modes, but its main purpose is to down-count the block move column value.

The Eight-Bit Counter is a modulo 256 counter. The Vector Generator's State Controller uses this counter to determine the number of times to repeat portions of microcode. The value loaded into to the counter always comes from the processor; the State Controller has no control over the count value. The counter itself is composed of two four-bit counter chips. The counter always operates in a down-count mode and does not count below state zero. Whenever the counter contains a value of zero, the LAST-0 signal is true. The processor may then read the contents of the counter.

When the processor reads the counter, the decoded read strobe places the counter's value onto the eight least-significant bits of the internal data bus (a Self Test feature). The counter may be loaded in two different ways.

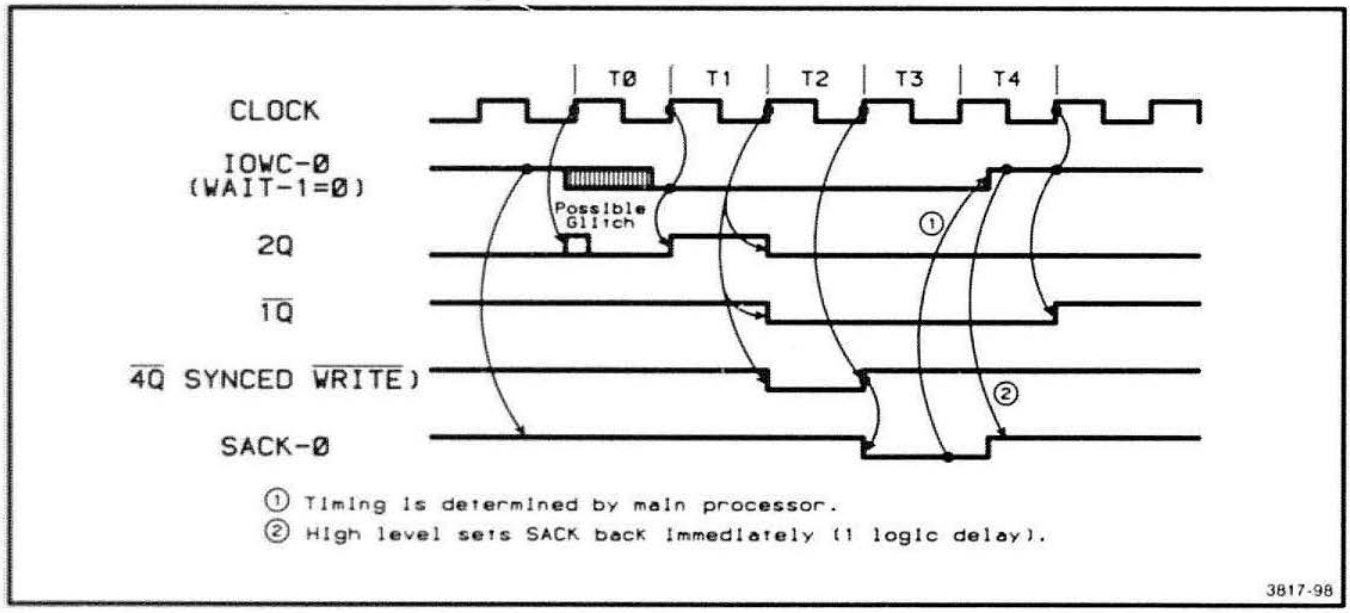


Figure 6-14. Write Synchronization Timing Diagram.

First, whenever the processor writes to the eight-bit counter, both of the counters and the input latches are loaded with the value written by firmware. To load the counters and latches, the decoded write strobe gates the latch and generates a load signal for the counters.

The second way to load the counters is via the State Controller-generated signal, POP8-0. When this signal occurs, only the counters receive a load signal (not the latch gate); this reloads the counters with the last value written by the processor.

The counter is enabled by the signal ENB8-0, generated by the State Controller.

Twelve-Bit Counter

This counter also has different uses for the various modes, but its primary purpose is to down-count the vector length value and the block move row value.

The Twelve-Bit Counter operates similarly to the Eight-Bit Counter in that it determines the number of times to repeat microcode loops. However, the Twelve-Bit Counter does not have a storage register on its input data as does the Eight-Bit Counter. The Twelve-Bit Counter may read from and write back to the internal data bus the 12 least-significant bits. Such a read or write is directed by the processor. Like the Eight-Bit Counter, its operating mode is countdown and the counter does not count below zero. When the counter contains zero, then the ZERO-0 signal is true. The Twelve-Bit Counter contains some additional logic associated with the ZERO signal, consisting of a flip-flop and the adjacent gates (to the left of the flip-flop on the schematic). This circuitry generates a ZERO signal, called PZERO-0, that is delayed one counter cycle. The PZERO logic operates in the following manner:

- Whenever the twelve-bit counter is loaded, the PZERO flip-flop is loaded with a one (PZERO false).
- When the State Controller enables the counter, the flip-flop delays the zero signal by one active clock cycle.

This means that if the counter is disabled during the same cycle that it reaches zero, the PZERO signal does not go true until the counter is enabled again. (When the counter is disabled, the PZERO flip-flop does not change state). The State Controller signal ENB12-0 enables this counter.

Slope Generator

Page A8-3 of the schematic contains three subblocks:

- Clock Buffers
- Axis Control Register
- Slope Generator Logic

The clock buffers are formed by four inverters and the associated output series terminator resistors. The input clock from the bus (VCLK-0) is buffered and fanned out to the rest of the board as signals BVCLK1-1 through BVCLK4-1.

The three-bit Axis Control Register takes D0 and D1 and makes the sign bits: XSIGN and YSIGN. These signals determine whether the addressing registers count up or down. (See the descriptions of *Y Axis Addressing Logic* and *X Axis Addressing Logic* next.) The Axis Control Register uses D2 to exchange the major and minor axes so that the Slope Generator needs to only calculate slopes between 0 and 45°. In other words, by selecting either X or Y as the major axis and selecting the correct signs, any vector's slope may be reduced to an angle between 0 and 45° (inclusive).

The direction control signals XSIGN and YSIGN are available on connector J350 for testing purposes. The exchange control signal is used in both its true and complement form by the two OR gates that generate the counter enable signals, XNEXT-0 and YNEXT-0. These signals are also available on J350 for testing purposes.

The remainder of the logic comprises the actual Slope Generator. Figure 6-15 shows a block diagram of that logic. Two 16-bit write-only registers (RX and RY) are multiplexed to one port of a 16-bit adder. The multiplexor is formed by enabling one register or the other onto a common bus. The 16-bit adder's sum outputs are the inputs to the accumulator register. The value in the accumulator register is the other input to the adder.

The Slope Generator circuit functions in this way. First, the processor programs all three registers with values it calculated for the Slope Generator (for the particular vector to be drawn). Each time the accumulator is clocked, its new value is the sum of the old accumulator value (before the clock) and RX or RY. The most-significant bit (sign bit) of the old accumulator determines which register is added to the accumulator. This bit also controls the select function of the multiplexor. This sign bit and the axis exchange bit (from the Axis Control Register) together determine which counter(s) are enabled by the Axis Control Logic Gates.

The firmware writes the initial values into the three registers as follows:

1. RX may be written directly and does not affect any other registers (signal LOADRX-0).

2. The firmware writes to the accumulator port (signal LOADRA-0). This does not cause the value to appear in the accumulator; instead, the accumulator is cleared to all zeros, and the value is temporarily stored in RY.

3. The firmware then writes the axis control value (via LOADAXIS-0). This signal acts as a clock that increments the accumulator once, causing the following actions:

   a. When the accumulator is cleared (in Step 2), RY is selected (sent) to the adder.

   b. Then, when the accumulator is clocked (by writing to the Axis Control Register), the new value becomes RY+ 0 (the value temporarly stored in RY). Thus the accumulator is effectively loaded without requiring a direct connection to the internal data bus.

4. Finally, the firmware writes only to the RY register (signal LOADRY-0).

The firmware can read the contents of the accumulator via the ACCREAD-0 signal applied to the bus drivers. Self Test uses this feature when testing the Slope Generator. The enable signal for the Slope Generator (DDA-0) comes from the State Controller.

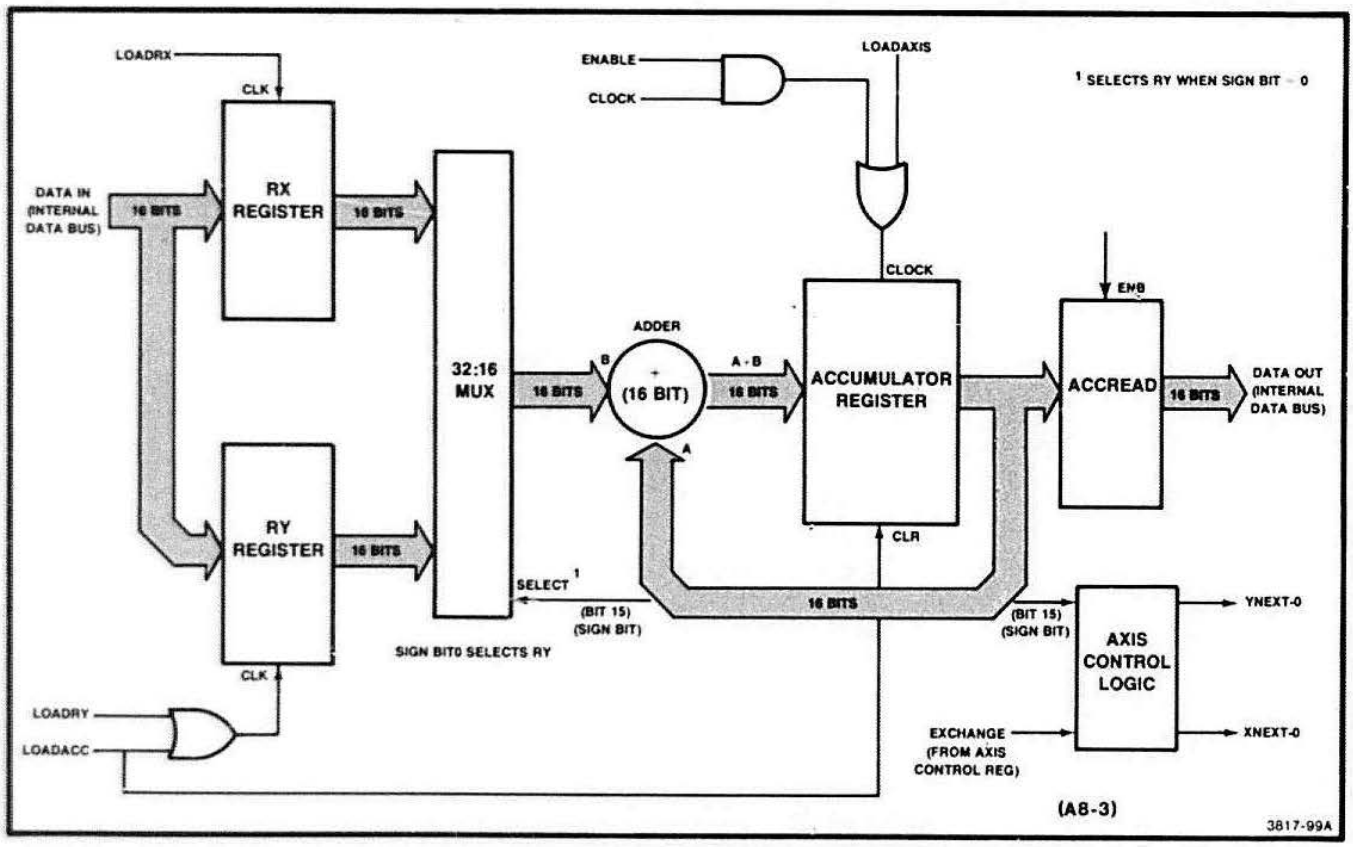


Figure 6-15. Slope Generator Block Diagram.

Y Axis Addressing Logic

The logic that generates Y axis addresses consists of four blocks (shown on the schematic) listed below.

- Y Counter
- Delta Y Counter
- Y and Delta Y Read Drivers
- Y and Delta Y Address Latches

Figure 6-16 is a block diagram that shows the structure of this addressing logic. The Y and Delta Y Counters consist of a pair of identical twelve-bit counters. These may be loaded from the twelve least-significant bits of the internal data bus. The contents of either counter may also be read back by firmware via the internal data bus. This happens only when the Vector Generator is not busy executing a command. The gates labeled "Y axis counter I/O steering" allow the processor to read the contents of these counters.

The Y counter is composed of three tristate counter chips. This counter is enabled by YCNTENB-0 (from the State Controller). The direction (count up or down) is controlled by the sign bit from the Axis Control Register (signal YSIGN-0). The Delta Y Counter is identical except for its count enable signal DYENB-0. Direction control is common with the Y counter.

The tristate outputs of both counters are connected on a common data bus. The counters are alternately enabled so that one or the other's outputs are connected to the bus. When the State Controller has control of the counter, signal Y-1/DY-0 selects which counter appears on the bus. Firmware is not allowed to read these registers until the controller is through running.

When the Vector Generator is at rest, the Y counter is normally present on the common bus. Signal YREAD-0 enables the read drivers, allowing firmware to read the Y counter. As firmware reads the Delta Y counter (signal DYREAD-0), that counter is placed on the common bus temporarily during the read cycle, in a manner similar to the control exercised by the State Controller.

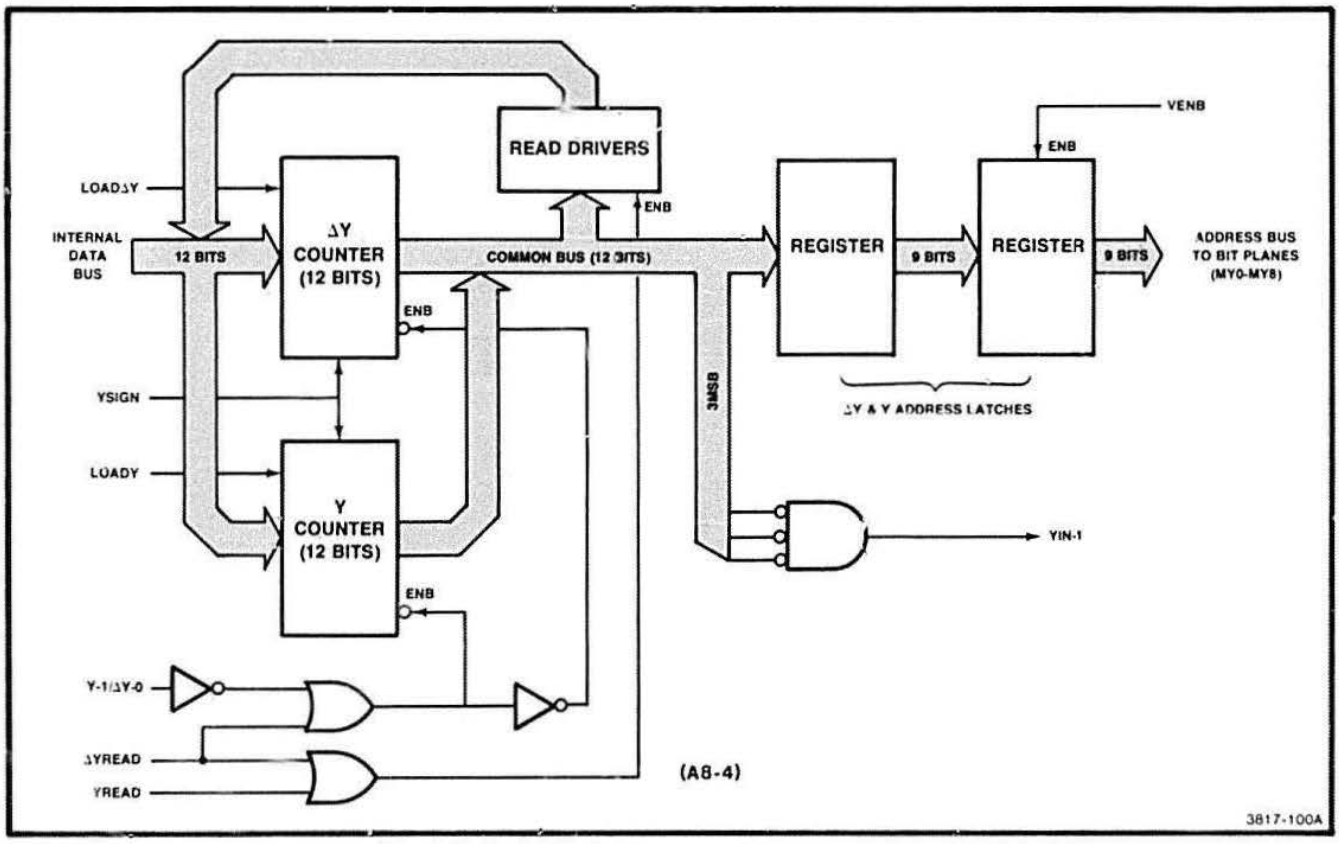


Figure 6-16. △ Y and Y Counters (Y Addressing Logic).

The common bus also connects tc the Y and Delta Y Address latches, which pipeline (delay) and buffer the address to the bit planes. While the Vector Generator is running, the State Controller coordinates the Y and Delta Y Address counters so that the correct address is present in the last address latch. Then the Video Controller generates a VENB-0 signal that places the address on the bus.

The Y/N-1 signal is generated whenever the three most-significant bits of the selected Y counter are zero. This signal informs the board control logic that actual memory cycles are allowed. The result is that this gate provides three bits of wrap-around protection, which creates a scissoring effect on the display image.

X Addressing Logic

The X Axis Addressing Logic is composed of these blocks:

- Pixel Counter
- X Counter
- X Address Latches
- Buffer Latches

Figure 6-17 illustrates the architecture of the X Axis Addressing Logic. The X address is composed of two parts, a PIXEL address and a WORD address. The pixel address is five bits and counts modulo 20 (00hex to 13hex).

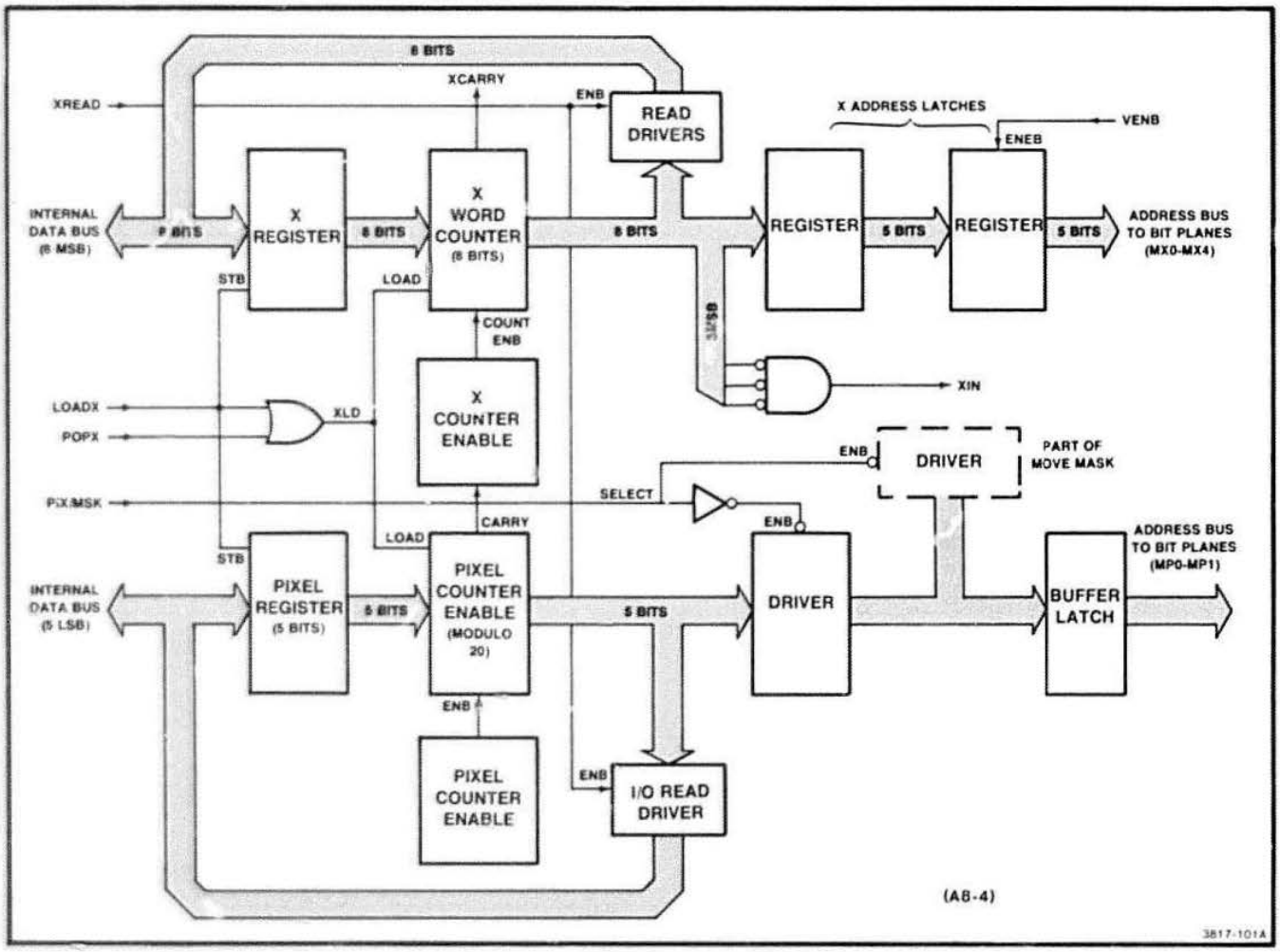


Figure 6-17. X Axis Addressing Logic.

The pixel address value carries into the X word address which is an eight-bit binary counter. As with the Y address, the three most-significant bits (MSB) of the X address are decoded to generate the scissoring signal XIN-1.

Like the eight-bit counter, both the pixel and X counters have a buffer register. This allows the State Controller to reload the last value written by the processor into the counters.

Note that both the pixel and X counters are synchronously loadable and count either up or down. Even though the counters are physically separate, the counter control logic (discussed later) enables a carry path from the pixel counter to the X counter, effectively forming one counter.

The five-bit pixel counter is composed of a flip-flop for the least-significant bit (LSB) and a decade counter for the 4 most-significant bits (MSB). This counter is written to and read from the 5 LSB of the internal data bus. A transparant latch forms the buffer register of the counter. The register enable signal (LOADX-1) and the counter load signal (XLD-0) are generated by two gates: one from the respective I/O write strobe (LOADX-0) and a second from the State Controller-generated signal POPX-0.

Refer to schematic A8-5 while reading the Pixel Counter theory. The Pixel Counter operates as follows.

1. The LSB always toggles when the counter is counting (in either direction).

2. It holds its state when the counter is not counting.

3. Or it may be loaded with the data from the buffer latch.

The three exclusive OR gates (XORA, XORB, and XORC) implement the necessary feedback paths (they operate as "programmable inverters" or "buffers"). Notice that the counter cannot be both enabled and loaded at the same time (microcode controls this). When in the hold mode (neither counting nor loading), gates XORA and XORB both invert, thus loading Q from the flip-flop back into the D input; this prevents the flip-flop from changing state. XORA is forced into the invert mode by the output of the first AND gate (NAND with inverting inputs), which is a logical 1. XORB is controlled by the PIXCNTENB-0 signal set to 1 (not counting). When XLD-0 goes low, the output of the OR gate is forced to a 1 (XORA still inverts) and the output of the first AND gate is the complement of the LSB from the buffer latch. This causes the flip-flop to receive the value in the LSB of the buffer latch when the next clock occurs. If PIXCNTENB-0 goes true (low) and XLD-0 is false (high), then XORB becomes noninverting while XORA remains inverting (as in hold mode); this causes the flip-flop to assume the toggle or count mode. Gate XORC generates the correct carry-out signal (low is true) so the buffer latch's higher four bits can enter the pixel counter chip. The XSIGN-0 signal provides pixel counter carry for either count direction.

XSIGN-0 controls the sense of the carry so that a negative true carry is generated when the flip-flop contains a 1 (when counting up) and when the flip-flop contains a 0 (counting down).

The four MSB of the pixel counter are connected to the synchronous decade counter. Direction control comes from XSIGN-0, and the enable is controlled by PIXCNTENB-0. A carry-out signal (PCARRY-0) happens when all five bits are one (count up mode) or zero (count down mode). The PCARRY-0 signal is generated by ANDing the zeros from both the counter and the flip-flop, which forms the LSB.

The five bits of output from the pixel counter connect to two tristate drivers. The I/O read driver drives the eight LSB of the internal data bus. The top three bits of this driver are Self Test bits that do not affect the operation of the pixel counter chip. The decoded read strobe XREAD-0 enables this driver. The other driver connects the pixel counter to the buffer latches via the internal bus. Data is driven onto the bus when the State Controller selects the pixel counter (the State Controller may also place the mask file data on these lines). Signal PIX-1/MSK-0 controls this select function.

The Buffer Latches buffer and delay:

1. the correct number of clock cycles,
2. the pixel counter or mask file data, and
3. some control signals.

The data on the MASK/PIXEL bus lines (signals MP0-0 to MP4-0) and VRQST-0 are delayed one clock cycle, while M0-0 and M1-0 are delayed two cycles to become MODE0-0 and MODE1-0 (bit plane control signals).

The other half of the X addressing logic is the X Counter. It is eight bits wide. The processor can write to it and read from it, via the eight MSB of the internal data bus. During I/O operations the X Counter and Pixel Counters both connect to the internal bus; while the Pixel Counter drives the five least-significant bits, the X Counter drives the bus's eight most-significant bits. The counter consists of two four-bit counters and a buffer latch that enables the State Controller to reload the counter with the last value written by I/O. The counter is read by an enabling driver. Reading and writing depends on the same set of control signals used by the Pixel Counter. Direction control is also common to both.

The Count Enable function, however, is independent of the Pixel Counter, so the State Controller can independently enable the X Counter via the Memory Control logic (discussed later). Note that the counter's enable input (XCNTENB-0) and its carry-out signal (XCARRY-0) are both connected to the memory control logic.

The data outputs of the X Counter are also connected to both the X Address Latches and the Read Driver. This two clock-cycle delay operates identically to the Y Address Latches. The output enable is the same VENB-0 signal from the bus.

In a similar manner to the Y axis, the three MSB of the X Counter value are decoded to generate the "scissoring" signal XIN-1. The address is driven onto bus lines MX0-0 to MX4-0 when the output latch is enabled.

Move and Wipe Logic

The Move and Wipe Logic is composed of two blocks:

- Move Masks
- First Logic

The Move and Wipe logic is used when the Vector Generator is executing in a Wipe (erase) or Block Move (scroll) mode. In this case, the meaning of the MP (Mask/Pixel) bus signals change. Instead of representing a pixel address within a word (pixel counter), the signals become a control field, where each line controls the action of a four-pixel group located within the word addressed by the X counter (see *Raster Memory Board Operating Modes*, later in this section).

The function of these signals is to define the left and right edges of a wipe or move to a group of four bits within a word, but not resolved to an individual pixel. In this mode, the data on the MP address lines comes from the Move Masks logic. This logic consists of a four-register port that may only be written by I/O (controlled by LOADMASK-0). The data to be written comes from the five LSB of the internal data bus. The code in Bits 8 and 9 of the internal data bus determines which register is loaded. Thus part of the data word (16 bits) written to the register determines which register is loaded, thereby squeezing four registers into one I/O address.

The logic states of two control lines (FIRST-0 and LAST-0) determine whether data may be read. The latter signal is merely the zero count of the 8-bit counter. Signal FIRST-0 is generated by the First Logic and delayed through one stage of the buffer latch.

Of the four possible states of the two control lines (FIRST and LAST), only three can occur on the read address pins of the Mask Registers. Table 6-2 shows the three possible read addresses. Note that address 1 is never selected for read, although it is possible to write to that address.

Table 6-2

MASK REGISTER ADDRESS SELECTION

FIRST-0, LAST-0	Selected Read Address
0,0	0
0,1	0
1,0	2
1,1	3

The FIRST-0 signal is generated in response to actions carried out by the State Controller on the X Axis Logic. Whenever the X axis is loaded (XLD-0), then the first flip-flop clocks to a 1 (FIRST-0 equals 0 or true). When neither XLD or XCNTENB is true, the flip-flop holds its state (either true or false); finally, whenever XCNTENB-0 is true, the first flip-flop clocks to a 0 (FIRST-0 false). FIRST-0, along with LAST-0, enables the Vector Generator to exercise independent control of the memories during the "first", the "last" and the "middle" accesses (of X word addresses) of a wipe or move operation.

(Read address 0 corresponds to the "first" access, address 2 to the "last," and address 3 to the "middle.") The Processor determines the contents of the mask registers, while the State Controller determines which register is used on which edge (first may be either the left or right edge depending on XSIGN). The State Controller also controls when the mask values appear on the bus by using PIX-1/MSK-0 to select either the Pixel Counter or Mask File.

Pattern Shift Registers

The Pattern Shift Registers contain the logic that sends dashed lines and dot matrix characters into the Raster Memory bit planes. Logically the shift register is 32-bits long and rotates toward the MSB of the high-order counter (see Figure 6-18). Each half of the composite shift register may be loaded and read from the internal data bus via its own set of read and write strobes

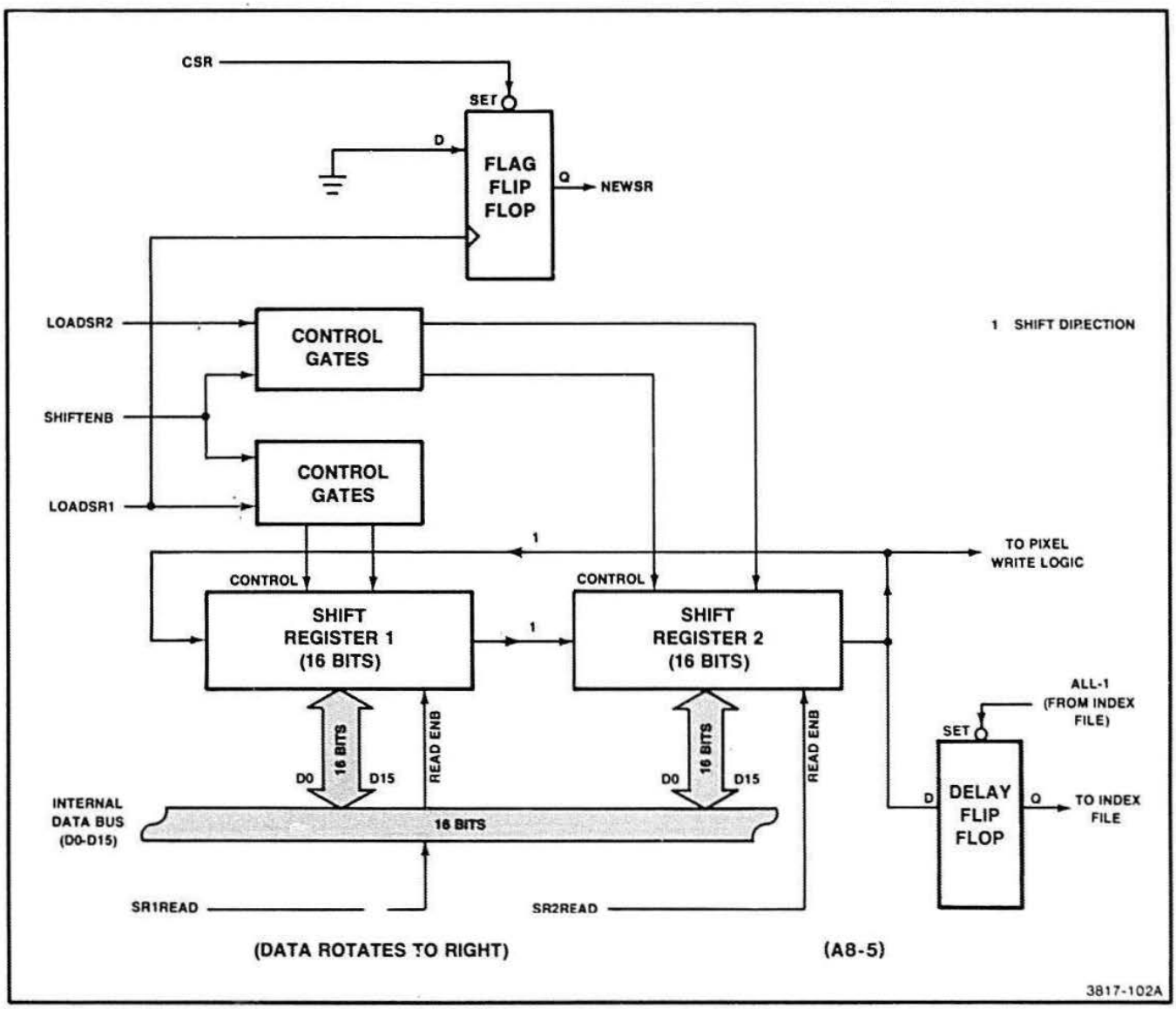


Figure 6-18. Pattern Shift Register.

(LOADSR1-0, LOADSR2-0, SR1READ-0, and SR2READ-0). Three modes in the shift registers are implemented by gates. When the respective LOAD signal is true, one half (16 bits) of the shift register is loaded. Both halves share a common shift enable (signal SHIFTENB-0) generated by the counter control logic. Notice that when Shift Register 1 is loaded (LOADSR1) the Flag Flip-Flop clocks to a zero, generating a true NEWSR-0 signal. This signal allows the State Controller to determine when this write action has occurred. The State Controller may then clear this flag by asserting CSR-0. Shift Register 1 is composed of U300 and U305, while U400 and U405 make up Shift Register 2.

Output from the rotating shift registers is taken from the high end of U504 (Pin 17) and passes directly to the Pixel Write Logic. This same data bit is delayed one clock cycle by a flip-flop (assuming this flip-flop is not held set by the index file signal) before connecting to the index file logic block.

Counter Control Logic

The Counter Control Logic is a 256-byte by four-bit ROM that implements the logic associated with control of the Y counter, X counter, Pixel Counter, and Pattern Shift Register. The outputs of the logic block are respectively YCNTENB-0, XCNTENB-0, PIXCNTENB-0, and SHIFTENB-0.

The inputs to the logic block consist of three bits of mode control from the State Controller (signals C0-1 — C2-1). These select a particular set of functions of the remaining input variables for each output. The input variables are:

- XCARRY-0 Pin 4 (carry-out of X Counter)
- INH-0 Pin 3 (last count from 12-Bit Counter)
- XENB-1 Pin 7 (Slope Generator X enable)
- YENB-1 Pin 6 (Slope Generator Y enable)
- PCARRY-0 Pin 5 (carry-out of Pixel Counter)

Table 6-3 describes the modes implemented for the eight mode values on signals C0-C2 (C0 is considered LSB).

Table 6-3

COUNTER CONTROL ROM MODES

Counter Mode	C2,C1,C0	Description
DRAW	000	The Pixel Counter, X Counter, and Y Counter are enabled by the Slope Generator and inhibited by INH-0. The Pixel Counter carries into the X Counter and the Pattern Shift Register shifts on each clock.
TEST 1	001	The Pixel Counter carries into the X Counter, which carries into the Y Counter (unless INH-0 is true, causing all counters to hold their state). Pattern Shift Register holds.
RASTER	010	Pixel Counter carries into X Counter (unless INH-0 is true) and then these counters hold. The Y Counter holds and the Pattern Shift Register shifts on each pixel count.
TEST 3	011	The Pattern Shift Register shifts, unless INH-0 is true, and then holds. The X, Y, and Pixel Counters all hold.
Y COUNT	100	The Y Counter counts if INH-0 is true; otherwise it holds. The Pattern Shift Register, and the Pixel and X Counters hold.
X COUNT	101	The Pattern Shift Register, and the Pixel and the Y Counters hold.
PIXEL COUNT	110	The Pixel Counter counts unless INH-0 is true and then it holds. The Pattern Shift Register, and the X and Y Counters hold.
HOLD	111	All Counters and the Pattern Shift Register hold.

Index File

The Index File circuit block works with the Pixel Write Logic to generate pixels. Part of the Index File block is the four video index (gray scale) value registers. These are arranged in two banks of two registers and are contained in U510. This block also contains a Mode Control Register (U520) that controls or selects the other registers in this circuit block. This register is strobed by LOADCC-1. Another part of this block is the Flag Control (U525) that produces two test flags: TF1 and TF2. These flags are inputs to the State Controller and are also used by the main processor to control the Vector Generator during certain routines. Also, the Index File has a flag flip-flop that is clocked to zero each time the processor writes to the Index File; thus asserting the signal NEWDAT-0. The Video Controller reads this flag and may clear it by asserting CDAT-0.

The Mode Control Register is a read/write register that accepts two bits (D0 and D1) from the internal data bus. The Mode Control Register input is located at I/O address F71A (Bits 0 and 1); its output is at F718 (Bits 9 and 10). Bit 9 is the bank selector, and Bit 10 selects the mode. There are two selectable color modes:

- Single Color/Shade Mode — When the Pattern Shift Register's SR31 is high, a pixel is written using the value in Register 1 of the selected bank. When SR31 is low, a pixel is not written.
- Dual Color/Shade Mode — When SR31 is high, a pixel is written using the color value in Register 1 of the selected bank. When SR31 is low, the value from Register 0 is used.

Basically, the first mode is a single index mode, such that a 1 in the shift register enables a PWRT, and a 0 skips the pixels. The second mode, enabled by ALL-1 = 1, is a two index mode; the shift register selects between two gray scale values.

The Index File receives nine bits from the internal data bus that have these functions:

- Bits 0-3: Video Index Value — Bit 0 affects plane 0, and Bit 3 affects plane 3. (Plane 3 is only used for the color option).
- Bit 7: Index Inhibit — When this bit is high, no value is written into the selected index register. However, TF1 and TF2 are set.
- Bits 8-9: Register Select Code — These bits select the Video Register that is to be loaded; this comes from the Mode Control Register. Bit 8 selects the register (0 or 1) while Bit 9 selects the bank (0 or 1).
- Bits 10-11: Test Flags 1 and 2 — These flags may be sensed by the State Controller. They are used for processor handshaking and for test purposes.

The output of the Index File is strobed onto the internal data bus by the CCREAD-1 signal. These output bits have the following meaning:

- Bits 0-2: Currently Active Video Index Value — These bits are Controlled by BANK-0, ALL-1, and the state of U414B.
- Bit 8: Current SR31 Value — State of the delay flip-flop (only when ALL-1 equals 1).
- Bit 9: Current Bank Selection — State of BANK-0.
- Bit 10: Current Mode Selection — State of ALL-1.

Pixel Write Logic

This circuit block generates a Pixel Write (PWRT-0) when enabled by PRQST-1, depending on several conditions. When the shade mode is single, a PWRT is generated whenever the circuit:

- Receives a pixel request (PRQST) from the memory control block,
- The value of SR31 is true.

When the mode select bit (from the Mode Control Register) is high, dual color operation is in effect. A PWRT is then generated for each pixel location (when PRQST occurs), regardless of the value of SR31.

Memory Control Logic

The Memory Control Logic consists of a 256-byte by four-bit ROM and three external gates that combine input terms into composite signals. The control ROM operates in a manner similar to the Counter Control block. Signals MC0-1 to MC2-1, from the State Controller, select the desired mode. Two output signals are generated (PRQST-1 and MRQST-0). PRQST-1 controls the generation of the PWRT signal that is sent to the bit planes. Signal MRQST-0 requests a memory cycle from the Video Controller. This request passes through a Buffer Latch to become Bus signal VRQST-0. (PRQST is discussed under the *Pixel Write Logic* heading.)

Signals XIN-1 and YIN-1 are ANDed to generate the input BIN-1 (Beam In). This input signal indicates that the writing beam is in a visible part of the bit map's address range. Likewise, signals ZER0-0 and PZERO-0 are gated with a strobe (ZENB-0) from the State Controller. The resulting signal allows the two outputs (INH-0 and PINH-0) to be either:

- the two zero signals from the 12-bit counter, or
- unconditionally false.

Table 6-4 lists a summary of parameters for the eight possible modes.

Table 6-4

MEMORY CONTROL ROM MODES

Memory Mode	MC2,MC1,MC0	Description
RASTER	000	This mode generates unconditional pixel writes when BIN-1 is true and INH-0 is false. Memory cycles occur whenever: PCARRY-0 is true, BIN-1 is true, and PINH-0 is false.
PIXEL AND MEMORY REQUEST	001	This mode generates an unconditional 001 pixel write and memory cycle. BIN-1 must be true. INH-0 (when false) inhibits PRQST-1, and PINH-0 inhibits VRQST-0.
MEMORY REQUEST	010	This mode generates an unconditional pixel write, unless PINH-1 is true.
PIXEL REQUEST	011	This mode generates an unconditional pixel write, unless INH-0 is true.
DRAW	100	Draw mode generates pixel writes on every cycle when BINH-1 is true, and generates memory requests whenever a memory boundary is crossed in the X or Y direction (BINH-1 must be free). INH-0 inhibits PRQST-1, and PINH-1 inhibits VRQST-1.
PIXEL MEMORY	101	An unconditional PRQST-1 is generated only if BIN-1 is true and INH-0 false.
MEMORY CYCLE	110	An unconditional memory cycle is initiated if BIN-1 is true and PINH-0 is false.
HOLD	111	No memory or pixel cycles are initiated.

State Controller

The State Controller controls and synchronizes the operation of the other logic blocks on this board. The "functions" performed by the Vector Generator are controlled by the state sequence encoded in the microcode and executed by the State Controller.

The State Controller operates as follows: A microaddress is applied to the state ROMs, whose outputs are held in the Microcode Latches. The data in the latches serves two purposes: (1) part of the current microcode word (in the latches) controls the generation of the next microcode address (the next state); (2) the remainder of the word is machine control for the logic blocks in the Vector Generator. The machine control bits appear to "tag along beside" the bits that control the sequencer. The program flow of the state sequencer can be modified by the state of several testable inputs; these come from various places in the Vector Generator logic blocks. This feature allows conditional operation capability, so logic can continue executing a sequence of instructions until a counter reaches zero.

Figure 6-19 is a block diagram showing the major parts of the State Controller. For clarity, this diagram omits clock signals, some microcode bits, and the test connectors used during board test. The 8-bit Address Sequencer is a pair of Type-2911 bit-slice sequencers; the resulting 8-bit microaddress appears on their Y output ports. This microaddress (signals A0 — A7) drives the address inputs of the microcode ROMs. Data out of the ROMs is connected to an array of microcode pipeline latches. ROM1 (U70) and its output latch (the instruction register) select the next address. Output bits I1 through I4 form the micro-opcode which connects to the inputs of the micro-opcode decoder. This ROM translates:

1. the four bits of opcode, and
2. the test condition signal,

into the control field needed by the address sequencer and two associated registers. Bits I5 through I7 select one input out of eight, from the test condition multiplexer. The remaining output of the instruction latch is the format control signal (FMAT-0).

The FMAT signal controls the meaning (format) of the bits from the two remaining ROMs. When FMAT-0 = 0 (logic low) the ROM outputs are loaded into the one device register. Similarly, when FMAT-0 = 1, the other two device latches receive the ROM output data. Pipeline latch U165 is part of the sequencer logic; it immediately places the address on the D ports of the 2911 Address Sequencers.

Two 2911 type Sequencers control the generation of microcode addresses. Block diagram, Figure 6-20, shows the internal layout of this pair of sequencers. This device chooses between four possible sources and places an address on its Y output. The output can come from one of these inputs:

- D Port input (direct transfer)
- Register
- Stack
- Microprogram Counter

The Microprogram Counter register always contains the current address plus one (regardless of which source is supplying the Y port address). Other control functions of the sequencer include:

- Two lines to control the action of the stack (File Enable and Push/Pop)
- A register control line (Register Enable)
- Output tristate enable for the Y port
- The ZERO control which serves to force the Y port to zero (regardless of the selected address source)
- The CIN and COUT (carry in and out) signals associated with the incrementer

The clock signal is not shown on the block diagram.

The function of the sequencer is controlled by the Microcode Decoder ROM. This ROM decodes: the opcode (from the instruction register), and the output of the test condition pipeline flip-flop; thus implementing the desired microinstruction. This decoder ROM also controls the output enables of the Pipeline Register and the Command Register. The Pipeline Register and its ROM supplies a jump address, so the Command Register jumps the Sequencer to the starting address of the microcode for the desired operation. (The jump address from the Pipeline Register is added to the address from the command register.)

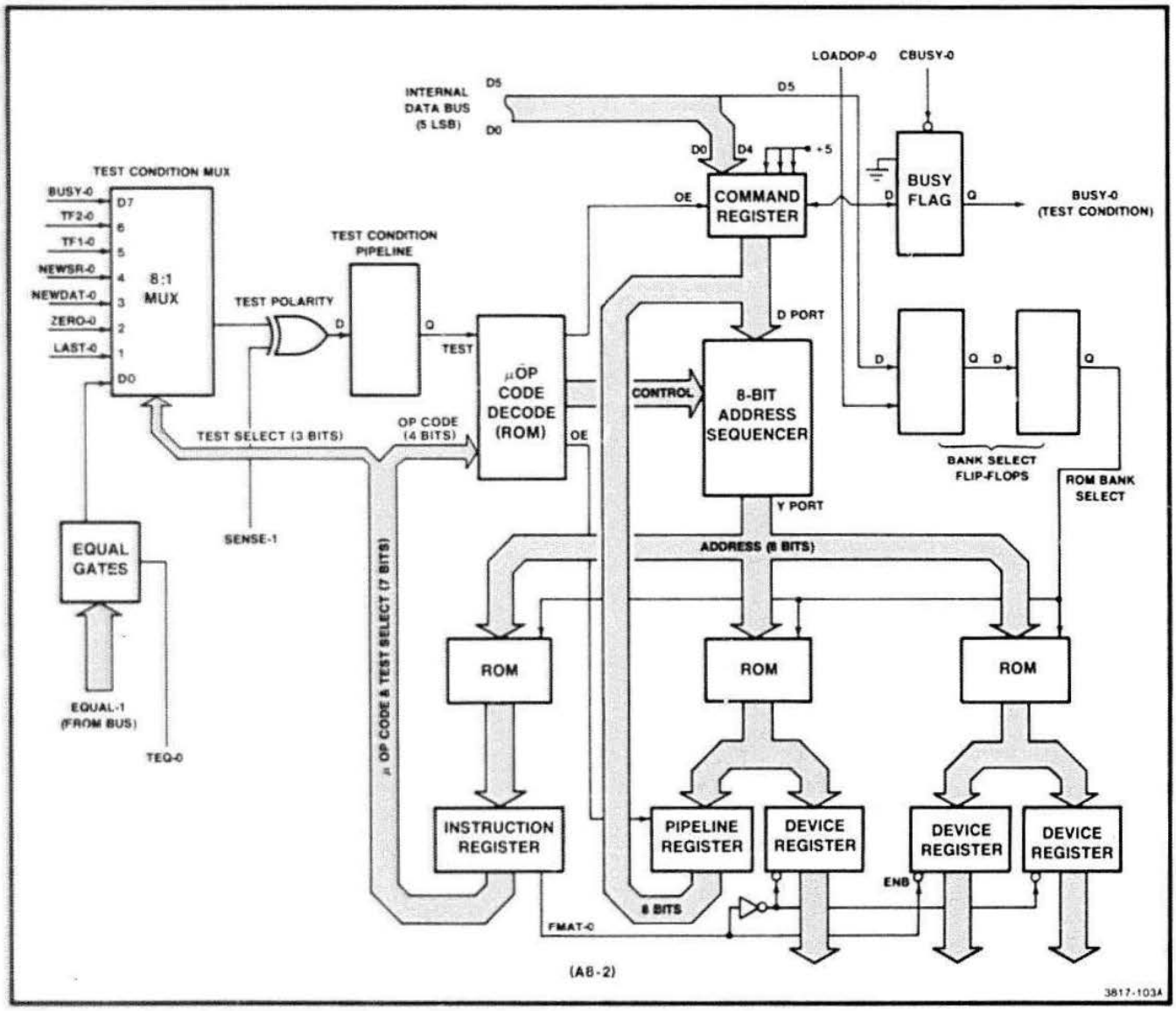


Figure 6-19. State Controller Block Diagram.

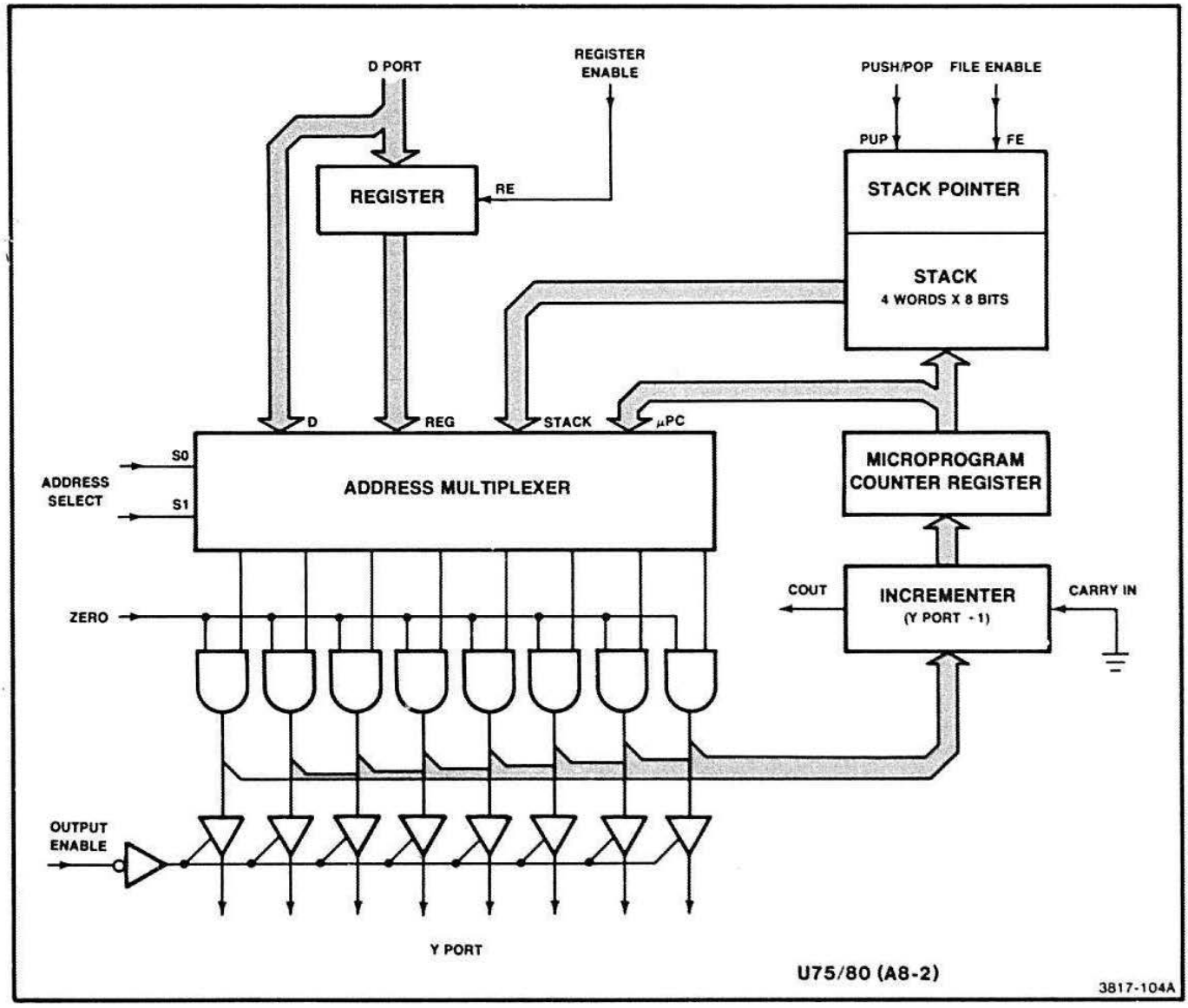


Figure 6-20. Address Sequencer.

Certain sequencer instructions depend on the state of a test condition. There are eight such test conditions, and a multiplexer selects the proper condition for the current instruction. The top three output lines from the microcode ROM act as a decoder/selector for the multiplexer. The selected test state is XORed with a SENSE-1 condition. Then it is delayed by a flip-flop, and finally enters the Opcode Decoder ROM. All the testable signals (except MUX inputs D0 and D7) come from the logic blocks already described. Input D7 is the command register busy flag. This flag indicates when the processor has written a command into the Command Register. The signal on the D0 input performs two functions. Normally this input is an unconditional low (fixed true or false depending on SENSE-1) used to make a conditional microinstruction UNconditional. If however, signal TEQ-1 is high, then multiplexer input D0 will reflect the inversion of the bus signal EQUAL-1. This feature allows branching based on the state of this signal; this is used for a video memory test written in microcode. Gates A, B, and D (collectively referred to as the "equal gates" on Figure 6-19) control the timing.

The remaining section of the sequencer includes:

- Command register
- Busy flag
- Bank select flip-flops

All of these devices are effected when the processor writes a command into the command register (from the Internal Data bus). Whenever this write occurs (signal LOADOP-0) the busy flag is clocked to a zero. The sequencer can test for this condition so it knows when to start executing a microcode routine. The contents of the Command Latch and the selected Microcode Bank determine which routine is executed. The five LSB (D0 to D4) of the Internal Data bus, and three ones (the three MSB of the register) are all clocked into the command register. This byte forms a jump address into a table in the top 32 words of the selected 256-word microcode bank. This table contains a pipeline jump to the actual starting address of the microcode routine. Using a table in this manner provides constant opcode values, even though microcode routines may change size if updates occur.

Internal Data bus bit, D5, forms a sixth bit of opcode and is clocked into a flip-flop by the I/O write LOADOP-0. It is then synchronized to the board clock, becoming an address bit to the 512-word ROM microcode store.

Jumper, W190, is for testability and restricts the system to Bank 0. W190 should be open. Note that the sequencer cannot change banks under program control. This restricts complete routines to a single ROM bank.

The busy flag is buffered onto the bus to become signal, VBUSY-0. This bit may be read as part of the Video Controller status word (see Video Controller theory of operation). This status bit informs the processor firmware when the Vector Generator is ready to start another operation.

Operating Modes

NOTE

Before studying the flow diagrams (Figures 6-21 through 6-25), refer to the explanation under the next heading: Interpreting the Flow Diagrams.

Figures 6-21 through 6-25, on foldouts at the back of this section, contain flow charts for the five main operations on the Display Bus. These operations are:

- Power-up (Figure 6-21)
- Writing a vector to the screen (Figure 6-22)
- Performing a blockmove (scrolling screen images) (Figure 6-23)
- Performing a wipe or erase of the screen contents (Figure 6-24)
- Writing a dot matrix (alpha text) character on the screen (Figure 6-25)

These flow diagrams are designed to provide a detailed analysis of Display Bus operation, showing how firmware routines manipulate the hardware to accomplish any given task.

The complete cycle of an opcode is summarized as follows:

First, the processor checks for a ready Vector Generator (VBUSY-0 = 1). When this condition is met, the processor firmware initializes the required registers in the Raster Memory Planes and in the Vector Generator. The last thing written by the processor is the opcode (to the Vector Generator's command register).

Meanwhile, the State Controller has been scanning the busy flag (signal BUSY-0) and detects when the command is written. The Controller then performs a jump through the table (mentioned earlier), and executes the selected microcode routine. When the routine is completed, the Vector Generator then clears its three I/O flags: New Data, New Shift Register, and Busy. It then resumes waiting for an opcode write (from the processor), at which time the entire cycle is repeated.

INTERPRETING THE FLOW DIAGRAMS

The symbols used on Figures 6-21 through 6-25 are standard, with a rectangular box representing each "task" accomplished by a state. A box alone represents a state that has no choice of where it proceeds next (unconditional). A box followed by a diamond, indicates a state that has a choice of where to go depending on the outcome of a test (conditional).

Each rectangular task box always has at least one region; some boxes have two (divided vertically into two regions). The leftmost region (always present) contains the next address information which is a description of State Sequencer activity. The rightmost region (not always present) shows what is being done to the other logic blocks in the Vector Generator. These blocks contain symbols or mnemonics that tell which signals and modes are active; these symbols are defined later in this discussion. If a mnemonic is not present, its associated hardware block is inactive (not enabled). If the right region is missing entirely, then all control to the external logic blocks are inactive and the State Sequencer is doing its own housekeeping (setting up for, or cleaning up after, a routine).

The number in the upper left corner of each box, represents the actual address of the microinstruction. These may be viewed using a logic analyzer when connected to the address outputs of the 2911 State Sequencers. Use J53 and sample on the rising edge of the clock signal, present on Pin 10 of J53. Trigger on an address within the routine and observe on the analyzer display. Remember that the routine must be executed in order to trigger.

Several things about the flow charts are not obvious and deserve explanation. First, due to hardware restrictions it is necessary to select the test code one cycle (state) before it is to be tested. A consequence of this is that a short loop will execute one cycle after the test becomes true. Second, because of the formatted nature of the microcode state latches (see State Sequencer description), it is sometimes necessary to include what appears to be an unnecessary state. An example of this is instruction 22 at the end of DRAW0 and DRAW1 routines. This instruction exists to "turn off" the PMCY state from the previous instruction. Microcode formatting precludes doing this in the JUMP instruction (number 23) since control for PMCY and the jump address are in different fields.

Mnemonics Used in Microcode Flow Diagrams

Most of these terms correspond to control signals that appear on the right edge of schematic sheet A8-2. The remaining terms are state names that are defined in Tables 6-3 and 6-4.

CBSY — When asserted, CBSY clears the Busy flag (signal BUSY-0).

CDAT — When asserted, the data flag in the Index File is cleared (signal NEWDAT-0).

CSR — When asserted, CSR clears the New Shift Register data flag (signal NEWSR-0).

DDA — When asserted, this signal enables the DDA (Digital Differential Analyzer) to compute slope information; when not asserted, the DDA holds its state.

DYENB — When asserted, this signal causes the DY Axis Counter to count on the next clock cycle; when not asserted, the counter holds.

DYSEL — When asserted, the DY Axis Counter contents are output to the MY bus; when not asserted, the Y Axis Counter contents are output instead.

ENB8 — This signal enables the 8-Bit Counter to count on the next clock cycle; when not asserted, the counter holds.

ENB12 — This signal enables the 12-Bit Counter in the same manner as ENB8 controls the 8-Bit Counter.

MASK — When MASK is asserted, the MASK file is output to the MP (move pixel) lines on the Display Bus. When not asserted, the Pixel Counter contents are output on the same lines.

NEWSR — New data is in State Sequencer Shift Register.

POP8 — This signal causes the 8-Bit Counter to reload (on the next clock cycle) the value last written by the Processor to the counter.

POPX — This signal causes the X-Axis and Pixel counters to reload (on the next clock cycle) the value last written to the counters by the Processor.

WAIT — This signal, when asserted, causes the Write Sync logic to delay acknowledging a Processor write (to the display system) until such time as WAIT is unasserted.

ZENB — When asserted, this signal allows the ZERO signal (from the 12-Bit Counter) to inhibit both the Counter and Memory control logic. This is necessary because of the extra loop caused by test condition delays within the controller. In other words, hardware shuts off the Memory and Counter controls at the end of the vector, and the microcode loops one more time before it sees the end of the vector state. When ZENB is not asserted, the Counter and Memory control logic behaves as if ZERO were false.

Memory Mode Control Field Mnemonics

The behavior of the memory planes during a vector memory cycle is determined by a two-bit code sent onto the Display Bus by the Vector Generator. See descriptions of memory plane operations under Raster Memory Board theory. The mnemonics for these boards are:

DEST — This mode asserted causes a Destination cycle.

READ — When this mode is asserted, the memory cycle will be a Processor Read cycle.

SRC — When this mode is asserted, the memory cycle becomes a Source cycle.

If none of the above modes are asserted, the cycle defaults to an Operate cycle, the standard vector drawing mode.

Counter Control Field Mnemonics

The behavior of the X axis, Y axis, Pixel, and Pattern Shift registers is controlled by a 3-bit field that may assume any of eight values. These are explained in the description of the Counter Control logic block. The following identifiers are defined in Table 6-3 (Counter Control ROM Modes):

DRAW = Draw (000)

RAST = Raster (010)

XCNT = X Count (101)

YCNT = Y Count (100)

Memory Cycle Control Field Mnemonics

The logic that generates the pixel writes and the memory cycle requests (signals PWRT and MRQ) is controlled by another 3-bit field. This field may assume one of eight values, but only the modes that are used in the flow charts are listed here. For detailed operating theory refer to Memory Control Logic in the accompanying text. The following identifiers, as used in the flow charts, are defined in Table 6-4 (Memory Cycle Control ROM Modes):

DRAWM = Draw Mode (100)

MEM = Memory Cycle (110)

MRQST = Memory Request (010)

PMCY = Pixel and Memory Request (001)

RASM = Raster Mode (000)

Subroutine Names

The routines/subroutines that comprise the flow diagram are named and defined here.

- ASCII Dot Matrix Routine — This routine produces alphanumeric characters in a dot matrix pattern.

  W8 (subroutine) — Writes eight pixels across and goes back to the first pixel location on the next line.

  W16 — Writes two lines of eight pixels each, and goes back to the first pixel on the third line.

  W32 — Writes four lines of eight pixels each, then goes back to the first pixel on the fifth line.

  FLAG — This routine loops while checking the flag that indicates new data in the Shift Register.

- BMOVE — This routine executes a block-move (scrolls screen contents).

- DRAW — These routines (DRAW0 and DRAW1) create vectors by counting and drawing, pixel-by-pixel, in the desired X and Y directions.

- POWER UP — This routine clears registers and sets up the State Sequencer for subsequent routines. This routine contains a pointer to the Jump Table.

- WIPE — This routine wipes (erases) the screen in preparation for new screen data.

RASTER MEMORY BOARD THEORY

INTRODUCTION

The Raster Memory Board stores graphic images in its 16k x 20 bit memory plane. Each X-Y location in its memory corresponds to a pixel point on the display screen. The memory plane data then is interpreted by a gray scale map, so the display may present shaded monochrome images. The optional Dual Plane Raster Memory board contains two additional memory planes. The resulting three planes may be grouped by the firmware or treated separately to give shaded or layered images. If all three planes are grouped together, their data can be used to paint an image with 2x2x2 (8) shades of gray. If each plane is treated separately, the display will contain three separate images (one per layer) with only two shading values allowed. Another possibility is two layers, one of which receives data from two memory planes (allowing it four (2x2) shades of gray). The remaining layer will only allow two shades of gray. The map can also be programmed to let each of the one to eight allowable shades represent any gray tone we choose.

The Raster Memory Board receives its graphic data from the Vector Generator board; which operates on command from the processor. Timing and control signals for this Raster Memory board come from the Video Controller board.

The Raster Memory board provides the following functions:

- Controls the memory plane RAMs for the display.
- Provides termination for the Display Bus. As such, the Raster Memory board occupies the slot in the card-cage furthest to the right (last one). All signals except SCAN SYNC and DAC0 — DAC3 are terminated on this board.
- Modifies data as desired by the processor and directed by the Vector Generator. It then passes the data back to the Video Controller (and then to the display).
- Allows data to be read from memory plane 2, the memory plane located on this board, which is always available. The Dual Plane Raster Memory board (when installed) accesses data in memory planes 0 and 1, located on this optional memory board.
- Decodes the block of addresses that the board uses for memory control and processor communication.

RASTER MEMORY BOARD OPERATING MODES

Refer to Figure 6-26 while reading the following descriptions of operating modes for the Raster Memories.

Decode and Startup Cycle

This topic describes the introductory operations required to place the Raster Memory hardware in one of its operating modes. First, the address of the pixel to be modified, MP0-0 through MP4-0, is applied to the address decoder as BMP0-0 through BMP4-0. PWRT-0 enables the gate of this address decoder. The two highest bits (BMP3-0 and BMP4-0) are decoded into P0, P1, and P2; these are the strobes for the three parallel latches in the Vector Data Input block. The Address Decoder decodes the five-bit pixel address (BMP0-0 to BMP4-0) into three groups of eight bits. Only the first 20 bits are used; these are applied to the "A" inputs of the RAM Enable block. The RAM Enable then sends the RAS0 to RAS19 to the memory plane RAMs in the RAM Array block. When operations on the current word have been completed by the Vector Generator, it requests a vector cycle via the Video Controller board. The refresh and vector cycles are described next.

Refresh Cycle

Refresh is the normal steady state mode of this board. In this mode the RAM data is written directly to the screen. The data is not written back into the RAM so the ALU mode does not affect this operation. The contents of the block move source and processor data latch are not modified during a refresh cycle. The RAS Enable latches are overridden during a refresh cycle, allowing all 20 bits of data to be read.

The REF-0 signal starts this refresh cycle. During this cycle all of the RAMs must receive a RAS signal (to read the data for display on the screen). REF-0 going low sets the B input NAND gates of the RAM Enable block to a high; and all the B inputs of the multiplexers go high. RAS-1, from the Video Controller, strobes the five multiplexers of RAM Enable so the RAMs are enabled to refresh the screen.

REF-0 is inverted and applied to the 'mode decoder' in the RAM Control block; this drives all of its outputs high. One of these outputs controls the selection of the RAM Enable multiplexers. As the select line goes high, the B inputs of the multiplexers are selected. Then when RAS-1 goes high, B is sent from the five multiplexers as RAS0-0 through RAS19-0; these enable the RAMs.

During refresh, the normal read/modify/write cycle does not write. This is caused by BREF-0 (going through an OR gate) which disables the write pulses (W1-0 through W4-0) to the RAMs. The ALU modes are not enabled and are unaffected by the BREF-0.

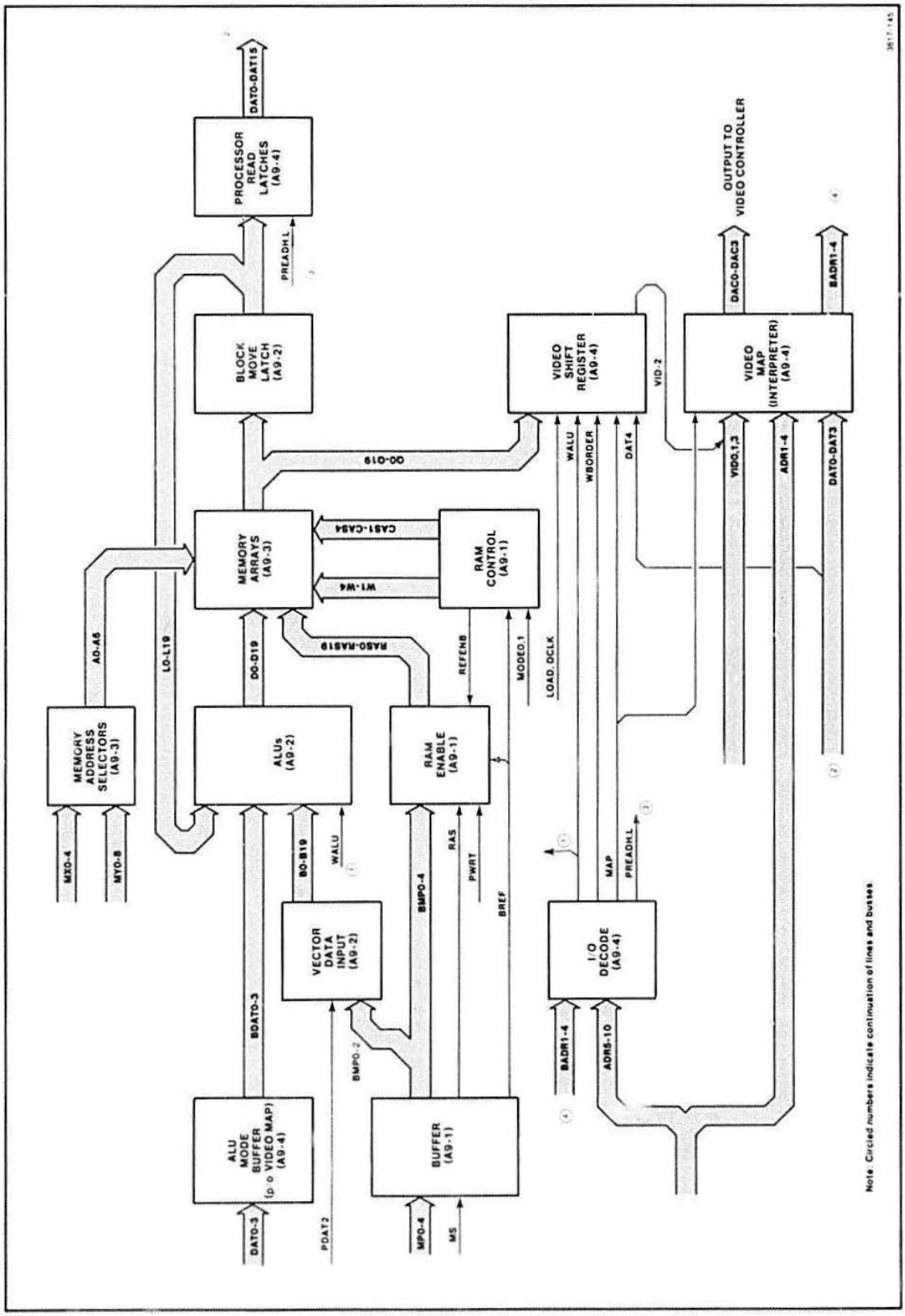


Figure 6-26. Raster Memory Simplified Block Diagram.

Vector Cycles

There are five variations (modes) of the vector cycle; these modes are listed in Table 6-5 and described in the following text. The two "mode bits" tell the Vector Generator which operation to perform on the data for each mode. The definitions of these bits are listed in Table 6-5.

Table 6-5

MODE0-0 AND MODE1-0 DECODER

MODE0-0	MODE1-0	Resulting Mode
0	0	Block move (destination)
1	0	Block move (source)
1	0	Block move (erase)
0	1	Processor Read
1	1	Operation mode

The vector cycle starts with a VENB-1 initiating a transfer of data from the input latches to the output latches of the Vector Data Input block. The addressable input latches are then cleared (by VACK-0) for the next vector cycle. This allows the Vector Generator to start generating the pixel data for the next word during the current 400 nsec vector cycle.

A vector cycle sets high the MODE0 and MODE1 inputs to the RAM Control, which forces its decoder's Y3 output low. This selects the RAM Enable inputs from the Addressable Latches, which causes only the pixels that need modification to receive a RAS. Those pixels that are not modified are not addressed.

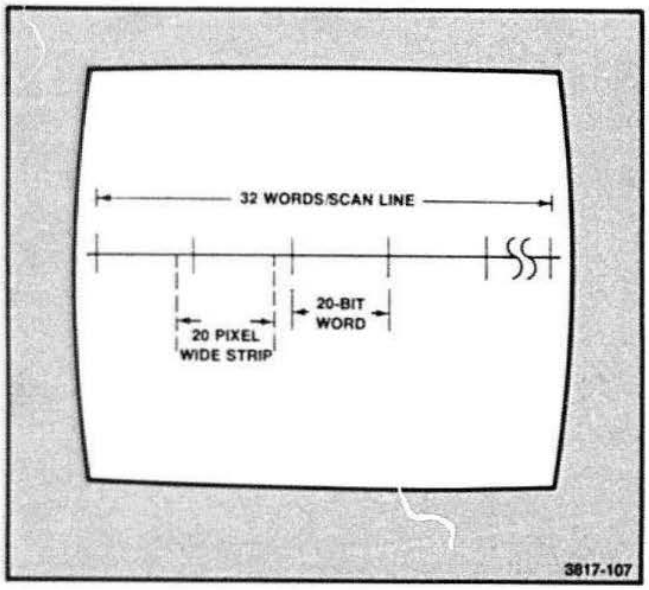
NOTE

A RAM must receive a RAS and a CAS in order for the system to read its data. Data may be written into the RAM only after it receives a RAS, a CAS, and a write pulse.

Operate Cycle. When a vector cycle is requested in operate mode, the RAM data is read, modified, and written back into the RAMs. However, depending on the vector being drawn, there are 20 RAS enable latches that control which RAMs are enabled by the cycle. This allows individual pixels to be modified without first reading and rewriting the entire contents of RAM. The ALU mode is a factor here and must be set by the processor to achieve the desired data modification. The block move destination data latch is modified during an operate cycle.

Blockmove Source/Destination/Erase. Blockmove is actually three different operating modes, all of which are intended to speed up the process of modifying data on the screen. These modes operate on parts of 20-bit words, rather than on one pixel at a time (as would be the case in vector mode). Blockmove moves data in the vertical direction only. It can replace data from the source locations with other data values as it performs the move; this is 'blockmove source mode.' Or, it can write a modification of the data to the destination location of the move: 'blockmove destination mode.'

Blockmove is normally used for scrolling of the display contents. During blockmove it is necessary to move only portions of the entire display. The Vector Generator's microcode accomplishes this by manipulating a 20-pixel wide strip; not necessarily falling on 20-bit word boundaries. The 20-pixel wide strip can be any 20 consecutive bits in a line. See Figure 6-27.



A tradeoff was made between allowing one-pixel strip moves (to obtain the best resolution), and the 20-bit word move (which gives the poorest resolution). The 20-bit word is divided into five four-bit sections which give four-bit screen resolution on move cycles. When additional resolution is needed, vectors must be used.

The 20-bit word is broken into five four-bit sections by changing the meaning of the MP0-0 through MP4-0 lines from pixel addresses to four-bit field designators. This change is done in the Vector Generator and the Raster Memory. The Vector Generator sends zeroes over MODE0-0 and MODE1-0 lines to request destination cycles, and it sends a one on MODE0-0 to request a source cycle for the move. The mode decoder in the RAM Control block controls the related circuitry in the RAM Enable and other blocks.

'Erase' is a type of blockmove source operation. The ALU mode data, necessary to produce an erase, is written to the source address.

Processor Read Cycle. This cycle causes the processor to read the full 20-bit field of data that is requested by the Vector Generator. This data is latched so the processor can read it when it wants to. Also, four bits of Self Test data are latched for the processor to read.

CIRCUIT BLOCK DESCRIPTIONS

The following block descriptions correspond to the Raster Memory and Dual Raster Memory circuit blocks as labeled on the schematic sheets A9-1 through A10-7 (in Volume 2 of this manual). Figure 6-28 is a detailed block diagram of the Raster Memory Board, showing how its circuit blocks relate to each other.

Buffer

The Buffer section provides isolation for the signals coming into the board from the Display Bus. The Buffer also converts most of the ECL signals to TTL signals. All signals, except SCAN SYNC and DAC0 through DAC3, terminate on the Raster Memory Board. The Buffer contains most of these line termination resistors.

Addressable Latches

Typically, the Vector Generator determines that a certain pixel needs to be modified. Then the Addressable Latches receive the vector serial data that comes from the Vector Generator. This vector serial data consists of the address bits: BMP0-0 through BMP4-0, and PWRT-0. The address bits correspond to the CRT electron beam position in the 20-bit word. The PWRT-0 signal latches the current data in the decoders. The data in this case is always a "1" on the decoder inputs.

RAM Enable

The RAM Enable circuitry directs the RAS signals to the RAMs that are needed for the currently selected mode of operation. This 2-to-1 multiplexer determines which input from the Addressable Latches, or the four-bit "zone input" (blockmove), are used to generate RAS signals during the current cycle being performed.

RAM Control

RAM control and the write disable circuitry are in this block, along with the write enable/disable flip-flop. The flip-flop is a write-to-memory control switch. MODE0-0 and MODE1-0 from the Vector Generator are decoded by the mode decoder to perform the operation on the raster memory. A buffer drives the write (W1-0 to W4-0) and column address strobe (CAS1-0 to CAS4-0) lines that enter the RAM memory array. The 51 and 43 Ω resistors keep the output signals clean and provide series termination.

The RAM Control block performs the following types of operations:

- Refresh of the screen
- Memory read cycle
- Vector cycles (The vector cycle was described earlier in this section.)
- Block move source and destination

Other vector cycles not specifically covered include:

- Alphanumeric characters
- Vectors
- Imagery data (Appears to Raster Memory as a Vector Cycle)

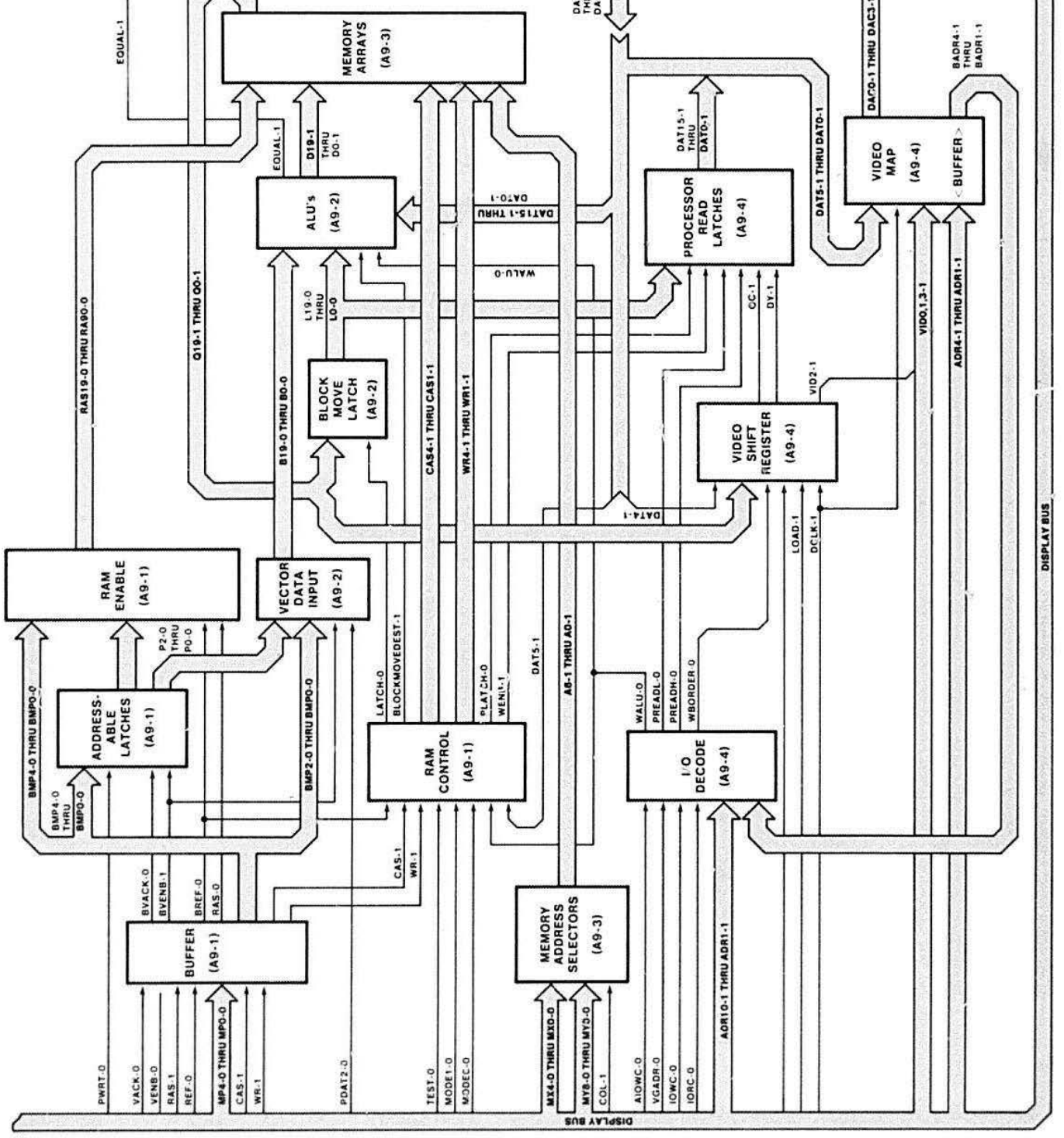


Figure 6-28. Single Plane Raster Memory Board Block Diagram.

Vector Data Input

The Vector Generator Board sends vector data to the ALUs[1] via this set of addressable latches. Serially transmitted pixel data enters these latches as PDAT2-0. (Memory Plane 1 receives PDAT1-0, and Memory Plane 0 receives PDAT0-0). The first of the two sets of latches places each pixel in a location in a 20-bit word. This location is specified by the address decoded from the combination of BMP0 to BMP2, and P0 to P2. P0 to P2 selects one of three chips, and BMP0 to BMP2 selects an eight-bit address in the chip. (Only 20 of the 24 possible combinations are used.)

[1]See description of an ALUs circuit block under next heading.

The second set of latches (D flip-flops) stores the outputs of the first set (pipeline style) until the data is needed by the ALUs. This allows the first latch to be decoding the next pixel, while the second is waiting for the ALU. These addressable latches are not cleared by VACK-0.

Figure 6-29 is a block diagram of the Vector Data Input circuitry, which appears on schematic sheet A9-2. Notice that another set of buffers, paralleling the first, are pictured but NOT installed on this board. This is the shaded area on the block diagram. This additional circuitry would buffer data from a future enhancement circuit. Notice also that the output enable signal, EXT-0, for the pipeline latch, is not used. If this additional data path were used, the EXT-0 would select one or the other of these paths.

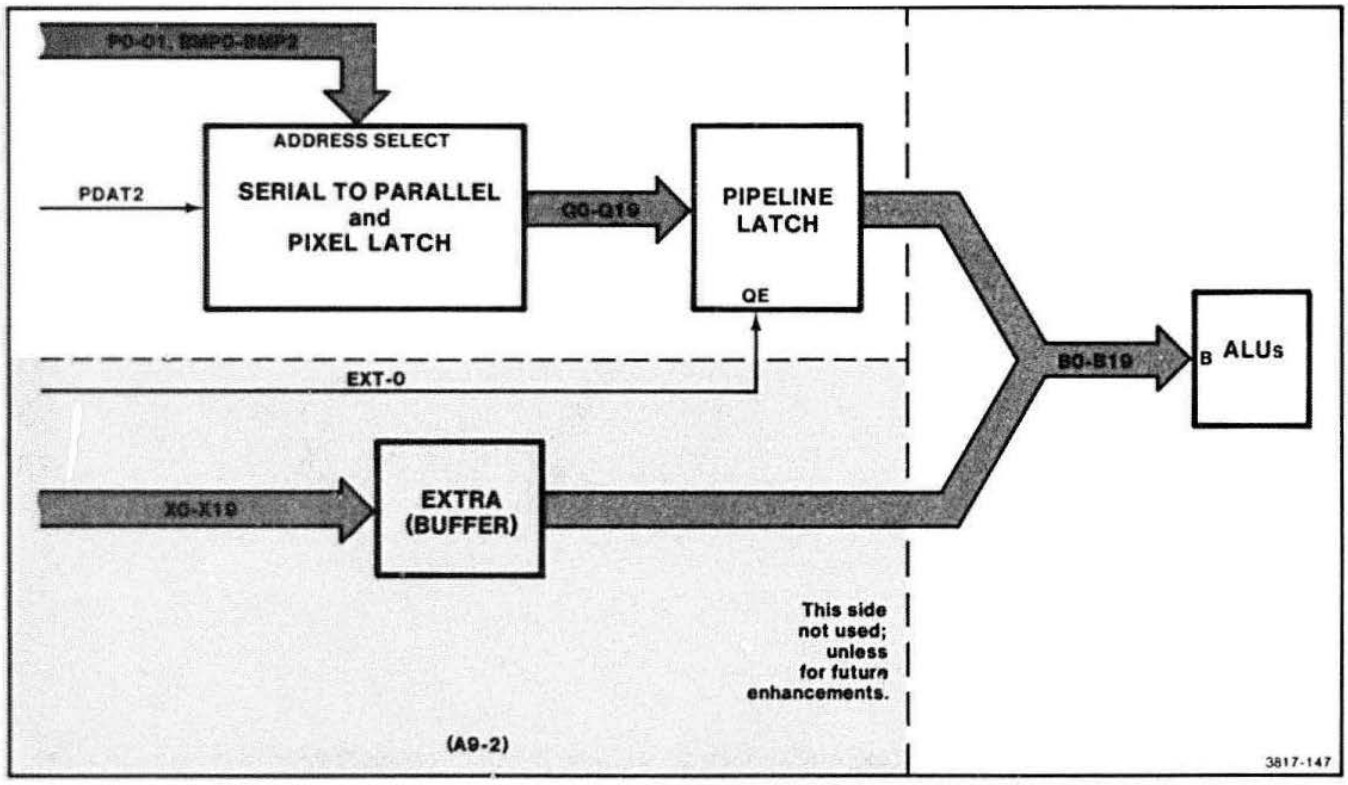


Figure 6-29. Vector Data Input Block.

ALUs Circuit Block

The ALUs (Arithmetic Logic Units) modify pixel data as desired by the processor and set by the mode latch (which selects the ALUs' logic functions). See Figure 6-30.

The source of data for the ALUs is:

- either the Vector Data (via Vector Data Input), or
- the Memory Array RAMs (via the Block Move Latch).

The ALUs do not operate on a pixel unless a word is being modified. A four-bit selector latch controls the logic mode of the ALU. There are 16 different modes the ALU can operate in; these are shown in Table 6-6.

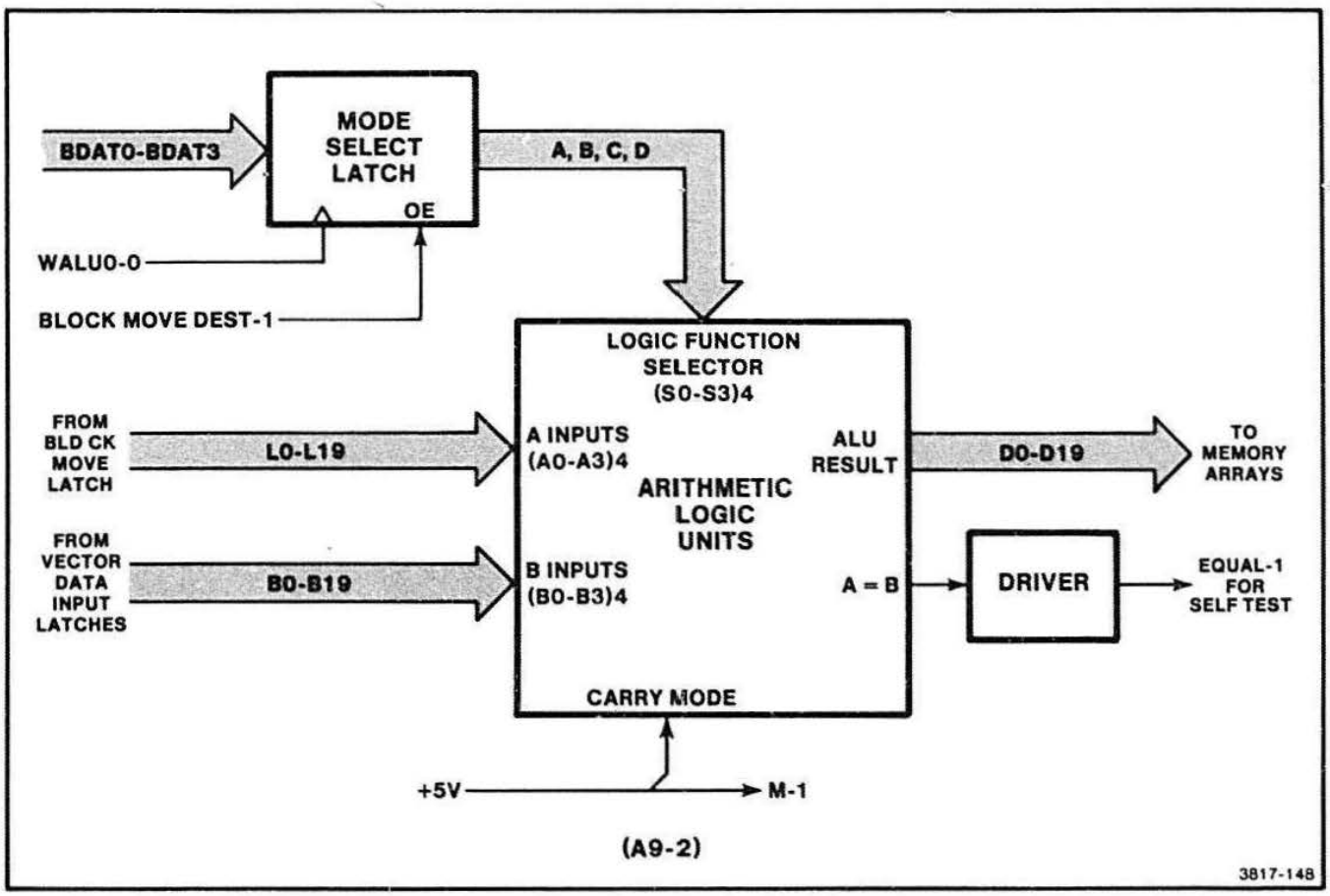


Figure 6-30. ALUs Circuit Block Diagram.

Table 6-6

ALU FUNCTION SELECTION

Selector Code[a]	Logic Functions[b]
Mode 0	F = NOT (A)
Mode 1	F = NOT (A OR B)
Mode 2	F = NOT A AND B
Mode 3	F = 0
Mode 4	F = NOT (A AND B)
Mode 5	F = NOT (B)
Mode 6	F = A XOR B
Mode 7	F = A AND NOT B
Mode 8	F = NOT A OR B
Mode 9	F = NOT (A XOR B), [A XNOR B]
Mode A	F = B
Mode B	F = A AND B
Mode C	F = 1
Mode D	F = A OR NOT B
Mode E	F = A OR B
Mode F	F = A

[a] The four-bit mode selector lines, A through D, are binary decoded into the ALU modes 0 through F (hex).

[b] A and B are the two data inputs to the ALU. F is the resulting data output.

The A = B output, which becomes EQUAL-1, is used only for Self Test. If the ALU is set to F = A XNOR B (MODE 9) and the two data inputs, A and B, are equal; the EQUAL-1 output will go high. The EQUAL outputs of the ALUs are all connected together and interface to the Display Bus via the transistors. The transistor circuitry is a simple buffer onto the bus. All 20 inputs must be the same to produce an EQUAL-1 indication from the ALU.

Blockmove Latch

The Blockmove Latch stores the data from the source cycle (of a blockmove) until it is time for the destination cycle. This set of latches are only used during block moves.

At the beginning of a source cycle, LATCH-0 (latch input enable, G) is held high during Memory Array CAS time; this causes the latch to wait until the RAMs are through sending data to its inputs. With stable data on the inputs, LATCH-0 then goes low, thus loading this source data into the latches. The data remains here through the destination cycle.

The destination cycle proceeds in the following manner. Since the Blockmove Latch outputs (OE) are always enabled, its data is transferred out as soon as the ALUs are enabled. The BLOCKMOVEDEST-1 signal disables the ALU Mode Latch, which places the ALUs in F = A mode; this allows the source data to enter and pass through to the RAMs exactly as read from the Blockmove Latch. The latch load control, LATCH-0, remains low during this destination cycle.

Memory Address Selectors

The Memory Address Selectors consist of flip-flops functioning as address buffers and multiplexers for the RAM Array addresses. The 43 Ω resistors shown on schematic sheet A9-3 provide series termination for the address lines. The 14 bits of address for the X — Y position on the screen come from MX0 through MX4 (X position) and MY0 through MY8 (Y position).[2] These lines come off of the bus and are time multiplexed into the RAM address inputs.

First, MX0 through MX4, MY1, and MY2 are applied to the RAMs. The RAS pulse latches this address into the RAM Array addresses. The 43 Ω resistors shown on address designated by MY0 and MY3 through MY8. CAS then latches the RAMs for this address. A time delay AND gate equalizes the delays in the RAM timing system.

[2] There are fewer X than Y address bits (though the screen is wider than it is tall) because the X dimension is divided into 20-bit words.

Memory Array

The Memory Array is a 16k by 20-bit set of RAMs that correspond to Bit Plane #2. The pixel data stored in these RAMs can be manipulated by the ALUs to achieve the arrangement of data as desired by the processor; finally, this data is sent to the Video Map (interpreter) on its way to the display screen.

It is convenient to think of the Memory Array as consisting of a block of RAM divided into 20-bit segments (words). Each of the twenty RAM chips shown on schematic sheet A9-3 stores one bit of this 20-bit word. Each RAM has room for 16k bits. Figure 6-31 is a simplified view of the Memory Arrays and the Memory Address Selectors, showing how the address and data buses flow. As indicated, there are 20 data inputs (D0 through D19), and 20 data outputs (Q0 through Q19). The 20 RAS lines (RAS0 through RAS19) correspond to the 20 data bits. The remaining write enables (W1 through W4) and column address strobes (CAS1 through CAS4) are buffered by the RAM Control block before entering the RAM chips.

The output data bits (0 through 19), and their RAM chips, are arranged from left to right across the top of the board (viewed from the component side).

Processor Read Latches

The Processor Read Latches allow the memory plane data to be read by the processor or other hardware off of this board. The processor first tells the Vector Generator to address the desired word in the Memory Plane. The processor then issues a memory read (MREAD) opcode. In response, the Vector Generator does a memory read cycle; it sets the MODE0-0 and MODE1-0 signals to 0, 1. This sets the RAM Control to read a cycle (no writes allowed). When CAS arrives, during a memory read cycle, the Processor Read Latches are loaded with the data that is coming out of the RAMs. The processor can now read these latches and use the data as it chooses. (The ALU has no effect on this operation.)

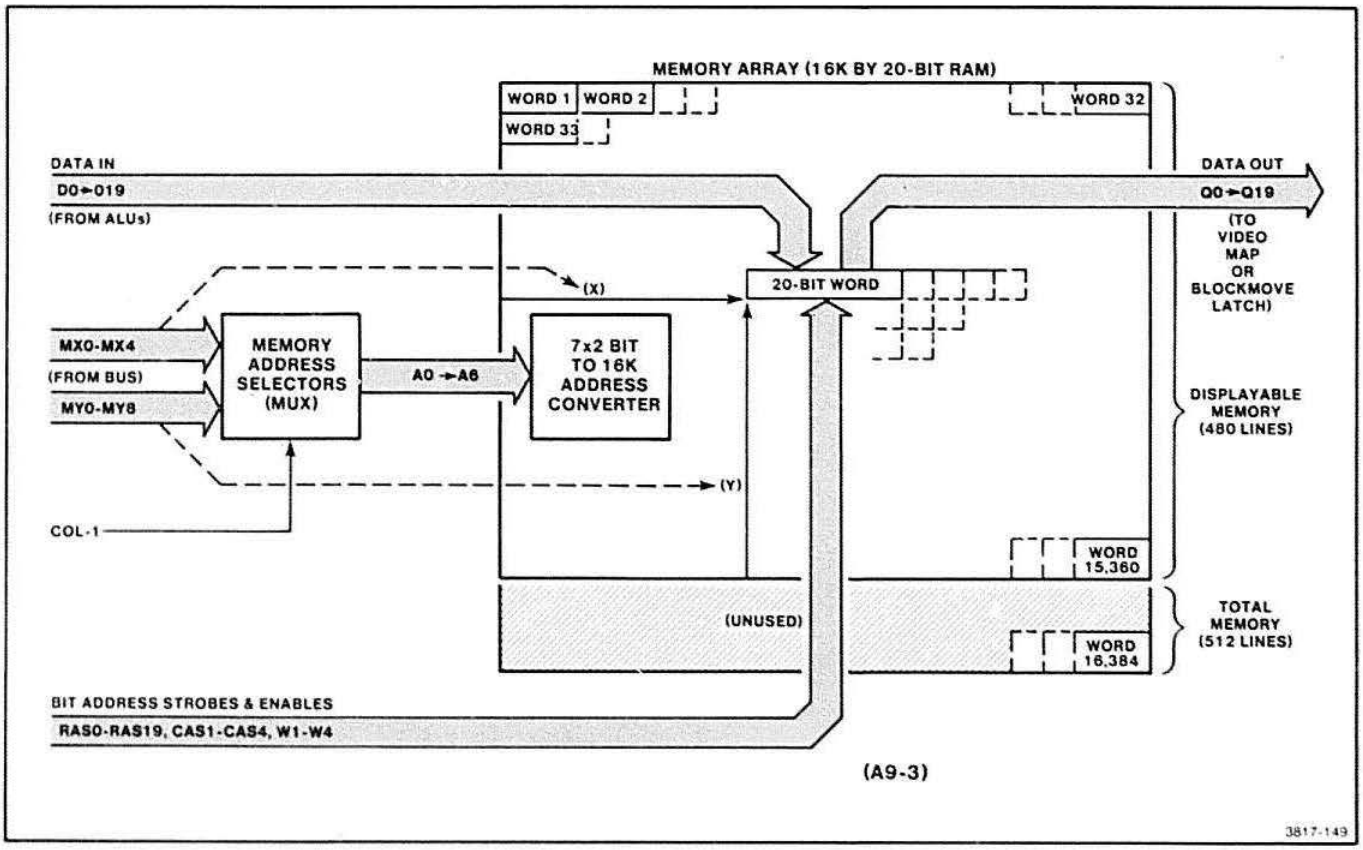


Figure 6-31. Memory Array Diagram.

The Processor Read Latches are arranged so that three eight-bit latches store: 20 bits of pixel data and, four bits of Self Test information. The processor reads these 24 bits over a 16 line bus; so 16 of the 24 output bits are read over one set of eight lines, and the remaining eight bits are read over the other eight lines. The high-versus-low selector lines: PREADH and PREADL, switch between two latch outputs, thus acting as a 16-to-8 line MUX. Since the processor sends the command for PREADH or PREADL, it knows which part of the word is coming over the bus at any given time.

The extra four (Self Test) data bits are:

- Write enable latch status (WENB-1)
- Video output (DY-1)
- Border latch status (QC-1)
- Ground.

These four bits are presented to the processor along with the four highest bits of pixel data.

I/O Decode

The group of addresses that control I/O (communications between the Raster Memories and the processor) are decoded by this circuit block. It decodes two write and two read signals plus the map write signal. The two read signals are for the processor readable pixel latches, and the two write signals are for the ALU/Write-enable Latch and the Border Latch. The processor, using the map write signal, writes values into the Video Map.

Video Shift Register

The Video Shift Register converts 20-bits of parallel data, from the Memory Array, into a serial data stream. This serial data is passed to the Video Map on its way to the Display. The pixel data (Q0 through Q19) enters three shift registers, which function as a parallel-to-serial converter. The ECL level LOAD-1 signal is converted to TTL and applied to the shift registers at the start of each refresh cycle. Refer to block diagram, Figure 6-32. DCLK-1 clocks:

- Three shift registers, and
- Clock Sync flip-flop (via its AND gate).

After the shift register's serial output is converted back to ECL, it enters the Clock Sync flip-flop. Since this flip-flop is clocked by the DCLK-1, it synchronizes the serial data with the main dot clock. MAP-0 clears the sync flip-flop when other circuits are writing to the Video Map. This tri-states the flip-flop so it does not affect the map write circuitry. The serial data enters this Video Map as VID2-0.

Another flip-flop, called Border Latch, generates a blank video signal at the beginning and end of each line. This places a blank border along each vertical edge of the screen; thus characters at the edges are easily readable, even if the display is inverted black on white. This latch generates border video between the first blanking pulse and the start of actual video from the Vector Generator. Then (at the end of the line) it again generates border video, following the actual video and before the end-of-line blanking pulse. See Figure 6-33.

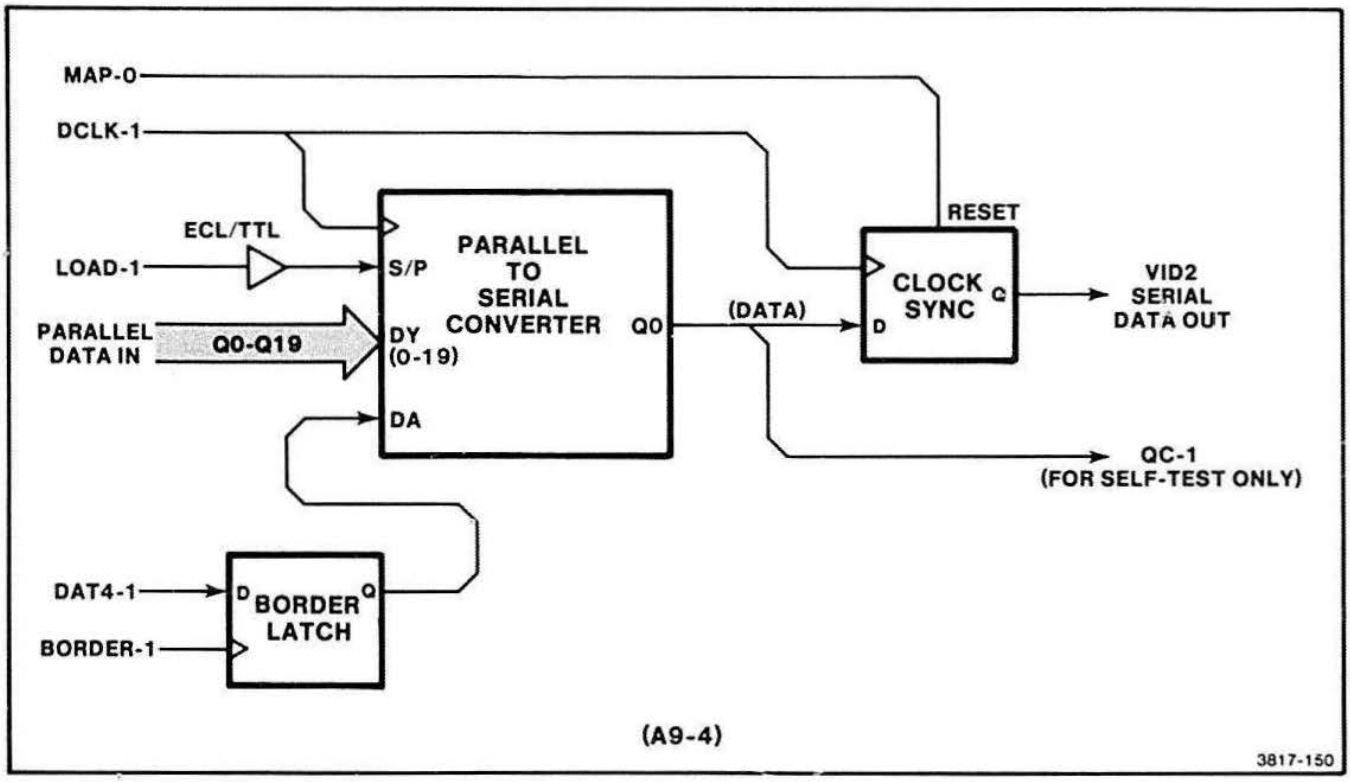


Figure 6-32. Video Shift Register.

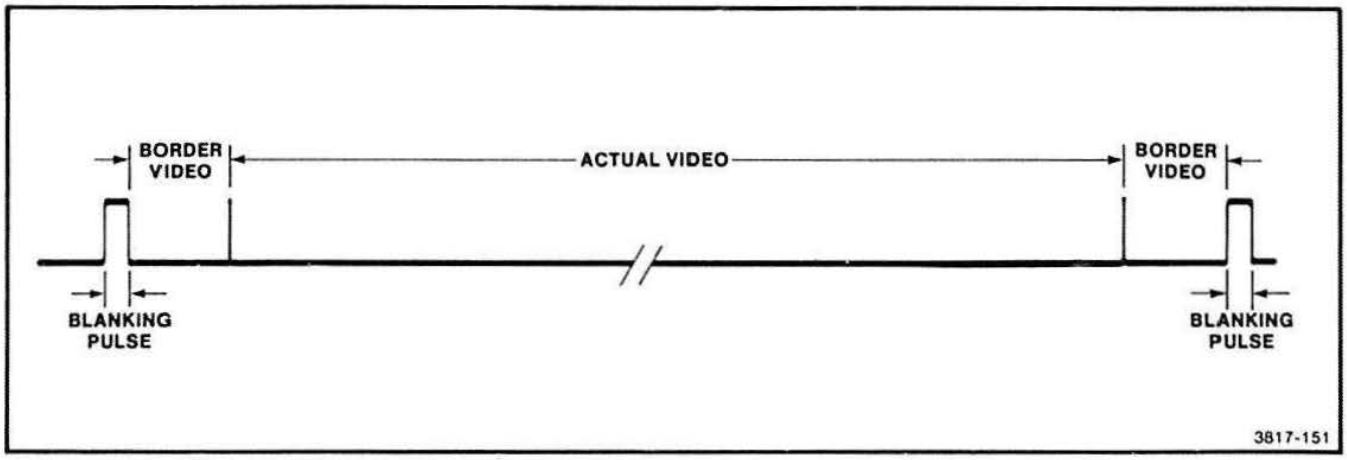


Figure 6-33. One Scan Line Showing Border Video.

Video Map

The Video Map is a pixel brightness index interpreter. The map is a RAM chip that contains 16 four-bit words. Each of these 16 words corresponds to one of the combinations of the three memory planes plus the cursor. Figures 6-34 through 6-36, on foldouts at the end of this section, are functional block diagrams of the Video Map and its related circuitry. Figure 6-34 shows how the map works during a typical pixel write from the standard Memory Plane 2. Here pixel data, VID2, enters the address port of the map. Since planes 0 and 1 and the cursor are inactive, the only addresses that are of interest are 0000 and 0100. These addresses contain four bits of pixel data which might typically be 1111 (white) and 0000 (black). Since the data at these addresses may be modified by the processor, the brightness values could have been 0010 (dark gray for pixel OFF) and 1100 (light gray for pixel ON), or any other set of values.

Next, Figure 6-35 shows two additional memory planes (Option 20) installed, and the cursor active. Study Figures 6-37 and 6-38 along with Figure 6-35 to see how the various combinations of pixels from the three memory planes can combine to create shaded images or multiple (layered) images on the display screen. The *4112 Host Programmer's Manual* has a good explanation of how the shades of gray are obtained. This knowledge is not necessary for servicing the terminal, but may help to understand how certain display screen effects are obtained.

The Map's Q0 to Q3 outputs carry the interpreted pixel data to a latch where the data is synchronized with the clock, DCLK-1. From here the pixel data enters the Display Bus as DAC0-1 through DAC3-1. These lines enter the DACs on the Video Controller board, where they are converted to an analog signal to drive the gun in the display CRT.

As already stated, the brightness index is arbitrary and can be altered by the processor. When the processor receives a command to reprogram the Bit Map, it sends an address (such as F00A) along with the four bits of data for that location. The I/O Decoder translates the address F00A into the four-bit address: 0101. This address passes through a buffer and an AND enable on its way to the map. Notice that the I/O address and the pixel data both share the map's address lines. One or the other of these addresses is selected by logic connections acting like a switch. With the address selected, the processor sends a write enable (WE) and then sends the new intensity value over the map's data inputs. RAM write is enabled only when the following signals are all true low:

- IOWC-0
- AIOWC-0 (this line toggles the "switch")
- VGADR-0
- ADR10-0

Figure 6-36 shows signal flow in the Bit Map circuits during reprogramming.

Power Components

Power into the Raster Memory board is 12 V, 5 V, and −2 V. The 12 V and 5 V come from the power supply. The −2 V for the ECL comes from the Video Controller board.

The power for the RAMs employs a greater degree of filtering. All the grounding is NOT at ground potential. See Note 1 and the IC Supplies chart on the schematic A9-5 for more complete information.

DUAL RASTER MEMORY BOARD

The Dual Raster Memory board adds two additional memory planes to the 4112 display memory. This board is identical to the Raster Memory board, with the following exceptions:

- There is no Video Map.
- There are two memory planes located on this board (Planes 0 and 1). Plane 2 is the only memory plane on the standard Raster Memory board.
- The I/O decoding is set for a different address: F7E0 – F7F7.

This dual plane memory board is called Option 20.

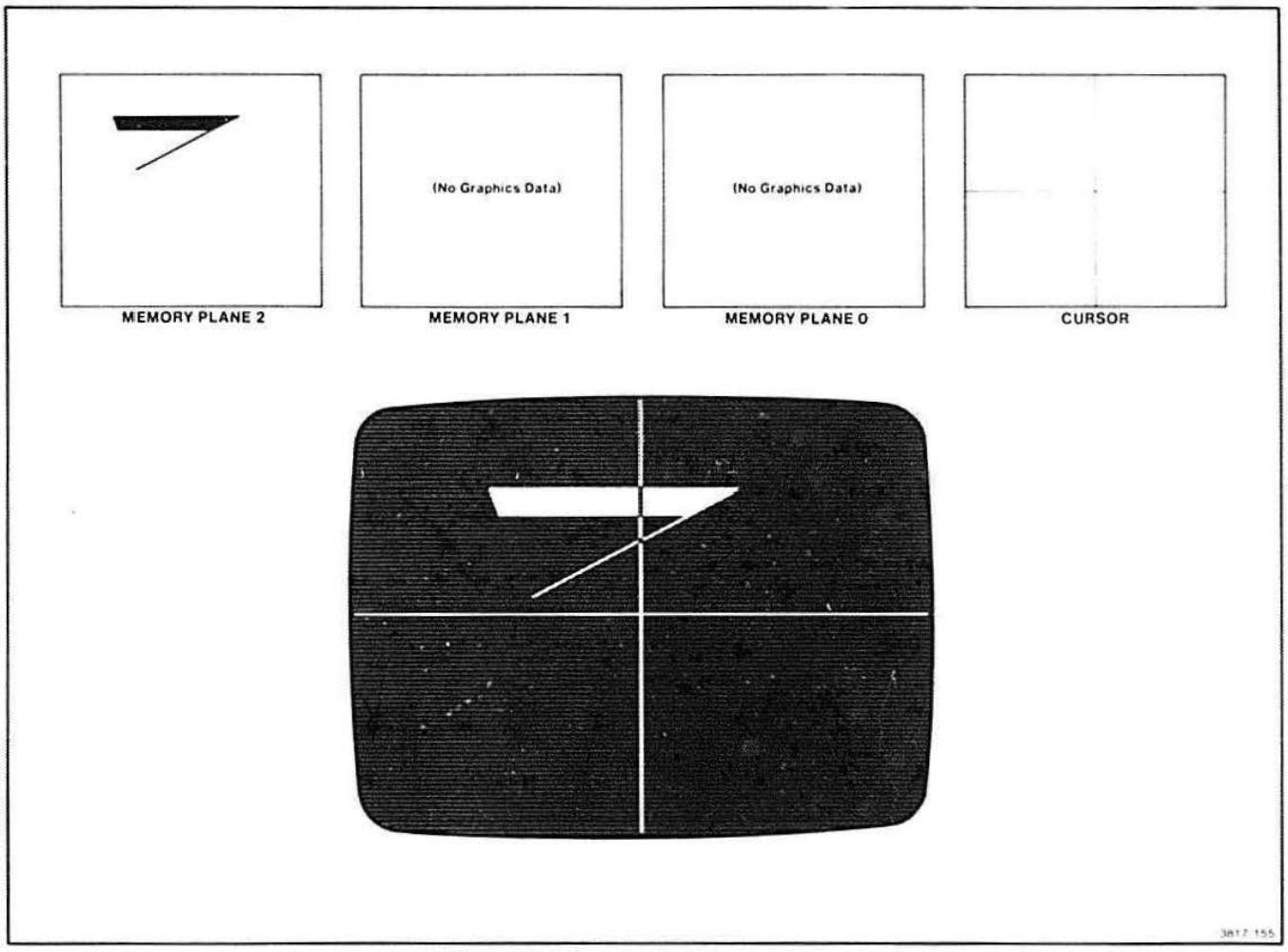


Figure 6-37. Video Map (One Plane and Cursor) and Display.

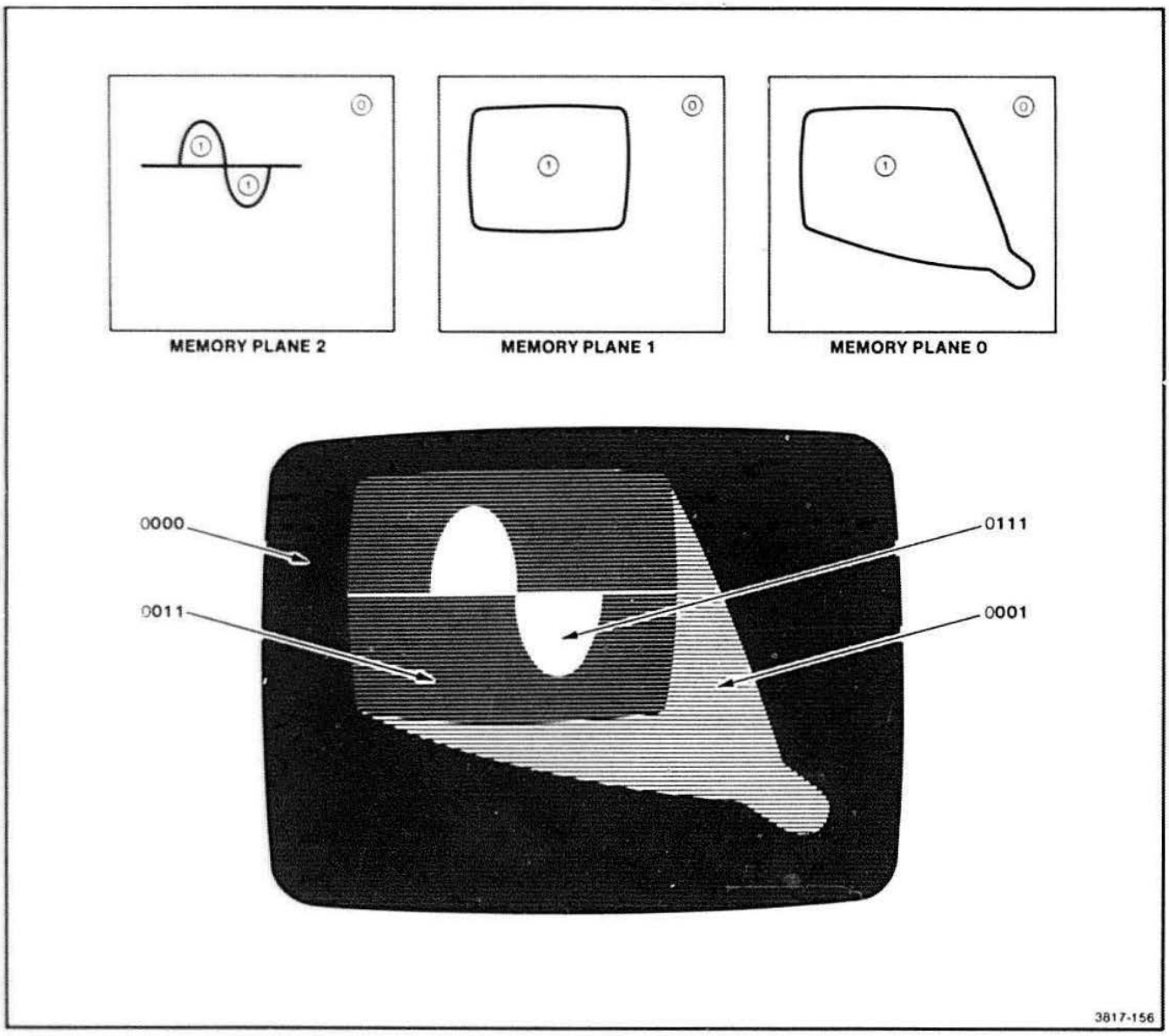


Figure 6-38. Video Map (3 Planes — Shading) and Display.

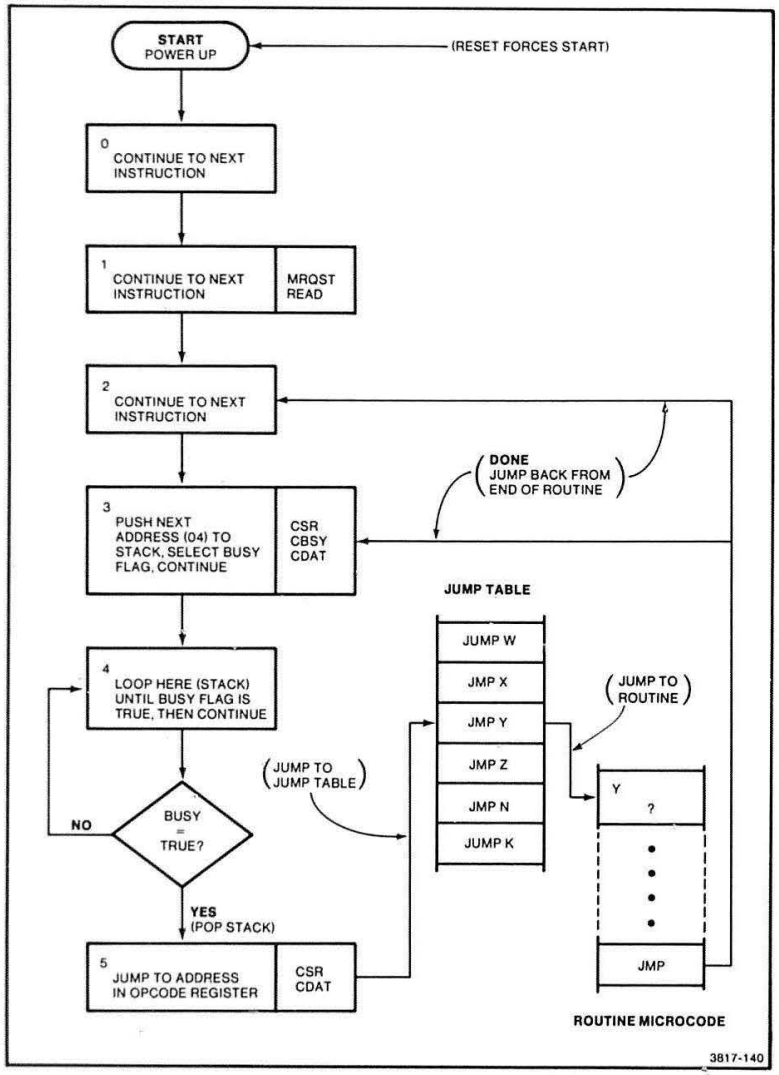


Figure 6-21. Power-Up Routines.

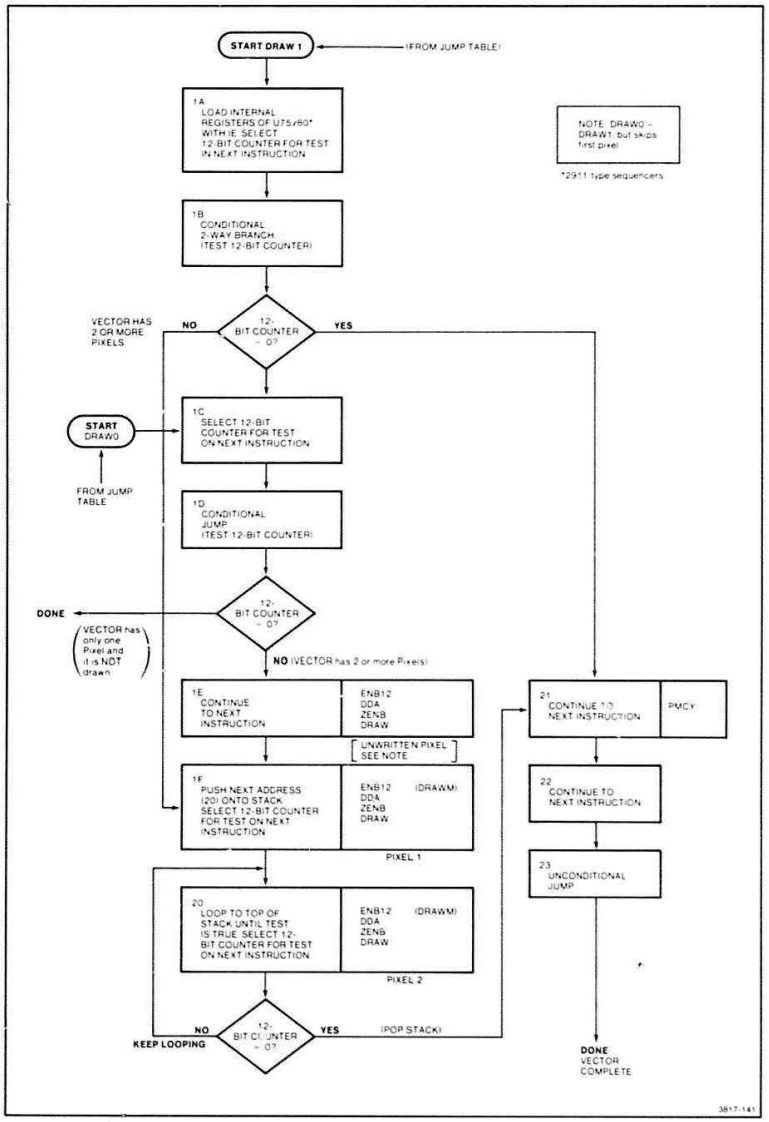


Figure 6-22. DRAW0 and DRAW1 Routines.

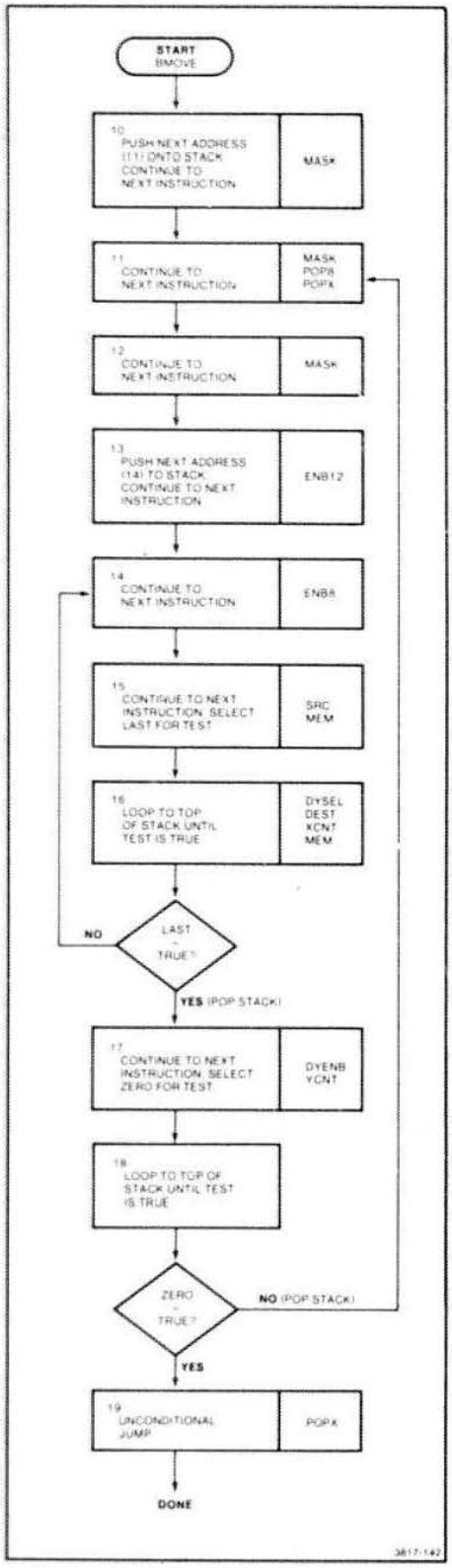


Figure 6-23. Blockmove Routine.

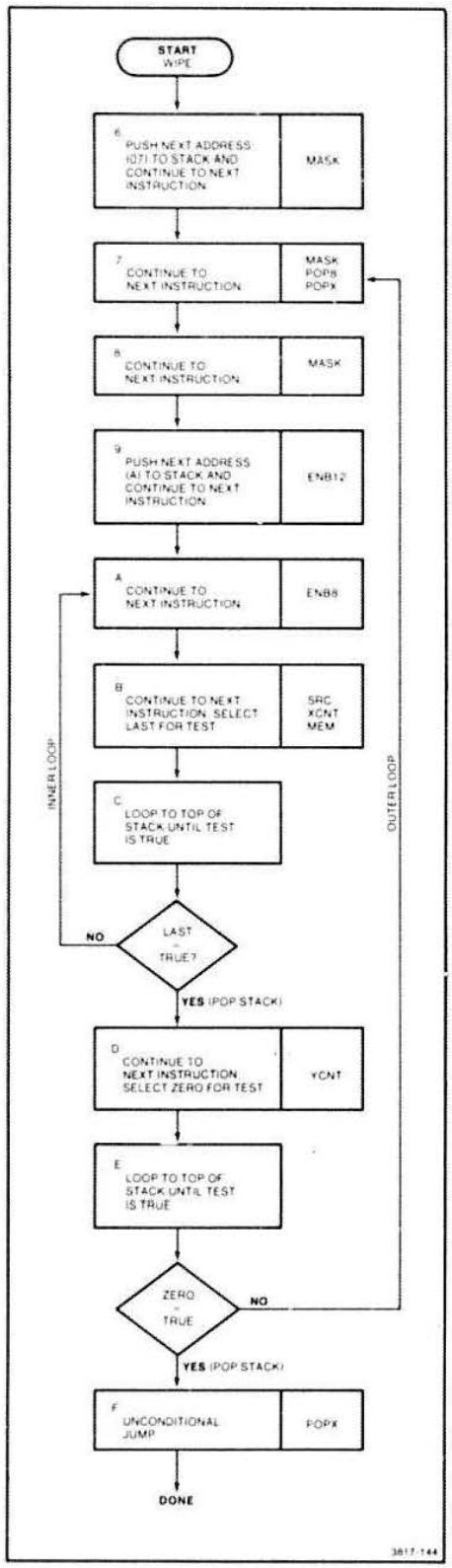


Figure 6-24. Wipe (Erase) Routine.

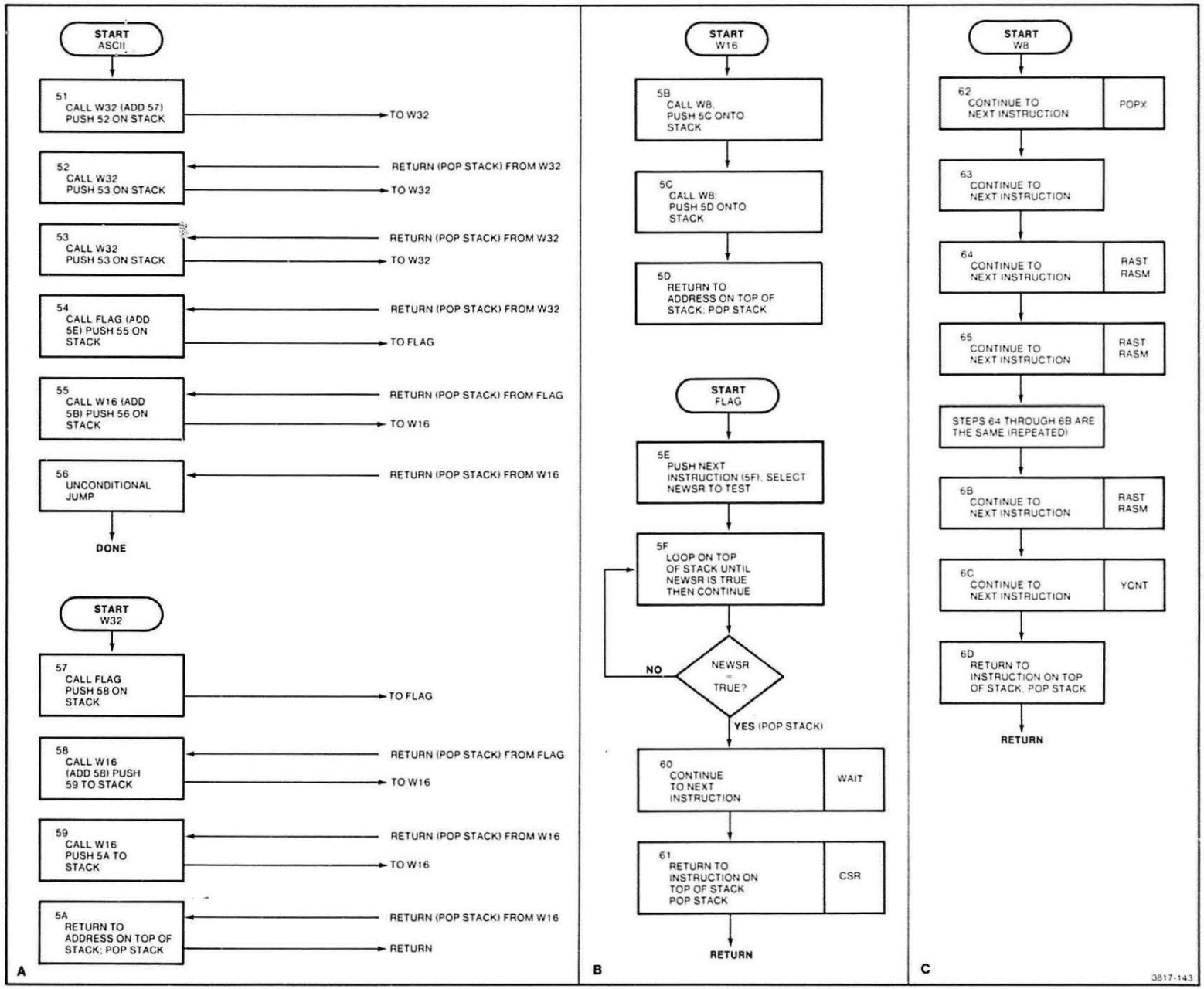


Figure 6-25. ASCII Dot Matrix Routine.

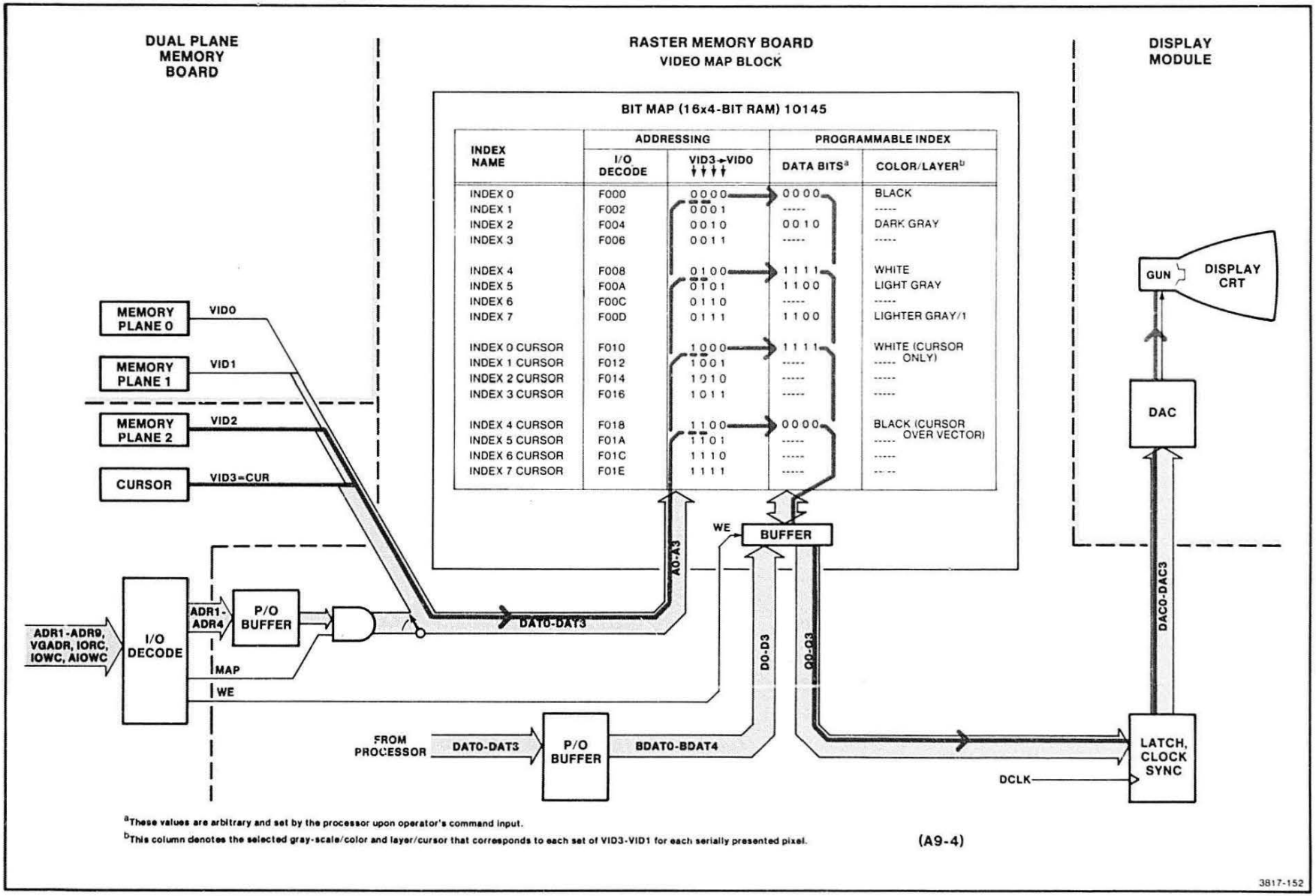


Figure 6-34. Video Map (Single Plane and Cursor).

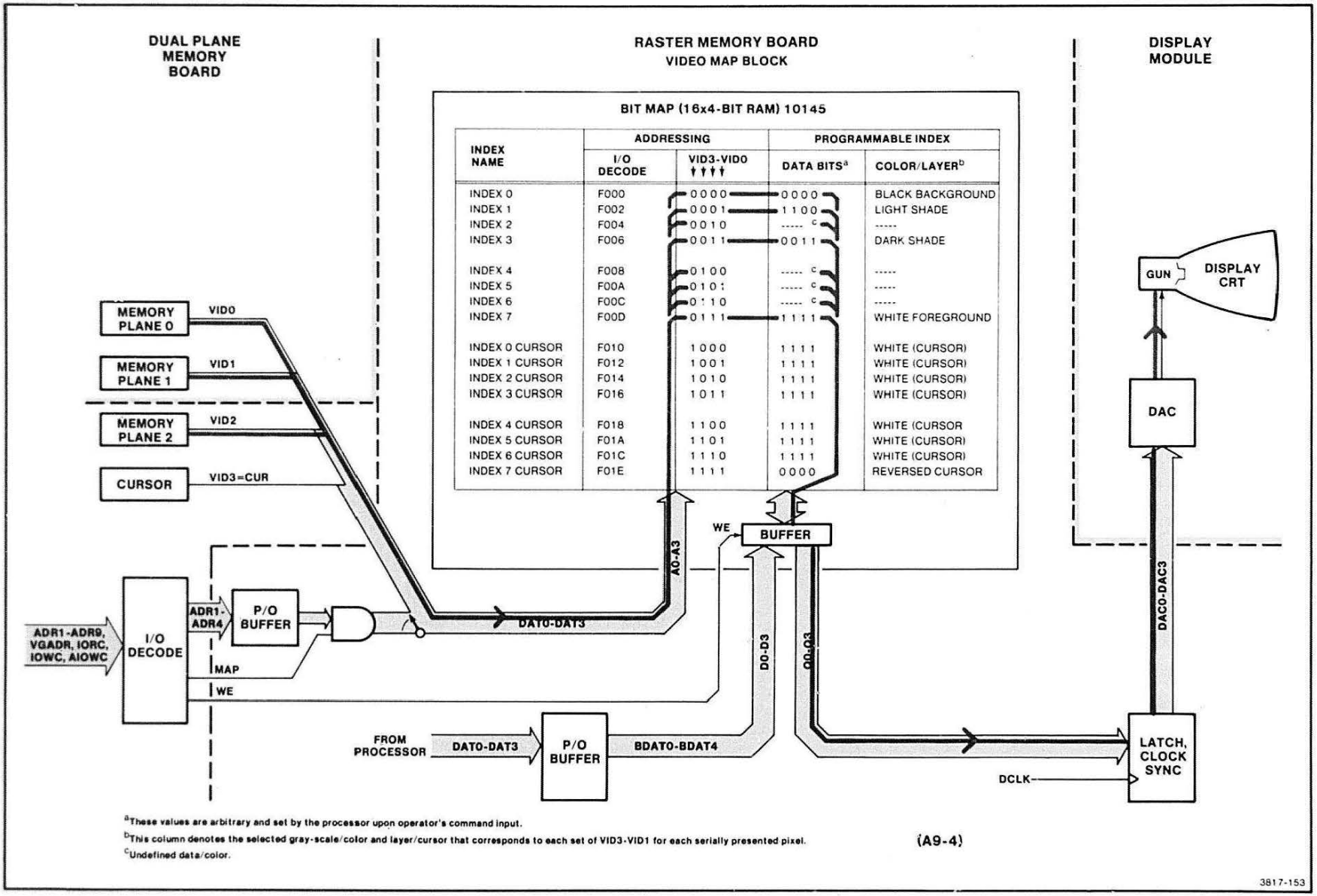
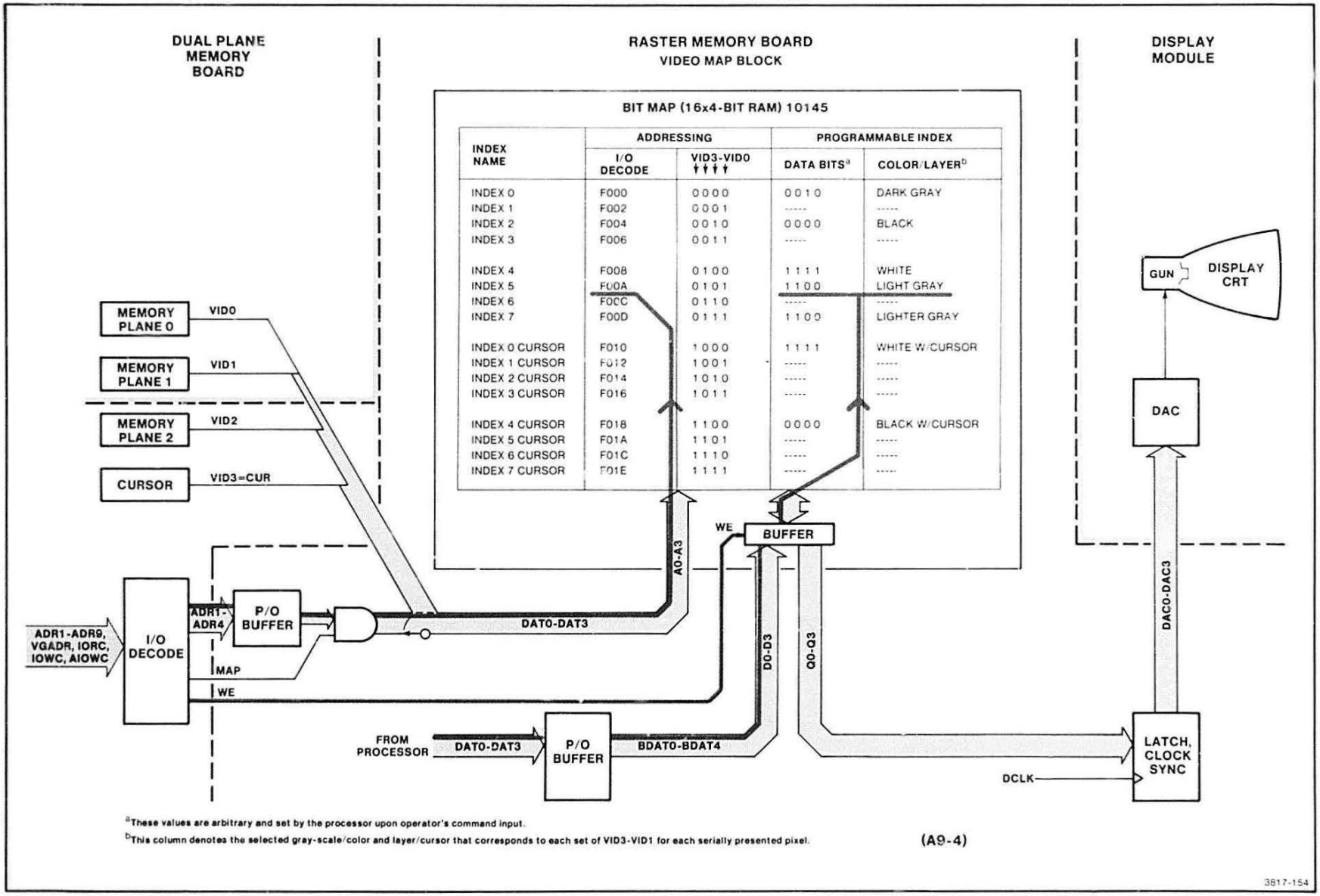


Figure 6-35. Video Map (Three-Plane Interpreter).



INDEX NAME	ADDRESSING I/O DECODE	ADDRESSING VID3-VID0	PROGRAMMABLE INDEX DATA BITS[a]	PROGRAMMABLE INDEX COLOR/LAYER[b]
INDEX 0	F000	0000	0010	DARK GRAY
INDEX 1	F002	0001	-----	-----
INDEX 2	F004	0010	0000	BLACK
INDEX 3	F006	0011	-----	-----
INDEX 4	F008	0100	1111	WHITE
INDEX 5	F00A	0101	1100	LIGHT GRAY
INDEX 6	F00C	0110	-----	-----
INDEX 7	F00D	0111	1100	LIGHTER GRAY
INDEX 0 CURSOR	F010	1000	1111	WHITE W/CURSOR
INDEX 1 CURSOR	F012	1001	-----	-----
INDEX 2 CURSOR	F014	1010	-----	-----
INDEX 3 CURSOR	F016	1011	-----	-----
INDEX 4 CURSOR	F018	1100	0000	BLACK W/CURSOR
INDEX 5 CURSOR	F01A	1101	-----	-----
INDEX 6 CURSOR	F01C	1110	-----	-----
INDEX 7 CURSOR	F01E	1111	-----	-----

[a]These values are arbitrary and set by the processor upon operator's command input.

[b]This column denotes the selected gray-scale/color and layer/cursor that corresponds to each set of VID3-VID1 for each serially presented pixel.

Figure 6-36. Video Map Reprogrammed by Processor.

Section 7

DISPLAY MODULE THEORY OF OPERATION

INTRODUCTION

The Display Module is a 15-inch raster scan noninterlaced video monitor. This theory section begins with a brief review of raster scan theory and continues with an explanation of each of the circuit blocks in the Display Module.

Figure 7-1 is a simplified block diagram of the Display Module, showing its three basic functional blocks. Each block requires an input signal to generate one of the three signals that causes the CRT to produce a picture.

The input signals are:

- VIDEO — This signal turns the CRT electron "beam" on or off and controls the gray scale. (Pixel data from Video DACs).
- HORIZ SYNC — This signal synchronizes the circuitry that deflects the beam left and right across the face of the CRT.
- VERT SYNC — This signal synchronizes the circuitry that deflects the beam up and down.

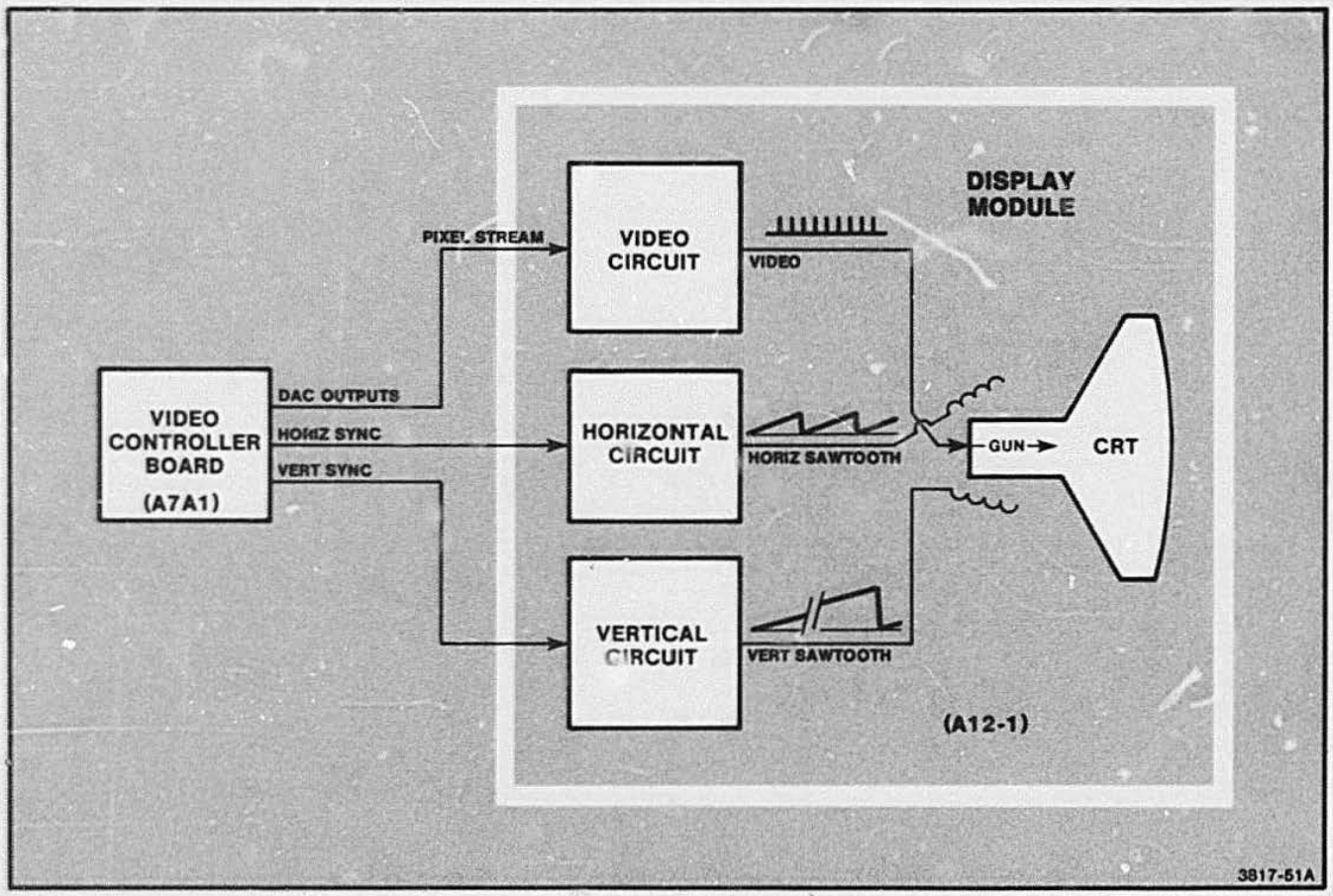


Figure 7-1. Display Module Simplified Block Diagram.

The Video Controller board supplies these signals to provide a complete picture on the CRT screen. See Video Controller theory in Section 6. The display picture consists of horizontal lines caused by the combined action of the video, horizontal, and vertical signals. Figure 7-2 shows the effects on the display image of each of the three circuit blocks shown in Figure 7-1. Figure 7-2A shows video only (no deflection) and the resulting dot of light in the center of the screen.[1] Part B of this illustration shows a single line of video created by adding only horizontal deflection to the video pixel stream. The horizontal sawtooth wave shows the voltage on the deflection coils as a function of time during trace and retrace. Likewise, Part C shows the complete picture created by adding vertical deflection. Notice that there are 525 horizontal sweep cycles for each vertical sweep sawtooth wave. During both horizontal and vertical retrace times, the writing beam is turned off. (Notice that the video signals for all lines are identical in this illustration; this is a simplified special case.)

[1] The video signal varies between +1 V (high = on) and +.075 V (low = off); voltages between these levels produce the corresponding levels of intensity.

DISPLAY MODULE TIMING

Figure 7-3 is a Display Module system timing diagram. This diagram shows sync and timing pulses and the relationship between the horizontal and vertical lines. Study these timing relationships before reading the detailed circuit theory. Refer back to this diagram while studying the block descriptions.

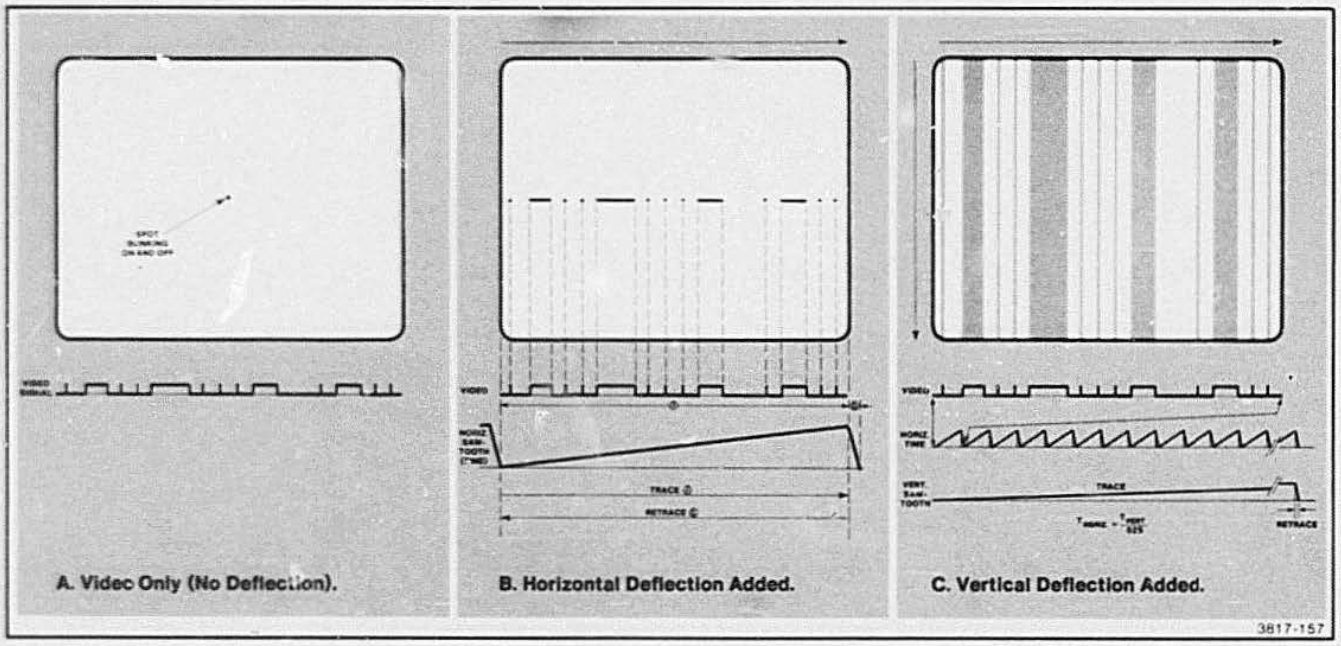


Figure 7-2. Display Image Composition.

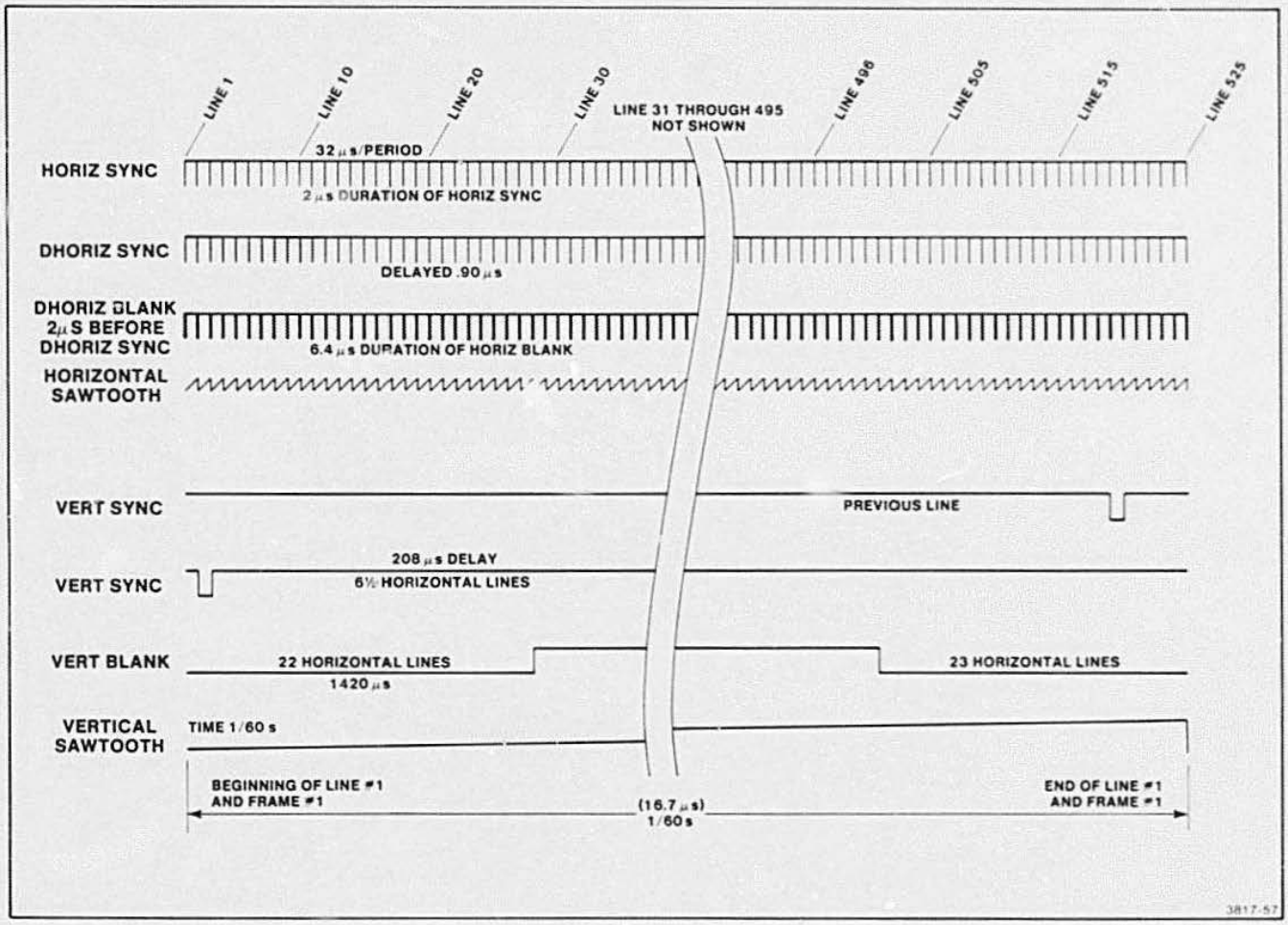


Figure 7-3. Sync and Blanking Timing Diagram.

VIDEO CIRCUITRY

The Video circuitry amplifies the VIDEO signal to a level that will drive the CRT. Figure 7-4 shows the circuit blocks associated with video signal amplification.

Multiplier Block

This block of circuitry amplifies/multiplies the video signal while allowing brightness and contrast adjustments. The MC1496 chip (typically used for modulator/demodulator applications) functions here as a "cascoded differential" amplifier. Figure 7-5 shows the internal parts of this IC, while external circuitry is represented in block form. The lower pair of transistors establish a DC level for the output signal; their bias voltages are controlled by the Brightness Control (labeled DC LEVEL on the schematic). The next pair of transistors accept the Video Input signal; one side of the differential pair accepts the high part of the AC component, while the other side accepts the low part.

The four output transistors have cross-coupled collectors. The voltage on the bases of each pair of transistors determines the gain of the system. As base voltages change, one set of transistors conducts more or less than the other, thereby subtracting more or less of the signal current. The DC output level remains fixed, while the AC output varies depending on the contrast setting. This section "multiplies" by one or a fraction depending on the contrast control.

A test signal may be inserted on pin 1 of connector P586. This test signal enters a zener-transistor stage. The resulting output is placed on the + SIGNAL input of the MC1496. This constant signal results in a completely white (fully written) screen for test purposes.

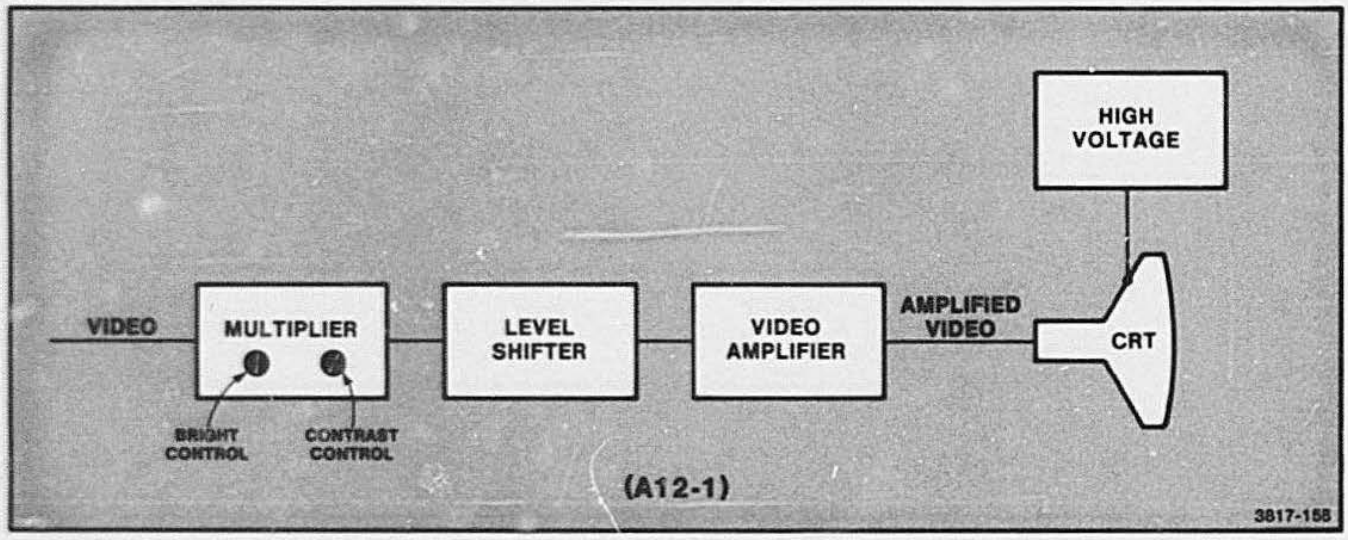


Figure 7-4. Video Circuit Block Diagram.

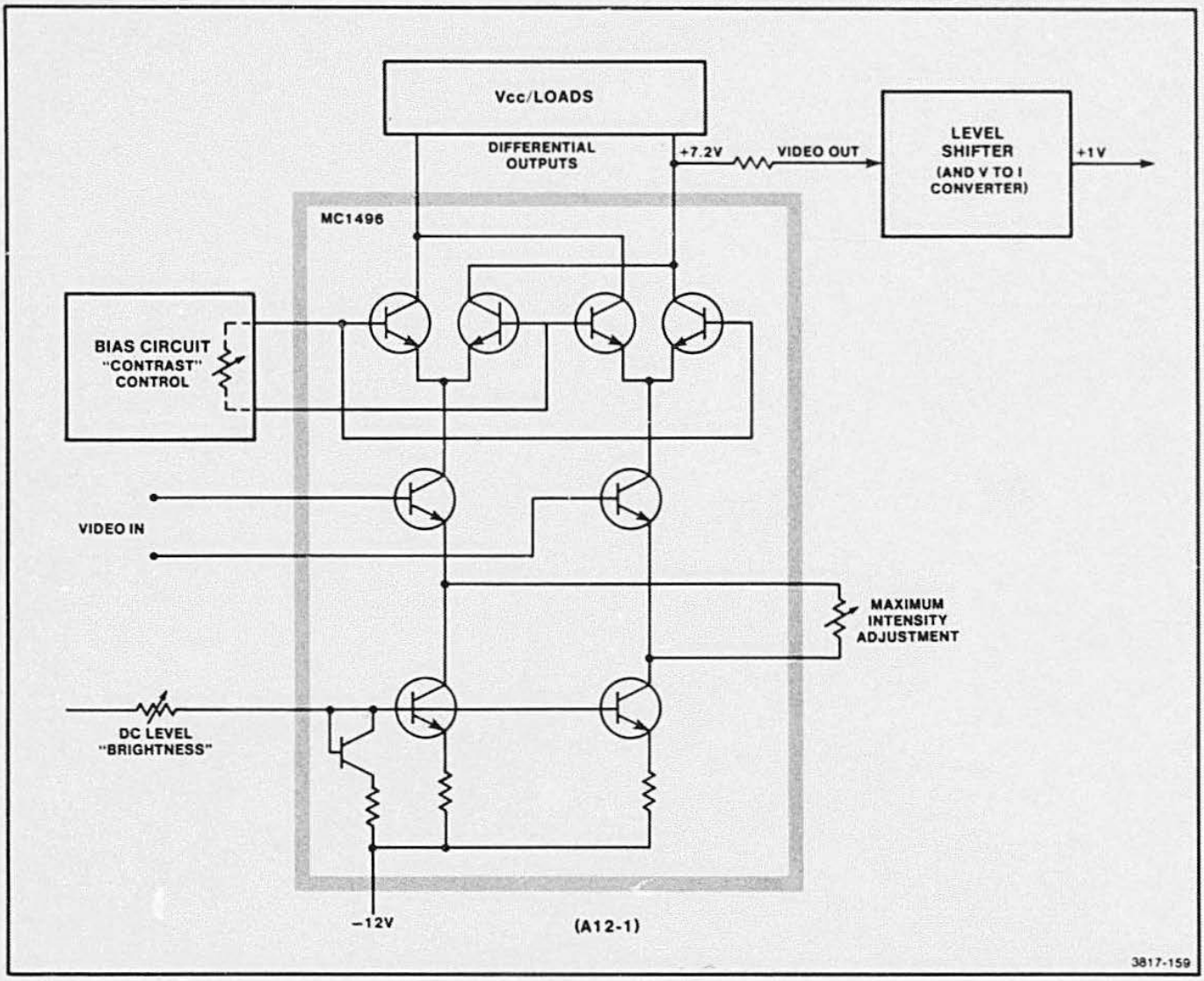


Figure 7-5. Multiplier Circuit Block Diagram.

Level Shifter

The Level Shifter consists of discrete components that perform three basic functions:

1. Voltage-to-current convertor; performed by a series resistor.

2. Voltage level shifter; a transistor with a gain of 1, converts the DC level from 7 V to 1 V.

3. Regulation against changes in ambient temperature; a 100kΩ thermistor regulates the operation of the transistor.

Figure 7-6 shows this circuitry. The VIDEO signal is sent to the Video Amplifier block.

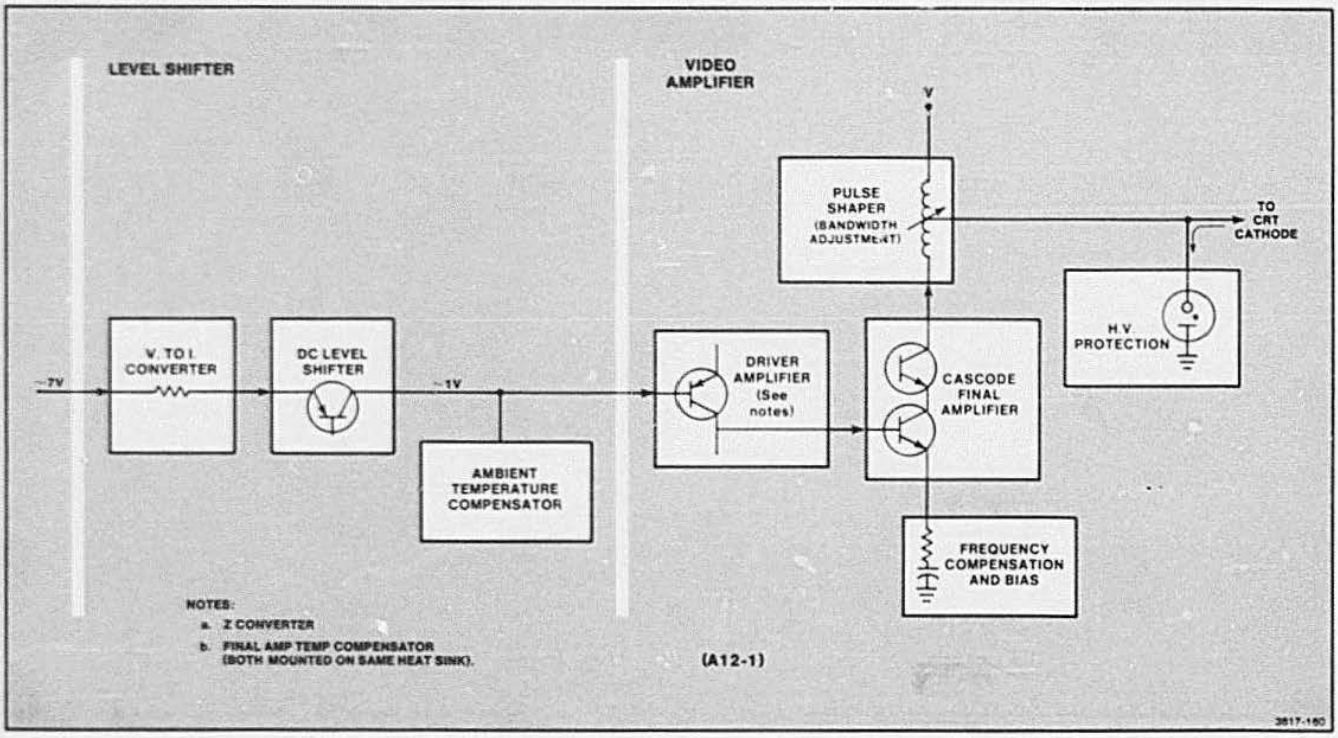


Figure 7-6. Level Shifter and Video Amplifier.

Video Amplifier

The Video Amplifier circuit block amplifies the VIDEO signal to a level sufficient to drive the cathode of the CRT. The VIDEO signal first enters a driver stage that consists of an emitter follower PNP transistor. The signal then is at the level required to drive the final output stage: a pair of cascoded NPN transistors. The driver stage acts as an impedance matching device. This transistor is mounted on the same heat sink as the final stage transistors; this allows the PNP to compensate for temperature-current effects in the NPN transistors.

The signal current through the Cascode Amplifier passes through a variable center-tapped inductor coil. This variable coil produces current spikes that add to the rounded off VIDEO signal; this restores the square shape of signal pulses. See Figure 7-7. The three RC networks on the emitter of Q341 provide bias and frequency compensation to preserve the square pulses. The VIDEO signal is taken from the center-tap of this coil. This output signal exits the Deflection Board on pin 1 of connector P588. This signal, when applied to the cathode of the CRT, turns the writing beam on and off and it also controls the overall brightness level of the information written on the screen.

An ionization tube, near the video output point, protects the Video Amplifier from induced high voltages (due to arcing) coming back from the CRT. Such statically induced voltages pass to ground through this high-voltage and high-current tube, instead of damaging the Deflection Board components.

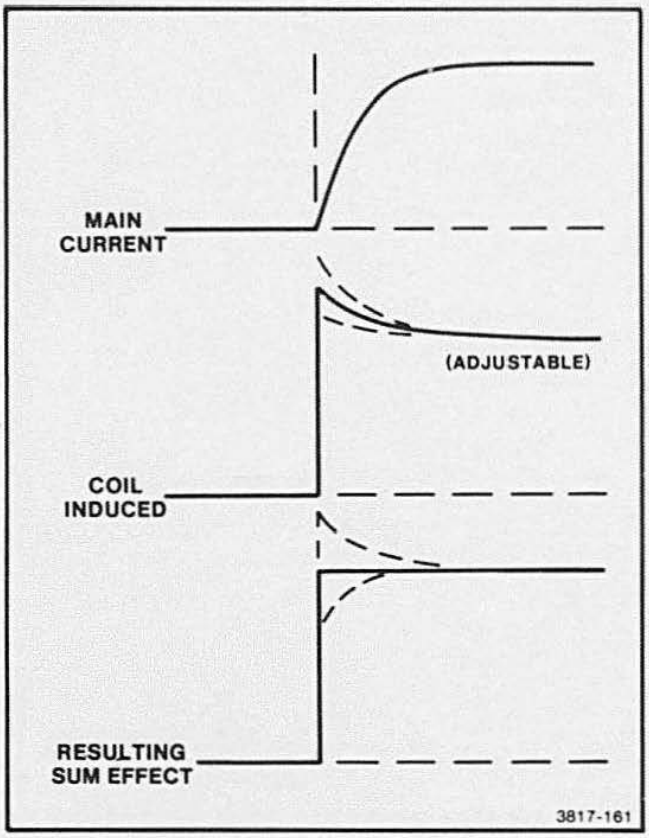


Figure 7-7. Wave Shaping by Inductor Coil.

HORIZONTAL CIRCUITRY

Block diagram, Figure 7-8, shows the four stages in the Horizontal Deflection circuitry. These circuit blocks produce the horizontal deflection of the writing beam in the CRT. This movement, combined with the vertical movement (discussed later in this section), produces the raster lines on the CRT.

Horizontal Delay

The Horizontal Delay circuit delays the HORIZ SYNC pulse from the Video Controller enough to make the retrace happen in the middle of the blanking period. This prevents the loss of data caused by writing during the blanking period.

This circuitry consists of two one-shots. The first one-shot delays the SYNC pulse by about 700 ns. The second one reshapes the SYNC pulse to eliminate any distortion that may have been introduced by the first one-shot. The DHSYNC (Delayed Horizontal Sync) is applied to the Phase-Locked Loop.

Phase-Locked Loop

The Phase-Locked Loop circuit keeps the output FLYBACK SIGNAL in step (synchronized) with the DHSYNC signal. These signals are compared and the synchronized output signal is applied to the Horizontal Driver.

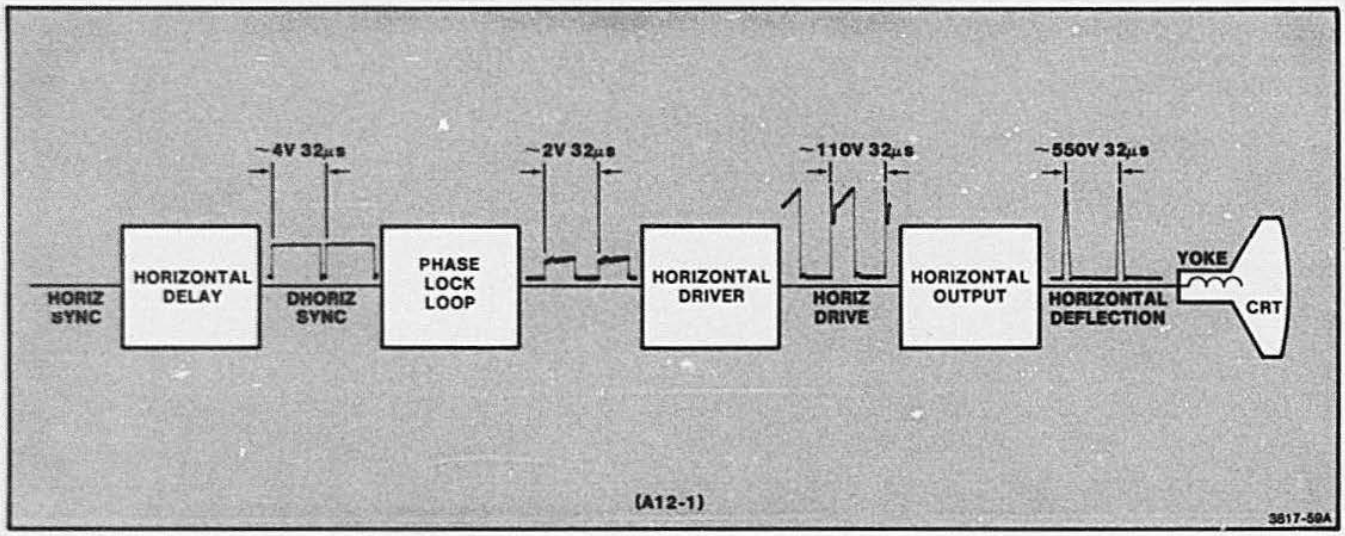


Figure 7-8. Horizontal Circuitry Block Diagram.

Figure 7-9 is a functional block diagram of this circuit block showing the internal blocks in the MC1391 chip. The DHSYNC signal path is shown in bold; the FLYBACK return signal path is in dotted bold. The PLL chip compares and synchronizes these two signals. Notice that the horizontal frequency adjustment is provided by the "H OSC" pot in the timing block. This timing block is located outside the chip, and between the Phase Detector and the VCO (Voltage Controlled Oscillator) inside the chip. The chip input labeled MSR Control, on the schematic, is actually a Duty Cycle Adjustment. MSR stands for: Mark Space Ratio.

Horizontal Driver

The driver circuit amplifies the horizontal signal from the PLL, thus providing the power necessary to drive the Horizontal Output Circuit. The combination of the power transistor and transformer provides 0.6 A for the base of the Final Amplifier transistor.

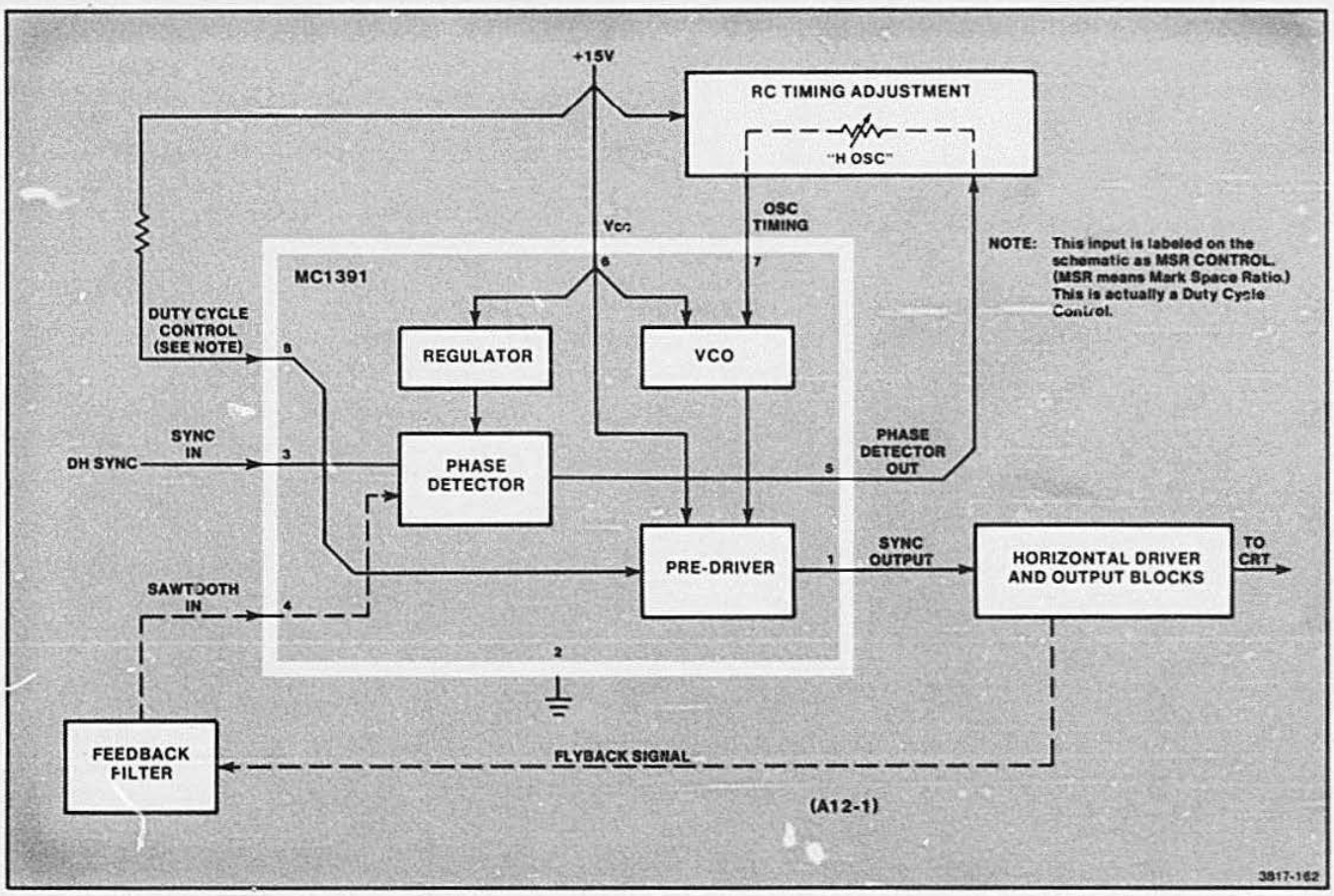


Figure 7-9. Phase-Locked Loop Circuit Diagram.

Horizontal Output

The Horizontal Output circuit produces two horizontal deflection signals:

1. Sawtooth left-to-right deflection voltage, and
2. Flyback pulse which is sent to the H.V. Board and makes the rapid retrace (right-to-left) deflection voltage.

The sawtooth current passes through the Horizontal Yoke coil around the CRT. This yoke current is bidirectional with the negative part of the sawtooth producing current in the opposite direction to the positive wave voltage. Figure 7-11A shows this sawtooth waveform.

The circuitry that makes this current is shown in Figure 7-10. The sync pulse enters the Horizontal Output block via the transformer in the Horizontal Driver. The pulse is placed on the base of the Final Transistor, Q1002. This produces a current through the transistor and the yoke which charges up the "S" capacitor. A reverse current results as this capacitor discharges. This current flows back through the yoke and a diode to ground; this completes the sawtooth wave cycle. The resulting wave would be quite linear except that the "S" capacitor acts like a current integrator (which rounds the linear parts of the wave). This is a desired effect, and the resulting "S" adjusted wave matches the deflection current to the curvature of the CRT. The amount of "S" compensation can be changed by adjusting the variable coil called, "HORIZ LINEARITY."

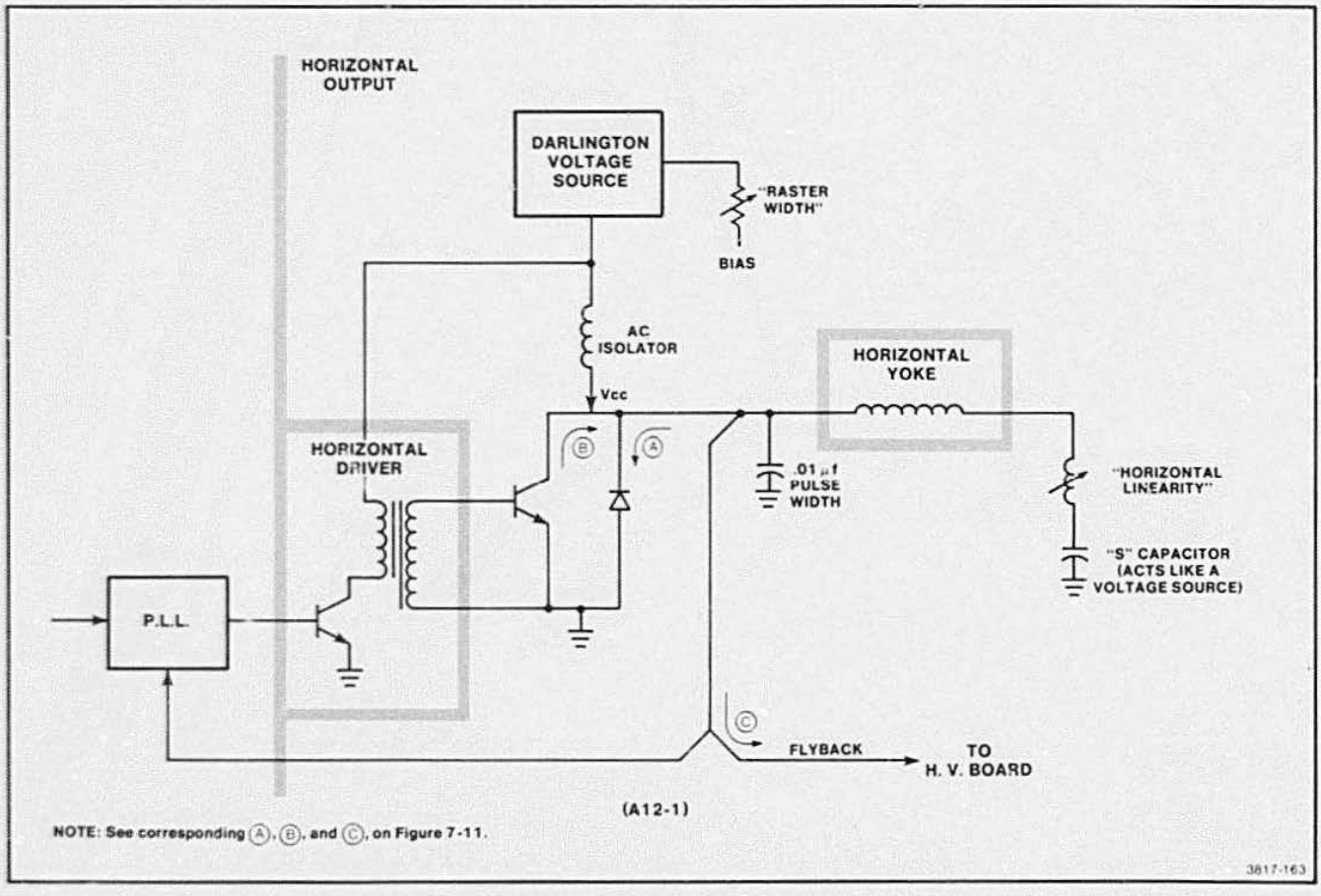


Figure 7-10. Horizontal Driver and Output Circuit.

The second output signal, FLYBACK, is a high voltage pulse produced by the rapid change in current through the yoke, during the time between the end of one sawtooth wave and the beginning of the next. This time, indicated by C in diagram Figure 7-11B is controlled by the combined effects of the inductance of the CRT yoke and the capacitor C611. The resonant frequency of the two creates a pulse width of ~4.2 μs. The amplitude of this FLYBACK pulse is about 550 V. This signal goes to the High Voltage board, and part of it is sampled by the Phase-Locked Loop circuit.

The Darlington transistors (Q1001 and Q721) supply power to the circuitry. Part of the Darlington voltage also supplies the Horizontal Driver Transistor. The voltage to the final driver transistor and yoke current path passes through an "AC Isolator" coil. This keeps FLYBACK high voltage and AC components from affecting the operation of the voltage-current supply. The voltage level is set by adjusting the Raster "Width" control. This adjustment sets the Darlington bias level, which affects the amplitude of the Sawtooth and Flyback wave outputs. The adjustment is labeled, WIDTH, because it directly adjusts the width of the raster lines on the face of the CRT.

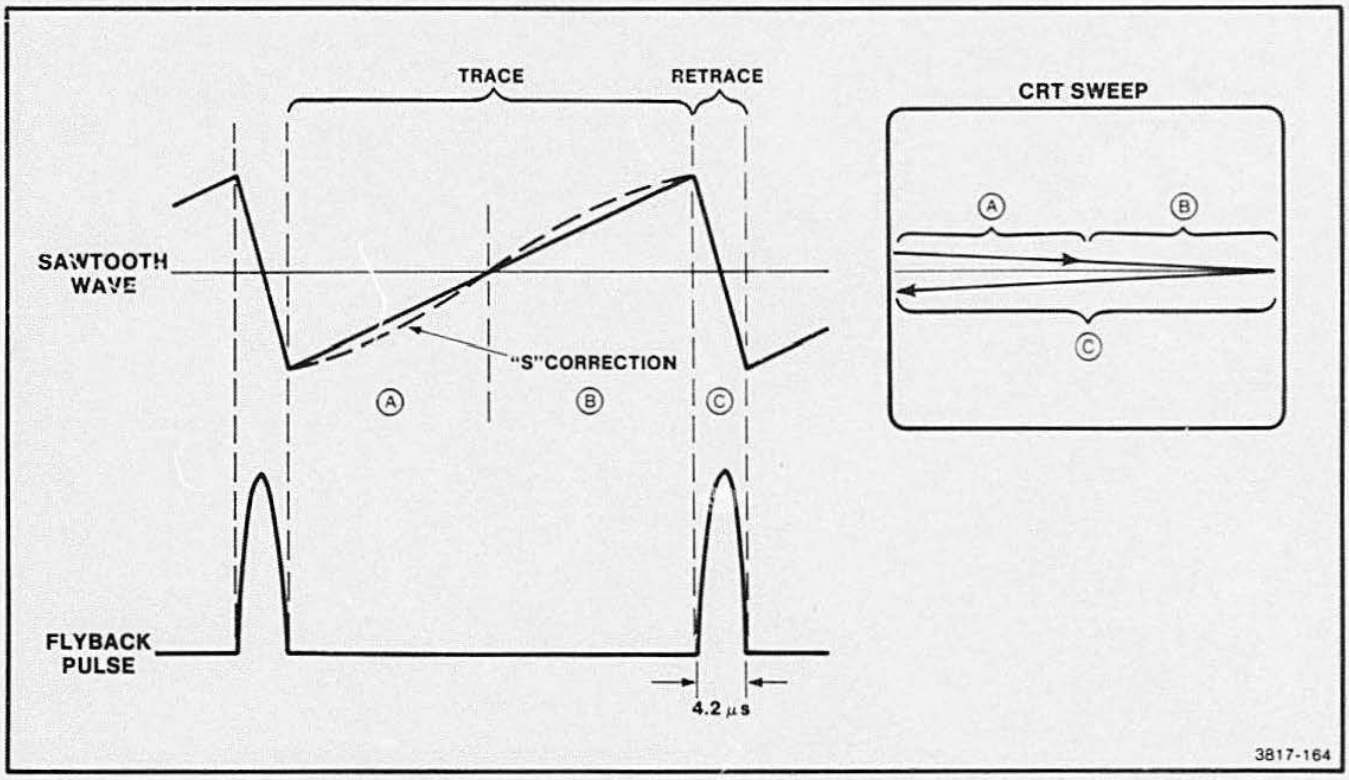


Figure 7-11. CRT Sweep Waveforms.

VERTICAL DEFLECTION CIRCUITRY

The Vertical Deflection circuitry moves the writing beam from the top to the bottom of the CRT (and back) using the circuit blocks shown in Figure 7-12. One Vertical Deflection signal occurs for each 525 Horizontal Deflection pulses. Only 480 of these lines are visible because of display memory size; the 45 bottom lines are blanked out accordingly.

Synchronization Delay Circuit

The VERT SYNC, from the Video Controller, synchronizes the Vertical Circuits with the video signal. The VERT SYNC signal is delayed 386 μs by the Shift Register in the Sync Delay circuit. This causes the SYNC signal to fall in the center of the blanking period; thus centering the video data on the raster. The DVSYNC (Delayed Vertical Sync) signal is then applied to the Vertical Ramp Generator.

Vertical Ramp Generator

The Vertical Ramp (Deflection) Generator creates the vertical deflection waveform that positions the beam vertically on the CRT. The SCR network's timing is controlled by the DVSYNC signal. The "Height" Control sets the cutoff point of the SCR's conduction curve; thus this control adjusts the rise time of the waveform. The DVSYNC causes the retrace signal as shown in Figure 7-13, which is timed to occur at a 60 Hz rate.

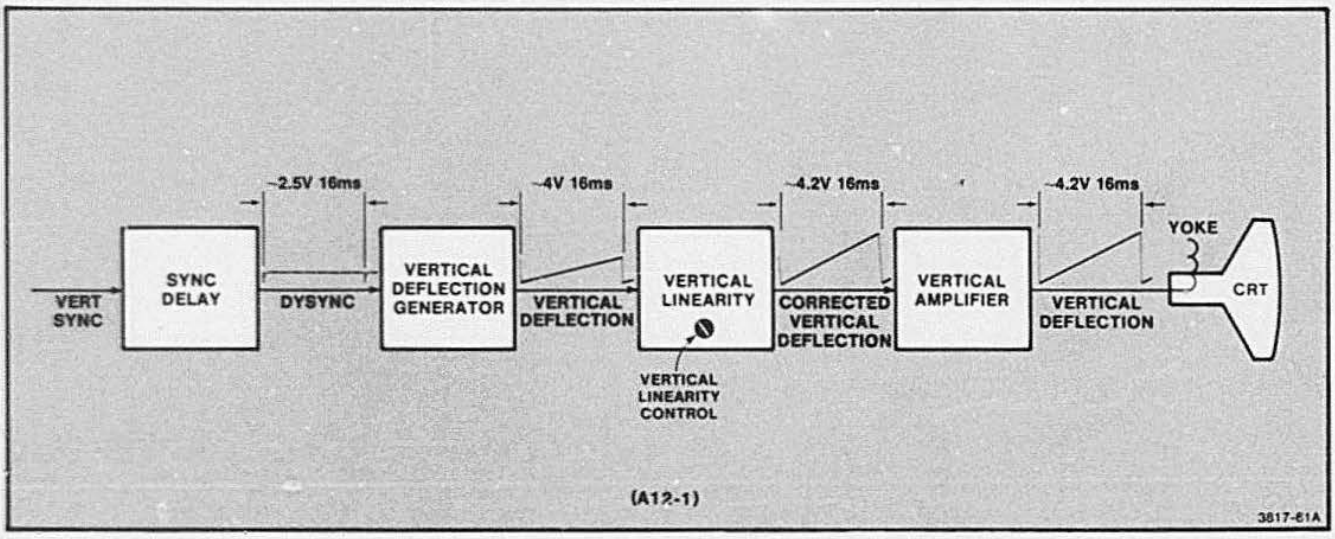


Figure 7-12. Vertical Circuitry Blocks.

Vertical Linearity

The Vertical Linearity circuit corrects for the curved face of the CRT by changing the linear deflection signal to an "S" waveform. This signal is further shaped by the output Amplifier, and then applied to the vertical deflection yoke.

The amplifier stage and the integrating output capacitor changes the linear ramp to the waveform shown in Figure 7-13A. The "Linearity" Control adjusts the amount of feedback and the amount of shaping. The output from the Vertical Linearity is applied to the Vertical Amplifier.

Vertical Amplifier

The Vertical Amplifier provides the power gain in the form of current to the deflection yoke for vertical deflection. This circuitry also provides additional shaping to create a uniform "S" corrected deflection current in the yoke. See Figure 7-13B.

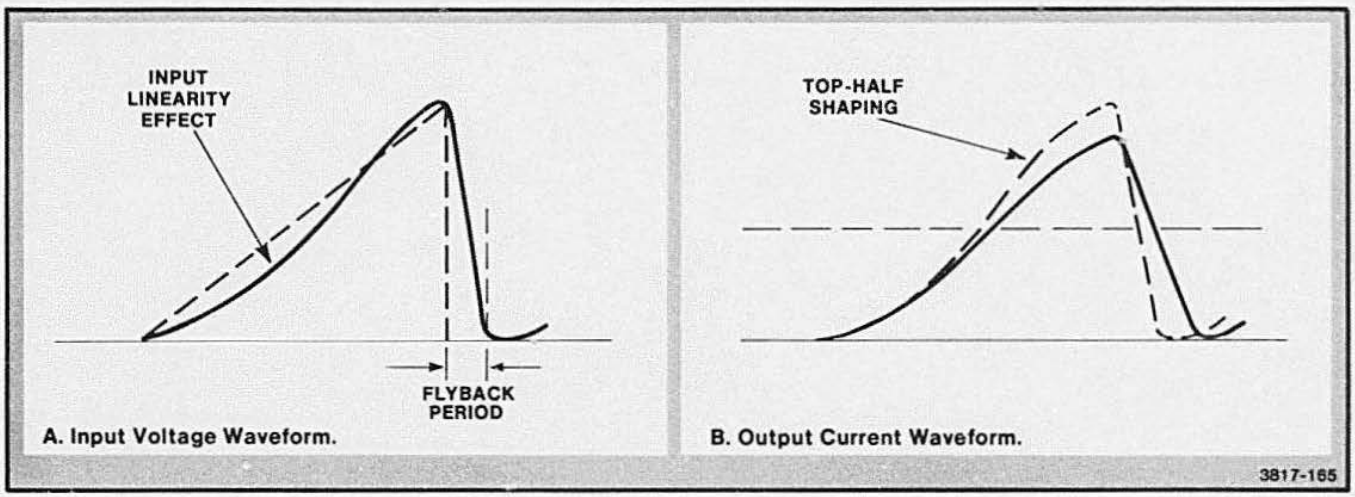


Figure 7-13. Deflection Waveforms.

This circuitry consists of several functional parts as shown in Figure 7-14. These are described as follows:

1. The Operational Amplifier (OP AMP) is an input stage and takes AC feedback, via the 10 μf Shaping Capacitor and "sense resistor," to make a regulated and uniform "S" waveform.
2. Next, a Driver transistor establishes the signal level required on the bases of the output transistors.
3. The Output stage is an NPN and a PNP power transistor connected as a "complementary class A-B emitter-follower" amplifier. Each of these transistors conducts for one-half of the output cycle; each one pumps current through the yoke in the opposite direction.
4. The diode and resistor fix the bias levels on the bases of the output transistors. This maintains the proper phase between the two output transistors.
5. The 330 μf AC coupling capacitor helps to establish the zero level for the output signal. This positions the raster vertically on the CRT face. Note that when the terminal is powered up, the CRT picture may oscillate up and down momentarily; this is caused by the initial charging time of this large coupling capacitor.

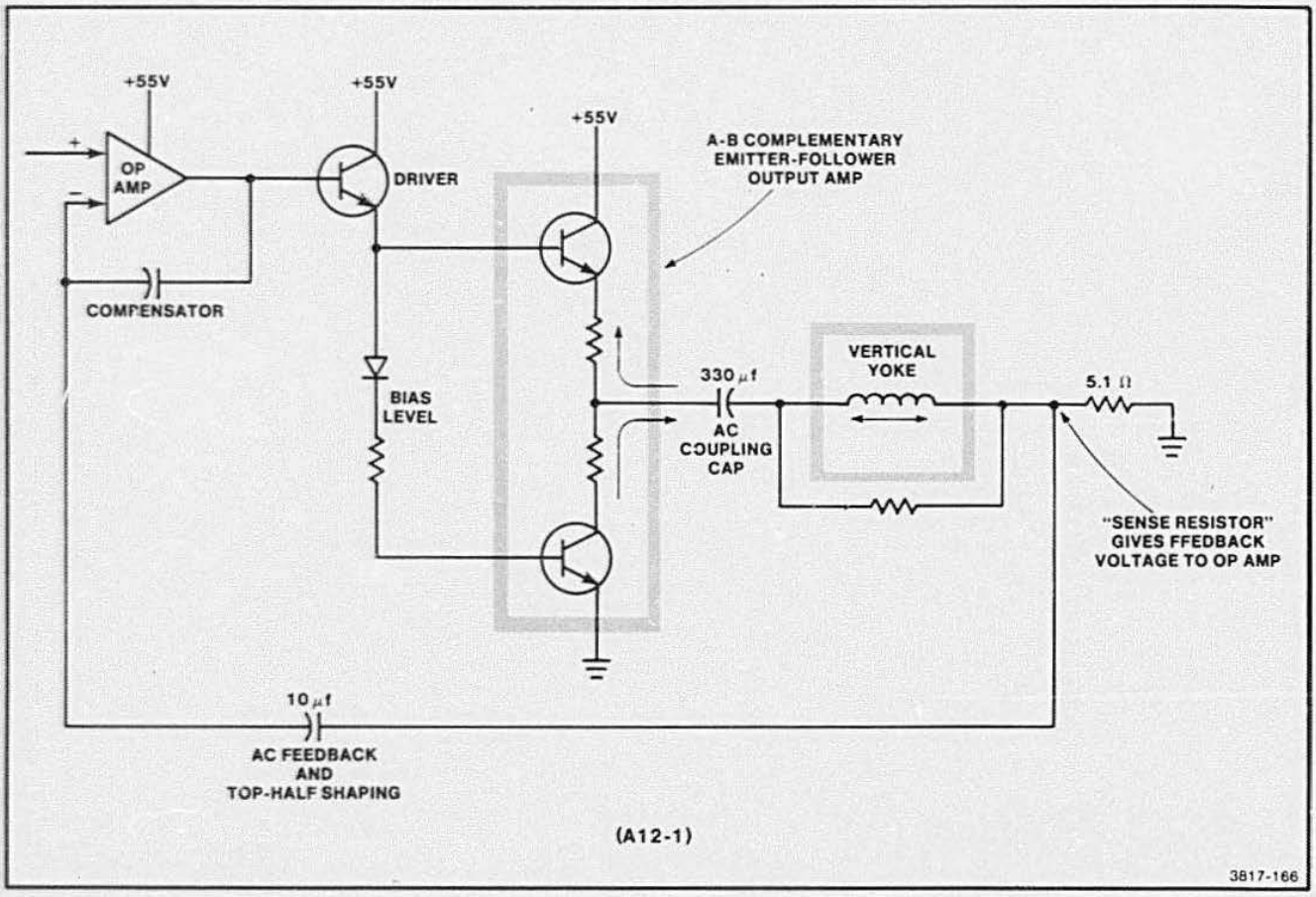


Figure 7-14. Vertical Output Circuit.

HIGH VOLTAGE SUPPLY

The High Voltage Supply (Figure 7-15) provides regulated 16 KVDC for the CRT, and other voltages for CRT and Deflection board. The circuit depends on the horizontal flyback pulse, from the Deflection board, for its operation. This feature protects the screen of the CRT from being exposed to the scanning beam without deflection. This flyback pulse also synchronizes the high voltage ripple with the horizontal scan.

Error Amplifier

The Error Amplifier accepts the Sense Output from the High Voltage Multiplier, as feedback, and indirectly regulates the transformer output voltages (via the Pulse Generator).

This circuit (part of Figure 7-16) consists of an Op-Amp based error amplifier, with the inverting (—) input connected to the "sense" (Vsense) feedback output of the 4X Multiplier; the non-inverting (+) input is connected to the 6.2 V reference. The output control voltage is a function of the magnitude and duration of the difference (6.2V — Vsense) on these inputs. The relatively high loop-gain of the overall system forces the control voltage to move to the level required to make Vsense equal to 6.2 V. Since Vsense is from a precision voltage divider, this circuit maintains 16.0 KV despite variations in load.

The output of this circuit is a signal, depicted in Figure 7-15, which enters the Pulse Width Generator.

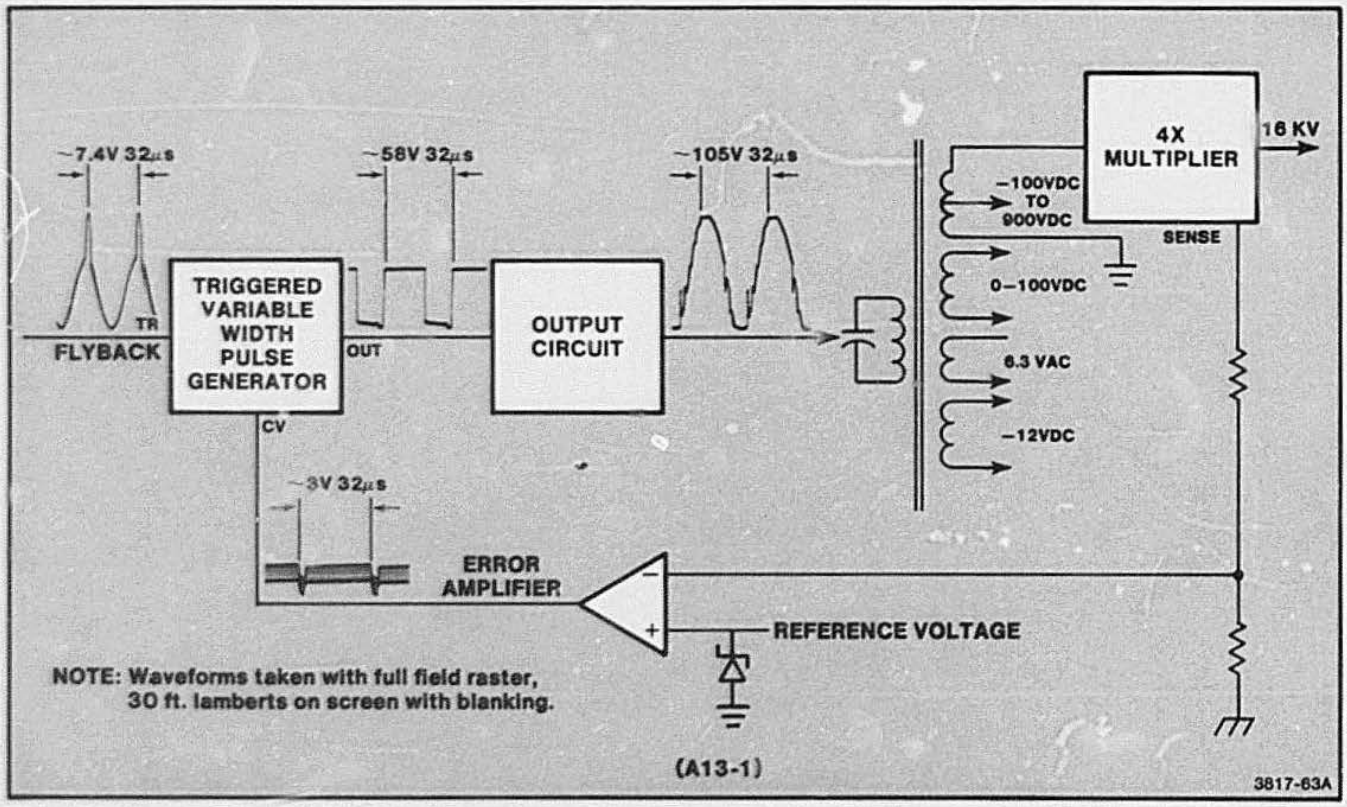


Figure 7-15. High Voltage Supply.

Triggered Variable Pulse Width Generator

The horizontal flyback pulse triggers this Pulse Generator, which produces an output pulse. The control voltage from the Error Amplifier determines the width of this pulse. Figure 7-16 is a functional diagram of this circuitry. The flyback pulse is amplified by a transistor and placed on the TR (trigger) input of the Pulse Generator. The 7555 chip is nearly identical in function to the more familiar 555 timer chip. The internal parts of this chip (a pair of comparators and a flip-flop) are shown in the block diagram.

The output signal is a variable width, constant amplitude, square wave. The flyback triggering synchronizes these pulses with the raster sweep frequency[2]. This output wave controls the current in the primary windings of the output transformer.

[2]This tends to eliminate a possible "swimming" effect (in the display image) caused by an out-of-sync condition.

Output Circuit

The Pulse Generator output pulse is converted into a sinusoidal high voltage pulse by the Output Circuit. Figure 7-17A is a functional diagram of this circuitry. An input driver transistor amplifies this voltage pulse and applies it to a combination of two transistors that function as a current switch. The main output transistor passes current (electron flow) from ground, through the transformer primary windings, to + 55 V. The internal capacitance of the transformer makes it look like a "tank circuit" that resonates at 31 KHz[3]. When a voltage pulse arrives, the final transistor (acting like a "class C amplifier") conducts the current pulse, which "rings" the transformer at 31 KHz. The variable width voltage pulse (A), at the input to this circuit, is transformed into a current pulse by the current switch.

[3]31 KHz corresponds to the horizontal sweep frequency on the CRT.

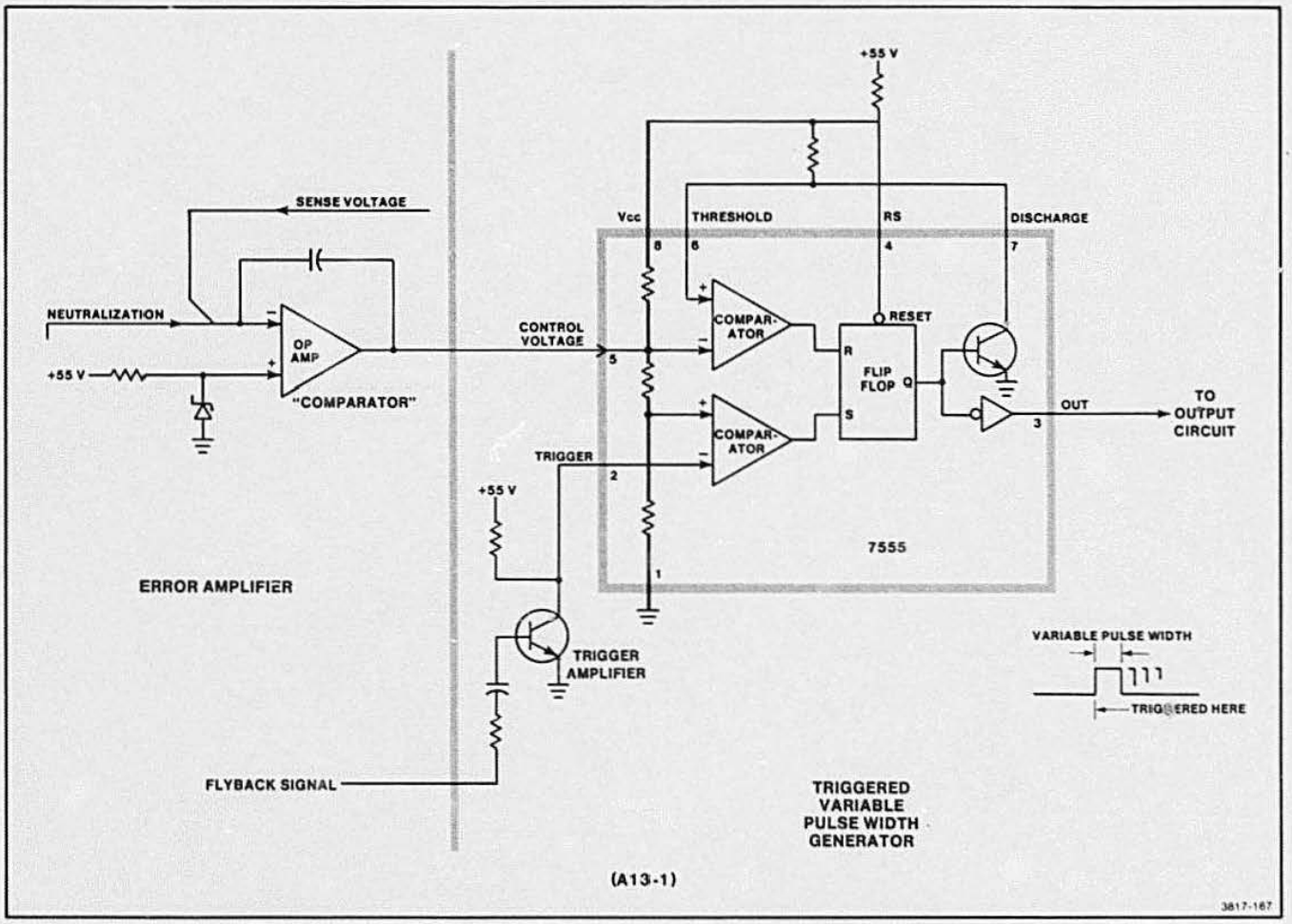


Figure 7-16. Error Amplifier and Pulse Width Circuits Functional Diagram.

This current pulse is then converted into a sinusoidal voltage wave (B) in the primary of the transformer. These waveforms are compared in figure 7-17B; notice the 180 degree phase angle between current (A) and voltage (B) waveforms. This is caused by the high current that flows when the output transistor switches on; this current pulls the voltage down to near zero. When the transistor turns off, the voltage recovers to the + 55V level and continues to rise to 110V (due to the inductance in the transformer). The voltage then immediately falls back creating a sinusoidal waveform. This induces voltages in the various secondary windings; one of these is the 4KV voltage that passes through the 4X Multiplier to make 16KV High Voltage for the CRT.

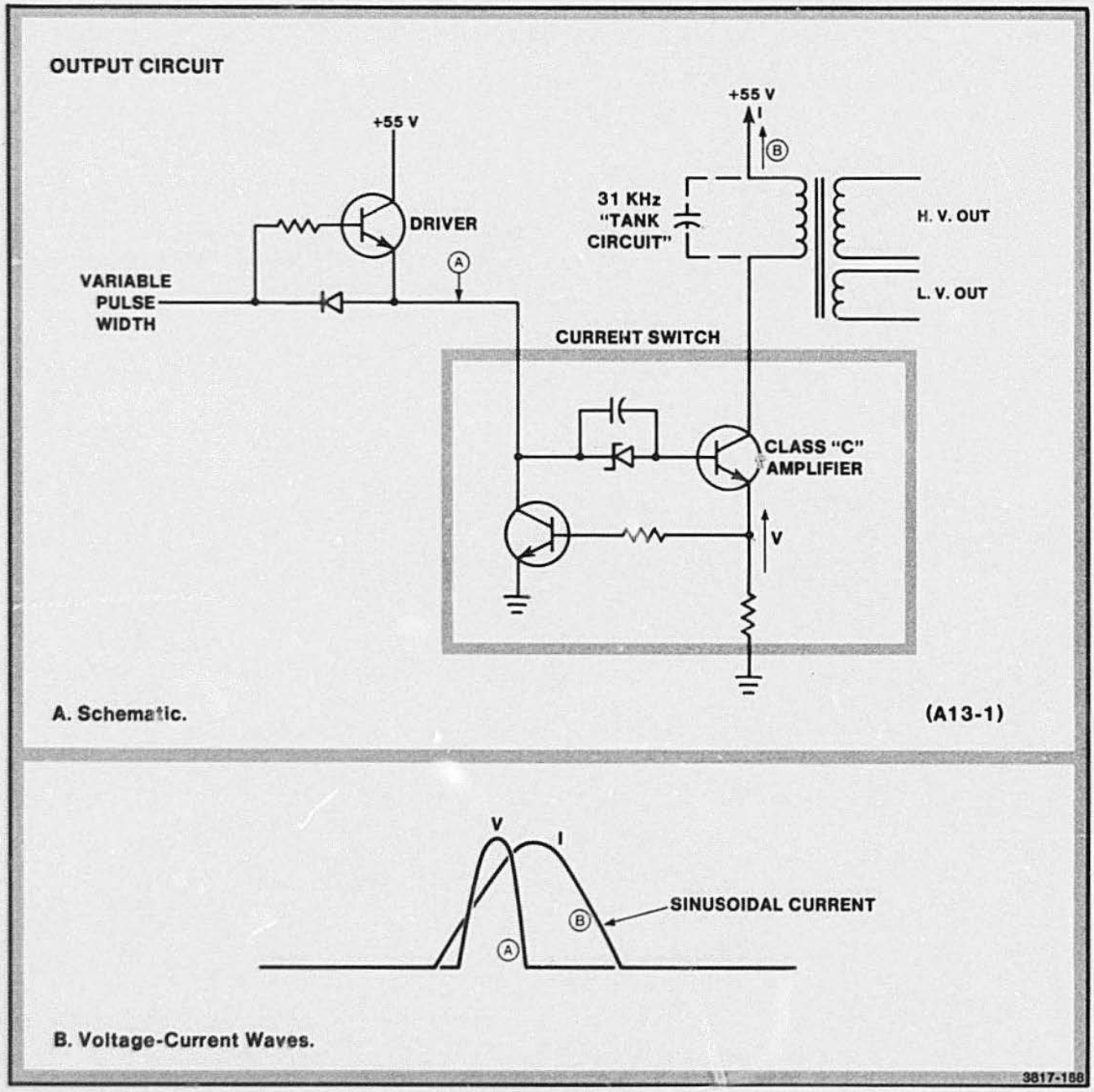


Figure 7-17. Output Circuit Functional Diagram.

High Voltage Multiplier and Rectifier Circuits

The High Voltage Multiplier module takes 8000 Vp-p AC from the transformer high voltage secondary and multiplies it to the required 16 KVDC for the CRT anode. This module also uses a series of passive elements to divide down its input voltage to a low level called "Sense." This Sense signal feeds back to the Error Amplifier to allow voltage regulation. See Figure 7-18.

A tapped output from this H.V. secondary, along with another secondary winding, produces the combination of voltages required for the various CRT grids. Figure 7-19 shows the placement and relative spacing of the grids in the CRT. This picture helps to show (without a detailed discussion of "electron optics") how the various grids affect the shaping, acceleration, and focus of the electron beam.

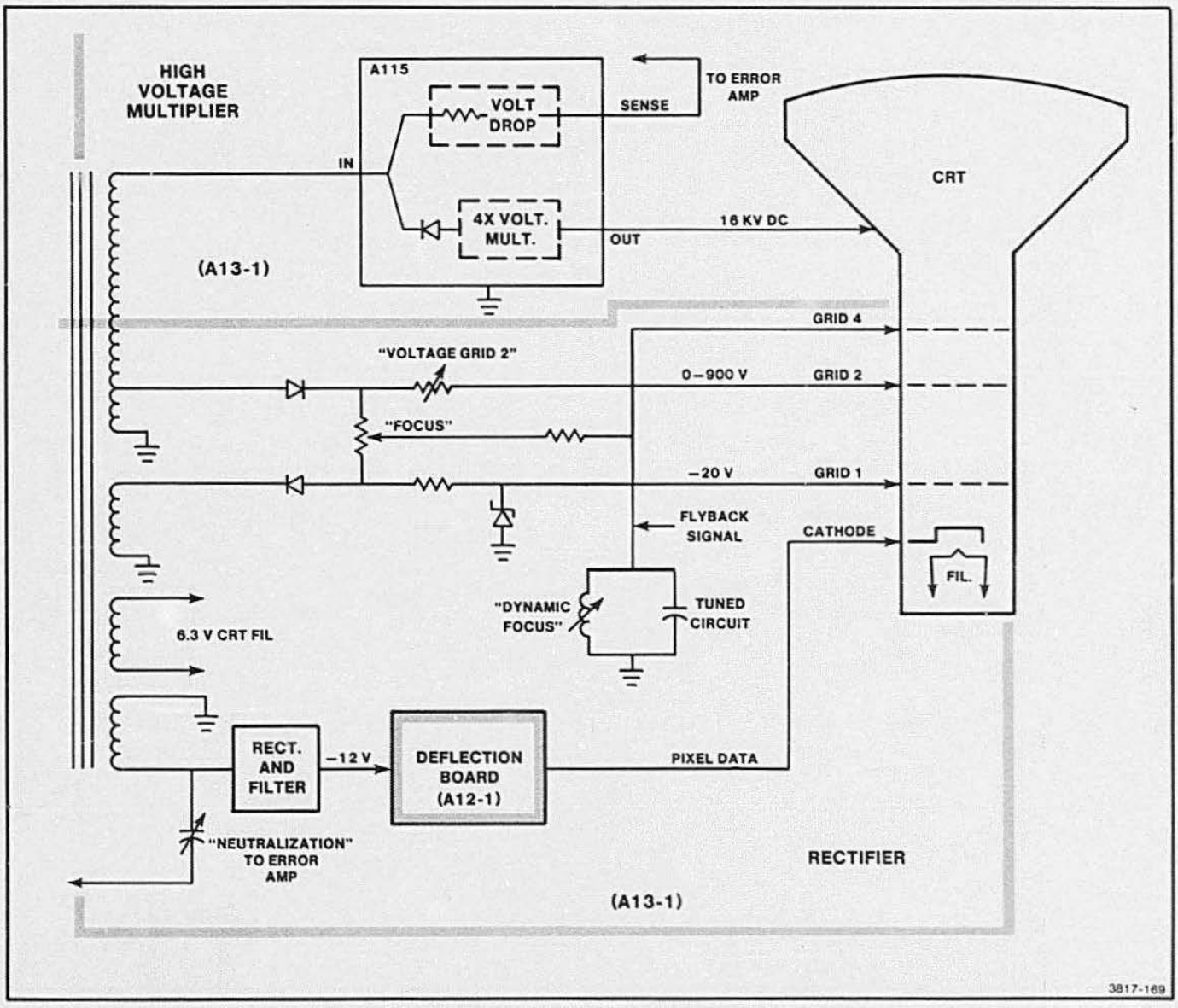


Figure 7-18. Multiplier and Rectifier Functional Diagram.

Pixel data is displayed by switching the cathode on and off, instead of switching Grid 1. The Grid 1 voltage affects CRT gain and cutoff. The −20 V Grid 1 value allows full intensity range from cutoff to full bright raster, using the available cathode voltage swing. The close proximity of Grid 1 to the cathode, with its −20 VDC, produces a preliminary focusing effect. Grid 4 is much further away from the cathode and is the primary focusing element; it pulls a much higher voltage from the variable resistor labeled "Focus." This variable resistor works between the −20 V on Grid 1 and the + 900 V on Grid 2. Grid 2 is called the "first anode" because it pulls the electron beam through the neck of the CRT; the 16 KV high voltage pulls the beam out to the screen. The adjustment for this Grid 2 voltage is labeled "VG2." It should be noted that the close proximity of these grids to each other causes their effects on the beam to be interrelated. See (A) in Figure 7-19. The consequences of this is dealt with in the Adjustment section of this manual.

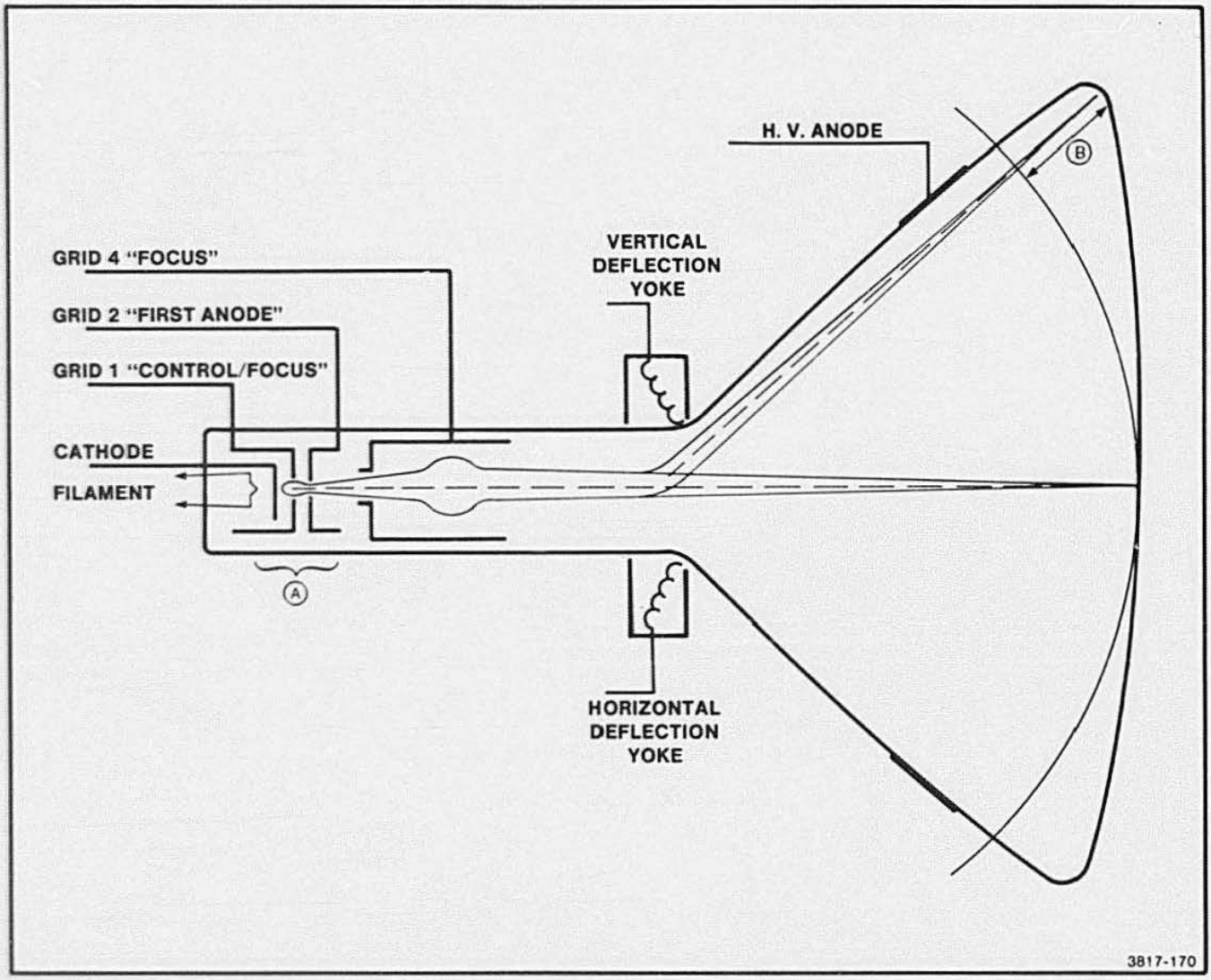


Figure 7-19. Internal Operation of CRT.

Another part of this circuitry provides dynamic focus. Figure 7-19 shows that the distance between the deflection point and the face of the CRT varies from the center outward (by a distance indicated as B). This means that the electron beam can be in focus at the center of the screen, and out of focus at the edges. This problem is corrected by first sensing where the edges are, and then adding a focus correction in those areas. One convenient way to detect the edges is to sample the flyback signal, which acts only when the beam reaches an edge of the screen. The flyback signal works with a tuned circuit to produce a bias component that is added to the main focus voltage. The adjustable coil in this tuned circuit changes the amplitude more than the resonant frequency of this bias voltage. This adjustment is labeled: "Dynamic Focus" on the schematic and on the High Voltage Board.

Two additional secondary windings on the transformer supply 6.3 VAC filament current for the CRT, and the −12 VDC for the Deflection Board circuitry.

Section 8

FUNCTIONAL CHECK AND PERFORMANCE CHECK PROCEDURES

INTRODUCTION

This section provides two kinds of quality check procedures:

1. Functional checks
2. Performance checks

The first procedure, functional checks, allows the user or service person to verify that all important aspects of terminal operation function properly. The second procedure allows the service person (or incoming inspection) to verify that the terminal operates in accordance with its advertized specifications. In the event that any performance check results do not meet the specifications listed there (and in Section 3), correct this by following the corresponding adjustment (calibration) procedure in Section 9.

FUNCTIONAL CHECK PROCEDURES

Functional check procedures for the 4112 consist of running Self-Test and using the Adjustment part of Self-Test to: display patterns on the screen, test the host port, perform a keyboard check, and reset CMOS parameters. If the terminal has Option 10 (3PPI) or Option 42 (disk option) installed, these may also be checked at the same time.

This section outlines the procedures for doing a functional check using the Self-Test and Adjustment Self-Test diagnostic programs. The details of these diagnostic programs are located in Section 10, *Troubleshooting and Self-Test*. If a problem is found during this functional check, refer to that section for further information about trouble-shooting and repair. Section 10 provides the following information which may be referenced while reading this section. Such information (which is not part of functional checks) is:

- The general theory behind Self-Test (and Adjustment part of Self-Test).
- The tests that Self-Test performs and the order in which it performs them.
- The light codes that are displayed on the keyboard as a particular test is running.
- Screen displayed error codes that appear if the terminal fails; with the explanations of these codes.
- Suggested corrective action to repair the problem (in some cases Self-Test will tell what the bad component is).
- Adjustment messages to aid in the adjustment of the graphics tablets.

POWER UP

Begin the performance testing of the 4112 by pressing the POWER button. The terminal immediately runs a diagnostic program (in firmware) that checks the essential functions of the 4112. This is the first part of the functional check.

A second, and more detailed, diagnostic routine is the the main Self-Test program. This routine may be used as a functional check since it verifies that all parts of the hardware are operational. Section 10, *Troubleshooting and Self-Test*, explains how to start Self-Test and how to interpret any error messages that it displays.

A separate part of Self-Test, called Adjustments, provides more of an interactive functional check of the display and other hardware. The remainder of this section deals with Adjustment Self-Test.

ADJUSTMENT SELF-TEST

Adjustment Self-Test is the third diagnostic program that may be used to check the terminal. Adjustment Self-Test is started in the same manner as the main Self-Test (the second part of the functional check). A procedure and some guidelines for Adjustment Self-Test are outlined as follows:

1. Start Adjustment Self-Test running by pressing and holding the SELF TEST and MASTER RESET buttons.
2. Release the MASTER RESET button.
3. After the keyboard lights begin to "cycle," release the SELF TEST button.
4. The keyboard LEDs will all turn on, and then off, and then cycle twice. This is the same as during main Self-Test.
5. After the keyboard lights finish "cycling," the keyboard bell will ring once. Then press the CTRL and C keys at the same time.
6. Once CONTROL C has been pressed, the terminal will pause for a few seconds and then display a general menu on the screen. The terminal is now in the Adjustment part of Self-Test.
7. The general menu tells which key to press to check any specified part of the terminal. These keys are always one of the eight "function keys" across the upper-left part of the keyboard.
8. Once one of these keys (designated by the menu) is pressed, a second menu (submenu) will be displayed.

Table 8-1

ADJUSTMENT CONTROL KEYS

Key	Action
CONTROL C	Displays (returns to) the general Self-Test menu.
CONTROL D	Displays the current menu.
CONTROL E	Exits from the current routine.
SPACE BAR	Repeats the current pattern/test.
Shifted Keys	A second function for specified key. The letters "Sh" in front of the key designation on the menu, means press the SHIFT key along with the designated key.

The General Menu

The General Menu is the first message that appears on the screen after Adjustment Self-Test is entered. The general menu is common for all 4110 Series terminals. An example of the general menu is shown below.

```
411X Menu
--
f1 4112 Display
f2 Processor Board
f3 Disk
f4 3PPI
f5 Tablet
--
Selection
*
```

The Disk, 3PPI, and Tablet functions only appear if that option is installed. The options may change key designations depending on which options are installed. For instance, if no disk option is installed, but the tablet and 3PPI options are, the 3PPI option would be selected by F3, and the tablet option would be selected by F4. Adjustment Self-Test for the tablet is used only in adjusting the tablet when Options 13 or 14 are installed. It is not used in this functional check procedure.

During Adjustment Self-Test, pressing CONTROL C will always cause this menu to be printed on the screen.

4112 Display Menu

After the general menu is obtained, select the display menu by pressing F1. This key is in the upper-left corner of the keyboard. After the 4112 Display Menu is selected, the following will appear on the screen:

```
4112 Display Menu
--
f1 Grid
f2 Gray Scale
f3 White Screen
f4 Dot Pattern
--
Selection
*
```

These patterns can be used during the functional check to insure that all display parameters are functioning properly.

1. Press function key, F3 —
   Observe a uniform white screen. Adjust the Intensity Control, as needed, to obtain a bright (white) screen. This control is located next to the upper-right corner of the display screen, above the optional disk drive unit. (This pattern is used later to calibrate the internal brightness adjustment.)
2. Press function key, F1 —
   Observe grid pattern, and verify that it is properly positioned (centered) on the screen.
3. Press function key, F2 —
   Observe in this pattern eight distinct levels of gray (from black to and including white).
4. Press function key, F4 —
   Observe full screen dot pattern. All dots must be visible as uniform dots. Verify uniform focus over the entire screen.
5. Press CTRL C to return to the General Menu.

Processor Board Menu

Once the General Menu has been displayed on the screen, select the Processor Board menu by pressing F2. After F2 is pressed, the Processor Board menu is displayed. The Processor Board menu looks like this:

```
Processor Board Menu
--
f1 CMOS-Reset
f2 Keyboard
f3 Host Port
--
Selection
*
```

Working from the Processor Board menu, perform the following tests.

CMOS-Reset, Function key F1. CMOS-Reset is used to restore the factory default settings of all the CMOS parameters. From the Processor board menu, press F1 function key. This action prints the following message on the display:

```
*f1
CMOS-Reset
Selection
*
```

This message means that the terminal's operating parameters have been restored to their factory default settings.

Keyboard, Function key F2. Pressing the F2 key causes every key on the keyboard to display two 2-digit hexadecimal numbers. These numbers represent the 8-bit codes that the Processor board generates for each downstroke and upstroke of a key. Each key has its own distinct hexadecimal code, and each down-stroke code is different than the corresponding up-stroke code. The first number of the up-stroke code is always eight more than the first number of the down-stroke code. The second character in the code is the same for both the down-stroke and the up-stroke of the key. This routine will verify that each key is operating properly. Figure 8-1 shows the Keyboard key codes.

Now return to the Processor Board menu by pressing CTRL D.

Host Port check, Function key F3. The Host Port routine checks the validity of the output port of the terminal. Enter the Host Port routine by pressing F3. Once this is done, the screen displays the following message:

```
Host Port
Attach Loopback
Press SpcBar
*
```

Connect the special LoopBack Connector onto the RS-232 port (labeled "to MODEM"). This connection is located on the back of the terminal. The LoopBack Connector forms a connection from the output port back to the input port. See Accessories List for the LoopBack Connector part number.

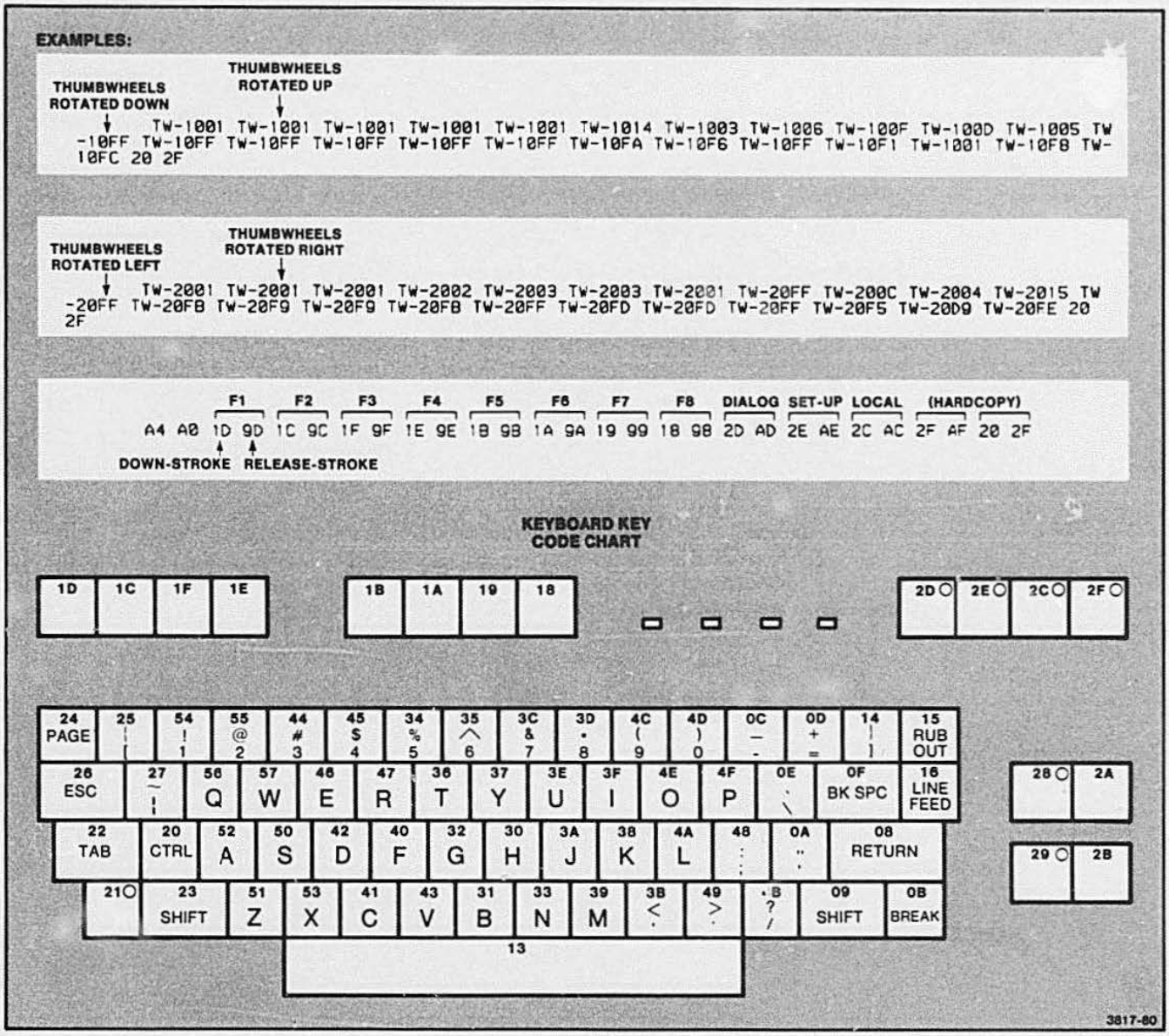


Figure 8-1. Keyboard Key Codes.

After the cable is connected, press the SPACE BAR. This starts the routine that sends signals representing characters 7F through 00 (at baud rates 9600 through 300). When this string of signals is sent and received properly, the screen indicates it by printing "Complete." This message means the terminal is ready to go on to the next test.

If there is an error during the Host Port routine, the following submessage will appear on the screen:

```
Host Port-Baud/Character
Baud: XXXX Expect: YY-AA Receive: ZZ-BB
```

where:

XXXX	is the baud rate in hexadecimal.
YY	is the signal sent (for example: 7F).
AA	is the expected bits in error, this should always read 00.
ZZ	is the signal received.
BB	is the bits in error.

After this Host Port check is complete, return to the general menu by pressing CONTROL C. If there are no options installed, this completes the functional check of the terminal. If there are options installed, select each option listed in the general menu and perform the following checks for that option.

NOTE

Only the disk and 3PPI options may be functionally checked using Adjustment Self-Test. The tablet menu is used for alignment purposes of the Graphic Tablet only (which is external to the terminal). The electronics for the tablet that resides in the terminal (Tablet Controller Board) were checked during main Self-Test. An alignment procedure for the graphic tablet using Adjustment Self-Test is contained in the 4110 Series F13/14 Graphic Tablet Instruction Manual.

Disk Option Menu

The Disk Menu may be obtained from the general menu by pressing F3. The Disk Menu is an optional menu and will only appear if Option 42 is installed. As Self-Test checked out the electronics of the Disk Controller board, this routine checks the drive unit. This menu is useful for drive unit head alignment. For this purpose a special alignment diskette (not used in this functional check) is required.

NOTE

The following is only a functional check and not an alignment procedure. This check only ensures that no error messages are received and that the drive does not hang up. An alignment procedure for the disk drives is found in the 4110 Series F42/43 Disk Options Service Manual and the 119-0977-01/03 Flexible Disk Drive Instruction Manual.

This is an example of the Disk Menu (items are self-explanatory):

```
Disk Menu
--
f1 No Operation
f2 Step Up One Track
f3 Step Down One Track
f4 Seek Track 0
f5 Seek Track 1
f6 Seek Track 38
f7 Seek Track 75
f8 Seek Track 76
Sh f1 Load Head
Sh f2 Unload Head
Sh f3 Arms Write Mode
Sh f4 Writes Track 76 With a 2F Pattern
Sh f5 Select Your Own Track
Sh f6 Change Device (Drive Unit) Address
Sh f7 Auto Load And Unload The Head On Track 0
--
Selection
*
```

If the disk option is installed, properly insert a disk in the drive unit before starting this test. Then make sure the WRITE PROTECT switch is set to the off position (the light is not lit).

CAUTION

It is best to perform this part of the functional check using a disk free of data. Performing this test may cause some data to be written on the disk. With the write protect switch off, it is possible to write over existing data. Therefore, it is best to use an outdated disk or one that contains unwanted data.

Press each of the disk menu keys in succession. No error messages should be received on any of the tests and the head should move to the selected area on the disk. After running through the head movements (in the menu), press CTRL C to return to the general menu.

NOTE

This is merely a check of the disk drive unit to ensure that no error messages are received and that the drive does not hang up. For a full alignment procedure of the drive unit, see the 4110 Series F42/43 Disk Options Service Manual.

3PPI ADJUSTMENT MENU/PROCEDURE

The key designations to select the 3PPI option from the general menu will depend on the options installed. If no disk or tablet options are installed, the F3 key will select the 3PPI Menu from the general menu. An example of this menu follows:

```
3PPI Menu
--
f1 3PPI Ports
--
Selection
*
```

This routine is designed to check the cables to the designated peripheral port. To start this test, press F1. The following will appear on the screen:

```
*f1
Select Port (0, 1 or 2)
*
Attach Host Port Cable to Selected
        3PPI Port and Press Spacebar
*
```

Connect the terminal host-port RS-232C cable to the 3PPI-port to be tested. Connect the other end of the cable to the terminal's host-port connection (called "MODEM"). Then type the number of the port to be tested (0, 1, 2) followed by pressing SPACEBAR.

If there are no errors, the following message will appear on the screen; then the next port may be tested. If an error occurs, consult Section 10.

```
Test in Progress
Procedure Complete
Select Port (0, 1, or 2)
*
```

This completes the 3PPI "Adjustment" procedure and messages.

TABLET OPTION MENU

If the tablet is installed, press F5 from the general menu to access the tablet adjustment and verification check. The tablet menu/message is:

```
Tablet Menu
--
f1 Tablet Timing Adjustment
--
Selection
*
```

At this time, the interconnect cable must be connected between the terminal and the tablet. After this is done, the F1 key may be pressed. When the pen or cursor is placed on the tablet, and the button or pen pressed, the following will appear on the screen.

```
*f1
X = 3.845  Y = 5.455  Button = Z  Using a Cursor
X = 3.845  Y = 5.605  Button = Z  Using a Cursor
```

Using the pen produces:

```
X = 3.405  Y = 3.765  Button = 0  Using pen
```

and pressing the pen button, out of tablet presence produces:

```
X Timing Straps = 00010001
Y Timing Straps = 00010000
```

Refer to Section 10 (Self-Test) for explanations of tablet error messages.

Tablet Timing Straps Verification

Figure 8-2 shows the location of the timing straps on the Tablet Controller Board. These straps are labeled and the values are marked on the board. X and Y have HEX values to FF. Y1, Y2, Y4, and Y8 are one digit and Y16, Y32, Y64, and Y128 are the second digit. The X straps are marked similarly. There are eight timing straps for each axis, X and Y. These switches are set using the precision grid and the firmware in the 4112. Each bit of the timing straps has a value of 0.01 inch. All eight straps give a total of 2.55 inches per axis.

If the strap is on the two upper pins, the input to the register is a logical one. When the strap is down, the input of the register is a logical zero. Y32, Y64, Y128, X32, X64, X128 are cut straps and are set to logical zero. Normally, they do not have to be changed.

This completes the functional checks for the terminal with options installed.

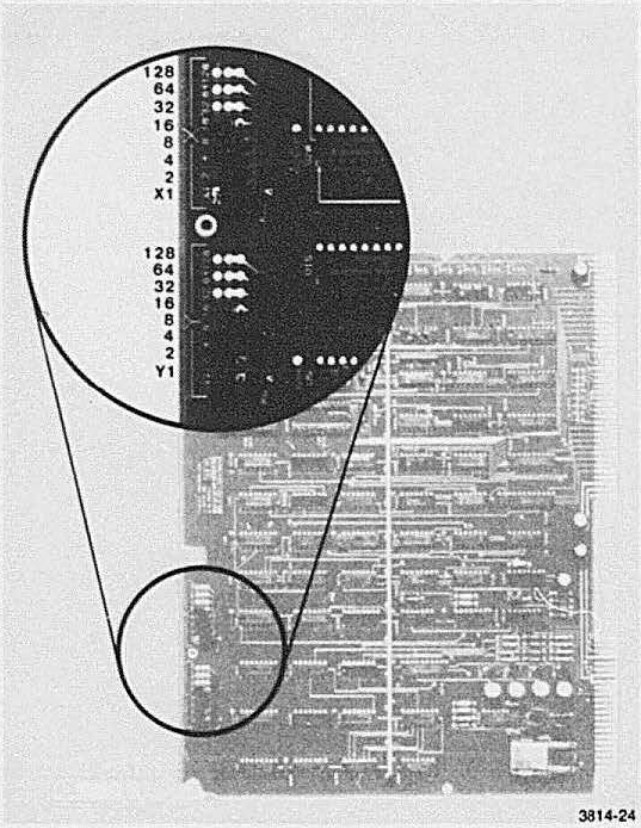


Figure 8-2. Tablet Controller Board Timing Strap Locations.

PERFORMANCE CHECK PROCEDURES

The verifiable specifications listed in Section 3 in Table 3-2 are listed here along with a verification procedure for each. These specifications all pertain to parameters/signals in the Display Module.

VIDEO SIGNAL LEVEL

Procedure:

1. Power OFF. Remove main cover from 4112.
2. Locate plug, P586, on Deflection board.
3. Connect 75 Ω 'scope probe to Pin 2 of P586.
4. Turn 4112 power ON.
5. CHECK - for High = 1.0 V max with writing beam on.

HORIZ SYNC FREQUENCY

Procedure:

1. Power OFF. Remove main cover panel from 4112.
2. Locate plug, P586, on Deflection board.
3. Connect 'scope probe to Pin 7 of P586.
4. Set time base for 31.5 KHz, and set amplitude for TTL logic level.
5. Turn 4112 power ON.
6. CHECK - for 31.500 KHz ±300 Hz (for 60 Hz sweep), or 31.250 KHz ±300 Hz (for 50 Hz sweep).

VERTICAL SYNC FREQUENCY

Procedure:

1. Power OFF. Remove main cover panel from 4112.
2. Locate plug, P586, on Deflection board.
3. Connect 'scope probe to Pin 5 of P586.
4. Set time base for 50/60 Hz, and set amplitude for TTL logic level.
5. Turn 4112 power ON.
6. CHECK - for 57 Hz min to 63 Hz max (for 60 Hz frame rate), or 47 Hz min to 53 Hz max (for 50 Hz frame rate).

Section 9

ADJUSTMENT PROCEDURES

This section describes the adjustment procedures for the 4112. The Display Module is the main analog part of the terminal and the focus of attention in this adjustment section. The Power Supply Module is used in other products and has a separate service manual where its adjustments are listed. See the *620-0295-00 Low Voltage Power Supply Service Manual.* A short-form adjustment list for this supply is at the end of this section.

This adjustment procedure is based on the use of function keys that are programmed by the Self-Test diagnostic program in 4112 firmware. This section includes direct instructions for using Self-Test for adjustments only. See Section 10 (Volume 1) for more detailed information about Self-Test.

RECOMMENDED TEST EQUIPMENT

Table 9-1 lists the test equipment needed to check and adjust the 4112. The listed equipment specifications are the minimum required to perform these tests. If alternate equipment is used, it must meet or exceed this specification.

Table 9-1

RECOMMENDED TEST EQUIPMENT

Description of Equipment	Equipment Minimum Specification	Example
Frequency Counter	0 — 50 kHz	TEKTRONIX DC 503
Oscilloscope (dual trace)	Vertical: 5 mV/div. Time base: 10 ns/div. 80 MHz.	TEKTRONIX SC 504
Scope probe	10:1 attenuation	TEKTRONIX P6108
Digital Voltmeter	0 — 100V DC & AC (p-p) 0.1 % accuracy	TEKTRONIX DM 501
High Voltage Probe	20 kV	FLUKE Model 80K-40
Photometer and Luminance Probe	Capable of reading 100 ft-lamberts max	TEKTRONIX J16 with J6503 probe
Flat blade screwdriver	1/8 inch	

DISPLAY MODULE ADJUSTMENT PROCEDURE

SHORT-FORM PROCEDURE

WARNING

Read the Safety Summary at the beginning of this manual before performing these adjustments.

Table 9-2 is an abbreviated procedure for the Display Module. This procedure is for quick field reference. This abbreviated listing assumes a familiarity with the detailed procedure that follows.

LONG-FORM ADJUSTMENT PROCEDURE

Figure 9-1 is on a pullout at the end of this manual. This figure shows the physical location of each adjustment referred to in this procedure. The bracketed letters by each of the adjustments listed in the text also appear on the illustration, thus showing the location of each component to be adjusted Pull out this diagram and refer to it while working through these procedures.

CAUTION

Section 11 (Maintenance) describes the procedures for opening the terminal and accessing the adjustments referred to in this section.

1. Initial Setup

a. Remove cover from terminal. See procedure in Section 11.

b. Unscrew and swing open the Card-cage to provide full access to the adjustments and test points on the Display Module.

c. Press POWER button.

2. Display Test Patterns

Put up a white screen on the display. To do this follow this procedure.

a. Press the SELF-TEST button and hold it in. This button is located on the back of the terminal, above the power supply, and to the left of the MASTER RESET button.

b. Press the MASTER RESET button and then release it. The keyboard LED lights come on and go off as different parts of circuitry are tested.

c. After the keyboard LED lights begin to "cycle," release the SELF-TEST button.

d. Press and hold the CONTROL and C keys at the same time, and then release them. After a general Power-Up sequence is run, a menu listing Self-Test Routines will be printed on the screen.

e. From this menu, select Display. This displays a second menu of the patterns to be used in adjusting the Display Module. Table 9-3 shows this menu.

f. After putting up a white screen on the display (function key F3), you may have to adjust the Intensity control to get a picture on the screen. This control is located next to the upper-right corner of the display screen, above the optional disk unit.

g. Observe the raster pattern on the screen.

h. VERIFY — that the vertical and horizontal sweeps are both functioning.

Table 9-3

4112 DISPLAY MENU

Function Key	Pattern
F1	Grid
F2	Gray scale
F3	White screen
F4	Dot pattern

Table 9-2

DISPLAY MODULE ADJUSTMENTS

Adjustment (& Setup)	Check	Adjust
1. Horiz Oscillator:		
a. Remove J586	b. Frequency at T741 Pin 2	R781 for 31.5 kHz ± 50 Hz
c. Replace J586		
2. Null H.V. Comp.	Voltage on TP141 (use scope and x10 probe.	C332 to min level (null to 2 V p-p)
3. DC Level:		
a. Self-Test Key F1 (grid pattern)	b. Z axis cathode signal	INTENSITY control for max contrast
	c. Voltage on J588 Pin 2 = 54 VDC	R381 for + 54 VDC at black level
4. Focus:		
a. Self-Test Key F4 (resolution pattern)	b. Dynamic focus	L535 to focus center of both sides of screen.
	c. Static focus	R250 to focus center of screen.
	d. Uniform focus overall	L535 and R250 again.
5. Picture Centering:		
a. Self-Test Key F1 (grid pattern)	b. Level picture	Rotate yoke
	c. Voltage on J591 Pin 1	R723 for + 47 VDC
	d. Uniform horiz spacing	L721 for H. linearity
	e. Uniform vertical spacing	R194 for V. linearity
	f. Vertical size	R179, lines = grid ptn.
	g. Grid pattern centered	Centering magnet rings
6. Final Linearity and Size:	a. Equal vertical spacing	L721 adjust
	b. Horizontal size	R723 adjust
	c. Vertical size	R179 adjust
	d. Vertical linearity	R194 adjust
	e. Horizontal linearity	Centering rings
7. Gray Scale tracking:		
a. Self-Test Key F3 (white pattern)	b. 0 ft-lambert intensity	INTENSITY control
	c. No background raster	VG2 pot (R510)
	d. Black level voltage on J588 Pin 2 to + 54 VDC	R380
	e. 44 ft-lambert at center of screen	BRITE pot (R580)
8. Gray Levels Check:		
Self Test Key F2 (shade pattern)	Eight distinct gray levels	
9. Horiz Oscillator Adjustment:	a. 100 V p-p on T741 Pin 2	
	b. 31.30 kHz on T741 Pin 2	H OSC pot (R781)
10. H.V. Ripple Check:	Less than 40 V p-p on the H.V. Anode button	
11. H.V. Level Check:	15.2 – 16.8 kV on the H.V. Anode button	

3. Check Horizontal Oscillator ("H OSC," R781)

This and the following adjustments are located on the Deflection board in the Display Module:

a. Remove the cable from J586 [P][1]; this allows the horizontal oscillator to run free.

b. CHECK — the horizontal sync frequency using a frequency counter. Put a probe on the collector of Q761 or Pin 2 of T741 [L][1]. The voltage at this point will be about 100 V p-p.

c. ADJUST — frequency to 31.500 kHz ±50 Hz by adjusting the horizontal oscillator control, R781 [M][1]. 60 Hz is set for 31.500 kHz; 50 Hz (option) is set for 31.250 kHz.

d. Turn off power to terminal.

e. Plug Video Cable onto J586 [P][1].

f. Turn power back on.

4. Test Mode

To test the signal circuit, use the Self-Test switch. The screen should light up with a full raster background.

5. Null High Voltage Compensation (C332)

This and the following adjustments are located on the High Voltage board in the Display Module.

a. Place the 10X 'scope probe on TP 141 (U138 Pin 6) [A][1]. This is the output of the error amplifier.

b. ADJUST — C332 [B][1] for minimum amplitude observed on the scope. (It should null within 2 V p-p.) This adjustment effects high voltage regulation.

6. Set D.C. Level (R381)

a. Place the 10X 'scope probe on the exposed Pin 2 of J588 [K][1].

b. CHECK — the Z-axis CRT cathode signal; see Figure 9-2.

c. Start Self-Test, and then press F1 (putting up the Grid Pattern).

d. ADJUST — Intensity control on front panel for maximum contrast.

e. ADJUST — R381 (Z-axis DC Level) [O][1], so the "black" level of video is at +54 VDC.

7. G1 (Grid 1) Level Check

CHECK — Grid 1 voltage. Use DVM (Digital Voltmeter) and put its probe on TP435 [C][1]. This voltage should be −19.3 V ±0.35 V (18.95 to 19.65V).

8. Focus Adjustment (L535, R520)

a. Put the Resolution Pattern on the screen by pressing function key F4.

b. ADJUST — the dynamic focus coil, L535 [F][1], to focus the center part of both sides of the screen.

c. ADJUST — R250 [E][1], Static Focus, for the best focus at the center of the screen.

d. ADJUST — focus so that it is uniform across center of screen.

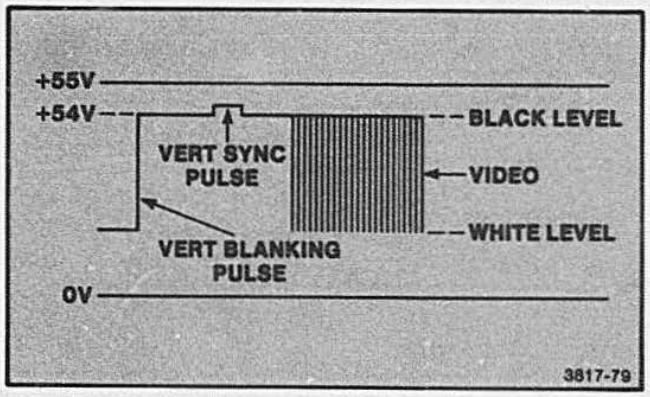


Figure 9-2. CRT Cathode Signal.

[1] This bracketed letter is a component location reference for Figure 9-1.

NOTE

The best dynamic focus is obtained when G4 (Blue Lead) amplitude is approximately 500 to 800 V p-p. Also, you may need to use a magnifying eyepiece to determine precise focus.

There is no dynamic focus adjustment for the vertical direction of the CRT, so the focus at the top and bottom corners may not be as sharp as the focus in the horizontal center area.

e. If necessary, repeat the dynamic focus adjustment to achieve overall uniform best focus.

CAUTION

When adjusting the ceramic potentiometers R179, R194, R381, and R580, be gentle with the screwdriver adjusting tool. Their ceramic cases are relatively fragile, and if cracked will cause erratic operation.

9. Picture Centering Procedure (R723, L721, R194, R179)

This procedure is a preliminary adjustment for linearity.

a. Put up the calibration grid pattern on the screen by pressing F1.

b. If picture is not level, ADJUST by rotating yoke.

c. Place DVM probe on emitter of Q1001 (Pin 1 of J591) [G][1].

d. ADJUST — Horizontal Width pot R723 [H][1] for correct emitter voltage on Q1001.

e. CHECK — for DVM reading of 47 VDC on Pin 1 of J591. This sets the horizontal width very close to its specified value.

f. ADJUST — Horizontal Linearity coil L721 [I][1] as per Step g.

g. CHECK — for equal distance (approximately 5 in. or 125 mm) from the center line to the outside line of both sides of the screen pattern. See Figure 9-3A. Use a scale/ruler.

h. ADJUST — R194 [Q][1] for optimum Vertical Linearity.

i. CHECK — for equal spacing from center line to the top and bottom lines on screen pattern. See Figure 9-3B.

[1] This bracketed letter is a component location reference for Figure 9-1.

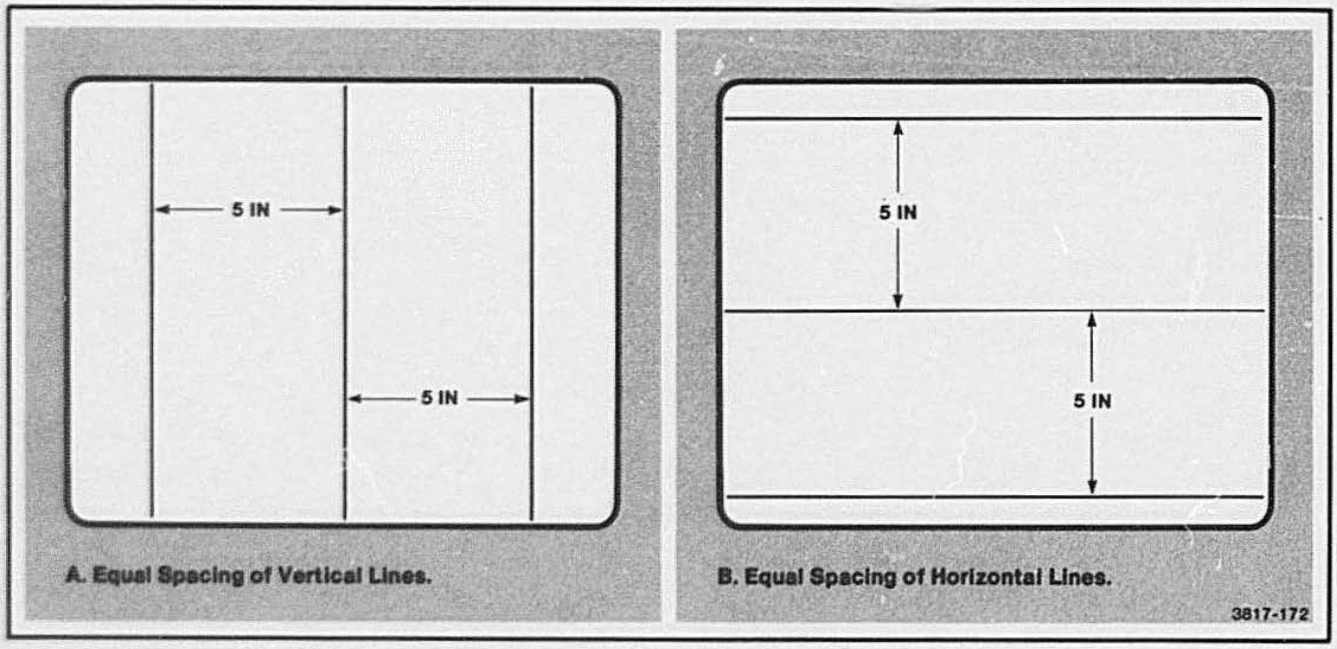


Figure 9-3. Picture Adjustment Pattern.

j. ADJUST — R179 [R][1] for correct Vertical Size as per Step k.

k. CHECK — that the top and bottom lines are approximately the size of the lines in the grid pattern and fill the screen.

l. ADJUST — the centering magnet rings [S][1] to center the grid pattern on the screen.

m. VERIFY — that calibration grid pattern is centered on the CRT screen. Use a scale/ruler to measure spacing between pattern lines and edges of screen/bezel.

This procedure positions the picture on the CRT screen.

10. Final Linearity and Size Adjustments (L721, R723, R179, R194)

This step is a calibration step and is intended to fine-tune the display adjustments. (Grid Pattern should be on screen from Step 9.)

a. ADJUST — L721 [I][1] for optimum horizontal linearity.

b. CHECK — for equal spacing between vertical lines.

c. ADJUST — R723 [H][1] for optimum Horizontal Width.

d. CHECK — Horizontal Width verifying that pattern fills screen in the horizontal direction.

e. ADJUST — R179 [R][1] for proper Vertical Size.

f. CHECK — to see that Grid Pattern fills screen in the vertical direction.

g. ADJUST — R194 [Q][1] for optimum Vertical Linearity.

h. CHECK — for equal spacing between all horizontal lines.

i. The Centering Rings [S][1] may need to be moved in order to position the Grid Pattern properly on the screen.

j. Repeat Steps a through i until the entire display is adjusted horizontally and vertically.

11. Gray Scale Tracking and Maximum Luminance Adjustment (INTENSITY, R510, R381, R580)

a. Put up a white screen (press F3).

b. ADJUST — Intensity Control on bezel to give 0 foot-lamberts of intensity.

c. ADJUST — "VG2" Pot, R510 [D][1], so background raster is barely visible.

d. ADJUST — R380 [O][1] for proper video black level voltage (+ 54V).

e. CHECK — video black level voltage by placing scope probe on the exposed Pin 2 of J588 [K][1]. Scope should read voltage at + 54 VDC.

f. ADJUST — "Brite" control, R580 [N][1], for a brightness level of 44 foot-lamberts.

g. CHECK — brightness at center of screen, using the J16 photometer and the P6503 brightness probe. Verify level of 44 foot-lamberts.

h. SET — "Intensity" control (on front panel) to give a luminance value of 34 foot-lamberts as measured by the probe and photometer.

i. Put gray scale pattern on screen (key F2).

j. CHECK — for eight distinct levels of gray (from black to, and including, white).

12. Resolution Test

Put up the Resolution Dot Pattern (key F4). All dots must be visible as individual dots. Repeat Step 11 if not.

[1] This bracketed letter is a component location reference for Figure 9-1.

13. Horizontal Oscillator Adjustment (R781)

This test checks the Horizontal Sync frequency.

a. Connect a probe from the frequency counter to the collector of Q761 or Pin 2 of T741 [L][1].

b. CHECK — voltage at this point. It should be 100 V p-p.

c. CHECK — frequency at this point. It should be 31.300 kHz.

d. ADJUST — "H OSC," R781 [M][1], so that the free running frequency of this oscillator is 31.300 kHz ±15 Hz.

14. High Voltage AC Ripple Test

NOTE

This test need only be performed if components in the High Voltage circuitry have been replaced.

CAUTION

The scope can be damaged if 500 pf is charged and discharged through the probe. Ground the scope end of the capacitor during power-up and power-down.

a. Power down the terminal and wait two minutes to allow the high voltage to drain down.

WARNING

Lethal voltages exist at the CRT anode button, and proper precaution must be taken to prevent injury.

b. Put one lead of a 500-pf 20-kV capacitor around the CRT anode button [T][1]. Be sure to make contact with the metal button under the insulating cover.

c. Ground the other lead of the 500-pf capacitor to the chassis.

d. Power up the terminal.

e. Disconnect grounded capacitor lead from ground point. Connect this lead to the 10X scope probe.

f. CHECK — for less than 40 V p-p ripple voltage.

g. Remove scope probe from capacitor lead, and ground this lead.

h. Turn terminal power off and wait two minutes for high voltages to leak off.

i. Remove capacitor lead from anode button.

15. Measure High Voltage

a. With terminal power off, connect Fluke high voltage probe to CRT anode button [S][1].

WARNING

Be sure to connect the ground wire of the high voltage probe to a chassis ground before turning on the power.

b. Set the digital voltmeter to 20 VDC scale and connect its high voltage probe.

c. Secure the high voltage probe to the metal part of the CRT anode button.

d. Turn terminal power on.

e. CHECK — high voltage to see if between 15.2 kV and 16.8 kV.

f. Turn power off, wait two minutes, and remove high voltage probe.

[1] This bracketed letter is a component location reference for Figure 9-1.

POWER SUPPLY ADJUSTMENTS

The full adjustment procedure for this part of the 4112 is located in the *620-0295-00 Power Supply Service Manual.* This is a condensed procedure, included here for convenience.

1. DC Voltages

a. CHECK — + 55V output at J74 (Pin 4) on the Invertor board.

b. ADJUST — R591 (on Invertor board) for reading of + 55.1V ± 100 mV, at test point J74 (Pin 4). See Figure 9-4.

c. CHECK — voltages and tolerances indicated in Table 9-4. These voltages track on + 55 V, so the adjustment in Step b should cause these voltages to meet specifications.

Table 9-4

POWER SUPPLY VOLTAGE LIMITS

Nominal Voltage	Test Point	Range (Tolerance)
+ 5 V	J73 Pin 4	4.85 to 5.15 V (5 V ± 3%)
−5.2 V	J73 Pin 10	−4.99 to −5.41 V (−5.2 V ± 4%)
+ 12 V	J73 Pin 1	11.64 to 12.36 V (12 V ± 3%)
−12 V	J73 Pin 8	−11.64 to −12.36 V (−12 V ± 3%)
+ 24 V	J74 Pin 2	23.28 to 24.72 V (24 V ± 3%)
+ 55 V	J74 Pin 4	53.90 to 56.10 V (55 V ± 2%)

2. CHECK — Control Voltages

Use the procedure in the *Power Supply Service Manual* to check: INIT-0 and PWRFL-0.

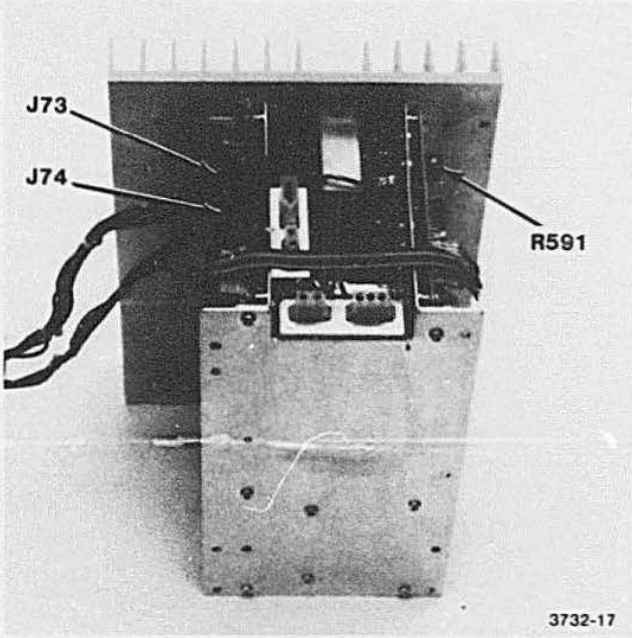


Figure 9-4. Power Supply Test Points.

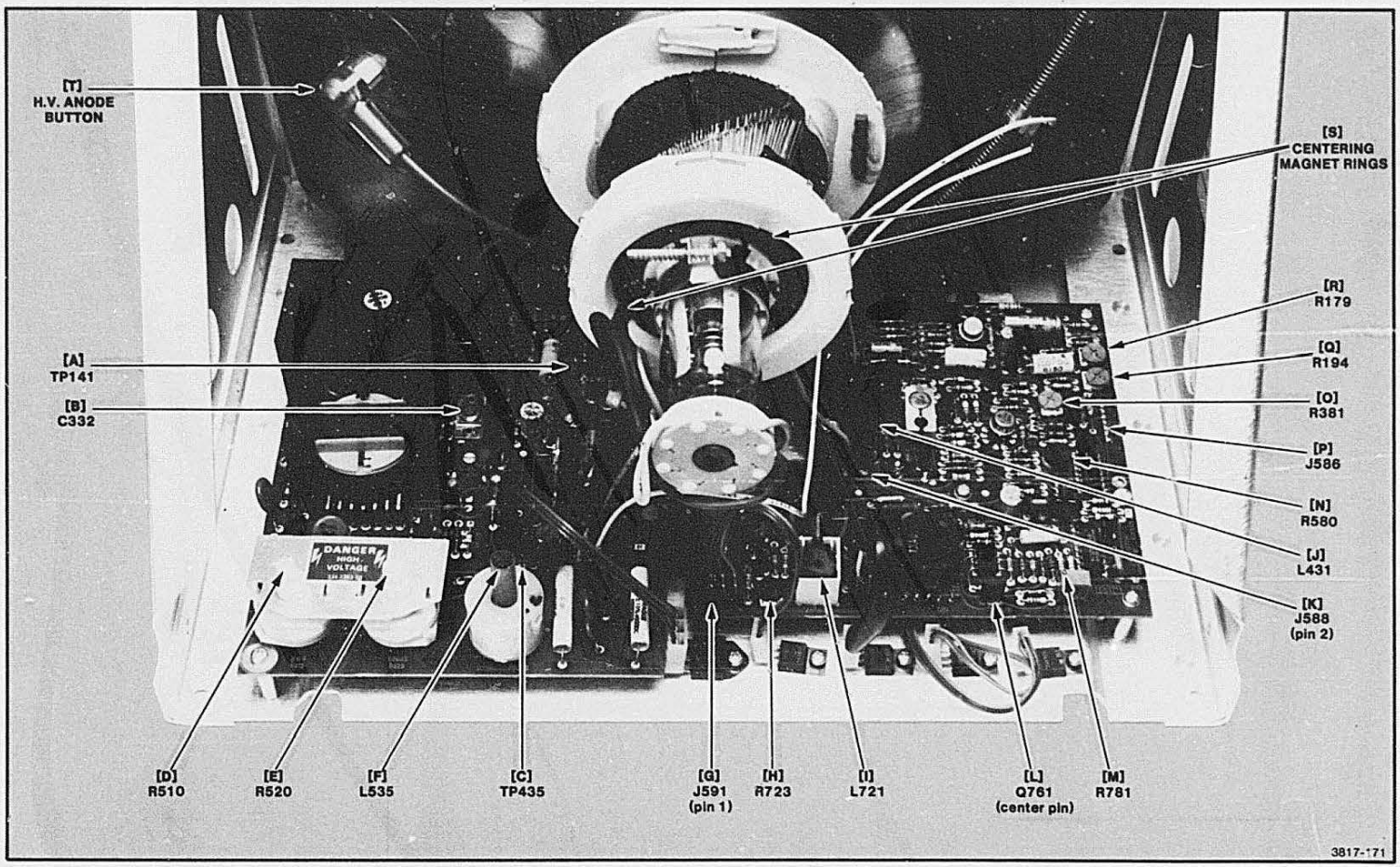


Figure 9-1. Display Module Adjustment Locations.

Section 10

TROUBLESHOOTING AND SELF-TEST DIAGNOSTIC

The 4112 is a minisystem that functions as a graphics terminal. The Self-Test program helps to isolate problems to a particular part of this system. Before running Self-Test or going into an involved troubleshooting procedure, check the most obvious kinds of faults first: diskette problems, improper connections to peripherals or host system, line voltage fluctuations, or a faulty data path. Avoid blind attention to seemingly obvious causes, thus overlooking the real (masked) problem.

Make full use of this manual as a troubleshooting aid. The theory of operation, diagrams in text and on foldouts, gridded circuit board photos, and schematic diagrams can help to isolate a problem.

WARNING

Before opening the terminal for servicing and troubleshooting, read the Safety Summary at the beginning of this manual.

TROUBLESHOOTING, INITIAL/VISUAL CHECKS

When a particular circuit board or module appears faulty, remove this board and carefully examine it for signs of heat or broken connections. If such signs appear, use the component location diagrams with the schematic to pinpoint the function of the defective circuit. If the component function matches the operational defect, replace the defective part(s) or replace the complete circuit board/module (depending on the availability of replacement boards at your service site).

DISPLAY MODULE PROBLEMS

The Display Module uses raster scanning display technology, and as such is very similar to the display section of most monochrome television receivers. Display problems can be grouped as follows:

- Blank screen — can mean 1) burned out filament in CRT, or 2) loss of 16KV high voltage to CRT, or 3) loss of low voltage to accelerating anodes of CRT (from LV Supply Module). If high voltage is low, check Multiplier circuit.
- Low contrast — check video multiplier, level shifter, and video amplifier circuits.
- Picture leans or breaks up into horizontal lines — check horizontal delay, phase-locked-loop, horizontal driver, and horizontal output stage.
- Dot of light — no vertical or horizontal deflection.
- Only a horizontal line — check vertical sync, vertical deflection generator, vertical linearity, and vertical amplifier.
- Vertical line only (no horizontal deflection) — check horizontal driver, and horizontal output.
- Raster on screen but no information displayed — trace the data signal path from input through to the CRT.

These are customary checks when troubleshooting a raster display.

LOW VOLTAGE POWER SUPPLY PROBLEMS

Check fuses and circuit breakers first. Then measure the voltage level on each of the outputs (no-load situation). Then watch these supplies as they are loaded up to the allowed current limits. See the *620-0295-00 Power Supply Service Manual* for specifications and procedures for adjusting and troubleshooting this module. The adjustment of this power supply module, as used only in a 4112 terminal, is treated in Section 9, *Adjustment*.

DISK OPTION TROUBLESHOOTING

The Self-Test helps to isolate problems to a particular part of the disk option subsystem. However, troubleshooting procedures should check the first and most obvious kinds of faults first: diskette problems, or line voltage fluctuations. Be sure to have the *Option 42/43 Service Manual*, and the *Disk Drive Unit Service Manual* on hand when troubleshooting disk-related faults.

Initial/Visual Checks

If your terminal is communicating properly with its host system but fails to read or write to its disk, look for disk-related problems. Check the media, cables and connectors, or the part of the power supply module that provides disk unit power.

Disk Media Problems

One of the first and easiest tests to make for disk-related problems is to remove the current diskette and replace it with a known good diskette. Try writing to the good disk and then read it, and see if the problem persists. If the problem remains, it is either in the drive unit of the Disk Controller board or in the connecting cables or power supply.

Hard and Soft Errors

When disk operations fail to execute properly, they are classified as:

- "Soft errors" — recoverable and random in nature
- "Hard errors" — persist after several retries.

Soft errors, related to the disk, happen when the R/W head can't find a file header, or when R/W data does not match expected data. The mechanical limitations of the disk and drive unit allows temporary misalignments, oxide dropout on the disk, dirt particles under the R/W head, etc. To keep these transitory problems from hanging up the system, the terminal's processor recognizes the condition and issues ten retries. If the problem persists, the processor issues a head move command and again calls for another ten retries. If this is unsuccessful, a hard error is reported.

Hard errors, related to processing on the Disk Controller Board, cause the main processor to issue ten retries. If the problem remains, the processor gives up and reports the condition as a hard error.

Another kind of hard error occurs when a write command finds that the disk is not inserted, the disk is write-protected, or a similar operator oversight. In such a case the problem appears constant, so no retries are made. The command/operation is aborted, and a message prompts the user to correct the problem.

Disk Drive Unit Faults

See the *119-0977-00* (or the equivalent) *Disk Drive Unit Service Manual*.

SELF-TEST DIAGNOSTIC PROGRAM

The primary troubleshooting aid for the 4112 is the Self-Test diagnostic program. This program resides in firmware and is arranged so it checks most of the hardware (see NOTE), starting with the initial error reporting mechanism (keyboard LEDs). Self-Test does not depend on any portion of the hardware until it has tested it; it may then use such hardware to aid in other tests.

NOTE

The main Self-Test program does not test the Power Supply or Display Module. Power Supply problems are relatively easy to isolate. Read the paragraph on Power Supply problems earlier in this section.

The Display Module is not checked automatically during the main Self-Test. However, you may verify the operation of its basic parts by running the Adjustment part of Self-Test (press function key F1). The four screen-adjustment patterns may be used to determine what part of the Display Module is malfunctioning.

PARTS OF SELF-TEST

There are three separate parts of the Self-Test program: the main Self-Test program, Power-Up, and Adjustment Self-Test. An additional diagnostic, System Errors Detector, is not really a part of Self-Test but is described in this section also. Figure 10-1 shows how these diagnostics are related to the main Self-Test firmware.

Power-Up

A subset of Self-Test is the Power-Up sequence. This diagnostic cannot be called directly by the user, but runs automatically each time the terminal is turned on. It performs a quick check of the various hardware modules. The *4112 Operator's Manual* describes the error messages that may appear during the Power-Up sequence. For detailed diagnostic examination of terminal hardware, use Self-Test. Self-Test will perform additional tests as well as repeating the same tests that were done during the Power-Up sequence.

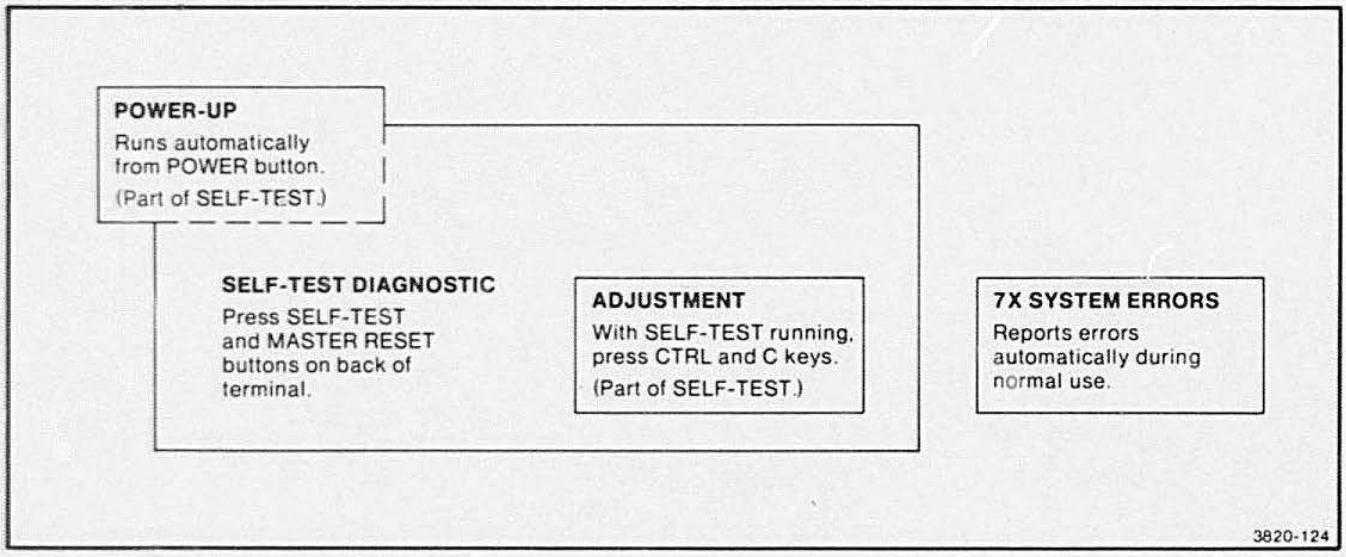


Figure 10-1. Self-Test Functional Diagram.

Main Self-Test

The main part of Self-Test is that portion which runs when the SELF TEST and MASTER RESET buttons are pressed. Tnis routine repeats the Power-Up sequence and then goes on to thoroughly test the entire terminal hardware, including any options that may be installed.

Adjustment Routine

The Adjustment part of Self-Test is used primarily for making adjustments and performance checks. However, this routine may also be used as a diagnostic tool, particularly on certain options such as the 3PPI. This routine is accessed from inside Self-Test by pressing the CTRL and C keys together. Detailed instructions about this part of Self-Test are located at the end of this section.

7x System Errors Detector

This error-detecting firmware contains routines that catch system level or operator-induced errors at the time they occur, not just during Self-Test. These error-reporting routines are in ROM and have the same general syntax as the Self-Test error messages, but this error-reporting device runs separately and independently of Self-Test. This allows it to report such errors spontaneously at the time a problem appears. The error codes that come under this category are listed and described in Table 10-1. If an error is reported that seems to be related to a hardware malfunction, run Self-Test to verify and locate it.

CONTROL FLOW OF SELF-TEST

Figure 10-2 shows the order in which the various hardware modules are tested. The three areas "flagged" with a 0 must function for Self-Test to run. After these three areas are verified as functional, the keyboard lights and keys are tested (1 on Figure 10-2). Then areas 2 through 9 are tested in that order.

Figure 10-7 (on the pull-out at the end of this section) shows the detailed logical flow of Self-Test. This is the order in which the diagnostic checks are made when Self-Test is initialized. This figure does not include any submessages. The flow chart shows a left-to-right flow across each page, as each test is checked and passed. When a negative response to a test occurs, the resulting checks and error report is indicated by the downward flow from that point. If the error is not fatal, the flow may loop up to the main path again, allowing Self-Test to continue running.

As stated earlier, a subset of Self-Test is the Power-Up sequence. This sequence checks approximately 60% of the 4112 circuitry and is performed every time that the 4112 is turned on.

In Table 10-1, the diagnostic checks that are performed during the Power-Up routine are marked by the letters PUP. When the full version of Self-Test is run, all the tests are performed, including a repeat of the Power-Up checks. This table only contains the tests executed by a standard 4112 terminal. The firmware used to check the options (such as the disk drive or Tablet Interface board) are contained on those optional boards.

NOTE

The light codes: FD (1111 1101), CF (1100 1111), and BB (1011 1011) represent subtests, and are not included in Table 10-1 even though they are listed in the tables that follow. These subordinate tests are not part of the main Self-Test path. Each is run only after its main test finds a fault. For a definition of these codes, see Tables 10-3 through 10-14.

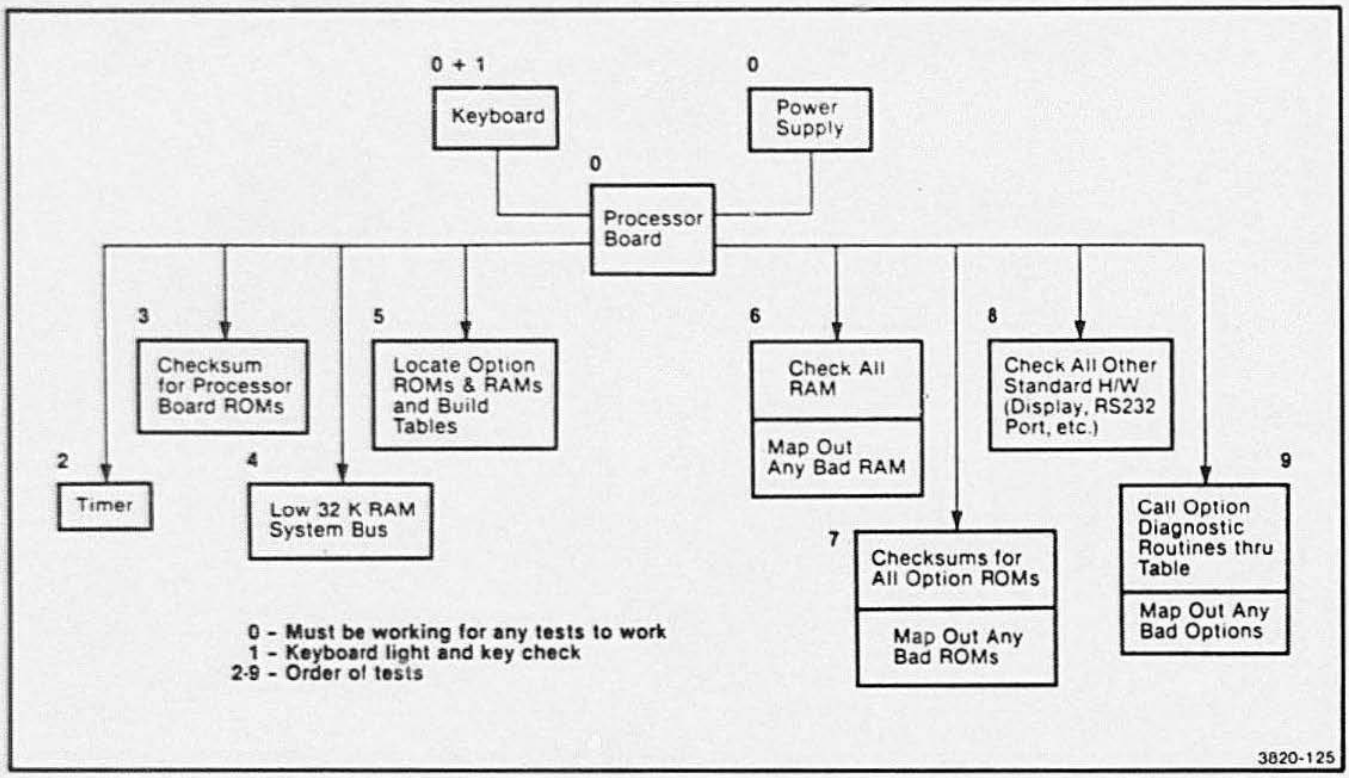


Figure 10-2. Self-Test Program Block Diagram.

Table 10-1

POWER-UP/SELF-TEST SEQUENCE

Error Code Hex/Binary	Explanation	When Executed[a]
FE 1111 1110	Light checking routine	SLF
FC 1111 1100	Keyboard key check	SLF
EF 1110 1111	Timer check	SLF/PUP
EE 1110 1110	Timer set up routine	SLF/PUP
EC 1110 1100	Standard system ROM check	SLF/PUP
DF 1101 1111	Lowest 32K bus address check	SLF/PUP
BF 1011 1111	Lowest 32K RAM walking ones check	SLF
BE 1011 1110	Lowest 32K RAM walking zeros check	SLF
BD 1011 1101	Lowest 32K RAM all ones check	SLF/PUP
BC 1011 1100	Lowest 32K RAM all zeros check	SLF/PUP
B5 1011 0101	RAM stack building	SLF/PUP
BA 1011 1010	RAM/ROM memory tables building	SLF/PUP
DE 1101 1110	High address bus check	SLF/PUP
B9 1011 1001	Upper RAM walking ones check	SLF

Table 10-1 (cont)

POWER-UP/SELF-TEST SEQUENCE

Error Code Hex/Binary	Explanation	When Executed[a]
B8 1011 1000	Upper RAM walking zeros check	SLF
B7 1011 0111	Upper RAM all ones check	SLF/PUP
B6 1011 0110	Upper RAM all zeros check	SLF/PUP
B4 1011 0100	System vector table expansion	SLF/PUP
FA 1111 1010	Keyboard identification set	SLF/PUP
CE 1101 1110	Processor ROM check	SLF/PUP
8F 1000 1111	Video Controller test	SLF/PUP
8E 1000 1110	Raster memory test	SLF
8D 1000 1101	Vector Generator test	SLF/PUP
8C 1000 1100	Raster memory address test	SLF/PUP
AF 1010 1111	CMOS and ROM to RAM load	SLF/PUP
EB 1110 1011	Interrupt checker	SLF/PUP
DD 1101 1101	Host port register checker	SLF/PUP
DC 1101 1100	Host port baud/character checker	SLF
CD 1100 1101	Option numbers checker	SLF/PUP
CC 1100 1100	Version compatibility checker	SLF/PUP

[a] SLF means the test is performed during Self-Test.
PUP means the test is performed during the Power-Up routine.

SELF-TEST FIRMWARE JUMP TABLES

To further aid in understanding how Self-Test works, refer to the ROM Header-Pointer diagram (Figure 10-3). This diagram shows how Self-Test is arranged around a jump-table system. This arrangement allows code updates and additions/deletions of option code sections to be mapped in or out easily.

HOW TO RUN SELF-TEST

Start Self-Test running by pressing the MASTER RESET and SELF TEST buttons. Press and hold MASTER RESET and SELF TEST; then release the MASTER RESET button first. After the Keyboard LEDs begin to "cycle," release the SELF TEST button also.

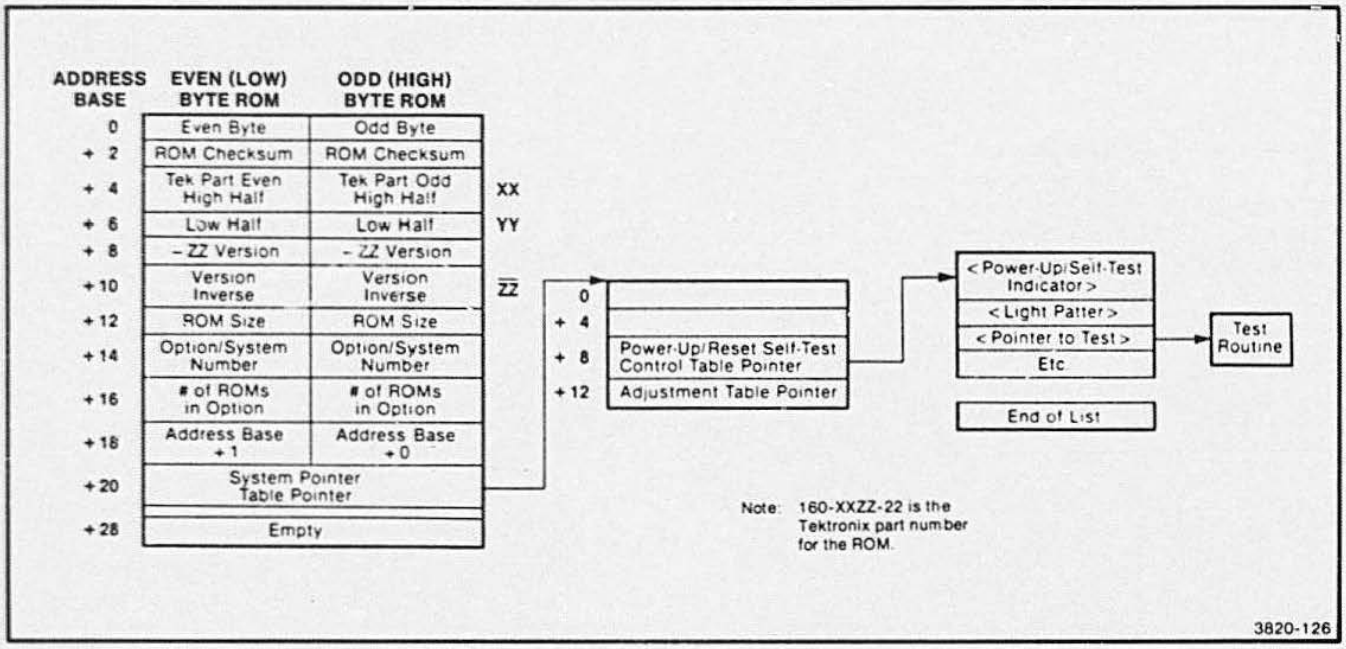


Figure 10-3. The ROM Header-Pointer Diagram.

The test begins by turning on all the keyboard lights ("CAPS LOCK" key, four function key LEDs, and four indicator LEDs). The CAPS LOCK key light should turn off immediately (while the other eight LEDs remain lit). If the CAPS LOCK key light remains lit, there is a major malfunction in the processor.

While Self-Test is running, the eight keyboard lights blink through the codes for the various tests. When a fatal error occurs during a particular test, its identifying light pattern comes on blinking, and the bell rings three times. These light patterns are displayed on the eight indicator LEDs, across the top of the keyboard[1]. These light patterns indicate the binary equivalent of a hexadecimal code assigned to each major set of tests. The error message tables (in this section) list and define these error codes. The tables give an explanation for each error condition and suggest which piece of circuitry malfunctioned. After the major error codes have been displayed, most problems can be narrowed down through the use of submessages. Submessages are displayed by first noting the major error codes, pressing RETURN, and noting the next set of lights displayed as the submessage. In some instances, there may be up to three levels of submessages.

The first error code to appear may not indicate the actual problem. Keep pressing RETURN after each error code to let Self-Test continue. The remaining error codes will isolate the real problem.

After the display has been checked, most error messages are printed on the display screen. Such screen-displayed error messages first print the name of the test or the hardware module being tested. Then a submessage, on the next line, tells which part of the test failed.

Suppose Self-Test finds a major hardware problem that prevents the test from running to completion. This is indicated by the light code for this test (where the problem was found) remaining lit indefinitely. This type of problem is highly unlikely, but could be caused by a bad ROM. Read the error code on the lights and use this to help determine where the test has aborted.

During the Delay Memory check (associated with Table 10-8, RAM Tests) there is a 14 second wait for each 32K of RAM being tested. In a fully loaded instrument (one with all RAM options installed), this test can take up to four minutes to run. Do not be surprised about this delay; it does not mean that Self-Test is "hung." If you wish to override this lengthy test, enter CONTROL D during the keyboard check and Self-Test will skip over this test.

[1] The eight LEDs extend from the KYBD LOCK light to the HARD COPY key light.

SELF-TEST ERROR MESSAGES

This part of the section lists and describes the Self-Test error codes. In the following discussion, tests are grouped in modules according to the hardware being tested. Under each heading (test module name) is a short general description of the test and hardware it checks. Each table of error messages defines those messages that may appear while that test is running. To determine which piece of circuitry malfunctioned, read the list of active circuits for each test. Since many circuits are used in several tests, eliminate as "good" those circuits that passed all previous tests. These tables are grouped together for referencing convenience rather than the order in which the tests occur. Tables start with the error code FE (1111 1110) and are listed in descending order of the binary codes. Table 10-2 shows this order.

ERRORS DIRECTORY

Table 10-2 is a reference that shows which table to consult when any given error message is displayed. The Hex codes, in the center column, correspond to the light codes (displayed in binary on the LEDs) for each test category.

Table 10-2

SELF-TEST ERRORS DIRECTORY

Test Module	Hex Code[a]	Table Number
KEYBOARD/PROCESSOR	Fx	10-3
PROCESSOR BOARD	Ex	10-4
RAM/BUS HOST PORT	Dx	10-5
SYSTEM OPTION ROMS	Cx	10-7
RAM TEST	Bx	10-8
CMOS MEMORY	Ax	10-9
DISPLAY BUS AND BOARD CHECKS	8x	10-10
SYSTEM (7x) ERROR MESSAGES[b]	7x	10-11
SELF-TEST OPTION ERRORS DIRECTORY		
3PPI (OPTION 10)	6x	10-12
DISK (OPTION 42)	5x	10-13
TABLET (OPTION 13/14)	4x	10-14

[a] 'X' indicates this digit will change within the table.

[b] The 7x error codes are not part of Self-Test but are rather error codes that are generated if a problem occurs during normal use of the terminal. Self-Test does not have to be initialized in order to receive these error messages.

NON-OPTION ERROR MESSAGES

This part of the section lists the error messages that correspond to the main 4112 hardware. The error codes for the options are listed later in this section.

Keyboard Check and Lights (F)

When Self-Test starts, the indicator LEDs will show FF (1111 1111). As the test continues the light patterns approach 00.

During the keyboard lights check, each light is slowly turned on and off in a sequential loop. The loop begins at the keypad, goes across the eight LEDs (right to left), and down to the CAPS key light. This circling light pattern is then repeated quickly.

At the beginning of the keyboard keys' test, the 4112 rings the bell once, and the CAPS key light starts blinking. This prompts the user to press a key (any key) after waiting a few seconds. When the bell rings and the CAPS key blinks, the test is supposed to stop and wait for a key stroke. If the test proceeds without you pressing a key, this means spurious key strokes are being generated. This type of problem could be caused by dirt or corrosion in the keyboard, or a poor connection in the keyboard-to-processor board ribbon cable. If the test waits for a key entry, then press a key, allowing the tests to continue. If you wait too long before pressing a key, the test will "time out" and continue (this usually takes about 20 seconds). Figure 10-4 shows the locations of the keyboard ROMs.

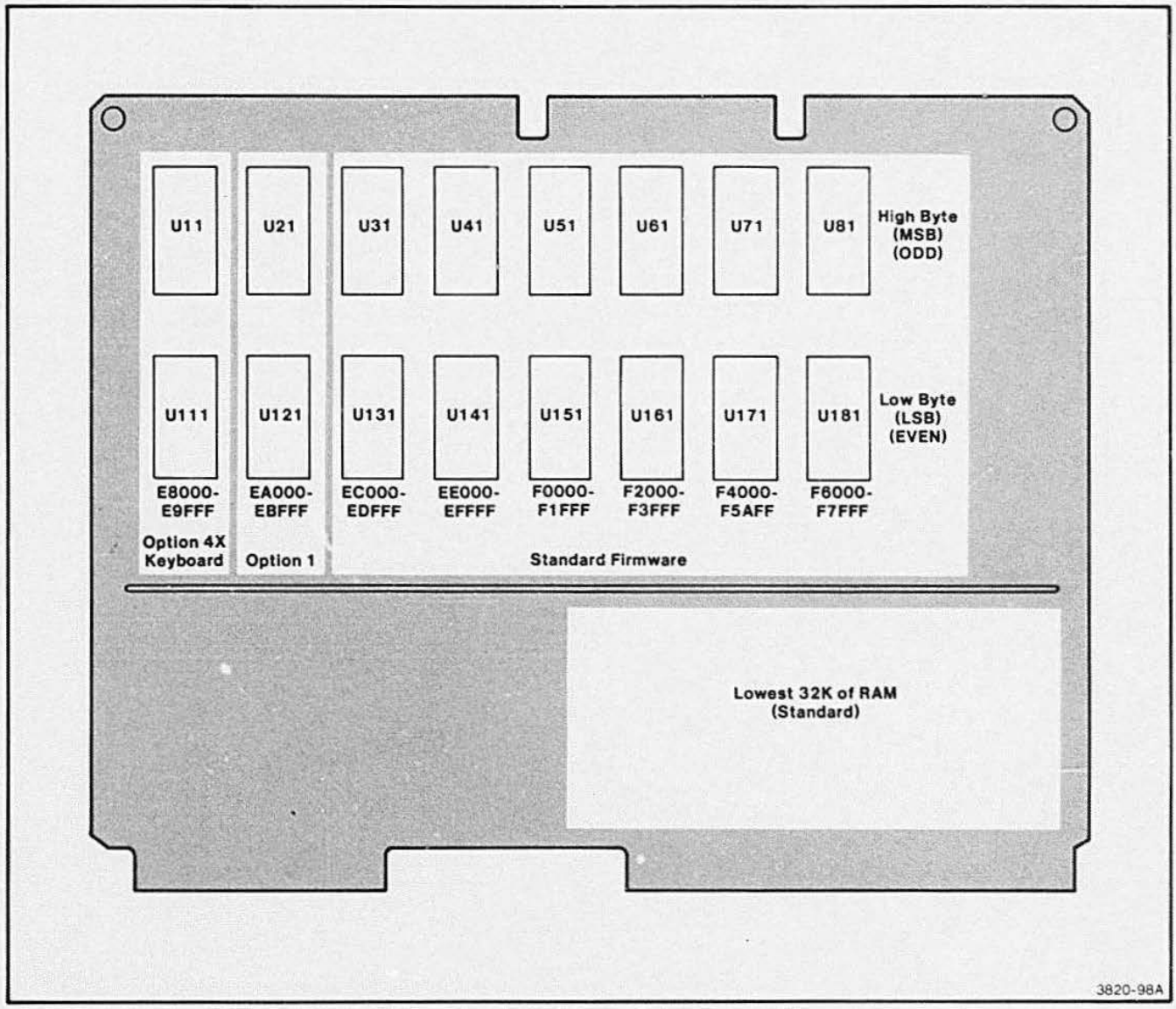


Figure 10-4. RAM/ROM Board ROM Locations.

Table 10-3

KEYBOARD/PROCESSOR BOARD ERRORS

ERROR CODE Binary / Hex		EXPLANATION
1111 1110	FE	Error at beginning of keyboard lights test. (Circling lights test happens here.)
1111 1101	FD	Error at end of keyboard lights test.
1111 1100	FC	Error during keyboard keys test.
1111 1010	FA	Error while loading Keyboard Identification Code. Submessage: (printed on screen) "Keybrd -ID XX" XX is the option number of the keyboard attached (example: a Swedish keyboard is Option 4C). This test then checks the validity of that Option number against the ROM Option number installed, and displays this message if the wrong ROMs or no ROMs (for the option) are present. See Figure 10-4 for the location of the keyboard ROMs. "Keybrd -ID fail" The identifcation test will fail when the 4112 cannot reset the keyboard and read the keyboard option number. This may be caused by a broken or loose connection.

CIRCUITS USED: Look for problems on Keyboard, Keyboard interface on the Processor Board, and keyboard ribbon cable and connectors.

Processor Check (E)

At this time, Self-Test does a more thorough test of Processor board and Keyboard functions. The processor and its related hardware are systematically exercised. Figure 10-5 shows the Processor board ROM locations.

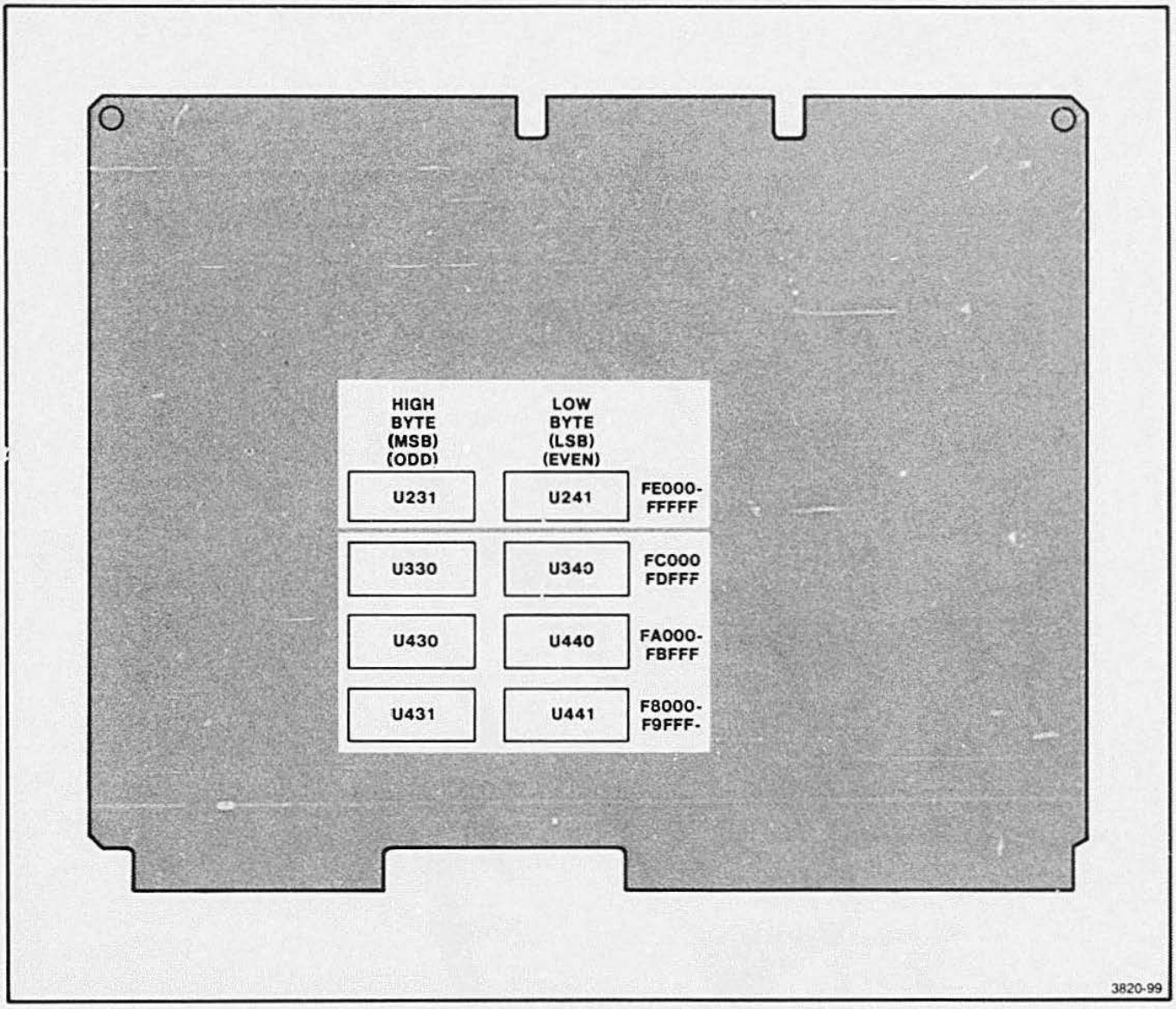


Figure 10-5. Processor Board ROM Locations.

Table 10-4

PROCESSOR BOARD ERRORS

ERROR CODE Binary / Hex		EXPLANATION
1110 1111	EF	Error detected during Timer test.

(a) Submessage: Bell; press RETURN, read light code.

The submessage for the timer test will consist of the following parts: The highest four bits will be one of two codes, the lower four bits will be one of two possible codes. These codes are listed below.

0001 ----	Failed static test; tests timers' outputs for high/low values.
0010 ----	Failed dynamic test; tests timers for correct count vs. processor execution.
---- 0000	Failure in Timer 0 (I/O address 00E1).
---- 0001	Failure in Timer 1 (" " 00E3).

NOTE: Timer 2 cannot be tested at this point. It is checked later during the host port check.

Table 10-4 (cont)

PROCESSOR BOARD ERRORS

ERROR CODE Binary / Hex		EXPLANATION
1110 1110	EE	Failure during timer initialization.
1110 1100	EC	Error during standard ROM checksum test.
(a) Submessage 1:		Bell; press RETURN, read light code.
X X nnnn nnnn		Address of ROM problem in Hex XX000. (i.e., 1111 1110 = FE --> Address where problem found is FE000 'X'. This is first ROM pair on the Processor Board.) See Figure 10-5 for the location of the Processor board ROMs.
(a) Submessage 2:		Bell, press RETURN again, read light code.
This submessage consists of two parts, with the highest four bits consisting of one of three codes, and the lowest four bits of the message consisting of one of three possible codes. These codes are seen below.		
0001 ----		ROM(s) not present.
0010 ----		ROM(s) checksum error.
0011 ----		Standard ROMs position check.
---- 0000		xxxxxxxxxxxxxxxxxxx
---- 0001		Problem isolated to high ROM of pair.
---- 0010		Problem isolated to low ROM of pair.
---- 0011		Problem found in both ROMs of pair.

(a) Submessages are obtained in the following manner: When an error is noted, the bell will ring before each submessage. After noting the error bits (read from the keyboard LEDs), press RETURN, then read the submessage as the next set of lights displayed.

Table 10-4 (cont)

PROCESSOR BOARD ERRORS

ERROR CODE Binary / Hex	EXPLANATION	
1110 1011 EB	Error detected in Interrupt Handler Check	
Submessages: (printed on screen)		
Interrupts-Static Error: XX	Bits that cannot be set in Interrupt Register (I/O base address 00EA).	
Interrupts-Dynamic Address: XX	Level 5 interrupt performed. Failed to reach interrupt vector address: XX + (4 x 5).	(b)
Interrupts-Div by 0 Address: XX	A divide by 0 instruction was performed, but did not vector through location 0. XX equals base interrupt address.	(c)
CIRCUITS USED: Interrupts circuit block on Processor Board.		

(b) Level five is the easiest level of interrupt to force (hence x5). Each time an increment of a level is made, it moves up four bytes in memory (hence the 4). XX equals the base interrupt address.

(c) This message with XX≠00 most likely implies an earlier version of a 8086 processor chip not acceptable for Processor board operation.

NOTE

If either T1 or T2 inputs to the interrupt chip are stuck at a TTL low, Self-Test cannot detect this condition. Also, if an "interrupt level" output (from the interrupt chip) is stuck at a TTL low, Self-Test cannot detect this condition, either. If the interrupt chip seems to be causing a problem, examine the outputs with an oscilloscope, or replace the Processor board.

Communications and Bus Checks (D)

This set of tests examine the operation of the main terminal bus and the host I/O port. This is accomplished by writing to low RAM (located between 0000 and 7FFF) its own address as data. It then reads this address back, using the comparison as a bus check. This assumes RAMs are good.

Table 10-5

RAM/BUS AND HOST PORT ERRORS

ERROR CODE Binary / Hex		EXPLANATION
1101 1111	DF	Problems with low bits of main terminal bus or addressing via this bus.
(a) Submessage 1: Bell, press RETURN, read light code.		
X X nnnn nnnn		XX indicates the base address of the RAM that caused the bus problem: XX000 'X'. (i.e., 00 = 00000 and 20 = 20000.)
(a) Submessage 2: Second Bell, press RETURN, read light code.		
Y Y nnnn nnnn		YY is the Low data byte, showing which bits are in error. If these bits are all ones, address bit zero is likely to be bad.
(a) Submessage 3: Third Bell, press RETURN, read light code.		
Z Z nnnn nnnn		ZZ is the High data byte, showing which bits are in error. If these bits are all ones, byte high enable (BHEN) is probably bad.
		NOTE: If YY and ZZ are all 1s, this indicates a time-out problem while attempting to access a RAM.

(a) Submessages 1 to 3: Bell rings before each submessage; after noting the error bits, press RETURN, read submessages as the next set of lights displayed.

Table 10-5 (cont)

RAM/BUS AND HOST PORT ERRORS

ERROR CODE Binary / Hex		EXPLANTION
1101 1110	DE	Problem with the high bits of the main bus or addressing via this bus. Here it is writing high RAM (between 8000 and highest address) its address as data; then reading it back.
1101 1101	DD	Error detected during host port I/O address check

Submessage: (printed on screen)

"Host Port-Registers
Expect: XX Receive: YY"

This test checks the reset of the USART. Ater resetting USART, it reads the data at status I/O address: E2. It expects to read XX. If instead it receives YY (where XX not = YY) this means the test failed and the USART cannot be reset.

"Host Port-Register
Expect: XX-YY Receive: ZZ-AA

The test checks USART Latch (I/O address EB), and USART Interrupt Request (" " E8).

XX - Latch status expected; is 0 if no bits are in error.

YY - Interrupt Request bits in error; is 0, if no bits are in error.

ZZ - Latch Status bits in error.

AA - Interrupt Request bits in error.

Table 10-5 (cont)

RAM/BUS AND HOST PORT ERRORS

ERROR CODE Binary / Hex		EXPLANATION
1101 1100	DC	Error detected during host port baud rate/ character check

Submessage: (printed on screen)

"Host Port-Baud/Character
Baud: XXXX Expect: YY-AA Receive: ZZ-BB"

XXXX - Baud rate in hex (see Table 10-6).
YY - character sent.
AA - USART data status bits in error; expect 00 (I/O address E4). See Figure 10-6.
ZZ - character received.
BB - USART Data Status bits in error.

CIRCUITS: All RAM locations 0000 to 7FFF and 8000 to top RAM address bus lines connecting Processor and RAM/ROM board.

NOTE

Self-Test cannot check the following signals if they are tied to a TTL low: MWTC; PFAIL; BCLK; INT1; INT2; INT3; INT4; INT6; INT7; BREQ; and BGT.

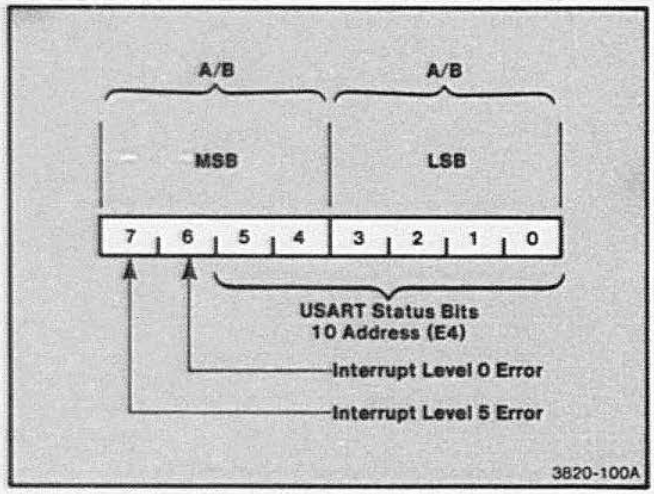


Figure 10-6. Status Byte.

The following table may be used to convert Hex numbers received into decimal numbers.

Table 10-6

HEX-TO-DECIMAL EQUIVALENTS

Hex Number	Decimal Number
12C	300
258	600
4B0	1200
708	1800
7D0	2000
960	2400
E10	3600
12C0	4800
1C20	7200
2580	9600
4B00	19200
9600	38400

Memory Tests

ROM Check (C). This set of tests examines the operation of all ROMs on the RAM/ROM board and all option ROMs. The ROMs on the Processor board were tested along with the processor in previous tests. For the locations of the bad ROMs on the RAM/ROM board, refer back to Figure 10-4.

Table 10-7

SYSTEM/OPTION ROM ERRORS

ERROR CODE Binary / Hex	EXPLANATION
1100 1111 CF	Failure during ROM Map generation.
1100 1110 CE	Error found during ROM checksums test.
Submessages:	Error messages are same as for main ROMs; see Table 10-4.
1100 1101 CD	ROMs found in wrong position (options only).
Submessages: (Displayed on screen) "ROM-Position Address: XXXX Expect: YY-ZZ Receive: AA-BB" ROM Set: CC-Fail	Address XXXX -- the base address of the ROM pair being checked. See NOTE 1, below. Expect YY-ZZ -- 1) YY is the ROM Set number (same as option number. 2) ZZ indicates even or odd ROM of pair. (If ZZ is odd, then odd ROM is problem; if ZZ is even, then even ROM is problem). Receive AA-BB -- found ROM Set number AA (instead of YY); BB (like ZZ) indicates odd vs. even of pair. ROM Set CC-Fail -- CC is option (ROM Set) number of ROM that failed.

NOTE 1: If FFFF, then Self-Test could not find the ROM pair indicated by "Expect: YY-ZZ".

Table 10-7 (cont)

SYSTEM/OPTION ROM ERRORS

ERROR CODE Binary / Hex		EXPLANATION
1100 1101	CD	(cont) ROMs in wrong position. Example> Address: 1600 Expect: 42-17 Receive: 42-15 ROM Set: 42-Fail Means -- that the base address of the ROM pair being checked is 16,000. 42 is the ROM set number expected (disk). 17 is base address + 1 (odd ROM of pair). If 16 is base address + 0 (even ROM " "). The test found 42-15 at the address; 42 was the ROM Set, and 15 means the odd ROM for location 14,900 was found there (instead of odd ROM for 16,000).
1100 1100	CC	ROM version compatibility problem Submessage: (printed on screen) "ROM-Version ROM Set: XX-VV Expect: YY-ZZ Receive: AA-BB ROM Set: CC-Fail" ROM Set used for reference is XX (see NOTE 2), and its version number is VV. "Expect YY-ZZ" refers to the expected ROM option name YY, and version number ZZ for for the ROM Set being checked. "Receive AA-BB" reports the actual ROM name (AA) and version (BB) in same socket. Example> ROM Set: 00-05 Expect: 42-03 Receive: 42-01 Means -- The main system firmware (called 00) is version 5. It expects Option 42 ROMs with version 3 or higher to be installed. Instead, it finds Option 42 ROMs, with only version 1 firmware, installed. ROM Set: CC-Fail ROM failure -- CC is number of Option where version problem appeared. This ROM set is mapped out of the option.

CIRCUITS USED: RAM/ROM Board ROMs and circuits, and ROMs on option boards.

NOTE 2: XX is option number.. System ROMs number is always 00.

RAM Check (B). This series of tests performs a systematic check of all system RAMs. Each set of tests are grouped, and each such group uses the same type of error reporting scheme (light codes). Refer back to Figure 10-4, which shows the physical location of the lowest 32K of RAM.

In the following tests, the RAM Memory Delay Check (BB) generates a light code which may remain lit for as much as 14 seconds while the test is running. This does not indicate an error. An error is indicated by a bell accompanied by a light code which stays on indefinitely. You may override the lengthy Delay Memory Check by entering CONTROL D during the keyboard check.

NOTE

In the following table, "Lowest 32K RAM" refers to the RAM from hexadecimal address 0000 to 7FFF, or the standard RAM of the 4112. "Upper RAM" refers to any extended RAM options installed in the 4112, starting at hexadecimal address 8000.

Table 10-8

RAM TEST ERRORS

ERROR CODE Binary / Hex	EXPLANATION
1011 1111 BF	Lowest 32K of RAM, walking ones check. (Here each bit is set and tested, in order from left to right, hence the "walking ones" term." This light code is accompanied by one of the following light code submessages.
(a) Submessage 1: Bell rings, press RETURN, read light code.	
X X nnnn nnnn	XX indicates the address of the RAM problem at XX000 'X'.
(a) Submessage 2: Second bell, press RETURN, read light code.	
Y Y nnnn nnnn	YY is the Low Data byte, showing which bits are in error.
(a) Submessage 3: Third bell, press RETURN, read light code.	
Z Z nnnn nnnn	ZZ is the High Data byte, showing which bits are in error.

Table 10-8 (cont)

RAM TEST ERRORS

ERROR CODE Binary / Hex			EXPLANATION
1011 1110	BE ------	(b)	Error in "walking zeroes check;" lowest 32K RAM.
1011 1101	BD ------	(b)	Error in "all ones check;" lowest 32K RAM.
1011 1100	BC ------	(b)	Error in "init (zero check);" lowest 32K RAM..
1011 1011	BB ------	(b)	Error in "RAM memory delay check." During the RAM memory delay check, data is held for 14 seconds and then rechecked. The light code will remain lit for this time.
1011 1010	BA ------		"RAM Memory Map Generation" error. This test checks for RAM and the absence of RAM and generates a corresponding memory map.
1011 1001	B9 ------	(b)	Error in "walking ones check;" upper RAM.
1011 1000	B8 ------	(b)	Error in "walking zeroes check;" upper RAM.
1011 0111	B7 ------	(b)	Error in "ail ones check;" upper RAM.
1011 0110	B6 ------	(b)	Error in "init (zero check);" upper RAM.
1011 0101	B5 ------		Error during RAM stack building.
1011 0100	B4 ------		Error in operating system vector table (lowest 32K of RAM)

(a) Submessages are obtained in the following manner: when an error is noted, the bell will ring. After noting the error bits (read from the Keyboard LEDs), press RETURN, then read the submessage as the next set of lights displayed.

(b) If one of these messages is displayed as an error (the bell rings), the three submessages earlier in the table will have to be read in order to locate the problem.

CMOS Check (AF). When a CMOS memory error is detected, the LEDs will show the "AF" pattern (1010 1111), and a message is written on the display screen. The only time a full CMOS check is performed is during the adjustment procedure. See Processor board menu.

NOTE

The following CMOS error messages report a change in default parameters. This may be caused by either changing EPROMs, or by a CMOS battery/circuit failure.

Table 10-9

CMOS MEMORY ERRORS

ERROR CODE Binary / Hex	EXPLANATION
1010 1111 AF	CMOS check
Submessage: (printed on screen)	
"Cmos-Error I/O Address: XXXX Expect: YY41 Receive: ZZZZ	XXXX = Address of problem. If it is addressing correctly, the address will read FFFE. YY41 = YY is the system version number (taken from EPROM) and 41 indicates 4110 series product. ZZZZ = this is what is actually read, instead of YY41.
"Cmos-Checksum"	Checksum error detected.
"Setup Default-Reset"	CMOS parameters have been updated. This is the same as the Power-up message.

Display Bus Checks (8)

The Self-Test program tests the three principle circuit boards in the Display Bus: Vector Generator, Raster Memory, and Display Controller. This set of tests does not exercise or check the Display Module.

Table 10-10

DISPLAY BUS/BOARD AND SYSTEM ERRORS

ERROR CODE Binary / Hex	EXPLANATION
1000 1111 8F	4112 Video Controller tests:
(a) Submessage: Bell, press RETURN, read light code.	
0000 0001	Bad vertical interrupt.
0000 0010	Video Controller not present.
0000 0011	No vertical interval interrupt.
0000 0100	Vertical interval too short.
0000 0101	Vertical interval too long.
0000 0110	Vector Generator ready, but interrupt never flagged.
0001 0001	Vector Generator problem.
1000 1110 8E	4112 Raster Memory tests:
(a) Submessage: Bell, press RETURN, read light code.	
0000 0001	Raster Memory fault.
0000 0010	No RND flag, test hung.
0001 0001	Vector Generator problem.
1010 ----	Standard plane (2) errors check, and option plane presence check.
---- 0000	Status I/O port error.
---- 0001	Non-memory error on plane. (Example: Addressable Latch.)
---- 0010	Dual Plane Status I/O Port errors.
1001 ----	Error detected on Memory Plane 1. (b)
1000 ----	Error detected on Memory Plane 0. (b)
---- 0000	Status I/O Port error.
---- 0001	Non-memory error on this plane.

(a) See end of Table 10-10 (next page). (continued)
(b) Error is on optional Dual Plane memory board.

Table 10-10 (cont)

DISPLAY BUS/BOARD AND SYSTEM ERRORS

ERROR CODE Binary / Hex		EXPLANATION
1000 1101	8D	4112 Vector Generator tests:
(a) Submessage: Bell, press RETURN, read light code.		
0000 0001		Bad Vector Generator register.
0001 0001		Vector Generator board not working.
1000 1100	8C	Raster Memory Addressing Tests:
(a) Submessage: Bell, press RETURN, read light code.		
0000 0001		Raster Memory Address Fault
1000 1100	8C	Raster Memory Addressing Tests:
(a) Submessage: Bell, press RETURN, read light code.		
0000 0001		Raster Memory Address Fault
0001 0001		Vector Generator board not working.

CIRCUITS: Replace Video Controller, Vector Generator, or Raster Memory boards, as indicated above. Check bus and cable connections first.

(a) Submessages are obtained in the following manner: When an error is noted, the bell will ring. After noting the error bits (read from the keyboard LEDs), press RETURN, and read the submessage from the next set of lights displayed.

SYSTEM LEVEL ERRORS (7X)

These error messages prompt the user whenever the specified problem occurs. These error codes may appear at any time: NOT just during Self-Test. When such an error message appears, run Self-Test to locate any defective circuitry that may be involved. Most of these errors involve improper use of the terminal and are referred to as "system level" errors, rather than hardware errors.

Table 10-11

SYSTEM LEVEL ERRORS (7x Codes)

ERROR CODE Binary - Hex	EXPLANATION
0111 1111 7F	CMOS memory lacking Could not get enough memory for system initialization. Try resetting CMOS parameters.
0111 111 7E	No monitor level procedure. A monitor procedure was called from an interrupt service routine (ISR). This error should only happen when a file is downloaded containing software ISRs.
0111 1101 7D	System data structures scrambled-RAM data lost. Try resetting the terminal or checking any routines created in the terminal or loaded into the terminal that may be writing into the wrong area.

Table 10-11 (cont)

SYSTEM LEVEL ERRORS (7x Codes)

ERROR CODE Binary - Hex	EXPLANATION
0111 1100 7C	Unexpected or illegal interrupt. If this error code is generated, it is suggested that Self-Test be run to pinpoint the interrupt failure area. Note: could spurious interrupt have been generated by operator?
0111 1011 7B	Error Handler could not set dynamic memory for an error message. Check the user allocation of RAM through the STA MEM (status memory) command for available memory.

4112 OPTION TESTS AND ERROR MESSAGES

Self-Test also checks three options that can be installed in the 4112. Option 42 (disk drive) requires a Disk Controller board. This circuit board contains ROMs that allow it to test itself when Self-Test is run. Likewise, the 3PPI board and Tablet Interface board (Options 10 and 13/14 respectively) also contain ROMs that allow these circuit boards to test themselves during Self-Test. Options 24 through 29 (extended RAM options) are also checked during Self-Test, but by the normal firmware, and not by firmware in ROMs on the optional RAM boards. RAM in addresses above the standard 32K bytes is called "Upper RAM" in the RAM test description (located earlier in this section).

Error messages for the 3PPI board, Disk Controller board, and Tablet Interface board are the same for both the 4114 and 4112 terminals, since these boards fit in both terminals.

3PPI Board Tests

These error codes may appear while running Self-Test, only if the 3PPI Option is installed and the host port cables are in use. For a 3PPI cable testing procedure, go to the "3PPI Adjustment Menu/Procedure" at the end of this section.

Table 10-12
3PPI ERRORS

ERROR CODE Binary / Hex	EXPLANATION
0110 1111 6F	Error detected during Register check. Submessage:(printed on screen) I/O Address: FBnn Expect WW-XX Receive: YY-ZZ Explanation: The information reported by this error code is interpreted as follows: nn = register in error WW = expected data YY = actual data ZZ = actual interrupt

Table 10-12 (cont)

3PPI ERRORS

ERROR CODE Binary	/ Hex	EXPLANATION
0110	1110 6E	Error detected during 3PPI Character check.

Submessage (printed on screen):

3PPI Baud/Character
Baud: nnnn Expect: WW-XX
Receive: YY-ZZ

Explanation: nnnn = Baud rate (Hex). WW, XX, YY, ZZ are explained under the 6F error message.

The following error messages may also appear on the screen.

3PPI Baud/Character Baud: nnnn Expect:00-02 Receive:00-FF	This means that no character data is received.
3PPI Baud/Character Baud: nnnn Expect: FF-00 Receive: nn-00	This means that there is a data transmission error where nn was was the character sent.

The Character check test uses internal loop-back testing. There is no interaction between this test and external equipment. The equipment operates at either the preset system rate or 1200 baud, whichever is higher.

NOTE

Refer to Table 10-6 earlier in this section when converting the displayed hexadecimal numbers into decimal numbers.

Option 42 Self-Test Error Messages

Start the program running in the same manner as for normal Self-Test. (Press the SELF TEST and MASTER RESET keys in the proper succession.)

NOTE

Do NOT insert or remove a disk while Self-Test is running as this will generate false interrupts.

Table 10-13

DISK OPTION ERRORS

ERROR CODE Binary / Hex	EXPLANATION
0101 1111 5F	Board Status Register Check

This test validates the operation of the hardware comprising the Board Status Register (at X'FC00'). Each Read/Write bit in the register is set (set=0) and tested; it is again reset and tested.

Submessage: (printed on screen)

"Disk - Board Status Register"	These tests check each bit in the BSR (Board Status Register).
(a) "Disk - ADR19-1 not = 0"	Wrote a 0 to ADR19 (D3 of FC01) and read back a 1.
(a) "Disk - ADR19-1 not = 1"	Wrote a 1 to ADR19, but read back a 0
(a) "Disk - ADR19-1 not reset, =1"	Wrote a 0 to reset ADR19, but read a 1.
"Disk - INTE-0 not working"	Did not read back what was written at D6.
"Disk - BUSW-0 not working"	Did not read back what was written at D5.
"Disk - HDL3-0 not working"	Did not read back what was written at D3.

(a) These submessages check the ADR19 Address Counter.

Table 10-13 (cont)
DISK OPTION ERRORS

ERROR CODE Binary / Hex	EXPLANATION
"Disk - HDL2-0 not working"	Did not read back what was written at D2.
"Disk - HDL1-0 not working"	Did not read back what was written at D1.
"Disk - HDL0-0 not working"	Did not read back what was written at D0.

Circuits used: Address Decode, Input Data Buffer, and Board Status Register.

0101 1110 5E — Initialize and check Disk Controller

The FDC is put into its command phase (regardless of its present state) via a series of command reads and writes. The following bits are tested for correct state:

Under X'FC00' -- D7 (EOC-1)
Under X'FC08' -- D7 (RQM-1) and D6 (DIO-1).

A SPECIFY command is then issued by the processor.

Submessages: (printed on screen)

"Disk - Controller Protocol"	
"EOC-0 is 0 after init"	FDC generates an unexpected interrupt, bit is in wrong state after initialization.
"Disk - DIO-1 is 0 - Write required"	FDC required a write to it, while processor expects to read from it.

Table 10-13 (cont)

DISK OPTION ERRORS

ERROR CODE Binary / Hex	EXPLANATION
"Disk - DIO-1 is 1 - Read required"	FDC requires a read from it, but processor expects to write to it.
"Disk - DIO-1 is 1 after init"	Bit D6 is in wrong state after initialization.
"Disk - RQM-1 remains 0"	FDC never sends RQM-1 (fails in 1000 tries).
"Disk - Cannot restore Protocol"	Runs initialization sequence, but cannot put FDC into a known state. (Processor has no idea what FDC is doing).

Circuits used: FDC, Board Status, Control Strobes, Data MUX, and Address Decode.

0101 1101 5D — Drive present check

The processor issues a SENSE DRIVE 0 STATUS (SDS) command. Drive 0 should be present. The D7 (RQM-1) and D6 (DIO-1) are tested for correct states before and during the command.

Submessage: (printed on screen)

"Disk- F0: not present"	Drive 0 should always be present. This message means the FDC or Disk Drive control cannot find drive unit 0.

Circuits used: FDC's disk control I/F, and Disk Drive Control circuits.

Table 10-13 (cont)
DISK OPTION ERRORS

ERROR CODE Binary / Hex	EXPLANATION
0101 1100 5C	Intersystem Interrupt check

The following procedure is used to generate an interrupt: The heads are unloaded (should already be unloaded from last test), and the processor issues a RECAL DRIVE 0 command. Recal is executed, but the head does not move. The FDC does not know that the heads were unloaded, so it generates an interrupt. An error is also reported, unless head was already at Track 0.

The processor then issues the SENSE INTERRUPT STATUS (SIS) command to read the results of the RECAL command. The results of the SIS command are checked as well as RQM-1 and DIO-1.

Submessages: (printed on screen)

"Disk - Intersystem Interrupt Check"	
"Disk -Bad FC00 init"	Board Status Register contains error (different state than expected).
"Disk -Bad FC08 init"	FDC status register contains an error (different state than expected).
"Disk -Bad FC00 RECAL-1 status"	Error in Board Status Register (BSR) after first byte of RECAL command written.
"Disk -Bad FC08 RECAL-1 status"	Error in FDC after first RECAL byte written.
"Disk -Bad FC00 RECAL-2 status"	Error in BSR after second RECAL byte written.
"Disk -Bad FC08 RECAL-2 status"	Error in FDC after second RECAL byte written.
"Disk -Level 7 interrupt not present"	Expected interrupt not present.

Table 10-13 (cont)

DISK OPTION ERRORS

ERROR CODE Binary / Hex	EXPLANATION
"Disk -Bad FC00 SIS status"	Error in BSR after Sense Interrupt status byte written.
"Disk -Bad FC08 SIS status"	Error in FDC after Sense Interrupt status byte written.
"Disk -ST0 data error"	Error in ST0, read at FDC.
"Disk -Bad FC00 ST0 status"	Error in BSR after ST0 status byte read.
"Disk -Bad FC08 ST0 status"	Error in FDC after STO status byte read.
"Disk -Track error"	Error in track number (PCN), read at FDC.
"Disk -Bad FC00 Track status"	Error in BSR after track number read.
"Disk -Bad FC08 Track status"	Error in FDC after track number read.
"Disk -Level 7 interrupt still present"	Interrupt still present.
Circuits used: Address Decode, Board Status, Control Strobes, Data MUX, and FDC.	

Table 10-13 (cont)
DISK OPTION ERRORS

ERROR CODE Binary / Hex	EXPLANATION
0101 1011 5B	DMA Operation check
Submessage: (printed on screen)	
"Disk - DMA transfer failed"	Data ('80') not found at current DMA address (RAM only).
Circuits: DMA State Machine, Data MUX, Control Strobes, Address Decode, Address Counters, Input Data Buffers, and Board Status blocks.	
0101 1010 5A	DMA addressing check
Both this test and the previous test must be completed before the DMA State Machine and the DMA Address Counters are fully tested; the testing of one requires the operation of the other.	
The DMA Address Counters are write only. The only way to look at these counters is to examine the most significant bit (MSB), which is at D4 of the Board Status Register (X'FC00').	
The twenty bit counters are subdivided into three groups: High Nibble (FC01), Middle Byte (FC02), and Low Byte (FC03). Each group is tested individually in the following manner.	

Table 10-13 (cont)
DISK OPTION ERRORS

ERROR CODE Binary / Hex	EXPLANATION

-- HIGH NIBBLE TEST --

Test high nibble first because all bits must ripple through the high nibble while testing the middle and low bytes.

STEP SET-UP
1. Load High Nibble with 0.
2. Does D4 = 0 ? See NOTE.

TEST
3. Load Middle Byte and Low Byte with X'FF.'
4. Step DMA.
5. Does D4 = 0 ?

TEST
6. Repeat steps 3 through 5 eight times.
7. On eighth time, does D4 = 1 ?
8. Repeat another eight times. (D4 should = 1 for these eight.)
9. On sixteenth time, does D4 = 0 ?

NOTE: If D equals 1, an error message is reported. All "D=N?" steps will cause an error unless the number is as expected. Error messages are in the accompanying tables.

DMA Address Check (continued)

-- MIDDLE BYTE TEST --

STEP SET-UP
10. Load High Nibble with 7.
11. Does D4 = 0 ?
12. Load Middle Byte X'FF.'

TEST
13. Load Low Byte with X'FF.'
14. Step DMA.
15. Does D4 = 0 ?
16. Reload Low Byte witX'FF' (leave Middle Byte since we are testing it).
17. Repeat steps 13 through 15; on 256th does D4 = 1? (Does High Nibble equal eight?).

Circuits used: FDC, Board Status, Control Strobes, Data MUX, and Address Decode.

Table 10-13 (cont)

DISK OPTION ERRORS

ERROR CODE Binary / Hex	EXPLANATION
	SET-UP
18.	Reload High Nibble with F.
19.	Does D4 = 1 ?
	TEST
20.	Reload Low Byte with X'FF,' and Step DMA.
21.	Repeat step 19 twohundred fiftysix times.
22.	On 256th time does D4 = 0 ? (High Nibble = 0)

-- LOW BYTE TEST --

Same procedure as Middle Byte test except the Low Byte and Middle Byte are reversed.

Error Messages for DMA Address Counters

Submessages (printed on screen):

"Disk - DMA Address Counters
- ADR19-1 Error

"Early 0-1 @ FC01"	Error detected at steps 2 or 5 (Counter reached 8 too soon)
"No 0-1 @ FC01"	Error detected at step 7.
"Early 1-0 @ FC01"	Error detected at step 8.
"No 1-0 @ FC01"	Error detected at step 9.
"Early 0-1 @ FC02"	Error detected at steps 11 or 15.
"No 0-1 @ FC02"	Error detected at step 17.
"Early 1-0 @ FC02"	Error detected at step 19.
"No 1-0 @ FC02"	Error detected at step 22.
"Early 0-1 @ FC03"	Same explanation as for FC02 messages, above, except substitute FC03 for FC02 in explanation of Middle Byte tests.
"No 0-1 @ FC03"	
"Early 1-0 @ FC03"	
"No 1-0 @ FC03"	

These tests check the clocking and carries of one counter to the next.

Circuits used: Same circuit blocks as used in DMA Operation Check, except Data MUX not used.

Tablet Self-Test Error Codes

The light codes for the tablet indicate the tablet failed to complete a Self-Test sequence. In this case, the operation of the Tablet Controller board should be investigated.

During the tablet test, error messages are printed on the terminal screen for each test that failed. These submessages are accompanied by one of the light codes listed in Table 10-14.

A "soft error" will allow the tablet to be used. However, it tells the operator that a problem exists.

A "fatal error" removes the tablet from the interrupt routine of the terminal. The tablet can not be used until the problem is corrected and the error is cleared.

Table 10-14

TABLET ERROR MESSAGES

ERROR CODE Binary / Hex	EXPLANATION
0100 1111 4F	Board Communications check error.
Submessage: (printed on screen)	
"Tablet -Board I/O Timeout"	
	May appear during either the Power-Up sequence or Self-Test. It indicates that the terminal firmware is unable to communicate with the Tablet Controller board, and that a processor timeout occurred wheen communication was attempted. This is a FATAL error.
0100 1110 4E	Data Register bit check error.
Submessage: (printed on screen)"	
"Tablet -Data Register Bit Error"	
	Each individual bit of the data register is tested for set and reset. Message indicates at least one bit is not acting properly. This is a SOFT error.

Table 10-14 (cont)

TABLET ERROR MESSAGES

ERROR CODE Binary / Hex	EXPLANATION
0100 1101 4D	Data Register count check error

Submessage: (printed on screen) - Only one of the following submessages will accompany the light code:

"Tablet -Data Register Counting Error (Low)"

Indicates that the data register was incapable of counting from 0 to 31 by one. This is a SOFT error.

"Tablet -Data Register Counting Error (High)"

Indicates that the data register was incapable of counting from 0 to 65539 by 29. This is a SOFT error.

0100 1100 4C	Digitization check error.

Submessage: (printed on screen) - Only one of the following submessages will accompany the light code:

"Tablet -Digitization Timeout Error"

A start digitization command was given to the tablet and one of the FIRE pulses was not returned within 0.5 seconds. This is a SOFT error.

"Tablet -Digitization Firing Sequence Error"

The status bits, indicating which data firing (X1, X2, Y1, Y2) is present, were out of sequence. This is a SOFT error.

Table 10-14 (cont)

TABLET ERROR MESSAGES

ERROR CODE Binary / Hex	EXPLANATION
"Tablet -Erroneous Interrupting Indication"	The tablet status indicates that it is trying to interrupt the processor when it should not. This is a SOFT error.
"Tablet -failed To Interrupt"	Indicates the tablet status is not trying to interrupt the processor when it should. This is a SOFT error.
"Tablet -Data Register Counting Error (Digitization)"	The data register failed to count at all during a start digitization. This is a SOFT error.

ADJUSTMENT SELF-TEST

Adjustment Self-Test is the third diagnostic program that can be used to check the terminal. Adjustment Self-Test is started in the same manner as the main Self-Test (the second part of the functional check). A procedure and some guidelines for Adjustment Self-Test are outlined as follows:

1. Start Adjustment Self-Test running by pressing and holding the SELF TEST and MASTER RESET buttons.

2. Release the MASTER RESET button, first.

3. After the keyboard lights begin to "cycle," then release the SELF TEST button.

4. The keyboard LEDs will all turn on, and then off, and then cycle twice. This is the same as during main Self-Test.

5. After the keyboard lights finish "cycling," the keyboard bell will ring once. Then press the CTRL and C keys at the same time.

6. After CONTROL C has been pressed, the terminal will pause for a few seconds and then display a general menu on the screen. The terminal is now in the Adjustment part of Self-Test.

7. The general menu tells which key to press to check any specified part of the terminal. These keys are always one of the eight "function keys" across the upper-left part of the keyboard.

8. When one of these keys (designated by the menu) is pressed, a second menu (submenu) will be displayed.

Table 10-15

ADJUSTMENT CONTROL KEYS

Key	Action
CONTROL C	Displays (returns to) the general Self-Test menu.
CONTROL D	Displays the current menu.
CONTROL E	Exits from the current routine.
SPACE BAR	Repeats the current pattern/test.
Shifted Keys	A second function for specified key. The letters "Sh" in front of the key designation on the menu, means press the SHIFT key along with the designated key.

THE GENERAL MENU

The General Menu appears on the screen immediately after entering the Adjustment part of Self-Test. This general menu is common for all 4110 series terminals. An example of the general menu is shown below.

```
411X Menu
--
f1 4112 Display
f2 Processor Board
f3 Disk
f4 3PPI
f5 Tablet
--
Selection
*
```

The Disk, 3PPI, and Tablet functions only appear if that option is installed. The options may change key designations depending on which options are installed. For instance, if no disk options were installed, but the tablet and 3PPI options were, the 3PPI option would be selected by F3, and the tablet options would be selected by F4. Adjustment Self-Test for the tablet is used only in adjusting the tablet when Options 13 or 14 are installed. It is not used in this function check procedure.

During Adjustment Self-Test, pressing CONTROL C will always cause this menu to be printed on the screen.

4112 DISPLAY ADJUSTMENT MENU

After the general menu is obtained, select the display menu by pressing F1. This key is in the upper-left corner of the keyboard. After the 4112 Display Menu is selected, the following will appear on the screen:

```
4112 Display Menu
--
f1 Grid
f2 Gray Scale
f3 White Screen
f4 Dot Pattern
--
Selection
*
```

These patterns can be used during the functional check to ensure that all display parameters are functioning properly.

1. Press function key, F3 —
   Observe a uniform white screen. Adjust the Intensity Control, as needed, to obtain a bright (white) screen. This control is located next to the upper-right corner of the display screen, above the optional disk drive unit. (This pattern is used later to calibrate the internal brightness adjustment.)

2. Press function key, F1 —
   Observe grid pattern, and verify that it is properly positioned (centered) on the screen.

3. Press function key, F2 —
   Observe in this pattern eight distinct levels of gray (from black to and including white).

4. Press function key, F4 —
   Observe full screen dot pattern. All dots must be visible as uniform dots. Verify uniform focus over the entire screen.

5. Press CTRL C to return to the General Menu.

PROCESSOR BOARD ADJUSTMENT MENU/PROCEDURE

With the General Menu displayed on the screen, select the Processor Board menu by pressing F2. After F2 is pressed, the Processor Board menu is displayed. The Processor Board menu looks like this:

```
Processor Board Menu
--
f1 CMOS-Reset
f2 Keyboard
f3 Host Port
--
Selection
*
```

Working from the Processor Board menu, perform the following tests.

CMOS-Reset, Function Key F1.

CMOS-Reset is used to restore the factory default settings of all the CMOS parameters. From the Processor Board menu, press F1 function key. This action prints the following message on the display:

```
*f1
CMOS-Reset
Selection
*
```

This message means that the terminal's operating parameters have been restored to their factory default settings.

Keyboard, Function Key F2.

Pressing the F2 key causes every key on the keyboard to display two 2-digit hexadecimal numbers. These numbers represent the 8-bit codes that the Processor Board generates for each downstroke and upstroke of a key. Each key has its own distinct hexadecimal code, and each down-stroke code is different than the corresponding up-stroke code. The first number of the up-stroke code is always eight more than the first number of the down-stroke code. The second character in the code is the same for both the down-stroke and the up-stroke of the key. This routine will verify that each key is operating properly. Figure 8-1 (Functional Check and Performance Check Procedures) shows the keyboard key codes.

Now return to the Processor Board menu by pressing CTRL D.

Host Port Check, Function Key F3.

The Host Port routine checks the validity of the output port of the terminal. Enter the Host Port routine by pressing F3. Once this is done, the screen displays the following message:

```
Host Port
Attach Loopback
Press SpcBar
```

Connect the special loopback connector from the output port back to the input port. These connections are located on the rear panel of the terminal. See Accessories List for the Loopback Connector part number.

After the cable is connected, press the SPACE BAR. This starts the routine that sends signals representing characters 7F through 00 (at baud rates 9600 through 300). When this string of signals is sent and received properly, the screen indicates it by printing "Complete." This message means the terminal is ready to go on to the next test.

If there is an error during the Host Port routine, the following submessage will appear on the screen:

```
"Host Port-Baud/Character
Baud: XXXX Expect: YY-AA Receive: ZZ-BB"
```

This means:

XXXX	is the baud rate in hexadecimal.
YY	is the signal sent (for example: 7F).
AA	are the expected bits in error, this should always read 00.
ZZ	is the signal received.
BB	are the bits in error.

After this Host Port check is complete, return to the general menu by pressing CONTROL C. If there are no options installed, this completes the functional check of the terminal. If there are options installed, select each option listed in the general menu and perform the following checks for that option.

NOTE

Only the disk and 3PPI options may be functionally checked using Adjustment Self-Test. The tablet menu is used for alignment purposes of the Graphic Tablet only (which is external to the terminal). The electronics for the tablet that reside in the terminal (Tablet Controller Board) were checked during main Self-Test. An alignment procedure for the graphic tablet using Adjustment Self-Test is contained in the 4110 Series F13/14 Graphic Tablet Instruction Manual.

DISK OPTION ADJUSTMENT MENU/PROCEDURE

The Disk Menu may be obtained from the general menu by pressing F3. The Disk Menu is an optional menu and will only appear if Option 42 is installed. As Self-Test checks the circuitry on the Disk Controller board, this routine checks the drive unit, also. This menu is useful for drive unit head alignment. For this purpose a special alignment diskette (not used in this functional check) is required.

NOTE

The following is only a functional check and not an alignment procedure. This check only ensures that no error messages are received and that the drive unit is functioning. An alignment procedure for the disk drives is located in the "4110 Series F42/43 Disk Options Service Manual," and the "Flexible Disk Drive Instruction Manual."

This is an example of the Disk Menu (items are self explanatory):

```
Disk Menu
--
f1 No Operation
f2 Step Up One Track
f3 Step Down One Track
f4 Seek Track 0
f5 Seek Track 1
f6 Seek Track 38
f7 Seek Track 75
f8 Seek Track 76
Sh f1 Load Head
Sh f2 Unload Head
Sh f3 Arms Write Mode
Sh f4 Writes Track 76 With a 2F Pattern
Sh f5 Select Your Own Track
Sh f6 Change Device (Drive Unit) Address
Sh f7 Auto Load And Unload The Head On
      Track 0
--
Selection
*
```

With the disk option installed, properly insert a disk in the drive unit before starting this test. Then make sure the WRITE PROTECT switch is set to the off position (the light is not lit).

CAUTION

It is best to perform this part of the functional check using a disk free of data. Performing this test may cause some data to be written on the disk. With the write protect switch off, it is possible to write over existing data. Therefore, it is best to use a new disk or one that contains unwanted data.

Press each of the disk menu keys in succession. No error messages should be received on any of the tests, and the head should move to the selected area on the disk. After running through the head movements (in the menu), press CTRL C to return to the general menu.

NOTE

This is merely a check of the disk drive unit to ensure that no error messages are received and that the drive unit is operational. For a full alignment procedure of the drive unit, see the "4110 Series F42/43 Disk Options Service Manual."

3PPI ADJUSTMENT MENU/PROCEDURE

The key designations, to select the 3PPI option from the general menu, will depend on the options installed. If no disk or tablet options are installed, the F3 key selects the 3PPI Menu from the general menu. An example of this menu follows:

```
3PPI Menu
--
f1 3PPI Ports
--
Selection
*
```

This routine is designed to check the cables to the designated peripheral port. To start this test, press F1. The following message will appear on the screen:

```
*f1
Select Port (0, 1 or 2)
*
Attach Host Port Cable to Selected
        3PPI Port and Press Spacebar
*
```

Connect the terminal host-port RS-232C cable to the 3PPI-port to be tested. Connect the other end of the cable to the terminal's MODEM connection. Then type the number of the port to be tested (0, 1, or 2) followed by pressing SPACEBAR.

If there are no errors, the following message will appear on the screen; then the next port may be tested. If an error occurs, consult the 3PPI errors description in Table 10-12.

```
Test in Progress
Procedure Complete
Select Port (0, 1, or 2)
*
```

This completes the 3PPI "Adjustment" procedure and messages.

TABLET ADJUSTMENT MENU/PROCEDURE

When the Tablet is selected from the general menu (part of Ajustment Self-Test), the following tablet message will appear on the screen:

```
Tablet Menu
--
f1 Tablet Timing Adjustment
--
Selection
*
```

At this time, the interconnect cable must be connected between the Graphic Tablet and the 4112 graphic tablet port. After this is done, the F1 key may be pressed.

The following submessages can be used to aid in adjusting the surface accuracy of the tablet. For more information on tablet adjustments, consult the Option F13/14 Graphics Tablet Instruction Manual. These submessages appear while running the Adjustment part of Self-Test only.

Submessages: (printed on screen)

Warning: - Tablet Firing Sequence Error -

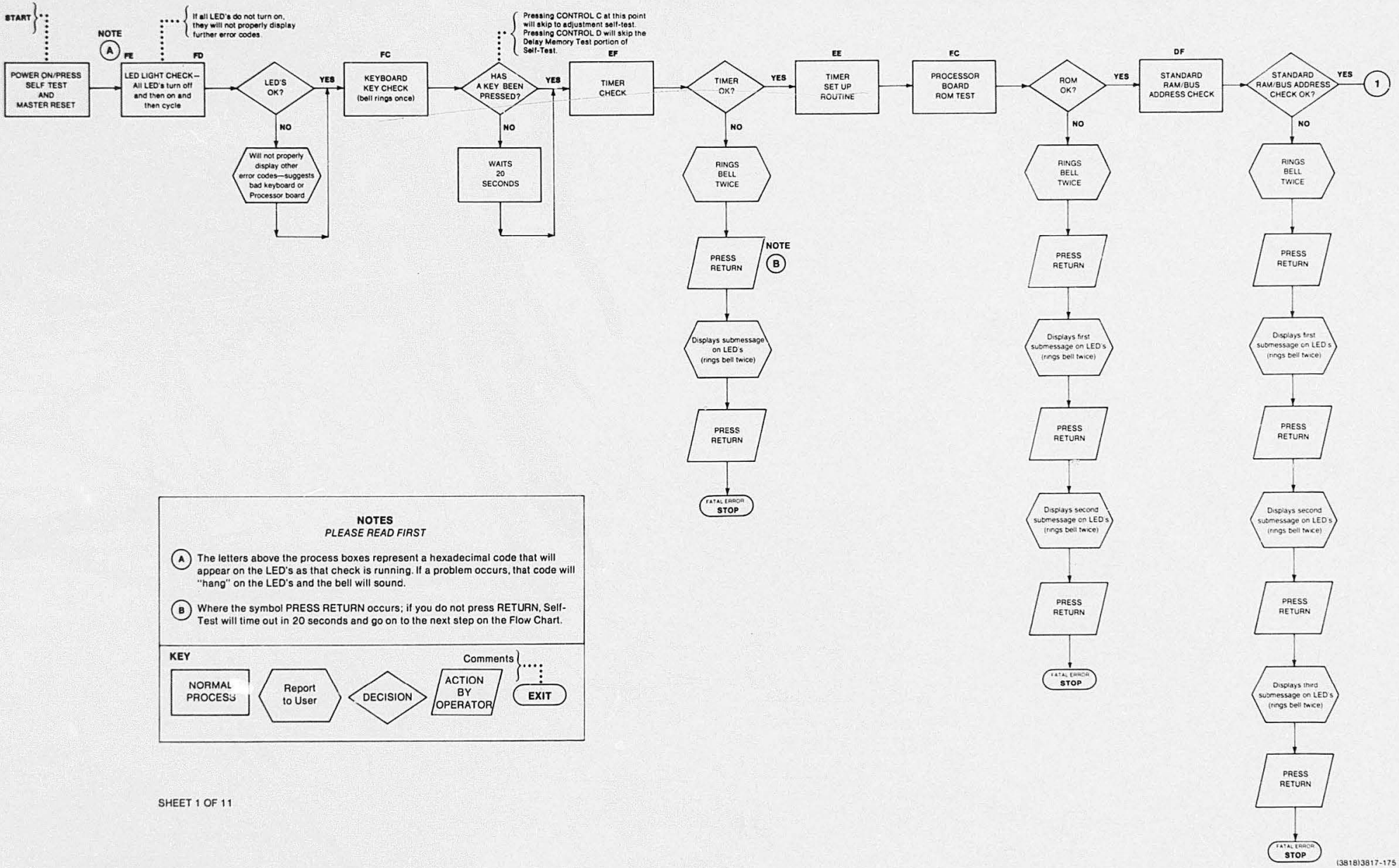
The status bits, that indicate which data firing (X1, X2, Y1, Y2) is being received, are out of sequence. This is a warning only; the routine will proceed normally. This message can indicate a problem on any of the circuit boards associated with the tablet.

X = NNN.NNN, Y = NNN.NNN,
Button = N (Using a Cursor Pen)

This is the standard message. It is displayed whenever the Z-axis switch is pressed while in presence. It displays X and Y in inches from the margin, the button number pressed (0 for stylus; Z, 1, 2, 3 for a cursor). It also indicates whether a pen (stylus) or cursor is in use.

X Timing Straps = NNNNNNNN,
Y Timing Straps = NNNNNNNN

This message is printed whenever a Z-axis switch is pressed with the stylus out of presence. It is a binary readout of the timing strap settings. A comparison of this readout with the actual strap settings will verify the proper operation of the timing straps.



SHEET 1 OF 11

(3818)3817-175

Figure 10-7A. 4112 Self-Test Flow Chart.

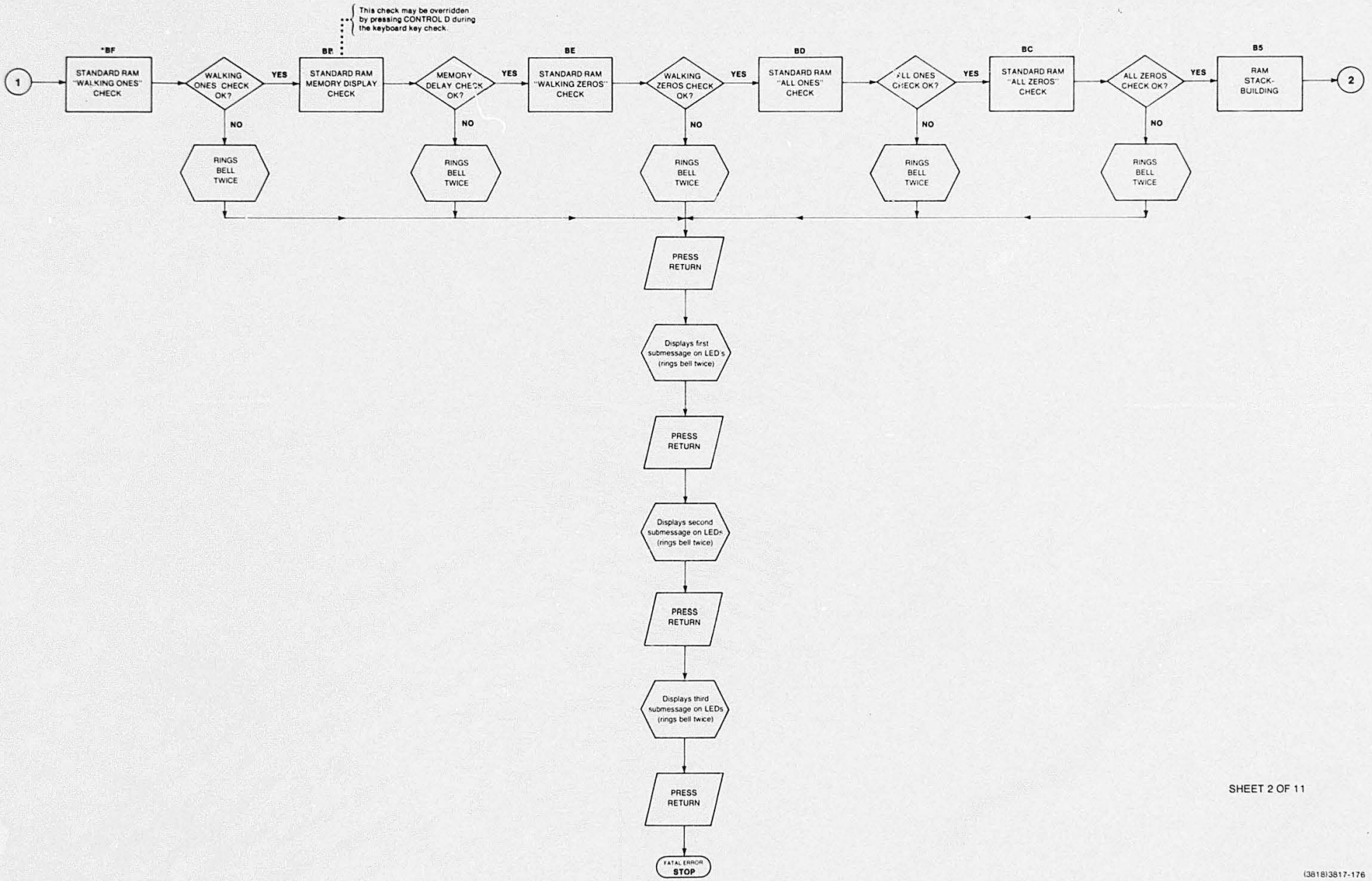


Figure 10-7B. 4112 Self-Test Flow Chart.

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(3818)3817-176

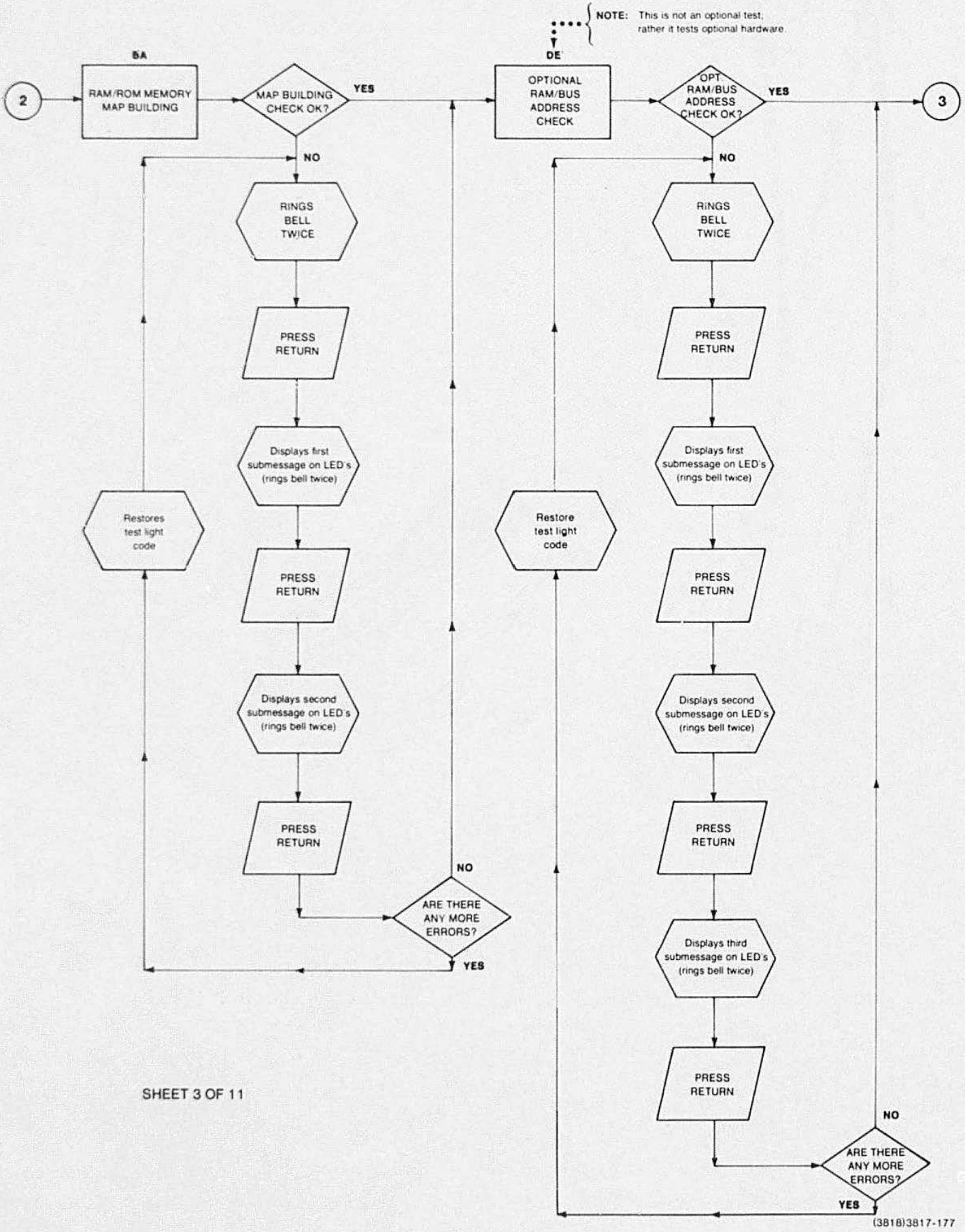

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Figure 10-7C. 4112 Self-Test Flow Chart.

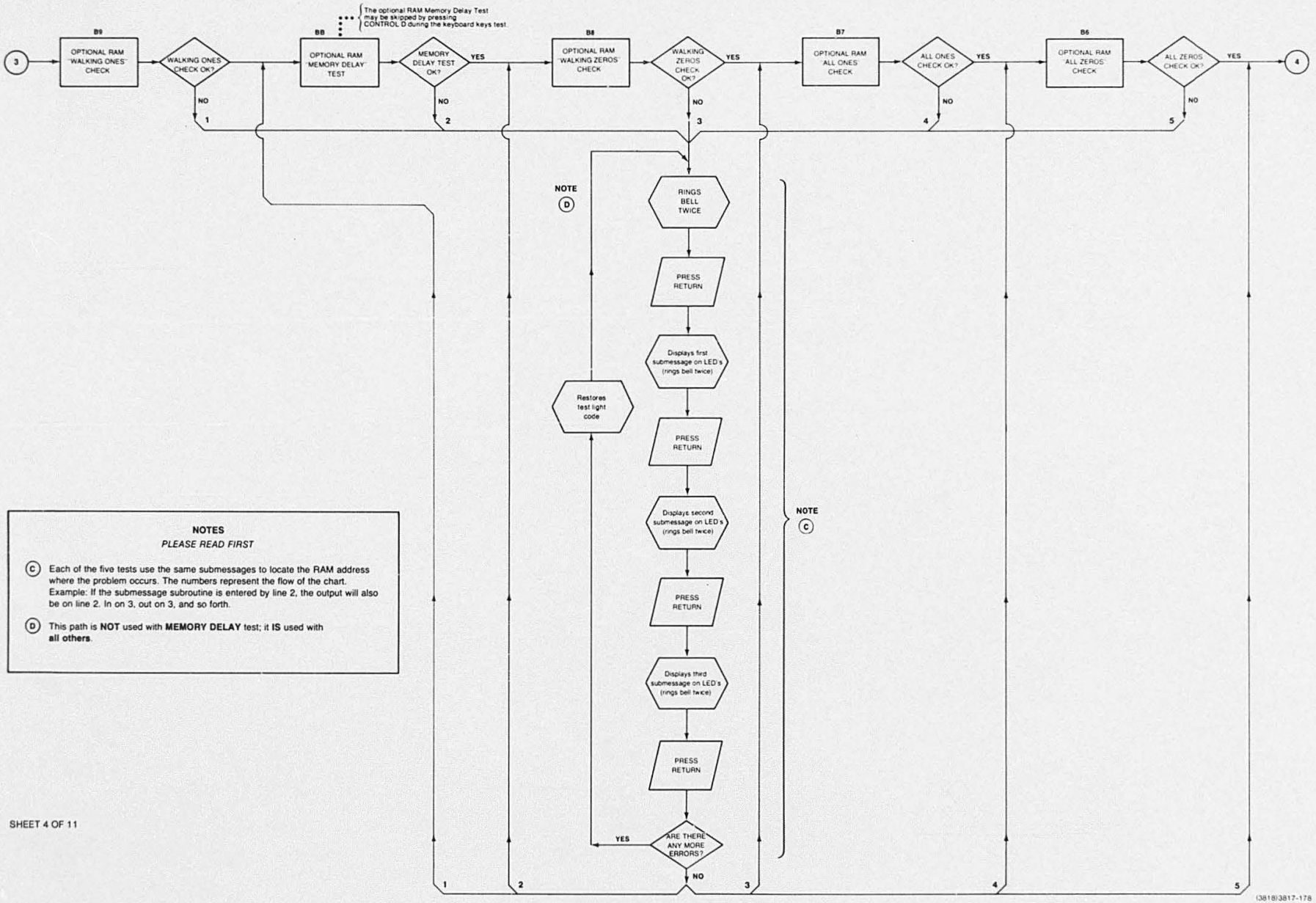

Figure 10-7D. 4112 Self-Test Flow Chart.

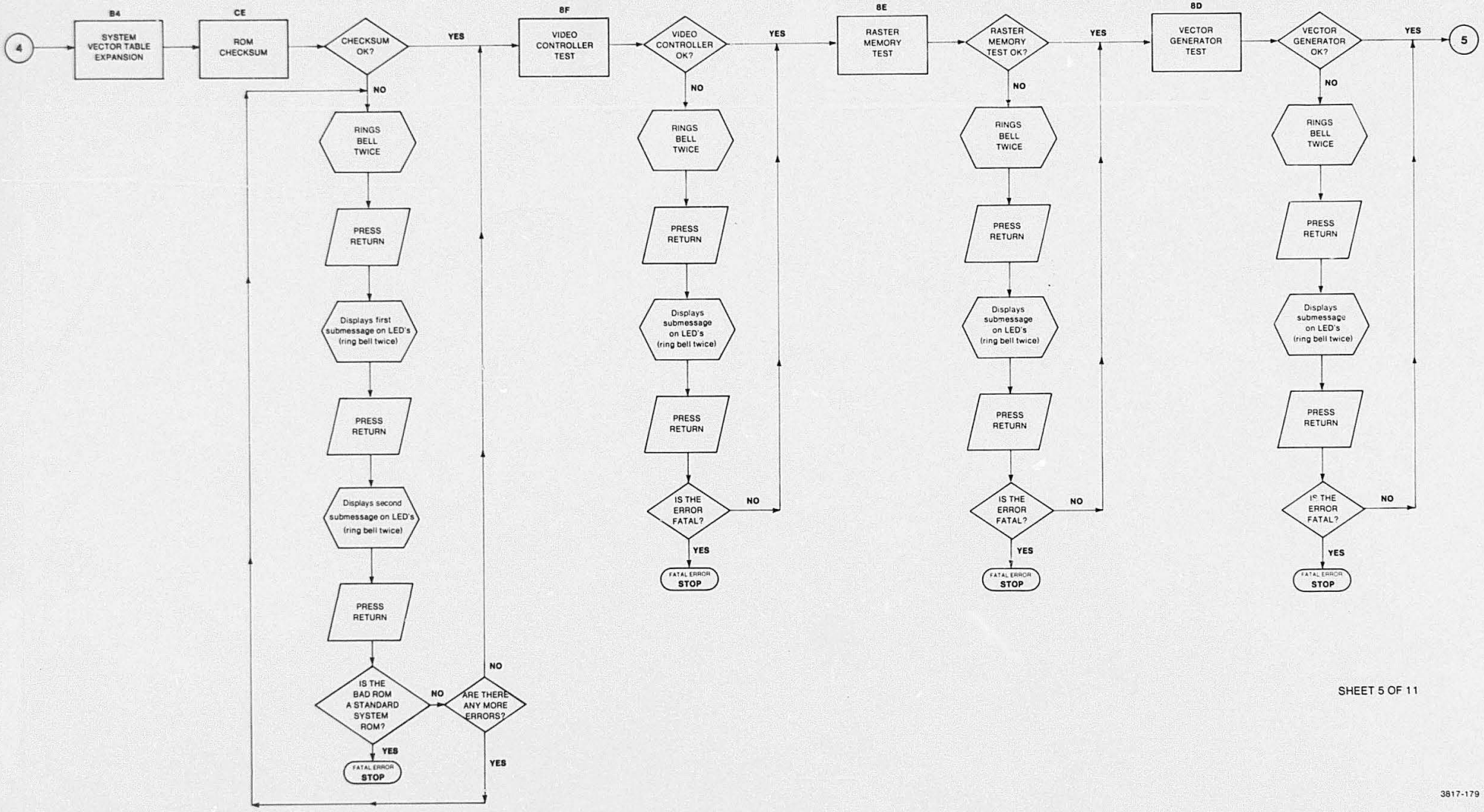

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Figure 10-7E. Self-Test Flow Chart.

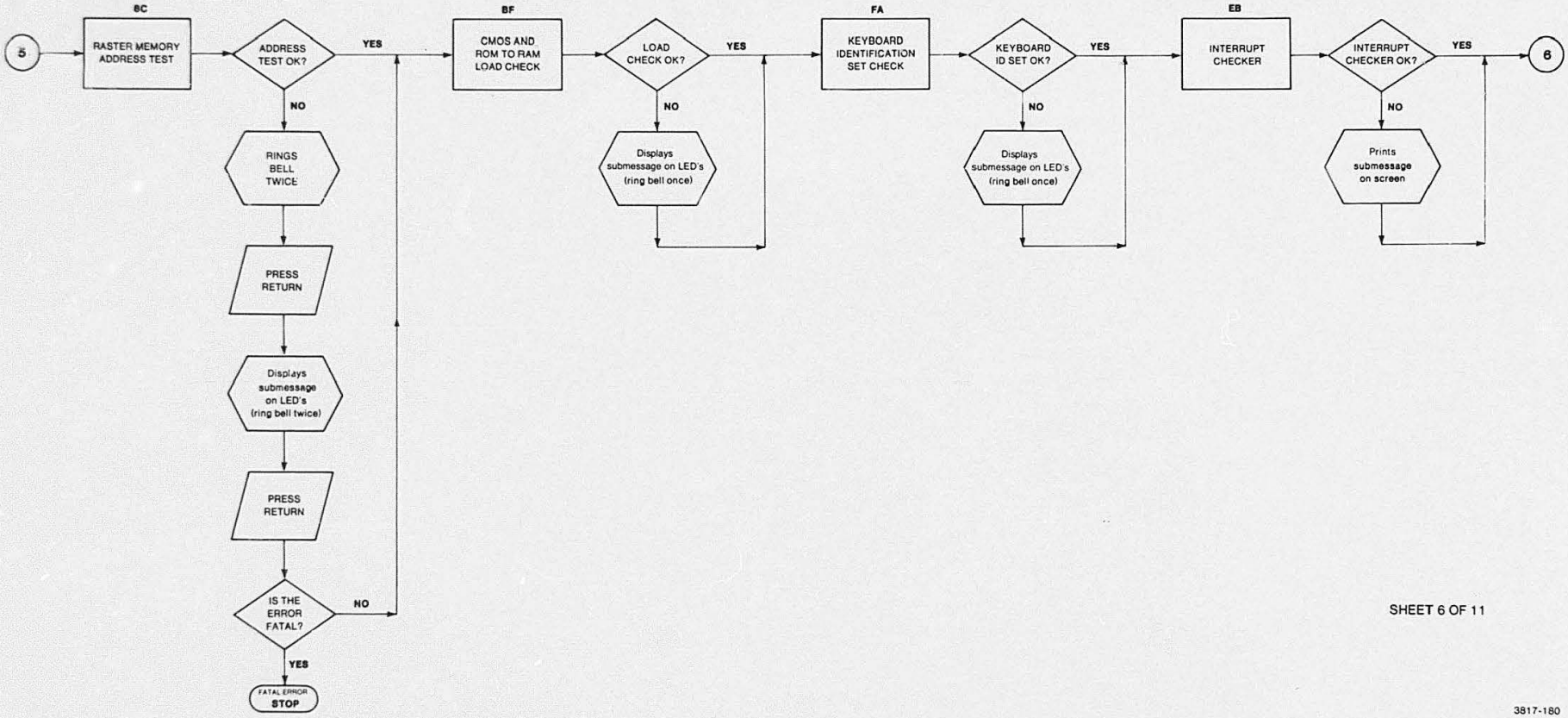

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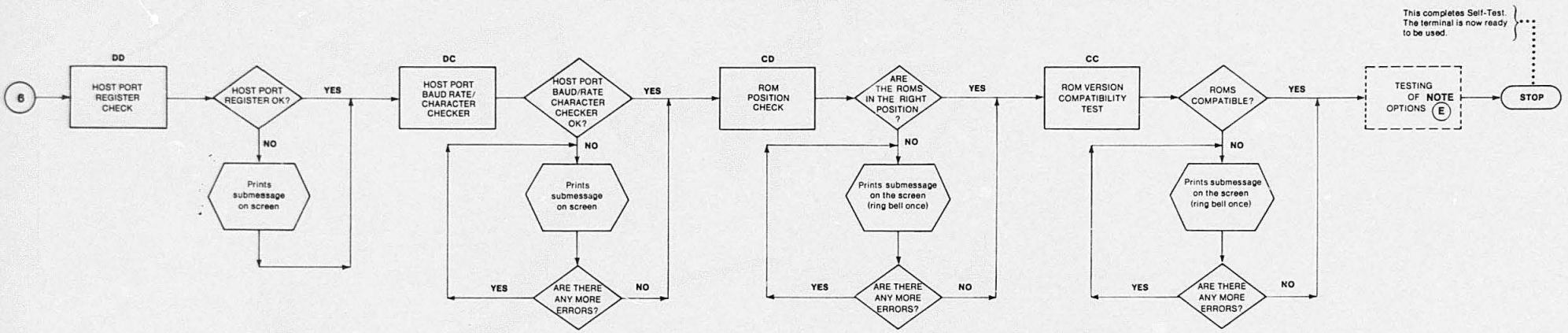
Figure 10-7F. Self-Test Flow Chart.



NOTE
PLEASE READ FIRST

(E) If any options are installed in the terminal, they will be tested at this point (except RAM options, which were tested earlier). The option boards tested include the Disk Controller board, 3 PPI board, and Tablet Controller board. Tests on these boards are performed in descending sequence of the hexadecimal error codes.

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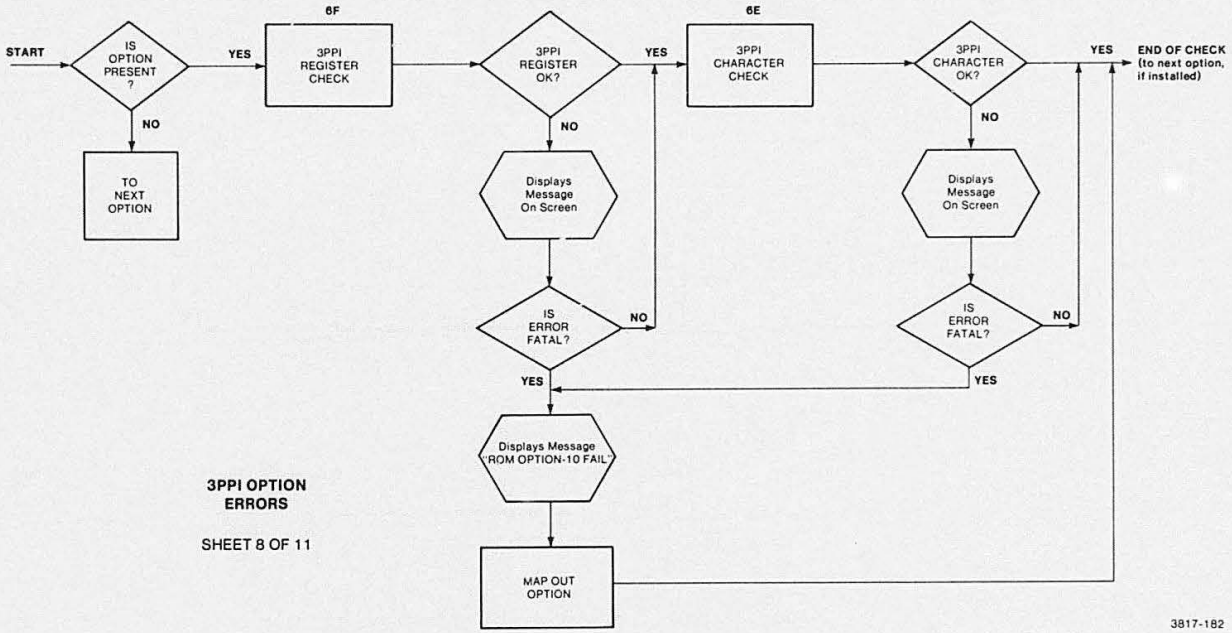
Figure 10-7G. Self-Test Flow Chart.



3PPI OPTION ERRORS

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Figure 10-7H. 3PPI Self-Test Flow Chart.

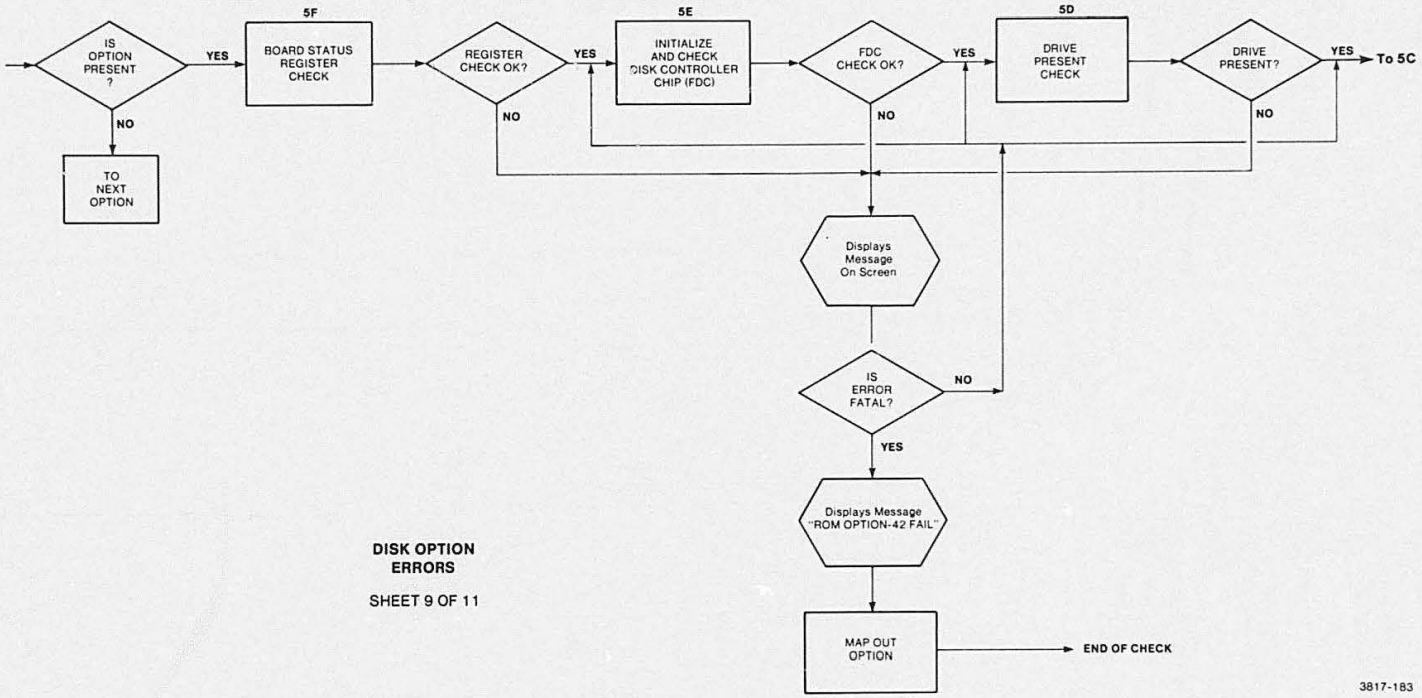
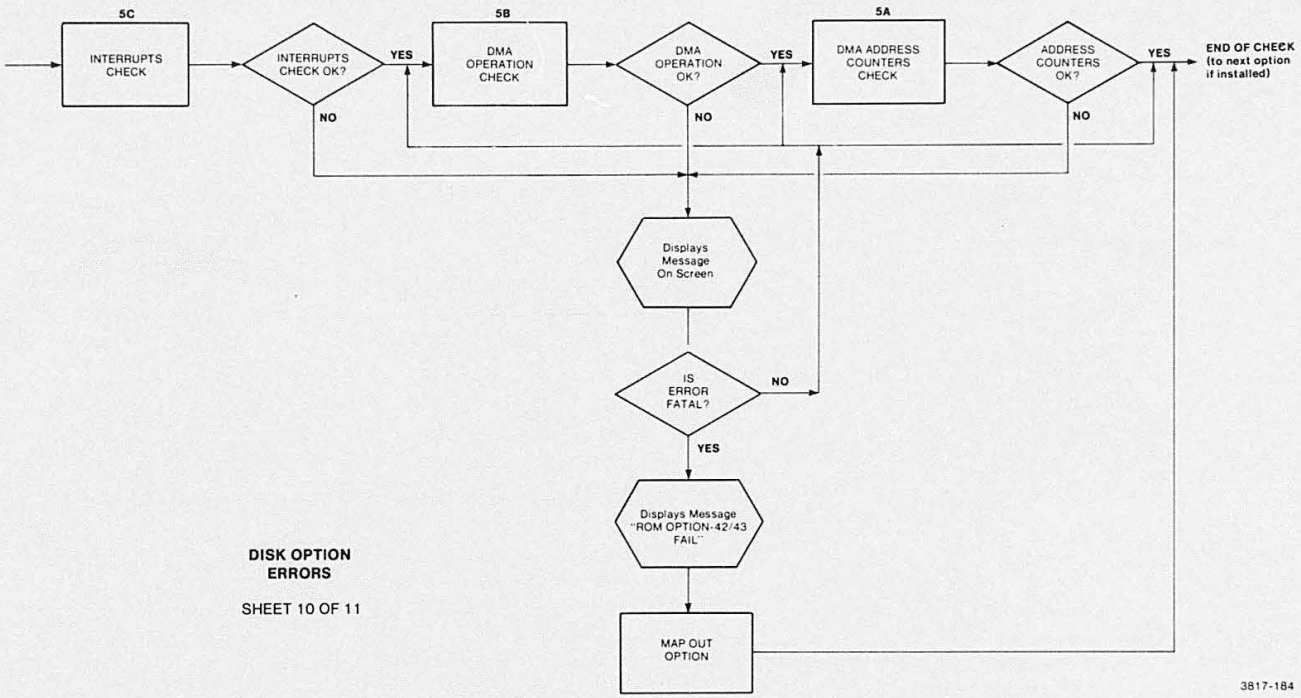


Figure 10-7I. Disk Self-Test Flow Chart.



DISK OPTION ERRORS

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Figure 10-7J. Disk Self-Test Flow Chart.

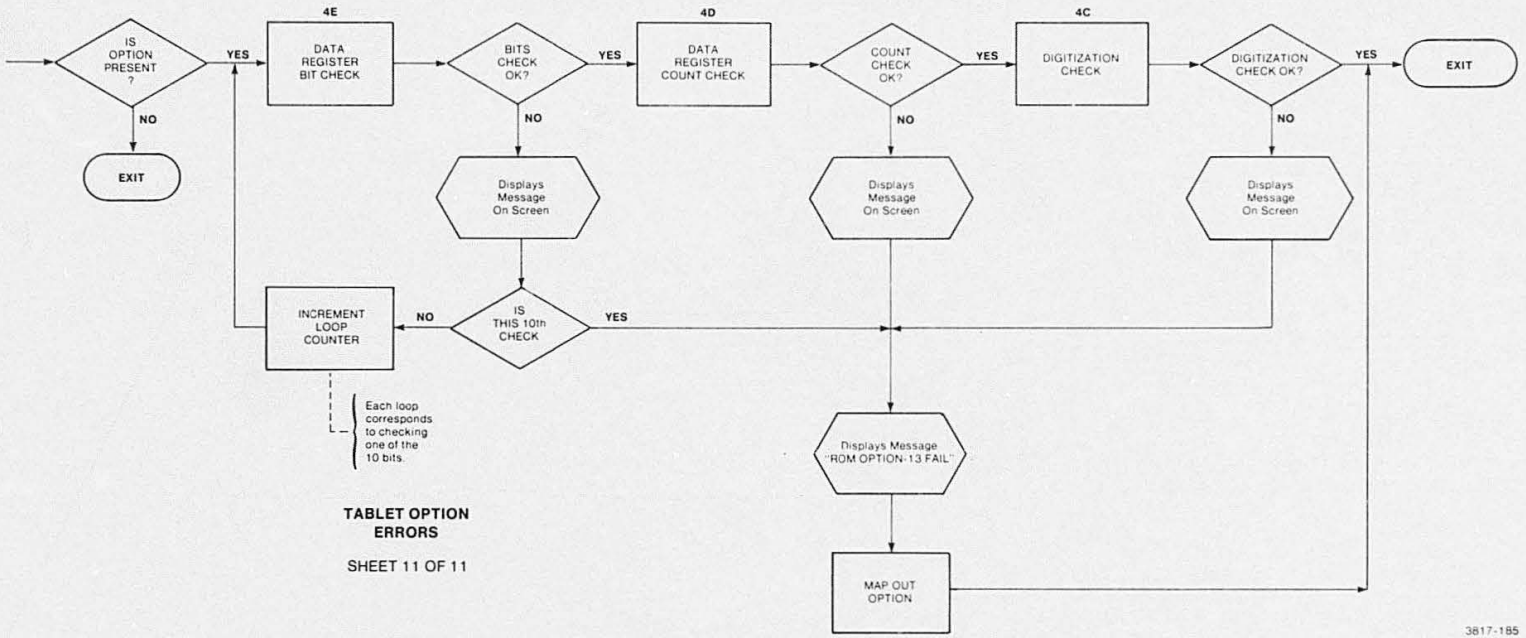

Figure 10-K. Tablet Self-Test Flow Chart.

Section 11

MAINTENANCE

This section contains the disassembly and reassembly procedures required for trouble shooting, calibration, and repair access of the 4112 terminal. This section contains the preventive and corrective maintenance procedures for the main 4112, and also includes a summary of maintenance information for its Low Voltage Power Supply, and the optional Flexible Disk Drive (and controller).

SAFETY CONSIDERATIONS

Before performing any of the maintenance procedures listed in this section, carefully read the Operators Safety Summary at the front of this manual.

PREVENTIVE MAINTENANCE SCHEDULES

The 4112 terminal is designed to require very little routine or preventive maintenance. Except for the optional disk drive units, no lubrication or cleaning is required. If routine cleaning and maintenance is desired, observe the following yearly P-M schedule.

The preventive maintenance procedures listed here are a summary of the P-M schedules for the various modules in the terminal:

- Display Module
- Keyboard and Thumbwheels
- Card-cage and Circuit cards
- Low-Voltage Power Supply
- Disk Drive options

CLEANING AND PREVENTIVE MAINTENANCE OF DISPLAY MODULE, KEYBOARD, AND INTERNAL PARTS

Read ALL of the warnings and cautions in this cleaning section before attempting any of the cleaning procedures given here.

CAUTION

To avoid damage to the plastics used in the Display Module and Keyboard, do NOT use cleaning agents that contain benzene, acetone, toluene, xylene, or similar cleaning agents.

Clean the outside of the display tube using a soft cloth dampened with a solution of mild detergent and water.

WARNING

Disconnect the line power cord before cleaning any parts inside the 4112. Dangerous voltages exist inside the Display Module and may cause injury if contacted.

Remove dust inside the Display Module occasionally. Dust conducts electricity under high humidity conditions. The 4112's interior is best cleaned with a vacuum cleaner. Remove any remaining dust with a soft-bristle brush (paint brush) or cloth dampened with a mild detergent and water solution. To clean narrow spaces, use a cotton-tipped applicator.

Cleaning the Keyboard

This procedure describes how to clean off the residue of liquids, such as coffee, soft drinks, and so forth, that have been spilled on the keyboard.

CAUTION

The cleaning procedure uses water, so try to avoid getting water on speakers, paper light shields, and other parts susceptible to water damage.

CAUTION

Do not crush or squeeze the exposed capacitive pads in the switch frame.

NOTE

Drying times may be shortened by forced air drying at a maximum temperature of 165° F (60° C).

1. Refer to the Keyboard Removal procedure in this section in order to separate the keyboard assembly into the printed circuit board and the switch and frame assembly.
2. Wash the frame assembly thoroughly in clean, lukewarm water. Avoid crushing or squeezing the foam pads.
3. Shake the excess water out of the assembly, and set it on blocks to dry in the air for about two to four days. Note that cleaning off the residue left by some liquids may require more than one washing.
4. Wash the circuit board thoroughly in clean, lukewarm water. Use a soft sponge or cloth to dry the board.
5. Set the circuit board on blocks to dry in the air for about one day.
6. Reassemble the keyboard assembly.

WARNING

If a dampened cloth is used for cleaning any parts of the terminal that are only accessible with the cover removed, take extreme care to NOT leave any remaining water or moisture in the instrument when the cover is reinstalled. This situation could provide a potentially lethal shock hazard to the user when power is reapplied to the instrument.

ROUTINE VISUAL INSPECTION

Inspect the terminal occasionally for such defects as broken connections, damaged circuit boards, loose connectors, heat damaged parts, and general mechanical fitness. If the terminal is used in a high vibration environment, pay particular attention to connectors, cable strain relief, and the CRT mounting brackets. Refer to the parts replacement procedures for appropriate details.

The corrective procedure for most visible defects is repair or replacement; however, particular care must be taken if heat-damaged components are found. Overheating usually indicates other trouble in the unit. It is important to correct the cause of overheating to prevent recurrence of the damage.

LOW VOLTAGE POWER SUPPLY MAINTENANCE

The Low Voltage Power Supply does not require routine maintenance. Figure 11-1 shows the heat sink which contains a pair of switches and a fuse holder.

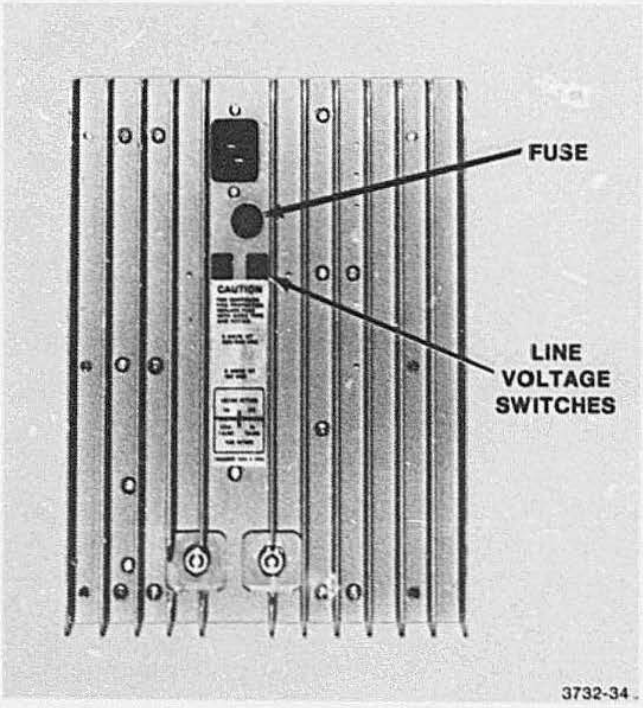

Figure 11-1. Power Supply Switches and Fuse Holder.

Fuse Replacement

The power supply contains just one fuse, mounted on the heat sink panel. If this fuse burns out, check for a possible overload which should be corrected. Then replace the fuse with the proper value as indicated in Table 11-1. This fuse is referred to as F9001 in the Replaceable Electrical Parts list (Volume 2).

Table 11-1

FUSE REPLACEMENT VALUES

Voltage Selected	Fuse Amperage
110 V (nominal)	6.25 A (medium blow)
220 V (nominal)	3.0 A (fast blow)

DISK DRIVE OPTIONS (42/43)

Options 42 and 43 are designed to require a minimum of maintenance and servicing. Once a year you should give the disk units a general inspection, looking for loose screws, connectors, and switches. Observe and clean any accumulated dust. Inspect fan motor shaft end play for excessive wear.

CAUTION

Do not attempt to oil any of the three motors in your unit. These motors have sealed bearings and therefore do not require lubrication.

As a general rule, the Option 42/43 does not require lubrication of any bearings or spindles, and any oil added will only catch dust and create greater wear problems.

Table 11-2 is a routine maintenance schedule for the disk drive units. Procedures 1 and 2 may be performed by the operator Procedures 3 through 6 are the responsibility of a technician and are fully described later in this section.

Table 11-2

DISK DRIVE UNIT MAINTENANCE SCHEDULE

Procedure	Item	Inspect For	Interval	Action Required
1	Read/write head	Oxide buildup resulting in hard or soft error.	12 months	Clean read/write head.
2	Read/write head load button	Replace button.[a]	12 months	Replace button.[a]
3	Stepper motor and lead screw	Nicks, burrs, and dirt.	12 months	Clean off oil, dust, and dirt. Dress down nicks or burrs, or replace part.
4	Belt	Frayed or weak areas.	12 months	Replace.
5	Base	Loose screws, switches and connectors. Check for dusk and dirt.	12 months	Tighten screws, connectors, and switches. Clean off dust and dirt.
6	Read/write head	Aborted I/O commands or distorted results	12 months	Align head. (See Section 5, *Adjustment Procedures*, in the *4110 Series F42/43 Disk Options Service Manual.*

[a]Replace load button at each 12 month interval regardless of condition.

DISASSEMBLY/REASSEMBLY PROCEDURES

REMOVING MAIN COVER PANEL

1. Position the terminal so the cover panel's attaching screws are accessible. (See Figure 11-2.) Remove screw from both sides.

2. Remove the cover's rear mounting screws. See Figure 11-2, again.

ACCESSING CARD-CAGE

Unscrew the two mounting screws from front and side of the card-cage. See Figure 11-3 (A and B). Tilt the cage back and away from the Display Module.

REMOVING CIRCUIT BOARDS

With the card-cage tilted up, determine which board is to be removed. Refer to Figure 11-4 for the slot number.

1. First, label all cables and wires that connect to the front edge of the circuit board. Then remove these cables.

2. Read the name label on the board to be sure you are removing the intended board.

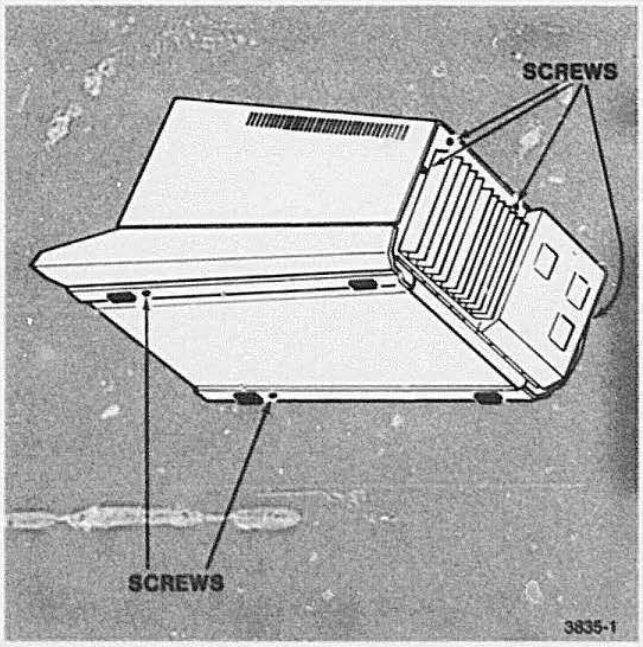

Figure 11-2. Location of Cover Panel Mounting Screws.

3. Grasp the upper and lower locking tabs as shown in Figure 11-5. Pull the tabs out toward you.

4. Pull the board straight out of the slot.

   Before reinserting a circuit board verify that you are placing it in the proper slot according to Figure 11-4.

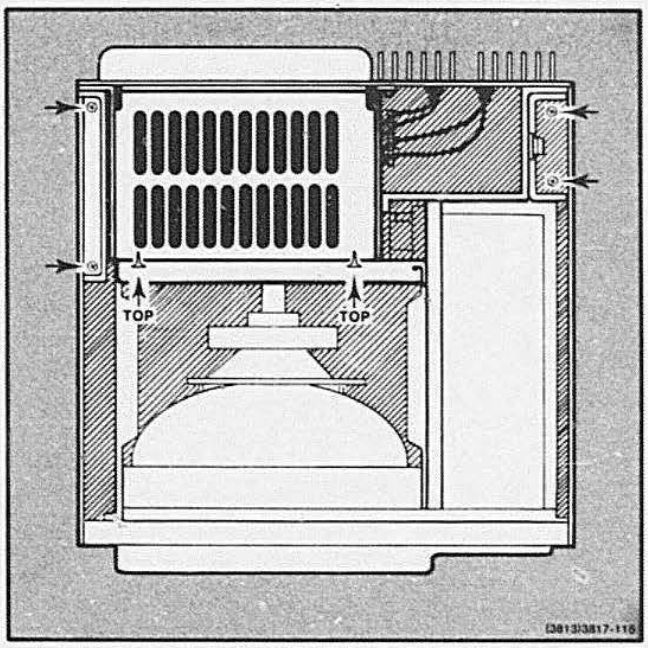

Figure 11-3. Location of Card-Cage Mounting Screws.

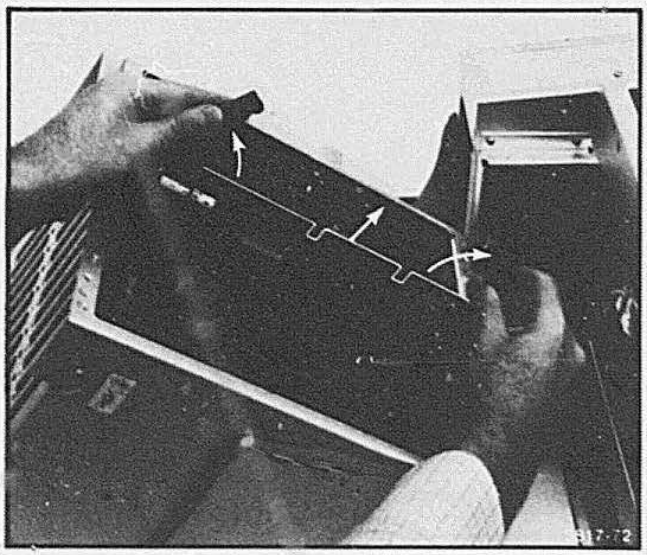

Figure 11-5. Lifting Tabs and Pulling Circuit Board.

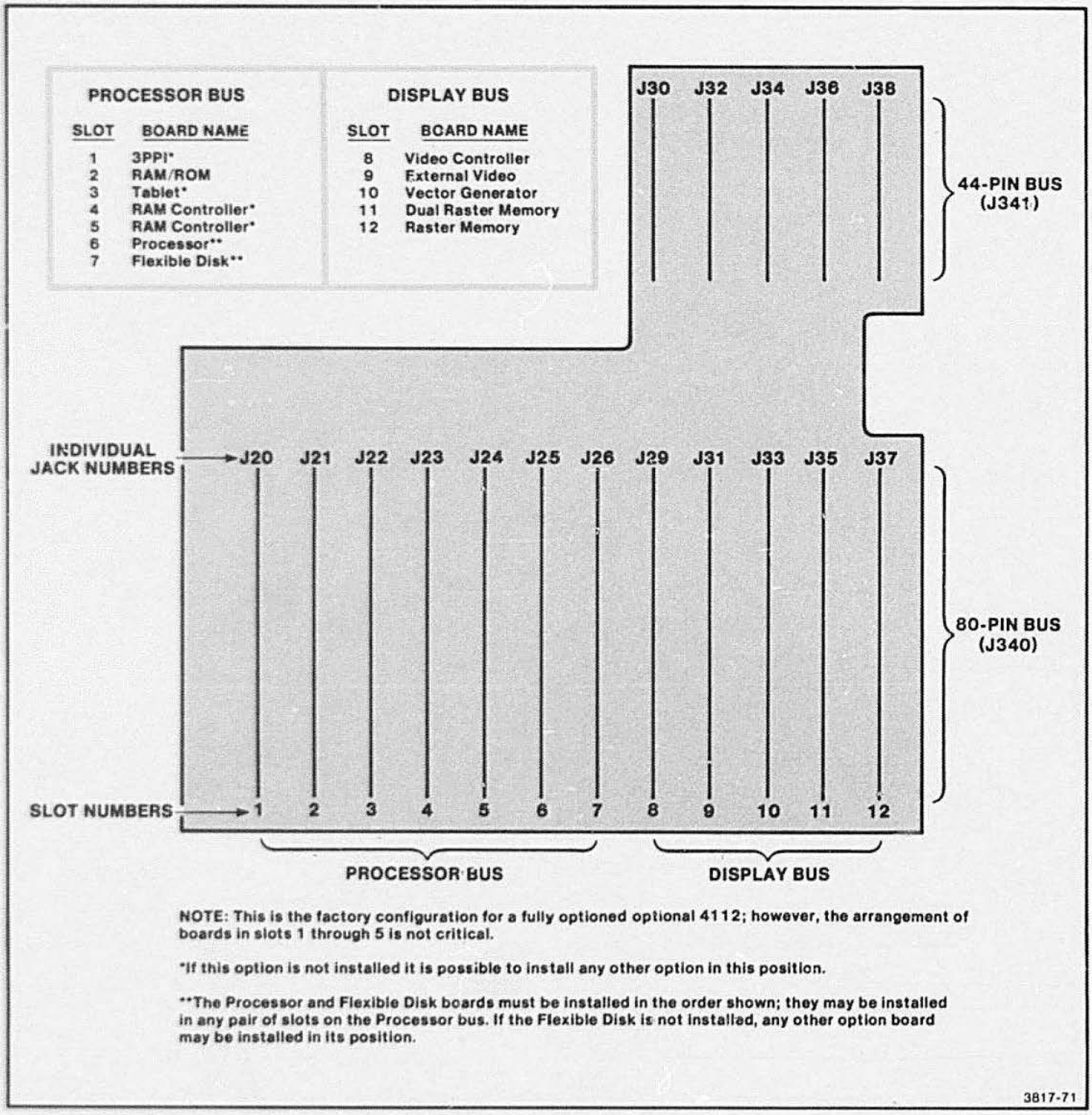

Figure 11-4. 4112 Motherboard.

REMOVING DRIVE UNIT

1. Remove the wrap-around cover from the disk drive unit. This panel attaches with three POZIDRIV® screws. See Figure 11-6.

2. Unplug all three cable connections from the rear of the drive unit. See Figure 11-7.

3. Remove the clamp-down from the rear of the drive unit; it attaches with two screws, shown in Figure 11-8.

4. Disconnect the write-protect/contrast control panel from the top of the drive unit enclosure. Only disconnect the wires to this panel if all testing is completed.

5. Remove four screws from the drive unit enclosure: two from the bottom outside lip, and two from the upper inside lip. See Figure 11-9 again. Pull the drive unit back away from the front bezel, and lift from terminal.

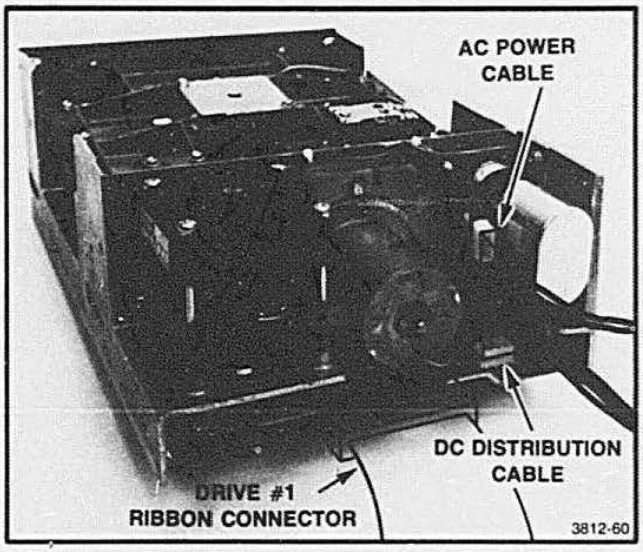

Figure 11-7. Left-Rear View of Drive Unit.

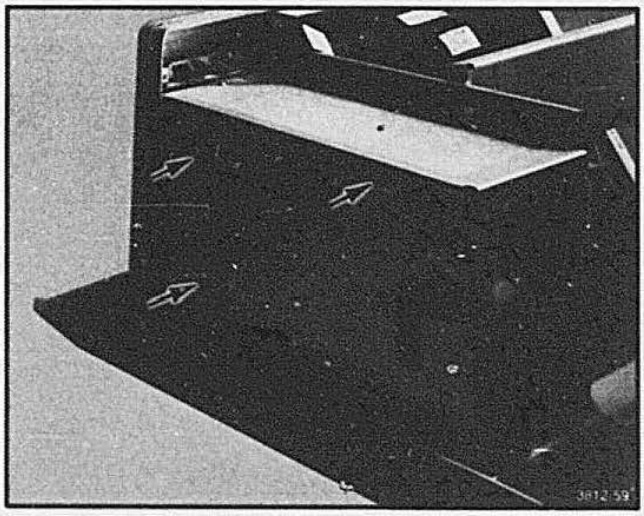

Figure 11-6. Removing Wrap-Around Cover.

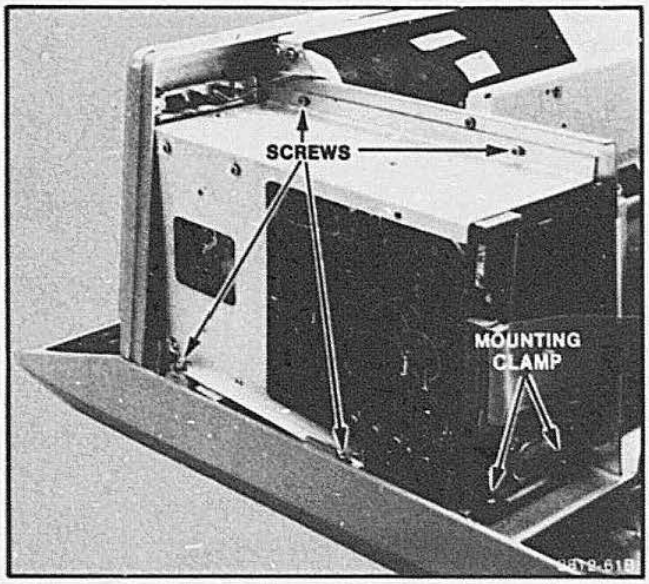

Figure 11-8. Dismounting the Drive Unit.

6. Remove the drive enclosure from the drive unit for complete service access to the drive unit. This enclosure attaches with six screws. See Figure 11-10.

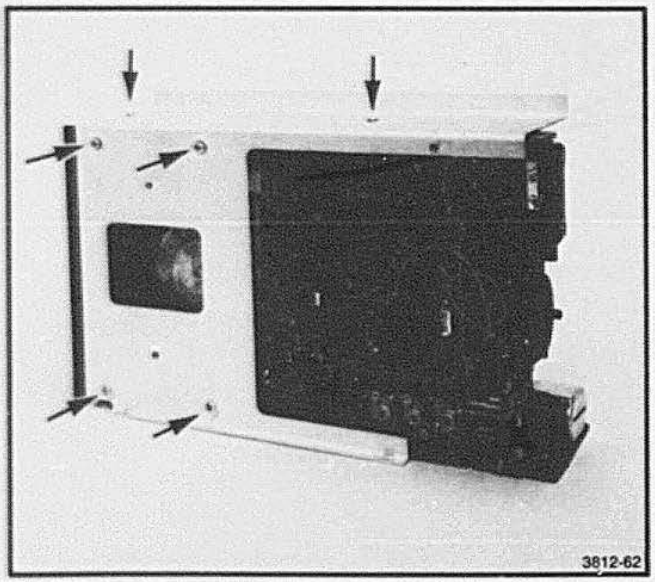

Figure 11-9. Drive Unit Enclosure Mounting Screws.

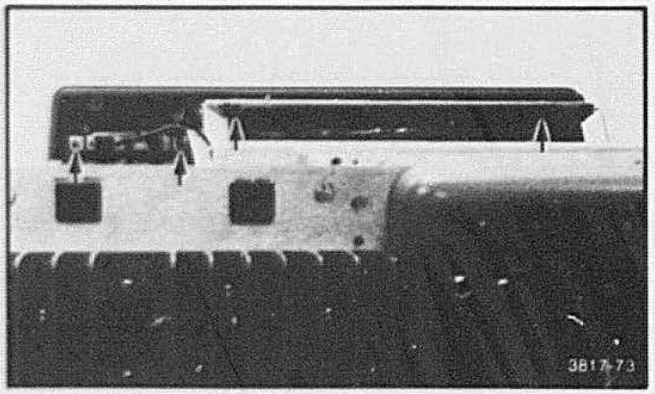

Figure 11-10. Bezel Upper Mounting Screws and Refresh Intensity Control.

REINSTALLING DRIVE UNIT

1. Replace the wrap-around cover over the drive unit. Attach with three POZIDRIV® screws. See Figure 11-6.

2. If the Disk Controller board was removed from the card-cage, insert it now in slot #7 (or the slot adjacent to the right side of the Processor board).

3. Allow the card-cage to swing back down into its normal mounted position. Fasten down the card-cage with two screws in front and side. Same as Figure 11-3.

4. Place the main cover back on the terminal. See Figure 11-2.

DRIVE UNIT DISASSEMBLY/ REASSEMBLY PROCEDURES

See the complete instructions in the *119-0977-00/03 Flexible Disk Drive Instruction Manual*, and the *Option 42/43 Service Manual.*

REMOVING AND REINSTALLING THE LOW VOLTAGE POWER SUPPLY

Remove the terminal's cover; then label and disconnect all cables and wires that connect to the power supply (unplug at the power supply connector end). See the *620-0295-00 Power Supply Service Manual* for removal and mounting information, and for servicing of its internal parts.

REMOVING AND REINSTALLING THE DISPLAY MODULE

1. Turn off terminal and disconnect terminal's power cord.

2. Remove cover from terminal. To do this, first remove four POZIDRIV® screws from the back panel, two screws from the bottom, and lift off the cover.

3. Remove front bezel from around the front of display and disk drive unit as follows:
   a. Remove Refresh Intensity control from front of the terminal after loosening the Allen set screw and knob.
   b. Remove the four screws shown in Figure 11-10.
   c. Remove a screw from the bottom-left and bottom-right of the bezel as shown in Figure 11-11A and B.
4. Remove four POZIDRIV® screws from bottom of Display Module chassis as shown in Figure 11-12.
5. Remove one POZIDRIV® screw from the upper part of the module chassis, next to disk drive unit. See Figure 11-13.
6. Remove the cables from J587, J586, and J582.
7. Lift Display Module out of terminal.
8. Reinstall Display Module by performing Steps 1 through 7 in reverse order.

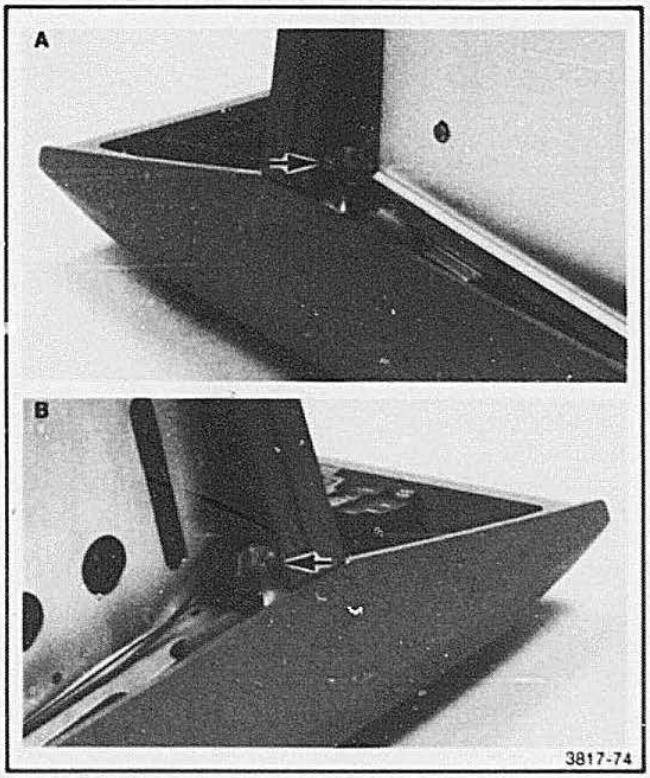

Figure 11-11. Bezel Left and Right Mounting Screws.

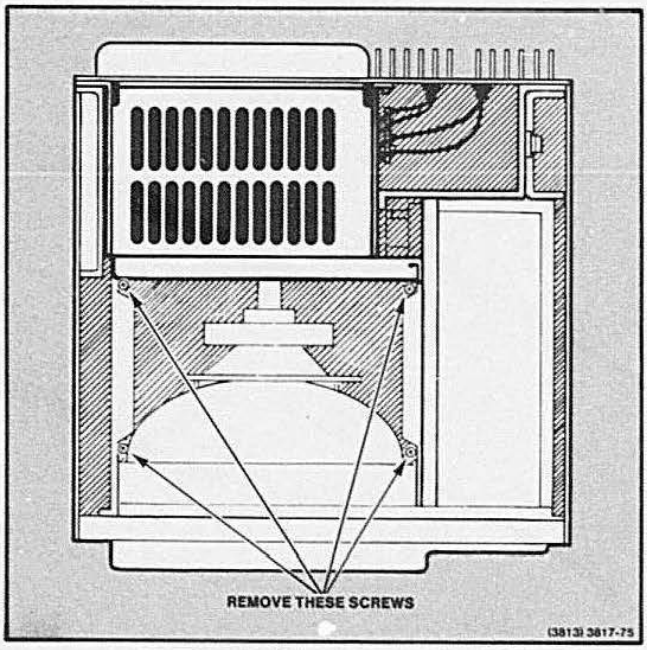

Figure 11-12. Display Module Base Mounting Screws.

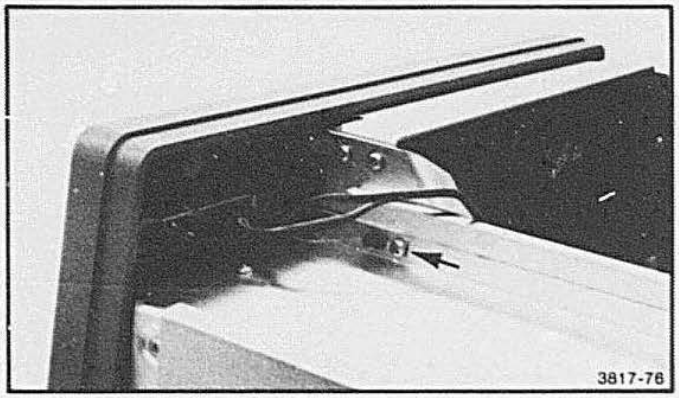

Figure 11-13. Display Module Upper Mounting Screws.

REMOVING AND REINSTALLING DISPLAY MODULE CIRCUIT BOARDS

When viewing the two Display Module circuit boards from the back of the terminal, the Delection Amplifier board is on the right, and the High Voltage board is on the left. To remove either of these boards:

1. Label all cables and wires that connect to the board with the jack number printed on the board connector.
2. Unscrew only the outer screws from the board (two on the Deflection board, and three on the High Voltage board).
3. Pull the board(s) away from the center of the display, and out of its dovetail channel in the center mounting piece. Lift board clear of the CRT and module.
4. Reinstall by reversing Steps 1 through 3.

REMOVING AND REINSTALLING THE DISPLAY CRT

1. Turn off terminal and disconnect power cord.
2. Remove cover: unscrew four POZIDRIV® screws from back, two screws from bottom, and lift off cover.
3. Remove front bezel (see procedure under *Removing Display Module*).
4. Unplug CRT socket from rear of tube.
5. Loosen yoke clamp by unscrewing 1/2-inch screw.
6. Remove yoke cables J589 and J583 from circuit board.
7. Remove yoke (slide it over neck of CRT).

WARNING

Do NOT touch the CRT anode connector or the high voltage lead connector. Dangerous voltages may be present.

Ground (discharge) the anode connection before removing the high voltage cable.

8. Insert flat-blade screwdriver under rubber boot on CRT high voltage lead. Then ground the screwdriver against chassis (Figure 11-14). Using screwdriver, push contacts together; then pull high voltage lead free of anode connection on CRT.
9. Remove clip from spring that grounds the aquadag coating, but leave spring attached to the CRT.
10. Unbolt four posts by unscrewing the four 3/8-inch nuts at each corner of the front of the CRT.
11. Remove CRT.

CAUTION

When you perform the following step, take care not to damage the CRT, its neck, or pins.

WARNING

To avoid electric shock when replacing defective parts, unplug the terminal's AC power source.

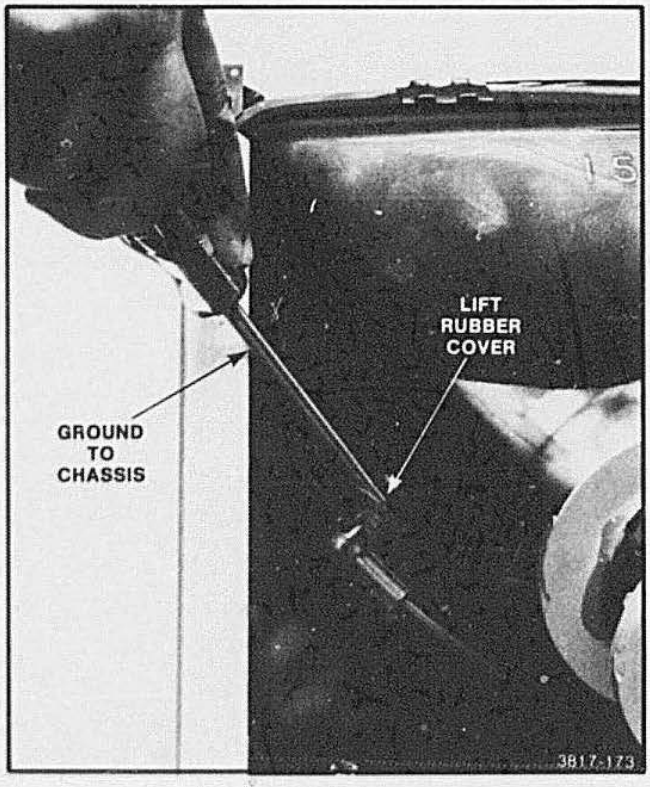

Figure 11-14. Removing H.V. Anode Cable From CRT.

UPPER FAN REPLACEMENT

One of the cooling fans in the 4112 is mounted next to the drive unit on the display tube side of a partition. To remove this fan:

1. Follow the instructions for gaining access to the drive unit found earlier in this section.
2. With the cover off of the terminal and the card-cage tipped back, this fan is now accessible.
3. Unplug the power wires from the fan.
4. Remove the three screws attaching the fan to the cooling shroud. See Figure 11-15.
5. To reinstall the new fan, follow the preceding steps in reverse order.

LOWER (SQUIRREL-CAGE) FAN REPLACEMENT

This fan, as the name implies, is a squirrel cage (~ 8-inches long) connected to a motor. The fan is located under a lateral channel under the rear of the Display Module and Disk Drive unit. This fan is mounted on a removable panel, fastened to the under side of the terminal with six screws. To remove this fan:

1. Turn terminal on its side, or otherwise position terminal so its bottom is accessible.
2. Locate the six POZIDRIV® screws in the fan panel. See Figure 11-16. Remove these screws.
3. Carefully lift panel out away from the terminal, while paying attention to not pull lose the fan's AC power wires.
4. Label and unplug the power wires from the fan motor.

If the fan motor or squirrel cage is defective, but not both, you may want to separate the squirrel cage from the motor, and replace only the defective part.

The motor and blower attach via a rubber sleeve on the connective drive shafts.

To reinstall the fan, follow the above steps, but in reverse order.

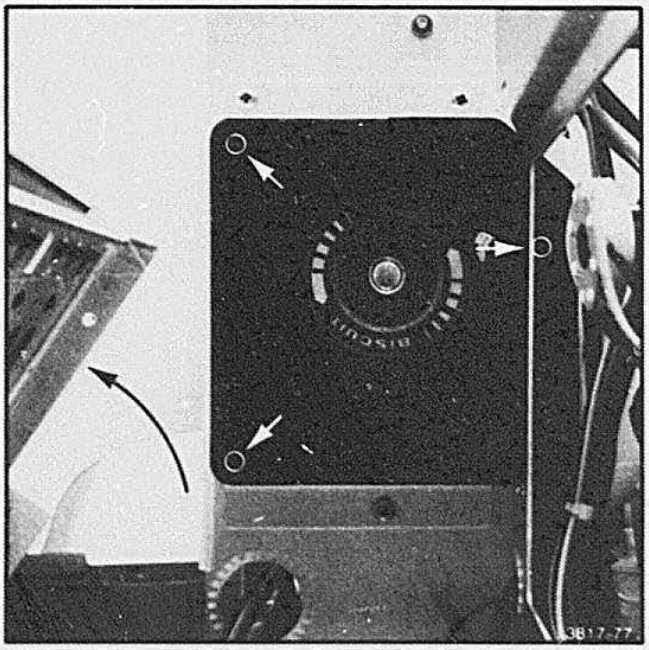

Figure 11-15. Removing Upper Cooling Fan.

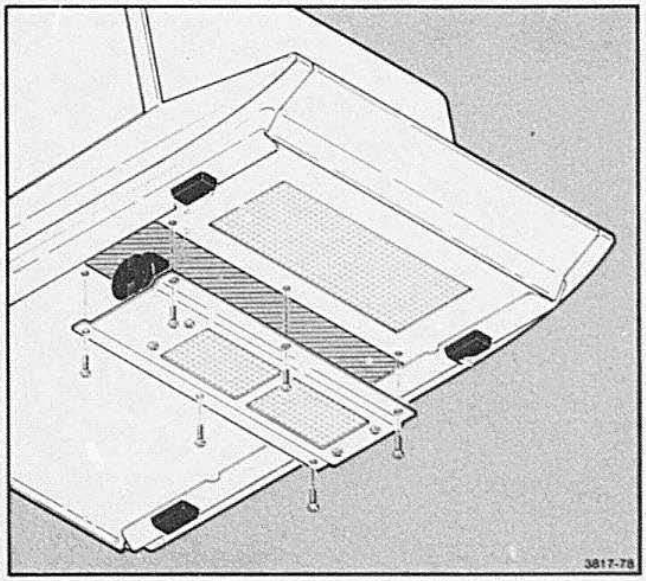

Figure 11-16. Removing Lower Cooling Fan.

WRITE-PROTECT AND CONTRAST CONTROLS REPLACEMENT

1. Remove mounting screws from terminal cover, and lift off the cover.
2. Remove the bracket that holds the write-protect and power switches. Unscrew two POZIDRIV® mounting screws.
3. Unplug the contrast cable from jack, J587, on the Deflection Amplifier board (under the display tube).
4. Unplug the write-protect cable from J206 on the Disk Controller board.
5. Mount new switch bracket and reconnect the contrast and write-protect cables to their jacks.

NOTE: The color coded wires should be soldered to the write-protect switch as follows:

- Middle switch contact — orange wire
- Lower switch contact — yellow wire

REMOVING REAR COVER PANEL

The protruding rear cover panel must be removed to gain access to the back side of the motherboard and the cabling to the various connectors on the rear panel of the 4112. Remove this panel by unscrewing the six POZIDRIV® screws shown in Figure 11-17. Then, carefully pull this panel away from the terminal, so that no cables are pinched or torn from their connectors.

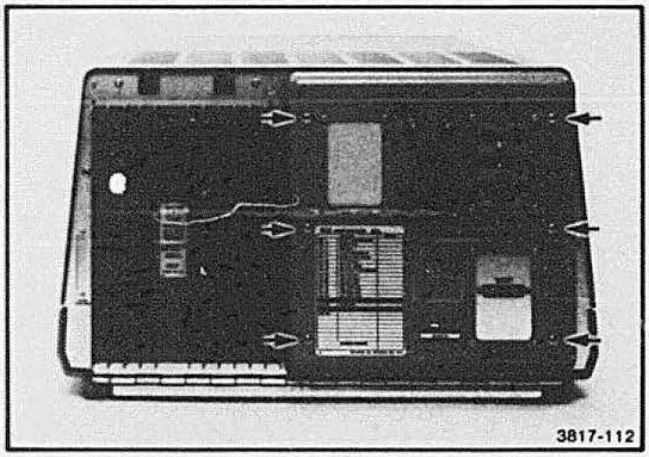

Figure 11-17. Removing Rear Cover Panel.

REMOVING/REPLACING THE KEYBOARD ASSEMBLY

If any key switches or other keyboard components need replacing, use the following procedures to gain access and replace such parts.

To access the Keyboard circuit board, use the following procedure:

1. Remove two POZIDRIV® screws from under the front of the terminal (see Figure 11-18).

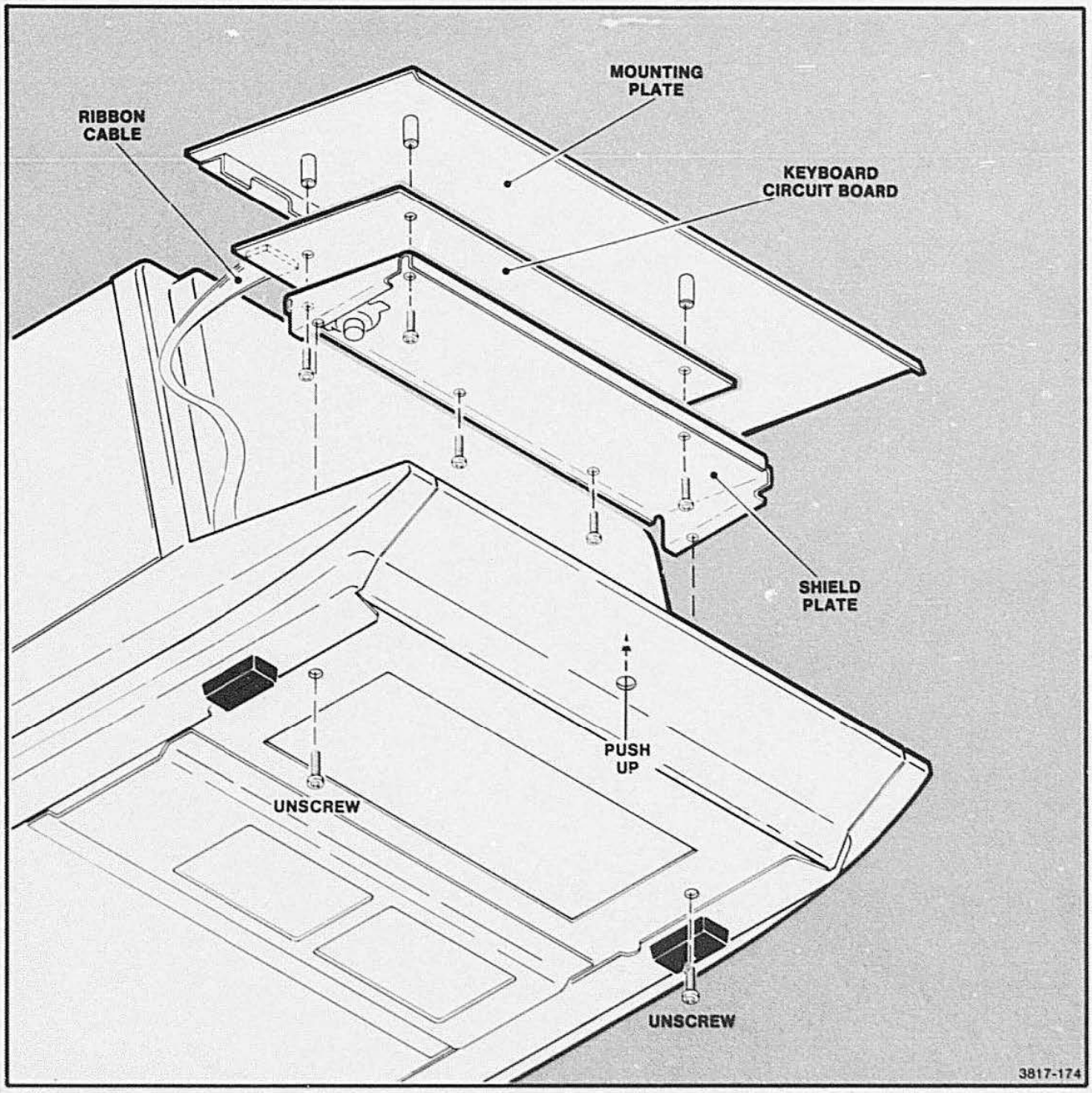

Figure 11-18. Removing the Keyboard Assembly.

2. Then, using the screwdriver bit holder, push up into the hole under the front edge of the terminal. This dislodges the front edge of the keyboard assembly so you may lift this assembly free of the terminal (as needed in the following steps).
3. Unplug the keyboard ribbon cable as needed.
4. Unplug the speaker wire from its connector on the end of the Keyboard circuit board.
5. Unscrew the five POZIDRIV® screws that attach the shield plate to the Keyboard circuit board. This allows the shield plate (with speaker), and circuit board, to be removed from the mounting plate.

Reassembly:

1. Install shield plate (with speaker), and circuit board, on mounting plate using the five screws noted in Step 5 above.
2. Plug the free end of the speaker wire onto the connector on the Keyboard circuit board.
3. Reconnect the keyboard ribbon cable onto its connector on the Keyboard circuit board.

NOTE

The ribbon cable between the keyboard and Processor board has plugs that appear to be keyed. These plugs can be accidentally reversed on either the keyboard or the Processor end. See that they are connected properly.

If either one of these plugs are reversed, the terminal will not function, leaving the PAGE FULL light on during Power-Up. There is no error code for this as Self-Test does not start.

4. Place the keyboard assembly back in the terminal; a lip on each side of the opening supports the assembly. The front edge of the exposed plate is bent downward so it fits into the crevice along the front end of the terminal.
5. Replace the two POZIDRIV® screws under the front part of the terminal (see Figure 11-18 again).

REPLACING KEYBOARD KEY CAPS

A key cap may be removed by simply pulling straight up on the key. A gripping device, such as a rubber glove, may facilitate removal of key caps from their switches. It is not necessary to remove the keyboard assembly from the terminal to replace a key cap.

Replace new key cap as follows:

1. First, position the key so that its nomenclature is pointing in the proper direction (not upside down or sideways). See Figure 11-19.
2. Then insert the fork (under cap) into the receptacle in the key switch plunger. Be sure the spring is still in place (around the plunger). Push the key cap all the way onto the switch so that it rests level with the other keys when released.

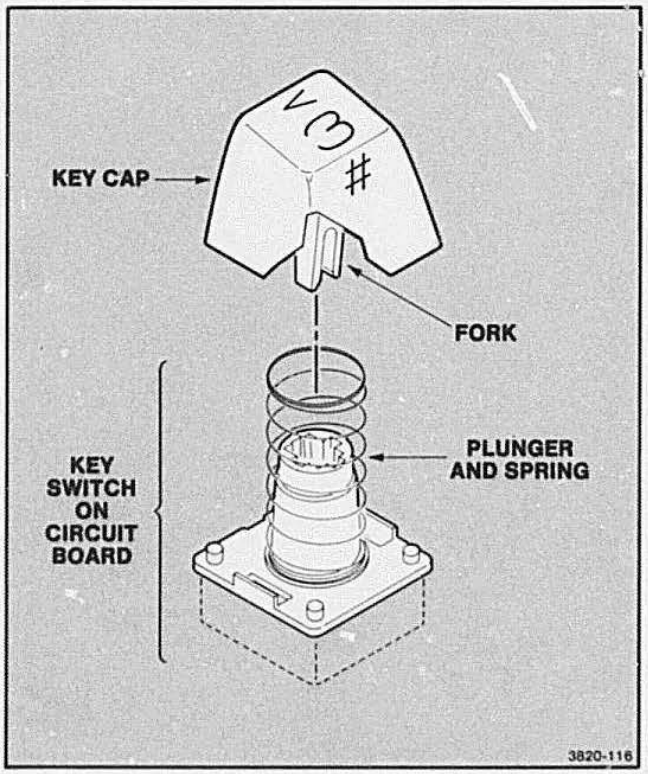

Figure 11-19. Installing Replacement Key Cap.

Appendix A

4112 SIGNAL LIST

The following is a list of all the signals appearing on the schematics (in Section 8 of Volume 2).

Signals can originate and terminate on the same board, going from schematic to schematic (example: A8-1;A8-4 originates on Page 1 of the Vector Generator board schematics and terminates on the Page 4 schematic of the same board). Signals may have more than one destination. There may also be more than one signal with the same name (example: Signal, WALU0-0, goes from schematic A9-4 to schematics A9-1 and A9-2.

There is also another signal on the Dual Raster Memory board also called WALU0-0. This signal originates in schematic A10-6 and goes to schematics A10-2 and A10-3.). Usually signals with the same name perform the same function or close to the same function. In the cases where signals with the same name perform a different function, a second definition is given.

In the following list the microprocessor unit is abbreviated MPU. The terms processor, MPU, and 8086 are interchangeable.

Signal	Source;Destination	Explanation
1STINTA-0	A2A1-2;A2A1-1	First Interrupt Acknowledge. This Processor board signal indicates when the first of two interrupt acknowledge (INTA) cycles is occurring. Only the second INTA contains useful information.
50Hz-0	A7A1-3;A7A1-2, A9-1	The 50Hz-0 line can be strapped for either a 50Hz or 60Hz refresh rate (60Hz American; 50Hz European).
A0-1 thru A19-1	A2A1-2;A2A1-3, 4, 5 A4A1-1;A4A1-3 A6-1;A6-2	(Local) Address (bits 0 through 19). This is the processor board address bus. It is created in the address drivers block from the MPU AD0-AD19 outputs. Note that some of these bits appear also on the RAM/ROM and RAM Controller boards with similar functions.
A15-0	A4A1-1;A4A1-3	A15-0 is the inverted local address line A15-1 and is used as a decoder bit for the ROM address decode section.
A6-1 thru A0-1	A10-4;A10-5	Demultiplexed address for raster memory RAMs.
ACCREAD-0	A8-1;A8-3	Decoded read strobe for slope generator RA register (at address F702).
ACK1-0	A4A1-1, A7A1-1;A2A1-1	Acknowledge 1. This system bus signal can be used as a slave response for no MPU wait states. The Processor board uses ACK1 to terminate a bus data transfer when it detects a bus timeout condition from the bus timeout detector circuitry. (This signal can be output from the RAM/ROM board through the use of a cut strap, not currently output from this board.)
ACK2-0	A4A1-1, A6-1;A2A1-1	Acknowledge 2. ACK2 serves as an advanced transfer acknowledge to eliminate WAIT states in the MPU. The signal derives from SACK-0 which is output by the timing and control block inside the dynamic RAM controller. SACK-0 indicates the beginning of a memory access cycle.

Signal	Source;Destination	Explanation
AD19-1 thru AD0-1	A2A1-1, 2;A2A1-2	(MPU) Address/Data (bits 0 through 19). These signals are the time-multiplexed memory I/O address and data bus output from the MPU. These bits are also input for data.
ADIS-0	J357;A8-2	Address Disable. ADIS-0 is a square pin test signal on J357-3. When ADIS-0 is tied low, the address outputs of the 2911 state sequencer chips will be tri-stated.
ADR0-1 thru ADR19-1	A2A1-2;A4A1-1, A6-1, A7A1-1, A8-1, A9-4, A10-6	(System) Address (bits 0 through 19). These are the system bus address lines.
AIOWC-0	A2A1-2;A2A1-1, A8-1, A9-4	Advanced I/O Write Command. This signal gives system bus I/O devices early indication of a write instruction. The timing is the same as a read command.
ALE-1	A2A1-2;A2A1-1	Address Latch Enable. ALE-1 strobes an address into the ADE block. It also synchronizes the Microprocessor Timing Generator, and de-glitches the ROM bank decoder.
ALL-1	A8-5;A8-5 (Internal to the schematic)	Output of the index control register. This causes the pixel write logic to generate a PWRT-0 on the Display Bus for every PRQST-1.
AMWC-0	A2A1-2;A2A1-1, A6-1	Advanced Memory Write Command. AMWC-0 gives early indication of a write instruction to the system bus memory. The timing is the same as a read command — MRDC.
AWT-0	A2A1-1;A2A1-2, 4, 5	Advanced Write. This is the advanced write command to all on-board devices. AWT-0 is derived from the MPU status lines and the Microprocessor Timing Generator.
BANK0-0	A8-5;A8-5 (Internal to the schematic)	Output of the index control register. This signal selects which bank of the index file is currently in use.
BANKIN-0	A6-2;A6-1	BANKIN-0 is used in the address decoding logic on the RAM Controller board to indicate the presence or absence of a RAM Array board.
BANKSELECT-1	A8-2;A8-2 (Internal to the schematic)	A signal which selects which half of the microcode ROMs to be used for the requested routine (most significant bit of the opcode).
BBCLK-1	A2A1-A;A2A1-5	Buffered Bus Clock. BBCLK is a 4.9152 MHz signal which synchronizes the bus transfer logic and is the frequency source for the Programmable Timer and (Transmit) Baud Rate Generator block. This signal is the invert of BCLK-0.
BCLK-0	A2A1-1;A2A1-1, P101	Bus Clock. BCLK-0 is the system bus clock. It is a 4.9152 MHz square wave and is used by bus devices to synchronize bus master transfers. It is also used as a stable frequency source.
BDAT3-1 thru BDAT0-1	A9-4;A9-2	Buffered 8086 data bus.
BHE-0	A2A1-1;A2A1-2	BHE-0 is a the low side of S7-1/BHE-0. BHE-0 is latched and then driven on to the system bus as BHEN-0 (see S7-1/BHE-0 and BHEN-0). BHE-0 is the local Processor board version of BHEN-0.

Signal	Source;Destination	Explanation
BHEN-0	A2A1-2;A4A1-1, A6-1	Byte High Enable. On the Processor board, BHE is latched and then driven onto the System bus as BHEN-0. BHEN-0 enables the high byte (D8-D15) on read, write, and interrupt acknowledge cycles.
BIN-1	A8-5;A8-5 (Internal to the schematic)	Beam In. This signal is the logical "AND" of XIN-1 and YIN-1. This signal tells the memory control logic that the current beam position is on the screen.
BLANK-0	A7A1-3;A7A1-1, 2	BLANK-0 is a video blanking signal from the Video Timing Generator block. BLANK-0 controls blanking during horizontal and vertical retrace.
BLOCKMOVEDEST-1	A9-1;A9-2 A10-1;A10-2, 3	Block Move Destination. The BLOCKMOVEDEST-1 signal is high during a vector cycle called Block Move Destination.
BMA-0 thru BMC-0	A1-2;P43	Bus Master A thru C. Used with a factory test fixture (for test purposes only).
BMP0-0 thru BMP2-0	A9-1;A9-2 A10-1;A10-2, 3	Buffered bus signals of MP0-0 through MP2-0.
BPRN-0	J104;A2A1-1	Bus Priority In. BPRN is a signal from the bus priority logic on the Mother board that informs a potential bus master board that it has permission to become bus master.
BREQ-0	A2A1-1;A1-2	Bus Request. BRQ is a signal from a potential bus master board to the bus priority logic on the Motherboard that indicates that the potential bus master board needs to become the actual bus master.
BUSAEN-0	A2A1-1;A2A1-2	Bus Address Enable. BUSAEN-0 indicates that a board is bus master of the system bus. BUSAEN-0 is input to the Address enable of the bus controller chip, as well as an enable to the address drivers. BUSAEN-0 enables the bus controller to output the bus commands MRDC, MWTC, AMWC, IORDC, etc. BUSAEN-0 is gated with INTA and input to the INTA input of the programmable interrupt controller.
BUSGRT-0	P104;A2A1-1	Bus Grant. BUSGRT-0 acts as a preset for the bus transfer logic, causing BUSY-0 to be output.
BUSGRT-1	A2A1-1;A2A1-5	Bus Grant. This signal is similar to BUSAEN, but has a slight timing difference. This signal enables data to be latched onto the data lines.
BUSY-0	A8-2;A8-2 (Internal to the schematic)	Output of the opcode flag. This signal is set true by an I/O write to the opcode register and set false by the state sequencer (signal CBUSY-0). This flag can be tested by the state sequencer and is used to start execution of the micro-opcode routine as requested through opcode.
BUSY-0	A2A1-1;A2A1-1	BUSY-0 indicates that a bus master is currently using the system bus. BUSY-0 delays bus master transfer until the current bus master is done.

Signal	Source;Destination	Explanation
BVCLK1-1	A8-3;A8-1, 2	Buffered vector clock from the Display Bus (buffers VCLK-0).
BVCLK2-1	A8-3, A8-1, 4, 5	Buffered vector clock from the Display Bus (buffers VCLK-0).
BVCLK3-1	A8-3;A8-4	Buffered vector clock from the Display Bus (buffers VCLK-0).
BVCLK4-1	A8-3;A8-2	Buffered vector clock from the Display Bus (buffers VCLK-0).
C2-1, C1-1, & C0-1	A8-2;A8-5	Counter. These signals act as a three bit control field from the state controller. These signals then select the mode for the counter control logic.
CAS-0	A6-1;A6-2 A4A1-1;A4A1-2	Column Address Strobe. This signal is generated by the Dynamic RAM Controller on both RAM/ROM and the RAM Controller boards. CAS-0 strobe the seven multiplexed column address bits appearing on RA0-1 thru RA6-1 (RAM address lines) on the RAM Array board.
CAS-1	A7A1-2;A9-1, A10-1	From RAM timing block. Column address strobe for the RAMs.
CAS0-1 thru CAS4-0	A9-1;A9-3 A10-1;A10-4, 5	Column Address Strobes for RAM.
CATHODE	A12-1;CRT	Ties cathode of crt to ground.
CBLANK-0	A7A1-3;A7A1-4	Cursor blanking. CBLANK-0 originates in the Video Timing Generator. CBLANK-0 blanks the cursor during retrace.
CBRQ-0	A2A1-1;A2A1-1	Common Bus Request. CBRQ-0 is used by potential bus masters to request bus mastership from higher priority bus masters. CBRQ-0 is generated by the Processor board along with BRQ (both of these signals are outputs of the same flip-flop). The Processor board then listens to CBRQ-0 and gives up the bus when another board asserts CBRQ-0.
CBUSY-0	A8-2;A8-3	Clear Busy flag. This state controller signal clears the busy flag that is set by writing an opcode to the Vector Generator.
CBUSY-0	P286;A7A1-1	(Hard) Copy Busy. From the Hard Copy Unit. Indicates that the HCU is busy making a copy.
CCREAD-0	A8-1;A8-5	Decoded read strobe for the index control register (at address F71A).
CDAT-0	A8-2;A8-5	Clear New Data flag. This state controller signal clears the New Data flag that is set by an I/O write to the Index file.
CLK-1	A2A1-1;A2A1-2	Clock. CLK-1 is a direct output of the Clock Generator IC. It outputs a 4.9152 MHz square wave with a one third duty cycle. All blocks that must be synchronized with the local processor bus use this signal.
CLKDIS-0	P129;A4A1-1 P166;A6-1	Clock Disable. A TTL logic low level applied to this input pin disables the clock circuitry on the RAM/ROM or the RAM Controller board. (This is a test point for factory use only).

Signal	Source;Destination	Explanation
CLR1-0	A8-1;A8-2, 5	Buffered reset signal which is the "OR" of (1) the bus reset (RESET-0), (2) the square pin reset (INIT-0), and, (3) the software reset (io write to address F71E).
CLR2-0	A8-1;A8-2	Buffered reset signal which is the "OR" of (1) the bus reset (RESET-0), (2) the square pin reset (INIT-0), and, (3) the software reset (io write to address F71E).
CLR3-0	A8-1;A-4, 5	Buffered reset signal which is the "OR" of (1) the bus reset (RESET-0), (2) the square pin reset (INIT-0), and, (3) the software reset (io write to address F71E).
CMD-1	A2A1-4;A2A1-5	Command. CMD-1 is the logical OR of RD and AWT on the Processor board.
CNT1READ-0	A8-1;A8-2	Decoded read strobe for the 12-bit counter (at address F70E).
COL-1	A7A1-2;A9-3, A10-4	From RAM timing, controls the ROW/COLUMN address multiplexer on the Raster Memory board.
COMINT-0	A2A1-5;A2A1-2	Communications Interrupt. COMINT-0 is the RS-232 Communications Interface received character interrupt signal. Other RS-232 interrupts are included in the TIMERINT signal.
CSR-0	A8-2;A8-5	Clear Shift Register flag. This state controller signal clears the new shift register flag (the flag is set by an I/O write to SR1).
CTS-1	P102;A2A1-5	Clear To Send. CTS-1 is an RS-232 status input.
CURCLK-1	A7A1-2;A7A1-4	Cursor clock. CURCLK-0 originates in the Pixel Timing block and serves to clock the Cursor Video D flip-flop.
CURSYNC-0	A7A1-1;A7A1-4	Cursor syncronizing pulse. CURSYNC-0 originates in the pixel timing block and serves to keep the cursor syncronized to the pixel timing.
D0-1 thru D19-1	A9-2;A9-3 A10-3;A10-5	20 bits of RAM memory input data.
D15-1 thru D0-1	A2A1-2;A2A1-3, 4, 5 A8-1, 2, 3, 4, 5	(Local) Data (Bus). These lines are the local data bus for the Processor board and the Vector Generator board.
DAC0-1 thru DAC3-1	A9-4;A7A1-4	Digital/analog converter signals.
DAT0-1 thru DAT15-1	A2A1-2, A4A1-2, A4A1-3, A6-2, A7A1-1, 4, A8-1, A9-1, 4, A10-1, 2, 3, 6	(System) Data (Bus). These lines are the system data bus. (Bidirectional on most boards).
DCD-1	P102;A2A1-5	Data Carrier Detect. DCD-1 is an RS-232 status input.
DCLK-1	A7A1-2;A9-4, A10-6	Dot (or dash) Clock. 25 Hz Clock for dot (or dash) pattern. Originates in Master Clock block of the Video Controller board.
DCRY-1	A7A1-2;A7A1-3	Dot carry clock. From the Pixel Timing block. DCRY-1 is the master clock for the CRT controller IC.

Signal	Source;Destination	Explanation
DDA-0	A8-2;A8-3	Slope Generator Enable. This is a state sequencer signal which allows the slope generator to function.
DIN15-1 thru DIN0-1	A4A1-2;A5-1 A6-2;A5-1	Data In bits 0 through 15. During RAM write operations, these 16 data bits contain the data that is written to RAM on the RAM Array board.
DINLSB-0	A6-1;A6-2	Data Input Enable Least Significant Byte. During RAM write operations, DINLSB-0 enables the data input buffer for the least significant byte of data to drive data from the bus onto RAM data lines DIN7-1 thru DIN0-1 to the RAM Array boards.
DINMSB-0	A6-1;A6-2	Data Input Enable Most Significant Byte. During RAM write operations, DINMSB-0 enables the data input buffer for the most significant byte of data to drive data from the bus onto RAM data lines DIN15-1 thru DIN8-1 to the RAM Array boards.
DOUT-0	A6-1;A6-2 A4A1-1;A4A1-2	Data Output Enable. During RAM read operations, DOUT-0 enables the Data Output Latches to output their data to the system bus.
DOUT15-1 thru DOUT0-1	A5-1;A4A1-2 A5-1;A6-2	Data Output bits 0 through 15. These 16 data bits from the RAM Array board contain the RAM data output bits during RAM read operations.
DSR-1	P102;A2A1-5	Data Set Ready. DSR-1 is an RS-232 status input.
DT-1/R-0	A2A1-2;A2A1-4	Data Transmit/Receive. DT-1/R-0 is a direct output of the bus controller. A high on this line indicates a WRITE to I/O or memory and a low is a READ.
DTR-1	A2A1-5;P102	Data Terminal Ready. DTR-1 is an RS-232 status output.
DY-1	A9-4;A9-4 (Internal to the schematic)	Border latch output bit.
DYENB-0	A8-2;A8-4	Delta Y Enable. This state controller signal selects the Delta Y counter instead of the Y counter to send to the Display Bus.
EARLYCARRY-0	A7A1-2;A7A1-3	Early Dot Carry clock. Early Dot Carry clock from the Pixel Timing block. EARLY-CARRY-0 is used to help generate the PAUSE-1 signal.
EBLANK-0	A7A1-3;A7A1-4	ECL blank. From the Video Timing block. EBLANK-0 is the ECL level composite blanking signal.
ECLR-0	A7A1-2;A7A1-4	ECL generated clear pulse. Clear pulse from the RAM Timing. ECLR-0 is used to control Y-cursor blanking.
ENB12-0	A8-2;A8-2 (Internal to the schematic)	Enable 12-Bit Counter. A state controller signal which enables the 12-bit counter to decrement.

Signal	Source;Destination	Explanation
ENB8-0	A8-2;A8-1	Enable 8-Bit Counter. This state controller signal allows the 8-bit counter to decrement.
EQ-1	A10-2;A10-3	A-B line from the ALU ICs on the Dual Plane Raster Memory board. This signal is used to generate EQUAL-1 (see EQUAL-1).
EQUAL-1	A9-2, A10-3, A8-2	EQUAL-1 is a signal to the Vector Generator board indicating that both input ports of the raster ALU are equal (provided the ALU mode is set to XNOR).
ESYNC-0	A7A1-3;A7A1-4	ECL synchronization pulse. ESYNC-0 is an ECL level composite video syncronization pulse from the Video Timing block to the DAC.
EXLD-0	P281;A7A1-3	Causes CRT controller to go through self-booting sequence.
EXT-0	J382;A9-2, A10-2	Not currently used.
FIRST-0	A8-1;A8-5	This signal is true after the X axis counter is loaded and it goes false when the X axis is counted. It is used to identify the first column of a wipe or blockmove.
FLYBACK SIGNAL	A12-1;A13-1	FLYBACK SIGNAL returns the beam to its starting point after a horizontal and/or vertical sweep.
FMAT-0 & FMAT-1	A8-2;A8-2 (Internal to the schematic)	Format. A state controller signal that controls which latches the micro-code ROM data will be latched into.
HSYN-1	A7A1-3;A7A1-4	Horizontal video synchronization pulse. HSYN-1 is used to synchronize the monitor (J361 must be in place).
HSYNC-0	A7A1-3;A12-1	Horizontal video synchronization pulse. Invert of HSYN-1.
HORIZ SYNC	A7A1-3;A12-1	HORIZ SYNC is derived from the HSYNC-0 pulse on the Video Conroller board and is used to control the timing of the left to right scan and return of the beam on the crt.
IDIS-0	J357;A8-2	Instruction Disable. IDIS-0 is a square pin test signal on J357-2. When IDIS-0 is tied low, the outputs of the micro-opcode decoder ROM will be tristated.
IN-0	A4A1-2;A5-1	IN-0 is used with OUT-0 to indicate the presence or absence of a RAM Array board.
INH-0	A8-5;A8-5 (Internal to the schematic)	Inhibit. The ZERO-0 signal from the 12-bit counter qualified by the ZENB-0 signal from the state controller. INH-0 serves to inform the counter control and memory control logic of the end of a vector.
INH-0	A6-1;A4A1-1	(Read) Inhibit. When true low, INH-0 inhibits memory circuitry from placing its data onto the system bus while memory circuits are reading data (see INHIBIT-0). INH-0 may be output by test circuitry. INH-0 is not currently used.
INHIBIT-0	A4A1-1;A4A1-3	This signal is a buffered version of the system bus signal INH-0. When true low, it inhibits the RAM/ROM board from outputting its data during RAM read or ROM read operations.

Signal	Source;Destination	Explanation
INIT-0	A14-1;A2A1-1, 4, A8-1, A7A1-3	Initialize. INIT is used to generate reset which goes directly to the MPU and does a power-up reset operation. It also resets much of the sequential logic on the Processor board, as well as reseting logic on the Video Controller and Vector Generator boards.
INT-0	A7A1-1;P280	Interrupt request.
INT0-0 thru INT7-0	[a];A2A1-2	Interrupt 0 through 7. INT0-1 thru INT7-0 are interrupt request signals to the Processor board. INT0-0, INT4-0, or INT5-0 can be generated by processor board devices.
INTA-0	A2A1-1;A2A1-1, 2	Interrupt Acknowledge. INTA-0 informs the Programmable Interrupt Controller that its interrupt is acknowledged and it can put vectoring data on the system data bus.
INTA-0	A2A1-2;A2A1-1, 2	Interrupt Acknowledge. INTA-0 is generated on the Processor board and is received by slave programmable interrupt counters (PICs) on other boards. INTA-0 notifies the slave PIC that its interrupt is acknowledged and it can put vectoring data on the system data bus.
INTERNAL-0	A9-2;A9-1 A10-2;A10-1, 3	Indicates where the input data for the B side of ALU comes from. 0 says data is from internal PDAT latches. 1 says data comes from an off board source. Always zero in the 4112 since there are no outside sources.
INTERNAL-1	A10-2;A10-3	INTERNAL-1 is the invert of INTERNAL-0. It acts in the same manner as INTERNAL-0 but is not currently used.
INTR-1	A2A1-2;A2A1-1	Interrupt. INTR-1 is a direct output of the INT pin of the programmable interrupt counter in the Interrupt Controller block. The signal is input directly to microprocessor INTR input. INT is the interrupt to the microprocessor.
IORC-0	A2A1-2;A7A1-1, A8-1, A9-4, A10-6	I/O Read Command. This signal when low indicates that an I/O device should drive its data onto the system bus.
IOWC-0	A2A1-2;A7A1-1, A8-1, A9-4, A10-6	I/O Write Command. This signal when low indicates that an I/O device should read data on the system bus.
K19-1 thru K0-1	A10-2;A10-4	K19-1 thru K0-1 on the Dual Plane Raster Memory board has the same function as D19-1 thru D0-1 (data for the plane 0 memory array).
KA0-1 thru KA3-1	A2A1-4;A3-1	Keyboard Address 0 through 3. These signal lines carry key matrix column addresses in addition to LED address and on-off information.
KBDINT-0	A4A1-4;A4A1-2	Keyboard Interrupt. This signal is the interrupt for the keyboard. It is output from pin 24 of the peripheral interface microprocessor and input to the Interrupt Controller block as INT4 into the programmable interrupt counter.

[a] From all boards in system.

Signal	Source;Destination	Explanation
KBT1-1	P104;A2A1-4	Keyboard Test. KBT is the test input to the MPU Keyboard Controller.
KD0-1 thru KD7-1	A3-1;A2A1-4	Keyboard Data 0 through 7. These lines carry key matrix data in addition to thumbwheel Grey code data.
KSTRB-0	A2A1-4;A3-1	Keyboard Strobe. KSTRB-0 latches KA0-1 thru KA3-1 data into the Keyboard board circuitry.
KWR-0	A2A1-4;A3-1	Keyboard Write. KWR latches KA0-1 thru KA3-1 into the Keyboard circuitry that controls the LEDs.
L19-1 thru L0-1	A9-2;A9-4 A10-3;A10-6	Latch pixel data bits to the processor read latches. The bits are then latched in the block move latch for a processor read.
LAST-0	A8-1;A8-2, 5	Zero count signal for the 8-bit counter.
LATCH-0	A9-1;A9-2	A low holds the previous RAM cycle output data in the block move latches. This data can then be used for the destination cycle of the block move.
LBHE-0	A2A1-2;A2A1-4	Latched Byte High Enable. LBHE-0 is the Processor board equivalent of the system bus signal, BHEN (Byte High Enable).
LINESYNC-0	A7A1-3;A7A1-2	LINESYNC-0 synchronizes the pixel timing to the video scan line.
LOADdelY-0	A8-1;A8-4	Decoded write strobe for delta Y axis register (at address F708).
LOAD-1	A7A1-2;A9-4, A10-6	Load enable for video shift registers.
LOADAXIS-0	A8-1;A8-3	Decoded write strobe for slope generator axis control register (at address F704).
LOADCC-0	A8-1;A8-5	Decoded write strobe for the index control register (at address F71A).
LOADCNT1-0	A8-1;A8-2	Decoded write strobe for 12-bit counter (at address F70E).
LOADCOL-0	A8-1;A8-5	Decoded write strobe for the index file (at address F718).
LOADMASK-0	A8-1;A8-5	Decoded write strobe for the mask file (at address F71C).
LOADOP-0	A8-1;A8-2	Decoded write strobe for the OPCODE register (at address F714).
LOADRA-0	A8-1;A8-3	Decoded write strobe for slope generator RA register (at address F702).
LOADRX-0	A8-1;A8-3	Decoded write strobe for slope generator RX register (at address F700).
LOADRY-0	A8-1;A8-3	Decoded write strobe for slope generator RY register (at address F706).
LOADSR1-0	A8-1;A8-5	Decoded write strobe for shift register 1 (at address F710).
LOADSR2-0	A8-1;A8-5	Decoded write strobe for shift register 2 (at address F712).
LOADX-0	A8-1;A8-4	Decoded write strobe for the X axis register (at address F70C). (NOTE: There is another signal called LOADX-0 on the Video Controller board, see second definition.)

Signal	Source;Destination	Explanation
LOADX-0	A7A1-1;A7A1-4	Load the X-Cursor register.
LOADX-1	A8-4;A-5	A positive logic version of the decoded write strobe for the X axis register (at address F70C).
LOADY-0	A8-1;A8-4	Decoded write strobe for the Y axis register (at address F70A). NOTE: There is another signal called LOADY-0 on the Video Controller board, see second definition.
LOADY-0	A7A1-1;A7A1-4	Load the Y-Cursor register.
LOCK-0	A2A1-1;A2A1-1, J104	If LOCK-0 is low, it indicates that other system bus masters may not take control of the bus from the Processor board. This signal is manipulated by a "lock" prefix to any firmware instruction.
LS2-0 thru LS0-0	A2A1-2;A2A1-1, 3, 5	Latched Status 0 through 2. These signals are the latched outputs of the MPU S0 — S2 signals. S0 — S2 indicate what state the MPU is in: interrupt acknowledge, read I/O, write I/O, halt, code access, read memory, or write memory.
M-1	A9-2;A9-4	A pull-up line to + 5 volts.
M1-1 & M0-0	A8-2;A8-5	Two state sequencer signals which, after buffering through two levels of latches, become MODE0-0 and MODE1-0 on the Display Bus.
MAKECOPY-0	A7A1-1;HCU	Caused by the host or the Hard Copy Key going low. Initiates hard copy cycle (makes a copy). Requires ground closure of TTL low for more than 1 ms.
MAP-0	A8-2;A8-2 (Internal to the schematic)	Output of the micro-opcode decode ROM which enables the outputs of the opcode register.
MAP-0	A9-4;A7A1-4, A10-6	Map write select. MAP-0 acts to disable the VID3-1 output as the map is being written.
MC2-1, MC1-1, & MC0-1	A8-2;A8-5	Memory Control. These signals act as a three-bit control field from the state controller. These signals then select the mode for the memory control logic.
MDEN-1	J104;A2A1-3	Memory Data Enable. When driven low, this signal disables data drivers on the Processor board.
MODE0-1 and MODE1-1	A8-5;A9-1, A10-1	The four states of these "mode bits" define the memory cycles as follows: 00 (0) defines operate, 01 (1) defines block move from source, 10 (2) defines blockmove to destination, and 11 (3) defines processor read cycles. NOTE: MODE0-1 is the least significant bit.
MP4-0 thru MP0-0	A8-5;A9-1, A10-1	Pixel (addressable latch) address for memory planes. MP4-0 thru MP0-0 originates in the Vector Generator board and is used to latch the PDAT bits and RAS mask for a 20-bit RAM word. During a block move, the address lines become five lines that mask the five zones in a 20-bit word.
MRDC-0	A2A1-2;A2A1-1, A4A1-1, A6-1	Memory Read Command. MRDC-0 instructs memory to release data to the system bus.

Signal	Source;Destination	Explanation
MRQST-0	A8-5;A8-5 (Internal to the schematic)	Memory Request. A signal from the memory control logic that requests a vector generator memory cycle. This signal becomes the Display Bus signal VRQST-0 after passing through a buffer latch.
MVIDEO	A7A1-4;A12-1	Monitor video signal. MVIDEO is the output taken from the four digital to analog converter lines DAC0-1 thru DAC3-1. MVIDEO becomes the VIDEO signal line on the Deflection Amplifier board.
MWTC-0	A2A1-2;P101	Memory Write Command. This signal indicates that memory should latch and store data on the system bus.
MX0-0 thru MX4-0	A7A1-3, A8-4;A9-3, A10-4	Multiplier X axis data. Latched data to the Memory Address Selector.
MY0-0 thru MY8-0	A7A1-3, A8-4;A9-3, A10-4	Multiplier Y axis data. Latched data to the Memory Address Selector.
N19-1 thru N0-1	A10-2;A10-6	N19-1 thru N0-1 on the Dual Plane Raster Memory board has the same function a L19-1 thru L0-1 on the Single Plane Raster Memory board (pixel data bits; see L19-1 thru L0-1).
NEWDAT-0	A8-5;A8-2	New Data. This signal indicates a value has been written into the index file by the 8086. It is set true by the I/O write, and set false by COAT-0.
NEWSR-0	A8-5;A8-2	New Shift Register. A Signal which indicates that an I/O write to shift register 1 has occured.
NMI-0	J104;A2A1-1	Non-Maskable Interrupt. This is the non-maskable interrupt for the 8086 microprocessor. The 4112 system does not use it, but it is available for use by a test device via J104.
NMI-1	A2A1-1;J104	Non-Maskable Interrupt. This is NMI-0 inverted.
NRFND-0	A8-5;A7A1-1, A9-1	Not ready for new data. NRFND-0 is a signal from the Vector Generator to signal that it is not ready for new data.
OBADR-0	A2A1-3;A2A1-1, 2	On-Board Address. OBADR-0 indicates that the 8086 microprocessor is accessing a device on the Processor board.
OBDEN-0	A2A1-3;A2A1-2	On-Board Data Enable. OBDEN enables the data transceivers during an on-board data access.
OBINTA-0	A2A1-2;A2A1-1, 3	On-Board Interrupt Acknowledge. OBINTA-0 indicates that the programmable interrupt counter is generating an interrupt vector address.
OBIOX&X-0	A2A1-3;A2A1-1, 2, 4, 5	On-Board I/O (select) signals. Local address lines A0, A2, and A3 select one of eight signals: OBIOD&F, OBIOC&E, OBIO9&B, OBIO8&A, OBIO5&7, OBIO4&6, OBIO1&3, and OBIO0&2. These are used to enable the RCI, PT&BRG, IC, KC, BTD, or SI blocks. These signals are selected during Processor board I/O reads and writes to X'00E0' through X'00EF'.

Signal	Source;Destination	Explanation
OBRAM-0	A2A1-3;A2A1-4	On-Board RAM. OBRAM-0 enables the CMOS RAM for a READ or WRITE operation.
OBROM-0	A2A1-3;A2A1-1	On-Board ROM. OBROM-0 enables the 32K of ROM on the Processor board for READ operations.
OUT-0	A5-1;A4A1-2, 1 A5-1;A6-2	OUT-0 is used with IN-0 to indicate the presence or absence of a RAM Array board.
OUT0-1	A2A1-5;A2A1-1	Output 0. OUT0-1 is the output of a 16-bit programmable down counter. This provides variable timing delays for the system firmware. In the bus timeout detector block, OUT0-1 clocks the bus timeout counter whose output to the system bus is ACK1.
P0-0 thru P2-0	A9-1;A9-2 A10-1;A10-2, 3	Decoded MP3-0 and MP4-0 signals used for the three addressable latch clocks.
PAUSE-1	A7A1-3;A7A1-2	Causes the 50 MHz clock to stop. PAUSE-1 enables the video controller to sync to an external sync signal.
PCARRY-0	A8-5;A8-5 (Internal to the schematic)	Pixel Carry. Carry out of the pixel counter (an input to the counter control logic).
PCLK-1	A7A1-2;A7A1-1	Power Supply synchronizer clock.
PDAT0-1	A8-5;A9-1	Raster Memory plane 0 RAM data bit input line. (PDAT0-1 is always tied high. It is reserved for future use.)
PDAT1-1	A8-5;A9-1, A10-2, 3	Raster Memory plane 1 RAM data bit input line (tied high if there is no Dual Plane Raster Memory board present).
PDAT2-1	A8-5;A9-2	Raster Memory plane 2 RAM data bit input line.
PINH-0	A8-5;A8-5 (Internal to the schematic)	Pipelined Inhibit. The PZERO-0 signal from the 12-bit counter qualified by ZENB-0 signal from the state controller. PINH-0 also serves to warn the memory control logic of the end of a vector.
PIPELINE-0	A8-2;A8-2 (Internal to the schematic)	The output of the micro-opcode decode ROM which enables the outputs of the pipeline address latch.
PIX-1/MSK-0	A8-2;A8-5	This state controller signal selects either the pixel counter or mask file data to send to the Display Bus.
PIXCNTENB-0	A8-5;A8-5 (Internal to the schematic)	Pixel Counter Enable. Output of the counter control logic. This signal enables the pixel counter to count.
PLATCH-0	A9-1;A9-4 A10-1;A10-6	Processor Latch. This latch is used to latch the pixel data into the processor read data latches.
POP8-0	A8-2;A8-1	POP the 8-bit counter value. This state controller signal loads the 8-bit counter with the value contained in its buffer latch (the last value written by I/O).
POPX-0	A8-2;A8-4	POP X Axis value. This state controller signal loads the X axis register with the last value written by I/O.

Signal	Source;Destination	Explanation
PREADH-0	A9-4;A9-4 (Internal to the schematic)	Processor Read Latch (high byte enable). A high will enable one of the three processor read latches.
PREADL-0	A9-4;A9-4 (Internal to the schematic)	Processor Read Latch (low byte enable). A high will enable two of the three processor read latches.
PRQST-1	A8-5;A8-5 (Internal to the schematic)	Pixel Request. A signal which requests a pixel write (this may or may not result in a PWRT-0 on the Display Bus, depending on the operating mode of the index file).
PSYNC-1	A7A1-1;A14-1	Power sypply sync pulse.
PWRT-0	A8-5;A9-1, A10-1	Write pulse for the data and RAS addressable latch (see ALL-1).
PZERO-0	A8-2;A8-5	Pipelined Zero. This signal is the zero count signal from the 12-bit counter delayed one clock cycle.
Q19-1 thru Q0-1	A9-3, 4;A9-2 A10-5;A10-3	Outputs of video shift registers and memory array. Acts as 20 bits of RAM output data.
QC-1	A9-4;A9-4 (Internal to the schematic)	Video output of the shift register.
QS0-1 and QS1-1	A2A1-1;J104	Queue Status 0 and 1. QS0-1 and QS1-1 are direct outputs of the microprocessor that are not used on the Processor board.
QUAL-0	A8-2;A8-2 (Internal to the schematic)	Qualifier. A State Controller signal that serves as a scope or logic analyzer trigger.
R19-1 thru R0-1	A10-4, 6;A10-2	R19-1 thru R0-1 on the Dual Plane Raster Memory board has the same function as Q19-1 thru Q0-1 on the Single Plane Raster Memory board (acts as 20 bits of RAM output data).
RA0-1 thru RA6-1	A4A1-1;A4A1-2, A5-1 A6-1;A6-2, A5-1	RAM Address bits 0 through 6. These signals are the seven multiplex row and column addresses from the dynamic RAM controller to the dynamic RAMs on the RAM Array board.
RAMWRITE-0	A4A1-1;A4A1-2	RAMWRITE-0 indicates to the Dynamic RAM Controller and the data input receivers on the RAM/ROM board that a RAM write operation has been requested.
RAS-0	A4A1-1; A4A1-2;A5-1	Row Address Strobe. RAS-0 is generated by the Dynamic RAM Controller on the RAM/ROM board. RAS-0 strobes the seven multiplexed row address bits appearing on RA0-1 thru RA6-1 into the RAMs on the RAM Array board.
RAS-1	A7A1-2;A9-1, A10-1	Row Address Strobe. RAS-1 originates in the RAM timing generator and is used to strobe the RAMs.
RAS0-0 thru RAS19-0	A9-1;A9-3 A10-1;A10-4, 5	Row Address Strobe. Strobe for the dynamic RAMs.

Signal	Source;Destination	Explanation
RAS0-0 thru RAS3-0	A6-1;A6-2	Row Address Strobe 0 through 3. These signals are generated by the Dynamic RAM Controller on the RAM Controller board. RAS0-0 thru RAS3-0 strobe the seven multiplexed row address bits appearing on RA0-1 thru RA6-1 into the RAMs on the appropriate RAM Array board (RAM Bank 0 through 3).
RCLK-1	P102;A2A1-5	Receive Clock. RCLK-1 is an RS-232 external clock signal generated by a modem or other external device. RCLK-1 can be used to clock data into the Processor board's UART.
RD-0	A2A1-1;A2A1-2, 4, 5	Read. If RD-0 is low, it indicates the microprocessor is performing an I/O or memory read cycle, either to the local or system bus.
RDATA-1	P102;A2A1-5	Received Data. RDATA-1 is the RS-232 serial data input from a modem or other external device to the Processor board.
RDIS-0	J357;A8-2	ROM Disable RDIS-0 is a square pin test signal on J357-4. When RDIS-0 is tied low, the outputs of the microcode ROMs will be tristated.
RDY-1	J104;A2A1-1	Ready. RDY-1 is the 8086 microprocessor RDY signal output to test connector J104.
RDYAND-0	J104;A2A1-1	Ready And. RDYAND-0 is an input from a test device connected to J104 that can disable the RDY line to the MPU, causing the MPU to enter a WAIT state.
RDYOR-0	J104;A2A1-1	Ready Or. RDYOR-0 is an input from a test device connected to J104 that can activate the RDY line to the MPU, causing the MPU to exit a WAIT state.
READ-0	A4A1-1;A4A1-3	READ-0 is the buffered version of the system bus signal MRDC.
REF-0	A7A1-2;A9-1, A10-1	Indicates that a screen refresh memory cycle is taking place.
RENB-0	A7A1-2;A7A1-3	Enable signal for screen refresh Memory Buffer.
RESET-0	A7A1-3;A7A1-1, 4 J357;A8-1	Logic reset pulse. RESET-0 is generated when INIT-0 is received from the 8086 bus. RESET-0 also appears on J357-5 and can be used to reset the logic on the Vector Generator board.
RING-1	P102;A2A1-5	RING-1 is an RS-232 status input indicating that an auto-answering modem is ringing.
ROMREAD-1	A4A1-3;A4A1-1	ROMREAD-1 indicates that a ROM read operation is in progress. This signal is used to generate an acknowledge signal (ACK1 or ACK2) to the bus master.
RQ-0/GT[0/1]-0	A2A1-1;J104	Request/Grant. RQ/GT0 is the local MPU bus request/grant signal. It is available to J104 test connector, but is not used on-board.
RST-0	A2A1-1;A2A1-2, 4, 5	Reset. RST-0 is RST-1 inverted (see RST-1).

Signal	Source;Destination	Explanation
RST-1	A2A1-1;A2A1-5	Reset. RST is derived from the system bus signal INIT-0 and is synchronized to the MPU clock. RST resets the MPU and other devices on the Processor board.
RTS-1	A2A1-5;P102	Request To Send. RTS-1 is an RS-232 signal generated by the RS232 Communications Interface block on the Processor board.
S0-0 thru S2-0	A2A1-1;A2A1-2	Status 0 through 2. These status lines have eight states taken together and indicate whether an interrupt acknowledge read I/O, write I/O, halt, code access, read memory, or write memory is occurring. The bus controller IC in the Bus Command Driver block interprets the S0-0, S1-0, and S2-0 signals and outputs INTA, IOWC, AIOWC, IORC, MRDC, MWTC, AMWC accordingly.
S7-1/BHE-0	A2A1-1;A2A1-2	Status 7/Byte High Enable. This signal is interpreted as BHE-0 during the MPU state T1. It enables D8 — D15 onto the local data bus. During T2, T3, or T4 this signal is interpreted as S7-1.
SACK-0	A8-1;A7A1-1, A9-1	Synchronized system acknowledge. SACK-0 originates at the Vector Generator board and is used to syncronize the I/O writes from the 8086 to the Vector Generator state machine.
SCANSYNC-1	A7A1-2;P281	Scan sync pulse. SCANSYNC-1 originates in the Pixel timing block and is used on the External Video board to syncronize the horizontal scanning of the External Video board with the Video Controller.
SDCD-1	P102;A2A1-5	Secondary Data Carrier Detect. SDCD-1 is the RS-232 secondary data carrier detect signal.
SENSE-1	A8-2;A8-2 (Internal to the schematic)	A state controller signal that controls the sense (inversion) of the selected test condition.
SHIFTENB-0	A8-5;A8-5 (Internal to the schematic)	Shift Enable. Output of the counter control logic. This signal enables the pattern shift registers to rotate.
SINIT-0	A8-1;A8-2	System initialize. Reset for the state sequencer. This is the logical "OR" of the (1) bus reset (RESET-0) and (2) software reset (I/O write to address F71E) signals.
SLOW-0	A7A1-3;A7A1-2	Causes the DCRY-1 signal to go at one half the normal rate (for external scan time during vertical sync).
SR1READ-0	A8-1;A8-5	Decoded read strobe for shift register 1 (at address F710).
SR2READ-0	A8-1;A8-5	Decoded read strobe for shift register 2 (at address F712).
SRTSA-1	A2A1-5;P102	Secondary Request To Send (RS-232A). SRTSA-1 is the RS-232A secondary request to send output. SRTS is defined on a different connector pin for RS-232C, and so is strappable on the board.
SRTSC-1	A2A1-5;P102	Secondary Request To Send (RS-232C). SRTSC-1 is the RS-232C counterpart to SRTSA-1 above.

Signal	Source;Destination	Explanation
STATEN-0	A2A1-5;A2A1-1	Status Enable. STATEN-0 is low during an MPU read of status at I/O location X'00ED' or X'00EF'.
STEST-0	A14-1;A2A1-5, A7A1-3	Self Test. STEST-0 is a line on the system bus which the processor can read via a 3-state driver. The line is low when the Self-Test button is pressed.
T3W4-1	A2A1-1;A2A1-3	(State) T3, Wait, 4 T3W4-1 is high when the MPU is in a T3, T4, or TW (WAIT) state. T3W4-1 enables on-board data transceivers.
T4I-0	A2A1-1;A2A1-3	(State) T4, Idle. T4I-0 is low during MPU T4 and TI (idle) states. It turns off data transceivers during T4 in on-board memory and I/O READs.
TBLANK-0	A7A1-3;A7A1-2	TTL level composite blank.
TCLK-1	P102;A2A1-5	Transmit Clock. TCLK-1 is the RS-232 transmit clock output from the Processor board.
TDATA-1	A2A1-5;P102	Transmitted Data. TDATA-1 is the RS-232 signal on which serial data is transmitted from the Processor board.
TEQ-1	A8-2;A8-2 (Internal to the schematic)	Test Equal. A state controller signal that allows the EQUAL-1 signal from the Display Bus to be tested by the state controller (used by the video memory test).
TEST SIG	P586;A12-1	TEST SIG causes a blank illuminated screen. TEST SIG comes from the Video Controller board under the name of STEST-0 (self test).
TEST-0	J104;A2A1-1	TEST-0 is an input to the processor. It is available at pin 50 on the test connector, but is not used on-board (see second definition).
TEST-0	A7A1-1;A8-5, A9-1, A10-1	TEST-0 puts the Raster Memory boards into test mode.
TEST-1	A2A1-5;A2A1-1	TEST-1 is a signal that the processor can set to enable the Clock Generator to locally terminate an on-board or off-board READ or WRITE operation. The signal is used for testing purposes, and is similar in function to the Bus Timout Detector circuit.
TESTCONDITION-1	A8-2;A8-2 (Internal to the schematic)	The output of the test condition mux, test gate, and delay flip-flop that acts as an input to the micro-opcode decode ROM. This signal allows conditional opcodes to "make a choice" between two actions.
TF1-0 & TF2-0	A8-5;A8-2	Test Flags 1 & 2. Two general purpose flags from the high byte of the index file register. These signals are used by the 8086 to direct the Vector Generator during some routines. These flags can be tested by the state controller.

Signal	Source;Destination	Explanation
TIMERINT-0	A2A1-5;A2A1-2	Timer Interrupt. TIMERINT-0 indicates the presence of either a Programmable Interval timer1 interrupt, a UART TXEMT interrupt, a UART TXRDY interrupt, an RS-232 status change interrupt, or an Programmable Interval TIMER0 interrupt (via RSCD).
TIMR1-1	A2A1-5;A2A1-1	Timer 1. This signal is output from the O1 output (pin 13) of the Programmable Interval Timer. O1 is the output of a 16-bit programmable down counter.
TXC-0	A2A1-5;P102	Transmit Clock. TXC is the buffered output of the Programmable Interval Timer 1 to the RS-232 connector. It is not presently used.
UBCLK-1	A2A1-1;A2A1-4, 5	Unbuffered Bus Clock. UBCLK-1 is a 4.9152 MHz square wave clock provided to clock the UART and peripheral interface microprocessor.
VACK-0	A7A1-2;A9-1, A10-1	Acknowledges that a memory cycle has been granted.
VBUSY-0	A8-2;A9-1	Vector Generator busy.
VCLK-0	A7A1-2;A8-3, A9-1	Clock for the Vector Generator.
VDRIVE-0	A9-1;P381	Tied high if no External Video board is installed.
VENB-0	A7A1-2;A8-4, A9-1, A10-1	Enables the Vector Generator memory address buffers.
VENB-1	A9-1;A9-2 A10-1;A10-2, 3	Vector Enable. VENB-1 is high when the RAM cycle is doing any type of Vector Generator function.
VERT SYNC	A7A1-3;A12-1	VERT SYNC controls the timing of the vertical scan and return of the beam on the crt. VERT SYNC is a direct line from VSYNC-0 on the Video Controller board.
VGADR-0	A7A1-1;A8-1, A9-4, A10-6	The decoded most significant five bits of the raster I/O Address.
VGRDY-1	P280;A7A1-1	Vector Generator ready status signal.
VID3-1	A7A1-4;P281	Video bits.
VID3-1 thru VID0-1	A7A1-4, A9-4;A10-6	Video Controller board cursor video output (VID3-1) and Raster Memory planes data bit input lines.
VIDEO	A7A1-4;HCU	Hard copy video signal.
VIDEO	A7A1-4;A12-1	VIDEO turns the crt electron beam on or off and controls the grey scales. VIDEO is a direct line from MVIDEO on the Vector Generator board (see MVIDEO).
VRQST-0	A8-5;A7A1-2, A9-1	Request from the Vector Generator to the Video Controller for a memory cycle.
VSYNC-0	A7A1-3;A7A1-1, P281	Vertical synchronizing signal.
VTIME-0	A7A1-1;A7A1-4	Vertical retrace time.
W1-0 thru W4-0	A9-1;A9-3 A10-1;A10-4, 5	Write pulse for RAMs.

Signal	Source;Destination	Explanation
WAIT-1	A8-2;A8-1	This state controller signal can delay the syncing of the write pulse. If the write pulse is delayed by WAIT-1 this delays SACK-0, thereby delaying the acknowledge to the 8086. This operation can allow the Vector Generator to sync the 8086 to the Vector Generator operation.
WALU0-0	A9-4;A9-1, 2 A10-6;A10-1, 2, 3	A clock pulse that latches the ALU mode latch and the write enable latch.
WBORDER-0	A9-4;A9-4 (Internal to the schematic)	Write Border Latch. Output of I/O Decode section. This signal acts as a clock for the flip-flop of the video shift register.
WELSB-0	A4A1-1;A4A1-2, A5-1 A6-1;A6-2, A5-1	Write Enable Least Significant Byte. WELSB-0 is a control strobe to the RAM Array board indicating that a write operation to the least significant byte of RAM is in progress.
WEMSB-0	A4A1-1;A4A1-2, A5-1 A6-1;A6-2, A5-1	Write Enable Most Significant Byte. WEMSB is a control strobe to the RAM Array board indicating that a write operation to the most significant byte of RAM is in progress.
WENB-1	A9-1;A9-4 A10-1;A10-6	Write Enable status bit for Self-Test. Output of flip-flop in the RAM control section.
WR-1	A7A1-2;A9-1, A10-1	WR-1 originates in the RAM timing generator and is the write enable signal for the RAMs.
WWENB-1	A10-1;A10-6	Write enable status bit for Self-Test. Output of flip-flop in the RAM control section. WWENB-1 is only used on the Dual Plane Raster Memory board and corresponds to WENB-1.
X19-1 thru X0-1	P382;A9-2, A10-3	Not currently used.
XACK-0	A4A1-1;A4A1-2 A6-1;A6-2	Transfer Acknowledge. The Dynamic RAM Controller generates XACK-0 to acknowledge that a RAM read or write operation is in progress. This signal latches the RAM output data into the data output latches.
XCARRY-0	A8-4;A8-5	Carry out of the X register.
XCLK-0	P129;A4A1-1 P166;A6-1	External Clock. When the clock circuitry is disabled using CLKDIS-0, an external TTL clock signal may be fed into XCLK to control the Dynamic RAM Controller (this is a test point for factory use only).
XCNTENB-0	A8-5;A8-1, 4	X Counter Enable. This is a state controller signal that enables the X axis register to count and causes the first signal to go false.
XEN-0	A9-1;A7A1-3, A7A1-1	External sync mode enable. From the External Video board to the Video Controller board. XEN-0 is tied high if there is no External Video board in place.
XENB-1	A3-3;A8-5	X Enable. The slope generator output that signifies that the X axis should be counted on the next cycle. This signal interfaces with the counter control logic.
XHSYNC-0	A9-1;A7A1-3	External horizontal sync. From the External Video board to synchronize the Video Controller's horizontal sync to an external source. Tied high if there is no External Video board attached.

Signal	Source;Destination	Explanation
XIN-1	A8-4;A8-5	A signal that means that the 3 most significant bits of the X axis register are zero. This signifies that the X position is in the physical screen.
XLD-0	A8-4;A8-1, 5	X Load. This signal loads the X axis counter and Pixel counter with the value in the buffer latch (the last value written by I/O). It also sets FIRST-0 true.
XLOAD-0	P381;A9-1	External sync pulse change signal (not currently used).
XNEXT-0	A8-3;J350	Inverted XENB-1 signal (for test purposes).
XREAD-0	A8-1;A8-4, 5	Decoded read strobe for the X axis register (at address F70C).
XSIGN-0	A8-3;A8-4, 5	Signal from the axis control register that determines which direction the X counter will count.
XSIGN-1	A8-3;J350	Inverted version of XSIGN-0 (for test purposes).
XTRA-1	A5-1;none	Extra. XTRA-1 is an extra line of the RAM Array board that is currently not used.
XVSYNC-0	A9-1;A7A1-3	External vertical sync. From the External Video board to syncronize the Video Controller board's vertical sync to an external source. Tied high if there is no External Video board installed.
Y19-1 thru Y0-1	P402;A10-2	Not currently used.
Y-1/-0	A8-2;A8-4	This is a state sequencer signal that selects either the Y axis or delta Y axis to be sent to the Display Bus.
YCNTENB-0	A8-5;A8-4	Y Counter Enable. Output of counter control logic which enables the Y axis register to count.
YENB-1	A8-3;A8-5	Y Enable. The slope generator output that signifies the Y axis should be counted on the next cycle.
YIN-0	A8-4;A8-5	A signal that means that the 3 most significant bits of the Y axis register are zero. This signifies that the Y position is in the physical screen.
YNEXT-0	A8-3;J350	Inverted YENB-1 signal (for test purposes).
YREAD-0	A8-1;A8-4	Decoded read strobe for the Y axis register (at address F70A).
READ-0	A8-1;A8-4	Decoded read strobe for the delta Y axis register (at address F708).
YSIGN-0	A8-3;A8-4	Signal from the axis control register that determines which direction the Y and delta Y counters will count.
YSIGN-1	A8-3;J350	Inverted version of YSIGN-0 (for test purposes).
ZENB-0	A8-2;A8-5	Zero Enable. This state controller signal enables two zero detect signals (ZERO-0 and PZERO-0).
ZERO-0	A8-2;A8-5	This signal indicates the 12-bit counter is zero. Testable by the state controller and also used to end a vector through hardware.

Appendix B

STRAP INFORMATION SUMMARY

The 4112 terminal has straps on the various circuit boards, which provide flexibility in its operating parameters. There are two kinds of straps: cut straps, and jumper straps. In cases where the terminal was designed to function one way, but provisions were made for future design enhancements, cut straps are often used. Jumper straps are used for most strap options, which allows: more than one kind of chip to be used in a given socket, or a change in timing or other operating parameters.

This summary gives the strap settings for each standard circuit board/module in the 4112. Also the disk option's recommended strap settings are given, because most terminals include this option.

PROCESSOR BOARD STRAPS

Several cut and jumper straps are provided on the Processor Board. Straps labeled "Jxxx" have square pins with movable jumpers. Straps labeled "Wxxx" are cut straps; they consist of circuit traces on layer 1 of the ECB (and no square pins). Table B-1 lists these strap settings.

Table B-1

PROCESSOR BOARD STRAP SETTINGS

Strap Label	Definition
ROM Logic Straps:	
ROM Size Strap (W126)	Select either 16K bit or 32K bit ROMs, or disable all Processor board ROMs.
ROM Wait States (W475)	This strap is normally strapped for ONE wait state. If all the ROMs on the Processor board are fast enough, this strap may be changed to indicate ZERO wait states.
ROM Type Straps (J226, J236, J426, J427)	There is one set of straps for each two-ROM bank of ROMs. These straps configure the board for the pin-outs of the ROM being used.
BLCK Source (W455, W456)	This strap is normally strapped to "on-board." If more than one Processor board is used in the system, only one should be strapped to "on-board;" all others should be strapped to "off-board."
Interrupt Level Straps (W470)	The processor can generate three different interrupts to the MPU bus. These straps define the interrupt priority levels of the three different interrupts. Normally, the "host port receiver interrupts" are set to interrupt level 0, "keyboard interrupts" set to level 4, and "host port transmitter" are set to interrupt level 5.
Bus Timout Enable (W561)	This strap prevents the Processor board from driving ACK1-0 on a bus timeout. It is used for multi-processor board systems.
Test 1 and Test 2 (J150 and J125)	Tests 1 and 2 disable clocks on the Processor board for ATE (automated test equipment) testing.
RS-232-C/RS-232-A (J522)	This is normally set for RS-232-C. When re-strapped for RS-232-A, the SRTS (Secondary Request To Send) signal is sent to pin 11 of the 25-pin RS-232 connector, rather than to pin 19.

KEYBOARD STRAPS

The 4112 keyboard circuit board has a set of cut straps that allows the firmware to interpret key strokes according to languages other than English. This strap consists of four individual cut straps labeled W1 through W4. The combinations of these straps are read as one hexadecimal number which corresponds to certain keyboard options. See Table B-2.

Table B-2

KEYBOARD LANGUAGE OPTION STRAPS

Language	Option Number	Open Cut-Strap[a]	Hex Code
Standard	—	none	00
United Kingdom	4A	E4	08
Swedish	4C	E2	02
APL	4E	E1	01
Danish/Norwegian	4F	E2 & E3	06

[a] These straps are labeled E1 - E4 on the circuit board, but are labeled W1 - W4 on the schematic sheet (A3-1).

RAM/ROM AND RAM CONTROLLER BOARD STRAPS

To install optional RAM memory, one or more RAM Controller boards must be installed in the card-cage. Each RAM Controller board has sockets for four RAM Array boards. The RAM Array boards contain 32K-byte banks of memory. Since six RAM Controller Boards can be installed in a 4112, it is necessary to specify the starting address of the four RAM banks on each RAM Controller board.

Strap J165 sets the Base Address for all memory on the board. Set the strap to "1," for the RAM Controller nearest the processor. Set the strap on the other RAM Controller boards to "2", "3", "4", etc. as they are placed in order farther away from the Processor board. Strap J165 allows strapping for a maximum of 6 RAM Controller boards. Figure B-1 shows the location of these straps.

VIDEO CONTROLLER BOARD STRAPS

The 4112's Video Controller Board has eleven straps. Most of these straps are used only during manufacturing testing. Only three of these straps are of interest here; they are J551, J310, and J501.

Table B-3

VIDEO CONTROLLER BOARD STRAPS

Strap	Position	Function
J551	RIGHT (on board) = UP (schematic)	Generates 60 Hz 525 line video.
	LEFT Normally set to RIGHT (60Hz)	Generates 50 Hz 625 line video.
J310	UP (on board) = DOWN (schematic)	Generates timing for 2118 type RAMs.
	DOWN Normally set to UP (2118s)	Generates timing for 4116 type RAMs.
J501	ON	The Video Controller cannot request the memory cycles required to refresh the screen.
	OFF Normally OFF	Normal Operation. This strap makes the image more stable during testing and is only used to debug the Vector Generator.
J55 J56 J201 J245 J260 J361 J563 J650		Used for manufacturing test only.

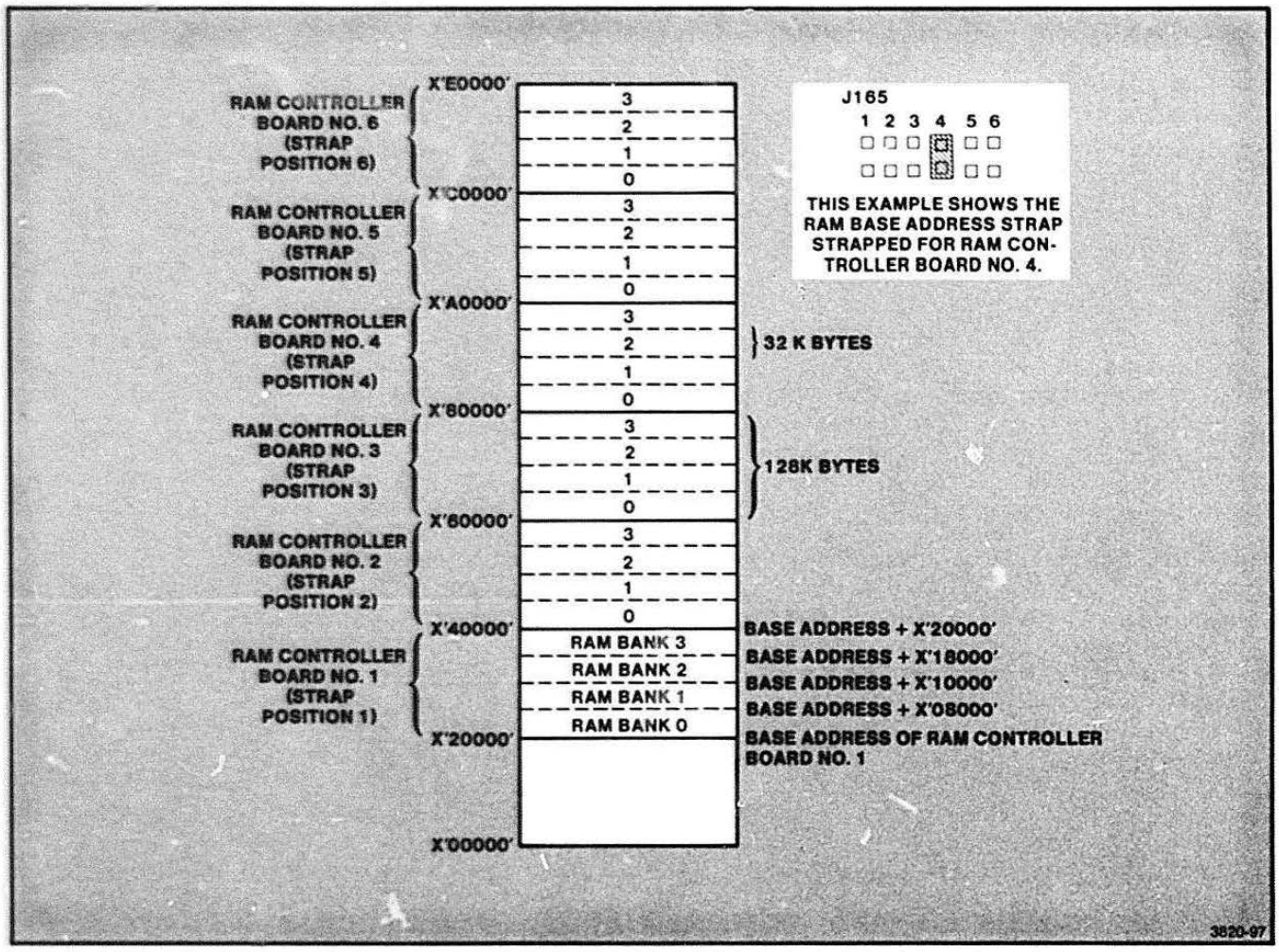

Figure B-1. Strapping RAM Controller Board Base Address.

VECTOR GENERATOR BOARD STRAPS

Strap, W190, may be installed to restrict microcode address space to 256 words when 74S471 type ROMs are used, instead of 74S472.

RASTER MEMORY BOARD STRAPS

There are two zero-ohm resistors for selecting which type of RAM chip is being used. One position is labeled "3S" for three power supply RAMs (4116-1). The second position is labeled "1S" for single power supply RAMs (2118-4).

DUAL PLANE RASTER MEMORY BOARD STRAPS

Jumper Straps:

1. There is a strap on each PDAT signal to disable its input.

2. There is a strap on each Video output to disable its output.

EXTERNAL VIDEO BOARD STRAPS

Option 11 (External Video) produces a standard interlaced video signal. The External Video Board contains these straps:

Table B-4

EXTERNAL VIDEO STRAPS

Jack	Position	Explanation		
J25	IN OUT	75 ohm termination		
		Video Levels		
		White Ref.	Blank	Sync Tips
J145	RS 170 RS 330	1 V 0.714 V	0 V 0 V	-0.4 V -0.286 V
J511	IN OUT	50-Hz aspect ratio correction is set to OUT only if a 4612 Hard Copy Unit is used while in the 50 Hz mode; only the 4612 aspect ratio is critical. If strap is set to OUT, in 50-Hz mode, external monitors will have an incorrect aspect ratio when adjusted to standard 50 Hz video specifications.		

Appendix C

EXTERNAL VIDEO OPTION

INTRODUCTION

This appendix describes the 018-0169-00 (Option 11) External Video/30 Hz/RS-170 board for the 4112 terminal. This appendix provides the following information:

- General information about the External Video board
- Specifications for Option 11
- Theory of operation
- Installation procedure
- Strap settings

Refer to Volume 2 for electrical parts list, schematic and interconnect diagrams, and mechanical parts lists.

PRODUCT DESCRIPTION

The External Video board contains circuitry that:

- Converts the terminal's 60/50 Hz non-interlaced video signal to 30/25 Hz interlaced video for standard video television monitors (see Figure C-1).
- Produces a standard studio video signal output without serration or equalization pulses (pulses for aiding horizontal and vertical synchronization).
- Corrects the aspect ratio (ratio of the width-to-height) for 50 Hz line frequency by adding 50 lines to the top and bottom of the raster.

RELATED DOCUMENTATION

Operator information for this option is contained in the *4112 Computer Display Terminal Operator's Manual.*

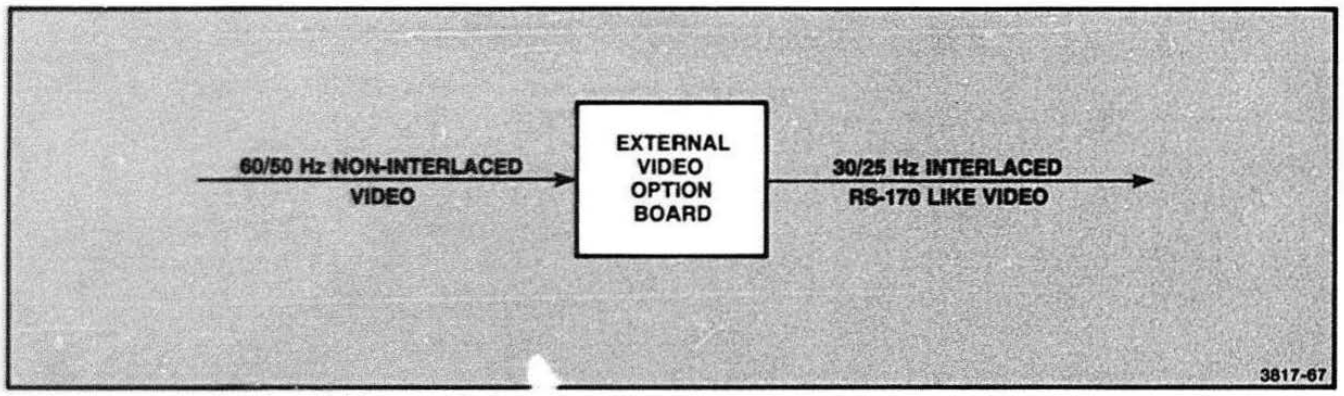

Figure C-1. External Video Option Basic Function.

SPECIFICATIONS

ELECTRICAL

Power Requirements

- 1.80 A at + 5 V
- 45 mA at −12 V
- 400 mA at −5.2 V
- 90 mA at −2 V
- 60 mA at + 12 V

ENVIRONMENTAL

All environmental specifications for Option 11 are identical to those for the terminal.

Heat dissipation is 43 BTU/hr (typical = 12.5 W).

THEORY OF OPERATION

INTRODUCTION

The first part of this theory section describes the overall operation of the Option 11 circuit board. The circuit blocks labeled on the schematic are grouped into four 'super blocks':

- Scan Conversion
- Line Control
- DAC
- External Synchronization

Figure C-2 shows how the super blocks are related.

The individual blocks that comprise each super block are described in detail in the later part of the theory discussion. These blocks are grouped under headings that are the super block names. Figure C-3 illustrates this grouping of circuit blocks.

Scan Conversion Buffer

The Scan Conversion Buffer:

- Latches the pixel data as an ECL (emitter coupled logic) signal.
- Converts the ECL signal to TTL and shifts it to eight bits of digital data.
- Stores the eight-bit data word in the input buffer. The eight bits of digital data remain in the buffer until written into memory. This latching, converting, and storing repeats every eight pixels.
- Latches (or passes) the eight-bit word from Memory to the Output Shift Register.
- Loads the output buffer data into the Output Shift Register.
- Converts the eight-bit parallel word to serial data.

The input from the terminal display to the converter is non-interlaced. The output of the converter is interlaced and is output in odd and even fields alternately.

The timing of one field of non-interlaced video is the same as one field of interlaced video. Both fields begin and end at the same time. The non-interlaced field is scanned twice. One scan furnishes the odd lines of the interlace and the second scan provides the even lines.

The Scan Conversion Buffer relies on the Video Controller for SCANSYNC and VDRIVE. SCANSYNC starts the scanning of the horizontal lines and VDRIVE starts the Line Counter at the beginning of each field.

Line Control

The Line Control logic:

- Receives horizontal and vertical sychronization signals from the Video Controller. Line Control uses these signals to start each line and field respectively.
- Determines whether the status of the Scan Conversion Buffer is in an odd or even field.
- Generates vertical and horizontal blanking pulses.
- Generates vertical and horizontal synchronization pulses.

It is normal to see a slight jitter on the internal display when using external synchronization. Approximately 1/4-pixel jitter appears line to line under these conditions. (A pixel is the smallest unit of information in the display.)

Flicker appears on an external monitor for certain display patterns. This is kept to a minimum by using a long persistence phosphor screen. A monitor with a minimum bandwidth of 13 MHz (15 MHz for 50 Hz line operation) is recommended. A lower bandwidth monitor may be used resulting in reduced picture quality.

DAC (Digital-to-Analog Converter)

The four-bit current summing DAC converts the digital video signal to the analog signal required by external display monitors.

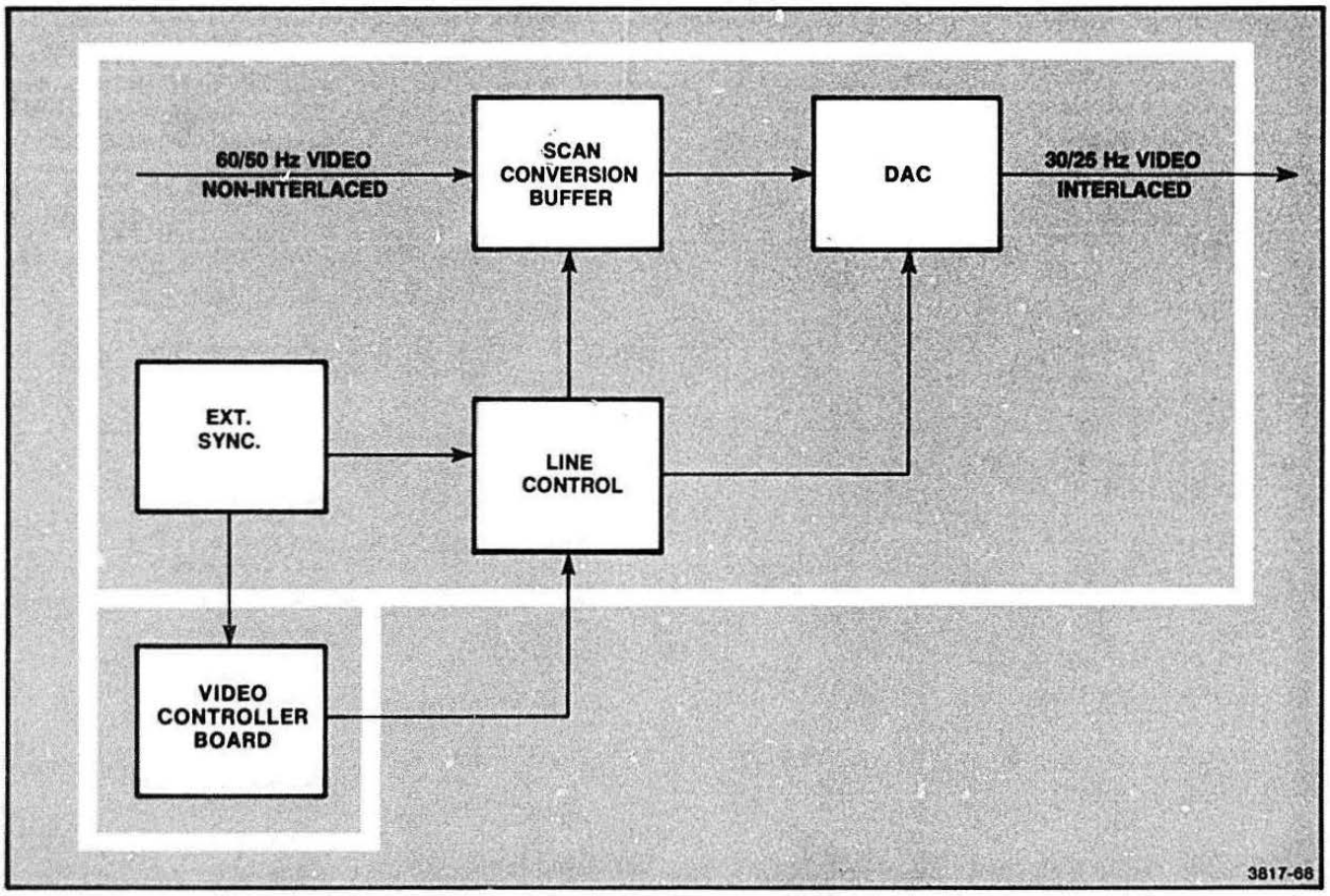

Figure C-2. Simplified Block Diagram.

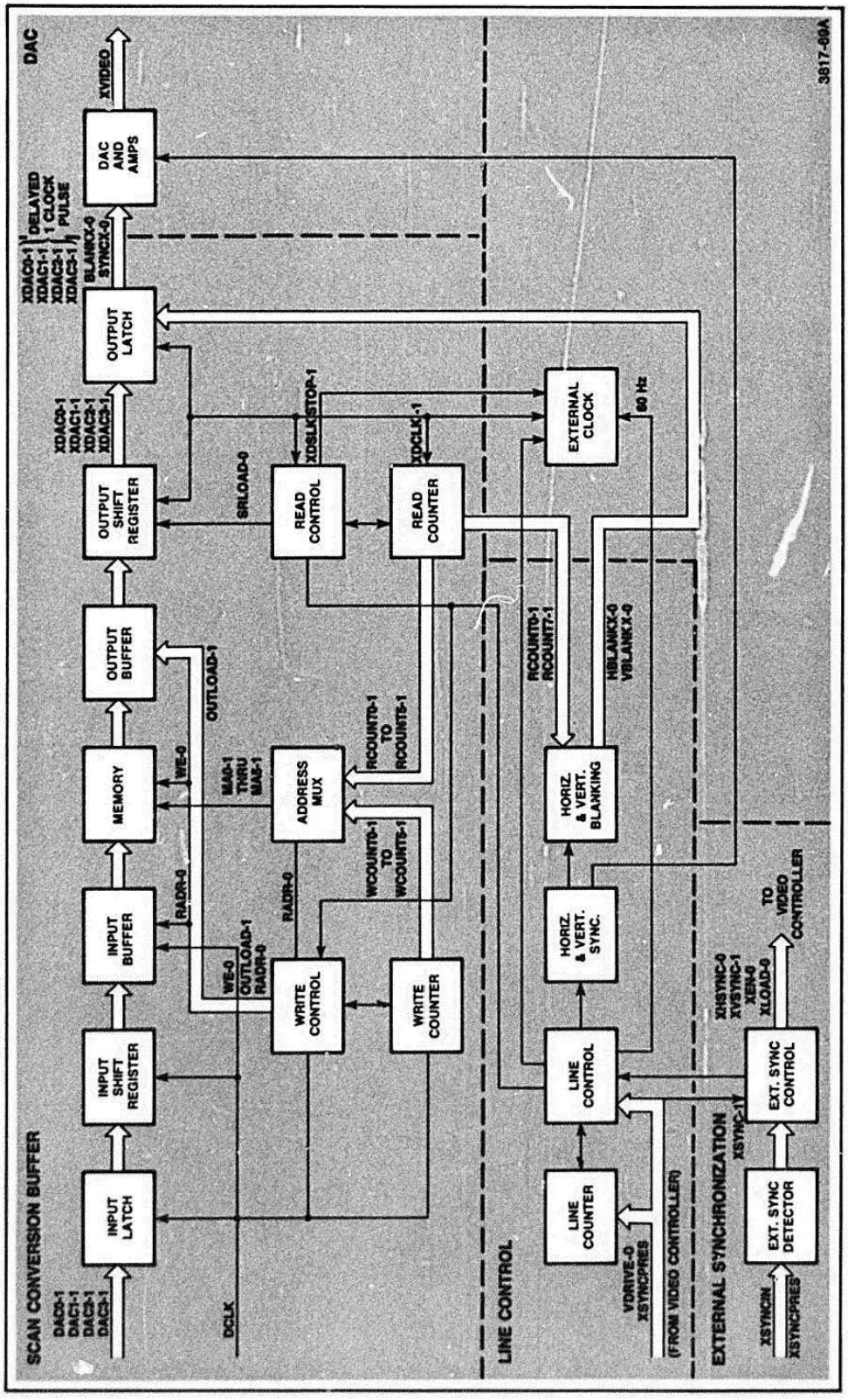

Figure C-3. External Video Board Block Diagram.

External Synchronization

The External Synchronization logic:

- Buffers the external synchronizing signal
- Locks to the external synchronizing signal
- Strips the horizontal and vertical synchronizing signals from the external synchronization input
- Generates synchronizing signals for the 4112 Video Controller

The output of the External Video board may be synchronized to an external source. The video output does not contain serration or equalization pulses. They will appear, however, if present on the source. If external synchronization is not used, the 75 Ω termination must be left in.

SCAN CONVERSION BUFFER OPERATION

The Scan Conversion Buffer consists of an Input Latch, Input Shift Register, Input Buffer, Memory, Output Buffer, Output Shift Register, Output Latch, Write Control, Write Counter, Read Control, Read Counter, Address Multiplexer, and External Dot Clock. The actual operation is described in the following block descriptions (see Figure C-3).

Input Latch

The Input Latch operates as a pipeline latch for the 60 Hz or 50 Hz noninterlaced video. It latches the video as an ECL signal. The video input is read in at a 40 ns pixel rate. The video input is converted to a TTL signal and placed in the Input Shift Register.

Input Shift Register

The serial input video data is loaded into the shift register by a 25 MHz clock. The resulting data is an eight-bit parallel word. The register shifts data on the positive edge of DCLK (Dot Clock).

Input Buffer

The Input Buffer latches and holds the eight-bit wide data from the Input Shift Register until the data is written into Memory.

Memory

The Write Controller initiates writing into Memory. It sends a WE (Write Enable) to Memory when the write data and address are settled. The Write Controller also controls RADR (use Read Address).

Changing the select input of the Address Multiplexer to Read Address (RADR) permits the Memory to be read out. Since the input and output sides of the Memory are asynchronous, the circuit reads the Memory out more often than is otherwise needed to be sure of getting valid output.

Output Buffer

The Output Buffer is a transparent latch. It has the following features:

- Latches data until the current line has been written into Memory
- Becomes transparent after writing the current line into Memory
- Is enabled by the Write Controller

Output Shift Register

The Output Shift Register:

- Changes the eight-bit words back to serial data at an 80 ns rate (70 ns for 50 Hz) after synchronous loading
- Is loaded with information every eight XDCLKs
- Sends the serial data to the Output Latch for mixing with the blanking pulses

Output Latch

The video from the Output Shift Register and the blanking signal are latched on the rising edge of XDCLK. The video data and blanking signal are then sent to the DAC.

Write Control

The Write Control section generates most of the control signals for the Scan Conversion Buffer. Write Control has a pixel counter that counts each pixel and wraps around. Its output goes to logic that generates the following timing signals:

- OUTLOAD-1 (This signal informs Write Control when to load the transparent latch and it is active during pixel count 7.)
- RADR-0 (RADR-0 tells Write Control when to use the read address and it is active during pixel counts 4-7.)
- WE-0 (This signal gives a write command to the memories and is active during pixel counts 2 and 3.)

These circuits go to their inactive states after completely writing the current line of data into Memory.

Write Counter

The Write Counter consists of a three-bit pixel counter and a six-bit word counter. They are started when the SCANSYNC signal is accepted.

The counters are loaded with a negative number and count up to 0. When they reach 0, valid information is written into Memory.

The output of the pixel counter is sent to the Write Control logic thus generating RADR-0, OUTLOAD-1, and WE-0 for the Memory Buffer.

The output of the word counter, the Write Address, is sent to the Address Multiplexer. This signal is then sent to the Memory during WRITE time.

Read Control

The Read Control logic generates the load command (for the output shift register) by asserting SRLOAD during count 7 of the Read Counters. The Output Shift Register is loaded on the next rising edge of XDCLK-1. It also stops XDCLK at the end of the active video time until the beginning of the next line.

Read Counters

The Read Counter consists of a three-bit pixel counter and a six-bit word counter. The three most significant bits of the Read Counter are the pixel count and are sent to the Read Control logic. The next six bits are the word count. These bits are sent to the Address Multiplexer to be used for reading from memory.

Blanking follows each active line of video. The Read Counter's load is asserted to prepare the counters for the next line of video data. Then XDCLK is stopped, until STARTREAD-0 is again asserted.

Address Multiplexer

The Address Multiplexer is a six-bit wide 2-to-1 multiplexer. RADR-0 determines whether it sends the output of the Write or the Read Counters to Memory.

External Dot Clock

The External Dot Clock generates the 12.5 MHz XDCLK (or 14.3 MHz in 50 Hz mode) for external video. It uses a 100 MHz crystal and a divide-by-eight or divide-by-seven counter to make the desired output frequency. The Read Control logic starts and stops the External Dot Clock.

LINE CONTROL CIRCUITRY

Line Control

The Line Control circuit receives horizontal and vertical synchronization signals from the Video Controller. This block uses these signals to start each line and field respectively. (See Figure C-3.)

Aspect ratio correction occurs when operating at 50 Hz. The raster has 525 lines for 60 Hz and 625 lines at 50 Hz. During 50 Hz operation the 480 active lines would appear shorter on the 625-line monitor. The video for the 625-line raster is sent out at a faster rate to reduce the width. This corrects the aspect ratio so it remains 4:3. See Figure C-4.

NOTE

The aspect ratio correction may need to be defeated if the External Video board drives certain hard copy units (such as the TEKTRONIX 4612) at the 50 Hz line rate. Defeating the aspect ratio correction maintains the correct aspect ratio for hard copy output (see Strap Settings at the end of this appendix).

Line Counter

The Line Counter performs the following functions:

- Identifies odd or even fields
- Generates vertical blanking
- Starts the Scan Conversion Buffer

The Line Counter relies on the Video Controller for SCANSYNC and VDRIVE.

Horizontal Synchronization

The Horizontal Synchronization Generator makes a 4.75 μs pulse (4.55 μs in 50 Hz mode) for the external video if there is no external synchronization present. The first XDCLK-1 after SCANSYNC-1 starts the XHSYNC-1 counter (if the XREADY signal is asserted). The XHSYNC counter is reset on count 128.

Vertical Synchronization

The Vertical Synchronization Generator makes the vertical synchronization signal for the external video. It does so by buffering the VDRIVE signal that comes from the Video Controller board. This signal occupies the same time as three lines of external video.

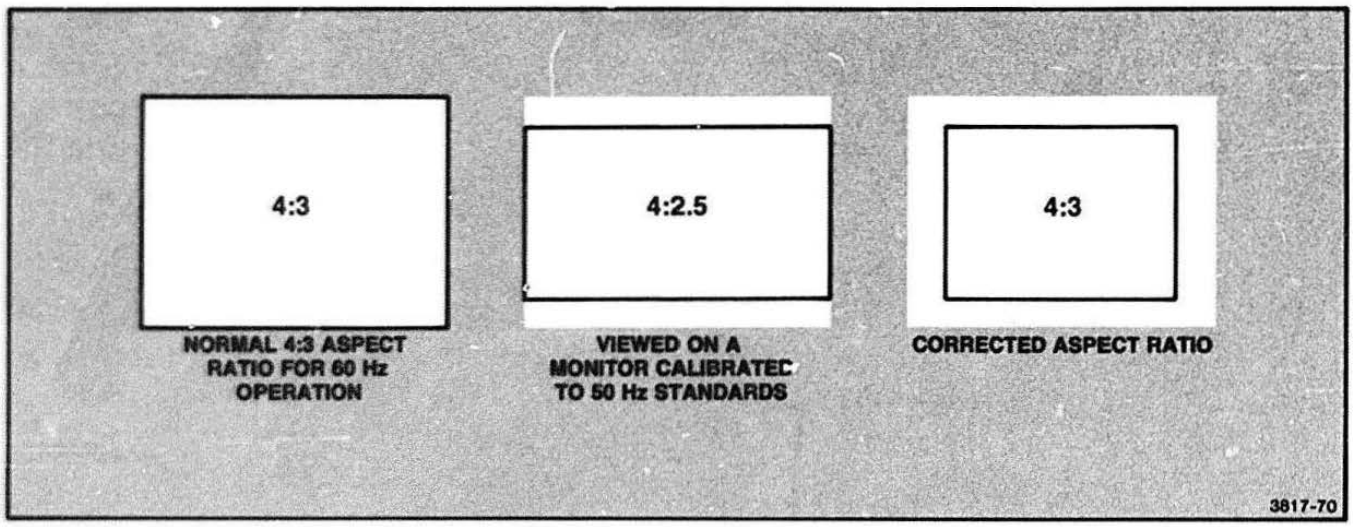

Figure C-4. Aspect Ratio Correction.

Horizontal and Vertical Blanking

The Blanking Generator makes video blanking during the horizontal and vertical retraces. Vertical blanking is accomplished by causing the output of the vertical blanking flip-flop clear the Output latch. Horizontal blanking is generated by the horizontal blanking circuitry in conjunction with the Output Latch.

DAC AND AMPLIFIER OPERATION

The DAC mixes video and blanking information (from the Output Latch) with the composite synchronization signal. This makes a composite video output signal. The DAC is a four-bit current summing DAC.

The External Video board's output voltage levels are normally set to RS-170 levels. These can be changed to RS-330 voltage levels (see *Strap Settings*, later in this appendix).

EXTERNAL SYNCHRONIZATION

External Sync Detector

A comparator converts the external synchronization input to a TTL level. This signal is an RS-170 video signal or an RS-170 standard synchronization generator signal. The synchronization reference signal must be 0.0 V and the sync signal tips must be ≤ -0.4 V and ≥ -4.0 V. Equalization and serration pulses are optional. The output of the comparator goes to the Horizontal Synchronization Stripper, Vertical Synchronization Stripper, and the External Synchronization Detector.

The detector is a 50 ms retriggerable multivibrator that senses if no external sync pulses have been received within the last 50 ms. This indicates that there is no external synchronization.

The Horizontal Synchronization Stripper is a phase-locked-loop (PLL). It uses a 4 μs one-shot to strip the horizontal synchronization from the external synchronization input. This one-shot gives a constant pulse width to the PLL.

The output frequency of the PLL is twice the input:

60 Hz 15,750 Hz input frequency
31,500 Hz output frequency

50 Hz 15,625 Hz input frequency
31,250 Hz output frequency.

The PLL is calibrated to run free at 31,375 Hz $\pm$ 25 Hz in 60 Hz mode, and at 31,125 $\pm$ 25 Hz in 50 Hz mode.

The Vertical Synchronization Stripper passes XHSYNC, but holds its output (XVSYNC-0) low for the duration of the external vertical synchronization pulse. The stripper accepts any pulse longer than 7 μs as a XVSYNC pulse.

External Synchronization Control

The external synchronization control generates a 400 ns XLOAD-0 signal at the end of the next VDRIVE time, only if there is a change in the status of XSYNCIN (it comes or goes). XLOAD-0 informs the Video Controller, then looks at XEN-0 and reboots itself accordingly.

TIMING SECTION

Each field begins when VDRIVE starts the Line Counter. The Line Counter counts up from a negative number to 0. Valid lines start coming out at this time. VBLANK is then released, until the end of the last active line of the field, when it is reasserted.

A flip-flop, toggled by VDRIVE, determines whether to use odd or even lines when there is no external synchronization. If there is no external sync, the XHSYNC signal makes this determination.

If SCANSYNC and HREADY are asserted together, SCANSYNC starts these:

- The Write Counters
- The HSYNC generator
- XDCLK-1 and the Read Counters

The Read Counters count at half the rate of the Write Counters. Both the Read and Write Counters start at a negative number and count up. At the time the Write Counter reaches 0, the Memory begins storing the active video information. The Read Counters reach 0 later and start reading out active video information.

The Read Counters and the Write Counters operate asynchronously. Therefore, every cycle that is not a write cycle is used as a read cycle to assure that valid information is loaded into the Output Shift Register.

FIELD INSTALLATION

These instructions describe the field installation of the Option 11 External Video board in the 4112 terminal. J307-1 serves as the Video Output for use with hard copy units. (J307-1 is connected to hard copy connector J5004 when a hard copy unit is used.)

The 018-0169-00 (Option 11) kit contains:

- Two (2) BNC connectors
- Two (2) solder lugs
- Two (2) hex nuts
- Two (2) varistors
- Two (2) cables
- One (1) External Video board
- Three (3) cable ties

EQUIPMENT REQUIRED

The following tools are needed to install this option:

- Screwdriver, Pozidriv® #2
- Screwdriver, Pozidriv® #1
- Wire cutters
- Long-nose pliers
- Soldering iron
- 5/16-inch nut driver
- 3/16-inch nut driver.

INSTALLATION PROCEDURE

1. TURN OFF power and disconnect terminal power cord.
2. REMOVE four Pozidriv® screws from back, two 5/16-inch screws from bottom, and remove top cover (see Figure C-5).
3. REMOVE six Pozidriv® screws from rear panel and remove rear panel (see Figure C-6).
4. MOUNT the two BNC connectors, with attached hardware, to the rear panel (see Figure C-7).
5. ADD two solder lugs and two hex nuts over the stud on the back side of the BNC connectors. See Figure C-7 again.
6. SOLDER a varistor between each solder lug and BNC connector after:
   - Turning the varistor so its value is readable.
   - Cutting as short as possible the lead to the BNC connector (this prevents possible short circuits).

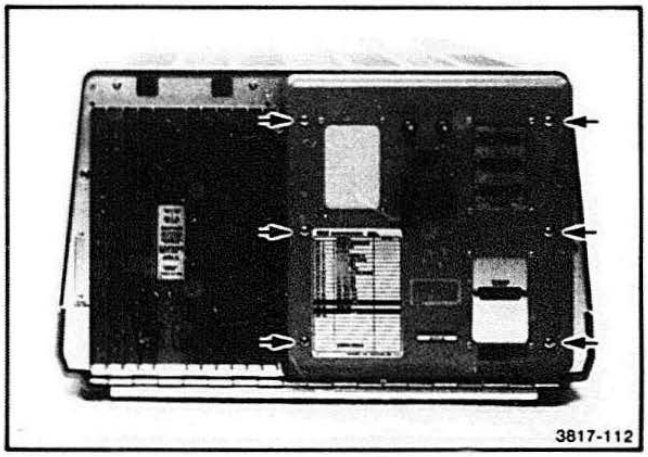

Figure C-6. 4112 Rear-Panel Mounting Screws.

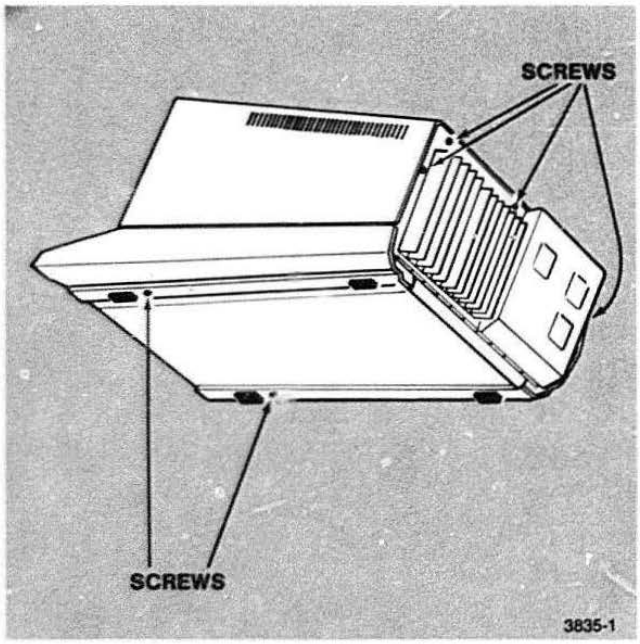

Figure C-5. 4112 Top-Cover Mounting Screws.

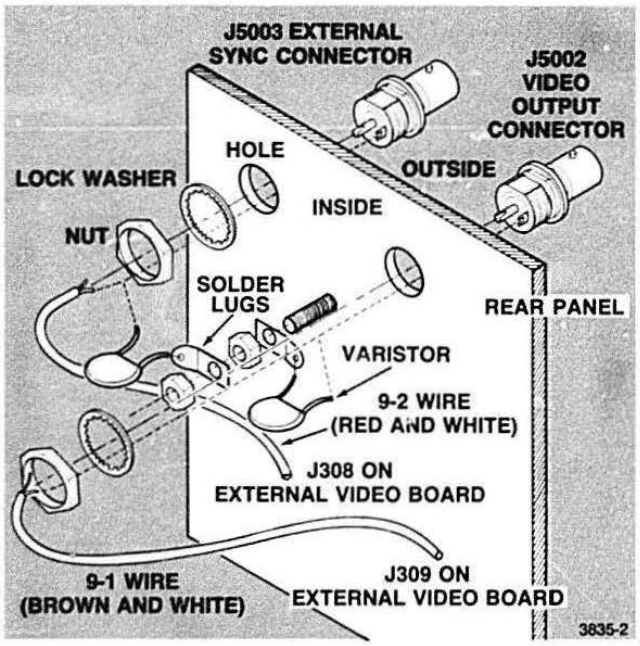

Figure C-7. Mounting Rear-Panel Connectors.

7. SOLDER as follows (cable to BNC connectors):
   - Brown and white wire to Video output J5002
   - Ground wire connects to varistor
   - Red and white wire connects to External Sync J5003
   - Ground wire to varistor lead (see Figure C-8)
8. ADD two cable ties on terminal cover side of card cage. Dress cables through hole in card cage and secure with cable ties (see Figure C-8 again).
9. ADD a brown and white and a red and white cable to the cable ties just added.
10. REPLACE rear panel by replacing the six screws shown in Figure C-6.

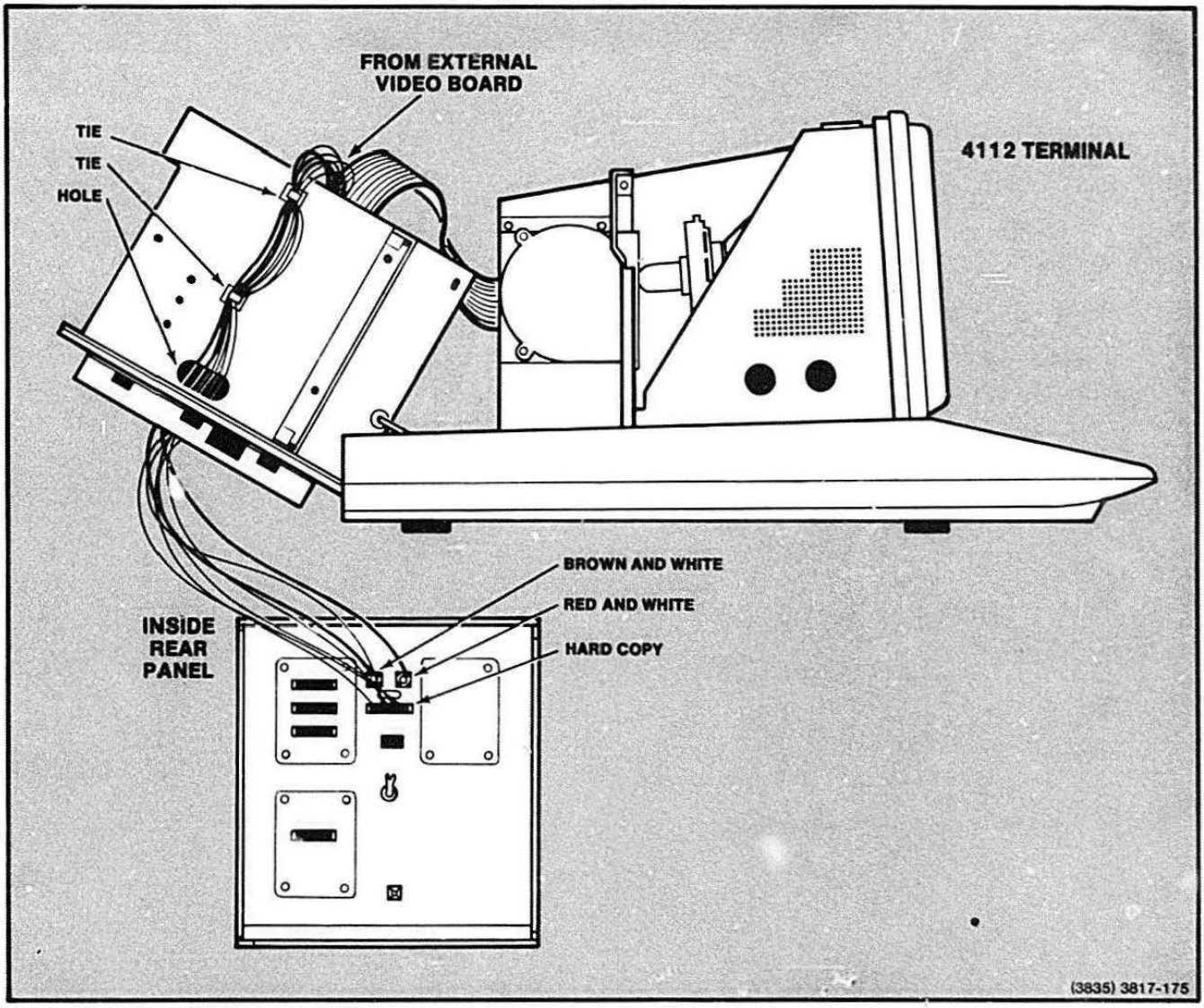

Figure C-8. Cable Route, via Card-Cage to Rear Panel.

11. REMOVE six screws (two in the top front, and two in each side) from the card cage. See Figure C-9. Rotate card cage up while watching the cables just installed to be sure they are long enough to reach and are not pinched. Lengthen cables if not long enough.

    With card cage up, slide bail forward and slip into retainer; this holds up the card cage.

12. INSERT External Video board into Slot 9 of card cage (see Figure C-10).

13. CONNECT brown and white wire to J308 on External Video board.

14. CONNECT red and white wire to J309 on External Video board.

15. LIFT locking bail and lower card cage back into its original position. Be careful not to crush or bind any cabling. Replace the six card cage mounting screws.

16. REPLACE terminal top cover and replace the six screws.

17. RECONNECT terminal power cord and turn terminal on.

This completes the installation. Connect a 75 Ω cable from the Video Output connector (on the back of the terminal) to a video monitor. If the information displayed on the terminal display screen shows up on the external video monitor, the installation is complete.

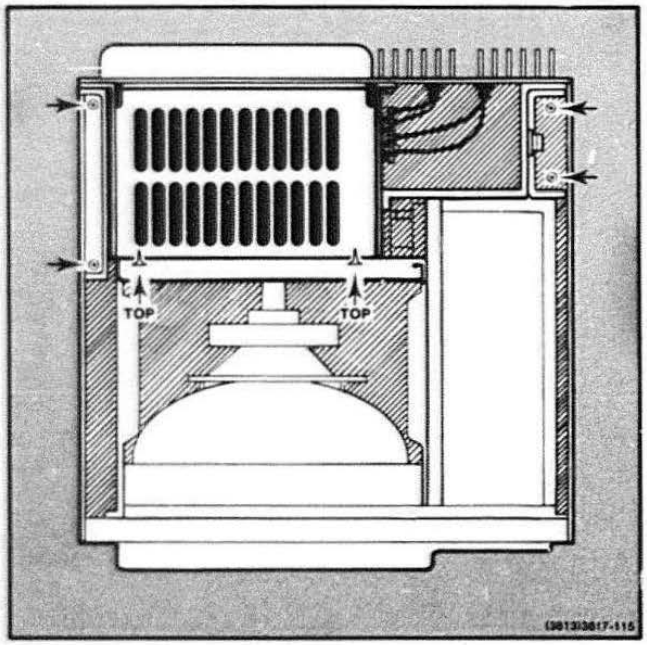

Figure C-9. 4112 Card-Cage Mounting Screws.

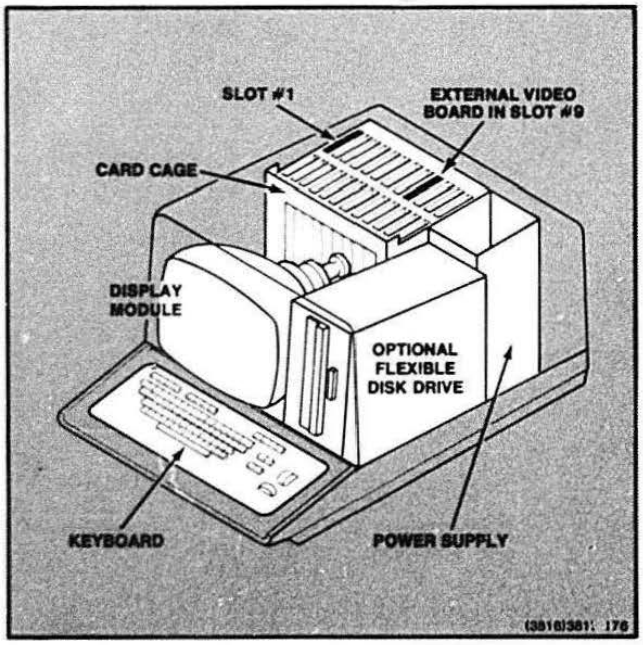

Figure C-10. External Video Board in Slot Nine of Card-Cage.

STRAP SETTINGS

The strap settings for the External Video Output board are shown in Table C-1.

Table C-1

STRAP SETTINGS

Straps	Description	Settings
J25	75 Ω termination (for the sync input). Leave in when operating without external sync.	IN OUT
J145	VIDEO LEVEL (Affects only the voltage level of the Video outputs). Refer to Table C-2.	RS-170 RS-330
J511	50 Hz aspect ratio correction is set to OUT only if a 4612 Hard Copy Unit is used while in the 50 Hz mode and the 4612 Hard Copy aspect ratio is critical. If this strap is set to OUT (in the 50 Hz mode), the external monitor adjusted to standard 50 Hz video specifications will have an incorrect aspect ratio. Hard Copy Connections: For 30/25 Hz hard copy, pull Pins 1 and 2 on the Video Controller Hard Copy connector J287 and install on External Video J307.	IN OUT

Table C-2

VIDEO LEVELS

Mode	White Ref.	Blank	Sync Tips
RS-170	1.0 V	0 V	−0.4 V
RS-330	0.714 V	0 V	−0.286 V

Appendix D

4112 OPTIONS INSTALLATION PROCEDURES

OPTION 01 (EXTENDED COMMUNICATIONS)

INTRODUCTION

Two EROMs contain Option 01 (Extended Communications). These EROMs are programmed with the added features of Half-Duplex, Block Mode, and Downloader.

The Option 01 EROMs are located at U21 and U121 on the RAM/ROM Board.

TOOLS REQUIRED

The following standard tools are needed for this installation procedure:

- Screwdriver, Pozidriv® #2
- Screwdriver, Pozidriv® #1
- Nut driver, 5/16-inch

INSTALLATION

CAUTION

Static voltages will damage EROMs. Before touching EROM, discharge your body's acquired static charges; touch a grounded metal object.

Step-by-step procedure:

1. Turn OFF terminal and disconnect power cord.

2. Remove four Pozidriv® screws from the back; remove two bolts from the bottom; and lift off cover. (See Figure D-1.)

3. Remove six screws from the card-cage (see Figure D-2). Tip card-cage up and back (to the rear) until it rests against the wire bail; watch attached cables to be sure none are pinched or pulled loose. If cables are not long enough, reroute them or lengthen them (make new cables) to fit.

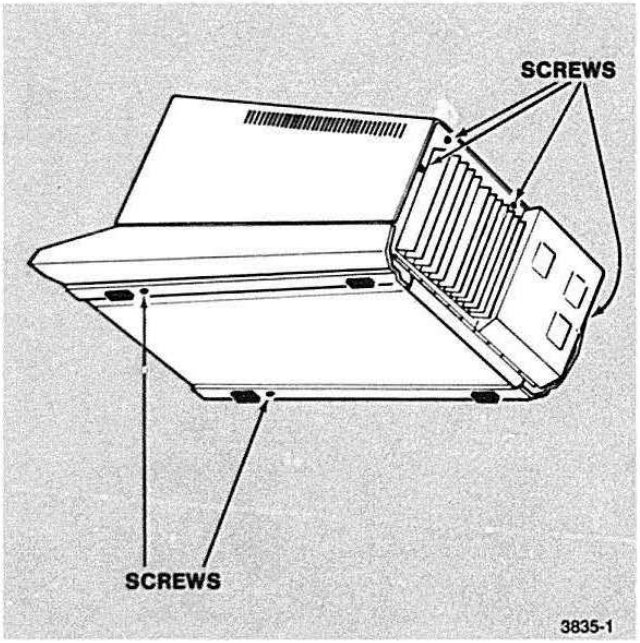

Figure D-1. Top-Cover Mounting Screws.

4. Remove RAM/ROM board from the card-cage.

5. Insert EROM (part number 160-0985-00, 01,...) into U21. Then insert EROM (part number 160-0984-00, 01,...) into U121.

6. Replace RAM/ROM board in the same slot it was removed from in the card-cage.

7. Lift locking lever/bail. Rotate card-cage back down, being careful to not crush or pinch any cables. Replace the six screws removed in Step 3.

8. Place the top cover on the terminal, and replace the screws that were removed in Step 2. (These are located in the bottom and rear.)

9. Plug in power cord and power-up the terminal.

10. Run Self-Test to be sure all parts of the terminal are operating properly. (Push SELF TEST and MASTER RESET buttons.)

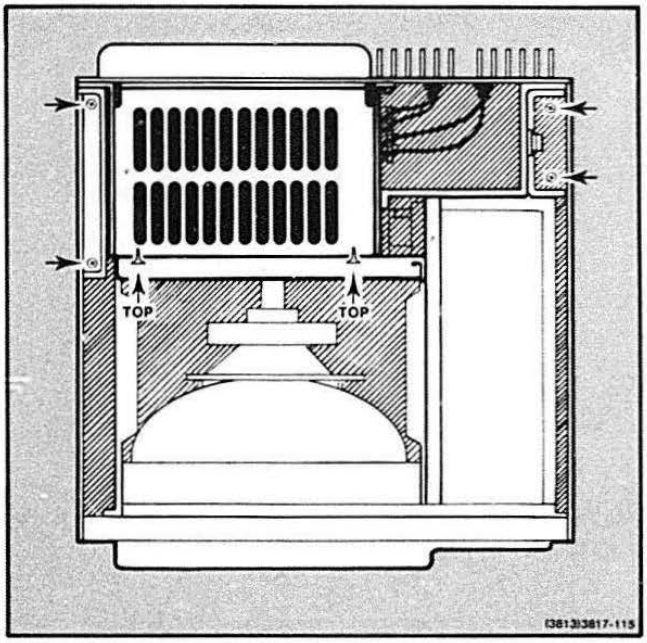

Figure D-2. Card-Cage Mounting Screws.

OPTIONS 4A-4F (KEYBOARDS)

INTRODUCTION

Four optional keyboards are available for this terminal:

- Option 4A — United Kingdom Keyboard
- Option 4C — Swedish Keyboard
- Option 4E — APL Keyboard
- Option 4F — Danish/Norwegian Keyboard

Changing a standard (North American) keyboard to one of the optional keyboards is a three part process, listed under the following procedure.

TOOLS REQUIRED

- Screwdriver, Pozidriv® #2
- Screwdriver, Pozidriv® #1
- Sharp knife, Exacto or similar
- Nut driver, 5/16-inch

KEYBOARD ROMS INSTALLATION PROCEDURE

CAUTION

Static voltages will damage ROMs. Before touching ROM, discharge your body's acquired static charges; touch a grounded metal object.

The standard keyboard requires no ROMs in the keyboard ROM position on the RAM/ROM board. But, if anyone of the keyboard options is installed, the keyboard ROMs must also be installed. One pair of ROMs are required, and this pair contains the firmware for all four of the keyboard options. This pair of ROMs is placed in the upper lefthand corner of the RAM/ROM board (see Figure D-3). The Tektronix part numbers for these keyboard option ROMs are:

- Most Significant Byte — 160-0983-01
- Least Significant Byte — 160-0982-01.

Step-by-step Keyboard ROMs installation procedure:

1. Turn OFF the terminal and remove the power cord.
2. Remove four Pozidriv® screws from the back; remove two bolts from the bottom; and lift the cover off. (See Figure D-1 again.)
3. Remove six screws from the card-cage (Figure D-2). Tip card-cage up into the board access position, and let it rest against the wire bail. Watch attached cables to be sure none are pinched or pulled loose. If cables are not long enough, reroute them or lengthen them to fit.
4. Pull out the pull tabs on the RAM/ROM board, and remove this board.
5. Install the Keyboard Option ROM at the left end of the board (as indicated in Figure D-3).
6. Reinstall the RAM/ROM board, lower the card-cage into the normal position, and replace the cover on the terminal. Go to next procedure.

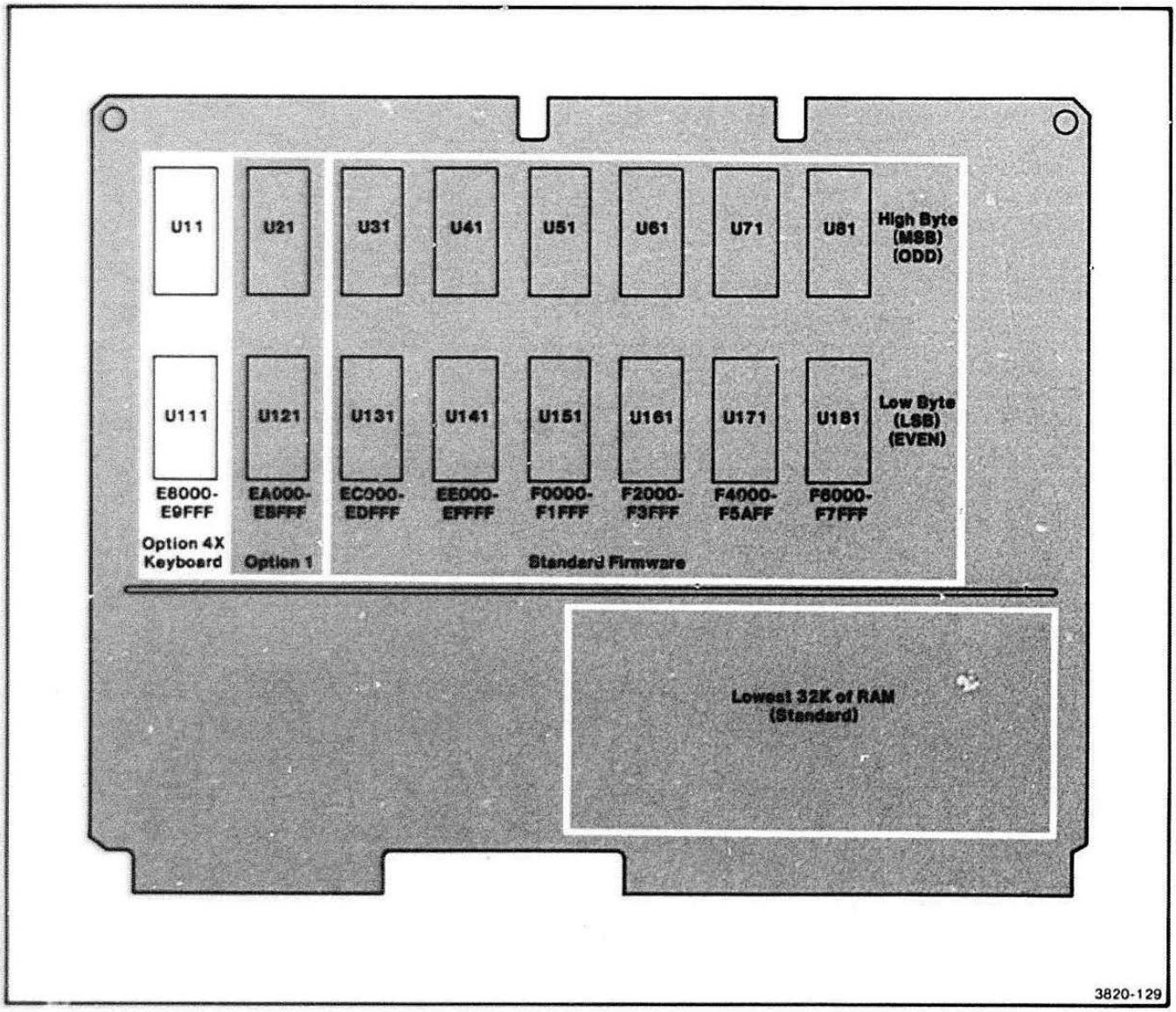

Figure D-3. RAM/ROM Board (Option 4X ROM Location).

CUTTING THE KEYBOARD STRAPS

The keyboard circuit board has a set of cut straps that allows the firmware to interpret key strokes according to languages other than English. This strapping consists of four individual cut straps labeled: E1 through E4 (labeled W1 - W4 on schematic sheet A3-1). Read this combination of straps as one hexadecimal number which corresponds to certain keyboard options. See Table D-1.

To access these cut straps, use the following procedure:

1. Remove two Pozidriv® screws from under the front of the terminal (see Figure D-4).
2. Then, using the screwdriver bit holder, push up into the hole under the front edge of the terminal. This dislodges the front edge of the keyboard assembly so you may lift this assembly free of the terminal (as needed in the following steps).
3. Unplug the keyboard ribbon cable as needed.
4. Unplug the speaker wire from its connector on the end of the keyboard circuit board.
5. Unscrew the five Pozidriv® screws that attach the shield plate to the keyboard circuit board. This allows the shield plate (with speaker) and circuit board to be removed from the mounting plate.

Cut Straps:

1. Locate the cut straps E1 through E4, shown in Figure D-5.
2. Use a sharp knife to cut only the straps indicated in Table D-1 that corresponds to the option/language being installed.

Table D-1

KEYBOARD LANGUAGE OPTION STRAPS

Language	Option Number	Open Cut Strap[a]	Hex Code
Standard	–	none	00
United Kingdom	4A	E4	08
Swedish	4C	E2	02
APL	4E	E1	01
Danish/Norwegian	4F	E2 & E3	06

[a] These straps are labeled E1 - E4 on the circuit board, but are labeled W1 - W4 on the schematic sheet (A3-1).

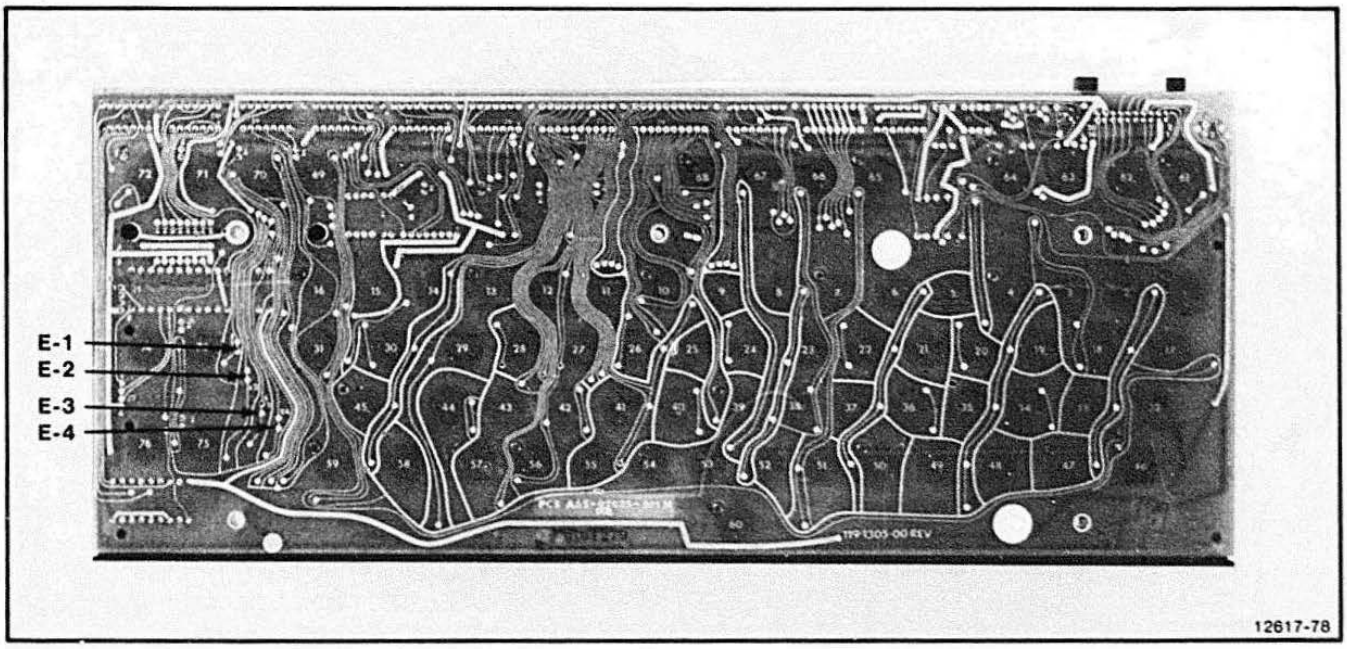

Figure D-5. Keyboard Circuit Board Strap Locations.

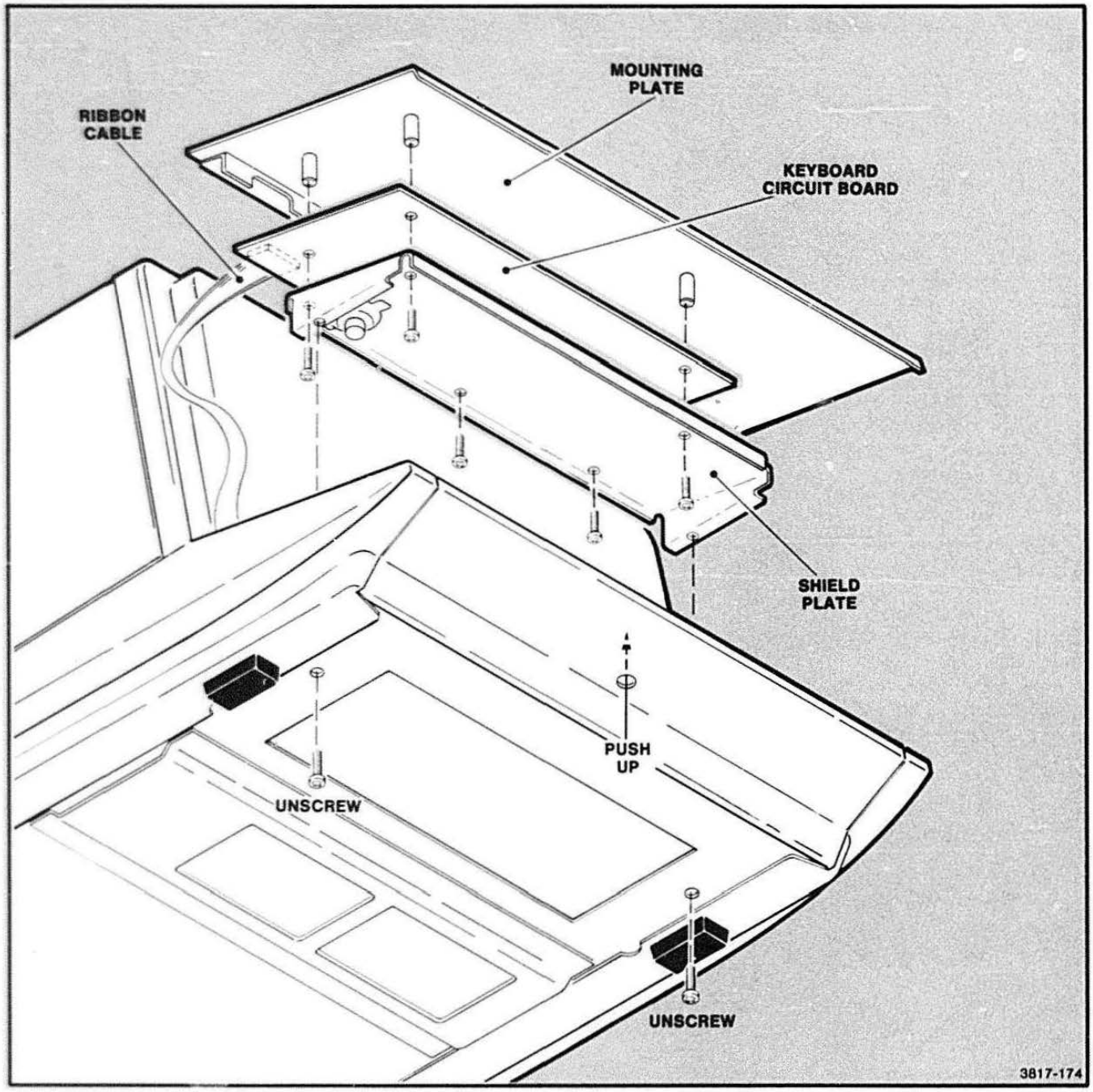

Figure D-4. Removing and Disassembling the Keyboard Assembly.

Reassembly:

1. Install the shield plate (with speaker), and circuit board, on the mounting plate using the five screws noted in step 4 above.

2. Plug the free end of the speaker wire onto the connector on the keyboard circuit board.

3. Reconnect the keyboard ribbon cable if it was disconnected. Be sure the connectors are mated in the proper direction. If the connectors are reversed, the PAGE FULL light will remain lit at Power-Up and the terminal will not function.

4. Place the keyboard assembly back in the terminal; a lip on each side of the opening supports the assembly. The front edge of the exposed plate is bent downward so it fits into the crevice along the front end of the terminal.

5. Replace the two Pozidriv® screws under the front part of the terminal (see Figure D-4 again).

REPLACING THE KEYBOARD KEYS

Options 4A, 4C, 4E and 4F all require new keyboard keys. Figures D-7 through D-10 show these new keys (the shaded keys are different than the standard character set). Tables D-2 through D-5 show the new code conversion charts.

The old key caps may be removed by simply pulling straight up on each key. A gripping device, such as a rubber glove, may facilitate removal of these keys from their switches. It is not necessary to remove the keyboard assembly from the terminal to replace these key caps.

Install the new key caps as follows:

1. First, position each key so that its nomenclature is pointing in the proper direction (not upside down or sideways). See Figure D-6.

2. Then insert the fork into the recepticle in the key switch plunger. Be sure the spring is still in place (around the plunger). Push the key cap all the way onto the switch so that it rests level with the other keys.

This completes the procedure.

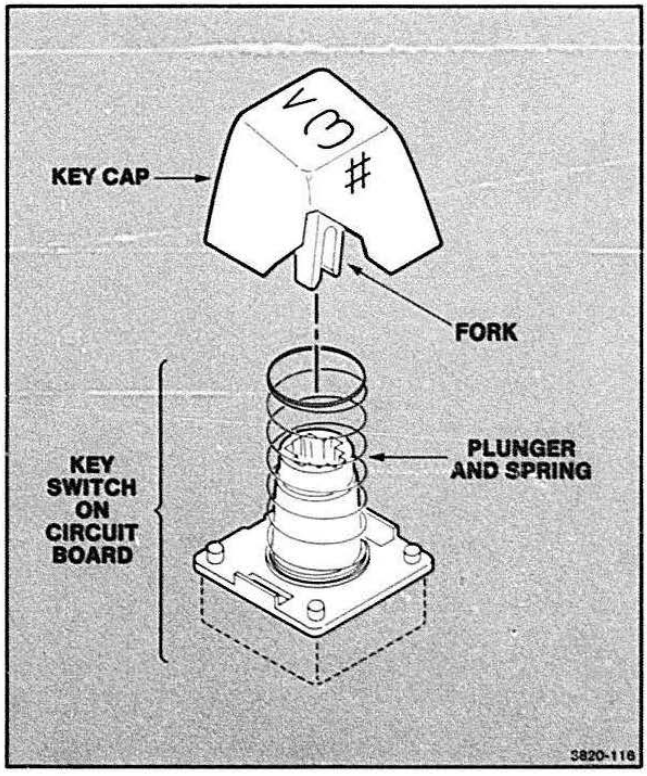

Figure D-6. Installing Replacement Key Cap.

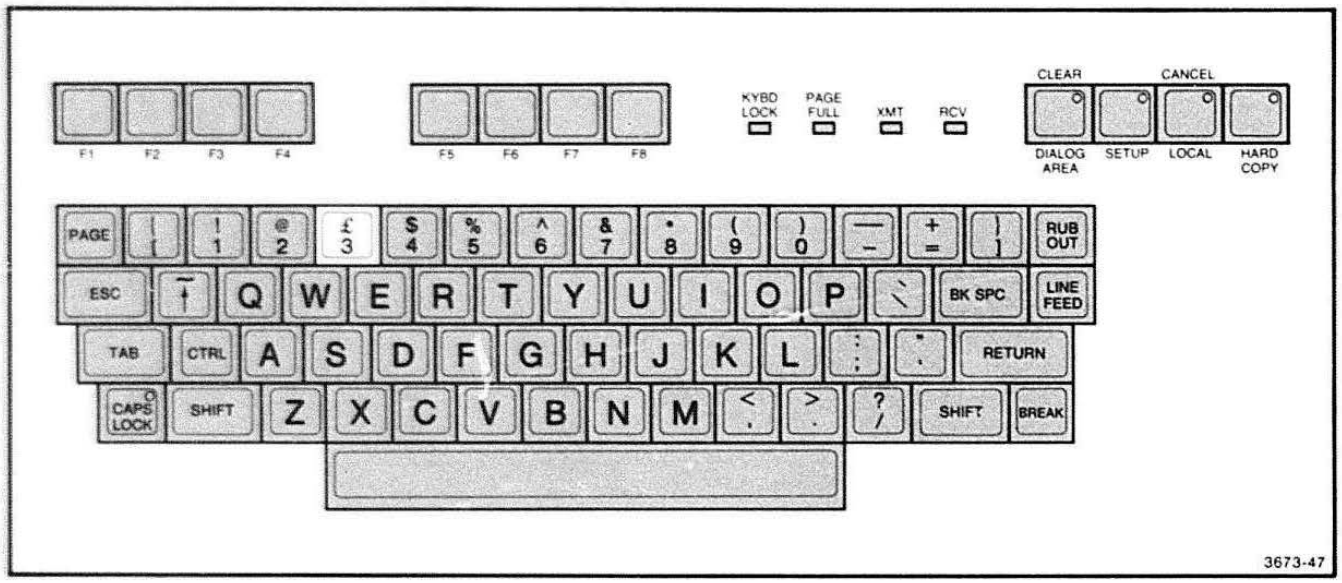

Figure D-7. United Kingdom Keyboard.

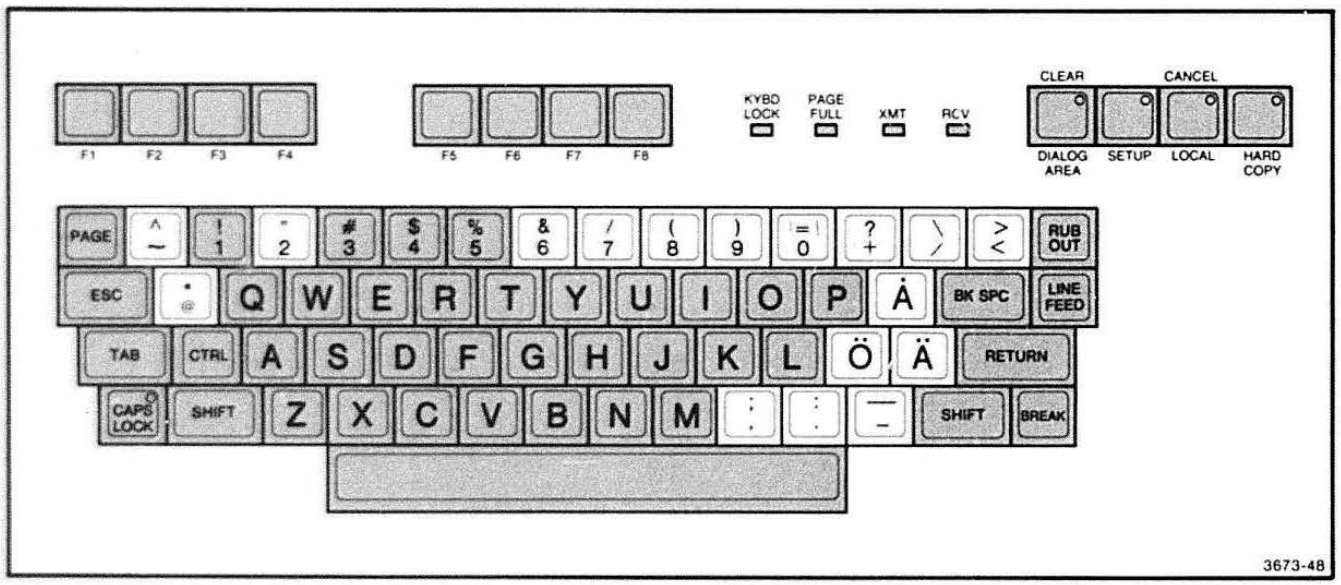

Figure D-8. Swedish Keyboard.

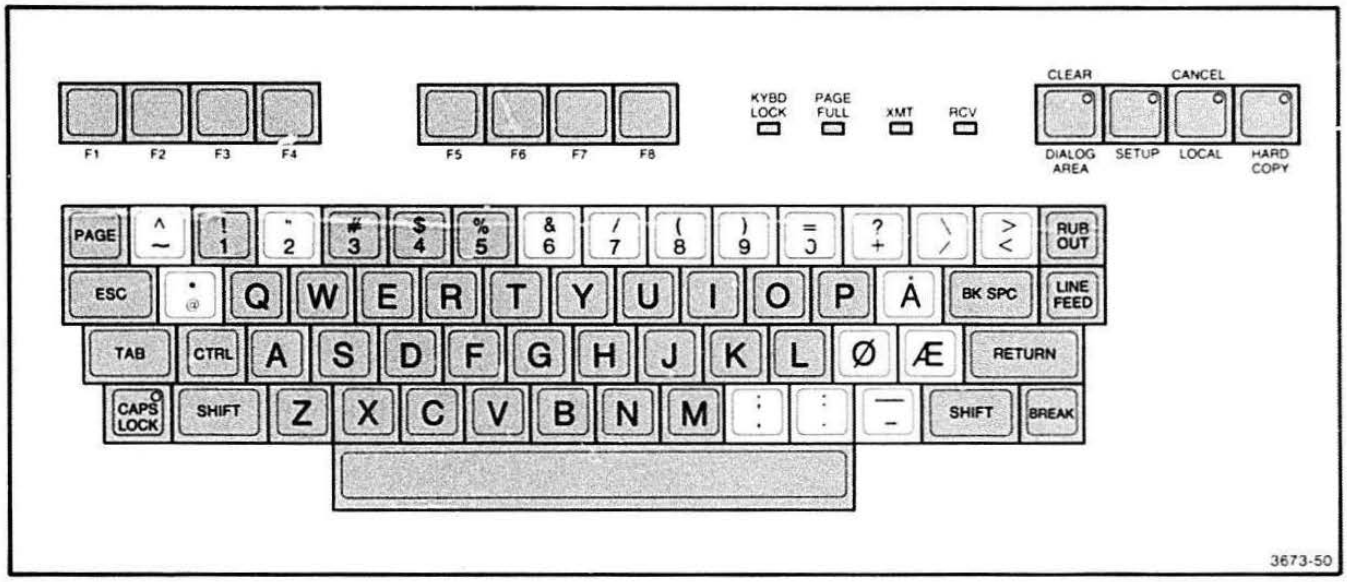

Figure D-9. Danish/Norwegian Keyboard.

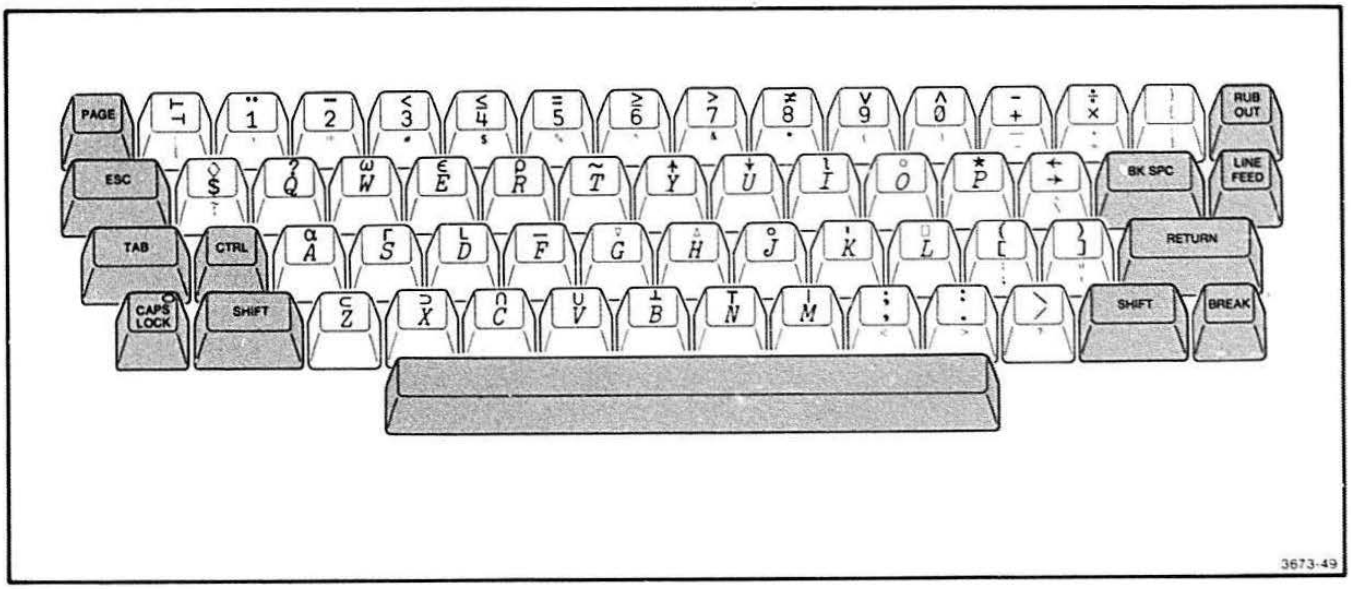

Figure D-10. APL Keyboard.

Table D-2

UNITED KINGDOM CHARACTER SET

BITS B4 B3 B2 B1	B7 B6 B5 = 0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
	CONTROL		HIGH X & Y GRAPHIC INPUT		LOW X		LOW Y	
0 0 0 0	NUL 0	DLE 16	SP 32	0 48	@ 64	P 80	\ 96	p 112
0 0 0 1	SOH 1	DC1 17	! 33	1 49	A 65	Q 81	a 97	q 113
0 0 1 0	STX 2	DC2 18	" 34	2 50	B 66	R 82	b 98	r 114
0 0 1 1	ETX 3	DC3 19	£ 35	3 51	C 67	S 83	c 99	s 115
0 1 0 0	EOT 4	DC4 20	$ 36	4 52	D 68	T 84	d 100	t 116
0 1 0 1	ENQ 5	NAK 21	% 37	5 53	E 69	U 85	e 101	u 117
0 1 1 0	ACK 6	SYN 22	& 38	6 54	F 70	V 86	f 102	v 118
0 1 1 1	BEL BELL 7	ETB 23	' 39	7 55	G 71	W 87	g 103	w 119
1 0 0 0	BS BACK-SPACE 8	CAN 24	(40	8 56	H 72	X 88	h 104	x 120
1 0 0 1	HT 9	EM 25	) 41	9 57	I 73	Y 89	i 105	y 121
1 0 1 0	LF 10	SUB 26	* 42	: 58	J 74	Z 90	j 106	z 122
1 0 1 1	VT 11	ESC 27	+ 43	; 59	K 75	[91	k 107	{ 123
1 1 0 0	FF 12	FS 28	, 44	< 60	L 76	\ 92	l 108	| * 124
1 1 0 1	CR RETURN 13	GS 29	- 45	= 61	M 77	] 93	m 109	} 125
1 1 1 0	SO 14	RS 30	. 46	> 62	N 78	^ 94	n 110	~ 126
1 1 1 1	SI 15	US 31	/ 47	? 63	O 79	_ 95	o 111	RUBOUT (DEL) 127

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Table D-3

SWEDISH CHARACTER SET

BITS B4 B3 B2 B1	B7 B6 B5 = Ø Ø Ø	Ø Ø 1	Ø 1 Ø	Ø 1 1	1 Ø Ø	1 Ø 1	1 1 Ø	1 1 1
	CONTROL		HIGH X & Y GRAPHIC INPUT		LOW X		LOW Y	
Ø Ø Ø Ø	NUL 0	DLE 16	SP 32	0 48	@ 64	P 80	\ 96	p 112
Ø Ø Ø 1	SOH 1	DC1 17	! 33	1 49	A 65	Q 81	a 97	q 113
Ø Ø 1 Ø	STX 2	DC2 18	" 34	2 50	B 66	R 82	b 98	r 114
Ø Ø 1 1	ETX 3	DC3 19	# 35	3 51	C 67	S 83	c 99	s 115
Ø 1 Ø Ø	EOT 4	DC4 20	$ 36	4 52	D 68	T 84	d 100	t 116
Ø 1 Ø 1	ENQ 5	NAK 21	% 37	5 53	E 69	U 85	e 101	u 117
Ø 1 1 Ø	ACK 6	SYN 22	& 38	6 54	F 70	V 86	f 102	v 118
Ø 1 1 1	BEL BELL 7	ETB 23	/ 39	7 55	G 71	W 87	g 103	w 119
1 Ø Ø Ø	BS BACK-SPACE 8	CAN 24	(40	8 56	H 72	X 88	h 104	x 120
1 Ø Ø 1	HT 9	EM 25	) 41	9 57	I 73	Y 89	i 105	y 121
1 Ø 1 Ø	LF 10	SUB 26	* 42	: 58	J 74	Z 90	j 106	z 122
1 Ø 1 1	VT 11	ESC 27	+ 43	; 59	K 75	Ä 91	k 107	ä 123
1 1 Ø Ø	FF 12	FS 28	, 44	< 60	L 76	Ö 92	l 108	ö 124
1 1 Ø 1	CR RETURN 13	GS 29	- 45	= 61	M 77	Å 93	m 109	å 125
1 1 1 Ø	SO 14	RS 30	. 46	> 62	N 78	∧ 94	n 110	~ 126
1 1 1 1	SI 15	US 31	/ 47	? 63	O 79	_ 95	o 111	RUBOUT (DEL) 127

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Table D-4

DANISH/NORWEGIAN CHARACTER SET

BITS B4 B3 B2 B1	B7 B6 B5 = 0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
	CONTROL		HIGH X & Y GRAPHIC INPUT		LOW X		LOW Y	
0 0 0 0	NUL 0	DLE 16	SP 32	0 48	@ 64	P 80	\ 96	p 112
0 0 0 1	SOH 1	DC1 17	! 33	1 49	A 65	Q 81	a 97	q 113
0 0 1 0	STX 2	DC2 18	" 34	2 50	B 66	R 82	b 98	r 114
0 0 1 1	ETX 3	DC3 19	# 35	3 51	C 67	S 83	c 99	s 115
0 1 0 0	EOT 4	DC4 20	$ 36	4 52	D 68	T 84	d 100	t 116
0 1 0 1	ENQ 5	NAK 21	% 37	5 53	E 69	U 85	e 101	u 117
0 1 1 0	ACK 6	SYN 22	& 38	6 54	F 70	V 86	f 102	v 118
0 1 1 1	BEL BELL 7	ETB 23	' 39	7 55	G 71	W 87	g 103	w 119
1 0 0 0	BS BACK-SPACE 8	CAN 24	(40	8 56	H 72	X 88	h 104	x 120
1 0 0 1	HT 9	EM 25	) 41	9 57	I 73	Y 89	i 105	y 121
1 0 1 0	LF 10	SUB 26	* 42	: 58	J 74	Z 90	j 106	z 122
1 0 1 1	VT 11	ESC 27	+ 43	; 59	K 75	Æ 91	k 107	æ 123
1 1 0 0	FF 12	FS 28	, 44	< 60	L 76	Ø 92	l 108	ø 124
1 1 0 1	CR RETURN 13	GS 29	- 45	= 61	M 77	Å 93	m 109	å 125
1 1 1 0	SO 14	RS 30	. 46	> 62	N 78	^ 94	n 110	~ 126
1 1 1 1	SI 15	US 31	/ 47	? 63	O 79	_ 95	o 111	RUBOUT (DEL) 127

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Table D-5

APL CHARACTER SET

BITS B4	B3	B2	B1	B7 B6 B5 = 0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
				CONTROL		HIGH X & Y GRAPHIC INPUT		LOW X		LOW Y	
0	0	0	0	NUL 0	DLE 16	SP 32	0 48	− 64	* 80	◇ 96	P 112
0	0	0	1	SOH 1	DC1 17	•• 33	1 49	α 65	? 81	A 97	Q 113
0	0	1	0	STX 2	DC2 18	) 34	2 50	⊥ 66	ρ 82	B 98	R 114
0	0	1	1	ETX 3	DC3 19	< 35	3 51	∩ 67	⌈ 83	C 99	S 115
0	1	0	0	EOT 4	DC4 20	≤ 36	4 52	⌊ 68	~ 84	D 100	T 116
0	1	0	1	ENQ 5	NAK 21	= 37	5 53	∈ 69	↓ 85	E 101	U 117
0	1	1	0	ACK 6	SYN 22	> 38	6 54	— 70	∪ 86	F 102	V 118
0	1	1	1	BEL BELL 7	ETB 23	] 39	7 55	∇ 71	ω 87	G 103	W 119
1	0	0	0	BS BACK-SPACE 8	CAN 24	∨ 40	8 56	Δ 72	⊃ 88	H 104	X 120
1	0	0	1	HT 9	EM 25	∧ 41	9 57	ι 73	↑ 89	I 105	Y 121
1	0	1	0	LF 10	SUB 26	≠ 42	(58	∘ 74	⊂ 90	J 106	Z 122
1	0	1	1	VT 11	ESC 27	÷ 43	[59	⍳ 75	← 91	K 107	{ 123
1	1	0	0	FF 12	FS 28	, 44	; 60	⍞ 76	⊢ 92	L 108	⊣ 124
1	1	0	1	CR RETURN 13	GS 29	+ 45	× 61	| 77	→ 93	M 109	} 125
1	1	1	0	SO 14	RS 30	. 46	: 62	⊤ 78	≥ 94	N 110	$ 126
1	1	1	1	SI 15	US 31	/ 47	\ 63	○ 79	- 95	O 111	RUBOUT (DEL) 127

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OPTIONS 24-29 (OPTIONAL RAM)

INTRODUCTION

To add optional RAM memory to the terminal, one or more RAM Controller boards must be installed in the card-cage. The RAM Controller board must be installed in a slot on the "Processor Bus." If no Processor Bus slot is available, then another optional interface board must be removed to make room for the new RAM Controller board.

Options 24 through 29 are achieved by the following configurations:

- Option 24 — One RAM Controller board. Includes 32K bytes of RAM, (one RAM Array board).
- Option 25 — One RAM Controller board. Includes 64K bytes of RAM, (two RAM Array boards).
- Option 26 — One RAM Controller board. Includes 96K bytes of RAM, (three RAM Array boards).
- Option 27 — One RAM Controller board. Includes 128K bytes of RAM, (four RAM Array boards).
- Option 28 — Two RAM Controller boards. Includes 256K bytes of RAM, (eight RAM Array boards).
- Option 29 — Four RAM Controller boards. Includes 512K bytes of RAM, (sixteen RAM Array boards).

TOOLS REQUIRED

These tools are required for the following installation procedure:

- Screwdriver, Pozidriv® #2
- Screwdriver, Pozidriv® #1
- Nut-driver, 5/16-inch

INSTALLATION

Step-by-step procedure:

1. Turn OFF terminal and disconnect power cord.
2. Remove four Pozidriv® screws from the back; remove two bolts from the bottom; and lift off cover panel. (See Figure D-1 again.)
3. Remove six screws from card-cage (see Figure D-2 again). Tip the card-cage up and back until it rests against wire bail. Watch all attached cables to be sure that none are pinched or pulled loose. If any cables are not long enough, reroute them or lengthen them (make new cables) to fit.
4. Check and verify that the J165 address straps on the RAM Controller board are as follows:

- 1st RAM Controller board - J165 in the "1" position
- 2nd RAM Controller board - J165 in the "2" position
- 3rd RAM Controller board - J165 in the "3" position
- 4th RAM Controller board - J165 in the "4" position
- 5th RAM Controller board - J165 in the "5" position
- 6th RAM Controller board - J165 in the "6" position

5. Install the RAM Controller board(s) in an empty Processor Bus slot(s).
6. Lift the locking lever/bail. Rotate card-cage down, being careful to not crush or pinch any cables. Replace the six screws removed in Step 3 of this procedure.
7. Place top cover on terminal and fasten with the screws and bolts removed in Step 2.
8. Plug in power cord and power-up the terminal.
9. Test the terminal by running Self-Test. (Press SELF TEST and MASTER RESET buttons.) Consult Section 10 of this volume if any error messages appear.

MEMORY QUANTITY VERIFICATION CHECK

Verify that the terminal's firmware recognizes all of the installed memory by comparing the user available memory to a calculated value. The command "STA MEM" typed in set-up mode will return two numbers. The first is the amount of memory available to the user and the second is the largest contiguous memory space. Both numbers returned are reported in units of memory blocks. One block is equal to 16 bytes of RAM. The second number is not needed here. To determine the available blocks of memory, thus verifying that optional memories are all functioning, do the following:

1. Plug in and power-up the terminal.
2. Run Self-Test and enter the Adjustment Self-Test mode.
3. Reset the CMOS RAM (press the MASTER RESET button).
4. Press CTRL and E keys to exit Self-Test.
5. Go into set-up mode (press SETUP key) and enter:

   STA MEM

   then press the RETURN key.
6. The amount of memory available and the largest contiguous memory space will be displayed on the screen.
7. Note the amount of available memory and compare with the calculated value for memory options installed.
8. Refer to Appendix F, *Memory Usage*. Compare the value on the screen with the calculated value determined by the procedure in Appendix F. Each optional RAM Array board contains 2048 bits (32K) of memory.

CHANGING THE LINE VOLTAGE

Two switches allow selection of either 115V or 230V nominal line voltage. The switches are accessible through the heat sink on the rear panel of the terminal. Follow this procedure:

1. Remove the power cord.

WARNING

To avoid electrical shock, make certain that the power is disconnected before changing the Line Voltage switches and fuse.

CAUTION

To avoid possible damage to the equipment, make certain that both switches are set to the same voltage.

2. Use a flatblade screwdriver to move the switches to the desired setting (Figure D-11).

3. Replace the fuse with one of the proper rating; refer to Table 11-1.

4. Replace the power cord with the proper type. The Mechanical Parts List gives part numbers and drawings identifying each type of optional power cord.

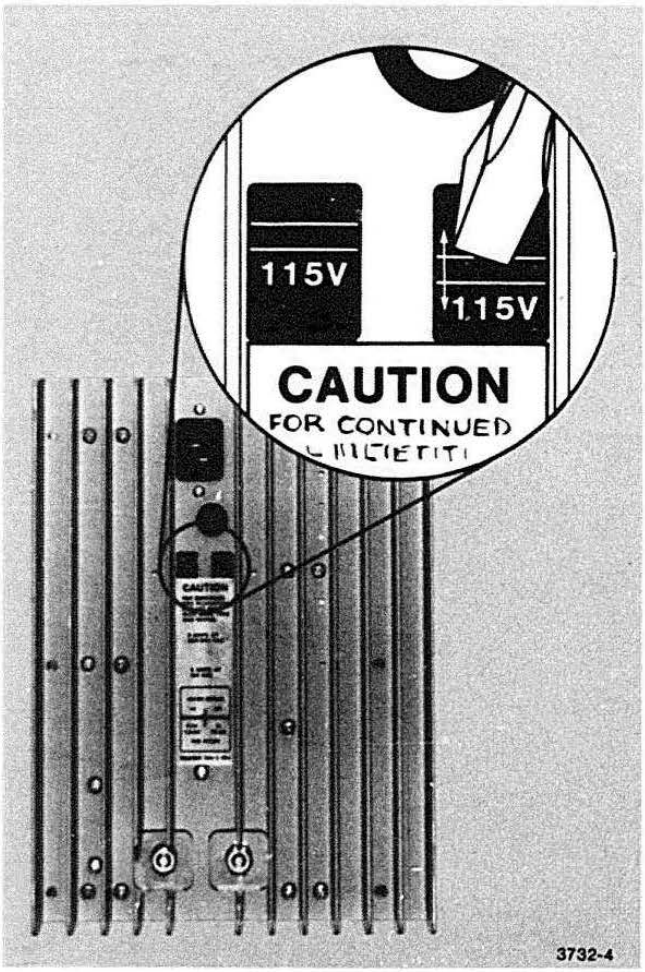

Figure D-11. Changing Line Voltage.

CHANGING THE LINE FREQUENCY

If the terminal is to be operated on 50 Hz power instead of the standard 60 Hz power, make the following alterations to the disk option hardware. This is the only modification required for such a change in line frequency.

The following tools are needed for this change:

- Allen wrench, 1/16-inch
- Nut driver, 5/16-inch (#10)
- Screwdriver, Pozidriv® #2

Step-by-step procedure:

WARNING

Unplug terminal and discharge large capacitors before working inside 4112.

1. Follow the procedures listed earlier in this section for removing the main cover and gaining access to the disk drive unit.
2. Remove the drive unit from the terminal.
3. Unplug the four cables from their connectors on the drive unit's circuit board. See Figure D-12A.
4. Remove the board's four mounting screws and remove the board. Use the screwdriver or 5/16-inch nut driver.
5. Slip the belt off of the drive motor pulley.
6. Loosen the Allen setscrew and remove the pulley (Figure D-12B).
7. Install the new belt and pulley. Part numbers for these items are listed at the end of the *Mechanical Parts List* (Section 9, Volume 2).
8. Reinstall the circuit board, and mount the drive unit in the terminal. Install the cover on the terminal.

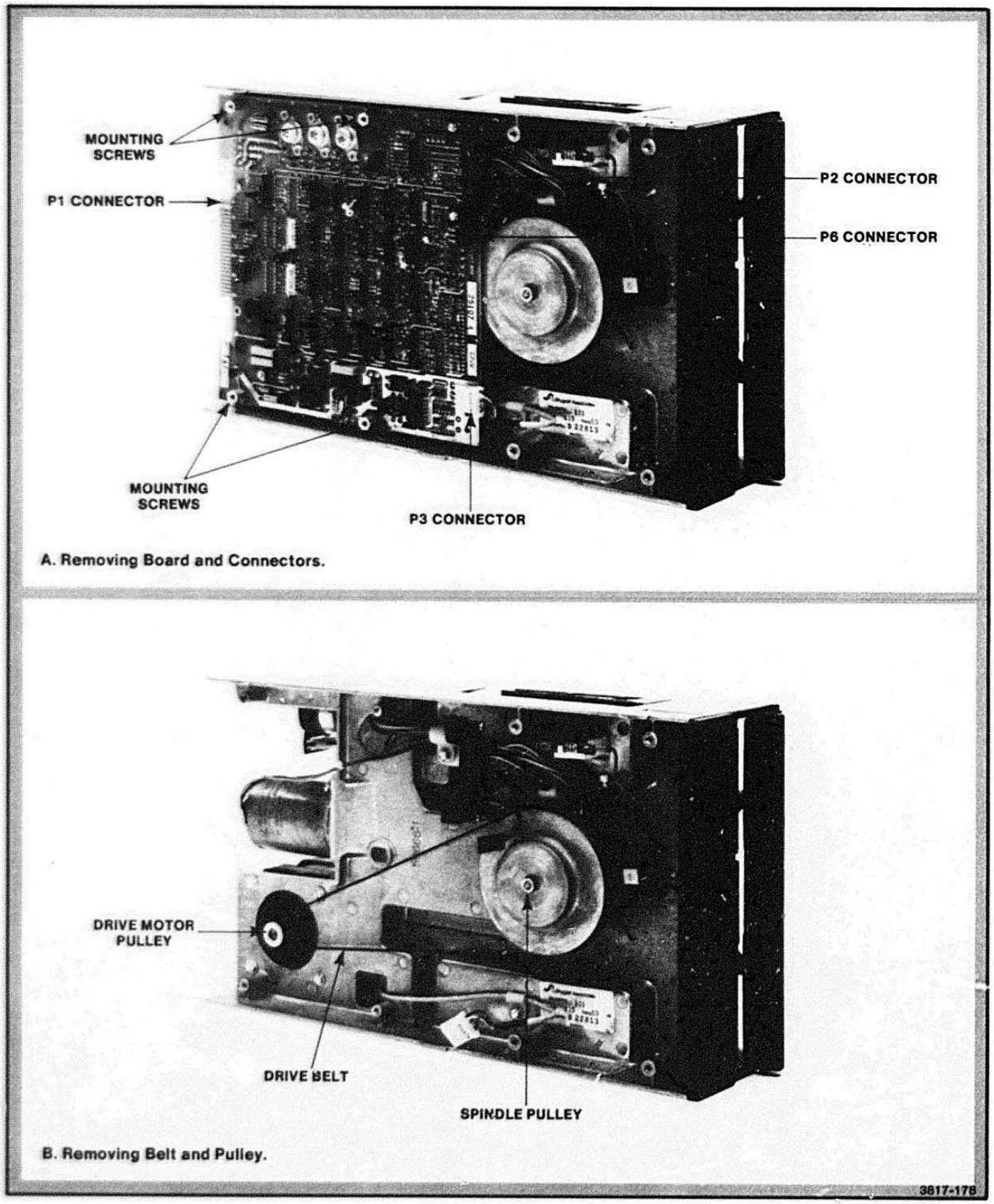

Figure D-12. Disk Drive Unit Belt and Pulleys.

Appendix E

RESTORING FACTORY DEFAULT SETTINGS

To restore the terminal's environment to the factory defaults, do the following steps:

1. Initiate Self-Test.

2. Within 20 seconds of initiating the Self-Test, enter CTRL C. The light in the CAPS LOCK key stops flashing and the following menu is displayed on the screen:

Figure E-1. Self Test Menu.

3. Press function key 2 (F2). The following menu appears on the screen:

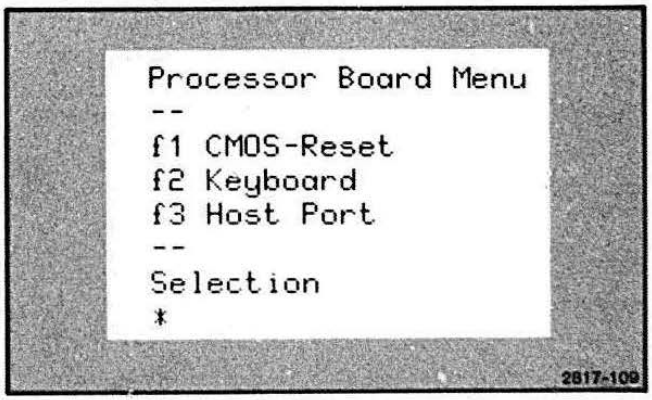

Figure E-2. Processor Board Menu.

4. Press function key 1 (F1). The following message appears below the menu:

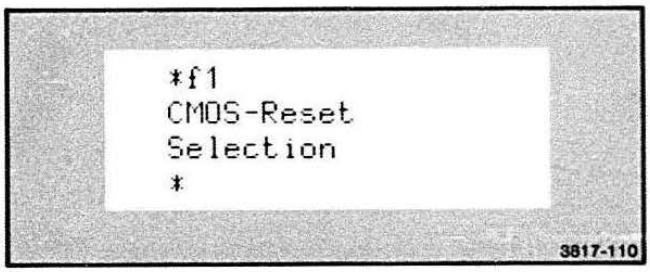

Figure E-3. CMOS Reset Message.

The term "CMOS Reset" means that the Setup memory has been restored to its factory default values.

5. Enter CTRL E. The terminal exits from the Self-Test procedure, runs the Power-Up sequence, and when the cursor appears, it is ready for use.

Appendix F

MEMORY USAGE

This appendix tells the user or service person how much available memory is installed in the 4112. "Available memory" is the amount of memory accessible to the user after the firmware has allocated its own use of RAM at power-up.

Use the STA MEM command to see how much memory *is* accessible. You may also calculate how much memory *should be* accessible; knowing which options are installed, use the procedure given here.

THE "STATUS MEMORY" COMMAND

The status memory command (STA MEM) tells the user how many blocks[1] of "free" memory is available for user programming.

To execute this command, press the SET UP and LOCAL keys (the red LED lights should light up) and type the letters STA MEM followed by a carriage return. This command provides two numbers. The first number is the amount of blocks of RAM memory available to the user. The second number indicates the largest contiguous memory space.

[1] A block of memory is equal to 16 bytes of RAM.

CALCULATING USER-AVAILABLE MEMORY

There are three areas that automatically use RAM upon power-up. These areas are (1) the dialog area (if enabled), (2) the communications queue area, and (3) some 4112 options.

The dialog area may be enabled and the parameters set in CMOS RAM. If this is done, the dialog area will be enabled upon power-up.

NOTE

The dialog area may be enabled but not visible. Under this condition, memory is still allocated to the dialog area even though the area is not visible.

Since the dialog area reserves memory for dialog (both local and from the host), this will subtract from the amount of "free" memory space. If the parameters are not set by the user, the dialog area is factory set for 15 lines (user definable by the DABUFFER command) with 73 characters to each line (user definable by the DACHARS command). This factory "default" allocates 180 blocks of RAM to the dialog area upon enabling. For the following discussion, it is assumed the dialog area is disabled (uses no RAM memory).

The communications queue area is an amount of memory allocated for communications from the host. If data is coming to the terminal at a high baud rate, the terminal may not be able to process the data as fast as it is received, and data must be stored in the communications queue. Another use for the queue occurs when the terminal is in Block mode. In this mode, the terminal waits until it has received a block of data before processing it.

The communication queue parameter is also stored in CMOS RAM (like the dialog area parameters) and are automatically established upon power-up. The communications queue space is user-definable (by the QUEUESIZE command). The factory default setting uses 24 blocks of memory space.

Some 4112 options require blocks of RAM in order to operate. With certain options installed, the amount of "free" memory available to the user is reduced.

Table F-1 shows the Communications queue, 4112 options, and the blocks of memory that each uses. Only the options listed require RAM memory to operate.

NOTE

All the values in Table F-1 are at power-up conditions. Special uses of options (such as down-loading information from a flexible disk into local memory) will require more blocks of memory.

Table F-1

USE OF RAM AT POWER-UP

Condition	Blocks of Memory
Standard 4112 (no options)	667
Communications Queue RAM (factory default setting)	−24
Option 01	−4
Option 10	−145
Option 13/14	−75
Option 42	−254
Option 10 and Option 13/14	+60[a]
Option 10 and Option 42	−1[b]

[a] The combination of these two options occupies 60 more blocks than the sum of the parts.

[b] The combination of these two options occupies 1 less block than the sum of the parts.

To calculate the amount of user-available memory, first determine the total RAM memory installed in the terminal. Then subtract from this total value the amount of RAM that the communication queue and each installed option requires (see Examples 1 and 2). The calculated net amount of memory is available at power-up. If the dialog area is enabled (at factory default parameters), subtract an additional 180 blocks of memory.

EXAMPLE 1: 4112 WITH OPTIONS 01 AND 42 INSTALLED

Standard 4112 memory	667 blocks
Communications Queue (factory default)	−24 blocks
Option 42, flexible disk drive	−254 blocks
Option 1, extended communications	−4 blocks
Blocks available to the user (upon power-up)	405 blocks

EXAMPLE 2: 4112 WITH OPTIONS 10, 13, 42, AND 27 INSTALLED

Standard 4112 memory	667 blocks
Option 27, additional 128K of RAM	+ (4x2048) blocks
Communications Queue (factory default)	−24 blocks
Option 10, 3PPI	−145 blocks
Option 13, graphics tablet	−75 blocks
Option 42, flexible disk drive	−254 blocks
Options 10 and 42 combined	−1 block
Blocks available to the user (upon power-up)	8360 blocks

Appendix G

MEMORY MAP

The 4112 terminal contains RAM and ROM on a number of circuit boards installed in the terminal. The microprocessor on the Processor board can address up to one megabyte of RAM/ROM memory on 20 address lines (ADR19-1 through ADR0-1). Figure G-1 shows the memory locations that the microprocessor designates for the terminal RAM/ROM.

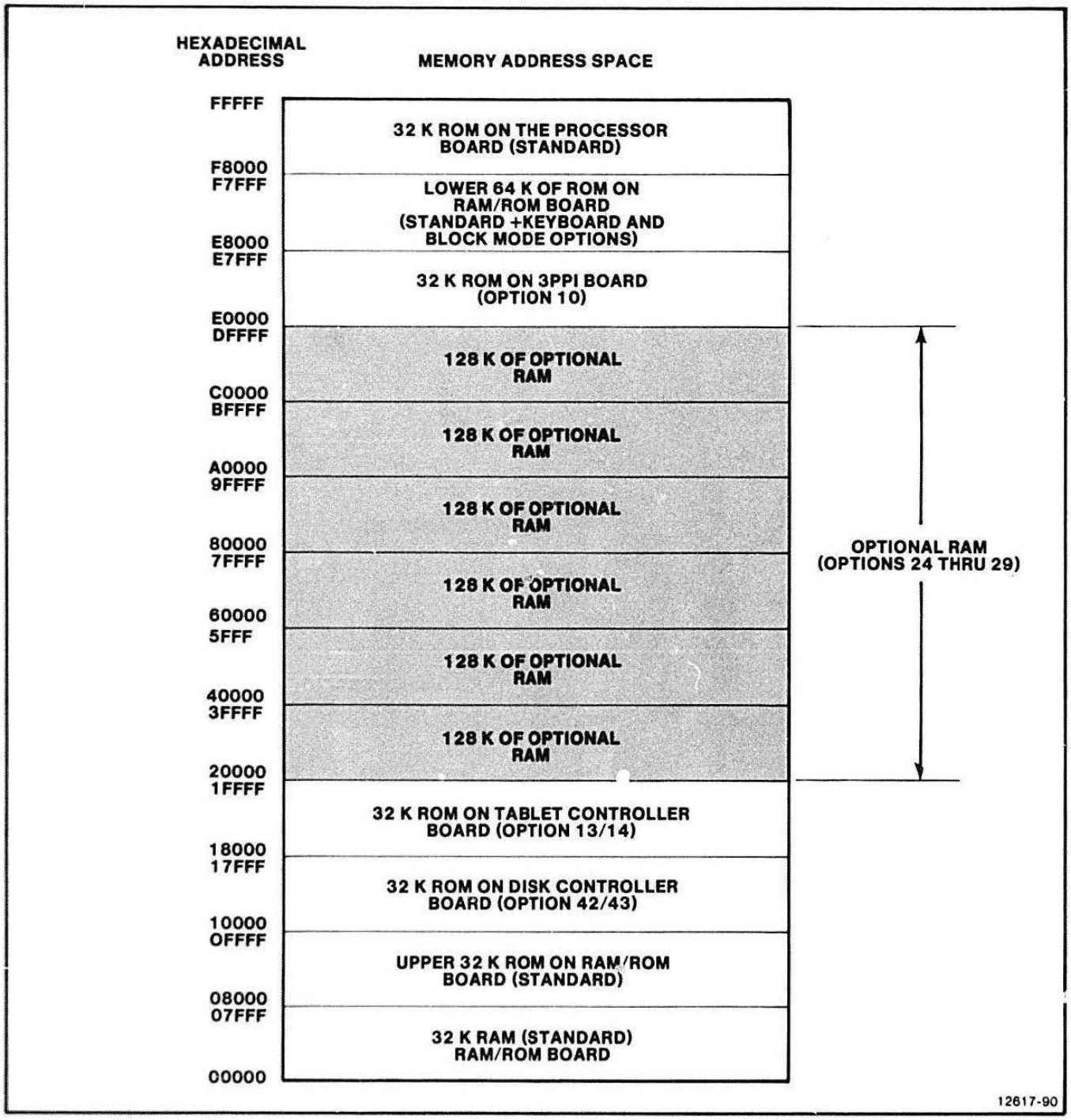

Figure G-1. 4112 Memory Map.