Tektronix®
COMMITTED TO EXCELLENCE

WARNING

THE FOLLOWING SERVICING INSTRUCTIONS ARE FOR USE BY QUALIFIED PERSONNEL ONLY. TO AVOID PERSONAL INJURY, DO NOT PERFORM ANY SERVICING OTHER THAN THAT CONTAINED IN OPERATING INSTRUCTIONS UNLESS YOU ARE QUALIFIED TO DO SO.

8002A
μPROCESSOR LAB
FLEXIBLE DISC UNIT
SERVICE MANUAL

Tektronix, Inc.
P.O. Box 500
Beaverton, Oregon 97077

Serial Number _____

070-2587-00

First Printing JAN 1979

WARRANTY

The 8001/8002A μProcessor Lab System and options, excluding customer supplied equipment, is warranted against defective materials and workmanship, under normal use, for a period of ninety (90) days from date of shipment. CRTs found to be defective after the ninety (90) day period and up to twelve (12) months from date of shipment will be exchanged at no charge for the material. Tektronix will repair or replace, at its option, those System components which Tektronix determines to be defective within the warranty period.

In addition, in those areas where Tektronix has service centers available for this system, on-site warranty repair is provided at no charge during the first ninety (90) days from date of shipment.

Tektronix shall be under no obligation to furnish warranty service if:

a. Attempts to install, repair, or service the equipment are made by personnel other then Tektronix service representatives.

b. Modifications are made to the hardware or software by personnel other than Tektronix service representatives.

c. Damage results from connecting the 8001/8002A μProcessor Lab System to incompatible equipment.

There is no implied warranty for fitness of purpose. Tektronix is not liable for consequential damages.

Printed in U.S.A. Specification and price change privileges are reserved.

PREFACE

About This Manual

Units Covered In This Manual

This manual presents service information on the 8002A μProcessor Lab Flexible Disc Unit. Coverage includes the flexible disc controller module, the +5-volt and +24-volt power supplies, and chassis-mounted parts. The flexible disc drive module has a separate service manual.

Intended Use Of This Manual

This manual is intended to be used by people who are knowledgeable in digital logic. It is not designed as a training tool. The manual provides detailed service information necessary to locate a trouble to a particular component on a circuit board.

DOCUMENTATION OVERVIEW

The 8001/8002A μProcessor Lab support documentation consists of two groups of manuals: user's manuals and service manuals. User's manuals, including Programmer's Reference and System User's manuals, explain the procedures required to operate the 8001/8002A μProcessor Lab system and its peripheral devices. They are identified by their gray covers and are a standard part of the system package.

Service manuals provide the information necessary to perform system testing and to repair system components. Service manuals are identified by their blue covers and may be purchased as optional accessories.

The following manuals contain service information for the 8001/8002A μProcessor Lab System:

8001/8002A μProcessor Lab Installation Guide

8001/8002A μProcessor Lab Service (optional)

8002A μProcessor Lab Flexible Disc Unit Service (optional)

Service manuals for
8001/8002A μProcessor Lab Emulator Processors (optional)

Service manuals for
8001/8002A μProcessor Lab optional modules (optional)

Service manuals for
8001/8002A μProcessor Lab peripheral equipment (optional)

TABLE OF CONTENTS

TABLE OF CONTENTS (cont)

TABLE OF CONTENTS (cont)

LIST OF TABLES

LIST OF ILLUSTRATIONS

OPERATORS SAFETY SUMMARY

The general safety information in this part of the summary is for both operating and servicing personnel. Specific warnings and cautions will be found throughout the manual where they apply, but may not appear in this summary.

TERMS

In This Manual

CAUTION statements identify conditions or practices that could result in damage to the equipment or other property.

WARNING statements identify conditions or practices that could result in personal injury or loss of life.

As Marked on Equipment

CAUTION indicates a personal injury hazard not immediately accessible as one reads the marking, or a hazard to property including the equipment itself.

DANGER indicates a personal injury hazard immediately accessible as one reads the marking.

SYMBOLS

In This Manual

This symbol indicates where applicable cautionary or other information is to be found.

As Marked on Equipment


DANGER — High voltage.


Protective ground (earth) terminal.


ATTENTION — refer to manual.

Grounding the Product

This product is grounded through the grounding conductor of the power cord. To avoid electrical shock, plug the power cord into a properly wired receptacle before connecting to the power input or output terminals. A protective ground connection by way of the grounding conductor in the power cord is essential for safe operation.

Use the Proper Power Cord

Use only the power cord and connector specified for your product.
Use only a power cord that is in good condition.

For detailed information on power cords and connectors, see (page/fig. ref.).

Refer cord and connector changes to qualified service personnel.

Use the Proper Fuse

To avoid fire hazard, use only the fuse specified in the parts list for your product, and which is identical in type, voltage rating, and current rating.

Refer fuse replacement to qualified service personnel.

Do Not Operate in Explosive Atmospheres

To avoid explosion, do not operate this product in an atmosphere of explosive gases unless it has been specifically certified for such operation.

Do Not Remove Covers or Panels

To avoid personal injury, do not remove the product covers or panels. Do not operate the product without the covers and panels properly installed.

Do Not Operate Without Covers (for TM 500 plug-ins only)

To avoid personal injury, do not operate this product without covers or panels installed. Do not apply power to the plug-in via a plug-in extender.

SERVICING SAFETY SUMMARY

FOR QUALIFIED SERVICE PERSONNEL ONLY

Refer also to the preceding Operators Safety Summary.

Do Not Service Alone

Do not perform internal service or adjustment of this product unless another person capable of rendering first aid and resuscitation is present.

Use Care When Servicing With Power On

Dangerous voltages exist at several points in this product. To avoid personal injury, do not touch exposed connections and components while power is on.

Disconnect power before removing protective panels, soldering, or replacing components.

Power Source

This product is intended to operate from a power source that will not apply more than 250 volts rms between the supply conductors or between either supply conductor and ground. A protective ground connection by way of the grounding conductor in the power cord is essential for safe operation.

8002A μProcessor Lab System with Optional CT8100 CRT Terminal and Prototype Control Probe.

Section 1

GENERAL INFORMATION

INTRODUCTION

The Flexible Disc is the mass storage device for the 8002A μProcessor Lab. The unit consists of a controller, two power supplies, and two disc drives (Drive 0 and Drive 1). The Flexible Disc Unit communicates directly with the System Processor module in the μProcessor Lab through an interconnecting cable.

Drive 0 is the default system drive. This drive is automatically accessed whenever a file name is specified without a drive number. The flexible disc that contains the system programs is normally placed in this drive. Drive 1 usually contains a second flexible disc that is used primarily for storing user files, modifying user files, or as a scratch data area. A second Flexible Disc Unit with two disc drives may be connected to the μProcessor Lab by special arrangement.

DESCRIPTION

The Flexible Disc Unit operates under direct control of the System Processor through parallel I/O control and data ports, as shown in Figs. 1-1 and 1-2. Data is written from or read into the System Processor in parallel 8-bit bytes; a single data transfer operation via the data port comprises 128 bytes of data, as well as the command and status bytes. For any operation (read or write) it commands, the System Processor always supplies the addresses of the Disc Drive and of the starting track and sector of the flexible disc to be selected by the Flexible Disc Controller. The Flexible Disc Controller performs all signal sequencing and data formatting for the Disc Drive. Data is transferred serially between the Controller and the Disc Drive.

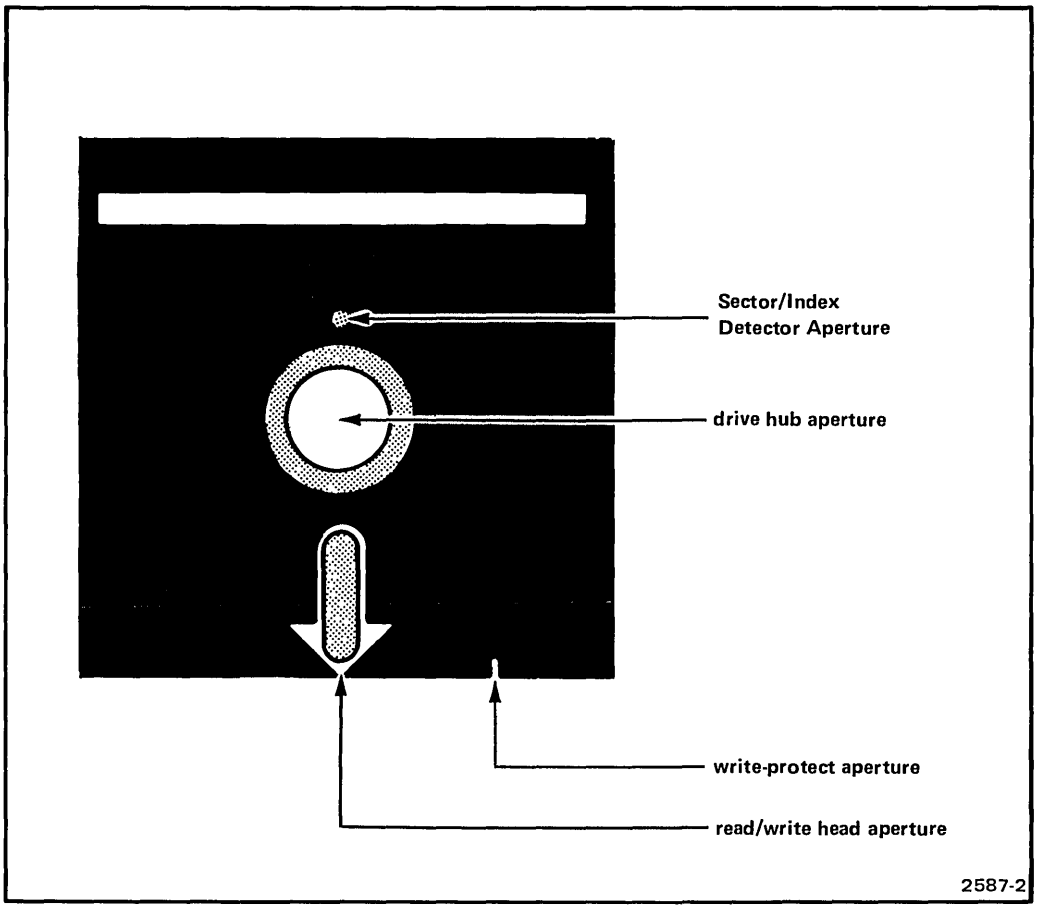


Fig. 1-1. Flexible Disc.

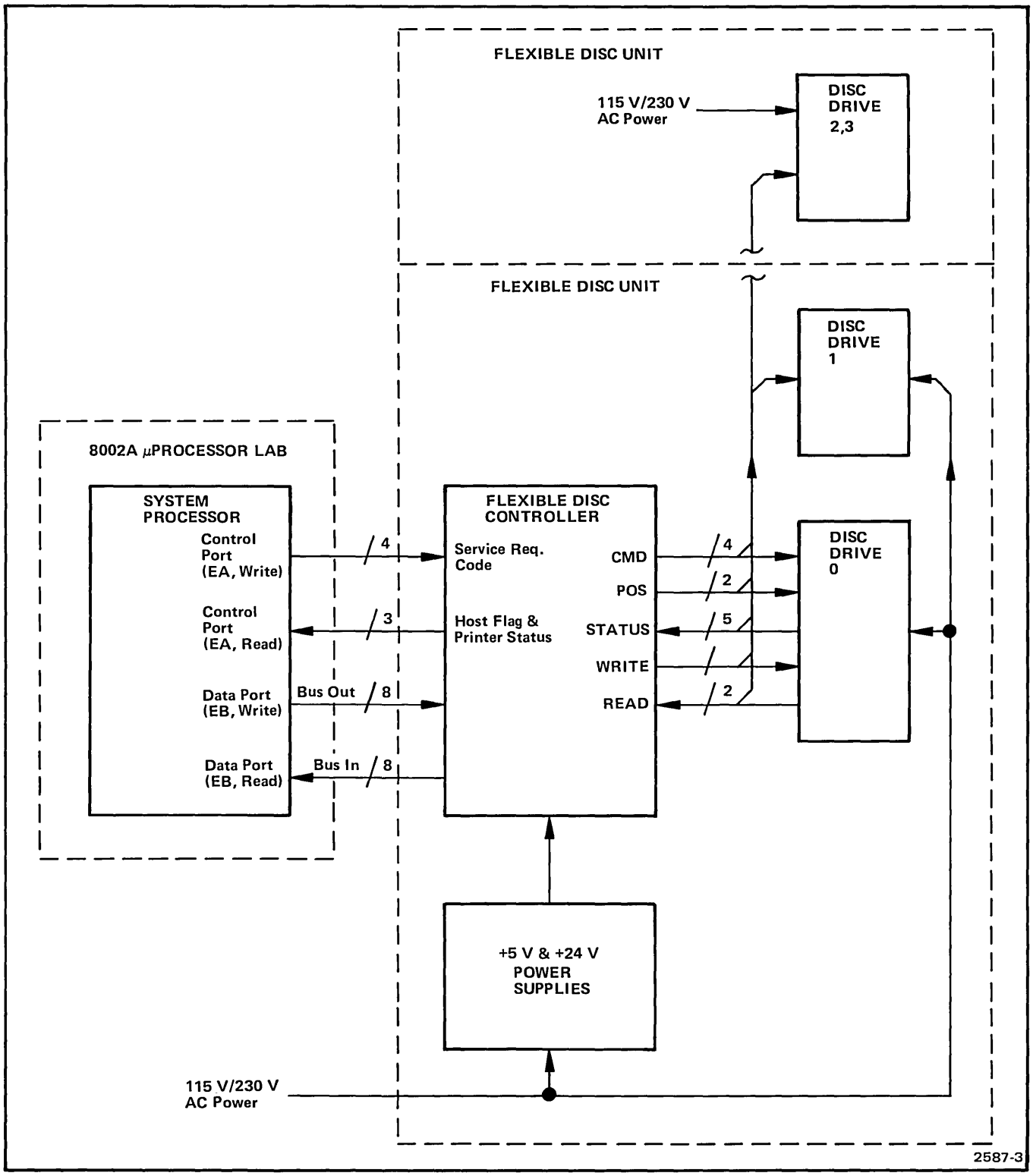


Fig. 1-2. Flexible Disc Unit, Simplified Block Diagram.

FLEXIBLE DISC FORMAT AND CONTENTS

The recording medium is a single-sided, oxide-coated flexible disc, enclosed within a protective plastic jacket. This jacket has openings for the drive hub, the read/write head, the write-protect detector, and the sector/index detector. (Refer to Fig. 1-3.) The Flexible disc is organized into 77 concentric recording tracks. Track 00 is located at the outer edge of the disc, and track 76 is located closest to the center of the disc. Refer to Fig. 1-4. Each track is divided into 32 equal recording areas, called sectors. The start of each sector is identified by a sector hole, from which a corresponding SECTOR pulse is derived. The number of each sector is established relative to a single index hole, located between Sector 31 and Sector 00. An INDEX pulse, derived from the index hole, marks a full rotation of the disc and the start of the recording tracks. Table 1-1 shows the application of disc organization to 8002A μProcessor Lab system programs. (Refer to the 118-0195-00 Flexible Disc Drive service manual for more information about disc construction and organization.)

Recording Method

The 8002A Flexible Disc Unit uses the Double Frequency FM (DFFM), Non-Return to Zero (NRZ) recording method. The recorded (raw) data includes a coded mix of clock pulses and data pulses representing logic 1s. During writing, the raw data is encoded from true data by the Flexible Disc Controller (WRT DATA signal). During reading, the raw data is separated into the SEP CLK and SEP DATA signals by the electronics within the Disc Drive. (Refer to the 118-0195-00 Flexible Disc Drive service manual for additional information about the recording method.)

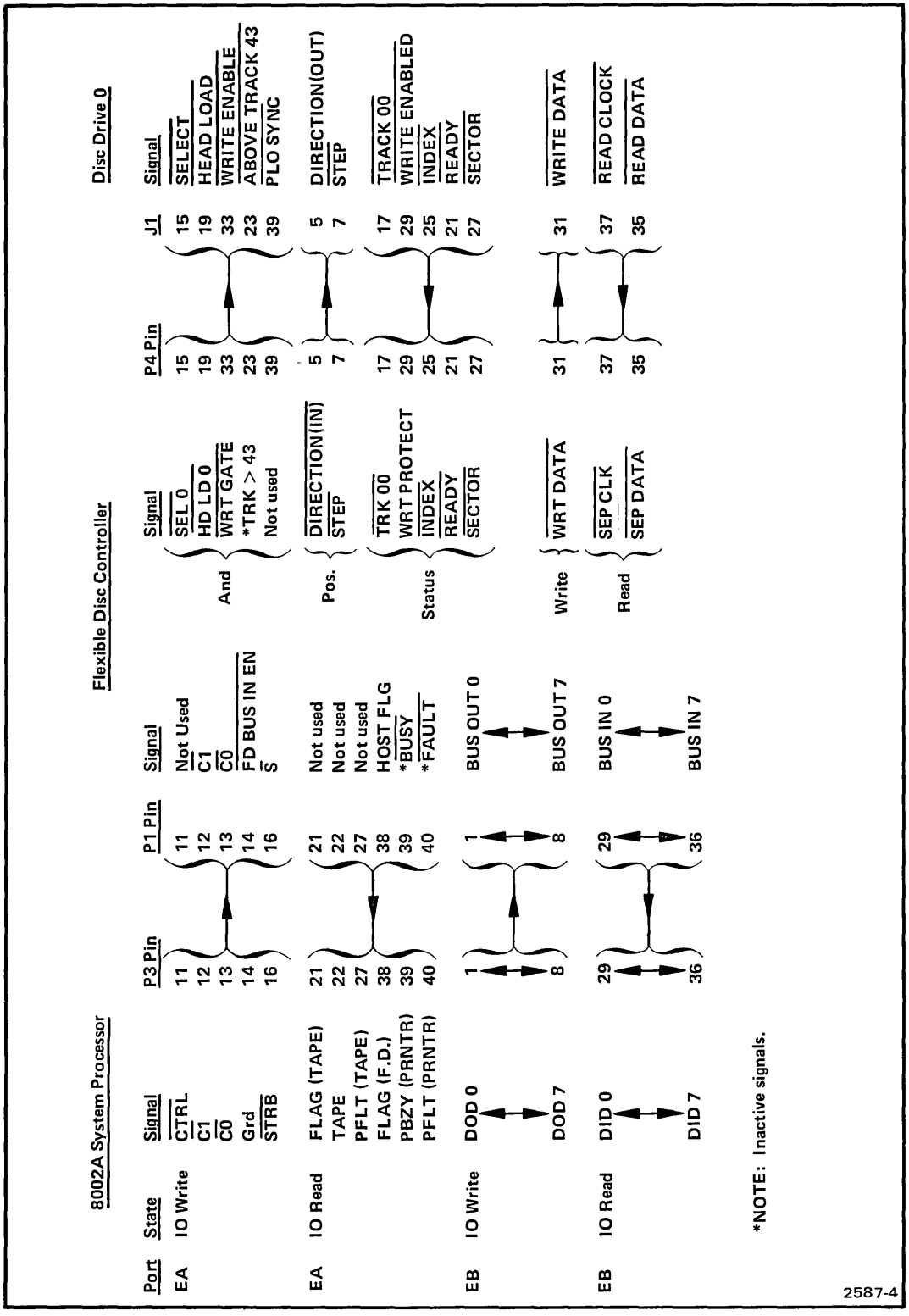


Fig. 1-3. Flexible Disc Unit Interface Diagram.

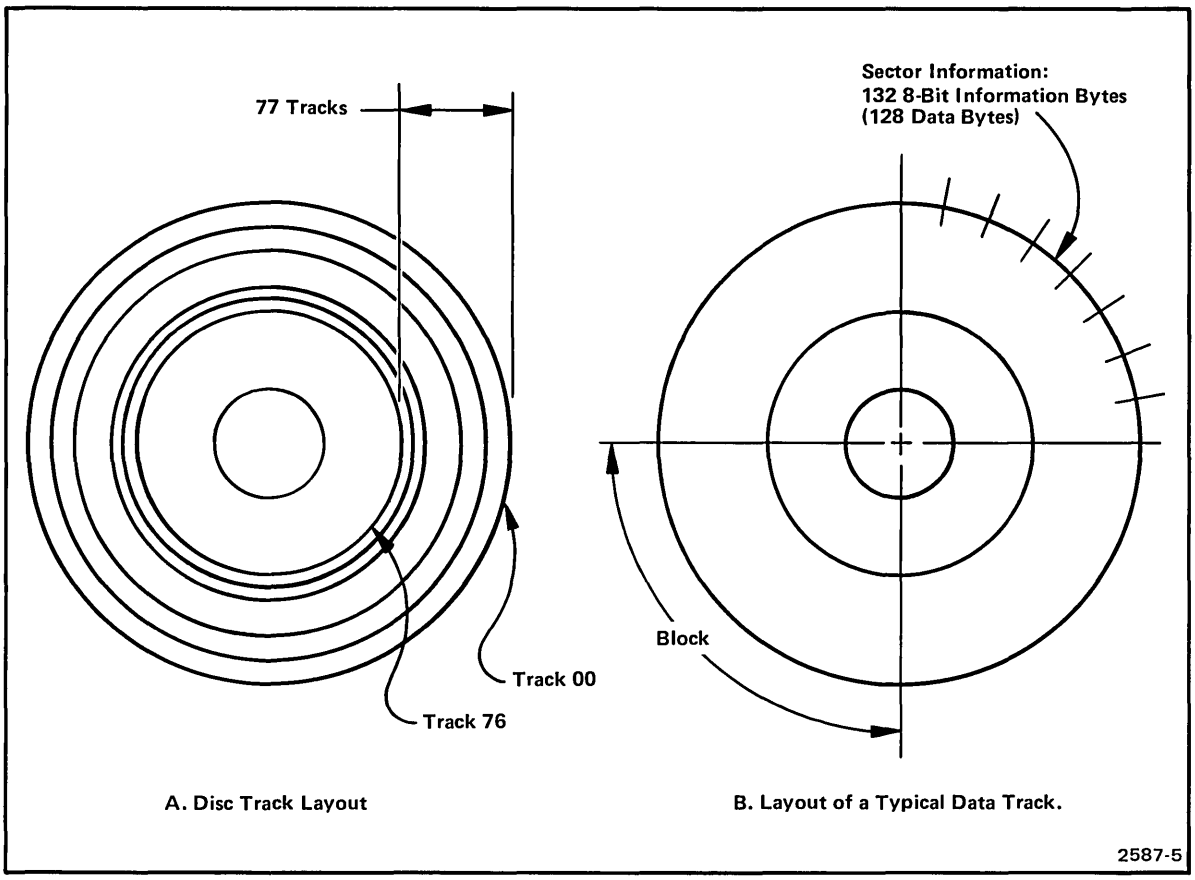


Fig. 1-4. Flexible Disc Organization.

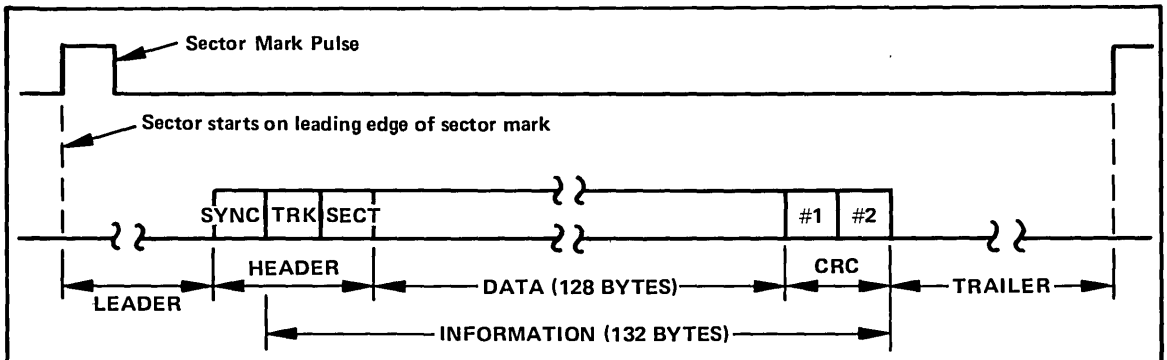
Peak Shift Precompensation (Prestressing)

Peak shift precompensation of data described in the service manual for the Disc Drive is not applicable to present 8002A μProcessor Lab systems.

Sector Data Format

The information recorded in a sector is identified in Fig. 1-5. The 0's forming the leader (preamble) and trailer (postamble) provide a tolerance that offsets variations in mark pulse timing between different Disc Drives. This tolerance ensures that the sync byte can be detected and that the information bytes be correctly retrieved.

Three header bytes are supplied by the Flexible Disc Controller each time a sector is written; the header is provided even when the μProcessor Lab supplies only the initial track and sector numbers for data blocks exceeding 128 bytes. The CRC (Cyclic Redundancy Code) word is generated by the Flexible Disc Controller during writing operations, and is used for a parity check of read data.



Format and Restrictions:

1. LEADER = 128 Bits, all 0's = 16 Bytes

2. SYNC BYTE = fixed at FB_{16} =

7							0
1	1	1	1	1	0	1	1

3. TRACK BYTE = Track Address Not Greater Than 76_{10}

4. SECTOR BYTE = Sector Address Not Greater Than 31_{10}

5. DATA BYTES = No Restrictions

6. CRC WORD = CRC Bytes 1 and 2

7. TRAILER = All 0's; Number (Length) Varies

2587-6

Fig. 1-5. Sector Recording Format.

Table 1-1

8002A μProcessor Lab Disc File Structure

General Format:	128 bytes/sector; 8 sectors/block; 4 blocks/track. 77 tracks/disc; 304 track blocks/disc (track 00 excluded); 2432 track sectors/ disc.
Track 00:	Disc File
Sector 0:	Bytes 0, 1: Millisecond Identification. Byte 2: Number of Active Files (Directory Names). Bytes 3-51: Disc Identifier. Bytes 52-89: Bad Block Bit Maps. Bytes 90-127: Master Bit Maps.
Sectors 1-5:	Directory (8 Bytes/Entry); 16 files per sector, except for 14 files in Sector 5. Bytes 0-7: File Name.
Sectors 6-31:	File Bit Maps (41 Bytes/File). Bytes 0-37: Bit Map for File (304 Bits). Bytes 38, 39: Number of Sectors Used. Byte 40: Number of Data Bytes in Last Sector.
Tracks 1-4:	Operating System
Tracks 5-76:	Files

NOTE

Due to directory limitations, a maximum of 78 files can be contained on one disc. The disc operating system and directory (Tracks 0-4) occupy the remaining capacity.

Sector Interleaving

Sectors are written sequentially in the following manner: sector 00, sector 16, sector 01, sector 17 . . . This pattern is called sector interleaving, and is produced by the Flexible Disc Controller. Interleaving increases system performance during multiple sector record transfers.

DISC DRIVE

The Disc Drive rotates a flexible disc at a constant 360 rpm, mechanically positions and engages (loads) the read/write head, and electrically writes or reads data. In the 8002A μProcessor Lab systems, two or four Disc Drives can be used. Only one drive may be accessed at any time. The accessed drive is determined by which SEL DR signal is activated; the Flexible Disc Controller activates one of the SEL DR signals in response to a μProcessor Lab command.

Drive Selection

Before a Disc Drive may be accessed, all drives must be up to speed, have flexible discs installed, and dc power steady. The status of all drives is determined by the Flexible Disc Controller from the wire-ORed READY signal, which enables drive selection. Following application of primary power to a Disc Drive, approximately 2.5 seconds are required for the drive to come up to speed, as shown in Fig. 1-6. The SEL DR signal, which enables the input and output gates of the selected Disc Drive, is supplied by the Flexible Disc Controller in response to a command from the μProcessor Lab.

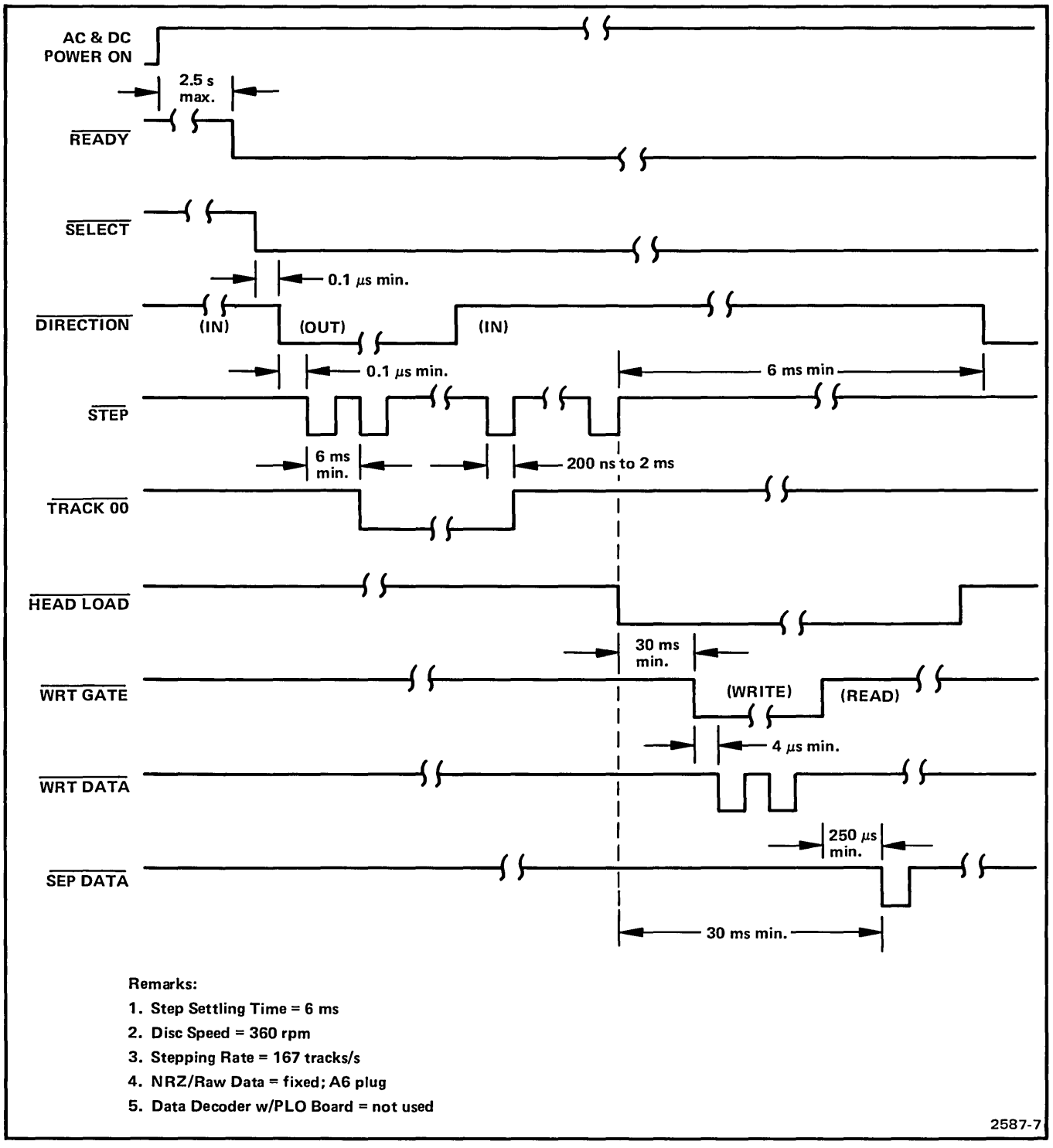


Fig. 1-6. Disc Drive Interface Timing.

Track Selection

One of the 77 recording tracks is accessed by the head carriage. The carriage is mechanically positioned by the Disc Drive in response to the DIRECTION (IN) and STEP commands from the Flexible Disc Controller. The DIRECTION (IN) signal (low=in; high=out), which must precede the first STEP pulse by at least 0.1 μs, determines whether the head carriage moves in (toward track 76) or out (toward track 00). The head carriage moves one track position for each STEP pulse received; STEP pulses occur at a rate of 167 pps (6 ms per track).

Track positioning is relative to track 00 position. When the head carriage is aligned with track 00, the Disc Drive sends an active TRK 00 signal to the Flexible Disc Controller. The controller uses this signal as a reference for STEP-pulse counting. If an access (position) error occurs, the Flexible Disc Controller may recover either by commanding the head carriage out to track 00 or by reading the header (ID) of a sector in the present, unknown track.

Head Loading

The Flexible Disc Controller readies the selected Disc Drive for reading or writing by sending the appropriate HD LD command, which causes the read/write head to engage the flexible disc. This is called head loading. Only one Disc Drive is loaded at a given time; the head may remain loaded while changing tracks. As shown in Fig. 1-6, a 30-ms delay for settling is required after initial head loading before data may be written or read; only 10 ms of settling time is required after changing tracks with the head loaded.

Sector Selection

As shown in Fig. 1-5, the SECTOR pulse issued by the Disc Drive marks the start of a disc sector. The number of the sector equals the number of SECTOR pulses counted by the Flexible Disc Controller following an INDEX pulse from the Disc Drive. Thus, data is not sent during writing and is not normally accepted by the Flexible Disc Controller during reading until the correct sector count has been reached. This enables the Disc Drive to read data continuously, which is useful when sector IDs must be read by the Controller before a read or write operation.

Reading or Writing Data

A write or read operation is commanded by the WRT GATE signal from the Flexible Disc Controller after head positioning and loading. Writing is selected if the signal is low (active); reading is selected if the signal is high. Writing is inhibited if the WRITE PROTECT status signal from the Disc Drive is active, signifying that the flexible disc is prerecorded and has the write-protect hole uncovered.

For writing, data is transferred serially from the Flexible Disc Controller one sector at a time via the WRT DATA line. The signal presented to the Disc Drive is an encoded composite of clock and data pulses. Write data timing is shown in Fig. 1-7. (The >TRK 43 command from Flexible Disc Controller, which reduces the current drive to the read/write head, is inactive in present 8002A μProcessor Lab system.)

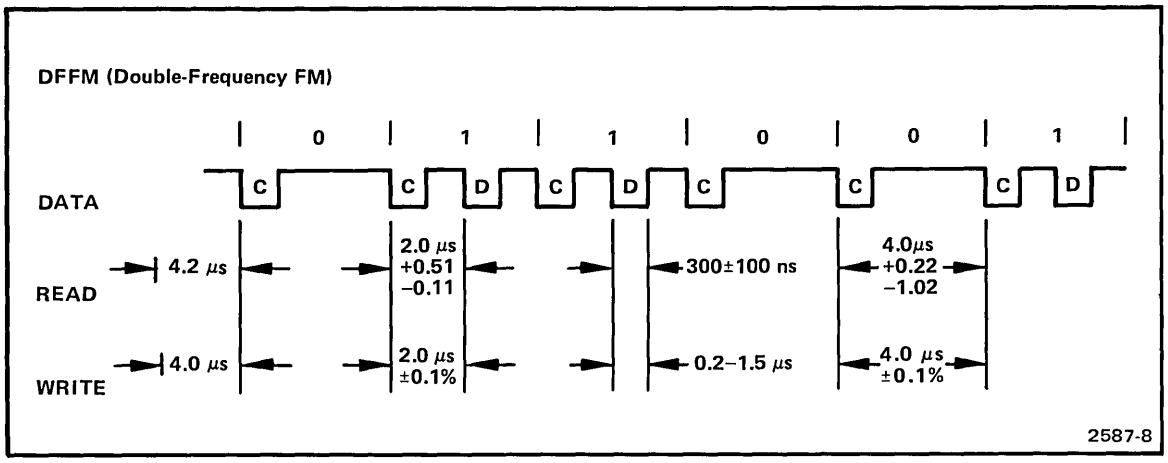


Fig. 1-7. Read and Write Data Timing.

During a read operation, the raw data from a disc is separated by the Disc Drive into the clock (SEP CLK) and data (SEP DATA) components. The Disc Drive transfers a full sector of information serially to the Flexible Disc Controller as reading occurs. Read data timing is shown in Fig. 1-7.

FLEXIBLE DISC CONTROLLER

The Flexible Disc Controller is a dedicated microcontroller that includes a full instruction set stored in ROM; a sector buffer for temporary, bidirectional (read or write) data storage; a drive control multiplexer; and 16 working registers (R0-R15). Present 8002A μProcessor Lab systems permit a maximum of four drives. (A line printer control circuit also is included in the Controller, but the circuit is not used by the μProcessor Lab, which instead uses the System Communications module for I/O control of optional peripherals.)

The Flexible Disc Controller has two primary functions. It selects and controls Disc Drives in response to program commands from the System Processor, and it formats data transferred bidirectionally between the System Processor and the selected Disc Drive. Addresses used in selecting the Disc Drive and the disc's initial track and sector are supplied by the System Processor for either a write or a read operation. All I/O operations are under direct control of the System Processor.

Controller I/O Operations

The timing and type of operation to be performed by the Controller are determined in an interlocking (handshake) manner by the System Processor via its parallel control ports. The Controller routinely monitors the strobe (S) bit of the input control code from the System Processor. (Figure 1-8 shows the format of the Controller input and output control bytes.) When the Controller is ready to perform a new operation, it decodes the service request, stores the input control code in working register R8 and activates the HOST FLAG bit at its output control port. By setting the HOST FLAG bit, the Controller acknowledges that it is ready to perform the new operation. The System Processor inactivates the strobe (S) bit of the input control code when it detects the acknowledge; in turn, the Controller inactivates the flag bit when the service routine is finished. In this way, the Controller indicates that it is aready for a new operation.

8002A μPROCESSOR LAB

INTERNAL CONTROL BYTE = Addr EA (Write)

Bit Function	Not Used	Not Used	PNTR INT EN	F.D. INT EN	F.D. CTRL	$\overline{C1}$	$\overline{C0}$	$\overline{STRB}$
Bit	7	6	5	4	3	2	1	0
Fixed Level	1	1	0	1	1	V	V	V

INPUT TAPE READER STATUS BYTE (NOT USED)

P3 Pin	27	26	25	24	23	22	21	20
Bit Function	$\overline{PFLT}$	Not Used	←	→	Not Used	TAPE	FLAG	Not Used
Bit	7	6	5	4	3	2	1	0

INTERNAL STATUS BYTE = Addr EA (Read)

Bit Function	FLAG	TAPE	Not Used	←	→	Not Used	$\overline{PFLT}$	$\overline{PBZY}$
Bit	7	6	5	4	3	2	1	0
Fixed Level	V	1	1	1	1	1	0	1

FLEXIBLE DISC CONTROLLER

INPUT CONTROL/STATUS BYTE

	$\overline{TRK\ 00}$	$\overline{INDEX}$	$\overline{C0}$	$\overline{SECTOR}$	$\overline{C1}$	$\overline{S}$	Not Used	DRIVE NOT READY
Input CSW	7	6	5	4	3	2	1	0
	V	V	V	V	V	V	1	V

Input CSW is stored in Working Register R3 via $\overline{WR}$ Bus on 'Input CSW' instruction; status bits 0, 4, 6, and 7 are obtained from Disc Drives.

SERVICE REQUEST

Code

C1	C0	$\overline{S}$	Label	Function
1	1	1	RST	Reset circuits
1	1	0	SIO	Start I/O
1	0	0	OTD	Receive Data
0	0	0	IND	Send Data

Not Used
(No Connections)

FLAG bit goes true to acknowledge host strobe; goes false after host strobe ends and service request is completed. Indicates Controller is ready to receive or send data.

HOST FLAG bit set to 1 (true) by 'Host Flag' instruction; $\overline{BUSY}$ and $\overline{FAULT}$ bits are constant levels (Printer Control Circuit inactive).

NOTES:
- V = active bit.
- 1 = high level.
- 0 = low level.
- N.C. = no connection

2587-9

Fig. 1-8. Control Port Formats.

The input control code to the Controller requests one of four I/O services:

(1) SIO: start a new I/O operation sequence; the sequence will be defined by the command byte presented in the next operation. SIO initializes Controller circuits.

(2) OTD: receive output data that is available on the BUS OUT lines. This request must be repeated for each byte placed at the output data port.

(3) IND: place input data on the BUS IN lines. This request must be repeated for each byte presented to the input data port.

(4) RST: reset all control circuits. This request is issued at the end of an I/O operation sequence, to prepare the Controller for a new sequence.

The data ports are used in parallel with the control ports to perform the following operations: (1) define the operation sequence to be performed by the Controller (command bytes); (2) report the status of the Disc Drive I/O operations (disc status byte); (3) send or receive address and data bytes (device number, sector number, track number, and data bytes); and (4) report the contents of the working registers after a fault has been reported. Figure 1-9 shows the format of the Controller input and output bytes applied to the System Processor data ports.

The sequence of events following an SIO request depends on the operating mode selected by the subsequent command byte appearing at the output data port of the System Processor. Except for the diagnostic read mode, all I/O operation sequences begin with the transmission of three address bytes; for diagnostic reading of the Controller working registers, no drive or disc addresses are required, since the information is already contained in the Controller. The unique I/O operation sequences are described in the following paragraphs. Table 1-2 lists these I/O sequences.

COMMAND BYTE (1): System μProcessor Address EB, Write.
Service Req: OTD

	BIT								
HEX	7	6	5	4	3	2	1	0	BYTE FUNCTION
00	0	0	0	0	0	0	0	0	Read F.D. Diagnostic Registers
0D	0	0	0	0	1	1	0	1	Write Unformatted
0E	0	0	0	0	1	1	1	0	Write Formatted
88	1	0	0	0	1	0	0	0	Normal Read
8E	1	0	0	0	1	1	1	0	Copy Write (Formatted/Unformatted)

DRIVE SELECT BYTE (1): System μProcessor Address EB, Write.
Service Req: OTD

00	0	0	0	0	0	0	0	0	Select Drive 0
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
07	0	0	0	0	0	1	1	1	Select Drive 7

SECTOR SELECT BYTE (1): System μProcessor Address EB, Write.
Service Req: OTD

00	0	0	0	0	0	0	0	0	Select Sector 0
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
1F	0	0	0	1	1	1	1	1	Select Sector 31

TRACK SELECT BYTE (1): System μProcessor Address EB, Write.
Service Req: OTD

00	0	0	0	0	0	0	0	0	Select Track 00
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
4C	0	1	0	0	1	1	0	0	Select Track 76

DATA BYTES (128): System μProcessor Address EB, Write.
Service Req: OTD

(NO RESTRICTIONS)

DISC STATUS BYTE (1): System μProcessor Address EB, Read.
Service Req: RST or SIO

–	0	0	–	–	–	–	–	0	Not Used
–	–	–	1	–	–	–	–	–	Illegal Operation
–	–	–	–	1	–	–	–	–	Error Recovery
–	–	–	–	–	1	–	–	–	Write Protect
–	–	–	–	–	–	1	–	–	Drive Fault
–	–	–	–	–	–	–	1	–	F.D. Failure

DATA BYTES (128): System μProcessor Address EB, Read.
Service Req: IND

(NO RESTRICTIONS)

2587-10

Fig. 1-9a. Data Port Formats.

DIAGNOSTIC REGISTER BYTES: System μProcessor Address EB, Read.
Service Req. IND

Reg. No.	BIT 7	6	5	4	3	2	1	0	BYTE FUNCTION
R1	V	V	V	V	V	V	V	V	Working (Temporary) Data; Function dependent
R2	V	V	V	V	V	V	V	V	Working (Temporary) Data; function dependent
R3	GT ID2	GT ID1	GT CRC	ERROR RECOV. FLAG	END of FILE	ERROR RECOV. STATE	SEEK STATE 1	SEEK STATE 0	Program state flags
R4	0	0	0	0	0	V	V	V	Device Address (selected Disc Drive)
R5	V	V	V	V	V	V	V	V	Head Delay Count
R6	V	0	0	0	V	V	V	V	Command Byte; from System Processor
R7	0	0	0	V	V	V	V	V	Sector N (Current)
R8	$\overline{\text{TRK 00}}$	$\overline{\text{INDEX}}$	$\overline{\text{C0}}$	$\overline{\text{SECTOR}}$	$\overline{\text{C1}}$	$\overline{\text{S}}$	0	$\overline{\text{RDY}}$	Input CSW
R9	0	0	0	V	V	V	V	V	Sector X (Target); from System Processor
R10	0	V	V	V	V	V	V	V	Track N (Current)
R11	0	V	V	V	V	V	V	V	Track X (Target); from System Processor
R12	V	V	V	V	V	V	V	V	Working (Temporary) Data; function dependent
R13	V	V	V	V	V	V	V	V	Host Byte Count (from −4 to 128)
R14	V	V	V	V	V	V	V	V	CRC Byte 1
R15	V	V	V	V	V	V	V	V	CRC Byte 2
R0	0	0	CRC FAIL	ID ERROR	SYNC ERROR	0	0	0	Sense (Error)

2587-11

Fig. 1-9b. Data Port Formats .

Table 1-2

I/O SEQUENCES

Seq. No.	SYSTEM PROCESSOR CONTROL PORTS		SYSTEM PROCESSOR DATA PORTS	
	Output Byte	Input Byte	Output Byte	Input Byte
STANDARD I/O COMMANDS				
1	RST	Flag	—	Disc Status
2	SIO	Flag	—	Disc Status
3	OTD	Flag	Command	—
4	OTD	Flag	Drive Select	—
5	OTD	Flag	Sector Select	—
6	ITD	Flag	Track Select	—
Copy Write Command				
7	RST	Flag	—	Disc Status
Normal Read Command				
7	IND	Flag	—	Data 0
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
134	IND	Flag	—	Data 127
135	RST	Flag	—	Disc Status
Write Formatted or Unformatted Commands				
7	OTD	Flag	Data 0	—
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
134	OTD	Flag	Data 127	—
READ DIAGNOSTIC REGISTERS COMMAND				
1	RST	Flag	—	Disc Status
2	SIO	Flag	—	Disc Status
3	OTD	Flag	Command	—
4	IND	Flag	—	R1
5	IND	Flag	—	R2
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
18	IND	Flag	—	R15
19	IND	Flag	—	RØ (Sense)

(1) Copy Write: no sector data is sent to or received from the Controller; this mode takes data already stored in the sector buffer and writes it in the new disc location defined by the address bytes. On the RST request, the disc status byte reports the validity of disc I/O operation.

(2) Normal Read: 128 data bytes are read from the flexible disc, checked for CRC validity, and sequentially applied to the input data port of the System Processor. On the RST request, the disc status byte reports on the disc I/O operation, including the results of the CRC check.

(3) Write Formatted or Unformatted: 128 bytes of sector data are sent to the Controller, which serializes the data, generates the CRC word, and writes encoded data in the addressed disc location. The two writing modes differ only in that, for formatted writing, the sector header of the disc location must be read and verified before the new data is written into the location. The RST request calls the disc status byte.

(4) Read Diagnostic Registers: a diagnostic read is requested by the System Processor after a fault has been reported by the disc status byte. The sense byte contained in the R0 register identifies the type of error that set the F.D. FAILURE bit in the disc status word. If the RST request is not issued by the System Processor after register RØ is read, the Controller loops back and reads out the registers again.

Disc Drive Selection and Control

Once the Controller has received a command byte and the three address bytes, it enables the I/O gates of the specified Disc Drive (SEL DR n) and causes the read/write head to engage the flexible disc (HD LD n). The other Disc Drive(s) are kept in the standby state, in which the I/O gates are inhibited and the heads unloaded.

The status of the Disc Drives is reported by the Controller in the disc status byte appearing at the input data port of the System Processor during SIO and RST requests. Each active bit of the disc status byte is described in Table 1-3; that table also describes the contents of the sense byte sent to the System Processor during diagnostic reading of the Controller working registers. The DRIVE FAULT bit of the disc status byte indicates the status of all drives, since the READY outputs are wire-ORed to form a composite signal. The remainder of the byte applies only to the selected drive.

The F.D. FAILURE bit is activated by the Controller when an error is detected in the sector ID heading (prior to formatted writing) or the 128 bytes of sector data (after normal reading) read from the Disc Drive. At the same time, the Controller enters active bits defining the error in the sense byte (stored in working register RØ), and activates the ERROR RECOVERY bit in the disc status byte. The Controller error recovery routine forces the Disc Drive to wipe the surface of the disc and to re-read the addressed sector. If the error recovery routine does not correct the fault, the Controller deactivates the ERROR RECOVERY bit and waits for the System Processor to command a diagnostic reading of the working registers, including the sense byte. If the error is corrected by the error recovery routine, the Controller resets the corresponding bits in the disc status byte and in the sense byte; it then repeats the original operation.

When the Controller selects a Disc Drive, the position of the read/write head is determined initially in one of two ways. The Controller may issue a positive DIRECTION (out) command and a series of STEP (track) pulses until the Disc Drive returns an active TRK 00 signal, which serves as the reference for track counting. Alternatively, the Controller may command a read ID operation, which supplies reference track and sector numbers if data is recorded on that disc track. Once initialized, the Controller keeps an algebraic count of the number of STEP pulses issued to the Disc Drive, with the polarity determined by that of the DIRECTION command. Direction polarity is obtained by comparing present and target addresses.

Table 1-3

DISC STATUS BYTE AND SENSE BYTE DEFINITIONS

Bit No.	Label	Description
	DISC STATUS BYTE (Control Byte SIO or RST)	
1	F.D. FAILURE (also called UNIT CHECK)	Failure in reading from disc; the nature of the fault is defined by the sense byte. Requests a diagnostic read operation if not cleared at end of ERROR RECOVERY bit period.
2	DRIVE FAULT	One or more Disc Drives is not up to speed, has no disc installed, or has unstable dc power.
3	WRITE PROTECT	Writing to selected Disc Drive is inhibited by write-protected disc.
4	ERROR RECOVERY	Controller is performing error recovery routine in attempt to clear F.D. FAILURE bit.
5	ILLEGAL OPERATION	Controller is seeking the address of an illegal track (>76) or sector (>31).
	SENSE BYTE (Command Byte 00)	
3	SYNC ERROR	Controller has detected an error in the sync byte read from the addressed sector ID header.
4	ID ERROR	An incorrect track or sector number has been read in the addressed disc location.
5	CRC FAIL	Sector data read from an addressed disc location has failed the CRC check.

The Controller uses the bipolar WRT GATE command to enable either the write or read circuit in the Disc Drive. An active (low) state selects the writing mode. When the Controller is idle, the reading mode is selected. Actual writing or reading of data is controlled by the data formatting logic, described later in this section.

The Controller keeps a running count of SECTOR pulses received from the Disc Drive; the count is initialized each time an INDEX pulse is received. The sector count identifies the number of the disc sector in which the read/write head is momentarily positioned. This information is used by the data formatting logic, described below, to control writing or reading data in an interleaved sequence.

Data Formatting

Data transfer between the System Processor and the selected Disc Drive occurs in two steps for both writing and reading operations. First, 128 data bytes (a sector block) are entered in the Controller sector buffer. Second, the Controller microcontroller takes the data from the sector buffer and converts it to serial (write) or parallel (read) format. At different times in the transfer, command and status bytes are also exchanged; these bytes are stored in the Controller working registers.

After the read/write head has been positioned during writing, the Controller performs the following data formatting operations:

(1) Accepts and stores in working registers the command and select bytes from the System Processor.

(2) Accepts and stores in the sector buffer 128 data bytes from the System Processor.

(3) Generates the CRC word and stores it in the working registers; the CRC calculation includes the sector header data.

(4) If formatted writing was commanded by the System Processor, locates the correct sector and reads the ID header (read ID operation) to verify the address before writing new data. No read ID operation is used during unformatted writing because the disc is unrecorded at the addressed location.

(5) Locates the correct sector, then generates and sends the preamble of 1200's that follow the leading edge of the SECTOR pulse.

(6) Generates and sends the sync byte in serial order to the Disc Drive.

(7) Reads the sector and track bytes from the working registers and sends these bytes in order to the Disc Drive.

(8) Successively reads each of the 128 data bytes from the sector buffer, encodes the data into DFFM NRZ format, and sends the data in serial order to the Disc Drive.

(9) Reads two CRC bytes from the working registers and sends this in serial order to the Disc Drive.

(10) Generates the postamble of Ø's until the next sector pulse occurs.

After the read/write head has been positioned during normal reading, the Controller performs the following sequence of data formatting operations:

(1) Accepts and stores in working registers the command and select bytes from the System Processor.

(2) After locating the correct sector, the Controller accepts, temporarily stores, and verifies the sync byte, received in serial order from the Disc Drive.

(3) Accepts, temporarily stores, and verifies the sector and track bytes from the Disc Drive.

(4) Accepts and stores in the sector buffer 128 data bytes from the Disc Drive.

(5) Accepts and stores the CRC word in the working registers. While reading the sector ID header and entering the serialized data in the sector buffer, the Controller also checks the accuracy of the data against the CRC word, which should equal Ø at the end of the check.

(6) Successively reads each of the 128 data bytes from the sector buffer, converting the data to parallel format, and sends each byte to the System Processor.

INSTALLATION

The Flexible Disc Unit should be installed according to the instructions contained in the applicable system installation manual. Unless otherwise specified:

(1) Connect the unit as shown in Fig. 1-10 and Table 1-4.

(2) Check that TB1 is strapped according to the input ac line voltage. If 115 volts, one strap should be installed between terminals 6-7 and another 8-9; if 230 volts, one strap should be installed between terminals 7-8.

(3) Check that interleave switch S4104 on the Flexible Disc Controller is set as follows:

5	4	3	2	1
Off	Off	On	On	On

(4) Check that the rating of fuses F1 and F3 correspond to those placarded for the selected line voltage.

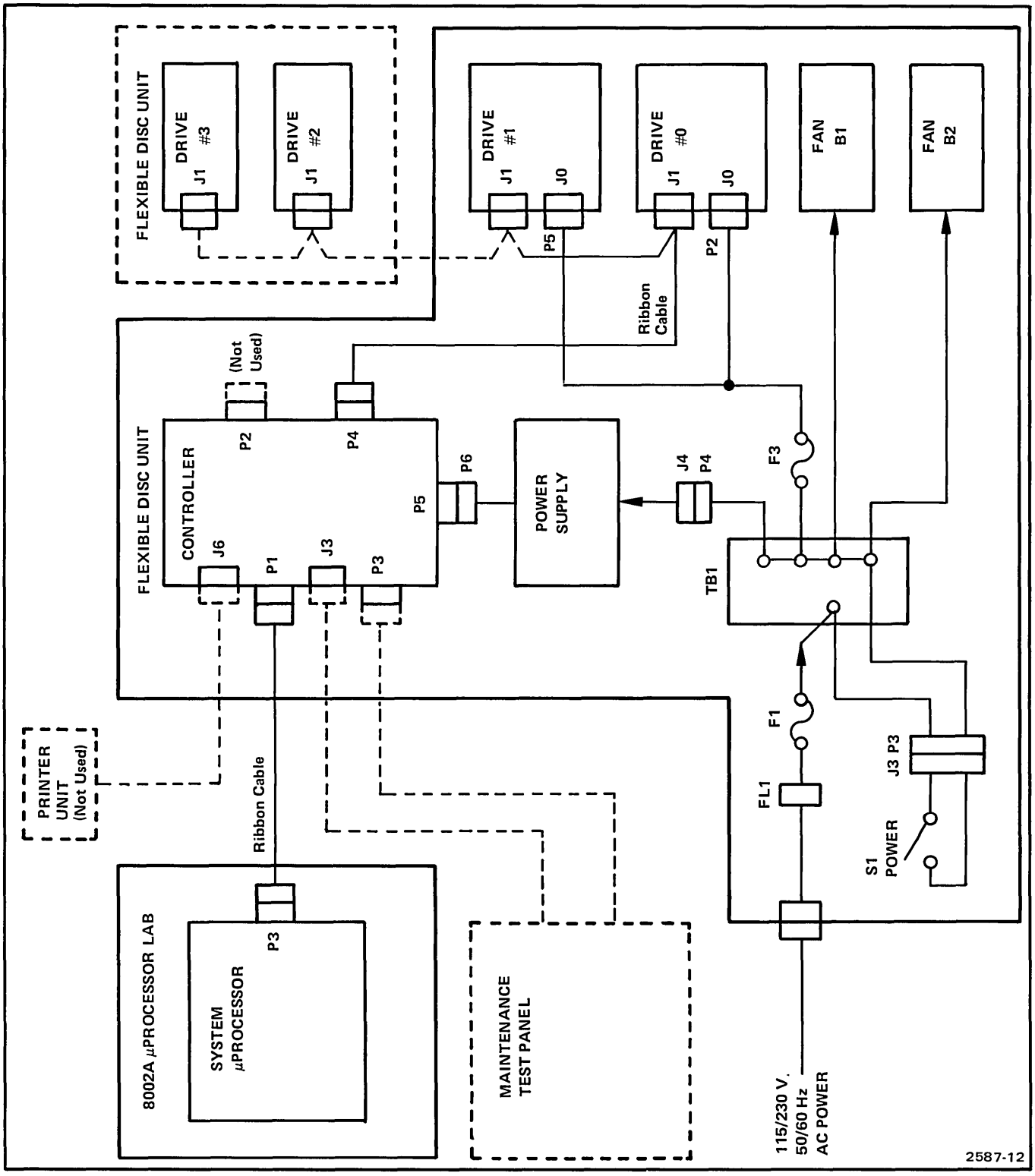


Fig. 1-10. Flexible Disc Unit Connection Diagram.

Table 1-4

CONTROLLER PIN OUT DATA

To System μProcessor P3			To Disc Drive J1		
P1-Pin	I/O	Signal Label	P4-Pin	I/O	Signal Label
1	In	BUS OUT 0	1	Out	+5 V
2	In	BUS OUT 1	3	Out	+5 V
3	In	BUS OUT 2	5	Out	DIRECTION (IN)
4	In	BUS OUT 3	7	Out	STEP
5	In	BUS OUT 4	9	Out	+24 V
6	In	BUS OUT 5	11	Out	+24 V
7	In	BUS OUT 6	13	Out	SELECT 7
8	In	BUS OUT 7	14	Out	HEAD LOAD 7
12	In	C1	15	Out	SELECT 0
13	In	C0	17	In	TRACK 00
14	In	FD BUS IN EN	19	Out	HEAD LOAD 0
16	In	S (STRB)	21	In	READY
17	—	Ground	23	Out	TRK >43
18	—	Ground	25	In	INDEX
19	—	Ground	27	In	SECTOR
29	Out	BUS IN 7	29	In	WRITE PROTECT
30	Out	BUS IN 6	31	Out	WRITE DATA
31	Out	BUS IN 5	33	Out	WRITE GATE
32	Out	BUS IN 4	35	In	SEPARATED DATA
33	Out	BUS IN 3	37	In	SEPARATED CLOCK
34	Out	BUS IN 2	39	Out	SELECT 6
35	Out	BUS IN 1	40	Out	HEAD LOAD 6
36	Out	BUS IN 0	41	Out	SELECT 5
38	Out	HOST FLG	42	Out	HEAD LOAD 5
39	Out	BUSY (Printer)	43	Out	SELECT 4
40	Out	FAULT (Printer)	44	Out	HEAD LOAD 4
			45	Out	SELECT 3
Note: No connection to unspecified pins through pin 50.			46	Out	HEAD LOAD 3
			47	Out	SELECT 2
			48	Out	HEAD LOAD 2
			49	Out	SELECT 1
			50	Out	HEAD LOAD 1
			Note: Even pins 2 and 12 and 16 to 38 are grounded.		

Section 2

SPECIFICATIONS

FLEXIBLE DISC UNIT

a. Electrical Characteristics

Input Current/Voltage	3.5 A max, at 115 Vac ±10%. 2.0 A max, at 230 Vac ±10%. (Unit is normally wired for 115 Vac operation. Change jumpers on TB1 to change from 115 to 230 Vac operation.)
Frequency	60 Hz ±10% 50 Hz ±10% (available by special order)
Fuses	
Primary (F1)	4 A at 115 Vac, 2 A at 230 Vac
F2	Spare
Disc Drives (F3)	2.5 A at 115 Vac, 1.5 A at 230 Vac
F4	Spare
Grounds	Chassis ground is connected internally to earth ground.

b. Environmental Characteristics

Temperature	
Operating	+10°C to +35°C
Storage	−40°C to +75°C
Humidity	20% to 80% relative, non-condensing
Altitude	
Operating	To 15,000 feet (4.57 km)
Storage	To 50,000 feet (15.24 km)

c. Physical Characteristics

Dimensions (Overall)	
Height	27 cm (10.5 inches)
Width	44 cm (17.5 inches)
Length	60 cm (23.6 inches)
Weight	38.6 kg (85 lbs.)

FLEXIBLE DISC UNIT POWER SUPPLIES

a. Electrical Characteristics

Output Power

+5 Vdc	6 A
+24 Vdc	4.8 A
AC Input	115/230 Vac ±10%, 47-440 Hz Derate output current 10% for 50 Hz operation

Regulation

Line	±0.05% for a 10% line change
Load	±0.05% for a 50% load change

Output Ripple

5 V	1.5 mV peak-peak, 0.4 mV RMS maximum
24 V	0.02% peak-peak, 0.01% RMS maximum
Stability	±0.3% for 24 hours after warm-up

b. Environmental Characteristics

Temperature

Rating	0°C to 50°C full rated, derated linearly to 40% at 70°C
Coefficient	±0.3%/°C maximum
Vibration	Per MIL-STD-810B, Method 514, Procedure I, Curve AB (to 50 Hz)
Shock	Per MIL-STD-810B, Method 516, Procedure V

Section 3

THEORY OF OPERATION

INTRODUCTION

This section presents a detailed description of the operation of the Flexible Disc Controller (subsequently referred to as the Controller). You should be familiar with the overview of the Flexible Disc Unit presented in Section 1 before proceeding to the material in this section.

CONTROLLER FUNCTIONAL DESCRIPTION

Refer to the detailed functional block diagram of the Controller (Fig. 3-1, in the Diagrams section) during these descriptions. The input control code (S, C1, C0) from the system Processor is gated to the WR bus when the Controller's microprogram periodically causes the Instruction Decoder to produce the INPUT CSW command. The ALU then transfers the input control code, together with the Disc Drive status bits appearing on the WR bus, through the TB bus to register R8 of the Working Register file. The Controller's microprogram monitors the state of the input control code for one of four service requests (SIO, OTD, IND, RST). A service request is initiated when the strobe bit (S) changes state, which causes a handshake I/O sequence in response to the HOST FLG signal from the Instruction Decoder. See Fig. 3-2 for a timing diagram of the I/O handshake.

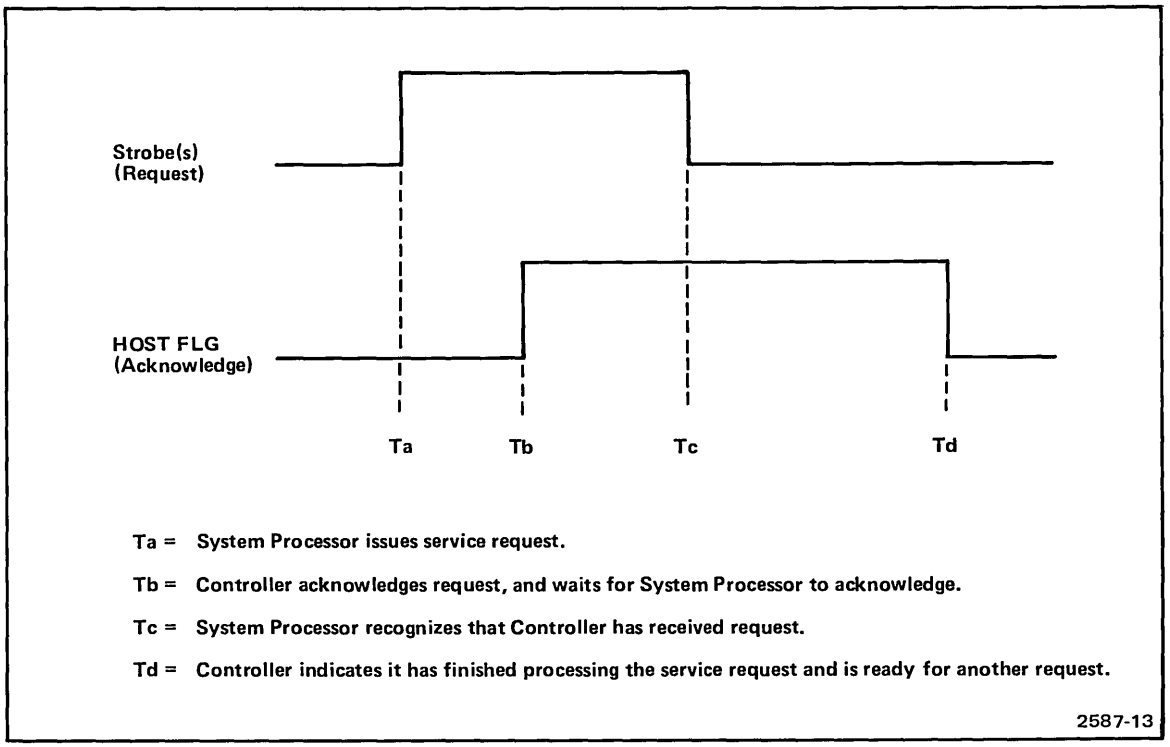


Fig. 3-2. I/O Service Request Timing.

Depending on the type of service request, data appears at either the input (BUS OUT) or output (BUS IN) port. In the case of the disc status byte, the I/O gates place the byte at the output port whenever input control code bit CO is inactive; this state signifies either an SIO or RST service request. When CO is active, the Accumulator output byte is placed at the output port. Data from the input port is enabled by the INPUT HOST OUTPUT BYTE signal from the Instruction Decoder when the microprogram has decoded an OTD service request and is ready to receive the data. Figure 3-3 shows the three standard I/O operation sequences.

20-MHz CLOCK

The timing of Controller operations is established by the crystal-controlled 20-MHz Clock circuit. Refer to Fig. 3-4. The 20-MHz oscillator frequency is divided by four and phased to produce two basic clock signals, TØ and T1, which provide the time frame for a 200 ns machine cycle. A cycle begins when TØ latches an instruction word into the ROM Instruction Register. Next in the cycle, T1 clocks the Instruction Decoder command latches, which respond to the contents of the instruction word. At the end of the cycle, the RAR CLK pulse (TØ+T1) transition advances the count in the ROM address Register, forcing the ROM to the next instruction address before TØ occurs again.

Instruction Execution Time

A maximum of 198 ns is required to execute an instruction. This worst-case data path is as follows:

(1)	RIR bus delay	35 ns
(2)	Register access	60 ns
(3)	ALU propagation delay	33 ns
(4)	T-Register propagation delay	30 ns
(5)	Register storage	40 ns
		198 ns

Carry Propagation Delay

A maximum of 164 ns is required to execute an instruction that includes a carry operation. The worst-case data path is:

(1)	RIR bus delay	35 ns
(2)	Register access	60 ns
(3)	Carry propagation delay	69 ns
		164 ns

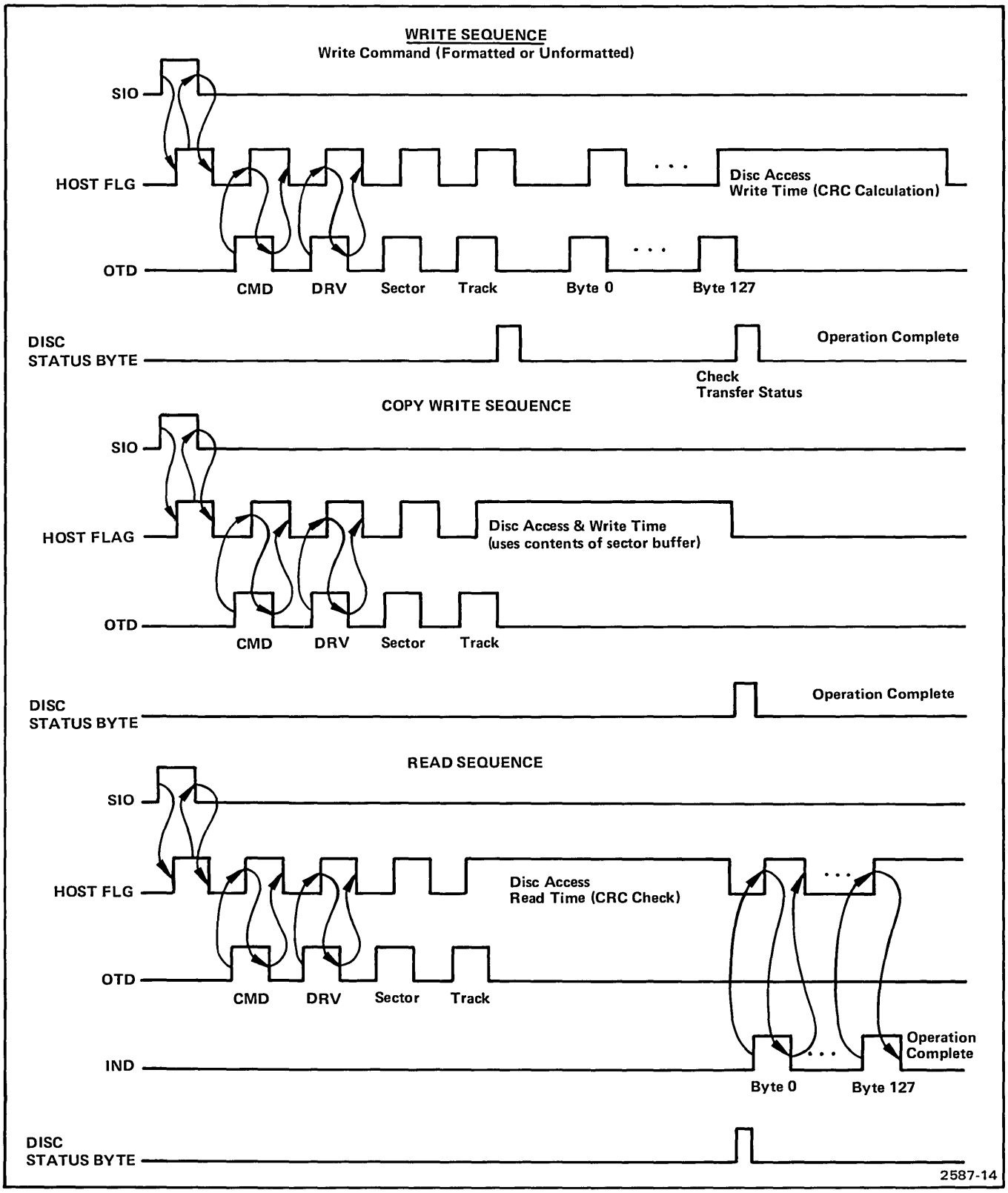


Fig. 3-3. Standard I/O Operation Sequences.

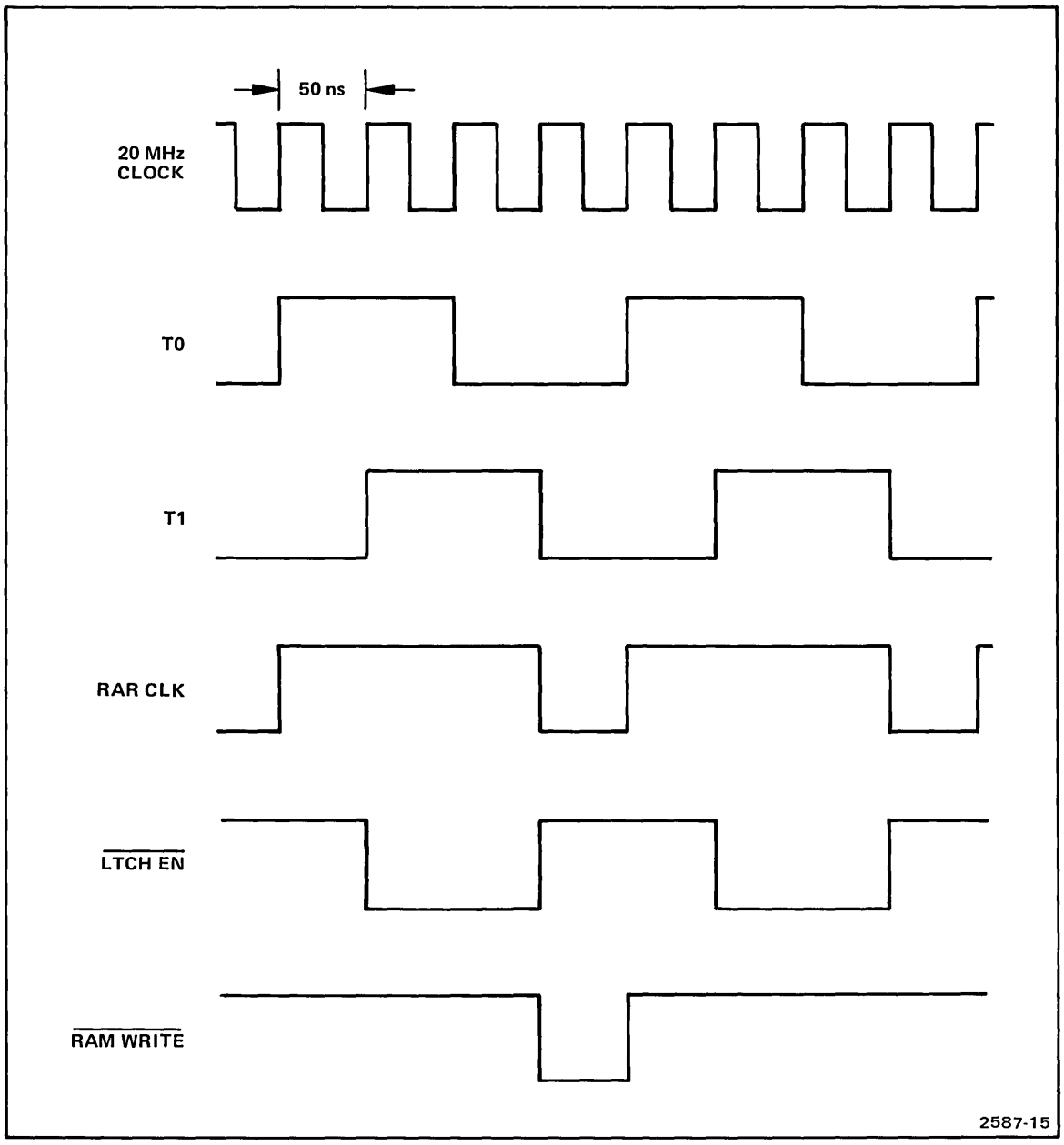


Fig. 3-4. Controller Clock Timing Diagram.

ROM ADDRESS REGISTER (RAR)

The ROM Address Register (RAR) is an 8-bit programmable counter. The RAR output byte is the ROM address for the instruction word of the next machine cycle. The RAR is reset when power is first applied. Until a jump condition occurs, the RAR count is advanced by the RAR CLK pulse. When a jump condition is detected by the Jump Control circuit, the RAR count is changed to the target address by loading the data byte present on the WR bus. After loading, the RAR resumes operation as a counter until the next forced jump.

READ-ONLY MEMORY (ROM)

Two parallel 512x8 bit ROMs contain the microprogram that controls each machine cycle of the Controller. The memory is divided into low and high banks of 512 16-bit instructions. The bank addressed by the RAR bus is determined by the state of UBANK, which selects the lower bank when inactive. The ROM output word is stored for one instruction cycle in the ROM Instruction Register. The ROM contents, expressed in hexadecimal notation, are shown in Fig. 3-5. Refer to Appendix C for a listing of the microprogram.

```
0000=0C AC 5F 5F 5F 5F 5C 5A 5A B5 AC 59 5F 5F 5F AC
0010=59 AC 59 5F 50 4C 02 50 07 05 AC 59 63 59 EC 59
0020=B8 4F B7 B0 CC BB BE 07 6D 59 B3 5F 4F B6 B1 53
0030=B0 0A 08 BE B5 AD 5A 4F B7 5C B0 AC 59 6C B1 EC
0040=6A AD 59 6C B2 8D B0 8D B0 4F B7 B0 4F B2 B4 6C
0050=4A B0 4C B9 0B BE 0B BE 6C B9 CF B4 B2 0C 5F AC
0060=59 BE B3 4F B4 BE EC 05 5C B1 4F B7 B1 4C B1 BA
0070=59 4F B4 B0 BE 4A B1 59 BE 4F B1 B6 AC 59 BE 59
0080=8D B1 06 BE 59 AC 59 0A 0B 5F 00 53 B0 BE 59 AC
0090=5D AC 45 B6 5C AC 6D B1 59 BE AC 59 0A 5C EF 5F
00A0=53 B0 6C 05 CC B8 BE 05 CC 10 6C CC B8 BE 6C BE
00B0=6C BE 6C BE 6C BE 6C BE 6C BE 6C BE 6C BE 6C BE
00C0=6C BE 6C BE 6C BE 6C BE 6C BE 6C BE 6C BE AC 59
00D0=53 53 7E 53 BA 6C B1 4C B0 6C BA 5C AC 58 BE CF
00E0=B7 5F 6C 65 B1 B6 0A 5C BE 53 08 5C 6C 65 B1 5C
00F0=AC 59 0A 53 B0 08 4F B9 AC BE 0B BE 07 BE 05 BE
0100=6C B4 B8 A8 59 BE AC 59 6C 59 5F 50 06 BE 04 5F
0110=5F AC 59 5C AC 5D B0 5C AC 65 B0 AC 58 BE 6C B8
0120=4F B6 6C B9 AC 58 BE B4 8C 10 A8 BE 4C 10 AD 59
0130=5C BE 04 04 AC 4D B1 B3 AC BE AC 5D BE 6F B4 0B
0140=05 B2 4F B6 B0 09 BE 5F 5F AC 08 BD CF 5F 4A B1
0150=5C B0 AC BE 5F 50 BD CF 5F 5F B0 50 6C B2 6C 4A
0160=B1 AC 58 BD CF 5F 5F B0 AC 4D B0 6C 4A B1 AC 58
0170=0A AC 59 6C 59 6C 59 5F 5F BE 7A 08 AC 59 4F B2
0180=BD CF 5F 5F B7 AC 5A AC 5A 5C B0 5C B8 BE 4C B8
0190=CF BE 4F BE 6C B4 6C 48 B1 AC 58 06 6C B2 BE AC
01A0=5D 09 BE 0A 6C 59 AC 59 6C BE AC 0A 59 5F AC 59
01B0=AC 59 AC BE 59 00 07 50 5F BE AC 50 53 B0 59 AC
01C0=59 5F BE BE BE BE 00 5F 71 BE BE BE BE AC 59 6C
01D0=59 50 BE AC 59 6C 59 50 BE 00 BE 5C 4F B6 50 AC
01E0=59 CF CF 6C 59 BE BE BE 00 5F B1 BE 00 BE 50 BE
01F0=6C 59 AC 59 50 BE AC 59 CC B4 00 BE AC 5D 05 BE

R0 Bits 15-8

2587-16
```

Fig. 3-5a. ROM Contents—MSB.

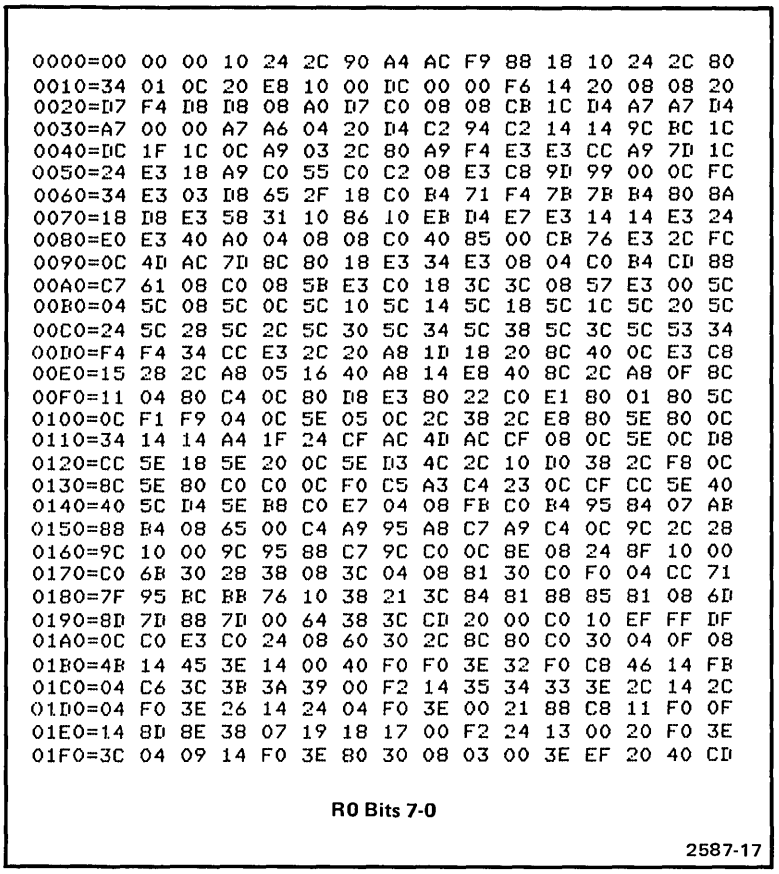


Fig. 3-5b. ROM Contents—LSB.

ROM INSTRUCTION REGISTER (RIR)

An instruction cycle is started when the 16-bit instruction word from the ROM is latched in the ROM Instruction Register (RIR) by clock TØ. The ROM Instruction Register produces an active JMP FRZ signal when the current instruction word represents a forced jump.

RIR BUS

Operation of the controller is established by the 16-bit instruction word contained in the ROM Instruction Register. As shown in Fig. 3-6, the format of the instruction word differs according to the type of instruction. (Refer to the Microprogram Descriptions in this section, for definitions of coding used in each format.) The instruction word is distributed as follows:

Bits	To	Function	Format
0-15	Instruction Decoder	Generate Commands	All
0-7	WR Bus Gates (U2050)	Jump Address	Type L Direct Transfer Group
2-5,15	Working Register	Select, Enable RØ-R15	Types A, U, and L Through-Register Transfer Group
6-9	Carry Generator	Enable, Force Carry	Type A
7-11	ALU	Select Logic or Arithmetic function	Types A, L Immediate Group
8-11	Jump Control Circuit	Select Jump Condition	Type L Direct and Through-Register Transfer Groups
9	Device Address Latch	Load Drive Address	Type S

The functions of the Source, Destination, and Special fields of the RIR word are described in Table 3-1.

INSTRUCTION DECODER

The Instruction Decoder circuit translates the instruction word appearing on the RIR bus into the signals that enable the Controller circuits to execute the instruction. Two dual two-line decoders (U3100, U5100) produce the signals for the Source, Destination, and Special fields of the RIR word and for controlling selection of the command latches. For Type A Input Group instructions, addressable 8-bit latch U4040 is selected by the INPUTS signal. For Type S instructions, the addressable 8-bit latch for either Command Group 1 (U6090) or Group 2 (U6080) may be enabled by the LTCHS signal. (Refer to the Microprogram Description in this section for definitions of the coding that selects individual commands.)

Type A Register Group
(Also Type U)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Source		Dest.		ALU function						Reg. Addr.				Spec.	

Causes ALU to perform selected function on data from Addressed Working Register. Results are stored in Destination, if applicable. Commands Special parallel operation, if required.

Type A Input Group
(Also Type U)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Source		Dest.		ALU function						Input Addr.				Spec.	

Causes ALU to perform selected function on data from Addressed Input. Results are stored in Destination, if applicable. Commands Special parallel operation, if required.

Type S

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Not Used				Command						Not Used					

Sets or resets Command in Instruction Decoder latch. Hex 0000 forces halt.

Type L Immediate Group

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Source		Dest.		ALU logic				Data Byte							

Causes ALU to perform Logic operation, with Data Byte used as operand. If applicable, causes result to be stored in Destination.

Type L Direct Transfer Group

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Source		Dest.		Condition				Target Address							

Forces jump on Condition to Target Address.

Type L Through-Register Transfer Group

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Source		Dest.		Condition				Not Used		Reg. Addr.				Not Used	

Forces jump on Condition to target address contained in Addressed Working Register.

2587-18

Fig. 3-6. RIR Bus (Instruction Word) Formats.

Table 3-1

RIR Bus Source, Destination, and Special Field Definitions

RIR Bits		Function	Op Code Label	Control Signal
15	14	**SOURCE FIELD**		
0	0	Enables Instruction Decoder Latches (Registers source of WR bus)	None	LTCHS
0	1	Registers source of WR bus	SR	None
1	0	RIR bus source of WR bus	I	RIRS
1	1	Selected Input source of WR bus	IN	INPUTS
13	12	**DESTINATION FIELD**		
0	0	Don't store TB bus data	L	None
0	1	Store TB data in Register	DR	RAMD
1	0	Store TB data in Accumulator	A	ACCD
1	1	Enter WR bus data in ROM Address Register (RAR)	M	RARD
2	1	**SPECIAL FIELD**		
0	0	No special operation	None	None
0	1	Start pushing C7 Carry into Sector Buffer	SPSH	START PUSH
1	0	Load Write Data flip-flop by C7 Carry	PULL	LOAD WRITE DATA
1	1	Finish pushing C7 Carry into Sector Buffer	EPSH	FINISH PUSH

WORKING REGISTERS

The Working Registers file comprises 16 8-bit registers (U4050, U4060), designated R0 through R15. RIR bus bits 2-5 select one of the registers, and bit 15 connects the register to the WR bus. TB data is written in the addressed register when the RAM WRITE signal is active. Fig. 3-7 defines the contents of the Working Registers.

COMMAND BYTE (1): System μProcessor Address EB, Write.

Service Req: OTD

	BIT								
HEX	7	6	5	4	3	2	1	0	BYTE FUNCTION
00	0	0	0	0	0	0	0	0	Read F.D. Diagnostic Registers
0D	0	0	0	0	1	1	0	1	Write Unformatted
0E	0	0	0	0	1	1	1	0	Write Formatted
88	1	0	0	0	1	0	0	0	Normal Read
8E	1	0	0	0	1	1	1	0	Copy Write (Formatted/Unformatted)

DRIVE SELECT BYTE (1): System μProcessor Address EB, Write.

Service Req: OTD

00	0	0	0	0	0	0	0	0	Select Drive 0
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
07	0	0	0	0	0	1	1	1	Select Drive 7

SECTOR SELECT BYTE (1): System μProcessor Address EB, Write.

Service Req: OTD

00	0	0	0	0	0	0	0	0	Select Sector 0
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
1F	0	0	0	1	1	1	1	1	Select Sector 31

TRACK SELECT BYTE (1): System μProcessor Address EB, Write.

Service Req: OTD

00	0	0	0	0	0	0	0	0	Select Track 00
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
4C	0	1	0	0	1	1	0	0	Select Track 76

DATA BYTES (128): System μProcessor Address EB, Write.

Service Req: OTD

(NO RESTRICTIONS)

DISC STATUS BYTE (1): System μProcessor Address EB, Read.

Service Req: RST or SIO

–	0	0	–	–	–	–	–	0	Not Used
–	–	–	1	–	–	–	–	–	Illegal Operation
–	–	–	–	1	–	–	–	–	Error Recovery
–	–	–	–	–	1	–	–	–	Write Protect
–	–	–	–	–	–	1	–	–	Drive Fault
–	–	–	–	–	–	–	1	–	F.D. Failure

DATA BYTES (128): System μProcessor Address EB, Read.

Service Req: IND

(NO RESTRICTIONS)

2587-10

Fig. 3-7a. Data Port Formats.

DIAGNOSTIC REGISTER BYTES: System μProcessor Address EB, Read.
Service Req. IND

Reg. No.	BIT 7	6	5	4	3	2	1	0	BYTE FUNCTION
R1	V	V	V	V	V	V	V	V	Working (Temporary) Data; Function dependent
R2	V	V	V	V	V	V	V	V	Working (Temporary) Data; function dependent
R3	GT ID2	GT ID1	GT CRC	ERROR RECOV. FLAG	END of FILE	ERROR RECOV. STATE	SEEK STATE 1	SEEK STATE 0	Program state flags
R4	0	0	0	0	0	V	V	V	Device Address (selected Disc Drive)
R5	V	V	V	V	V	V	V	V	Head Delay Count
R6	V	0	0	0	V	V	V	V	Command Byte; from System Processor
R7	0	0	0	V	V	V	V	V	Sector N (Current)
R8	$\overline{\text{TRK 00}}$	$\overline{\text{INDEX}}$	$\overline{\text{C0}}$	$\overline{\text{SECTOR}}$	$\overline{\text{C1}}$	$\overline{\text{S}}$	0	$\overline{\text{RDY}}$	Input CSW
R9	0	0	0	V	V	V	V	V	Sector X (Target); from System Processor
R10	0	V	V	V	V	V	V	V	Track N (Current)
R11	0	V	V	V	V	V	V	V	Track X (Target); from System Processor
R12	V	V	V	V	V	V	V	V	Working (Temporary) Data; function dependent
R13	V	V	V	V	V	V	V	V	Host Byte Count (from −4 to 128)
R14	V	V	V	V	V	V	V	V	CRC Byte 1
R15	V	V	V	V	V	V	V	V	CRC Byte 2
R0	0	0	CRC FAIL	ID ERROR	SYNC ERROR	0	0	0	Sense (Error)

2587-11

Fig. 3-7b. Data Port Formats.

Resistor RØ—Sense Byte

One or more of the bits in the Sense Byte are activated when the F.D. FAILURE signal (included in the disc status byte) occurs. The bits describe the type of execution error.

Register R1—Temporary Byte

Register R1 serves as a working register, in which a data byte is temporarily stored during various instruction cycles.

Register R2—Temporary Byte

Register R2 serves as a working register.

Register R3—Program State Flag Byte

The byte stored in Register R3 contains state information used to control various routines in the microprogram. The functions of the bits are as follows:

Bit	Label	Function
1,Ø	Seek State flags	Idle, 00 Enable Seek, 01 Step Ahead, 10
4,2	Error Recovery	Idle, 00 Read ID Error, 01 Reset Program Flags, 10 Wipe Disc, 11
3	Physical End of File	Track 77
5	GTCRC	Generating CRC word
6	GTID1	Head unknown, read sector ID
7	GTID2	Verify track number after seek

Register R4—Drive Number

Register R4 contains the number (device address) of the Disc Drive currently being accessed. The coding of this byte is defined in Fig. 3-7.

Register R5—Head Delay

Register R5 contains information regarding head up and down delays. The meaning of the contents is as follows:

(1) Positive Value—signifies that the read/write head in the selected Disc Drive is down and has settled. (The down delay has transpired.) The delay is initially set to +20 and is decremented with each revolution of the flexible disc (INDEX pulse).

(2) Zero Value—signifies that the read/write head is raised.

(3) Negative Value—signifies that the read/write head has just been lowered and that the down delay is in effect. The delay is initially set to −10 and is incremented by each SECTOR pulse, giving a 50 ms delay.

@

Register R6—Command Byte

Register R6 stores the command byte received from the System Processor. The coding of this byte is defined in Fig. 3-7.

Register R7—Sector N

The value (0 to 31) stored in Register R7 identifies the sector number where the read/write head is currently located. During power application or switching between Disc Drives, the sector is unknown and the byte value is set to −1.

Register R8—Input CSW Byte

The byte stored in Register R8 represents the most recent sampling of the input control byte from the System Processor and of the status signals from the Disc Drive. This byte is used to determine the leading edge function (Op Code label LEF).

Register R9—Sector X

Register R9 contains the target sector number, obtained from the System Processor.

Register R10—Track N

The value (0 to 76) stored in Register R10 identifies the track number with which the read/write head is currently aligned. During power application or switching between Disc Drives, the track number is unknown and the byte value is set to −1.

Register R11—Track X

Register R11 contains the target track number, obtained from the System Processor. During the error recovery routine, Register R11 serves as a working register after the target track number has been transferred to Registered R14.

Register R12—Temporary Byte

Register R12 serves as a working register.

Register R13—Host Byte Count

The byte stored in Register R13 identifies the current byte in a data exchange between the System Processor and the Controller. The counts and their meaning are as follows:

Count	State
−4	Set by SIO
−3	Command byte from host
−2	Drive select byte from host
−1	Sector select byte from host
0	Track select byte from host
+1	First data byte (in or out)
+2	Second data byte (in or out)
.	.
.	.
.	.
+128	Last data byte (in or out)

Register R14—CRC Byte 1

Register R14 contains the LSB of the CRC word that is compiled when data is written for use when the data is read back from a disc. During the error recovery routine, Register R14 temporarily stores the target track number from Register R11.

Register R15—CRC Byte 2

Register R15 contains the MSB of the CRC word.

WORKING REGISTER (WR) BUS

As shown in Fig. 3-8, the information present on the WR bus is obtained from one of 24 open-collector sources, counting the 16 separate Working Resistors. The WR bus provides the input to the A port of the ALU during arithmetic and logic operations. During a jump instruction, the WR bus provides the target address to the ROM Instruction Register from either the RIR bus (RIRS true) or one of the Working Registers (RIRS false).

ACCUMULATOR

The Accumulator is an 8-bit latch (U3070) that serves as the input source for the B port of the ALU. Information on the TB bus is clocked into the Accumulator when signal ACCD is active; this signal designates the Accumulator as the destination of an ALU operation.

$\overline{WR}$ Bus Bit*

7	6	5	4	3	2	1	0	Source	Op Code Label
$\overline{WR7}$	$\overline{WR6}$	$\overline{WR5}$	$\overline{WR4}$	$\overline{WR3}$	$\overline{WR2}$	$\overline{WR1}$	$\overline{WR0}$	Working Register	R0-R15
$\overline{RIR7}$	$\overline{RIR6}$	$\overline{RIR5}$	$\overline{RIR4}$	$\overline{RIR3}$	$\overline{RIR2}$	$\overline{RIR1}$	$\overline{RIR0}$	RIR Bus LS Byte	I
$\overline{TRK00}$	$\overline{INDEX}$	$\overline{C0}$	$\overline{SECTOR}$	$\overline{C1}$	$\overline{S}$	1	READY	Input Control Status	CSW
$\overline{DATA}$	1	1	1	1	1	1	1	Sector Buffer to MSB	SBH
1	1	1	1	1	1	1	$\overline{DATA}$	Sector Buffer to LSB	SBL
$\overline{DATA}$	1	1	1	1	1	1	1	Input Read Data	DBT
$\overline{DB7}$	$\overline{DB6}$	$\overline{DB5}$	$\overline{DB4}$	$\overline{DB3}$	$\overline{DB2}$	$\overline{DB1}$	$\overline{DB0}$	Input Host Output Byte	BYT
1	1	$\overline{SW5}$	$\overline{SW4}$	$\overline{SW3}$	$\overline{SW2}$	$\overline{SW1}$	0	Interleave Switch S4104	INL
$\overline{SR7}$	$\overline{SR6}$	$\overline{SR5}$	$\overline{SR4}$	$\overline{SR3}$	$\overline{SR2}$	$\overline{SR1}$	$\overline{SR0}$	Input Test Panel	TST

*1 = high level = logic false state.

2587-19

Fig. 3-8. Working Register (WR) Bus Formats.

ALU FUNCTION GENERATOR

All arithmetic and logic functions required by the microprogram are performed by the 8-bit ALU Function Generator (U3050, U3060). The results of an operation are temporarily stored in the T-Register (discussed later in this section). The logic mode is forced by RIR 7 (for Type A Register Group instructions) or by RIRS (for Type S instructions). A carry CO output is generated when the CI input from the Carry Generator circuit is active, except during the logic mode when the CI input is ignored. A map of the ALU functions is presented in Table 3-2. (Refer to Microprogram Description in this section for applications of ALU functions.)

CARRY INPUT GENERATOR

When active, the carry (CI) input to the ALU forces a carry to be added to the result. The carry input is generated (gates U6070B,C) when enabled by bit RIR 6, signifying an arithmetic function with carry is required (during certain Type A or U instructions). The carry is forced either by the instruction (RIR 9) or by a carry from the previous instruction (CARRY) stored in the Carry flip-flop (U5010B).

CARRY FLIP-FLOP

The C7 carry output of the ALU during the arithmetic mode (M) is applied directly to the Read/Write Logic and is stored temporarily in the Carry flip-flop (U5010B). The CARRY output serves as a jump condition for the Jump Control circuit and is circulated back into the ALU via the Carry Input Generator during ADC and RLC functions.

T-REGISTER

The T-Register is an 8-bit, direct-set latch (U4070, U4080) that provides temporary (single instruction) storage for the ALU result when LTCH EN is active. Thus, the T-Register is clocked during execution of Types A, U, and L Immediate Group instructions, when ALU functions are required. The T-Register is inhibited during a jump instruction (Type L Transfer Groups) or when the Instruction Decoder latches are conditioned (Type S instructions).

TB BUS

The contents of the T-Register are stored via the TB bus in the Accumulator (ACCD true), the selected Working Register (RAMD true), or the Device Address Latch (GROUP Ø EN true); the storage location is a function of the destination field of the RIR word. During a jump execution (RARD true), the T-Register supplies four of the jump conditions to the Jump Control Circuit.

Table 3-2

ALU FUNCTION MAP

LABEL	CODE						FUNCTION	
RIR Bit	11	10	9	8	7	6		
[a]ALU Control	S3	S2	S1	S0	M	CI	(Output (F=)	Description
ADD	1	0	1	0	1	1	A plus B	Add
ADC	1	0	1	0	1	0	A plus B plus 1	Add with Carry
SUB	0	1	0	1	1	0	A minus B	Subtract
INC	1	1	0	0	1	0	A plus 1	Increment
DEC	0	0	1	1	1	1	A minus 1	Decrement
RLL	1	1	1	1	1	1	A plus A	Shift Left with Carry
RLC	1	1	1	1	1	0	A plus A plus 1	Rotate Left with Carry
LMN	0	0	0	0	1	1	−1	Result = −1 s
LON	0	0	0	0	0	0	+1	Result = +1 s
LRZ	1	1	1	1	0	0	0	Result = 0
XOR	1	0	1	0	0	0	A + B	Logical Exclusive OR
LOD	1	1	0	0	0	0	A	Pass Operand (Load)
CMD	0	0	1	1	0	0	A	Complement
NXR	0	1	0	1	0	0	A + B	Logical Exclusive NOR
NOR	0	1	1	1	0	0	A + B	Logical NOR
NAN	0	0	1	0	0	0	AB	Logical NAND
AND	1	1	0	1	0	0	AB	Logical AND
OR	1	0	0	0	0	0	A + B	Logical OR

[a]All ALU control inputs are positive true; this notation is used to simplify correlating ALU function with RIR bus levels; bit 6-9 are inverted before application to the ALU.

JUMP CONTROL CIRCUIT

The Jump Control circuit forces the ROM to jump to a target address; the address is obtained from the WR bus when a selected jump condition is recognized. An 8-to-1 data selector (U4090) decodes the instruction word (RIR 9, 10, 11) to select the jump condition. A forced jump is enabled by RARD at gates U5090A,B only during Type L Transfer Group instructions. The sense (i.e., TB4 or TB4) of the jump condition is selected by RIR 8. When a jump is detected by gate U3020B, the ROM Address Register is loaded from the WR bus and an active jump freeze (JMP FRZ) signal is set in the ROM Instruction Register latch. JMP FRZ holds the jump condition for a full machine cycle, as RARD goes false at the start of the jump instruction. (Refer to the Microprogram Description in this section for definitions of jump codes used in the Type L Direct Transfer and Through-Register Transfer Groups.)

SECTOR BUFFER

The Sector Buffer (shift register U6020) accepts and stores 128 bytes of serialized sector data either directly from the Disc Drive (SELECT CARRY false) or from the System Processor (SELECT CARRY true) via the Read Logic after serialization by the ALU. Each of the 1024 data bits is clocked into the Sector Buffer by the START PUSH pulse via the Read Logic when enabled by the EN STACK command. The EN STACK and SELECT CARRY signals are activated by the ESK and RDC Type S instructions, respectively. The Sector Buffer output is put on the MSB of the WR bus by INPUT SECTOR MSB signal (SBH, Type A Input Group instruction) during data formatting operations, and on the LSB of the WR bus by the INPUT SECTOR LSB signal (SBL, Type A Input Group instruction) when the CRC word is being compiled.

DC-TO-DC CONVERTER

The Dc-to-Dc Converter serves as a precisely filtered −12 volt source for the Sector Buffer. The 5 MHz clock T1B is converted to a chopped dc level by four-bit counter U7010. The symmetrical squarewave output is rectified to a negative level by CR8016 and CR8017, smoothed by C8014 and R8017, and clamped by CR8018.

READ AND WRITE LOGIC

The Read and Write Logic controls the serializing, deserializing, and formatting of input and output data.

Read Logic

The Read Logic comprises the Data Ready flip-flop (U4010A, U5010A), Stack flip-flop (U5020B), and Push flip-flop (U5020A). When sector data is to be read from the Disc Drive, the Stack flip-flop is enabled by the EN STACK signal (ESK, Type S instruction), and the Sector Buffer is switched to the SEPARATED DATA input (RDD, Type A Input Group instruction by default). The Controller waits until the SEPARATED CLOCK pulse arrives, which enables the Data Ready flip-flop to be set by the next TØ clock pulse. The following instruction produces two parallel functions: (1) the START PUSH signal (Op Code SPSH) clears the Data Ready flip-flop and sets the Stack flip-flop, which clocks the value of the SEPARATED DATA line into the Sector Buffer; and (2) the INPUT READ DATA signal places the SEPARATED DATA bit on the MSB of the WR bus for CRC checking by the ALU. The next instruction produces the FINISH PUSH signal (Op Code EPSH), which resets the Stack flip-flop.

The subroutine described above is repeated for each of the remaining 1023 data bits. Preceding the receipt of the sector data, the sync, track and sector bytes are placed on the WR bus, as described above, but the Sector Buffer is inhibited by the inactive EN STACK signal; thus, the parallel push operation does not occur.

The Push flip-flop places the carry C7 bit from the ALU into the Sector Buffer. This occurs when sector data is being received from the System Processor or when data is being circulated from the Sector Buffer through the ALU, i.e., when the CRC word is being generated during a write mode. In these cases, (1) the Stack flip-flop is enabled by the EN STACK signal; (2) the Sector Buffer is switched to the IN2 port by the SELECT CARRY signal; (3) the START PUSH signal conditions the Stack flip-flop and clocks the Push flip-flop to the value of the carry C7 line; (4) the T1 pulse clocks the Stack flip-flop, which in turn clocks the value of the Push flip-flop into the Sector Buffer; and (5) the FINISH PUSH signal resets the Stack flip-flop.

Write Logic

The Write Logic, which comprises the write flip-flop (U4010B) and NAND gate (U6070A), generates the NRZ data that the Disc Drive writes on the flexible disc. The write flip-flop is conditioned by the output of the NAND gate, which is strobed by the carry C7 signal from the ALU and enabled by the LOAD WRITE DATA signal (Op Code PULL). The carry C7 signal causes the write flip-flop to produce the Double Frequency FM code, in which a clock pulse is followed by a logic 1 in 2 μs or by another clock pulse in 4 μs.

MICROPROGRAM DESCRIPTION

A microprogram directs all Controller functions in response to the control and command bytes received from the System Processor. The microprogram consists of a series of microinstructions stored in the ROM. An annotated listing of the microinstructions is presented in Appendix C. In the listing, each microinstruction is described in symbolic form by an Op Code that is formatted according to type and class of instruction it represents. The format and content of each kind of Op Code is defined in Fig. 3-9 through 3-15. Refer back to Tables 3-1 and 3-2.

A. Op Code Example: DEC SR,A,R14

B. Field Definition:

Source		Destination		ALU Function						Reg. Addr.				Spec.	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

C. Restrictions:

Source	Destination	ALU Function	Register Addr	Special*
SR (01)	L,DR,A [See D(1)]	Label [See D(2)]	Any [See D(3)]	Any [See D(4)]

D. Special Coding:

(1) Destination:

Label	13	12	Description
L	0	0	TB bus data is not stored
DR	0	1	Store TB data in Register
A	1	0	Store TB data in Accumulator

(2) ALU Function:

Label	11	10	9	8	7	6	Function
ADD	1	0	1	0	1	1	Add
SUB	0	1	0	1	1	0	Subtract
INC	1	1	0	0	1	0	Increment
DEC	0	0	1	1	1	1	Decrement
OR	1	0	0	0	0	0	Logical OR
AND	1	1	0	1	0	0	Logical AND
NAN	0	0	1	0	0	0	Logical NAND
NOR	0	1	1	1	0	0	Logical NOR
NXR	0	1	0	1	0	0	Logical Exclusive NOR
CMD	0	0	1	1	0	0	Complement
LOD	1	1	0	0	0	0	Pass Operand
ADC	1	0	1	0	1	0	Add with Carry
XOR	1	0	1	0	0	0	Logical Exclusive OR
RLC	1	1	1	1	1	0	Rotate Left with Carry
RLL	1	1	1	1	1	1	Shift Left with Carry
LRZ	1	1	1	1	0	0	Result = 0
LMN	0	0	0	0	1	1	Result = −1s
LON	0	0	0	0	0	0	Result = 1s

2587-20

Fig. 3-9a. Type A Register Group Instruction Format.

(3) Register Address: R0 (0000) through R15 (1111).

*(4) Special:

Label	1	0	Description
None	0	0	No special function
SPSH	0	1	Start pushing carry C7 into Sector Buffer
PULL	1	0	Load Write Data flip-flop with carry C7
EPSH	1	1	Finish pushing carry C7 into Sector Buffer

E. Remarks: (1) Source label SR indicates the Working Registers as $\overline{WR}$ bus source.

*(2) Special command is added to Op Code only if concurrent control of the Sector Buffer or Write Data flip-flop is required.

2587-21

Fig. 3-9b. Type A Register Group Instruction Format.

A. Op Code Example: LOD IN,A,SBH

B. Field Definition:

Source		Destination		ALU Function						Source Addr				Spec.	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

C. Restrictions:

Source	Destination	ALU Function	Source Addr	Special*
IN (11)	L,A [See D(1)]	Label [See D(2)]	Label [See D(3)]	Any [See D(2)]

D. Special Coding:

(1) Destination:

Label	13	12	Description
L	0	0	TB Bus data is not stored
A	1	0	Store TB data in Accumulator

(2) ALU Function and Special: Same as Register Group.

(3) Source Address:

Label	5	4	3	2	$\overline{WR}$ Bus Input from
None	0	0	0	0	Not used
TST	0	0	0	1	Test Panel switches
CSW	0	0	1	0	Input control/status byte
SBH	0	0	1	1	Sector Buffer to high bit ($\overline{WR7}$)
SBL	0	1	0	0	Sector Buffer to low bit ($\overline{WR0}$)
DBT	0	1	0	1	Read data bit ($\overline{WR7}$)
BYT	0	1	1	0	Host output byte
INL	0	1	1	1	Interleave switch S4104

E. Remarks: (1) Source label IN indicates that Inputs are $\overline{WR}$ bus source.

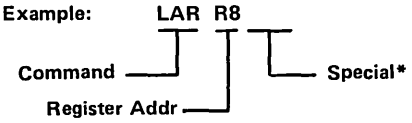
*(2) Special command is added to Op Code only if concurrent control of the Sector Buffer or Write Data flip-flop is required.

2587-22

Fig. 3-10. Type A Input Group Instruction Format.

@

A. Op Code Example: LAR R8



B. Field Definition:

Unary Command										Reg. Addr.				Spec.	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

C. Restrictions:

Unary Command	Register Addr	Special*
Label	Any	Any
[See D(1)]	[See D(2)]	[See D(3)]

D. Special Coding:

(1) Unary Command:

	Source		Dest.		ALU Function						
Label	15	14	13	12	11	10	9	8	7	6	Description
LAR	0	1	1	0	1	1	0	0	0	0	Load Accumulator from Register
LRA	0	1	0	1	1	0	0	1	0	0	Load Register from Accumulator
COM	0	1	1	0	0	1	1	0	0	0	Complement Accumulator
CMR	0	1	1	0	0	0	1	1	0	0	Complement Register
LCA	0	1	0	1	0	1	1	0	0	0	Load Register with Complement of Accumulator
LCR	0	1	1	0	0	0	1	1	0	0	Load Accumulator with Complement of Register
LRZ	0	1	0	1	0	1	1	1	0	0	Load Register with 0s
LAZ	0	1	1	0	1	1	1	1	0	0	Load Accumulator with Os
LRM	0	1	0	1	0	0	0	0	1	1	Load Register with 1s
LAM	0	1	1	0	0	0	0	0	1	1	Load Accumulator with 1s
NOP	0	0	0	0	0	0	0	0	0	0	Wait (No Operation)
LDL	0	0	0	1	0	0	0	0	0	0	Load Latches

(2) Register Addr and (3) Special: Same as Type A Register Group.

E. Remarks: (1) Source of $\overline{WR}$ bus is Registers.

*(2) Special command is added only if concurrent control of Sector Buffer or Write Data flip-flop is required.

2587-23

Fig. 3-11. Type U Unary Instruction Format.

A. Op Code Example: RSP

Command

B. Field Definition:

Source		Destination		Command						(Not Used)					
				Type		Function									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

C. Restrictions:

Source	Destination	Command
No Code*	L	Label
(00)	(00)	(See D)

D. Special Coding:

(1) Command Type:

Label	11	10	9	8	7	6	Hex	Description
CDA	0	0	1	0	0	0	0200	Load Drive Address
Noted	0	1	x	x	x	x	See D(2)	Command Group 1
Noted	1	0	x	x	x	x	See D(2)	Command Group 2
RST	1	1	0	0	0	0	0C00	Reset Group 1
NOP	0	0	0	0	0	0	0000	No operation (Wait)

(2) Command Function:

Group 1

Label	9	8	7	6	Hex	Command
RBY	0	0	0	0	0400	Reset BUSY
SBY	1	0	0	0	0600	Set BUSY
RIP	0	0	0	1	0440	Reset ILLEGAL OP
SIP	1	0	0	1	0640	Set ILLEGAL OP
RER	0	0	1	0	0480	Reset ERROR RECOVERY
SER	1	0	1	0	0680	Set ERROR RECOVERY
RCK	0	0	1	1	04C0	Reset UNIT CHECK
SCK	1	0	1	1	06C0	Set UNIT CHECK
RFI	0	1	0	0	0500	Reset FILE INOP RST/LD HD
SFI	1	1	0	0	0700	Set FILE INOP RST/LD HD
RWR	0	1	0	1	0540	Reset WRITE GATE
SWR	1	1	0	1	0740	Set WRITE GATE
RPT	0	1	1	0	0580	Reset PRINT STRB
SPT	1	1	1	0	0780	Set PRINT STRB
SFG	0	1	1	1	05C0	Set HOST FLG
RFG	1	1	1	1	07C0	Reset HOST FLG

2587-24

Fig. 3-12a. Type S Output Group Instruction Format.

(2) Command Function: (Continued)

Group 2

Label	9	8	7	6	Hex	Command
RHD	0	0	0	0	0800	Reset RAISE HEADS
SHD	1	0	0	0	0A00	Set RAISE HEADS
DR0	0	0	0	1	0840	Reset DIRECTION (IN)
DRI	1	0	0	1	0A40	Set DIRECTION (IN)
RSP	0	0	1	0	0880	Reset STEP
SSP	1	0	1	0	0A80	Set STEP
DSK	0	0	1	1	08C0	Reset EN STACK
ESK	1	0	1	1	0AC0	Set EN STACK
EDY	0	1	0	0	0B00	Reset EN DISPLAY
DDY	1	1	0	0	0900	SET EN DISPLAY
RDD	0	1	0	1	0940	Reset SELECT CARRY
RDC	1	1	0	1	0B40	Set SELECT CARRY
TKL	0	1	1	0	0980	Reset > TRK43
TKH	1	1	1	0	0B80	Set > TRK43
SLB	0	1	1	1	09C0	Reset UBANK
SHB	1	1	1	1	0BC0	Set UBANK

E. Remarks: (1) Command Groups 1 and 2 globally reset on power up.

*(2) Source selects Instruction Decoder latches.

2587-25

Fig. 3-12b. Type S Output Group Instruction Format.

A. Op Code Example: LOD I,A,Value

Function — LOD
Source — I
Destination — A
Data Byte — Value

B. Field Definition:

Source		Destination		ALU Function				Data Byte							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

C. Restrictions:

Source	Destination	ALU Function	Data Byte
I	L,A	Label	Any
(RIR)	(None,Acc.)	(See D)	(RIR)

D. Special Coding:

Label	11	10	9	8	Description
OR	1	0	0	0	Logical Inclusive OR
XOR	1	0	1	0	Logical Exclusive OR
AND	1	1	0	1	Logical AND
NAN	0	0	1	0	Logical NAND
NOR	0	1	1	1	Logical NOR
NXR	0	1	0	1	Logical Exlusive NOR
LOD	1	1	0	0	Pass Operand
NOP	1	1	1	1	Results = 0

E. Remarks:
(1) Registers (DR,R) cannot be used as a destination.
(2) ALU is forced into Logic mode.
(3) Data byte is used by ALU as operand.

2587-26

Fig. 3-13. Type L Immediate Group Instruction Format.

A. Op Code Example: J4Z I,M,Address

Condition — J4Z
Source — I
Destination — M
Target Address* — Address

B. Field Definition:

Source		Destination		Condition				Target Address							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

C. Restrictions:

Source	Destination	Condition	Target Address*
I	M	Label	Any of 256
(RIR)	(RAR)	(See D)	(RIR)

D. Special Coding:

Label	(11	10	9	8)	Condition: Jump On
JMP	1	1	1	0	Unconditional Jump
JNZ	0	0	0	0	Non-Zero Result
JZR	0	0	0	1	Zero Result
JDR	1	1	0	0	Data Ready
JNR	1	1	0	1	Data Not Ready
JLB	1	0	1	0	Bit 0 = True
JLZ	1	0	1	1	Bit 0 = False
J2N	1	0	0	0	Bit 2 = True
J2Z	1	0	0	1	Bit 2 = False
J4N	0	1	0	0	Bit 4 = True
J4Z	0	1	0	1	Bit 4 = False
J6N	0	0	1	0	Bit 6 = True
J6Z	0	0	1	1	Bit 6 = False
JNC	0	0	1	0	Carry = True
JZC	0	0	1	1	Carry = False

E. Remarks: (1) Source defines RIR bus as source of target address.

(2) Transfer from Source (RIR) to Destination (RAR) occurs only on specified jump condition

*(3) Destination (target) address is the 1s complement of the address on RIR bus.

2587-27

Fig. 3-14. Type L Direct Transfer Group Instruction Format.

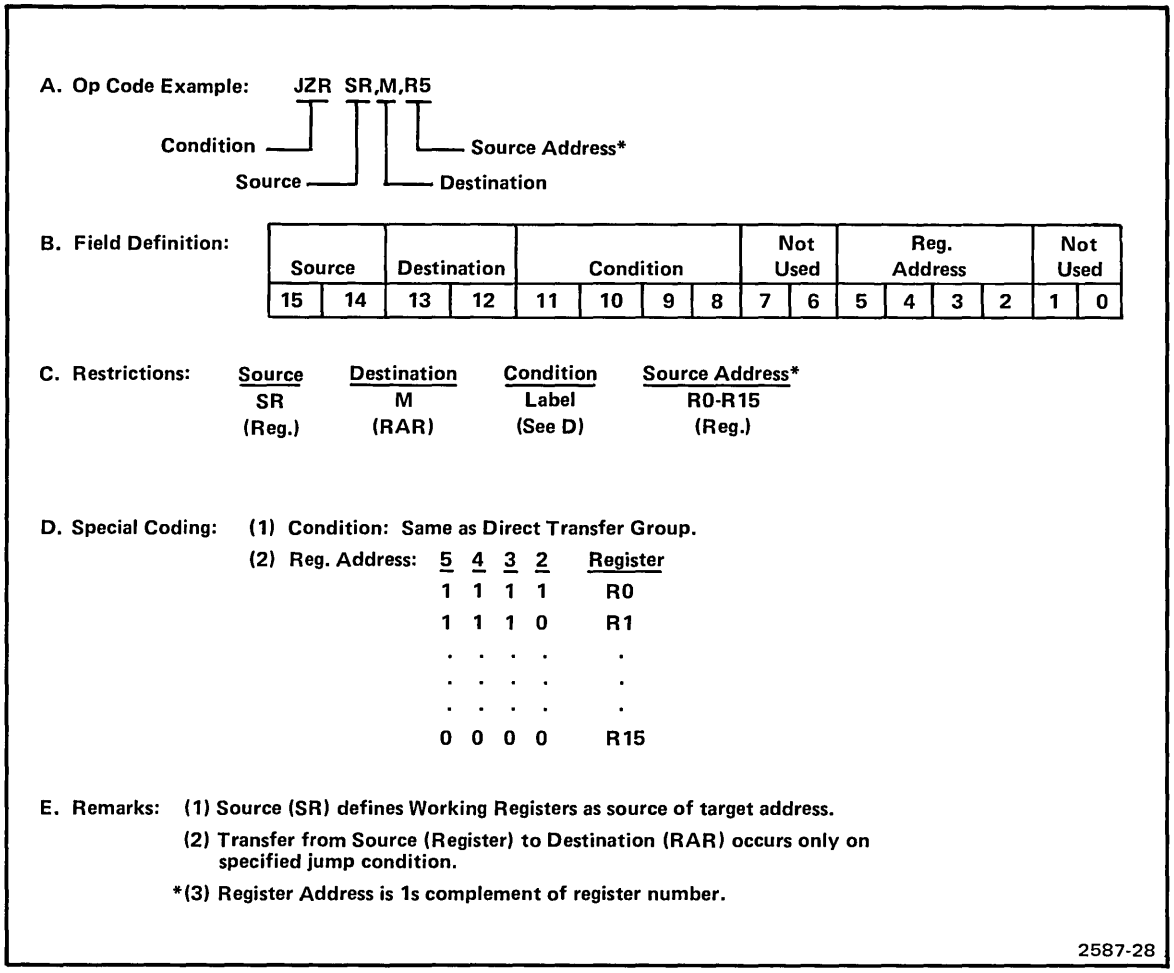


Fig. 3-15. Type L Through-Register Transfer Group Instruction Format.

The microprogram is organized into five routines: (1) Executive; (2) Seek; (3) Read; (4) Write; (5) Error Recovery and Cleanup. The remainder of this section discusses each of these routines.

EXECUTIVE ROUTINE

The executive routine runs continuously while looking for events. It monitors the state of the Disc Drive and the input control byte from the System Processor. The executive routine determines the appropriate response to the input control request, based on the operating state of the Controller. Tasks performed by the executive routine include selection of the Disc Drive, loading and unloading the read/write head, sector counting, and I/O control. Subroutines are as follows:

(1) Power On: Initializes all Controller circuits, and provides a 2.5 second delay to allow the Disc Drives to reach full running speed.

(2) EX3: The main scan loop, triggered by the following signals:

   a. Strobe (S); starts communication with the System Processor.

   b. INDEX; updates the head-up delay and resets the sector counter.

   c. SECTOR; updates the sector count and synchronizes other major subroutines (read, write, CRC generation).

(3) E6B: Output data service request (OTD).

(4) E6A+: Print command or input data request (IND).

(5) SIO: Start I/O operation.

(6) EX8: Input data service.

(7) E9B: Read diagnostic service.

(8) EX7: Target track input.

(9) DTA: Receive output data byte from System Processor.

(10) SCT: Target sector input.

(11) DRV: Drive address input.

(12) CNT = −2: Input and interpret command byte.

(13) EX5: Looks for tasks ready for execution that require sector sync.

SEEK ROUTINE

The seek routine issues DIRECTION and STEP commands to the Disc Drive. These commands position the read/write head to the target track (Track X). The TRACK 00 signal from the Disc Drive is used as reference for maintaining the current track (Track N) count. STEP commands are issued until Track X equals Track N.

READ ROUTINE

The read routine verifies the sector ID header, inputs the sector data in the Sector Buffer, compiles the CRC word during the write modes, and checks the CRC word against the data read from the disc during the read modes. Subroutines are as follows:

(1) RD: Handles the read and read ID functions, and is the entry point for CRC generation.

(2) ICRC: Generates the CRC word.

(3) RD1: Searches for the sync byte (hex FB).

(4) RD2: Inputs the track byte and checks it against Track X if GTID1 is false (track position is known).

(5) RD3: Inputs the sector byte and checks it against Sector X if both GTID1 and GTID2 are false.

(6) RD4: Compiles the CRC word during the write mode, or checks the CRC word against data read from the disc.

CRC Generation

The CRC word is generated by a microcode equivalent of a Modulus 2 divider circuit (A + B plus 1). As shown in Fig. 3-16, the CRC polynomial is $X^{16} + X^{12} + X^5 + 1$. The CRC word is compiled during the write mode in registers R1 and R2, then shifted into registers R14 and R15. The sector and track bytes are processed first, followed by 128 sector data bytes, which are circulated from the Sector Buffer through the ALU. After compilation is finished, the contents of registers R1 and R2 are shifted into registers R14 and R15 by a series of 16 0s.

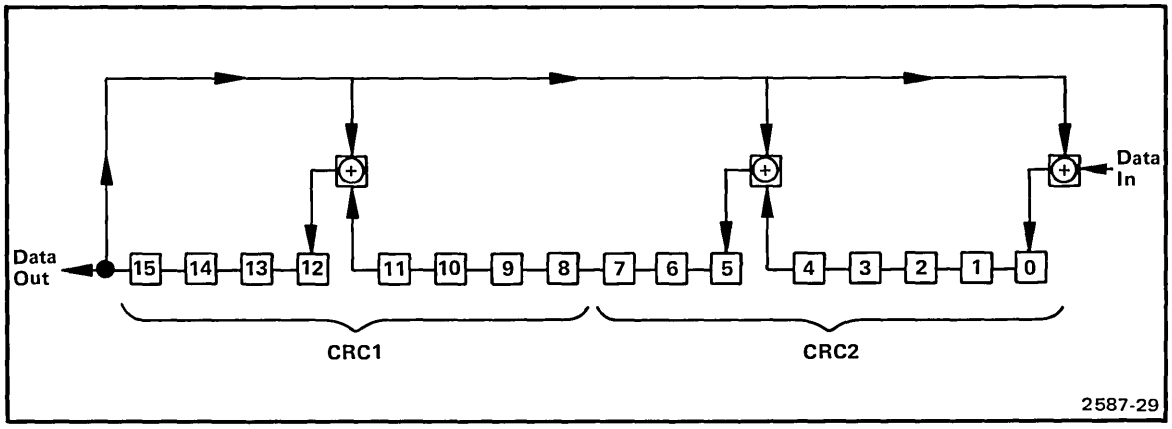


Fig. 3-16. CRC Generator Schematic.

WRITE ROUTINE

The write routine formats all of the data that is written in a disc sector. It generates the preamble, sync byte, and postamble; and it transfers the header ID, sector data, and CRC word. The write routine encodes the transmitted data into the Double Frequency FM format, establishing a 4 μs bit period by adding clock pulses to the data stream. The write routine includes the following subroutines:

(1) WRT: The entry point for the write routine. Initializes the Disc Drive by sending one clock pulse, then setting the WRITE GATE command. Initialization is a safety requirement of the Disc Drive that prevents unintentional writing.

(2) DOUT: A subroutine that encodes and sends a byte of data to the Disc Drive. The return vector is stored in register R12.

(3) WRT 1: Sends the 120-bit preamble of 0s, followed by the sync byte.

(4) WRT 3: Sends the target track byte.

(5) WRT 4: Sends the target sector byte.

(6) WRT 5, A, B: Sends the contents of the Sector Buffer one byte at a time. DOUT subroutine is not used.

(7) WRT 6, 7: Sends the CRC word.

(8) WRT 8: Sends the postamble of 0s until the leading edge of the SECTOR pulse is detected.

ERROR RECOVERY AND CLEANUP ROUTINE

The error recovery and cleanup routine checks the program flag byte (register R3) for an error state, causes the Disc Drive to wipe the disc if a read error is detected, and performs the cleanup and indexes the track and sector counts after successful reads. This routine includes the following subroutines:

(1) X: The entry point for the error recovery routine when an error return from a read or read ID operation occurs.

(2) X2: The entry point for a successful return from a read or write operation. Performs cleanup and indexes sector and track count.

(3) X1: Causes the Disc Drive to wipe the disc. The read/write head is stepped out to track 00, then to track 76, and back to Track X.

(4) STCK: Checks the program flag byte to see if an error state exists.

Section 4

MAINTENANCE

INTRODUCTION

This section describes procedures for preventing or reducing equipment malfunction, and includes techniques for troubleshooting and corrective maintenance. Preventive maintenance improves equipment reliability. Should the equipment fail to function properly, corrective measures should be taken immediately; otherwise, additional problems may develop within the equipment.

CAUTION

STATIC DISCHARGE CAN DAMAGE MANY SEMICONDUCTOR COMPONENTS USED IN THIS EQUIPMENT.

Many semiconductor components, especially MOS types, can be damaged by static discharge. The damage may not be catastrophic, and therefore may not be immediately apparent. A "weakening" of the semiconductor characteristics may indicate that damage has occurred. Devices that are particularly susceptible are: MOS, CMOS, JFET, and high-impedance operational amplifiers. Damage can be significantly reduced by observing the following precautions:

1. Handle static-sensitive components or circuit assemblies on a static-free surface. Work station areas should contain a static-free bench cover or work plane, such as conductive polyethylene sheeting and grounding wrist strap. The work plane should be connected to earth ground.

2. All test equipment, accessories, and soldering tools should be connected to earth ground.

3. Minimize handling by keeping the components in their original containers until ready for use. Minimize the removal and installation of semiconductors from their circuit boards.

4. Hold the IC devices by the body rather than by the terminals.

5. Use containers made of, or filled with, conductive material, for storage and transportation. Avoid using ordinary plastic containers. Any static-sensitive part or assembly (circuit board) that is to be returned to Tektronix, Inc., should be packaged in its original container or in one with anti-static packaging material.

REDUCTION OF SUSCEPTIBILITY TO STATIC DISCHARGE

The following safeguards have been provided within the 8002 μProcessor Lab system to minimize susceptibility to static discharge:

1. The ground (earth) wire of the primary power cable is connected to the chassis where the cable enters the unit.

2. The shields of interconnecting EIA cables are grounded to the chassis at the cable entrance or egress of each unit.

3. All interconnecting ribbon cables have a built-in ground plane which is grounded to the chassis at the cable entrance or egress of each unit.

4. Ground loops have been avoided by installing a common ground between all units. Grounding straps are utilized where necessary. Refer to the 8001/8002 μProcessor Lab Installation Guide.

CAUTION

Violation or modification of the preceding safeguards can result in ground loops and/or static discharge problems.

PREVENTIVE MAINTENANCE

Preventive maintenance consists of cleaning, visual inspection, and performance check. The preventive maintenance schedule established for the equipment should be based on the amount of use, and on the environment in which the equipment is operated.

Cleaning

Clean the equipment often enough to prevent dust or dirt from accumulating in or on it. Dirt acts as a thermal insulating blanket and prevents efficient heat dissipation. It also provides high-resistance electrical leakage paths between conductors or components in a humid environment.

EXTERIOR

Clean the dust from the outside of the equipment by cleaning the surface with a soft cloth or brush. The brush will remove dust from around the front panel selector buttons. Hardened dirt may be removed with a cloth dampened in water that contains a mild detergent. Abrasive cleaners should not be used.

INTERIOR

Normally the interior of the equipment will not require cleaning unless it has been left uncovered for an extended period of time. Clean the interior by loosening accumulated dust with a dry soft brush, then blow the loosened dirt away with low-pressure air.

High-velocity air can damage some components. If the circuit board assemblies need cleaning, remove the circuit board and clean with a dry soft brush. Hardened dirt or grease may be removed with a cotton-tipped applicator dampened with a solution of mild detergent and water. Do not leave detergent on critical memory components. Abrasive cleaners should not be used.

After cleaning, allow the interior to dry thoroughly before applying power to the equipment.

CAUTION

Do not allow water to get inside any enclosed assembly or components, such as switch assemblies, memory capacitors, potentiometers, etc. Instructions for removing assemblies for maintenance are provided in the Corrective Maintenance part of this section. Do not clean any plastic materials with organic cleaning solvents (such as benzene, toluene, xylene, acetone, or similar compounds); they may damage the plastic.

VISUAL INSPECTION

After cleaning, carefully check the equipment for such defects as defective connections and damaged parts. The remedy for most visible defects is obvious. If heat-damaged parts are discovered, try to determine the cause of overheating before replacing the damaged part; otherwise, the damage may be repeated.

TROUBLESHOOTING

The following aids and suggestions may assist in locating a problem. After the defective assembly or component has been located, refer to the Corrective Maintenance part of this section for removal and replacement instructions.

Troubleshooting Aids

DIAGRAMS

Circuit diagrams are given on foldout pages in the Diagrams section of the manual. The circuit number and electrical value of each component are shown on the diagram (see the first tab page for definition of the reference symbology used to identify components in each circuit). Components on circuit boards are assigned vertical and horizontal grid numbers which correspond to the location of the component on the circuit board. Refer to the Replaceable Electrical Parts list section for a complete description of each component and assembly. Those portions of the circuit that are on circuit boards are enclosed with a black border line, with the name and assembly number shown on the border.

NOTE

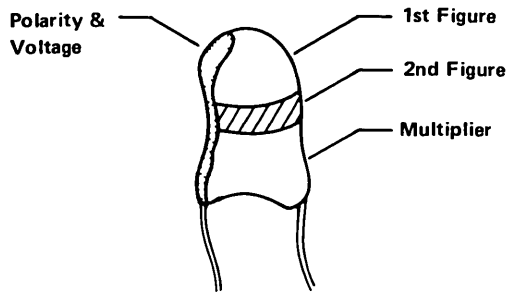
Corrections and modifications to the manual and equipment are described on inserts bound into the rear of the manual. Check this Change Information section for manual or instrument changes and corrections.

CIRCUIT BOARD ILLUSTRATIONS

Electrical components, connectors, and test points are identified on circuit board illustrations located on the inside fold of the corresponding circuit diagram or on the back of the preceding diagram. This allows cross-referencing between the diagram and the circuit board, and shows the physical location of components.

CAPACITOR MARKING

The capacitance value of common disc capacitors and some electrolytics is marked in microfarads on the side of the component body. The white ceramic capacitors are color-coded in picofarads. Tantalum capacitors are color-coded as shown in Fig. 4-1.



DIPPED TANTALUM CAPACITOR MARKING

A AND B CASE

CAPACITANCE AND VOLTAGE COLOR CODE

Rated Voltage VDC 25°C	Color	CODE FOR CAPACITANCE IN PICOFARADS		
		1st Figure	2nd Figure	Multiplier
3-4	Black	0	0	None
3-6	Brown	1	1	X10
3-10	Red	2	2	$X10^2$
3-15	Orange	3	3	$X10^3$
3-20	Yellow	4	4	$X10^4$
3-25	Green	5	5	$X10^5$
3-35	Blue	6	6	$X10^6$
3-50	Violet	7	7	$X10^7$
	Gray	8	8	
3	White	9	9	

(1733) 2312-15

Fig. 4-1. Tantalum Capacitor Color Code.

@

DIODE CODE

The cathode of each glass-encased diode is indicated by a stripe, a series of stripes, or a dot. Some diodes have a diode symbol printed on one side. Figure 4-2 illustrates diode types and polarity markings that are used in this equipment.

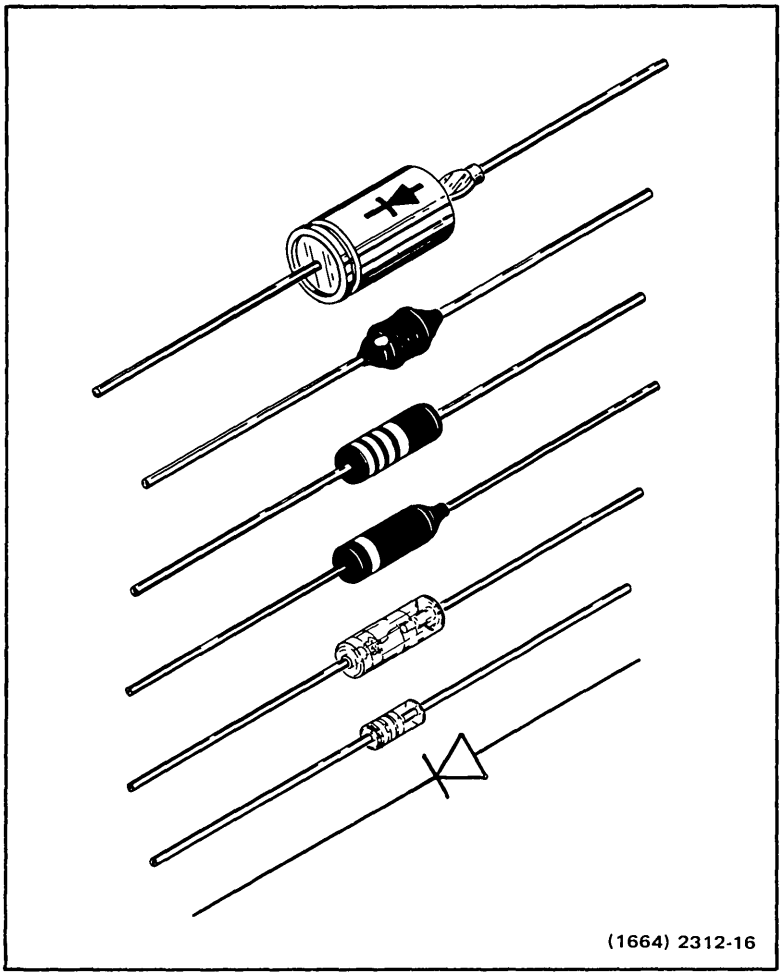


Fig. 4-2. Diode Polarity Marking.

TRANSISTOR AND INTEGRATED CIRCUIT ELECTRODE CONFIGURATION

Lead identification for the transistors is shown in Fig. 4-3. IC pin-out diagrams are shown, when necessary, on the back of the adjoining pullout schematic diagram.

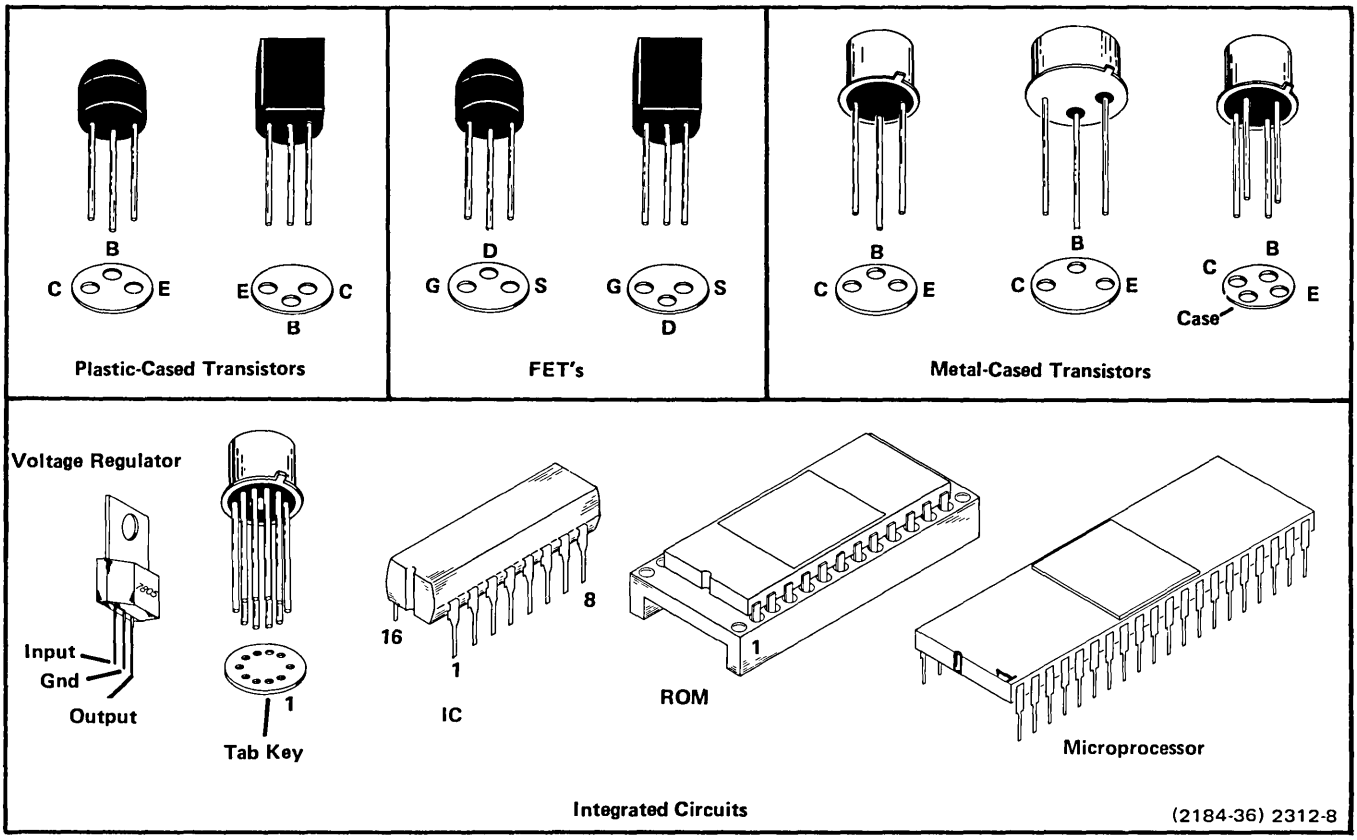


Fig. 4-3. Electrode Configuration For Semiconductor Components.

DIODE CHECKS

Most diodes can be checked in the circuit by taking measurements across the diode and comparing these with voltages listed on the diagram. Forward-to-back resistance ratios can be taken by referring to the schematic and pulling appropriate transistors and pin connectors to remove low-resistance loops around the diode.

CAUTION

Do not use an ohmmeter scale with a high external current to check the diode junction.

INTEGRATED CIRCUIT (IC) CHECKS

When substitution is impossible, check input and output signal states, as described in the Circuit Description and on the diagrams. Lead configuration and data for the IC used in this equipment are provided on the inside fold of the schematic or the back of the previous schematic.

CAUTION

To avoid possible damage from static charges, handle all ICs in accordance with the instructions at the beginning of this section.

@

General Troubleshooting Techniques

The following procedure is recommended to isolate a problem and expedite repair.

1. Using the Diagnostic Tests in the 8002 μProcessor Lab System Service Package (not available at this writing), check the operation of the various modules.

2. Try to isolate the problem to a module and, if possible, to a functional block on the module.

3. Troubleshoot the circuit using standard procedures and tests. A logic analyzer (TEKTRONIX 7403 mainframe with 7D01F plug-in, or equivalent) is a valuable test item for evaluating circuit performance.

4. Determine the extent of the repair needed. If complex, contact your local Tektronix Field Office or representative. If the damage is minor, such as component replacement, see the Parts List for replacement information. Removal and replacement procedures of these assemblies and sub-assemblies are described under Corrective Maintenance.

CORRECTIVE MAINTENANCE

Corrective maintenance consists of component replacement and equipment repair. The following discussion describes special techniques and procedures required to replace components in this equipment.

Obtaining Replacement Parts

Most electrical and mechanical parts are available through your local Tektronix Field Office or representative. The Replaceable Parts list section contains information on how to order these replacement parts. Many standard electronic components can be obtain locally in less time than required to order from Tektronix, Inc. It is best to duplicate the original component as closely as possible. Parts orientation and lead dress should be duplicated because orientation may affect circuit interaction.

If a component you have ordered has been replaced with a new or improved part, your local Field Office or representative will contact you concerning the change in the part number.

Parts Repair and Exchange Program

Tektronix service centers provide replacement or repair service on major assemblies, in addition to the unit itself. Contact your local service center for this service.

Soldering Technique

CAUTION

Disconnect the equipment from its power source before replacing or soldering components.

DISCRETE COMPONENT REPLACEMENT

Because it is easy to damage the plating in the board holes to which the component is soldered, it is recommended to cut the old component free and leave some lead length to solder the new component leads to. If the leads are pulled through the board, use caution when pulling them through the plated hole. Excessive heat or bent leads can damage the plating. Using a 15-watt pencil-type iron, straighten the leads on the back side of the board; then, when the solder melts, gently pull the soldered lead through the hole. A desoldering tool should be used to remove the old solder.

INTEGRATED CIRCUIT REPLACEMENT

Most of the ICs within this equipment are soldered into the module boards; therefore, extreme care must be taken to prevent damage to the module boards if the ICs are removed and replaced. The procedure used to remove ICs from the module boards is dependent upon: the cost of the IC, the competency of the technician accomplishing the repairs, and the degree of certainty that the IC is defective. One of the following procedures is recommended.

1. **Inexpensive ICs or ICs that are known to be defective.** Cut the defective IC from the board. Cut each pin close to the body of the IC, leaving as much of the pin as possible attached to the board. On the back side of the board use a 15-watt pencil-type soldering iron to melt the solder around the pins. When the solder melts, gently pull the pin out of the hole from the component side of the board. Repeat this procedure for each pin. A desoldering tool should be used to remove the old solder. Use caution when pulling the pins through the plated hole. Excessive heat or bent leads can damage the plating. When all pins have been removed and the holes are free of solder, install the new IC (ensure proper orientation of IC pin numbers). Solder each pin from the back side of the board and cut off excess pin length. Visually inspect the board for excess solder or solder bridges before operational testing of the board.

2. **Expensive ICs or ICs that *may* be defective.** On the back side of the board use a 15-watt pencil-type soldering iron to melt the solder around the pins. A desoldering tool should be used to remove the excess solder. Using needle-nose pliers, gently wiggle the pin in the hole while removing the solder. When the pin is free of solder in the hole, repeat the same procedure for each pin on the IC. When all pins are free, use an extracting tool and gently pull the IC from the board. Do not use force if the IC does not come free of the board. Use the soldering iron to remove excessive solder from the pin or pins at the same time the IC is being pulled from the board. When the IC is free of the board, carefully straighten each pin. If the IC is to be replaced or a new IC is to be installed, follow the same procedure as stated above for inexpensive ICs.

NOTE

An extracting tool to remove the ICs may be ordered from Tektronix, Inc. If an extracting tool is not available, use care to avoid damaging the pins. Pull slowly and evenly on both ends of the IC. Try to avoid having one end of the IC disengaged from the board before the other end.

DISASSEMBLY AND REPLACEMENT OF FLEXIBLE DISC UNIT ASSEMBLIES

The Flexible Disc Unit consists of the following major assemblies: front panel, back panel, two disc drives, the +5 Vdc and +24 Vdc power supplies, and the Flexible Disc Controller (circuit board). Removing the power supplies requires an almost complete disassembly of the Flexible Disc Unit; thus, power supply removal is the only disassembly procedure included here.

NOTE

The power supply modules (+5.0 Vdc and +24 Vdc) are listed in the Replaceable Electrical Parts list as one number for each power supply. Component part numbers are not furnished. Complete assembly replacement is recommended.

Both the +5 Vdc and +24 Vdc power supplies are fastened together; if either supply is to be serviced or replaced, both supply modules must be removed from the Flexible Disc Unit.

Replacement or removal of the power supplies requires that all major assemblies except the Controller be removed from the Flexible Disc Unit. The following paragraphs describe the procedure for servicing or replacing a power supply.

1. REMOVAL OF POWER SUPPLIES

WARNING

Before the Flexible Disc Unit is disassembled, make sure that the primary power cord has been disconnected from the pack panel.

a. Remove the three screws on each side of the Flexible Disc Unit. Lift the top cover off the mainframe.

b. Close and latch the covers on both Disc Drives (0 and 1).

c. Remove the four screws in the front cover. Disconnect connector J4 of the main power switch cable. Remove front cover and set aside.

d. Remove the six screws in the rear support bracket: two screws in the disc drives, two screws in the power supply mounting frame, and one screw in each end of the rear support bracket through left and right sides of the mainframe. Remove the rear support bracket and set aside. Remove the screen cover for the power supply.

e. Remove the screw in the front support bracket through the left side of the mainframe. Remove the four screws in the disc drives through the front support bracket.

f. The two Disc Drives are attached to a mounting plate that is secured to the mainframe. Remove the six screws in the mounting plate: three screws on the left side of the mainframe and three screws along right side of mounting plate into bottom of the mainframe.

g. Slide both disc drives about four inches out the front of the unit.

CAUTION

Only the left side of the front support bracket was loosened in Step 1e; therefore, the disc drives must be carefully pulled out of the unit. When pulling the drives out, observe the connecting cable lengths in the rear of the drives; do not pull further than four inches at this time.

h. Disconnect disc drive power connectors P2 and P3. Disconnect the two in-line ribbon cable connectors, one on each disc drive. The disc drives are now free to slide out of the Flexible Disc Unit.

NOTE

To remove a disc drive or to separate the two disc drives for servicing, remove the four screws that attach each disc drive to the mounting plate.

i. Remove the eight screws holding the back panel to the mainframe: six screws through the back panel and one screw in each end of the top motor support bracket through the left and right sides of the mainframe.

j. Tilt the top of the back panel away from the mainframe and disconnect P1. Then remove the four screws attaching the drive expansion plate to the back panel.

k. Free the wires and cabling attached to edge connectors P1, P2, P3, and P4 within the unit. Now remove the back panel and set aside.

l. Disconnect connector P5 on the Flexible Disc Controller. Remove the six screws that secure the power supply mounting frame to the mainframe.

m. Remove the power supply mounting frame (containing both power supplies) from the Flexible Disc Unit. Place the supply mounting frame on a flat work surface.

2. REPLACING DEFECTIVE POWER SUPPLY

If only one of the power supplies is defective, only the defective supply must be replaced. The following replacement procedure is the same for either power supply.

CAUTION

The following procedure requires you to unsolder and remove existing wires on the defective power supply and to reconnect and solder these wires to the replacement power supply. Use extreme care to make sure that the existing wires are not damaged and that the wires are reconnected to their correct terminals.

a. Locate primary winding termination numbers 1 through 4 on the power transformer. For each of these four terminations, cut the protective tubing from the wire and transformer terminal. Unsolder the four terminations and remove the wires. Make sure each wire is tagged as the wires are removed.

NOTE

Only the primary winding terminations are disconnected on the power transformer. The secondary windings are connected internally.

b. Unsolder and remove the output wires. Make sure all wires are tagged.

c. Remove the mounting screws for the defective power supply and separate it from the mounting frame. Using existing mounting brackets, attach the replacement power supply to the mounting frame.

d. Before reconnecting the wires, slip heat-shrink tubing (or similar tubing) over the primary wires; then reconnect and solder the wires removed in Step 2, parts a and b to the terminals of the replacement power supply module. Heat and shrink the tubing over the wires and terminals after soldering. Cover as much of the transformer connecting lugs as possible before shrinking the tubing.

3. REPLACEMENT OF POWER SUPPLIES

To replace the power supply mounting frame in the Flexible Disc Unit, reverse the procedures listed above under "Removal of Power Supplies".

Section 5
REPLACEABLE ELECTRICAL PARTS

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

SPECIAL NOTES AND SYMBOLS

X000	Part first added at this serial number
00X	Part removed after this serial number

ITEM NAME

In the Parts List, an Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

ABBREVIATIONS

ACTR	ACTUATOR	PLSTC	PLASTIC
ASSY	ASSEMBLY	QTZ	QUARTZ
CAP	CAPACITOR	RECP	RECEPTACLE
CER	CERAMIC	RES	RESISTOR
CKT	CIRCUIT	RF	RADIO FREQUENCY
COMP	COMPOSITION	SEL	SELECTED
CONN	CONNECTOR	SEMICOND	SEMICONDUCTOR
ELCTLT	ELECTROLYTIC	SENS	SENSITIVE
ELEC	ELECTRICAL	VAR	VARIABLE
INCAND	INCANDESCENT	WW	WIREWOUND
LED	LIGHT EMITTING DIODE	XFMR	TRANSFORMER
NONWIR	NON WIREWOUND	XTAL	CRYSTAL

CROSS INDEX—MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip
01121	ALLEN-BRADLEY COMPANY	1201 2ND STREET SOUTH	MILWAUKEE, WI 53204
01295	TEXAS INSTRUMENTS, INC., SEMICONDUCTOR GROUP	P O BOX 5012, 13500 N CENTRAL EXPRESSWAY	DALLAS, TX 75222
04009	ARROW-HART, INC.	103 HAWTHORNE STREET	HARTFORD, CT 06106
04713	MOTOROLA, INC., SEMICONDUCTOR PROD. DIV.	5005 E MCDOWELL RD,PO BOX 20923	PHOENIX, AZ 85036
07263	FAIRCHILD SEMICONDUCTOR, A DIV. OF FAIRCHILD CAMERA AND INSTRUMENT CORP.	464 ELLIS STREET	MOUNTAIN VIEW, CA 94042
07910	TELEDYNE SEMICONDUCTOR	12515 CHADRON AVE.	HAWTHORNE, CA 90250
09023	CORNELL-DUBILIER ELECTRONIC DIVISION FEDERAL PACIFIC ELECTRIC CO.	2652 DALRYMPLE ST.	SANFORD, NC 27330
11237	CTS KEENE, INC.	3230 RIVERSIDE AVE.	PASO ROBLES, CA 93446
18324	SIGNETICS CORP.	811 E. ARQUES	SUNNYVALE, CA 94086
27014	NATIONAL SEMICONDUCTOR CORP.	2900 SEMICONDUCTOR DR.	SANTA CLARA, CA 95051
27264	MOLEX PRODUCTS CO.	5224 KATRINE AVE.	DOWNERS GROVE, IL 60515
32997	BOURNS, INC., TRIMPOT PRODUCTS DIV.	1200 COLUMBIA AVE.	RIVERSIDE, CA 92507
56289	SPRAGUE ELECTRIC CO.		NORTH ADAMS, MA 01247
71400	BUSSMAN MFG., DIVISION OF MCGRAW-EDISON CO.	2536 W. UNIVERSITY ST.	ST. LOUIS, MO 63107
72982	ERIE TECHNOLOGICAL PRODUCTS, INC.	644 W. 12TH ST.	ERIE, PA 16512
75378	CTS KNIGHTS, INC.	400 REIMANN AVE.	SANDWICH, IL 60548
75915	LITTELFUSE, INC.	800 E. NORTHWEST HWY	DES PLAINES, IL 60016
80009	TEKTRONIX, INC.	P O BOX 500	BEAVERTON, OR 97077
91637	DALE ELECTRONICS, INC.	P. O. BOX 609	COLUMBUS, NE 68601

Ckt No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A10	670-5294-00			CKT BOARD ASSY:CONTROLLER BOARD	80009	670-5294-00
C0037	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C1011	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C1041	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C1094	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C1096	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C2019	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C2081	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C3031	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C3041	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C4011	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C4035	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C4091	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C5009	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C5034	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C5035	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C5069	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C5099	290-0177-00			CAP.,FXD,ELCTLT:1UF,20%,50V	56289	162D105X0050CD2
C5101	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C6016	283-0783-00			CAP.,FXD,MICA DI:10PF,5%,500V	09023	CD15ED100J
C6025	283-0067-00			CAP.,FXD,CER DI:0.001UF,10%,200V	72982	835-515B102K
C6051	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C6099	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C7045	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C7065	290-0209-00			CAP.,FXD,ELCTLT:50UF,+75-10%,25V	56289	30D688
C7081	290-0177-00			CAP.,FXD,ELCTLT:1UF,20%,50V	56289	162D105X0050CD2
C7083	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C8010	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C8014	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C8028	290-0209-00			CAP.,FXD,ELCTLT:50UF,+75-10%,25V	56289	30D688
CR8015	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	07910	1N4152
CR8016	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	07910	1N4152
CR8018	152-0168-00			SEMICOND DEVICE:ZENER,0.4W,12V,5%	04713	1N963B
Q7082	151-0302-00			TRANSISTOR:SILICON,NPN	04713	2N2222A
Q8011	151-0302-00			TRANSISTOR:SILICON,NPN	04713	2N2222A
R0031	315-0562-00			RES.,FXD,CMPSN:5.6K OHM,5%,0.25W	01121	CB5625
R0032	315-0562-00			RES.,FXD,CMPSN:5.6K OHM,5%,0.25W	01121	CB5625
R0033	315-0562-00			RES.,FXD,CMPSN:5.6K OHM,5%,0.25W	01121	CB5625
R0034	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
R0035	315-0562-00			RES.,FXD,CMPSN:5.6K OHM,5%,0.25W	01121	CB5625
R0036	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	01121	CB2025
R0101	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
R0102	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
R0103	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
R0104	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
R1035	307-0541-00			RES,NTWK,THK FI:(7)1K OHM,10%,1W	91637	CSP08G01102G
R1055	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
R1093	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
R1095	307-0541-00			RES,NTWK,THK FI:(7)1K OHM,10%,1W	91637	CSP08G01102G
R2068	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
R2072	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025

Ckt No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
R2075	307-0541-00			RES,NTWK,THK FI:(7)1K OHM,10%,1W	91637	CSP08G01102G
R3081	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
R4015	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
R4045	307-0541-00			RES,NTWK,THK FI:(7)1K OHM,10%,1W	91637	CSP08G01102G
R4065	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
R4092	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
R5015	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
R6014	315-0821-00			RES.,FXD,CMPSN:820 OHM,5%,0.25W	01121	CB8215
R6015	315-0821-00			RES.,FXD,CMPSN:820 OHM,5%,0.25W	01121	CB8215
R6056	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
R6065	315-0682-00			RES.,FXD,CMPSN:6.8K OHM,5%,0.25W	01121	CB6825
R7029	307-0594-00			RES.,NTWK,FXD FI:7,220 OHM,2%,1.0W	32997	4308R-101-221
R7034	307-0598-00			RES.,NTWK,FXD FI:7,330 OHM,2%,1.0W	32997	4308R-101-221
R7071	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
R7072	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
R7083	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
R7084	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
R7094	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
R7095	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
R8012	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
R8013	303-0751-00			RES.,FXD,CMPSN:750 OHM,5%,1W	01121	GB7515
R8017	315-0201-00			RES.,FXD,CMPSN:200 OHM,5%,0.25W	01121	CB2015
R8019	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
R8035	307-0541-00			RES,NTWK,THK FI:(7)1K OHM,10%,1W	91637	CSP08G01102G
R8079	307-0541-00			RES,NTWK,THK FI:(7)1K OHM,10%,1W	91637	CSP08G01102G
R8085	307-0541-00			RES,NTWK,THK FI:(7)1K OHM,10%,1W	91637	CSP08G01102G
S4101	118-0321-00			SWITCH,SLIDE:5 SPST,50M AMP,24V	11237	206-5
U1010	156-0186-00			MICROCIRCUIT,DI:QUAD 2-INPUT NAND GATE	01295	SN7403N
U1020	156-0186-00			MICROCIRCUIT,DI:QUAD 2-INPUT NAND GATE	01295	SN7403N
U1030	156-0186-00			MICROCIRCUIT,DI:QUAD 2-INPUT NAND GATE	01295	SN7403N
U1040	156-0186-00			MICROCIRCUIT,DI:QUAD 2-INPUT NAND GATE	01295	SN7403N
U1050	156-0117-00			MICROCIRCUIT,DI:SYNC 4-BIT BINARY COUNTER	01295	SN74161N
U1060	156-0117-00			MICROCIRCUIT,DI:SYNC 4-BIT BINARY COUNTER	01295	SN74161N
U1070	160-0025-00			MICROCIRCUIT,DI:BIPOLAR 512 X 8 PROM,PROGRAM	80009	160-0025-00
U1080	160-0029-00			MICROCIRCUIT,DI:BIPOLAR 512 X 8 PROM,PROGRAM	80009	160-0029-00
U2010	156-0186-00			MICROCIRCUIT,DI:QUAD 2-INPUT NAND GATE	01295	SN7403N
U2020	156-0186-00			MICROCIRCUIT,DI:QUAD 2-INPUT NAND GATE	01295	SN7403N
U2030	156-0058-00			MICROCIRCUIT,DI:HEX.INVERTER	01295	SN7404N
U2040	156-0186-00			MICROCIRCUIT,DI:QUAD 2-INPUT NAND GATE	01295	SN7403N
U2050	156-0186-00			MICROCIRCUIT,DI:QUAD 2-INPUT NAND GATE	01295	SN7403N
U2070	156-0222-00			MICROCIRCUIT,DI:HEX.LATCH	01295	SN74174N
U2080	156-0222-00			MICROCIRCUIT,DI:HEX.LATCH	01295	SN74174N
U2090	156-0222-00			MICROCIRCUIT,DI:HEX.LATCH	01295	SN74174N
U3020	156-0129-00			MICROCIRCUIT,DI:QUAD 2-INPUT GATE	01295	SN7408N
U3050	156-0351-00			MICROCIRCUIT,DI:ARITHMETIC LOGIC UNIT	01295	SN74181PC
U3060	156-0351-00			MICROCIRCUIT,DI:ARITHMETIC LOGIC UNIT	01295	SN74181PC
U3070	156-0521-00			MICROCIRCUIT,DI:DUAL 4-BIT LATCH 9308,TTL	07263	9308PC
U3090	156-0058-00			MICROCIRCUIT,DI:HEX.INVERTER	01295	SN7404N
U3100	156-0541-00			MICROCIRCUIT,DI:DECODER/DEMULTIPLEXER	27014	DM74LS139N

Ckt No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
U4010	156-1015-00			MICROCIRCUIT,DI:DUAL J-K EDGETRIG FF	80009	156-1015-00
U4020	156-1015-00			MICROCIRCUIT,DI:DUAL J-K EDGETRIG FF	80009	156-1015-00
U4030	156-0058-00			MICROCIRCUIT,DI:HEX.INVERTER	01295	SN7404N
U4040	156-0061-00			MICROCIRCUIT,DI:SGL,BCD TO DEC DECODER	01295	SN7442N
U4050	156-0199-00			MICROCIRCUIT,DI:64 BIT RAM	18324	N82S25B
U4060	156-0199-00			MICROCIRCUIT,DI:64 BIT RAM	18324	N82S25B
U4070	156-0040-00			MICROCIRCUIT,DI:QUAD LATCH,TTL	80009	156-0040-00
U4080	156-0040-00			MICROCIRCUIT,DI:QUAD LATCH,TTL	80009	156-0040-00
U4090	156-0075-00			MICROCIRCUIT,DI:SGL 8-BIT DATA SEL MUX	80009	156-0075-00
U5010	156-1015-00			MICROCIRCUIT,DI:DUAL J-K EDGETRIG FF	80009	156-1015-00
U5020	156-1015-00			MICROCIRCUIT,DI:DUAL J-K EDGETRIG FF	80009	156-1015-00
U5030	156-1015-00			MICROCIRCUIT,DI:DUAL J-K EDGETRIG FF	80009	156-1015-00
U5040	156-0058-00			MICROCIRCUIT,DI:HEX.INVERTER	01295	SN7404N
U5050	156-0304-00			MICROCIRCUIT,DI:DUAL 4-INPUT,NAND GATE	18324	N74S20A
U5060	156-0030-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND GATE	01295	SN7400N
U5070	156-0058-00			MICROCIRCUIT,DI:HEX.INVERTER	01295	SN7404N
U5080	156-0035-00			MICROCIRCUIT,DI:SGL 8-INPUT POS NAND GATE	80009	156-0035-00
U5090	156-0047-00			MICROCIRCUIT,DI:TPL 3-INPUT POS NAND GATE	80009	156-0047-00
U5100	156-0541-00			MICROCIRCUIT,DI:DECODER/DEMULTIPLEXER	27014	DM74LS139N
U6010	156-0323-00			MICROCIRCUIT,DI:HEX. INVERTER	01295	SN74S04N
U6020	156-0485-00			MICROCIRCUIT,DI:1024 BIT STATIC SR 2533V	18324	2533V
U6030	156-0058-00			MICROCIRCUIT,DI:HEX.INVERTER	01295	SN7404N
U6040	156-0218-00			MICROCIRCUIT,DI:8-BIT ADDRESSABLE LATCH	07263	9334PC
U6050	156-0218-00			MICROCIRCUIT,DI:8-BIT ADDRESSABLE LATCH	07263	9334PC
U6060	156-0462-00			MICROCIRCUIT,LI:HEX SCHMITT TRIG,TTL	80009	156-0462-00
U6070	156-0043-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NOR GATE	80009	156-0043-00
U6080	156-0218-00			MICROCIRCUIT,DI:8-BIT ADDRESSABLE LATCH	07263	9334PC
U6090	156-0218-00			MICROCIRCUIT,DI:8-BIT ADDRESSABLE LATCH	07263	9334PC
U6100	156-0058-00			MICROCIRCUIT,DI:HEX.INVERTER	01295	SN7404N
U7010	156-0117-00			MICROCIRCUIT,DI:SYNC 4-BIT BINARY COUNTER	01295	SN74161N
U7020	156-0521-00			MICROCIRCUIT,DI:DUAL 4-BIT LATCH 9308,TTL	07263	9308PC
U7040	156-0145-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND BFR	01295	SN7438N
U7050	156-0145-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND BFR	01295	SN7438N
U7060	156-0145-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND BFR	01295	SN7438N
U7070	156-0145-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND BFR	01295	SN7438N
U7080	156-0145-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND BFR	01295	SN7438N
U7090	156-0145-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND BFR	01295	SN7438N
U7100	156-0129-00			MICROCIRCUIT,DI:QUAD 2-INPUT GATE	01295	SN7408N
U8100	156-1015-00			MICROCIRCUIT,DI:DUAL J-K EDGETRIG FF	80009	156-1015-00
Y7011	158-0154-00			XTAL UNIT,QTZ:20MHZ,0.015%,PARALLEL	75378	MP 200

CHASSIS

B1	119-0721-00			FAN,VENTILATING:75 CFM,7W,115VAC,50/60 HZ	80009	119-0721-00
B2	119-0721-00			FAN,VENTILATING:75 CFM,7W,115VAC,50/60 HZ	80009	119-0721-00
F1	159-0017-00			FUSE,CARTRIDGE:3AG,4A,250V,FAST-BLOW	71400	MTH4
F2	159-0017-00			FUSE,CARTRIDGE:3AG,4A,250V,FAST-BLOW	71400	MTH4
F3	159-0029-00	B010100	B010230	FUSE,CARTRIDGE:3AG,0.3A,250V,20 SEC	75915	313.300
F3	159-0126-00	B010231		FUSE,CARTRIDGE:3AG,2.5A,250V,0.65 SEC	71400	AGC2-1/2
F4	159-0126-00			FUSE,CARTRIDGE:3AG,2.5A,250V,0.65 SEC	71400	AGC2-1/2
S1	260-1842-00			SWITCH,ROCKER,DPST,16A,250VAC	04009	2600-11E

Section 6
DIAGRAMS

Symbols and Reference Designators

Graphic symbols for electrical and logic symbols, used on the diagrams, are based on ANSI Y32.2, 1975, and ANSI Y32.14, 1973, "American National Standards Institute." Logic symbols depict the logic function of the device in positive logic. Copies of these standards can be obtained from the Institute of Electrical and Electronics Engineers, 345 East 47th Street, New York, N.Y., 11017. Exceptions and additions are shown on this sample diagram. These conform or are based on the manufacturers data sheet and industry trends.

Resistor values are in ohms, unless noted otherwise, and the Ω symbol is omitted. Capacitor values ≤ 1 (e.g. 10) are in picofarads (pF) and values < 1 (e.g. 0.01) are in microfarads unless otherwise noted.

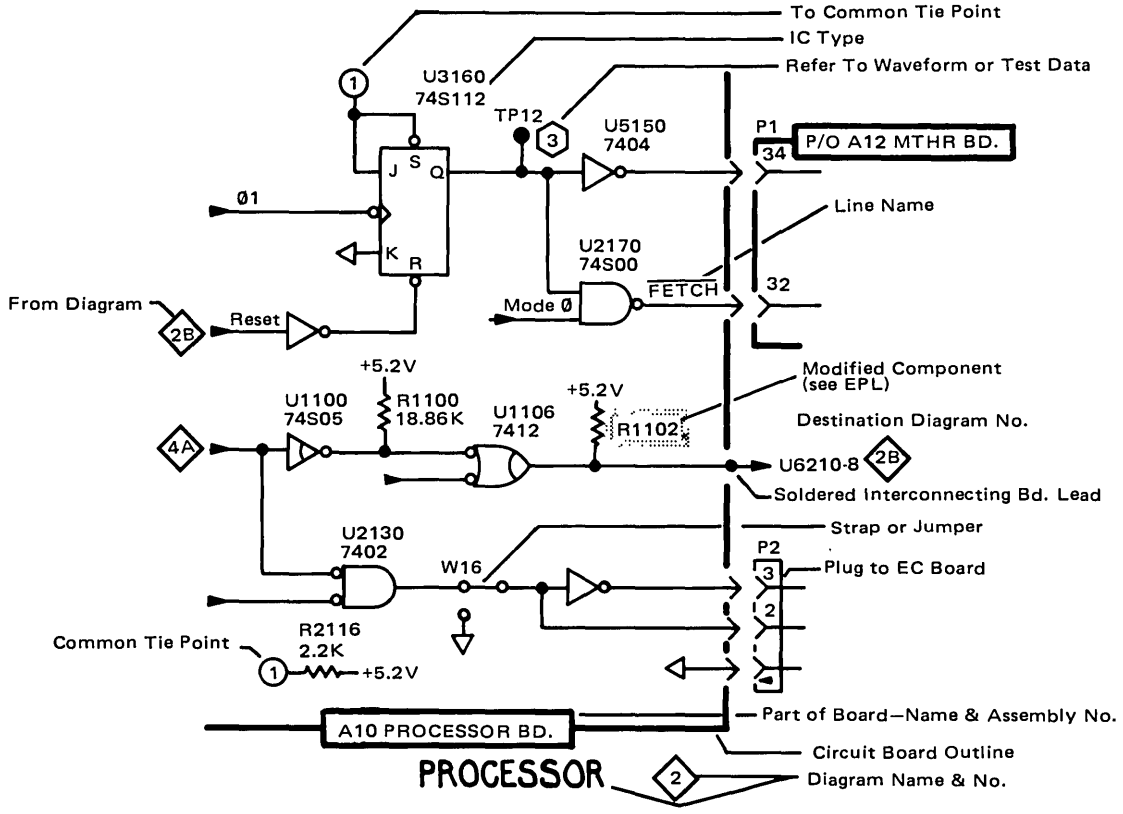
Component Circuit Numbers

Circuit numbers for the components (resistors, IC's, etc.) on the μProcessor Lab modules (boards) are assigned according to their physical location. Some circuit boards have a grid of alphanumeric notation screened or etched on the board. The letters denote row (horizontal) position, the numerals column (vertical) position. Circuit numbers for the schematics or other documentation convert the alpha notation to a number. The letter A converts to 1, B to 2, etc. All component circuit numbers can be found in the Replaceable Electrical Parts List under the assembly number. The schematic assembly number is located in the bottom center of the schematic.

The following prefix letters are used as reference designators to identify components or assembles on the diagrams.

A	Assembly, separable or repairable circuit board, etc)	HY	Hybrid circuit	T	Transformer
C	Capacitor, fixed or variable	J	Connector, stationary portion	TC	Thermocouple
CR	Diode, signal or rectifier	K	Relay	TP	Test Point
DL	Delay line	L	Inductor, fixed or variable	U	Integrated circuit
DS	Indicating device (lamp)	P	Connector, movable portion	V	Electron tube
E	Spark Gap, Ferrite bead	Q	Transistor or silicon-controlled rectifier	VR	Voltage regulator (zener diode, etc.)
F	Fuse	R	Resistor, fixed or variable	W	Wirestrap or cable
FL	Filter	RT	Thermistor	Y	Crystal
H	Heat dissipating device (heat sink, heat radiator, etc.)	S	Switch or contactor	Z	Phase shifter

The following partial diagram illustrates special symbology and practices used on the diagrams with a description of the meaning.



CIRCUIT NUMBER ASSIGNMENT GUIDE

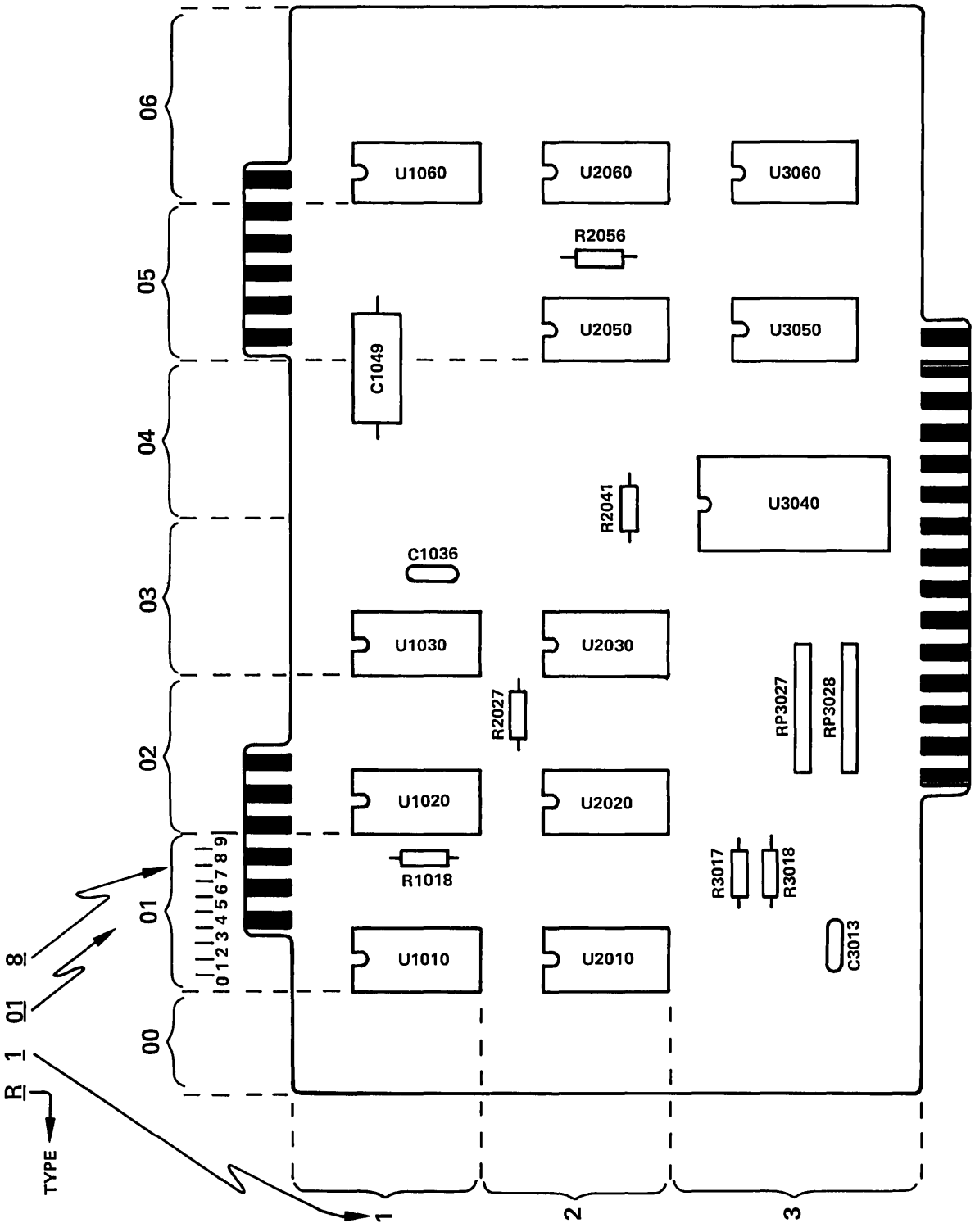
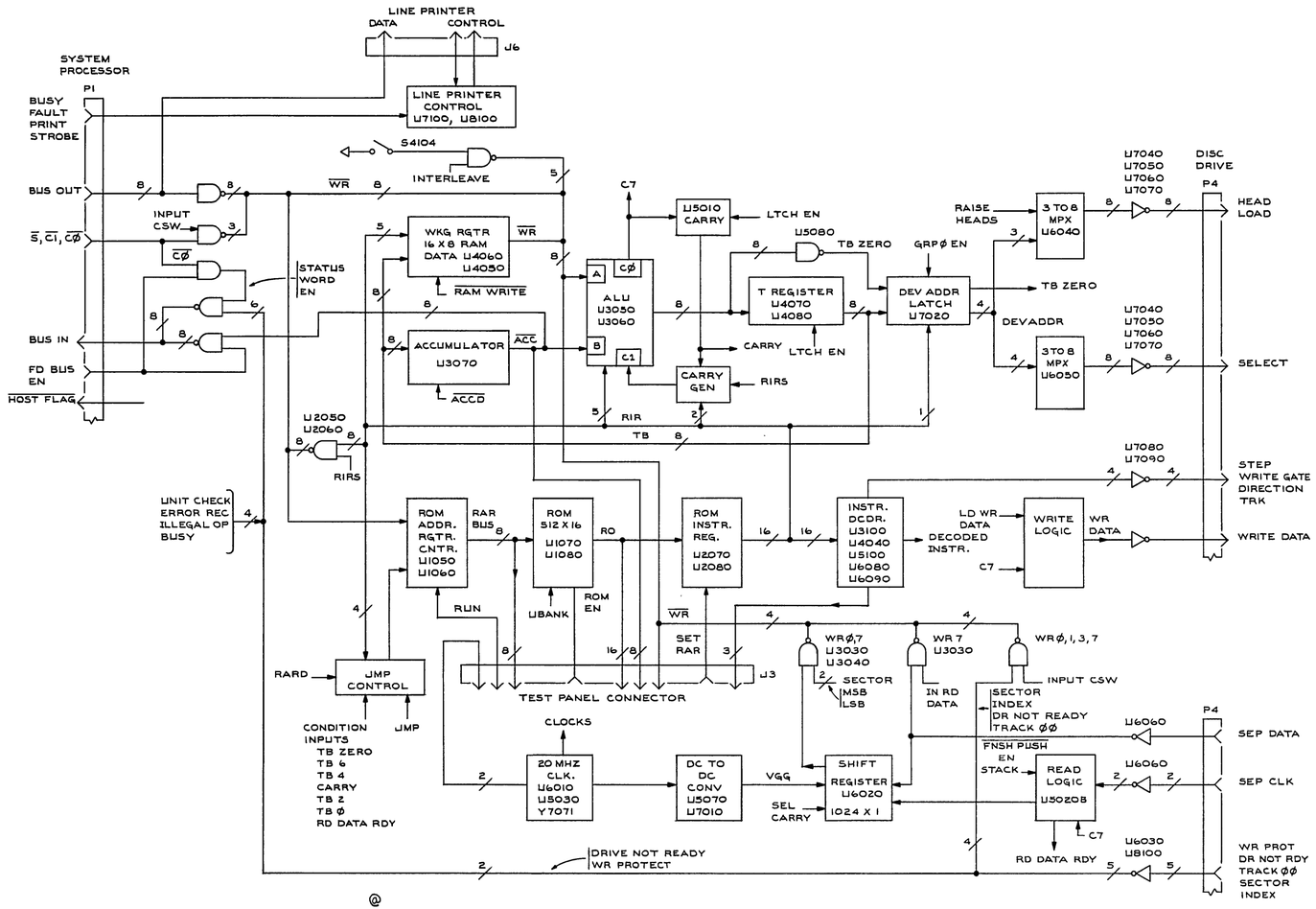


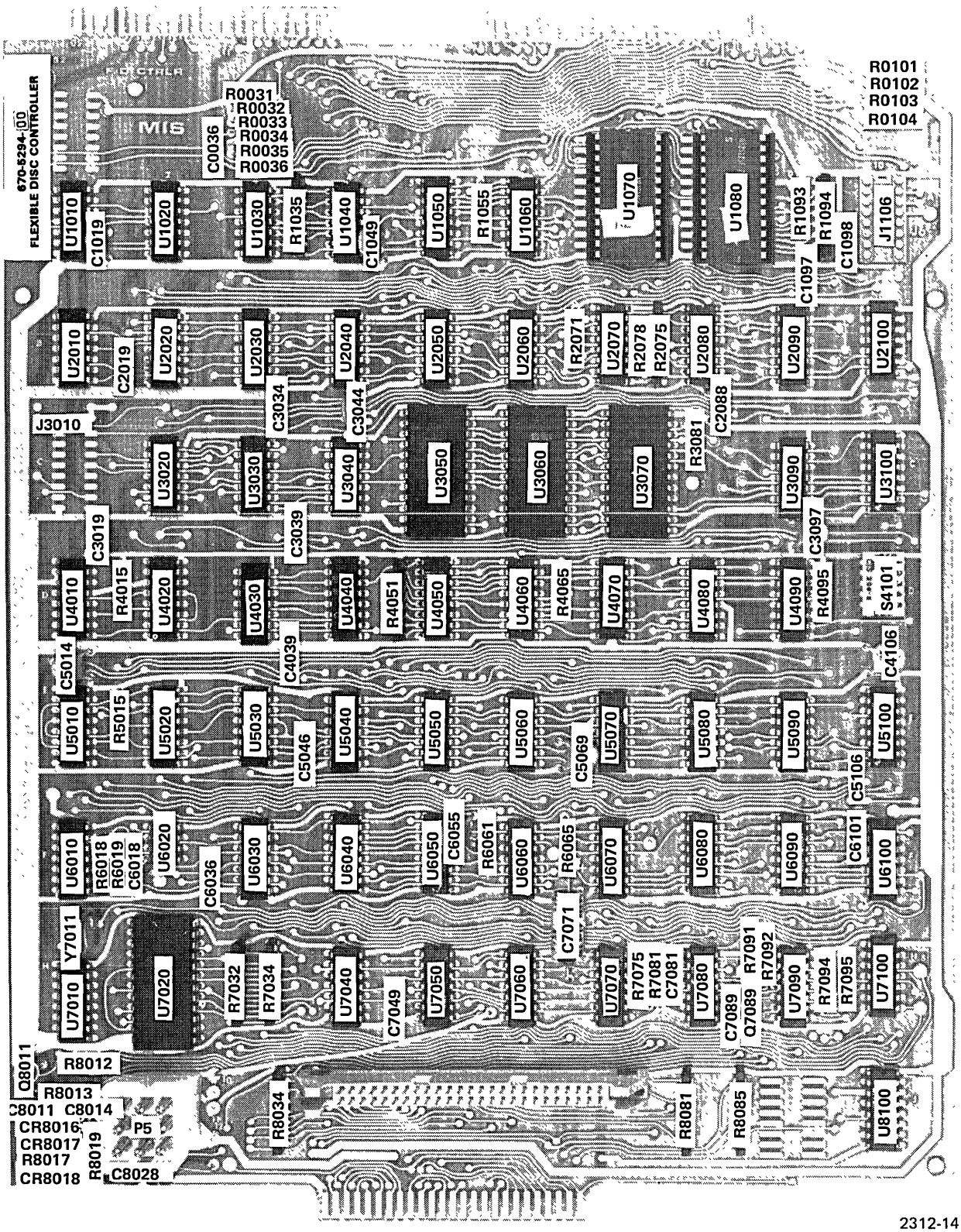
TABLE 6-1
VCC/GND Pinout of IC Types For 8002A Flexible Disc Unit

Type	VCC	GND
2533	8	4
7400	14	7
7402 (S)	14	7
7403	14	7
7404	14	7
7408	14	7
7410	14	7
7414	14	7
7438	14	7
7442	16	8
7475	5	12
74S20	14	7
74109	16	8
74116	24	12
74151A	16	8
74161	16	8
74174	16	8
74181	24	12
74LS139	16	8
82S25	16	8
82S115	24	12
9334	16	8



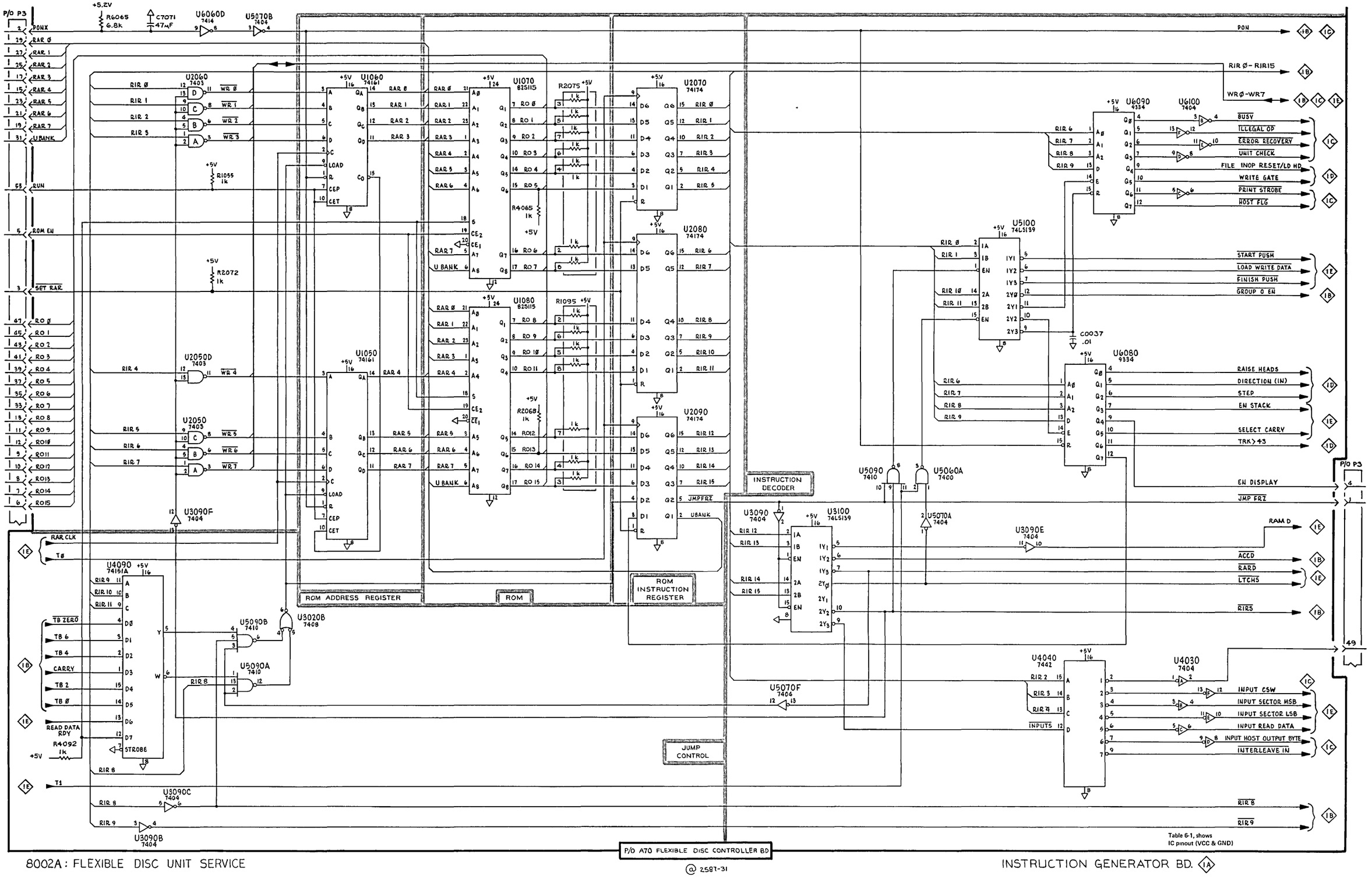
2687-30

FIG. 3-1. FLEXIBLE DISC CONTROLLER FUNCTIONAL BLOCK DIAGRAM



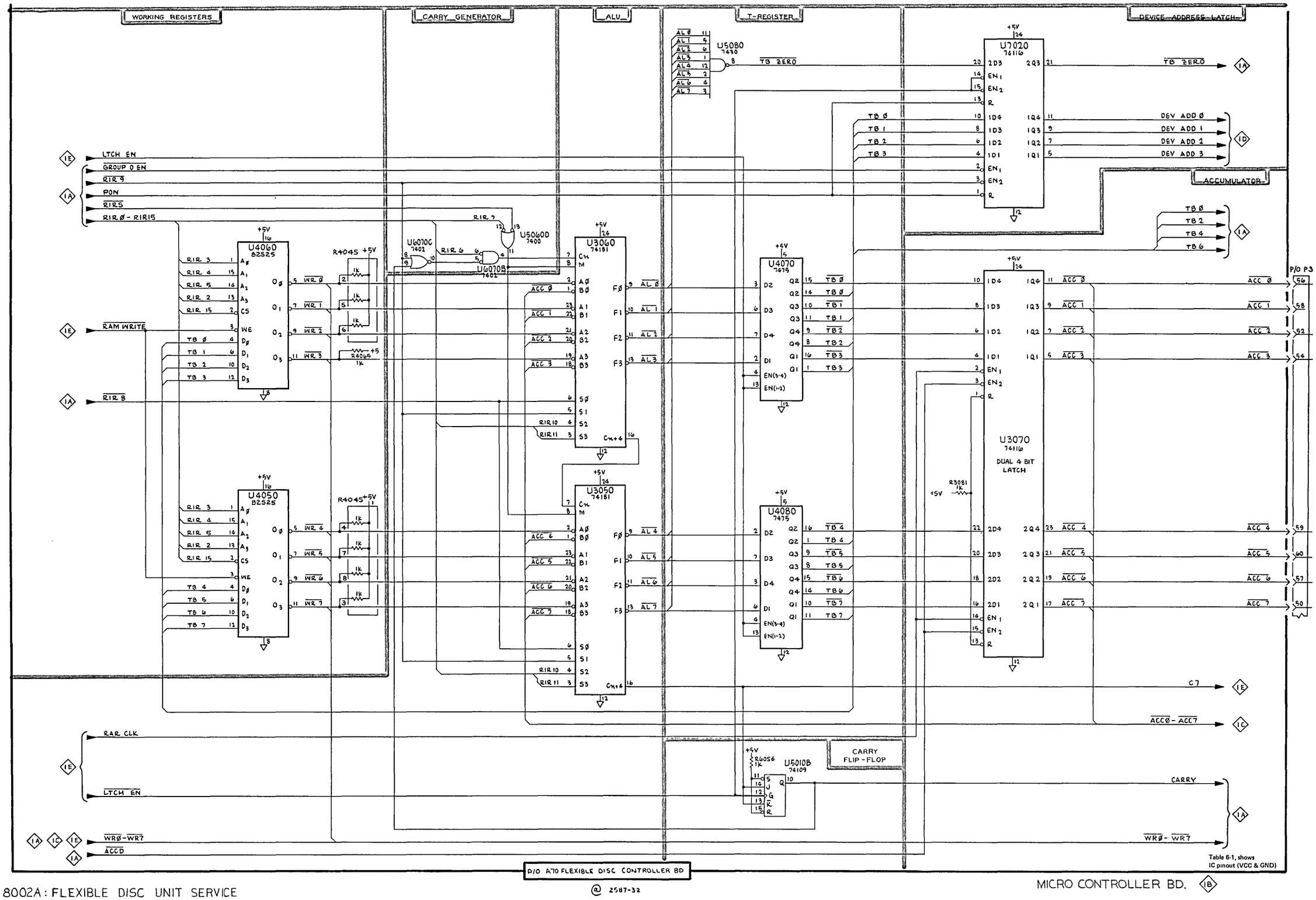
2312-14

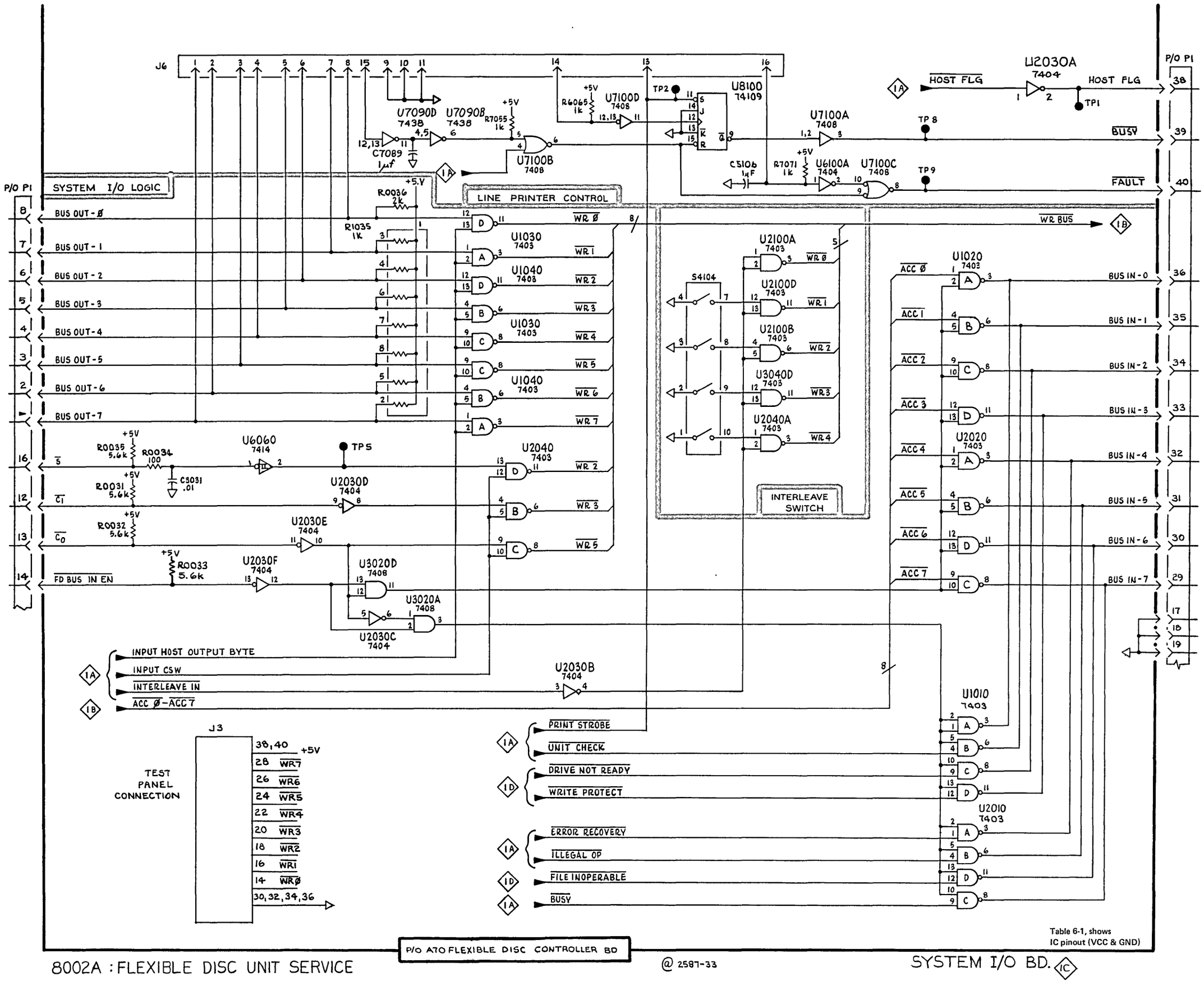
A70 Flexible Disc Controller



8002A: FLEXIBLE DISC UNIT SERVICE

INSTRUCTION GENERATOR BD. 1A

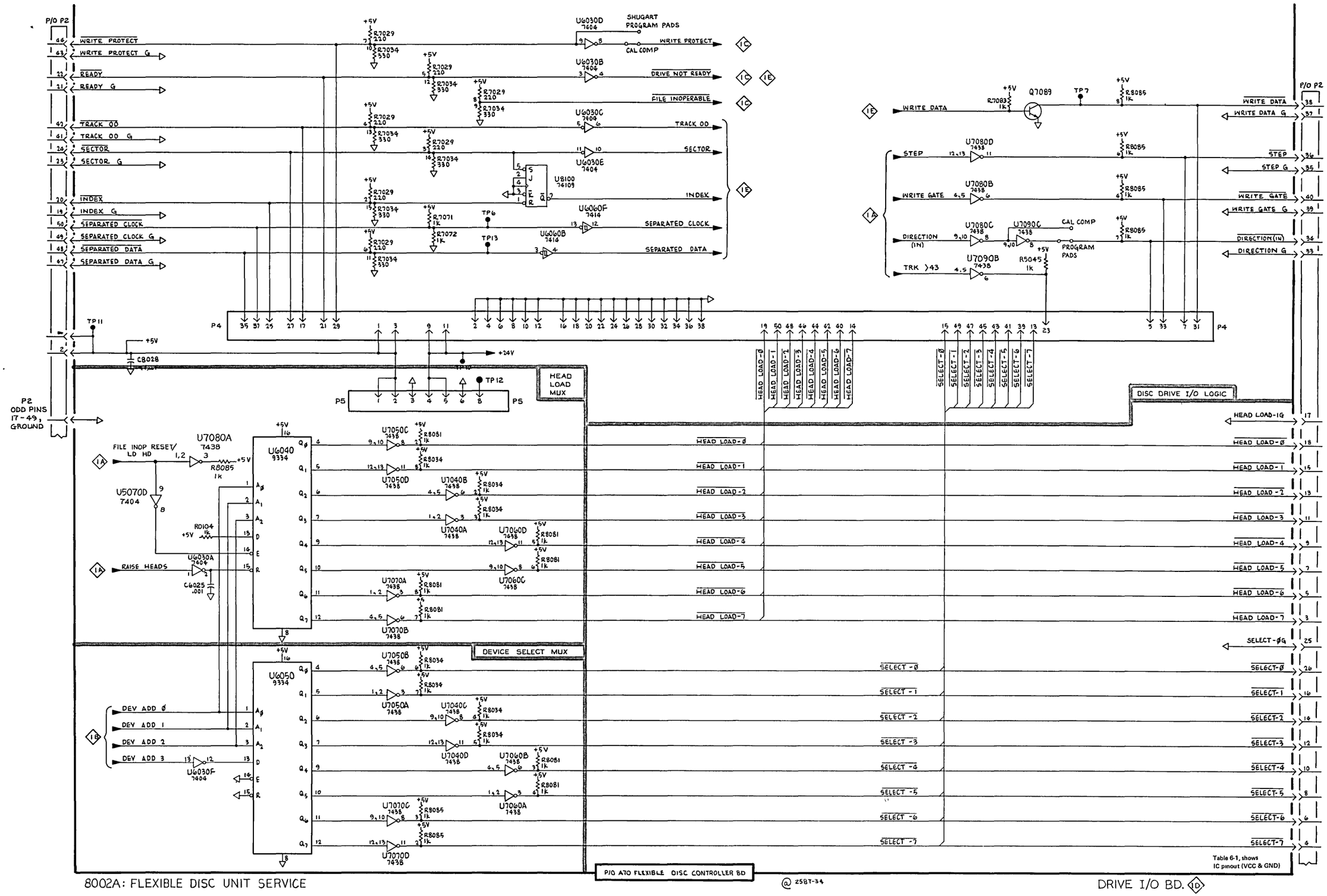

WORKING REGISTERS
CARRY GENERATOR
ALU
T-REGISTER
DEVICE ADDRESS LATCH
ACCUMULATOR
U4060 82S25
U4050 82S25
U3060 74181
U3050 74181
U3070 74116 DUAL 4 BIT LATCH
U7020 74116
U4070 7475
U4080 7475
U5080 7430
U6070C 7402
U6070B 7402
U5060D 7400
U5010B 74109
CARRY FLIP-FLOP
R4045 1k
R4065 1k
R4056 1k
R3081 1k
LTCH EN
GROUP 0 EN
R1R 9
PON
R1R5
R1R0 - R1R15
RAM WRITE
R1R 8
R1R 7
R1R 6
RAR CLK
LTCH EN
WR0-WR7
ACC0
TB ZERO
DEV ADD 0
DEV ADD 1
DEV ADD 2
DEV ADD 3
TB 0
TB 2
TB 4
TB 6
ACC 0
ACC 1
ACC 2
ACC 3
ACC 4
ACC 5
ACC 6
ACC 7
C7
ACC0 - ACC7
CARRY
WR0 - WR7
P/O P3
P/O A70 FLEXIBLE DISC CONTROLLER BD
@ 2587-32
Table 6-1, shows IC pinout (VCC & GND)
8002A: FLEXIBLE DISC UNIT SERVICE
MICRO CONTROLLER BD. 1B



8002A : FLEXIBLE DISC UNIT SERVICE

@ 2587-33

SYSTEM I/O BD. (1C)


P/O P2
WRITE PROTECT
WRITE PROTECT G
READY
READY G
TRACK 00
TRACK 00 G
SECTOR
SECTOR G
INDEX
INDEX G
SEPARATED CLOCK
SEPARATED CLOCK G
SEPARATED DATA
SEPARATED DATA G
SHUGART PROGRAM PADS
CAL COMP
DRIVE NOT READY
FILE INOPERABLE
U6030D 7404
U6030B 7404
U6030C 7404
U6030E 7404
U8100 74109
U6060F 7414
U6060B 7416
TP6
TP13
TP11
TP12
+5V
+24V
C8028
P4
P5
P2 ODD PINS 17-49, GROUND
HEAD LOAD MUX
DISC DRIVE I/O LOGIC
HEAD LOAD-0
HEAD LOAD-1
HEAD LOAD-2
HEAD LOAD-3
HEAD LOAD-4
HEAD LOAD-5
HEAD LOAD-6
HEAD LOAD-7
SELECT-0
SELECT-1
SELECT-2
SELECT-3
SELECT-4
SELECT-5
SELECT-6
SELECT-7
FILE INOP RESET/ LD HD
U7080A 7438
U5070D 7404
U6040 9334
RAISE HEADS
U6030A 7404
C6025 .001
R8085 1K
R0104 1K
U7050C
U7050D
U7040B
U7040A
U7060D
U7060C
U7070A
U7070B
DEVICE SELECT MUX
DEV ADD 0
DEV ADD 1
DEV ADD 2
DEV ADD 3
U6030F 7404
U6050 9334
U7050B
U7050A
U7040C
U7040D
U7060B
U7060A
U7070C
U7070D
WRITE DATA
Q7089
R7083 1K
STEP
WRITE GATE
DIRECTION (IN)
TRK >43
U7080D 7438
U7080B 7438
U7080C 7438
U7090C 7438
U7090B 7438
R5045 1K
PROGRAM PADS
WRITE DATA G
STEP G
WRITE GATE G
DIRECTION(IN)
DIRECTION G
SELECT-0G
P/O A70 FLEXIBLE DISC CONTROLLER BD
Table 6-1, shows IC pinout (VCC & GND)

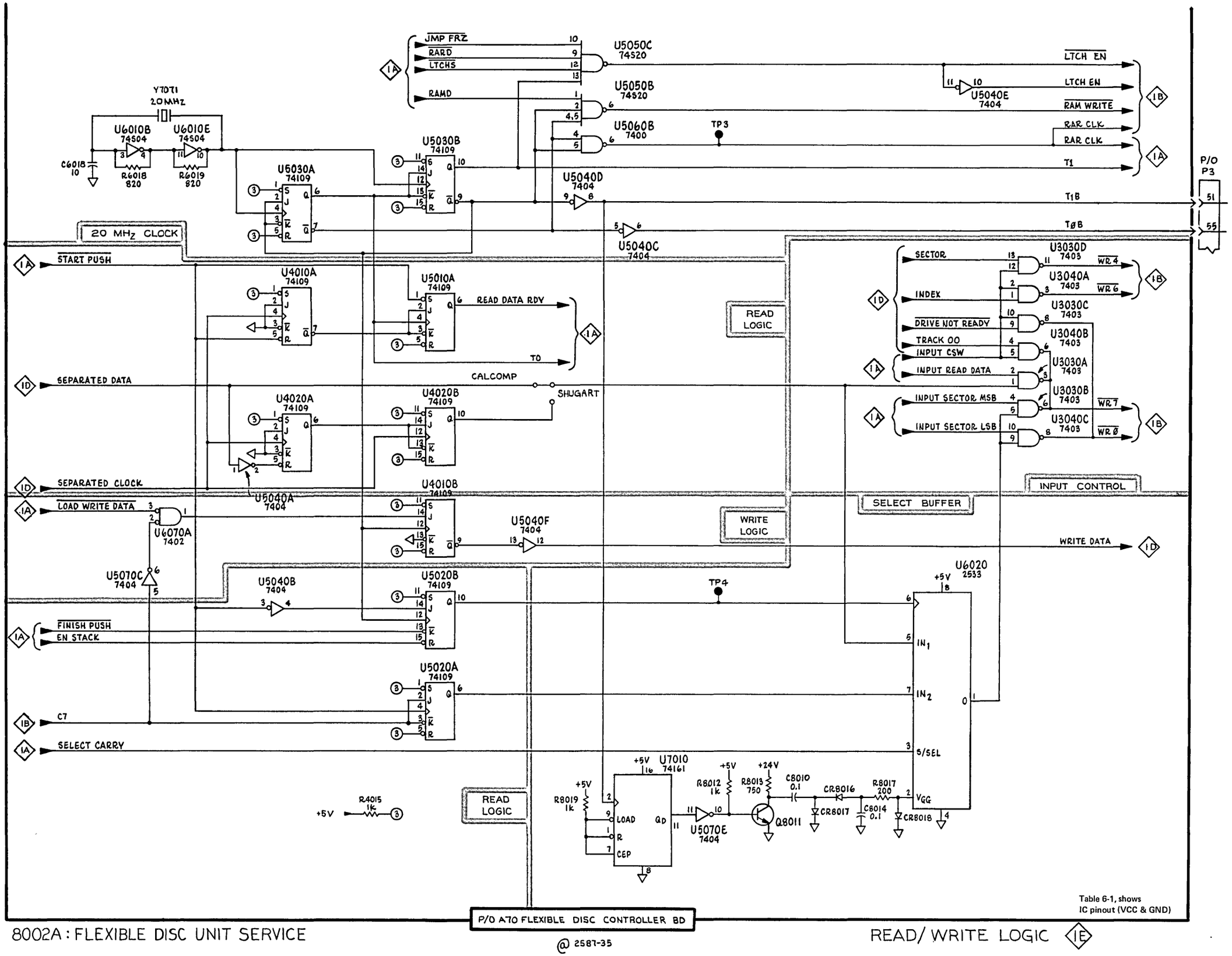
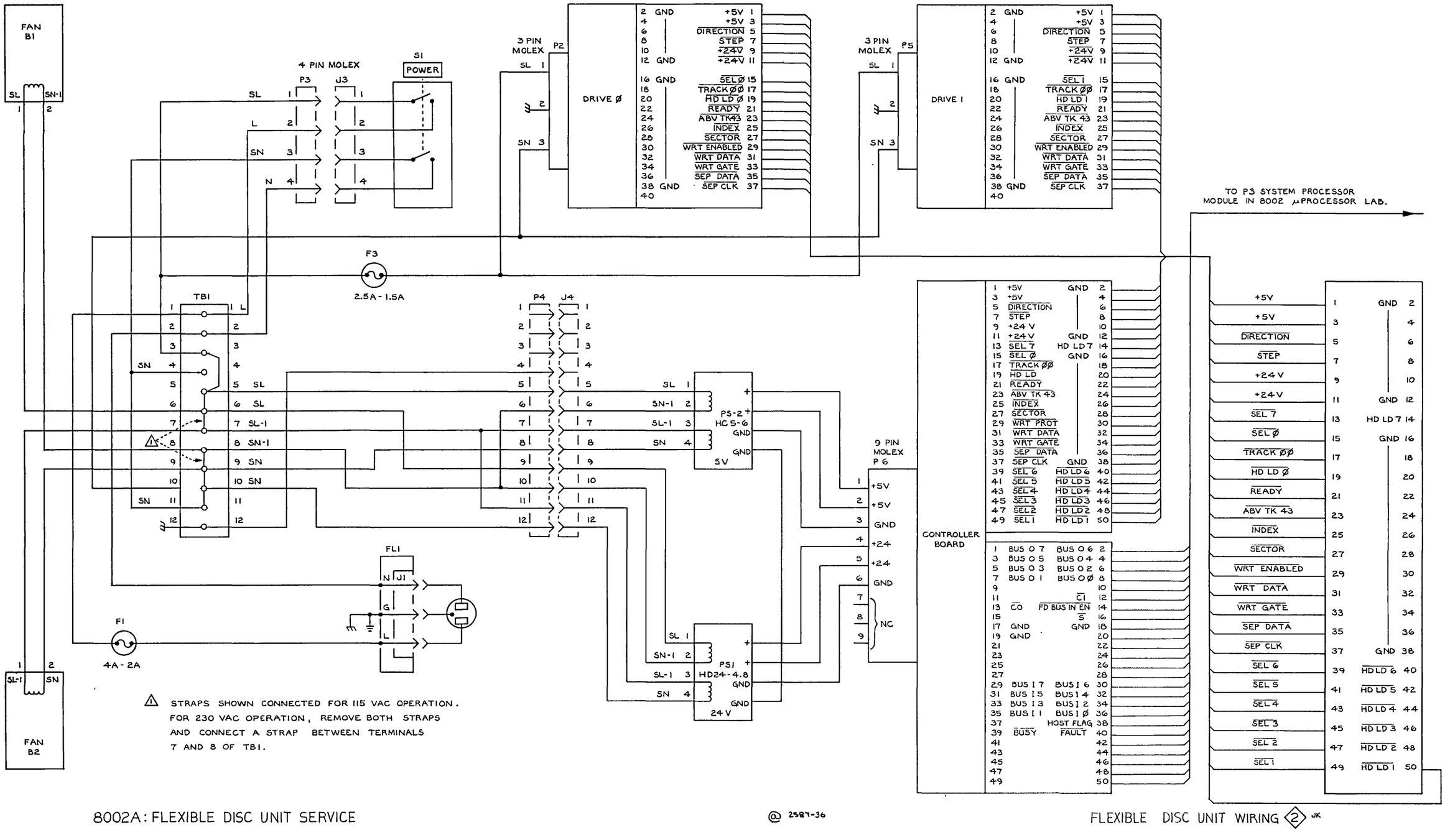
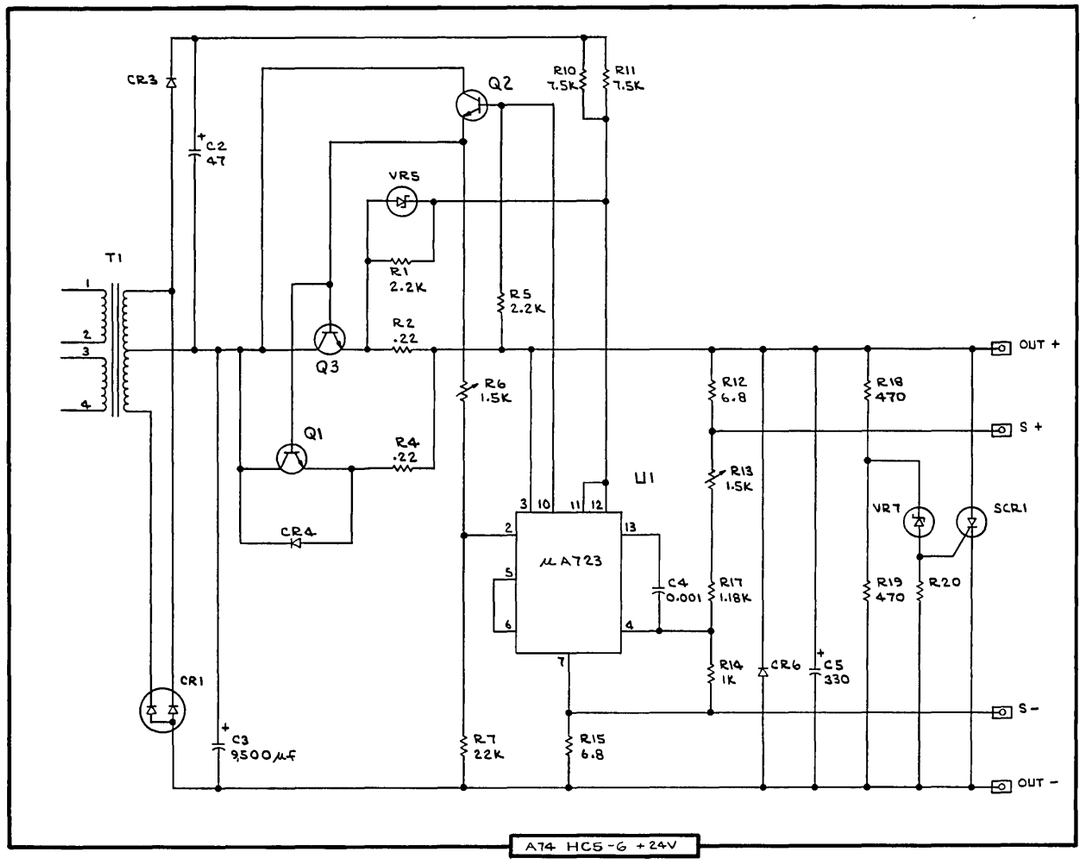


Table 6-1, shows IC pinout (VCC & GND)

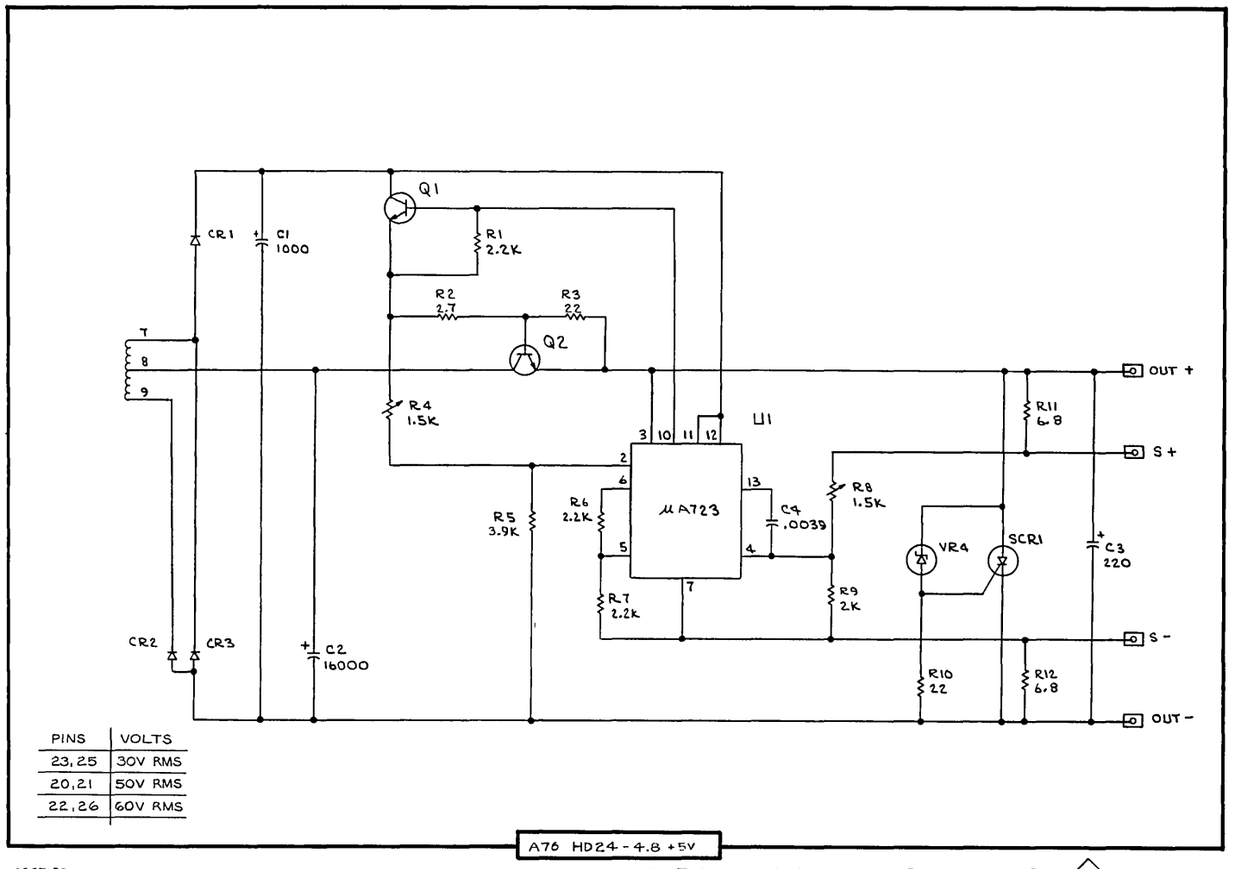


8002A: FLEXIBLE DISC UNIT SERVICE

FLEXIBLE DISC UNIT WIRING ◇2◇ JK



A74 HC5-6 +24V



PINS	VOLTS
23,25	30V RMS
20,21	50V RMS
22,26	60V RMS

A76 HD24-4.8 +5V

Section 7
REPLACEABLE MECHANICAL PARTS

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

SPECIAL NOTES AND SYMBOLS

X000	Part first added at this serial number
00X	Part removed after this serial number

FIGURE AND INDEX NUMBERS

Items in this section are referenced by figure and index numbers to the illustrations.

INDENTATION SYSTEM

This mechanical parts list is indented to indicate item relationships. Following is an example of the indentation system used in the description column.

```
1 2 3 4 5                    Name & Description

Assembly and/or Component
Attaching parts for Assembly and/or Component
                - - - * - - -
  Detail Part of Assembly and/or Component
  Attaching parts for Detail Part
                - - - * - - -
    Parts of Detail Part
    Attaching parts for Parts of Detail Part
                - - - * - - -
```

Attaching Parts always appear in the same indentation as the item it mounts, while the detail parts are indented to the right. Indented items are part of, and included with, the next higher indentation. The separation symbol - - - * - - - indicates the end of attaching parts.

Attaching parts must be purchased separately, unless otherwise specified.

ITEM NAME

In the Parts List, an Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

ABBREVIATIONS

"	INCH
#	NUMBER SIZE
ACTR	ACTUATOR
ADPTR	ADAPTER
ALIGN	ALIGNMENT
AL	ALUMINUM
ASSEM	ASSEMBLED
ASSY	ASSEMBLY
ATTEN	ATTENUATOR
AWG	AMERICAN WIRE GAGE
BD	BOARD
BRKT	BRACKET
BRS	BRASS
BRZ	BRONZE
BSHG	BUSHING
CAB	CABINET
CAP	CAPACITOR
CER	CERAMIC
CHAS	CHASSIS
CKT	CIRCUIT
COMP	COMPOSITION
CONN	CONNECTOR
COV	COVER
CPLG	COUPLING
CRT	CATHODE RAY TUBE
DEG	DEGREE
DWR	DRAWER
ELCTRN	ELECTRON
ELEC	ELECTRICAL
ELCTLT	ELECTROLYTIC
ELEM	ELEMENT
EPL	ELECTRICAL PARTS LIST
EQPT	EQUIPMENT
EXT	EXTERNAL
FIL	FILLISTER HEAD
FLEX	FLEXIBLE
FLH	FLAT HEAD
FLTR	FILTER
FR	FRAME or FRONT
FSTNR	FASTENER
FT	FOOT
FXD	FIXED
GSKT	GASKET
HDL	HANDLE
HEX	HEXAGON
HEX HD	HEXAGONAL HEAD
HEX SOC	HEXAGONAL SOCKET
HLCPS	HELICAL COMPRESSION
HLEXT	HELICAL EXTENSION
HV	HIGH VOLTAGE
IC	INTEGRATED CIRCUIT
ID	INSIDE DIAMETER
IDENT	IDENTIFICATION
IMPLR	IMPELLER
IN	INCH
INCAND	INCANDESCENT
INSUL	INSULATOR
INTL	INTERNAL
LPHLDR	LAMPHOLDER
MACH	MACHINE
MECH	MECHANICAL
MTG	MOUNTING
NIP	NIPPLE
NON WIRE	NOT WIRE WOUND
OBD	ORDER BY DESCRIPTION
OD	OUTSIDE DIAMETER
OVH	OVAL HEAD
PH BRZ	PHOSPHOR BRONZE
PL	PLAIN or PLATE
PLSTC	PLASTIC
PN	PART NUMBER
PNH	PAN HEAD
PWR	POWER
RCPT	RECEPTACLE
RES	RESISTOR
RGD	RIGID
RLF	RELIEF
RTNR	RETAINER
SCH	SOCKET HEAD
SCOPE	OSCILLOSCOPE
SCR	SCREW
SE	SINGLE END
SECT	SECTION
SEMICOND	SEMICONDUCTOR
SHLD	SHIELD
SHLDR	SHOULDERED
SKT	SOCKET
SL	SLIDE
SLFLKG	SELF-LOCKING
SLVG	SLEEVING
SPR	SPRING
SQ	SQUARE
SST	STAINLESS STEEL
STL	STEEL
SW	SWITCH
T	TUBE
TERM	TERMINAL
THD	THREAD
THK	THICK
TNSN	TENSION
TPG	TAPPING
TRH	TRUSS HEAD
V	VOLTAGE
VAR	VARIABLE
W/	WITH
WSHR	WASHER
XFMR	TRANSFORMER
XSTR	TRANSISTOR

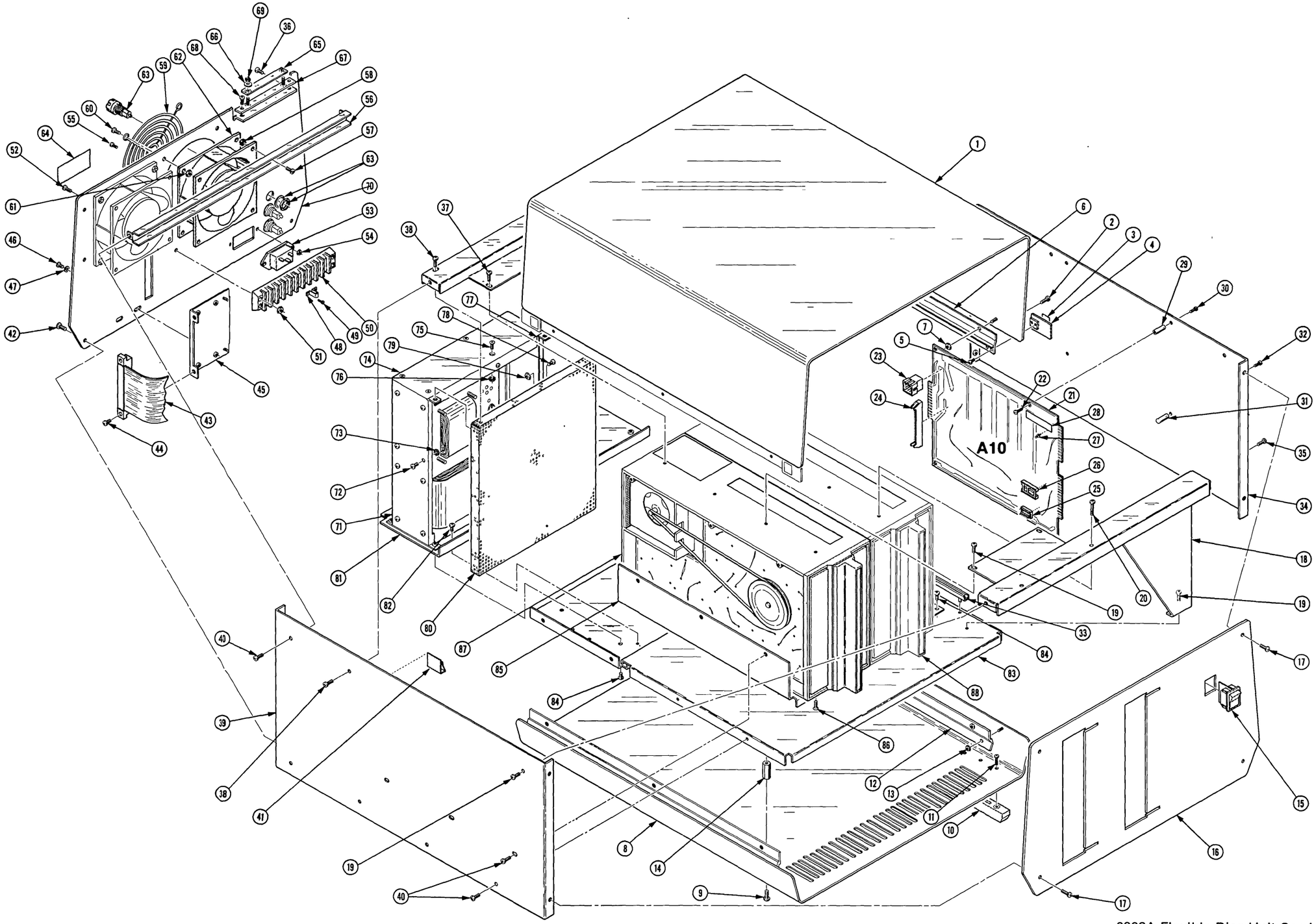
CROSS INDEX—MFR. CODE NUMBER TO MANUFACTURER

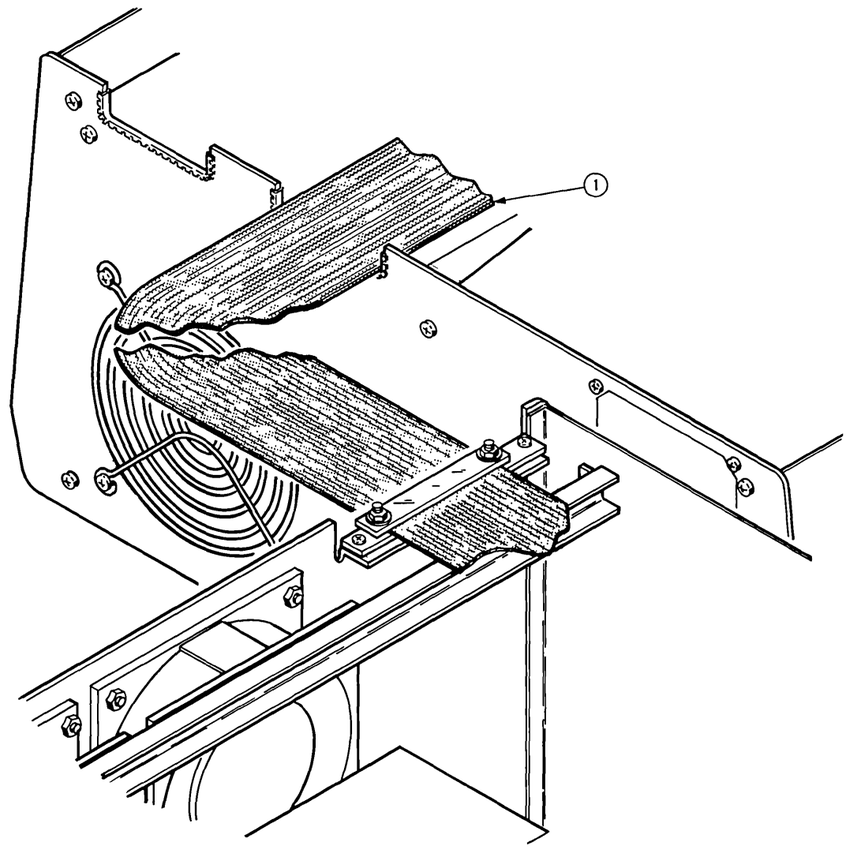
Mfr. Code	Manufacturer	Address	City, State, Zip
01295	TEXAS INSTRUMENTS, INC., SEMICONDUCTOR GROUP	P O BOX 5012, 13500 N CENTRAL EXPRESSWAY	DALLAS, TX 75222
02777	HOPKINS ENGINEERING COMPANY	12900 FOOTHILL BLVD.	SAN FERNANDO, CA 91342
04009	ARROW-HART, INC.	103 HAWTHORNE STREET	HARTFORD, CT 06106
05574	VIKING INDUSTRIES, INC.	21001 NORDHOFF STREET	CHATSWORTH, CA 91311
12327	FREEWAY CORPORATION	9301 ALLEN DRIVE	CLEVELAND, OH 44125
27264	MOLEX PRODUCTS CO.	5224 KATRINE AVE.	DOWNERS GROVE, IL 60515
73743	FISCHER SPECIAL MFG. CO.	446 MORGAN ST.	CINCINNATI, OH 45206
78189	ILLINOIS TOOL WORKS, INC. SHAKEPROOF DIVISION	ST. CHARLES ROAD	ELGIN, IL 60120
80009	TEKTRONIX, INC.	P O BOX 500	BEAVERTON, OR 97077
83385	CENTRAL SCREW CO.	2530 CRESCENT DR.	BROADVIEW, IL 60153

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
1-1	390-0584-00			1		CAB,TOP,MODULE:	80009	390-0584-00
						(ATTACHING PARTS)		
-2	212-0137-00			6		SCREW,MACHINE:8-32 X 0.375 L,RNH,STEEL	83385	OBD
						- - - * - - -		
-3	334-1555-00			4		PLATE,IDENT:TRADEMARK	80009	334-1555-00
-4	426-0928-00			4		FRAME,TRIM:GRAY PLASTIC	80009	426-0928-00
						(ATTACHING PARTS FOR EACH)		
-5	213-0088-00			1		SCR,TPG,THD CTG:4-24 X 0.25 INCH,PNH STL	83385	OBD
						- - - * - - -		
-6	426-1444-00			2		FRAME SECT,CAB:UPPER	80009	426-1444-00
						(ATTACHING PARTS FOR EACH)		
-7	210-0457-00			4		NUT,PLAIN,EXT W:6-32 X 0.312 INCH,STL	83385	OBD
						- - - * - - -		
-8	390-0582-00			1		CABINET,BOTTOM:	80009	390-0582-00
						(ATTACHING PARTS)		
-9	212-0008-00			4		SCREW,MACHINE:8-32 X 0.500 INCH,PNH STL	83385	OBD
						- - - * - - -		
-10	348-0128-01			4		FOOT,CABINET:POLYURETHANE,BLACK	80009	348-0128-01
						(ATTACHING PARTS FOR EACH)		
-11	212-0008-00			2		SCREW,MACHINE:8-32 X 0.500 INCH,PNH STL	83385	OBD
						- - - * - - -		
-12	426-1445-00			2		FRAME SECT,CAB:LOWER	80009	426-1445-00
						(ATTACHING PARTS FOR EACH)		
-13	210-0457-00			4		NUT,PLAIN,EXT W:6-32 X 0.312 INCH,STL	83385	OBD
						- - - * - - -		
-14	129-0663-00			2		SPACER POST:0.928 L,8-32 THD,AL,0.5 HEX	80009	129-0663-00
-15	260-1842-00			1		SWITCH,ROCKER:DPST,16A,250VAC	04009	2600-11E
-16	333-2345-00			1		PANEL,FRONT:	80009	333-2345-00
						(ATTACHING PARTS)		
-17	212-0137-00			4		SCREW,MACHINE:8-32 X 0.375 L,PNH STEEL	83385	OBD
						- - - * - - -		
-18	386-3791-00			1		STIFFENER,MDL:TOP,FRONT	80009	386-3791-00
						(ATTACHING PARTS)		
-19	212-0023-00			5		SCREW,MACHINE:8-32 X 0.375 INCH,PNH STL	83385	OBD
-20	212-0082-00			2		SCREW,MACHINE:8-32 X 1.250 INCH,PNH STL	83385	OBD
						- - - * - - -		
-21	----- -----			1		CKT BOARD ASSY:CONTROLLER BOARD(SEE A10 EPL)		
						(ATTACHING PARTS)		
-22	211-0008-00			2		SCREW,MACHINE:4-40 X 0.25 INCH,PNH STL	83385	OBD
						- - - * - - -		
	----- -----			-		. CKT BOARD ASSY INCLUDES:		
-23	131-2226-00			1		. CONN,PLUG,ELEC:9 CONTACT,FEMALE	27264	03-09-2091
-24	131-2229-00			1		. CONN,RCPT,ELEC:CKT BD,50 CONT,MALE	05574	5935
-25	131-2227-00			1		. TERM,FEED THRU:16 PIN,INSULATED	80009	131-2227-00
-26	136-0578-00			2		. SKT,PL-IN ELEK:MICROCIRCUIT,24 DIP,LOW PF	01295	5935
-27	118-0317-00			12		. TERMINAL PIN:	80009	118-0317-00
-28	334-3160-00			1		. MARKER,IDENT:MARKED FLEXIBLE DISC CONT	80009	334-3160-00
-29	361-0046-00			2		SPACER,POST:	80009	361-0046-00
						(ATTACHING PARTS FOR EACH)		
-30	211-0008-00			1		SCREW,MACHINE:4-40 X 0.25 INCH,PNH STL	83385	OBD
						- - - * - - -		
-31	361-0870-00			2		SPACER,CKT BD:0.531 L,W/4-40 THD ONE END	80009	361-0870-00
						(ATTACHING PARTS FOR EACH)		
-32	211-0008-00			1		SCREW,MACHINE:4-40 X 0.25 INCH,PNH STL	83385	OBD
						- - - * - - -		
-33	351-0574-00			1		GUIDE,KEYBOARD:LEFT 4016	80009	351-0574-00
-34	386-3796-00			1		PLATE,MODULE:RIGHT	80009	386-3796-00
						(ATTACHING PARTS)		
-35	212-0023-00			6		SCREW,MACHINE:8-32 X 0.375 INCH,PNH STL	83385	OBD
-36	212-0137-00			3		SCREW,MACHINE:8-32 X 0.375 L,PNH,STEEL	83385	OBD
						- - - * - - -		

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
1-37	386-3793-00			1		SPRT,PWR SUPPLY:	80009	386-3793-00
						(ATTACHING PARTS)		
-38	212-0023-00			5		SCREW,MACHINE:8-32 X 0.375 INCH,PNH STL	83385	OBD
						- - - * - - -		
-39	386-3797-00			1		PLATE,MODULE:LEFT	80009	386-3797-00
						(ATTACHING PARTS)		
-40	212-0023-00			8		SCREW,MACHINE:8-32 X 0.375 INCH,PNH STL	83385	OBD
-41	212-0137-00			3		SCREW,MACHINE:8-32 X 0.375 L,PNH,STEEL	83385	OBD
						- - - * - - -		
-42	343-0775-00			10		CLIP,SPR TNSN:	80009	343-0775-00
-43	012-0771-00			1		CABLE,INTCON:45.0 L FLEX DISC TO CONT. TO R/P	80009	012-0771-00
						(ATTACHING PARTS)		
-44	211-0012-00			2		SCREW,MACHINE:4-40 X 0.375 INCH,PNH STL	83385	OBD
						- - - * - - -		
	012-0770-01			1		CABLE,INTCON:72.0 L FLEX DISC TO CONT UNIT	80009	012-0770-01
-45	407-2140-00			1		BRACKET,SUPPORT:ALUMINUM	80009	407-2140-00
						(ATTACHING PARTS)		
-46	211-0510-00			4		SCREW,MACHINE:6-32 X 0.375 INCH,PNH STL	83385	OBD
-47	210-0803-00			4		WASHER,FLAT:0.15 ID X 0.375 INCH OD,STL	12327	OBD
						- - - * - - -		
-48	131-2236-00			4		BUS,CONNECTOR:	80009	131-2236-00
						(ATTACHING PARTS FOR EACH)		
-49	211-0504-00			2		SCREW,MACHINE:6-32 X 0.25 INCH,PNH STL	83385	OBD
						- - - * - - -		
-50	124-0364-00			1		TERMINAL BOARD:30 CONT,PLASTIC W/HDWR	80009	124-0364-00
						(ATTACHING PARTS)		
-51	210-0457-00			2		NUT,PLAIN,EXT W:6-32 X 0.312 INCH,STL	83385	OBD
-52	211-0513-00			2		SCREW,MACHINE:6-32 X 0.625 INCH,PNH STL	83385	OBD
	214-2816-00			1		HARDWARE KIT:JACK SOCKET	80009	214-2816-00
-53	119-0420-00			1		FILTER,RFI:6A,250VAC,400HZ	02777	F-11935-6
						(ATTACHING PARTS)		
-54	210-0586-00			2		NUT,PLAIN,EXT W:4-40 X 0.25 INCH,STL	78189	OBD
-55	211-0012-00			2		SCREW,MACHINE:4-40 X 0.375 INCH,PNH STL	83385	OBD
						- - - * - - -		
-56	386-3790-00			1		STIF,REAR PANEL:	80009	386-3790-00
						(ATTACHING PARTS)		
-57	211-0511-00			4		SCREW,MACHINE:6-32 X 0.50 INCH,PNH STL	83385	OBD
-58	210-0457-00			4		NUT,PLAIN,EXT W:6-32 X 0.312 INCH,STL	83385	OBD
						- - - * - - -		
-59	200-2222-00			2		GUARD,FAN:	80009	200-2222-00
						(ATTACHING PARTS FOR EACH)		
-60	211-0513-00			4		SCREW,MACHINE:6-32 X 0.625 INCH,PNH STL	83385	OBD
-61	210-0457-00			8		NUT,PLAIN,EXT W:6-32 X 0.312 INCH,STL	83385	OBD
						- - - * - - -		
-62	119-0721-00			2		FAN,VENTILATING:75C FM,7W,115VAC 50/60 HZ	80009	119-0721-00
-63	118-0405-00			4		FUSEHOLDER:	80009	118-0405-00
-64	334-3445-00			1		MARKER,IDENT:MARKED WARNING	80009	334-3445-00
	343-0709-00			1		CLAMP,CABLE:4.38 L,ALUMINUM	80009	343-0709-00
-65	343-0722-01			1		CLAMP,CABLE:3.125 L,ALUMINUM,W/BUSHINGS	80009	343-0722-01
						(ATTACHING PARTS)		
-66	210-0949-00			2		WASHER,FLAT:0.141 ID X 0.50 INCH OD,BRS	12327	OBD
						- - - * - - -		
-67	214-2721-00			1		ADAPTER BAR:CABLE TO FLEX DISC DRIVE	80009	214-2721-00
						(ATTACHING PARTS)		
-68	211-0511-00			2		SCREW,MACHINE:6-32 X 0.50 INCH,PNH STL	83385	OBD
-69	210-0408-00			2		NUT,PLAIN,HEX.:6-32 X 0.312 INCH,BRS	73743	3040-402
						- - - * - - -		
-70	333-2341-00			1		PANEL,REAR:	80009	333-2341-00
-71	407-2081-00			1		BRKT,POWER SPLY:LEFT,ALUMINUM	80009	407-2081-00
						(ATTACHING PARTS)		
-72	212-0023-00			10		SCREW,MACHINE:8-32 X 0.375 INCH,PNH STL	83385	OBD
-73	210-0458-00			8		NUT,PLAIN,EXT W:8-32 X 0.344 INCH,STL	83385	OBD
						- - - * - - -		

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
1-74	407-2082-00			1		BRKT,POWER SPLY:ALUMINUM	80009	407-2082-00
						(ATTACHING PARTS)		
-75	212-0023-00			7		SCREW,MACHINE:8-32 X 0.375 INCH,PNH STL	83385	OBD
-76	210-0458-00			6		NUT,PLAIN,EXT W:8-32 X 0.344 INCH,STL	83385	OBD
						- - - * - - -		
-77	407-2080-00			1		BRKT,POWER SPLY:RIGHT,ALUMINUM	80009	407-2080-00
						(ATTACHING PARTS)		
-78	212-0023-00			8		SCREW,MACHINE:8-32 X 0.375 INCH,PNH STL	83385	OBD
-79	210-0458-00			6		NUT,PLAIN,EXT W:8-32 X 0.344 INCH,STL	83385	OBD
						- - - * - - -		
-80	200-2159-00			1		COVER,PWR SUPPLY:	80009	200-2159-00
-81	432-0122-00			1		BASE,PWR SUPPLY:	80009	432-0122-00
						(ATTACHING PARTS)		
-82	212-0023-00			6		SCREW,MACHINE:8-32 X 0.375 INCH,PNH STL	83385	OBD
						- - - * - - -		
-83	441-1395-00			1		CHAS,FLEX DISC:MAIN	80009	441-1395-00
						(ATTACHING PARTS)		
-84	212-0023-00			3		SCREW,MACHINE:8-32 X 0.375 INCH,PNH STL	83385	OBD
						- - - * - - -		
-85	436-0143-00			1		TRAY,FLEX DISC:	80009	436-0143-00
						(ATTACHING PARTS)		
-86	212-0040-00			8		SCREW,MACHINE:8-32 X 0.375 100 DEG,FLH STL	83385	OBD
						- - - * - - -		
-87	118-0195-00			2		MODULE:FLEX DISC DR,60HZ,110V	80009	118-0195-00
-88	333-2345-00			1		PANEL,FRONT:	80009	333-2345-00


A10



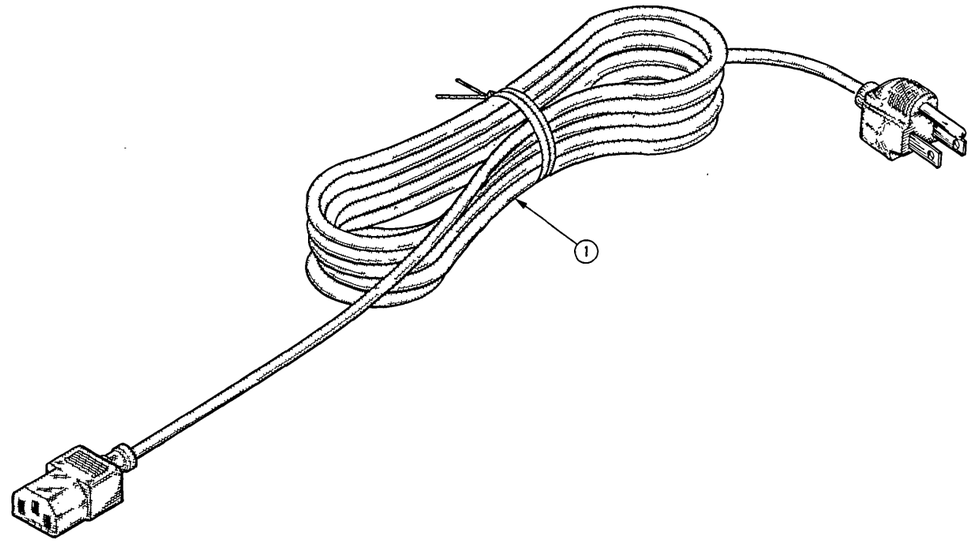


Fig. 2

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
						STANDARD ACCESSORIES		
	070-2587-00			1		MANUAL,TECH:INSTRUCTION	80009	070-2587-00
-1	161-0066-00			1		CABLE ASSY,PWR,:3 WIRE,98 INCH LONG	80009	161-0066-00

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
-1	012-0770-01			1		CABLE,INTCON:72.0 LONG FLEX DISC TO CONT UNIT	80009	012-0770-01

Tektronix®
COMMITTED TO EXCELLENCE

MANUAL CHANGE INFORMATION

Date: 6-26-79 Change Reference: C1/679

Product: 8002A µPROCESSOR LAB FLEXIBLE DISC SERVICE Manual Part No.: 070-2587-00

DESCRIPTION

SCHEMATIC CORRECTIONS

SECTION 6 DIAGRAMS

FLEXIBLE DISC POWER SUPPLY - DIAGRAM 3, left-side schematic, assembly number block

CHANGE TO:

A74 HD24 - 4.8 +5V

FLEXIBLE DISC POWER SUPPLY - DIAGRAM 3, right-side schematic, assembly number block

CHANGE TO:

A76 HC5-6 +24V

PARTS LIST CORRECTIONS

SECTION 5 REPLACEABLE ELECTRICAL PARTS

Page 5-3 circuit number A10

CHANGE TO:

A70 670-5294-00 CKT BOARD ASSY:CONTROLLER BOARD

SECTION 5 REPLACEABLE ELECTRICAL PARTS and

SECTION 7 REPLACEABLE MECHANICAL PARTS

ADD the electrical and mechanical parts listings for board assemblies A74 and A76 as follows:

DESCRIPTION

ELECTRICAL

Ckt No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A74	118-0511-00			CKT BOARD ASSY:HD24-4.8 +5V	80009	118-0511-00
C2	290-0868-00			CAP.,FXD,ELCTLT:47UF,+50-10%,50VDC	000F0	50UBSL47
C3	290-0872-00			CAP.,FXD,ELCTLT:16000UF,50V	09023	160005083
C4	283-0065-00			CAP.,FXD,CER DI:0.001UF,5%,100V	72982	805-518-Z5D0102J
C5	290-0866-00			CAP.,FXD,ELCTLT:330UF,+50-10%,35VDC	000F0	35VBSL330
CR1	152-0729-00			SEMICOND DVC,DI:RECT,SI,DUAL,30A,100V	24039	R711A
CR3	152-0066-00			SEMICOND DEVICE:SILICON,400V,750MA	80009	152-0066-00
CR4	152-0066-00			SEMICOND DEVICE:SILICON,400V,750MA	80009	152-0066-00
Q1	151-0140-00			TRANSISTOR:SILICON,NPN	80009	151-0140-00
Q2	----- -----			(P/N NOT AVAILABLE AT THIS PRINTING)		
Q3	151-0140-00			TRANSISTOR:SILICON,NPN	80009	151-0140-00
R1	301-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.50W	01121	EB2225
R2	308-0465-00			RES.,FXD,WW:0.225 OHM,10%,2W	80009	308-0465-00
R4	308-0465-00			RES.,FXD,WW:0.225 OHM,10%,2W	80009	308-0465-00
R5	301-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.50W	01121	EB2225
R6	118-0485-00			RES.,VAR,WW:1.5K OHM,20%,1.5W	11236	TYPE 110
R7	301-0223-00			RES.,FXD,CMPSN:22K OHM,5%,0.50W	01121	EB2235
R10	301-0752-00			RES.,FXD,CMPSN:7.5K OHM,5%,0.50W	01121	EB1005
R11	301-0752-00			RES.,FXD,CMPSN:7.5K OHM,5%,0.50W	01121	EB1005
R12	307-0060-00			RES.,FXD,CMPSN:6.8 OHM,5%,0.50W	01121	EB68G5
R13	118-0485-00			RES.,VAR,WW:1.5K OHM,20%,1.5W	11236	TYPE 110
R14	322-0193-00			RES.,FXD,FILM:1K OHM,1%,0.25W	75042	CEBT0-1001F
R15	307-0060-00			RES.,FXD,CMPSN:6.8 OHM,5%,0.50W	01121	EB68G5
R17	322-0201-00			RES.,FXD,FILM:1.21K OHM,1%,0.25W	75042	CEBT0-1211F
R18	307-0060-00			RES.,FXD,CMPSN:6.8 OHM,5%,0.50W	01121	EB68G5
R19	301-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.50W	01121	EB2225
T1	118-0447-00			XFMR,PWR,STPDN:	000FR	082-12253
U1	156-0053-00			MICROCIRCUIT,LI:VOLTAGE REGULATOR	80009	156-0053-00
VR5	152-0175-00			SEMICOND DEVICE:ZENER,0.4W,5.6V,5%	80009	152-0175-00

MECHANICAL

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
	----- -----			1		CKT BOARD ASSY:HD24(SEE A74 EPL)		
	407-2080-00			1		. BRKT,POWER SPLY:RIGHT,ALUMINUM	80009	407-2080-00
	407-2081-00			1		. BRKT,POWER SPLY:LEFT, ALUMINUM	80009	407-2081-00
	118-0438-00			1		. CHAS,PWR SUPPLY:ALUMINUM	000FR	41211051
	----- -----			1		. TRANSFORMER:(SEE T1 EPL)		
						(ATTACHING PARTS)		
	210-0457-00			4		. NUT,PLAIN,EXT W:6-32 X 0.312 INCH,STL	83385	OBD
						- - - * - - -		
	118-0508-00			1		. RETAINER,CAP:	000FR	178503
						(ATTACHING PARTS)		
	211-0559-00			2		. SCREW,MACHINE:6-32 X 0.375"100 DEG,FLH STL	83385	OBD
	211-0578-00			2		. SCREW,MACHINE:6-32 X 0.438 INCH,PNH STL	83385	OBD
						- - - * - - -		
	----- -----			3		. CAPACITORS:(SEE C2,C3,C5 EPL)		
						(ATTACHING PARTS FOR EACH)		
	211-0578-00			2		. SCREW,MACHINE:6-32 X 0.438 INCH,PNH STL	83385	OBD
						- - - * - - -		
	386-0978-00			4		. INSULATOR,PLATE:TRANSISTOR	80009	386-0978-00
	343-0775-00			4		. CLIP,SPR TNSN:	76381	3484-1000

DESCRIPTION

ELECTRICAL

Ckt No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A76	118-0510-00			CKT BOARD ASSY:HC5-6+24V	80009	118-0510-00
C1	290-0869-00			CAP.,FXD,ELCTLT:1000UF,+50-10%,16VDC	000F0	16UBSL1000
C2	290-0879-00			CAP.,FXD,ELCTLT:2000UF,+50-10%,16VDC	50545	16TR22000
C3	290-0867-00			CAP.,FXD,ELCTLT:220UF,+50-10%,16VDC	000F0	16VBSL220
C4	283-0627-00			CAP.,FXD,MICA D:0.0033UF,5%,500V	00853	D195E332J0
CR1	152-0066-00			SEMICOND DEVICE:SILICON,400V,750MA	80009	152-0066-00
CR2	152-0659-00			SEMICOND DEVICE:SILICON,100V,6A	04713	MR751
CR3	152-0659-00			SEMICOND DEVICE:SILICON,100V,6A	04713	MR751
Q1	151-0439-00			TRANSISTOR:SILICON,NPN	80009	151-0439-00
Q2	----- -----			(P/N NOT AVAILABLE AT THIS PRINTING)		
R1	301-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.50W	01121	EB2225
R2	307-0051-00			RES.,FXD,CMPSN:2.7 OHM,5%,0.50W	01121	EB27G5
R3	301-0220-00			RES.,FXD,CMPSN:22 OHM,5%,0.50W	01121	EB2205
R4	118-0485-00			RES.,VAR,WW:1.5K OHM,20%,1.5W	11236	TYPE 110
R5	301-0392-00			RES.,FXD,CMPSN:3.9K OHM,5%,0.50W	01121	EB3925
R6	301-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.50W	01121	EB2225
R7	301-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.50W	01121	EB2225
R8	118-0485-00			RES.,VAR,WW:1.5K OHM,20%,1.5W	11236	TYPE 110
R9	322-0222-00			RES.,FXD,FILM:2K OHM,1%,0.25W	75042	CEBT0-2001F
R10	301-0220-00			RES.,FXD,CMPSN:22 OHM,5%,0.50W	01121	EB2205
R11	307-0060-00			RES.,FXD,CMPSN:6.8 OHM,5%,0.50W	01121	EB68G5
R12	307-0060-00			RES.,FXD,CMPSN:6.8 OHM,5%,0.50W	01121	EB68G5
SCR1	151-0534-00			SCR:SI,S0508LS3	000FP	50508LS3
T1	118-0448-00			XFMR,PWR,STPDN:	000FR	08212247
U1	156-0053-00			MICROCIRCUIT,LI:VOLTAGE REGULATOR	80009	156-0053-00
VR4	152-0175-00			SEMICOND DEVICE:ZENER,0.4W,5.6V,5%	80009	152-0175-00

MECHANICAL

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
	----- -----			1		CKT BOARD ASSY:HC55(SEE A76 EPL)		
	407-2080-00			1		. BRKT,POWER SPLY:RIGHT,ALUMINUM	80009	407-2080-00
	407-2081-00			1		. BRKT,POWER SPLY:LEFT, ALUMINUM	80009	407-2081-00
	118-0525-00			1		. CHASSIS,XSTR:ALUMINUM	000FR	412-11031
	210-0458-00			20		. NUT,PLAIN,EXT W:8-32 X 0.344 INCH,STL	83385	OBD
	212-0023-00			20		. SCREW,MACHINE:8-32 X 0.375 INCH,PNH STL	83385	OBD
	118-0514-00			2		. HEAT SINK:	000FR	082-128-2
						(ATTACHING PARTS)		
	211-0517-00			2		. SCREW,MACHINE:6-32 X 1 INCH,PNH,STL	83385	OBD
						- - - * - - -		
	----- -----			1		. TRANSISTOR:(SEE Q2 EPL)		
						(ATTACHING PARTS)		
	211-0578-00			1		. SCREW,MACHINE:6-32 X 0.438 INCH,PNH STL	83385	OBD
						- - - * - - -		
	118-0509-00			3		. SPACER,XSTR:PLASTIC	000FQ	BB103-G
	343-0149-00			2		. CLAMP,LOOP:NYLON	80009	343-0149-00
	343-0775-00			3		. CLIP,SPR TNSN:	76381	3484-1000

MANUAL CHANGE INFORMATION

Tektronix® COMMITTED TO EXCELLENCE

Date: 8-15-79 Change Reference: M36140

Product: 8002A µPROCESSOR LAB SERVICE Manual Part No.: 070-2587-00

DESCRIPTION

EFF SN B062397

ELECTRICAL PARTS LIST AND SCHEMATIC CHANGES

CHANGE TO:

A70	670-5294-03	CKT BOARD ASSY:CONTROLLER BOARD

ADD:

R6011	315-0202-00	RES.,FXD,CMPSN:2K OHM,5%,0.25W

DIAGRAM 1A FLEXIBLE DISC CONTROLLER/ INSTRUCTION GENERATOR

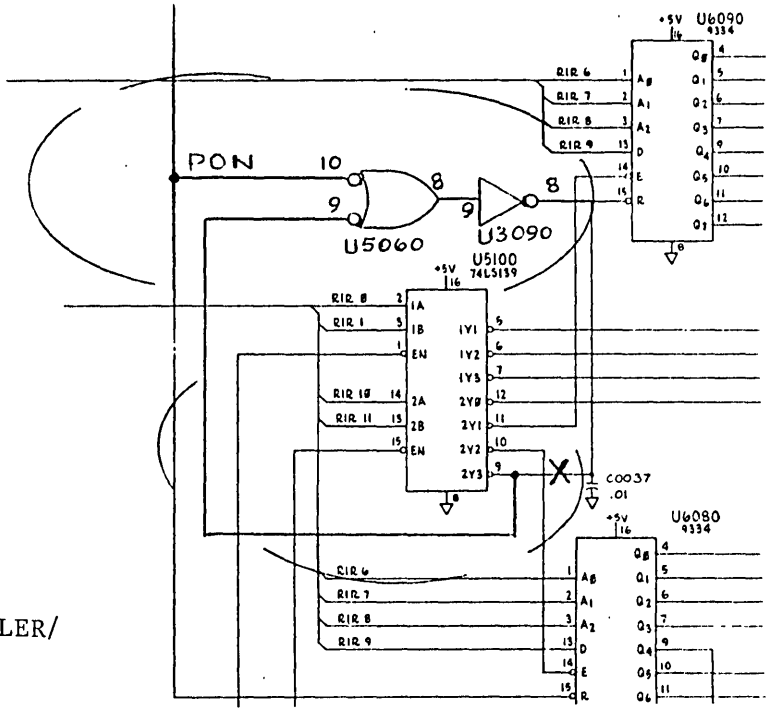


DIAGRAM 1D FLEXIBLE DISC CONTROLLER/ DRIVE I/O

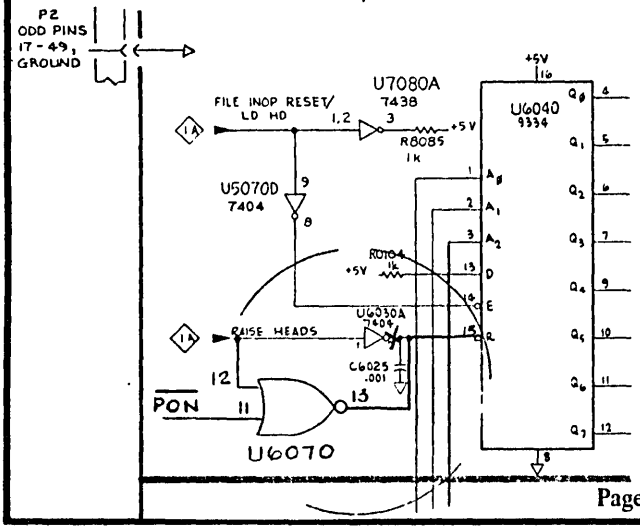
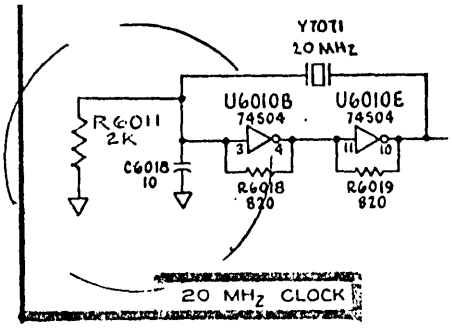


DIAGRAM 1E FLEXIBLE DISC CONTROLLER/READ/WRITE LOGIC



Appendix A

DECIMAL-HEXADECIMAL-BINARY EQUIVALENTS 0-255$_{10}$

Decimal-Hexadecimal-Binary Equivalents 0-255$_{10}$

Decimal	Hexadecimal	Binary 8-bit Code	Decimal	Hexadecimal	Binary 8-bit Code	Decimal	Hexadecimal	Binary 8-bit Code	Decimal	Hexadecimal	Binary 8-bit Code
0	00	0000 0000	64	40	0100 0000	128	80	1000 0000	192	C0	1100 0000
1	01	0000 0001	65	41	0100 0001	129	81	1000 0001	193	C1	1100 0001
2	02	0000 0010	66	42	0100 0010	130	82	1000 0010	194	C2	1100 0010
3	03	0000 0011	67	43	0100 0011	131	83	1000 0011	195	C3	1100 0011
4	04	0000 0100	68	44	0100 0100	132	84	1000 0100	196	C4	1100 0100
5	05	0000 0101	69	45	0100 0101	133	85	1000 0101	197	C5	1100 0101
6	06	0000 0110	70	46	0100 0110	134	86	1000 0110	198	C6	1100 0110
7	07	0000 0111	71	47	0100 0111	135	87	1000 0111	199	C7	1100 0111
8	08	0000 1000	72	48	0100 1000	136	88	1000 1000	200	C8	1100 1000
9	09	0000 1001	73	49	0100 1001	137	89	1000 1001	201	C9	1100 1001
10	0A	0000 1010	74	4A	0100 1010	138	8A	1000 1010	202	CA	1100 1010
11	0B	0000 1011	75	4B	0100 1011	139	8B	1000 1011	203	CB	1100 1011
12	0C	0000 1100	76	4C	0100 1100	140	8C	1000 1100	204	CC	1100 1100
13	0D	0000 1101	77	4D	0100 1101	141	8D	1000 1101	205	CD	1100 1101
14	0E	0000 1110	78	4E	0100 1110	142	8E	1000 1110	206	CE	1100 1110
15	0F	0000 1111	79	4F	0100 1111	143	8F	1000 1111	207	CF	1100 1111
16	10	0001 0000	80	50	0101 0000	144	90	1001 0000	208	D0	1101 0000
17	11	0001 0001	81	51	0101 0001	145	91	1001 0001	209	D1	1101 0001
18	12	0001 0010	82	52	0101 0010	146	92	1001 0010	210	D2	1101 0010
19	13	0001 0011	83	53	0101 0011	147	93	1001 0011	211	D3	1101 0011
20	14	0001 0100	84	54	0101 0100	148	94	1001 0100	212	D4	1101 0100
21	15	0001 0101	85	55	0101 0101	149	95	1001 0101	213	D5	1101 0101
22	16	0001 0110	86	56	0101 0110	150	96	1001 0110	214	D6	1101 0110
23	17	0001 0111	87	57	0101 0111	151	97	1001 0111	215	D7	1101 0111
24	18	0001 1000	88	58	0101 1000	152	98	1001 1000	216	D8	1101 1000
25	19	0001 1001	89	59	0101 1001	153	99	1001 1001	217	D9	1101 1001
26	1A	0001 1010	90	5A	0101 1010	154	9A	1001 1010	218	DA	1101 1010
27	1B	0001 1011	91	5B	0101 1011	155	9B	1001 1011	219	DB	1101 1011
28	1C	0001 1100	92	5C	0101 1100	156	9C	1001 1100	220	DC	1101 1100
29	1D	0001 1101	93	5D	0101 1101	157	9D	1001 1101	221	DD	1101 1101
30	1E	0001 1110	94	5E	0101 1110	158	9E	1001 1110	222	DE	1101 1110
31	1F	0001 1111	95	5F	0101 1111	159	9F	1001 1111	223	DF	1101 1111
32	20	0010 0000	96	60	0110 0000	160	A0	1010 0000	224	E0	1110 0000
33	21	0010 0001	97	61	0110 0001	161	A1	1010 0001	225	E1	1110 0001
34	22	0010 0010	98	62	0110 0010	162	A2	1010 0010	226	E2	1110 0010
35	23	0010 0011	99	63	0110 0011	163	A3	1010 0011	227	E3	1110 0011
36	24	0010 0100	100	64	0110 0100	164	A4	1010 0100	228	E4	1110 0100
37	25	0010 0101	101	65	0110 0101	165	A5	1010 0101	229	E5	1110 0101
38	26	0010 0110	102	66	0110 0110	166	A6	1010 0110	230	E6	1110 0110
39	27	0010 0111	103	67	0110 0111	167	A7	1010 0111	231	E7	1110 0111
40	28	0010 1000	104	68	0110 1000	168	A8	1010 1000	232	E8	1110 1000
41	29	0010 1001	105	69	0110 1001	169	A9	1010 1001	233	E9	1110 1001
42	2A	0010 1010	106	6A	0110 1010	170	AA	1010 1010	234	EA	1110 1010
43	2B	0010 1011	107	6B	0110 1011	171	AB	1010 1011	235	EB	1110 1011
44	2C	0010 1100	108	6C	0110 1100	172	AC	1010 1100	236	EC	1110 1100
45	2D	0010 1101	109	6D	0110 1101	173	AD	1010 1101	237	ED	1110 1101
46	2E	0010 1110	110	6E	0110 1110	174	AE	1010 1110	238	EE	1110 1110
47	2F	0010 1111	111	6F	0110 1111	175	AF	1010 1111	239	EF	1110 1111
48	30	0011 0000	112	70	0111 0000	176	B0	1011 0000	240	F0	1111 0000
49	31	0011 0001	113	71	0111 0001	177	B1	1011 0001	241	F1	1111 0001
50	32	0011 0010	114	72	0111 0010	178	B2	1011 0010	242	F2	1111 0010
51	33	0011 0011	115	73	0111 0011	179	B3	1011 0011	243	F3	1111 0011
52	34	0011 0100	116	74	0111 0100	180	B4	1011 0100	244	F4	1111 0100
53	35	0011 0101	117	75	0111 0101	181	B5	1011 0101	245	F5	1111 0101
54	36	0011 0110	118	76	0111 0110	182	B6	1011 0110	246	F6	1111 0110
55	37	0011 0111	119	77	0111 0111	183	B7	1011 0111	247	F7	1111 0111
56	38	0011 1000	120	78	0111 1000	184	B8	1011 1000	248	F8	1111 1000
57	39	0011 1001	121	79	0111 1001	185	B9	1011 1001	249	F9	1111 1001
58	3A	0011 1010	122	7A	0111 1010	186	BA	1011 1010	250	FA	1111 1010
59	3B	0011 1011	123	7B	0111 1011	187	BB	1011 1011	251	FB	1111 1011
60	3C	0011 1100	124	7C	0111 1100	188	BC	1011 1100	252	FC	1111 1100
61	3D	0011 1101	125	7D	0111 1101	189	BD	1011 1101	253	FD	1111 1101
62	3E	0011 1110	126	7E	0111 1110	190	BE	1011 1110	254	FE	1111 1110
63	3F	0011 1111	127	7F	0111 1111	191	BF	1011 1111	255	FF	1111 1111

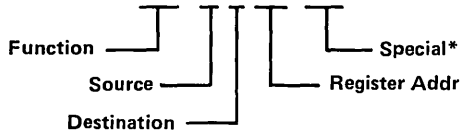
Appendix B

MICROPROGRAM INSTRUCTION FORMATS

The instruction formats and definitions of the descriptive Op Codes are presented in the following pages for the following types and classes:

Type A Register Group
Type A Input Group
Type U Unary Instruction
Type S Output Group
Type L Immediate Group
Type L Direct Transfer Group
Type L Through-Register Transfer Group

A. Op Code Example: DEC SR,A,R14



B. Field Definition:

Source		Destination		ALU Function						Reg. Addr.				Spec.	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

C. Restrictions:

Source	Destination	ALU Function	Register Addr	Special*
SR (01)	L,DR,A [See D(1)]	Label [See D(2)]	Any [See D(3)]	Any [See D(4)]

D. Special Coding:

(1) Destination:

Label	13	12	Description
L	0	0	TB bus data is not stored
DR	0	1	Store TB data in Register
A	1	0	Store TB data in Accumulator

(2) ALU Function:

Label	11	10	9	8	7	6	Function
ADD	1	0	1	0	1	1	Add
SUB	0	1	0	1	1	0	Subtract
INC	1	1	0	0	1	0	Increment
DEC	0	0	1	1	1	1	Decrement
OR	1	0	0	0	0	0	Logical OR
AND	1	1	0	1	0	0	Logical AND
NAN	0	0	1	0	0	0	Logical NAND
NOR	0	1	1	1	0	0	Logical NOR
NXR	0	1	0	1	0	0	Logical Exclusive NOR
CMD	0	0	1	1	0	0	Complement
LOD	1	1	0	0	0	0	Pass Operand
ADC	1	0	1	0	1	0	Add with Carry
XOR	1	0	1	0	0	0	Logical Exclusive OR
RLC	1	1	1	1	1	0	Rotate Left with Carry
RLL	1	1	1	1	1	1	Shift Left with Carry
LRZ	1	1	1	1	0	0	Result = 0
LMN	0	0	0	0	1	1	Result = −1s
LON	0	0	0	0	0	0	Result = 1s

2587-20

Fig. B-1a. Type A Register Group Instruction Format.

@

(3) Register Address: R0 (0000) through R15 (1111).

*(4) Special:

Label	1	0	Description
None	0	0	No special function
SPSH	0	1	Start pushing carry C7 into Sector Buffer
PULL	1	0	Load Write Data flip-flop with carry C7
EPSH	1	1	Finish pushing carry C7 into Sector Buffer

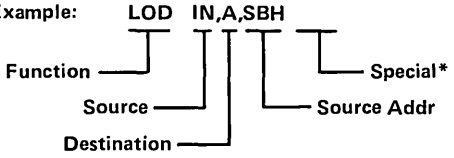
E. Remarks: (1) Source label SR indicates the Working Registers as $\overline{WR}$ bus source.

*(2) Special command is added to Op Code only if concurrent control of the Sector Buffer or Write Data flip-flop is required.

2587-21

Fig. B-1b. Type A Register Group Instruction Format.

A. Op Code Example: LOD IN,A,SBH



B. Field Definition:

Source		Destination		ALU Function						Source Addr				Spec.	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

C. Restrictions:

Source	Destination	ALU Function	Source Addr	Special*
IN (11)	L,A [See D(1)]	Label [See D(2)]	Label [See D(3)]	Any [See D(2)]

D. Special Coding:

(1) Destination:

Label	13	12	Description
L	0	0	TB Bus data is not stored
A	1	0	Store TB data in Accumulator

(2) ALU Function and Special: Same as Register Group.

(3) Source Address:

Label	5	4	3	2	$\overline{WR}$ Bus Input from
None	0	0	0	0	Not used
TST	0	0	0	1	Test Panel switches
CSW	0	0	1	0	Input control/status byte
SBH	0	0	1	1	Sector Buffer to high bit ($\overline{WR7}$)
SBL	0	1	0	0	Sector Buffer to low bit ($\overline{WR0}$)
DBT	0	1	0	1	Read data bit ($\overline{WR7}$)
BYT	0	1	1	0	Host output byte
INL	0	1	1	1	Interleave switch S4104

E. Remarks: (1) Source label IN indicates that Inputs are $\overline{WR}$ bus source.

*(2) Special command is added to Op Code only if concurrent control of the Sector Buffer or Write Data flip-flop is required.

2587-22

Fig. B-2. Type A Input Group Instruction Format.

A. Op Code Example: LAR R8

Command — LAR
Register Addr — R8
Special* — (blank)

B. Field Definition:

Unary Command										Reg. Addr.				Spec.	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

C. Restrictions:

Unary Command	Register Addr	Special*
Label	Any	Any
[See D(1)]	[See D(2)]	[See D(3)]

D. Special Coding:

(1) Unary Command:

	Source		Dest.		ALU Function						
Label	15	14	13	12	11	10	9	8	7	6	Description
LAR	0	1	1	0	1	1	0	0	0	0	Load Accumulator from Register
LRA	0	1	0	1	1	0	0	1	0	0	Load Register from Accumulator
COM	0	1	1	0	0	1	1	0	0	0	Complement Accumulator
CMR	0	1	1	0	0	0	1	1	0	0	Complement Register
LCA	0	1	0	1	0	1	1	0	0	0	Load Register with Complement of Accumulator
LCR	0	1	1	0	0	0	1	1	0	0	Load Accumulator with Complement of Register
LRZ	0	1	0	1	0	1	1	1	0	0	Load Register with 0s
LAZ	0	1	1	0	1	1	1	1	0	0	Load Accumulator with Os
LRM	0	1	0	1	0	0	0	0	1	1	Load Register with 1s
LAM	0	1	1	0	0	0	0	0	1	1	Load Accumulator with 1s
NOP	0	0	0	0	0	0	0	0	0	0	Wait (No Operation)
LDL	0	0	0	1	0	0	0	0	0	0	Load Latches

(2) Register Addr and (3) Special: Same as Type A Register Group.

E. Remarks: (1) Source of $\overline{WR}$ bus is Registers.

*(2) Special command is added only if concurrent control of Sector Buffer or Write Data flip-flop is required.

2587-23

Fig. B-3. Type U Unary Instruction Format.

@

A. Op Code Example: RSP

Command

B. Field Definition:

Source		Destination		Command: Type		Command: Function				(Not Used)					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

C. Restrictions:

Source	Destination	Command
No Code* (00)	L (00)	Label (See D)

D. Special Coding:

(1) Command Type:

Label	11	10	9	8	7	6	Hex	Description
CDA	0	0	1	0	0	0	0200	Load Drive Address
Noted	0	1	x	x	x	x	See D(2)	Command Group 1
Noted	1	0	x	x	x	x	See D(2)	Command Group 2
RST	1	1	0	0	0	0	0C00	Reset Group 1
NOP	0	0	0	0	0	0	0000	No operation (Wait)

(2) Command Function:

Group 1

Label	9	8	7	6	Hex	Command
RBY	0	0	0	0	0400	Reset BUSY
SBY	1	0	0	0	0600	Set BUSY
RIP	0	0	0	1	0440	Reset ILLEGAL OP
SIP	1	0	0	1	0640	Set ILLEGAL OP
RER	0	0	1	0	0480	Reset ERROR RECOVERY
SER	1	0	1	0	0680	Set ERROR RECOVERY
RCK	0	0	1	1	04C0	Reset UNIT CHECK
SCK	1	0	1	1	06C0	Set UNIT CHECK
RFI	0	1	0	0	0500	Reset FILE INOP RST/LD HD
SFI	1	1	0	0	0700	Set FILE INOP RST/LD HD
RWR	0	1	0	1	0540	Reset WRITE GATE
SWR	1	1	0	1	0740	Set WRITE GATE
RPT	0	1	1	0	0580	Reset PRINT STRB
SPT	1	1	1	0	0780	Set PRINT STRB
SFG	0	1	1	1	05C0	Set HOST FLG
RFG	1	1	1	1	07C0	Reset HOST FLG

2587-24

Fig. B-4a. Type S Output Group Instruction Format.

(2) Command Function: (Continued)

Group 2

Label	9	8	7	6	Hex	Command
RHD	0	0	0	0	0800	Reset RAISE HEADS
SHD	1	0	0	0	0A00	Set RAISE HEADS
DR0	0	0	0	1	0840	Reset DIRECTION (IN)
DRI	1	0	0	1	0A40	Set DIRECTION (IN)
RSP	0	0	1	0	0880	Reset STEP
SSP	1	0	1	0	0A80	Set STEP
DSK	0	0	1	1	08C0	Reset EN STACK
ESK	1	0	1	1	0AC0	Set EN STACK
EDY	0	1	0	0	0B00	Reset EN DISPLAY
DDY	1	1	0	0	0900	SET EN DISPLAY
RDD	0	1	0	1	0940	Reset SELECT CARRY
RDC	1	1	0	1	0B40	Set SELECT CARRY
TKL	0	1	1	0	0980	Reset > TRK43
TKH	1	1	1	0	0B80	Set > TRK43
SLB	0	1	1	1	09C0	Reset UBANK
SHB	1	1	1	1	0BC0	Set UBANK

E. Remarks: (1) Command Groups 1 and 2 globally reset on power up.

*(2) Source selects Instruction Decoder latches.

2587-25

Fig. B-4b. Type S Output Group Instruction Format.

A. Op Code Example: LOD I,A,Value

Function — LOD
Source — I
Destination — A
Data Byte — Value

B. Field Definition:

Source		Destination		ALU Function				Data Byte							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

C. Restrictions:

Source	Destination	ALU Function	Data Byte
I	L,A	Label	Any
(RIR)	(None,Acc.)	(See D)	(RIR)

D. Special Coding:

Label	11	10	9	8	Description
OR	1	0	0	0	Logical Inclusive OR
XOR	1	0	1	0	Logical Exclusive OR
AND	1	1	0	1	Logical AND
NAN	0	0	1	0	Logical NAND
NOR	0	1	1	1	Logical NOR
NXR	0	1	0	1	Logical Exlusive NOR
LOD	1	1	0	0	Pass Operand
NOP	1	1	1	1	Results = 0

E. Remarks: (1) Registers (DR,R) cannot be used as a destination.
(2) ALU is forced into Logic mode.
(3) Data byte is used by ALU as operand.

2587-26

Fig. B-5. Type L Immediate Group Instruction Format.

A. Op Code Example: J4Z I,M,Address

Condition — J4Z
Source — I
Destination — M
Target Address* — Address

B. Field Definition:

Source		Destination		Condition				Target Address							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

C. Restrictions:

Source	Destination	Condition	Target Address*
I	M	Label	Any of 256
(RIR)	(RAR)	(See D)	(RIR)

D. Special Coding:

Label	(11	10	9	8)	Condition: Jump On
JMP	1	1	1	0	Unconditional Jump
JNZ	0	0	0	0	Non-Zero Result
JZR	0	0	0	1	Zero Result
JDR	1	1	0	0	Data Ready
JNR	1	1	0	1	Data Not Ready
JLB	1	0	1	0	Bit 0 = True
JLZ	1	0	1	1	Bit 0 = False
J2N	1	0	0	0	Bit 2 = True
J2Z	1	0	0	1	Bit 2 = False
J4N	0	1	0	0	Bit 4 = True
J4Z	0	1	0	1	Bit 4 = False
J6N	0	0	1	0	Bit 6 = True
J6Z	0	0	1	1	Bit 6 = False
JNC	0	0	1	0	Carry = True
JZC	0	0	1	1	Carry = False

E. Remarks: (1) Source defines RIR bus as source of target address.

(2) Transfer from Source (RIR) to Destination (RAR) occurs only on specified jump condition

*(3) Destination (target) address is the 1s complement of the address on RIR bus.

2587-27

Fig. B-6. Type L Direct Transfer Group Instruction Format.

A. Op Code Example: JZR SR,M,R5

Condition — JZR
Source — SR
Destination — M
Source Address* — R5

B. Field Definition:

Source		Destination		Condition				Not Used		Reg. Address				Not Used	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

C. Restrictions:

Source	Destination	Condition	Source Address*
SR (Reg.)	M (RAR)	Label (See D)	R0-R15 (Reg.)

D. Special Coding: (1) Condition: Same as Direct Transfer Group.

(2) Reg. Address:

5	4	3	2	Register
1	1	1	1	R0
1	1	1	0	R1
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
0	0	0	0	R15

E. Remarks: (1) Source (SR) defines Working Registers as source of target address.

(2) Transfer from Source (Register) to Destination (RAR) occurs only on specified jump condition.

*(3) Register Address is 1s complement of register number.

2587-28

Fig. B-7. Type L Through-Register Transfer Group Instruction Format.

Appendix C

MICROPROGRAM LISTING

The following pages contain an annotated listing of the Flexible Disc Unit microprogram.

SYMBOL	ADDRESS HEX	DECIMAL	OCTAL	BINARY	ASCII
WEND	01FC	00508	000774	0000000111111100	A <
WRT8	01F6	00502	000766	0000000111110110	A6
WRT7	01F1	00496	000760	0000000111110000	A 0
WRT6	01EE	00494	000756	0000000111101110	A .
WRT5B	01DE	00479	000737	0000000111011111	A ←
WRT5A	01DB	00475	000733	0000000111011011	A (
WRT5	01D9	00473	000731	0000000111011001	A Y
WRT4	01D3	00467	000723	0000000111010011	A S
WRT3	01CD	00461	000715	0000000111001101	A M
DOUT	01C1	00449	000701	0000000111000001	A A
WRT2	01BA	00442	000672	0000000110111010	A :
WRT1	01B4	00436	000664	0000000110110100	A 4
WRT	01AA	00426	000652	0000000110101010	A *
ICRC	01A3	00419	000643	0000000110100011	A #
X4	01A1	00417	000641	0000000110100001	A !
RTN	019F	00415	000637	0000000110011111	A ←
ERTN	019B	00411	000633	0000000110011011	A (
FNRD	0194	00404	000624	0000000110010100	A T
CRC	018E	00398	000616	0000000110001110	A N
CRC2	0182	00386	000602	0000000110000010	A B
SBLP	017E	00382	000576	0000000101111110	A >
RD4	0174	00372	000564	0000000101110100	A 4
RD4A	0171	00369	000561	0000000101110001	A 1
RD3	0163	00355	000543	0000000101100011	A #
RIDE	0161	00353	000541	0000000101100001	A !
RD2	0156	00342	000526	0000000101010110	A V
RD1	014B	00331	000513	0000000101001011	A K
RD	013D	00317	000475	0000000100111101	A =
X2	0132	00306	000462	0000000100110010	A 2
X1A	0130	00304	000460	0000000100110000	A 0
X1	0127	00295	000447	0000000100100111	A '
STCK	011E	00286	000436	0000000100011110	A ↑
X3	010F	00271	000417	0000000100001111	A O
ERN	010E	00270	000416	0000000100001110	A N
X	0100	00256	000400	0000000100000000	A @

SYMBOL	ADDRESS				
	HEX	DECIMAL	OCTAL	BINARY	ASCII
PNT	00FC	00252	000374	0000000011111100	@ <
S5	00FA	00250	000372	0000000011111010	@ :
S4	00EB	00235	000353	0000000011101011	@ +
S3	00E9	00233	000351	0000000011101001	@)
S1	00E2	00226	000342	0000000011100010	@ "
SK0	00DF	00223	000337	0000000011011111	@ ←
S0R	00DD	00221	000335	0000000011011101	@)
S0	00D5	00213	000325	0000000011010101	@ U
SEEK	00D3	00211	000323	0000000011010011	@ S
E9B	00D0	02208	000320	0000000011010000	@ P
EX9	00AE	00174	000256	0000000010101110	@ .
E10	00A7	00167	000247	0000000010100111	@ '
E11	00A3	00163	000243	0000000010100011	@ #
EX8	009A	00154	000232	0000000010011010	@ 7
EX7	008E	00142	000216	0000000010001110	@ N
DTA	0084	00132	000204	0000000010000100	@ D
ILOP	0082	00130	000202	0000000010000010	A B
SCT	007F	00127	000177	0000000001111111	@ ?
DRV	0075	00117	000165	0000000001110101	@ 5
E6B	0066	00102	000146	0000000001100110	@ &
E6A	0062	00098	000142	0000000001100010	@ "
EX6	0059	00089	000131	0000000001011001	@ Y
E5A	0058	00088	000130	0000000001011000	@ X
GRD	0056	00086	000126	0000000001010110	@ V
GWRT	0054	00084	000124	0000000001010100	@ T
EX5	0043	00067	000103	0000000001000011	@ C
E4A	003D	00061	000075	0000000000111101	@ =
EX4	0034	00052	000064	0000000000110100	@ 4
EX3	001C	00028	000034	0000000000011100	@ /
EX2	0018	00024	000030	0000000000011000	@ X
EX2A	0017	00023	000027	0000000000010111	@ W
EX1	0014	00020	000024	0000000000010100	@ T
CNT	0006	00006	000006	0000000000000110	@ F
EXEC	0000	00000	000000	0000000000000000	@ @
MSK2	FFDE	65502	177736	1111111111011110	? ↑
MSK1	FFEF	65519	177757	1111111111101111	? /
SYNC	FF04	65284	177404	1111111100000100	? D

FLOPPY DISC MICROCODE

SEQ#	ADRS HED	BINARY-INSTRUCTION-HEX FLOPPY DISC		LABEL	OP-CODE		
003	*	SYMBOL DEFINITIONS					
YNC	E						
0005		1111111100000100	FF04	SYNC	EQU	-251-1	ONES COMPLEMENT OF 251(10)
0006		1111111111101111	FFEF	MSK1	EQU	-16-1	ONES COMPLEMENT OF 16(10)
0007		1111111111011110	FFDE	MSK2	EQU	-33-1	ONES COMPLEMENT OF 33(10)
XEC	R						
0009	0000	0000110000000000	0C00	EXEC	RST		INIT. NEEDED FOR AUTOLOAD, PON FORCES RST
0010	0001	1010110000000000	AC00		LOD	I,A,0	THE FOLLOWING SEQUENCE EFFECTS A 2 SEC DELAY
0011	0002	0101111100000000	5F00		LRZ	R0	
0012	0003	0101111100010000	5F10		LRZ	R4	
0013	0004	0101111100100100	5F24		LRZ	R9	
0014	0005	0101111100101100	5F2C		LRZ	R11	
0015	0006	0101110010010000	5C90	CNT	INC	SR,DR,R4	TRIPLE BYTE INCREMENT
0016	0007	0101101010100100	5AA4		ADC	SR,DR,R9	
0017	0008	0101101010101100	5AAC		ADC	SR,DR,R11	
0018	0009	1011010111111001	B5F9		J4Z	I,M,CNT	
0019	000A	1010110010001000	AC88		LOD	I,A,'H88	SET CMD TO READ FOR AUTO-LOAD
0020	000B	0101100100011000	5918		LRA	R6	
0021	000C	0101111100010000	5F10		LRZ	R4	SET DRIVE ADD TO ZERO
0022	000D	0101111100100100	5F24		LRZ	R9	SET TARGET SECTOR TO ZERO
0023	000E	0101111100101100	5F2C		LRZ	R11	SET TARGET TRACK TO ZERO
0024	000F	1010110010000000	AC80		LOD	I,A,128	SET COUNT TO 128
0025	0010	0101100100110100	5934		LRA	R13	
0026	0011	1010110000000001	AC01		LOD	I,A,1	SET FLAGS TO ZERO EXCEPT SEEK = 1
0027	0012	0101100100001100	590C		LRA	R3	
0028	0013	0101111100100000	5F20		LRZ	R8	CLEAR INTERNAL CSW (ICSW)
0029	0014	0101000011101000	50E8	EX1	LRM	R10	SET CURRENT TRACK UNKNOWN
0030	0015	0100110000010000	4C10		LOD	SR,L,R4	PUT CURRENT DRIVE ADDRESS IN LATCHES
0031	0016	0000001000000000	0200		CDA		SELECT THE DRIVE
0032	0017	0101000011011100	50DC	EX2A	LRM	R7	SET CURRENT SECTOR UNKNOWN
0033	0018	0000011100000000	0700	EX2	SFI		PULSE THE FILE INOP/LOWER THE HEAD
0034	0019	0000010100000000	0500		RFI		
0035	001A	1010110011110110	ACF6		LOD	I,A,246	SET BOUND DELAY = −10, 50 MS
0036	001B	0101100100010100	5914		LRA	R5	

FLOPPY DISC MICROCODE (cont)

SEQ#	ADRS	BINARY-INSTRUCTION-HEX	LABEL	OP-CODE		
0037	001C	0110001100100000 6320	EX3	CMD	SR,A,R8	COMPLEMENT LAST ICSW
0038	001D	0101100100001000 5908		LRA	R2	SAVE IN R2
0039	001E	1110110000001000 EC08		LOD	IN,A,CSW	GET CURRENT CSW
0040	001F	0101100100100000 5920		LRA	R8	UPDATE LAST CSW
0041	0020	1011100011010111 B8D7		J2N	I,M,*+8	TEST STROBE HIGH
0042	0021	0100111111110100 4FF4		RLL	SR,L,R13	NO, IS CNT = 128?
0043	0022	1011011111011000 B7D8		JZC	I,M,*+5	NO RESET
0044	0023	1011000011011000 B0D8		JNZ	I,M,*+4	
0045	0024	1100110000001000 CC08		LOD	IN,L,CSW	TEST DRIVE READY
0046	0025	1011101110100000 BBA0		JLZ	I,M,E6A−3	
0047	0026	1011111011010111 BED7		JMP	I,M,*+2	
0048	0027	0000011111000000 07C0		RFG		RESET HOST FLAG
0049	0028	0110110100001000 6D08		AND	SR,A,R2	LEADING EDGE FUNCTION TO R2 AND ACC
0050	0029	0101100100001000 5908		LRA	R2	
0051	002A	1011001111001011 B3CB		J6Z	I,M,EX4	TEST FOR LEADING EDGE OF INDEX
0052	002B	0101111100011100 5F1C		LRZ	R7	YES, SET SECIN = 00
0053	002C	0100111111010100 4FD4		RLL	SR,L,R5	TEST R5 GREATER THAN ZERO (DELAY REG)
0054	002D	1011011010100111 B6A7		JNC	I,M,E5A	NO, MINUS
0055	002E	1011000110100111 B1A7		JZR	I,M,E5A	NO, ZERO
0056	002F	0101001111010100 53D4		DEC	SR,DR,R5	YES. DECREMENT DELAY
0057	0030	1011000010100111 B0A7		JNZ	I,M,E5A	TEST FOR DELAY = ZERO
0058	0031	0000101000000000 0A00		SHD		
0059	0032	0000100000000000 0800		RHD		YES. RAISE HEAD
0060	0033	1011111010100111 BEA7		JMP	I,M,E5A	
0061	0034	1011010110100110 B5A6	EX4	J4Z	I,M,EX6	TEST FOR LEADING EDGE OF SECTOR
0062	0035	1010110100000100 AD04		AND	I,A,'H04	MASK OFF STROBE FROM LEF, IF IT WAS HIGH
0063	0036	0101101000100000 5A20		XOR	SR,DR,R8	ZERO STROBE OF ICSW IF STROBE LEF WAS "1"
0064	0037	0100111111010100 4FD4		RLL	SR,L,R5	TEST FOR DELAY LESS THAN ZERO
0065	0038	1011011111000010 B7C2		JZC	I,M,E4A	NO
0066	0039	0101110010010100 5C94		INC	SR,DR,R5	YES, INCREMENT
0067	003A	1011000011000010 B0C2		JNZ	I,M,E4A	DELAY = ZERO?
0068	003B	1010110000010100 AC14		LOD	I,A,20	YES, SET DELAY = 20
0069	003C	0101100100010100 5914		LRA	R5	
0070	003D	0110110010011100 6C9C	E4A	INC	SR,A,R7	SECON = −1?
0071	003E	1011000110111100 B1BC		JZR	I,M,EX5	YES. GO TO EX5
0072	003F	1110110000011100 EC1C		LOD	IN,A,INL	ADD PROG FORMAT TO EACH SEQ. SECTOR

FLOPPY DISC MICROCODE (cont)

SEQ#	ADRS	BINARY-INSTRUCTION-HEX	LABEL	OP-CODE		
0073	0040	0110101011011100 6ADC		ADD	SR,A,R7	
0074	0041	1010110100011111 AD1F		AND	I,A,31	MASK OFF HIGHER BITS
0075	0042	0101100100011100 591C		LRA	R7	UPDATE CURRENT SECTOR
0076	0043	0110110000001100 6C0C	EX5	LAR	R3	PROG FLAGS TO ACC AND ATCHS
0077	0044	1011001010101001 B2A9		J6N	I,M,GRD	GTID1 NOT ZERO, READ
0078	0045	1000110100000011 8D03		AND	I,L,3	TEST FOR SEEK
0079	0046	1011000000101100 B02C		JNZ	I,M,SEEK	GO TO SEEK
0080	0047	1000110110000000 8D80		AND	I,L,128	TEST GTID2 FOR ZERO
0081	0048	1011000010101001 B0A9		JNZ	I,M, GRD	NO
0082	0049	0100111111110100 4FF4		RIL	SR,L,R13	YES. TEST COUNT
0083	004A	1011011111100011 B7E3		JZC	I,M,EX3	GO GET LEADING EDGE FUNCTION
0084	004B	1011000011100011 B0E3		JNZ	1,M,EX3	
0085	004C	0100111111001100 4FCC		RLL	RS,L,R3	
0086	004D	1011001010101001 B2A9		J6N	I,M,GRD	TEST GTCRC
0087	004E	1011010001111101 B47D		J4N	I,M,ILOP	TEST EOF PHYSICAL
0088	004F	0110110000011100 6C1C		LOD	SR,A,R7	TEST FOR SECTN = SECTX
0089	0050	0100101000100100 4A24		XOR	SR,L,R9	
0090	0051	1011000011100011 B0E3		JNZ	I,M,EX3	CONTINUE SEARCH
0091	0052	0100110000011000 4C18		LOD	SR,L,R6	TEST OPCODE
0092	0053	1011100110101001 B9A9		J2Z	I,M,GRD	
0093	0054	0000101111000000 0BC0	GWRT	SHB		
0094	0055	1011111001010101 BE55		JMP	I,M,WRT	GO TO WRITE (UPPER BANK)
0095	0056	0000101111000000 0BC0	GRD	SHB		
0096	0057	1011111011000010 BEC2		JMP	I,M,RD	GO TO READ (UPPER BANK)
0097	0058	0110110000001000 6C08	E5A	LAR	R2	LEF TO ACC AND LATCHES
0098	0059	1011100111100011 B9E3	EX6	J2Z	I,M,EX3	TEST FOR LE OF STROBE
0099	005A	1100111111001000 CFC8		RLL	IN,L,CSW	DECODE THE CONTROL PORT MODIFIER C0, C1
0100	005B	1011010010011101 B49D		J4N	I,M,E6A	
0101	005C	1011001010011001 B299		J6N	I,M,E6B	
0102	005D	0000110000000000 0C00		RST		START I/O
0103	005E	0101111100001100 5F0C		LRZ	R3	
0104	005F	1010110011111100 ACFC		LOD	I,A,252	SET COUNT TO −4
0105	0060	0101100100110100 5934		LRA	R13	
0106	0061	1011111011100011 BEE3		JMP	I,M,EX3	
0107	0062	1011001100000011 B303	E6A	J6Z	I,M,PNT	PRINT REQUEST?
0108	0063	0100111111011000 4FD8		RLL	SR,L,R6	NO. INPUT DATA REQUEST
0109	0064	1011010001100101 B465		J4N	I,M,EX8	
0110	0065	1011111000101111 BE2F		JMP	I,M,E9B	READ DIAGNOSTIC REQUEST
0111	0066	1110110000011000 EC18	E6B	LOD	IN,A,BYT	OUTPUT DATA REQUEST
0112	0067	0000010111000000 05C0		SFG		SET HOST FLAG
0113	0068	0101110010110100 5CB4		INC	SR,DR,R13	INC COUNT

FLOPPY DISC MICROCODE (cont)

SEQ#	ADRS	BINARY-INSTRUCTION-HEX		LABEL	OP-CODE		
0114	0069	1011000101110001	B171		JZR	I,M,EX7	SET DESIRED TRACK
0115	006A	0100111111110100	4FF4		RLL	SR,L,R13	TEST FOR DATA BYTE
0116	006B	1011011101111011	B77B		JZC	I,M,DTA	
0117	006C	1011000101111011	B17B		JZR	I,M,DTA	128TH BYTE
0118	006D	0100110010110100	4CB4		INC	SR,L,R13	COUNT NEGATIVE
0119	006E	1011000110000000	B180		JZR	I,M,SCT	COUNT = −1 (SECTOR)
0120	006F	1011101010001010	BA8A		JLB	I,M,DRV	COUNT = −2 (DRIVE)
0121	0070	0101100100011000	5918		LRA	R6	COUNT = −3 (CMD)
0122	0071	0100111111011000	4FD8		RLL	SR,L,R6	TEST FOR STANDARD CMD
0123	0072	1011010011100011	B4E3		J4N	I,M,EX3	YES, CONTINUE SCAN LOAD
0124	0073	1011000001011000	B058		JNZ	I,M,E10	NO, READ DIAG?
0125	0074	1011111000110001	BE31		JMP	I,M,E9B-2	READ DIAG CMD
0126	0075	0100101000010000	4A10	DRV	XOR	SR,L,R4	SAME DRIVE?
0127	0076	1011000110000110	B186		JZR	I,M,*+3	YES
0128	0077	0101100100010000	5910		LRA	R4	NO, UPDATE DRV REG
0129	0078	1011111011101011	BEEB		JMP	I,M,EX1	REINIT
0130	0079	0100111111010100	4FD4		RLL	SR,L,R5	SAME DRV, HEAD DOWN?
0131	007A	1011000111100111	B1E7		JZR	I,M,EX2	NO, GO LOWER HEAD
0132	007B	1011011011100011	B6E3		JNC	I,M,EX3	YES (IN 50 MS DELAY)
0133	007C	1010110000010100	AC14		LOD	I,A,20	YES, REFRESH HEAD DOWN TIMER
0134	007D	0101100100010100	5914		LRA	R5	
0135	007E	1011111011100011	BEE3		JMP	I,M,EX3	
0136	007F	0101100100100100	5924	SCT	LRA	R9	STORE TARGET SECTOR
0137	0080	1000110111100000	8DE0		AND	I,L,'HE0	MASK
0138	0081	1011000111100011	B1E3		JZR	I,M,EX3	SECTOR LEGAL
0139	0082	0000011001000000	0640	ILOP	SIP		ILLEGAL, SET ILLEGAL OP STATUS
0140	0083	1011111010100000	BEA0		JMP	I,M,E6A-3	
0141	0084	0101100100000100	5904	DTA	LRA	R1	HOST BYTE TO R1
0142	0085	1010110000001000	AC08		LOD	I,A,8	SET BIT COUNT IN R2
0143	0086	0101100100001000	5908		LRA	R2	
0144	0087	0000101011000000	0AC0		ESK		ENABLE STACK
0145	0088	0000101101000000	0B40		RDC		CARRY TO SECTOR BUFFER SELECT
0146	0089	0101111110000101	5F85		RLC	SR,DR,R1,SPSH	DATA BIT TO SECTOR BUFFER
0147	008A	0000000000000000	0000		NOP		DELAY
0148	008B	0101001111001011	53CB		DEC	SR,DR,R2 EPSH	DEC BIT COUNT
0149	008C	1011000001110110	B076		JNZ	I,M,*−3	TEST FOR FINISH
0150	008D	1011111011100011	BEE3		JMP	I,M,EX3	BYTE IN STACK, CONTINUE SCAN

FLOPPY DISC MICROCODE (cont)

SEQ#	ADRS	BINARY-INSTRUCTION-HEX	LABEL	OP-CODE		
0151	008E	0101100100101100 592C	EX7	LRA	R11	STORE TARGET TRACK
0152	008F	1010110011111100 ACFC		LOD	I,A,252	GET SEEK STATE MASK
0153	0090	0101110100001100 5D0C		AND	SR,DR,R3	SEEK STATE = 0
0154	0091	1010110001001101 AC4D		LOD	I,A,77	TRACK BOUNDS CHECK
0155	0092	0100010110101100 45AC		SUB	SR,L,R11	R11 G.E., CARRY
0156	0093	1011011001111101 B67D		JNC	I,M,ILOP	R11 L.T. 77, NO CARRY
0157	0094	0101110010001100 5C8C		INC	SR,DR,R3	TRK OR, SET SEEK
0158	0095	1010110010000000 AC80		LOD	I,A,128	TEST FOR READ OR COPY WRITE
0159	0096	0110110100011000 6D18		AND	SR,A,R6	
0160	0097	1011000111100011 B1E3		JZR	I,M,EX3	NO
0161	0098	0101100100110100 5934		LRA	R13	YES, SET COUNT = 128
0162	0099	1011111011100011 BEE3		JMP	I,M,EX3	
0163	009A	1010110000001000 AC08	EX8	LOD	I,A,8	PREPARE TO RCV BYTE
0164	009B	0101100100000100 5904		LRA	R1	FROM STACK
0165	009C	0000101011000000 0AC0		ESK		ENABLE STACK
0166	009D	0101110010110100 5CB4		INC	SR,DR,R13	INC INPUT COUNT
0167	009E	1110111111001101 EFCD		RLL	IN,A,SBH,SPSH	GET BIT FROM STACK
0168	009F	0101111110001000 5F88		RLC	SR,DR,R2	ROTATE BIT INTO BYTE REG R2
0169	00A0	0101001111000111 53C7		DEC	SR,DR,R1,EPSH	TEST FOR BYTE COMPLETE
0170	00A1	1011000001100001 B061		JNZ	I,M,*−3	NO, CONTINUE
0171	00A2	0110110000001000 6C08		LAR	R2	YES, BYTE TO ACC
0172	00A3	0000010111000000 05C0	E11	SFG		SET HOST FLAG HIGH
0173	00A4	1100110000001000 CC08		LOD	IN,L,CSW	TEST FOR STROBE HIGH
0174	00A5	1011100001011011 B85B		J2N	I,M,*−1	WAIT FOR HOST TO ACK
0175	00A6	1011111011100011 BEE3		JMP	I,M,EX3	
0176	00A7	0000010111000000 05C0	E10	SFG		LOOP BACK CMD
0177	00A8	1100110000011000 CC18		LOD	IN,L,BYT	INPUT HOST BYTE TO LTCHS
0178	00A9	0001000000111100 103C		LDL	R15	LTCHS TO R15
0179	00AA	0110110000111100 6C3C		LAR	R15	R15 to ACC: THIS IS A TEST
0180	00AB	1100110000001000 CC08		LOD	IN,L,CSW	TEST FOR STROBE HIGH
0181	00AC	1011100001010111 B857		J2N	I,M,*−4	LOOP UNTIL STROBE GOES HIGH
0182	00AD	1011111011100011 BEE3		JMP	I,M,EX3	RETURN TO EXEC SCAN LOOP. LOOPBACK ENDED
0183	00AE	0110110000000000 6C00	EX9	LAR	R0	DIAGNOSTIC READ EXECUTION (R(I) TO ACC)
0184	00AF	1011111001011100 BE5C		JMP	I,M,E11	
0185	00B0	0110110000000100 6C04		LAR	R1	
0186	00B1	1011111001011100 BE5C		JMP	I,M,E11	
0187	00B2	0110110000001000 6C08		LAR	R2	
0188	00B3	1011111001011100 BE5C		JMP	I,M,E11	

FLOPPY DISC MICROCODE (cont)

SEQ#	ADRS	BINARY-INSTRUCTION-HEX	LABEL	OP-CODE		
0189	00B4	0110110000001100 6C0C		LAR	R3	
0190	00B5	1011111001011100 BE5C		JMP	I,M,E11	
0191	00B6	0110110000010000 6C10		LAR	R4	
0192	00B7	1011111001011100 BE5C		JMP	I,M,E11	
0193	00B8	0110110000010100 6C14		LAR	R5	
0194	00B9	1011111001011100 BE5C		JMP	I,M,E11	
0195	00BA	0110110000011000 6C18		LAR	R6	
0196	00BB	1011111001011100 BE5C		JMP	I,M,E11	
0197	00BC	0110110000011100 6C1C		LAR	R7	
0198	00BD	1011111001011100 BE5C		JMP	I,M,E11	
0199	00BE	0110110000100000 6C20		LAR	R8	
0200	00BF	1011111001011100 BE5C		JMP	I,M,E11	
0201	00C0	0110110000100100 6C24		LAR	R9	
0202	00C1	1011111001011100 BE5C		JMP	I,M,E11	
0203	00C2	0110110000101000 6C28		LAR	R10	
0204	00C3	1011111001011100 BE5C		JMP	I,M,E11	
0205	00C4	0110110000101100 6C2C		LAR	R11	
0206	00C5	1011111001011100 BE5C		JMP	I,M,E11	
0207	00C6	0110110000110000 6C30		LAR	R12	
0208	00C7	1011111001011100 BE5C		JMP	I,M,E11	
0209	00C8	0110110000110100 6C34		LAR	R13	
0210	00C9	1011111001011100 BE5C		JMP	I,M,E11	
0211	00CA	0110110000111000 6C38		LAR	R14	
0212	00CB	1011111001011100 BE5C		JMP	I,M,E11	
0213	00CC	0110110000111100 6C3C		LAR	R15	
0214	00CD	1011111001011100 BE5C		JMP	I,M,E11	
0215	00CE	1010110001010011 AC53		LOD	I,A,EX9-2	
0216	00CF	0101100100110100 5934		LRA	R13	
0217	00D0	0101001111110100 53F4	E9B	DEC	SR,DR,R13	UPDATE R13 WITH NEXT REG OUTPUT VECTOR
0218	00D1	0101001111110100 53F4		DEC	SR,DR,R13	THIS TAKES TWO DEC'S
0219	00D2	0111111000110100 7E34		JMP	SR,M,R13	GO OUTPUT R(I) TO ACC
0220	00D3	0101001111001100 53CC	SEEK	DEC	SR,DR,R3	SEEK = SEEK-1
0221	00D4	1011101011100011 BAE3		JLB	I,M,EX3	JMP TO EXEC IF SEEK # 0
0222	00D5	0110110000101100 6C2C	S0	LAR	R11	TEST FOR TRACKX = 00
0223	00D6	1011000100100000 B120		JZR	I,M,SK0	YES, SEE IF HEAD AT TRACK 00
0224	00D7	0100110010101000 4CA8		INC	SR,L,R10	TEST FOR TRACKN = −1
0225	00D8	1011000000011101 B01D		JNZ	I,M,S1	NO, GO COMPARE TRACKN, TRACKX

FLOPPY DISC MICROCODE (cont)

SEQ#	ADRS	BINARY-INSTRUCTION-HEX		LABEL	OP-CODE		
0226	00D9	0110110000011000	6C18		LAR	R6	TEST FOR WRITE UNFORMATTED
0227	00DA	1011101000100000	BA20		JLB	I,M,SK0	YES, SEEK TO TRACK 00
0228	00DB	0101110010001100	5C8C		INC	SR,DR,R3	SET SEEK = 1
0229	00DC	1010110001000000	AC40		LOD	I,A,64	SET GTID1 = 1
0230	00DD	0101100000001100	580C	S0R	OR	SR,DR,R3	
0231	00DE	1011111011100011	BEE3		JMP	I,M,EX3	RETURN TO EXEC SCAN LOOP
0232	00DF	1100111111001000	CFC8	SK0	RLL	IN,L,CSW	TEST TRACK 00 STATUS BIT
0233	00E0	1011011100010101	B715		JZC	I,M,S3+1	NO, GO CONTINUE/SET UP OUTWARD SEEK
0234	00E1	0101111100101000	5F28		LRZ	R10	YES, SET TRACKN = 0
0235	00E2	0110110000101100	6C2C	S1	LAR	R11	TEST FOR TRACKN = TRACKX
0236	00E3	0110010110101000	65A8		SUB	SR,A,R10	TEST BY SUBTRACTING TO DETECT DIRECTION
0237	00E4	1011000100000101	B105		JZR	I,M,S5	YES, TEST ERROR RECOVERY STATE
0238	00E5	1011011000010110	B616		JNC	I,M,S3	NO, SEEK OUT, TOWARD TRACK 00
0239	00E6	0000101001000000	0A40		DRI		NO, SEEK IN, TOWARD TRACK 76
0240	00E7	0101110010101000	5CA8		INC	SR,DR, R10	INC TRACKN
0241	00E8	1011111000010100	BE14		JMP	I,M,S4	GO TO STEP ROUTINE
0242	00E9	0101001111101000	53E8	S3	DEC	SR,DR,R10	DEC TRACKN, SEEK OUT
0243	00EA	0000100001000000	0840		DRO		SET DIR OUT
0244	00EB	0101110010001100	5C8C	S4	INC	SR,DR,R3	
0245	00EC	0110110000101100	6C2C		LAR	R11	TEST FOR TRACKN = TRACKX
0246	00ED	0110010110101000	65A8		SUB	SR,A,R10	YES, SEEK = 01
0247	00EE	1011000100001111	B10F		JZR	I,M,*+2	NO, SEEK = 10
0248	00EF	0101110010001100	5C8C		INC	SR,DR,R3	
0249	00F0	1010110000010001	AC11		LOD	I,A,17	SET UP COUNTER FOR A 10 MICROSECOND DELAY
0250	00F1	0101100100000100	5904		LRA	R1	
0251	00F2	0000101010000000	0A80		SSP		SET STEP
0252	00F3	0101001111000100	53C4		DEC	SR,DR,R1	WAIT FOR STEP PULSE WIDTH DELAY
0253	00F4	1011000000001100	B00C		JNZ	I,M,*−1	
0254	00F5	0000100010000000	0880		RSP		RESET STEP
0255	00F6	0100111111011000	4FD8		RLL	SR,L,R6	TEST FOR WRITE FORMATTED
0256	00F7	1011100111100011	B9E3		J2Z	I,M,EX3	NO, RETURN TO EXEC
0257	00F8	1010110010000000	AC80		LOD	I,A,128	YES, SET GTID2 = 1 IN ACC
0258	00F9	1011111000100010	BE22		JMP	I,M,S0R	
0259	00FA	0000101111000000	0BC0	S5	SHB		
0260	00FB	1011111011100001	BEE1		JMP	I,M,STCK	
0261	00FC	0000011110000000	0780	PNT	SPT		SET PRINT STROBE

FLOPPY DISC MICROCODE (cont)

SEQ#	ADRS	BINARY-INSTRUCTION-HEX		LABEL	OP-CODE		
0262	00FD	1011111000000001	BE01		JMP	I,M,*+1	PRINT STROBE DELAY
0263	00FE	0000010110000000	0580		RPT		RESET PRINT STROBE
0264	00FF	1011111001011100	BE5C		JMP	I,M,E11	GO TO SET FLAG
0266	0100				ALIGN	256	
0267	0100	0110110000001100	6C0C	X	LAR	R3	LOAD FLAGS
0268	0101	1011010011110001	B4F1		J4N	I,M,ERN	ERROR FLAG ON, GO RESET ERROR RECOVERY
0269	0102	1011100011111001	B8F9		J2N	I,M,*+4	ERROR STATE ON, TAKE RECOVERY ACTION
0270	0103	1010100000000100	A804		OR	I,A,4	SET STATE FLAG ON
0271	0104	0101100100001100	590C		LRA	R3	
0272	0105	1011111001011110	BE5E		JMP	I,M,X4	GO TO COMMON EXEC RETURN
0273	0106	1010110000000101	AC05		LOD	I,A,5	STATE FLAG ON, WIPING ACTION REQUIRED
0274	0107	0101100100001100	590C		LRA	R3	SET GTID1 = 0 SEEK = 1
0275	0108	0110110000101100	6C2C		LAR	R11	SAVE TRACKX IN CRC1 REG (TEMP)
0276	0109	0101100100111000	5938		LRA	R14	
0277	010A	0101111100101100	5F2C		LRZ	R11	SET TARGET TRACK (X) TO 00
0278	010B	0101000011101000	50E8		LRM	R10	SET TRACKN = −1 (UNKNOWN)
0279	010C	0000011010000000	0680		SER		SET ERROR RECOVERY IN STATUS BYTE
0280	010D	1011111001011110	BE5E		JMP	I,M,X4	GO TO COMMON EXEC RETURN
0281	010E	0000010010000000	0480	ERN	RER		RESET ERROR RECOVERY IN STATUS BYTE
0282	010F	0101111100001100	5F0C	X3	LRZ	R3	RESET ALL FLAGS
0283	0110	0101111100110100	5F34		LRZ	R13	SET COUNT = 0
0284	0111	1010110000010100	AC14		LOD	I,A,20	SET DELAY = 20
0285	0112	0101100100010100	5914		LRA	R5	
0286	0113	0101110010100100	5CA4		INC	SR,DR,R9	INC SECTX (TARGET)
0287	0114	1010110000011111	AC1F		LOD	I,A,31	MASK OFF HIGHER BITS, TEST FOR ROLLOVER
0288	0115	0101110100100100	5D24		AND	SR,DR,R9	
0289	0116	1011000011001111	B0CF		JNZ	I,M,X1A	NO, GO TO COMMON EXEC RETURN
0290	0117	0101110010101100	5CAC		INC	SR,DR,R11	YES, ONC TRACKX (TARGET)
0291	0118	1010110001001101	AC4D		LOD	I,A,77	TEST FOR LAST TRACK
0292	0119	0110010110101100	65AC		SUB	SR,A,R11	
0293	011A	1011000011001111	B0CF		JNZ	I,M,X1A	NO, GO TO SET SEEK AND RETURN TO EXEC
0294	011B	1010110000001000	AC08		LOD	I,A,8	SET PHYSICAL END OF FILE IN PROG FLG BYTE
0295	011C	0101100000001100	580C		OR	SR,DR,R3	

@

FLOPPY DISC MICROCODE (cont)

SEQ#	ADRS	BINARY-INSTRUCTION-HEX		LABEL	OP-CODE		
0296	011D	1011111001011110	BE5E		JMP	I,M,X4	SET SEEK AND RETURN TO EXEC
0297	011E	0110110000001100	6C0C	STCK	LAR	R3	CHECK MACHINE STATE
0298	011F	1011100011011000	B8D8		J2N	I,M,X1	GO COMPLETE ERROR RECOVERY
0299	0120	0100111111001100	4FCC		RLL	SR,L,R3	TEST GTID2 = 1
0300	0121	1011011001011110	B65E		JNC	I,M,X4	YES, GO CHECK ID
0301	0122	0110110000011000	6C18		LAR	R6	NO, IS IT A WRITE COMMAND?
0302	0123	1011100101011110	B95E		J2Z	I,M,X4	NO, RETURN TO EXEC
0303	0124	1010110000100000	AC20		LOD	I,A,32	YES, SET GTCRC = 1
0304	0125	0101100000001100	580C		OR	SR,DR,R3	
0305	0126	1011111001011110	BE5E		JMP	I,M,X4	GO CALCULATE CRC
0306	0127	1011010011010011	B4D3	X1	J4N	I,M,*+5	YES RESTORE TRACKX
0307	0128	1000110001001100	8C4C		LOD	I,L,76	NO, SET TRACKX = 76
0308	0129	0001000000101100	102C		LDL	R11	
0309	012A	1010100000010000	A810		OR	I,A,16	SET ERROR FLAG = 1
0310	012B	1011111011010000	BED0		JMP	I,M,*+4	GO UPDATE PROG FLG BYTE AND RETURN TO EXEC
0311	012C	0100110000111000	4C38		LOD	SR,L,R14	ERROR FLAG ON, RESTORE TARGET TRACK (X)
0312	012D	0001000000101100	102C		LDL	R11	
0313	012E	1010110111111000	ADF8		AND	I,A,248	RESET ERROR RECOVERY STATE
0314	012F	0101100100001100	590C		LRA	R3	UPDATE PRG FLG BYTE
0315	0130	0101110010001100	5C8C	X1A	INC	SR,DR,R3	SET SEEK = 1
0316	0131	1011111001011110	BE5E		JMP	I,M,X4	GO TO COMMON RETURN TO EXEC
0317	0132	0000010010000000	0480	X2	RER		RESET ERROR RECOVERY STATUS
0318	0133	0000010011000000	04C0		RCK		RESET UNIT CHECK STATUS
0319	0134	1010110011000000	ACC0		LOD	I,A,192	TEST GTID1 OR GTID2
0320	0135	0100110100001100	4D0C		AND	SR,L,R3	
0321	0136	1011000111110000	B1F0		JZR	I,M,X3	BOTH BITS ZERO. GO TO CLEANUP
0322	0137	1011001111000101	B3C5		J6Z	I,M,*+3	GTID1 = 0, GO RESET GTID2
0323	0138	1010110010100011	ACA3		LOD	I,A,163	SET GTID1, ERRFLG, ERRSTE = 0
0324	0139	1011111011000100	BEC4		JMP	I,M,*+2	
0325	013A	1010110000100011	AC23		LOD	I,A,35	SET GTID2, ERRFLG AND ERRSTE = 0
0326	013B	0101110100001100	5D0C		AND	SR,DR,R3	RESET APPROPRIATE FLAG BITS
0327	013C	1011111011001111	BECF		JMP	I,M,X1A	
0328	013D	0110111111001100	6FCC	RD	RLL	SR,A,R3	TEST FLAG WORD FOR END OF DISC

FLOPPY DISC MICROCODE (cont)

SEQ#	ADRS	BINARY-INSTRUCTION-HEX		LABEL	OP-CODE		
0329	013E	1011010001011110	B45E		J4N	I,M,X4	RETURN TO EXEC ILLEGAL OP IS ON
0330	013F	0000101101000000	0B40		RDC		SET CARRY TO SECTR BUFF SWITCH
0331	0140	0000010101000000	0540		RWR		RESET WRITE GATE (SHOULD BE OFF)
0332	0141	1011001001011100	B25C		J6N	I,M,ICRC	
0333	0142	0100111111010100	4FD4		RLL	SR,L,R5	TEST FOR HEAD DOWN
0334	0143	1011011001011110	B65E		JNC	I,M,RTN+2	50 MS DELAY, GO TO EXEC
0335	0144	1011000010111000	B0B8		JNZ	I,M,*+3	BY PASS RETURN, HEAD IS DOWN
0336	0145	0000100111000000	09C0		SLB		SWITCH TO LOWER BANK
0337	0146	1011111011100111	BEE7		JMP	I,M,EX2	GO TO LOWER HEAD ROUTINE
0338	0147	0101111100000100	5F04		LRZ	R1	INIT DESERIALIZING REG R1
0339	0148	0101111100001000	5F08		LRZ	R2	INIT BIT COUNT REG R2
0340	0149	1010110011111011	ACFB		LOD	I,A,SYNC	PUT SYNC BYTE 'FB' IN ACC
0341	014A	0000100011000000	08C0		DSK		DISABLE SECTOR BUFFER
0342	014B	1011110110110100	BDB4	RD1	JNR	I,M,*	WAIT FOR DATA READY
0343	014C	1100111110010101	CF95		RLC	IN,L,DBT,SPSH	DATA BIT TO CARRY, CLEAR DATA READY
0344	014D	0101111110000100	5F84		RLC	SR,DR,R1	CARRY TO LSB OF R1
0345	014E	0100101000000111	4A07		XOR	SR, L,R1 ,EPSH	COMPARE BYTE WITH 'FB', DROP SB CLOCK
0346	014F	1011000110101011	B1AB		JZR	I,M,RD2−2	FOUND SYNC, GO GET TRACK/ SECTOR
0347	0150	0101110010001000	5C88		INC	SR,DR,R2	INC R2
0348	0151	1011000010110100	B0B4		JNZ	I,M,RD1	CONTINUE SEARCH FOR HEADER
0349	0152	1010110000001000	AC08		LOD	I,A,8	LOAD ACC WITH SYNC ERROR BIT MASK
0350	0153	1011111001100101	BE65		JMP	I,M,ERTN−1	GO TO ERTN−1 TO 'OR' IN SYNC ERROR BIT
0351	0154	0101111100000000	5F00		LRZ	R0	
0352	0155	0101000011000100	50C4		LRM	R1	INIT BIT CNTR TO 1'S
0353	0156	1011110110101001	BDA9	RD2	JNR	I,M,*	WAIT FOR DATA RDY
0354	0157	1100111110010101	CF95		RLC	IN,L,DBT,SPSH	INPUT DATA TO CARRY, START PUSH
0355	0158	0101111110101000	5FA8		RLC	SR,DR,R10	SHIFT BIT INTO TRACK N
0356	0159	0101111111000111	5FC7		RLL	SR,DR,R1,EPSH	TEST BIT CNTR FOR FINISH
0357	015A	1011000010101001	B0A9		JNZ	I,M,RD2	NO, CONTINUE DESERIALIZING TRACK BYTE

FLOPPY DISC MICROCODE (cont)

SEQ#	ADRS	BINARY-INSTRUCTION-HEX		LABEL	OP-CODE		
0358	015B	0101000011000100	50C4		LRM	R1	TRACK ASSEMBLED, INIT BIT CNTR
0359	015C	0110110000001100	6C0C		LAR	R3	GTID1 = 1?
0360	015D	1011001010011100	B29C		J6N	I,M,RD3	YES, SKIP TRACK VERIFICATION
0361	015E	0110110000101100	6C2C		LOD	SR,A,R11	NO, VERIFY TRACKN = TRACKX
0362	015F	0100101000101000	4A28		XOR	SR,L,R10	
0363	0160	1011000110011100	B19C		JZR	I,M,RD3	MTCH OK, GO TO SECTOR READ
0364	0161	1010110000010000	AC10	RIDE	LOD	I,A,16	PUT ID ERROR IN R0
0365	0162	0101100000000000	5800		OR	SR,DR,R0	
0366	0163	1011110110011100	BD9C	RD3	JNR	I,M,*	WAIT FOR DATA RDY
0367	0164	1100111110010101	CF95		RLC	IN,L,DBT,SPSH	INPUT DATA TO CARRY, START PUSH
0368	0165	0101111110001000	5F88		RLC	SR,DR,R2	SHIFT BIT INTO R2
0369	0166	0101111111000111	5FC7		RLL	SR,DR,R1,EPSH	TEST BIT CNTR FOR FINISH
0370	0167	1011000010011100	B09C		JNZ	I,M,RD3	NO, CONTINUE DESERIALIZING SECTOR BYTE
0371	0168	1010110011000000	ACC0		LOD	I,A,192	PUT GTID1, GTID2 MASK INTO ACC
0372	0169	0100110100001100	4D0C		AND	SR,L,R3	MASK OUT ALL BUT GTID1, GTID2
0373	016A	1011000010001110	B08E		JNZ	I,M,RD4A	GO TO READ WITHOUT SECTOR COMPARE
0374	016B	0110110000001000	6C08		LAR	R2	TEST FOR R2 + SECTORX (TARGET)
0375	016C	0100101000100100	4A24		XOR	SR,L,R9	
0376	016D	1011000110001111	B18F		JZR	I,M,*+3	GO TO ID ERROR
0377	016E	1010110000010000	AC10		LOD	I,A,16	
0378	016F	0101100000000000	5800		OR	SR,DR,R0	SET ID ERROR IN R0
0379	0170	0000101011000000	0AC0		ESK		ENABLE STACK
0380	0171	1010110001101011	AC6B	RD4A	LOD	I,A,FNRD	LOAD FINISH READ RETURN ADDRESS IN R12
0381	0172	0101100100110000	5930		LRA	R12	
0382	0173	0110110000101000	6C28		LAR	R10	TRACK N TO CRC1; INITIAL VALUE
0383	0174	0101100100111000	5938	RD4	LRA	R14	
0384	0175	0110110000001000	6C08		LAR	R2	SECTOR BYTE READ TO CRC2; INITIAL VALUE
0385	0176	0101100100111100	593C		LRA	R15	
0386	0177	0101111100000100	5F04		LRZ	R1	INIT TO ZERO, SECTOR BUFF CNTRS R1,R2
0387	0178	0101111100001000	5F08		LRZ	R2	
0388	0179	1011111010000001	BE81		JMP	I,M,SBLP	

FLOPPY DISC MICROCODE (cont)

SEQ#	ADRS	BINARY-INSTRUCTION-HEX		LABEL	OP-CODE		
0389	017A	0111101000110000	7A30		JLB	SR,M,R12	RETURN VIA REG TO READ OR WRITE CALLER
0390	017B	0000100011000000	08C0		DSK		DISABLE STACK, PREPARE TO PROCESS 16 0's
0391	017C	1010110011110000	ACF0		LOD	I,A,240	−16 TO INNER COUNT (R1)
0392	017D	0101100100000100	5904		LRA	R1	
0393	017E	0100111111001100	4FCC	SBLP	RLL	SR,L,R3	TEST GETCRC = 1
0394	017F	1011001001110001	B271		J6N	I,M,CRC	TO GET NEXT DATA BIT FOR CRC GEN
0395	0180	1011110101111111	BD7F		JNR	I,M,*	CRC CHECKING, WAIT FOR READ DATA
0396	0181	1100111110010101	CF95		RLC	IN,L,DBT,SPSH	DATA BIT TO BUFFER
0397	0182	0101111110111100	5FBC	CRC2	RLC	SR,DR,R15	DATA BIT TO CRC2, LEFT ROTATED
0398	0183	0101111110111011	5FBB		RLC	SR,DR,R14,EPSH	MSB CRC2 TO LSR CRC1
0399	0184	1011011101110110	B776		JZC	I,M,*+5	NO CARRY, CORRECTION NOT REQUIRED
0400	0185	1010110000010000	AC10		LOD	I,A,MSK1	CORRECTION MASK FOR CRC1
0401	0186	0101101000111000	5A38		XOR	SR,DR,R14	CORRECT CRC1
0402	0187	1010110000100001	AC21		LOD	I,A,MSK2	CORRECTION MASK FOR CRC2
0403	0188	0101101000111100	5A3C		XOR	SR,DR,R15	CORRECT CRC2
0404	0189	0101110010000100	5C84		INC	SR,DR,R1	INCREMENT THE DOUBLE WORD COUNT
0405	018A	1011000010000001	B081		JNZ	I,M,SBLP	CONTINUE, FIRST BYTE HASN'T ROLLED OVER
0406	018B	0101110010001000	5C88		INC	SR,DR,R2	FIRST BYTE ROLLED OVER INC SECOND BYTE
0407	018C	1011100010000101	B885		J2N	I,M,SBLP−4	DBLE CNT G.E. 1024 FINISH CALC WITH 0'S
0408	018D	1011111010000001	BE81		JMP	I,M,SBLP	CONTINUE CRC CALC, SECTOR INCOMPLETE
0409	018E	0100110000001000	4C08	CRC	LOD	SR,L,R2	TEST FOR CRC CALC ZERO FLUSH (16 0'S)
0410	018F	1011100001101101	B86D		J2N	I,M,*+3	YES DATA BIT = 0
0411	0190	1100111110001101	CF8D		RLC	IN,L,SBH,SPSH	NO, TAKE DATA FROM SECTOR BUFFER
0412	0191	1011111001111101	BE7D		JMP	I,M,CRC2	GO CALC CRC2
0413	0192	0100111110001000	4F88		RLC	SR,L,R2	SET CARRY TO ZERO FOR CRC ZERO FLUSH

FLOPPY DISC MICROCODE (cont)

SEQ#	ADRS	BINARY-INSTRUCTION-HEX	LABEL	OP-CODE		
0414	0193	1011111001111101 BE7D		JMP	I,M,CRC2	GO CALC CRC
0415	0194	0110110000000000 6C00	FNRD	LAR	R0	TEST R0 FOR ID ERROR
0416	0195	1011010001100100 B464		J4N	I,M,ERTN	YES, GO TO SET UNIT CHECK
0417	0196	0110110000111000 6C38		LOD	SR,A,R14	TEST FOR CRC1, CRC2 = 0 (NO DATA ERRORS)
0418	0197	0100100000111100 483C		OR	SR,L,R15	
0419	0198	1011000111001101 B1CD		JZR	I,M,X2	NO ERRORS, GO TO SUCCESSFUL RETURN
0420	0199	1010110000100000 AC20		LOD	I,A,32	SET CRC ERROR IN SENSE BYTE
0421	019A	0101100000000000 5800		OR	SR,DR,R0	
0422	019B	0000011011000000 06C0	ERTN	SCK		SET UNIT CHECK
0423	019C	0110110000010000 6C10		LAR	R4	RECOVER ERROR
0424	019D	1011001011101111 B2EF		J6N	I,M,X3+1	NO, GO TO CONTINUE
0425	019E	1011111011111111 BEFF		JMP	I,M,X	GO TO ERROR RECOVERY
0426	019F	1010110011011111 ACDF	RTN	LOD	I,A,223	SET GETCRC = 0
0427	01A0	0101110100001100 5D0C		AND	SR,DR,R3	
0428	01A1	0000100111000000 09C0	X4	SLB		SET LOWER BANK
0429	01A2	1011111011100011 BEE3		JMP	I,M,EX3	JUMP TO LOWER BANK
ICRC						
0431	* ICRC IS USED TO INITIALIZE FOR THE CRC ROUTINE (STACK, CRC1&2, RET REG)					
CRC	E					
0433	01A3	0000101011000000 0AC0	ICRC	ESK		ENABLE STACK
0434	01A4	0110110000100100 6C24		LAR	R9	SECTX TO R2
0435	01A5	0101100100001000 5908		LRA	R2	
0436	01A6	1010110001100000 AC60		LOD	I,A,RTN	LOAD RETURN VECTOR
0437	01A7	0101100100110000 5930		LRA	R12	IN R12
0438	01A8	0110110000101100 6C2C		LAR	R11	TRACKX TO ACC (TO BE PUT IN CRC1)
0439	01A9	1011111010001100 BE8C		JMP	I,M,RD4−1	GO CALC CRC
0440	01AA	1010110010000000 AC80	WRT	LOD	I,A,128	PREPARE TO SEND ONE CLOCK PULSE
0441	01AB	0000101011000000 0AC0		ESK		ENABLE STACK
0442	01AC	0101100100110000 5930		LRA	R12	SET CLOCK OUTPUT BYTE FOR ONE BIT
0443	01AD	0101111100000100 5F04		LRZ	R1	SET DATA OUTPUT BYTE TO ZERO
0444	01AE	1010110000001111 AC0F		LOD	I,A,15	LOAD BTYE COUNT TO 15 (120 BITS FOR CLK)
0445	01AF	0101100100001000 5908		LRA	R2	PUT IN R2
0446	01B0	1010110001001011 AC4B		LOD	I,A,WRT1	SET DOUT RETURN VECTOR TO WRT1
0447	01B1	0101100100010100 5914		LRA	R5	PUT IN R5
0448	01B2	1010110001000101 AC45		LOD	I,A,WRT2	FUTURE RETURN VECTOR (WRT2) IN ACC

FLOPPY DISC MICROCODE (cont)

SEQ#	ADRS	BINARY-INSTRUCTION-HEX		LABEL	OP-CODE		
0449	01B3	1011111000111110	BE3E		JMP	I,M,DOUT	OUTPUT THE 120 BIT CLOCK PREAMBLE
0450	01B4	0101100100010100	5914	WRT1	LRA	R5	SET DOUT RETURN VECTOR TO WRT2
0451	01B5	0000000000000000	0000		NOP		NEED 10 CYCLES IN THIS SEQUENCE OF CODE
0452	01B6	0000011101000000	0740		SWR		SET WRITE GATE
0453	01B7	0101000011110000	50F0		LRM	R12	SET CLOCK OUTPUT BYTE TO EIGHT
0454	01B8	0101111111110000	5FF0		RLL	SR,DR,R12	DROP ONE SINCE INITIAL BIT WAS SENT
0455	01B9	1011111000111110	BE3E		JMP	I,M,DOUT	GO OUTPUT PREAMBLE OF 120 ZEROS
0456	01BA	1010110000110010	AC32	WRT2	LOD	I,A,WRT3	LOAD ACC WITH RETURN VECTOR WRT3
0457	01BB	0101000011110000	50F0		LRM	R12	SET CLOCK OUTPUT BYTE TO EIGHT
0458	01BC	0101001111001000	53C8		DEC	SR,DR,R2	DEC LOOP COUNT
0459	01BD	1011000001000110	B046		JNZ	I,M,*−4	GO TO DOUT, SEND NEXT BYTE
0460	01BE	0101100100010100	5914		LRA	R5	SET DOUT RETURN VECTOR TO WRT3
0461	01BF	1010110011111011	ACFB		LOD	I,A,SYNC	
0462	01C0	0101100100000100	5904		LRA	R1	SET DATA OUTPUT BYTE TO FB
0463	01C1	0101111111000110	5FC6	DOUT	RLL	SR,DR,R1,PULL	SEND DATA BIT OUT
0464	01C2	1011111000111100	BE3C		JMP	I,M,*+1	400 NS DELAY PER EXECUTED JUMP
0465	01C3	1011111000111011	BE3B		JMP	I,M,*+1	
0466	01C4	1011111000111010	BE3A		JMP	I,M,*+1	
0467	01C5	1011111000111001	BE39		JMP	I,M,*+1	
0468	01C6	0000000000000000	0000		NOP		200 NS DELAY
0469	01C7	0101111111110010	5FF2		RLL	SR,DR,R12,PULL	SEND CLOCK BIT
0470	01C8	0111000100010100	7114		JZR	SR,M,R5	TEST FOR FINISH
0471	01C9	1011111000110101	BE35		JMP	I,M,*+1	400 NS DELAY
0472	01CA	1011111000110100	BE34		JMP	I,M,*+1	
0473	01CB	1011111000110011	BE33		JMP	I,M,*+1	
0474	01CC	1011111000111110	BE3E		JMP	I,M,DOUT	CONTINUE SENDING DATA
0475	01CD	1010110000101100	AC2C	WRT3	LOD	I,A,WRT4	SET DOUT RETURN VECTOR TO WRT4
0476	01CE	0101100100010100	5914		LRA	R5	
0477	01CF	0110110000101100	6C2C		LAR	R11	TRACKX TO ACC

FLOPPY DISC MICROCODE (cont)

SEQ#	ADRS	BINARY-INSTRUCTION-HEX		LABEL	OP-CODE		
0478	01D0	0101100100000100	5904		LRA	R1	TRACKX TO DATA OUTPUT BYTE
0479	01D1	0101000011110000	50F0		LRM	R12	SET CLOCK OUTPUT BYTE TO EIGHT
0480	01D2	1011111000111110	BE3E		JMP	I,M,DOUT	GO TO OUTPUT THE TRACK BYTE
0481	01D3	1010110000100110	AC26	WRT4	LOD	I,A,WRT5	SET DOUT RETURN VECTOR TO WRT5
0482	01D4	0101100100010100	5914		LRA	R5	
0483	01D5	0110110000100100	6C24		LAR	R9	SECTX TO ACC
0484	01D6	0101100100000100	5904		LRA	R1	SECTX TO DATA OUTPUT BYTE
0485	01D7	0101000011110000	50F0		LRM	R12	SET CLOCK OUTPUT BYTE TO EIGHT
0486	01D8	1011111000111110	BE3E		JMP	I,M,DOUT	GO TO OUTPUT THE SECTOR BYTE
0487	01D9	0000000000000000	0000	WRT5	NOP		NEED A 600 NS DELAY PRECEDING WRT5B
0488	01DA	1011111000100001	BE21		JMP	I,M,*+4	
0489	01DB	0101110010001000	5C88	WRT5A	INC	SR,DR,R2	INC LOOP COUNT (ZERO UPON ENTRY)
0490	01DC	0100111111001000	4FC8		RLL	SR,L,R2	TEST FOR 128 ITERATIONS (1 BYTE EACH)
0491	01DD	1011011000010001	B611		JNC	I,M,WRT6	SECTOR DATA WRITTEN, GO WRITE CRC
0492	01DE	0101000011110000	50F0		LRM	R12	SET CLOCK OUTPUT BYTE TO EIGHT
0493	01DF	1010110000001111	AC0F	WRT5B	LOD	I,A,WRT7	SET DOUT RETURN VECTOR TO WRT7
0494	01E0	0101100100010100	5914		LRA	R5	
0495	01E1	1100111110001101	CF8D		RLC	IN,L,SBH,SPSH	RECIRCULATE SECTOR BUFFER START PUSH
0496	01E2	1100111110001110	CF8E		RLC	IN,L,SBH,PULL	SEND DATA BIT
0497	01E3	0110110000111000	6C38		LAR	R14	CRC1 TO DATA OUTPUT BYTE
0498	01E4	0101100100000111	5907		LRA	R1,EPSH	AND END PUSH
0499	01E5	1011111000011001	BE19		JMP	I,M,*+1	400 NS DELAY
0500	01E6	1011111000011000	BE18		JMP	I,M,*+1	
0501	01E7	1011111000010111	BE17		JMP	I,M,*+1	
0502	01E8	0000000000000000	0000		NOP		200 NS DELAY
0503	01E9	0101111111110010	5FF2		RLL	SR,DR,R12,PULL	SEND CLOCK BIT
0504	01EA	1011000100100100	B124		JZR	I,M,WRT5A	GO TO INIT FOR NEXT BYTE, IF REQUIRED

FLOPPY DISC MICROCODE (cont)

SEQ#	ADRS	BINARY-INSTRUCTION-HEX		LABEL	OP-CODE		
0505	01EB	1011111000010011	BE13		JMP	I,M,*+1	400 NS DELAY
0506	01EC	0000000000000000	0000		NOP		200 NS DELAY
0507	01ED	1011111000100000	BE20		JMP	I,M,WRT5B	CONTINUE SENDING CURRENT BYTE
0508	01EE	0101000011110000	50F0	WRT6	LRM	R12	CRC2 TO ACC
0509	01EF	1011111000111110	BE3E		JMP	I,M,DOUT	GO SEND CRC1 BYTE, (IN DATA OUT BYTE REG)
0510	01F0	0110110000111100	6C3C	WRT7	LAR	R15	CRC2 TO ACC
0511	01F1	0101100100000100	5904		LRA	R1	PUT IN DATA OUTPUT BYTE
0512	01F2	1010110000001001	AC09		LOD	I,A,WRT8	SET DOUT RETURN VECTOR TO WRT9
0513	01F3	0101100100010100	5914		LRA	R5	
0514	01F4	0101000011110000	50F0		LRM	R12	SET CLOCK OUTPUT BYTE TO EIGHT
0515	01F5	1011111000111110	BE3E		JMP	I,M,DOUT	GO SEND CRC BYTE
0516	01F6	1010110010000000	AC80	WRT8	LOD	I,A,128	SET CLOCK OUTPUT BYTE TO 1
0517	01F7	0101100100110000	5930		LRA	R12	
0518	01F8	1100110000001000	CC08		LOD	IN,L,CSW	INPUT CURRENT CSW
0519	01F9	1011010000000011	B403		J4N	I,M,WEND	SECTOR MASK DETECTED, GO TO FINISH
0520	01FA	0000000000000000	0000		NOP		200 NS DELAY
0521	01FB	1011111000111110	BE3E		JMP	I,M,DOUT	GO SEND ANOTHER CLOCK FOR POSTAMBLE
0522	01FC	1010110011101111	ACEF	WEND	LOD	I,A,'HEF	
0523	01FD	0101110100100000	5D20		AND	SR,DR,R8	
0524	01FE	0000010101000000	0540		RWR		
0525	01FF	1011111011001101	BECD		JMP	I,M,X2	
0526					END		

TOTAL ERRORS = 0000

SYMBOL	VAL/ADRS	SEQ. DEFN	SEQ. REFERENCES		(PAGE 001)			
ALIGN	.....	....	0266					
CNT	0006	0015	0018					
CRC	018E	0409	0394					
CRC2	1082	0397	0412	0414				
DOUT	01C1	0463	0515	0521				
			0449	0455	0474	0480	0486	0509
DRV	0075	0126	0120					
DTA	0084	0141	0116	0117				
E10	00A7	0176	0124					
E11	00A3	0172	0184	0186	0188	1090	0192	0194
			0196	0198	0200	0202	0204	0206
			0208	0210	0212	0214	0264	
E4A	003D	0070	0065	0067				
E5A	0058	0097	0054	0055	0057	0060		
E6A	0062	0107	0046	0100	0140			
E6B	0066	0111	0101					
E9B	00D0	0217	0110	0125				
ERN	010E	0281	0268					
ERTN	019B	0422	0350	0416				
EX1	0014	0029	0129					
EX2	0018	0033	0131	0337				
EX2A	0017	0032	—					
EX3	001C	0037	0083	0084	0090	0098	0106	0123
			0132	0135	0138	0150	0160	0162
			0175	0182	0221	0231	0256	0429
EX4	0034	0061	0051					
EX5	0043	0076	0071					
EX6	0059	0098	0061					
EX7	008E	0151	0114					
EX8	009A	0163	0109					
EX9	00AE	0183	0215					
EXEC	0000	0009	—'					
FNRD	0194	0415	0380					
GRD	0056	0095	0077	0081	0086	0092		
GWRT	0054	0093	—					
ICRC	01A3	0433	0332					
ILOP	0082	0139	0087	0156				
MSK1	FFEF	0006	0400					
MSK2	FFDE	0007	0402					
PNT	00FC	0261	0107					
RD	013D	0328	0096					
RD1	014B	0342	0348					
RD2	0156	0353	0346	0357				

SYMBOL	VAL/ADRS	SEQ. DEFN	SEQ. REFERENCES		(PAGE 002)			
RD3	0163	0366	0360	0363	0370			
RD4	0174	0383	0439					
RD4A	0171	0380	0373					
RIDE	0161	0364	—					
RTN	019F	0426	0334	0436				
S0	00D5	0222	—					
S1	00E2	0235	0225					
S3	00E9	0242	0233	0238				
S4	00EB	0244	0241					
S5	00FA	0259	0237					
SBLP	017E	0393	0388	0405	0407	0408		
SCT	007F	0136	0119					
SEEK	00D3	0220	0079					
SK0	00DF	0232	0223	0227				
SOR	00DD	0230	0258					
STCK	011E	0297	0260					
SYNC	FF04	0005	0340	0461				
WEND	01FC	0522	0519					
WRT	01AA	0440	0094					
WRT1	01B4	0450	0446					
WRT2	01BA	0456	0448					
WRT3	01CD	0475	0456					
WRT4	01D3	0481	0475					
WRT5	01D9	0487	0481					
WRT5A	01DB	0489	0504					
WRT5B	01DF	0493	0507					
WRT6	01EE	0508	0491					
WRT7	01F0	0510	0493					
WRT8	01F6	0516	0512					
X	0100	0267	0425					
X1	0127	0306	0298					
X1A	0130	0315	0289	0293	0327			
X2	0132	0317	0419	0525				
X3	010F	0282	0321	0424				
X4	01A1	0428	0272	0280	0296	0300	0302	0305
			0316	0329				

@