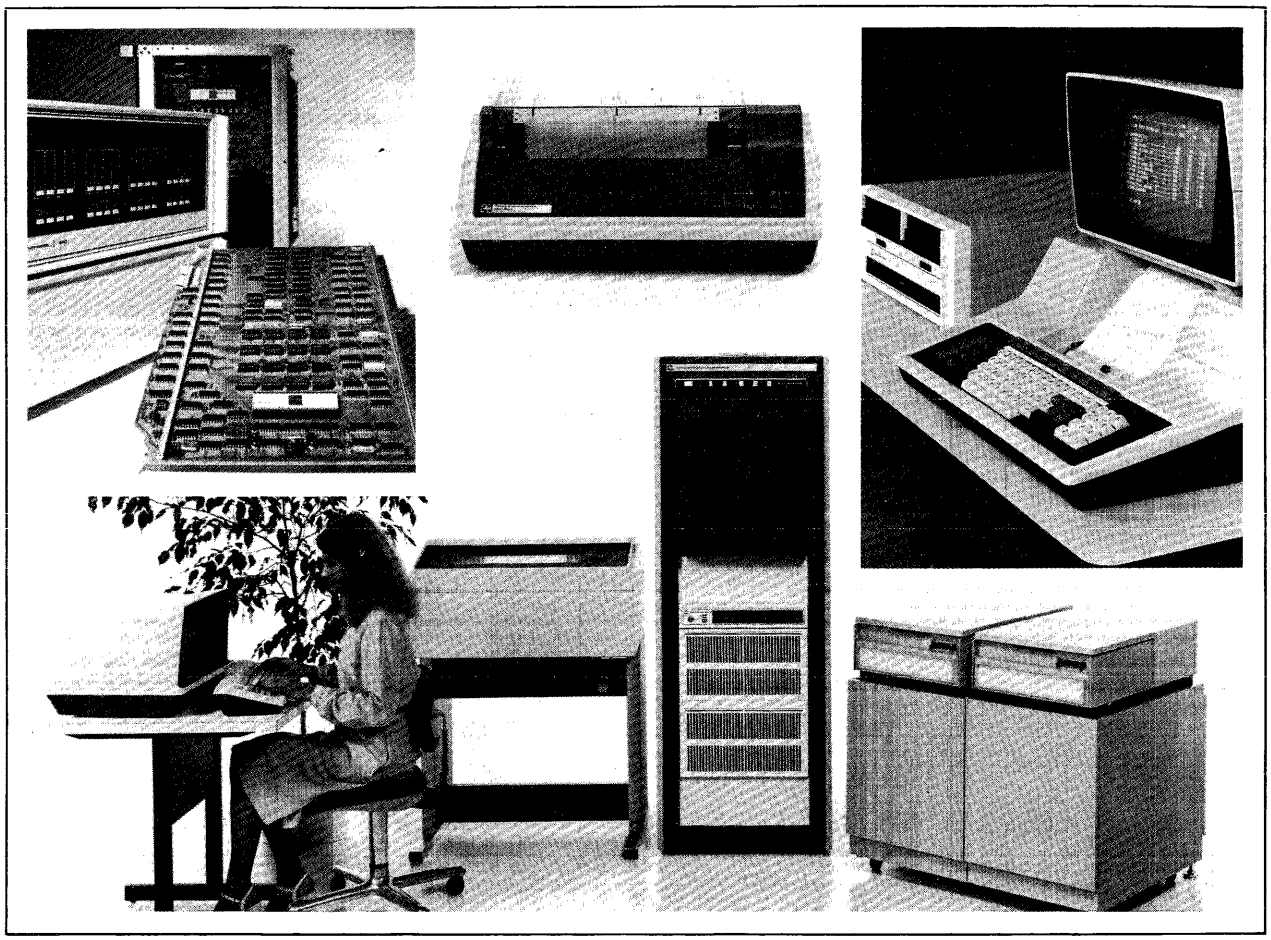
Model 990/10 Computer System Hardware Reference Manual



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PREFACE

This manual provides theory of operation and installation information required to install and to operate a Model 990/10 Computer System manufactured by Texas Instruments Incorporated.

This manual contains three sections including:

1 General Description – Provides an overview of the 990/10 System and briefly describes the system options.

2 Installation – Contains information and procedures for unpacking the computer from its shipping container, installing interrupts and performing initial checkout procedures on the newly installed system.

3 Principles of Operation – Provides detailed functional theory for the AU, memory and CRU expansion circuit cards, the power supplies, and the programmer panel assembly. This section also provides detailed information about the CRU and TILINE* interfaces to permit the user to custom-build interface modules for use in the 990/10 computer.

Texas Instruments also provides full installation and maintenance services for all computer and peripheral products. Contact your local Texas Instruments sales or service office for additional information. These offices can also assist you in obtaining more information about available software and price lists for all TI products.

If you plan to perform your own maintenance and need more detailed information than is provided in this manual, the following publications are available through your Texas Instruments sales or service office:

System-Level Maintenance Manuals

Title	Part Number
Model 990 Computer Family Maintenance Drawings	945421-9701 945421-9702
Model 990 Computer Diagnostics Handbook	945400-9701
Model 990/10 Computer Field Maintenance Manual	945402-9701
Model 990/10 Computer Depot Maintenance Manual	945404-9701
Model 990 Computer Peripheral Equipment Field Maintenance Manual	945419-9701

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Installation and Operation Manuals

Title	Part Number
Model 990 Computer Model 913 CRT Display Terminal Installation and Operation	943457-9701
Model 990 Computer Model FD800 Floppy Disc Installation and Operation	945253-9701
Model 990 Computer PROM Programmer Installation and Operation	945258-9701
Model 990 Computer 733 ASR/KSR Terminal Installation and Operation	945259-9701
Model 990 Computer 743 KSR Terminal Installation and Operation	943462-9701
Model 990 Computer, Model T200 Disc System Installation and Operation	949615-9701
Model 990 Computer, Model DS25/DS50 Disc System Installation and Operation	946231-9701
Model 990 Computer, Model DS31/DS32 Disc Installation and Operation	945260-9701
Model 990 Computer, Local Multidrop Module Installation and Operation	949610-9701
Model 990 Computer, Communications System Installation and Operation	945409-9701
Model 990 Computer Pulse/Tone Auto Calling Unit Installation and Operation	945425-9701
Model 990 Computer, Models 306 and 588 Line Printers Installation and Operation	945361-9701
Model 990 Computer, Model 979A Magnetic Tape System Installation and Operation	946229-9701
Model 990 Computer Model 804 Card Reader Installation and Operation	945262-9701
Model 990 Computer, Model 810 Line Printer Installation and Operation	939460-9701
Model 990 Computer, Models 2230 and 2260 Line Printers Installation and Operation	946256-9701
Model 990 Computer, Digital/Analog, Analog/Digital Converter Modules Installation and Operation	944774-9701

Peripheral Depot Maintenance Manuals

Title	Part Number
Model 990 Computer, Model 913 CRT Display Terminal Depot Maintenance Manual	945406-9701
Technical Manual, Model 306 Printer (plus Model 306C Addendum)	974993-9701
Technical Manual, Model 500 Printer (plus Model 588 Addendum)	974998-9701
Model 990 Computer, Model FD800 Floppy Disc Controller Depot Maintenance Manual	945418-9701
Model 990 Computer, Model 979A Magnetic Tape Controller Depot Maintenance Manual	946237-9701

Programming Manuals

Title	Part Number
Model 990 Computer/TMS 9900 Microprocessor Assembly Language Programmer's Guide	943441-9701
Model 990 Computer Fortran Programmer's Guide	945411-9701
Model 990 Computer Cobol Programmer's Guide	945412-9701
Model 990 Computer TX990 Operating System Programmer's Guide	945416-9701

Other Software Manuals

Title	Part Number
Model 990/10 Program Development System Operation Guide	945256-9701
Model 990 Computer, PDP-10 Cross Assembler User's Guide	943443-9701
Model 990 Computer, IBM System/3X0 Cross Assembler User's Guide	943444-9701
Model 990 Computer Cross Support System User's Guide	945252-9701

Other Software Manuals (Continued)

Title	Part Number
Model 990 Computer, Hexadecimal Debug User's Guide	943445-9701
Model 990 Computer Terminal Source Editor User's Guide	943449-9701
Model 990 Computer Linking Loader User's Guide	943450-9701
Model 990 Computer, 733 ASR System Software Operation Guide	945254-9701
Model 990 Computer, 16 Input/Output EIA Data Module Depot Maintenance Manual	945415-9701
Model 990 Computer, 16 Input/Output Data Module Depot Maintenance Manual	945407-9701
Model 990 Computer Full Duplex EIA Module Depot Maintenance Manual	945408-9701
Model 990 Computer Analog/Digital, Digital/Analog Converter Modules Depot Maintenance Manual	944775-9701
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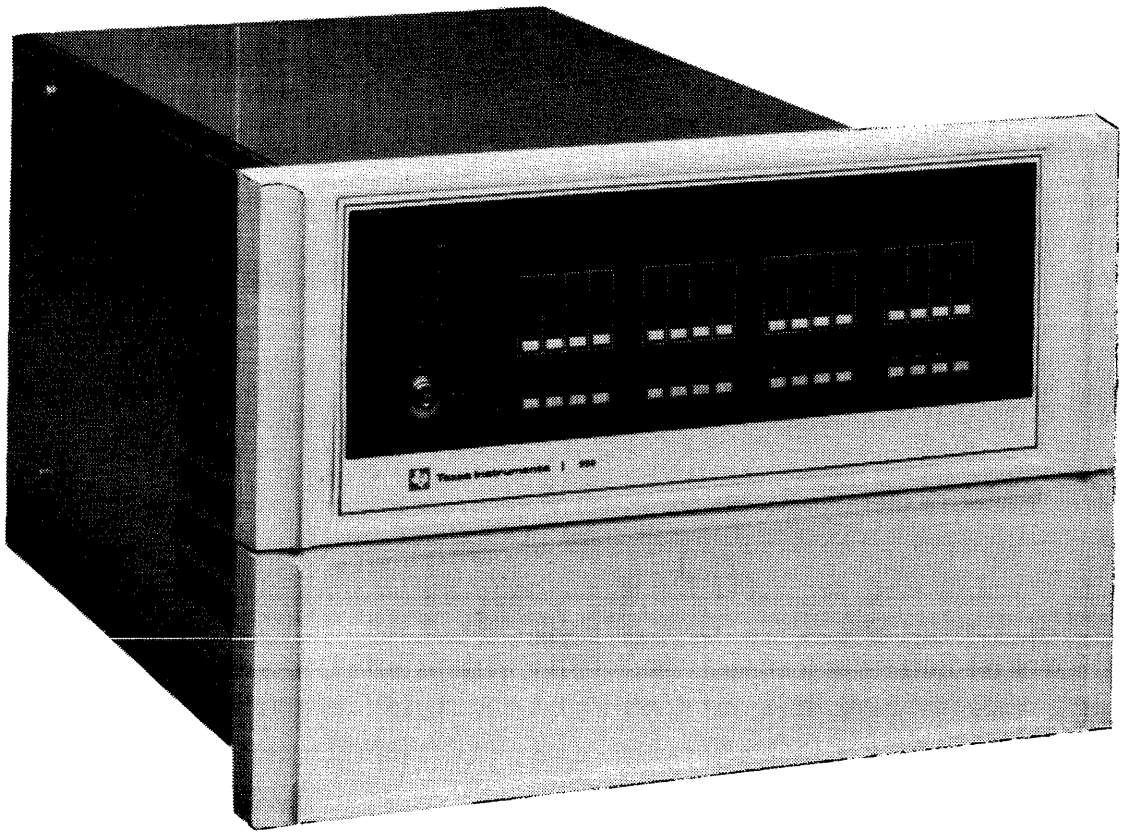

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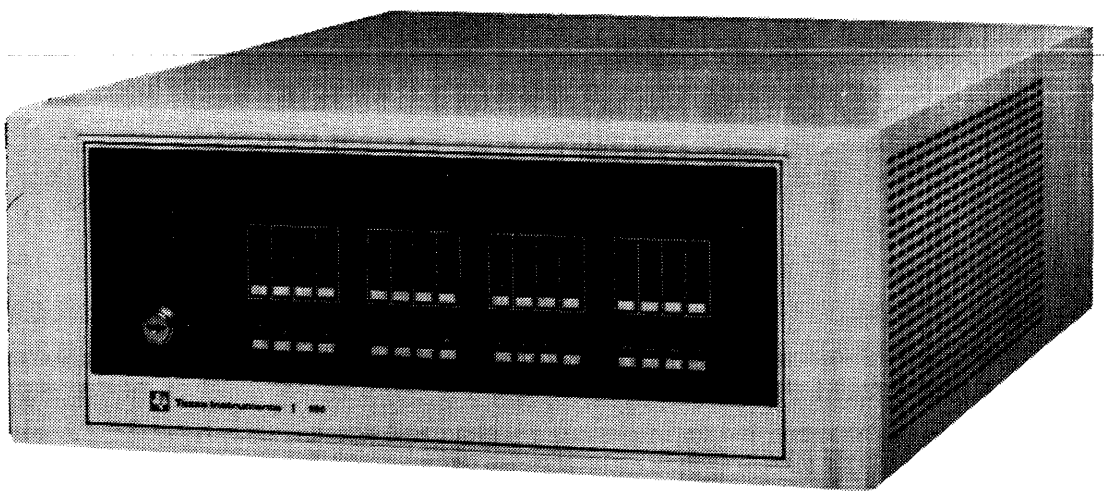

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Figure 1-1. Model 990/10 Minicomputer in Two Packaging Options

SECTION 1

GENERAL DESCRIPTION

1.1 GENERAL

This manual provides principles of operation for the Model 990/10 Minicomputer System manufactured by Texas Instruments Incorporated. Also provided are instructions for the installation and operation of the system.

This section contains functional and physical descriptions that acquaint the user with the hardware components and capabilities of the Model 990/10 Minicomputer System. For ease of reference, the Model 990/10 Minicomputer System will hereinafter be referred to as the minicomputer system.

To satisfy the requirements of dedicated computer systems, the minicomputer system is available in a number of optional configurations for use in a wide variety of applications. These options are discussed in this section.

1.2 PURPOSE OF EQUIPMENT

The minicomputer system features the 990/10 minicomputer as the heart of the system. The 990/10 minicomputer consists of three full-sized TTL printed circuit boards; an arithmetic unit board, a system interface/memory mapping board, and a memory board. When the three boards are mounted in a chassis and augmented with additional memory, interface modules, and input/output peripherals the 990/10 minicomputer becomes a highspeed, flexible and powerful minicomputer system with the capability of handling a wide range of computer applications at low cost.

The minicomputer system may be implemented in a 177.04-millimetre (6.97-inch) chassis that has chassis slots for installing 6 full-sized logic boards or a 310.39-millimetre (12.22-inch) chassis into which may be installed 13 full-sized logic boards (see figure 1-1). The 6-slot chassis and the 13-slot chassis may have either an operator panel or programmer panel as the front panel of the chassis. Figure 1-1 shows the programmer panel version of both the 6-slot and 13-slot chassis.

1.3 HARDWARE DESCRIPTION

The minicomputer system consists of two (or optionally three) major units as shown in figure 1-2; the 990/10 minicomputer, a chassis assembly, and (when implemented) a memory expansion module. The flexibility of design is such that the 990/10 minicomputer is available in standard options equipped with from 16K 8-bit bytes to 40K 8-bit bytes of memory in 8KB increments either with or without the mapping feature that increases the addressing capability of the processor from 64K bytes to 2M bytes. Also, three configurations of memory boards with error checking and correcting circuitry (ECC) (with or without the mapping feature) are available for use with the 990/10 computer system as described in later paragraphs.

The chassis assembly consists of either a 6-slot or 13-slot chassis, a 20-ampere or 40-ampere power supply, a programmer panel or operator panel, and may optionally have a standby power supply.

When system requirements are for greater than 40K bytes of memory, additional memory can be implemented by installing memory expansion modules in full-sized slots of the chassis. The interface to the minicomputer system for all memory is made through the TILINE*. The features and options of each of the units are discussed in depth in the following paragraphs.

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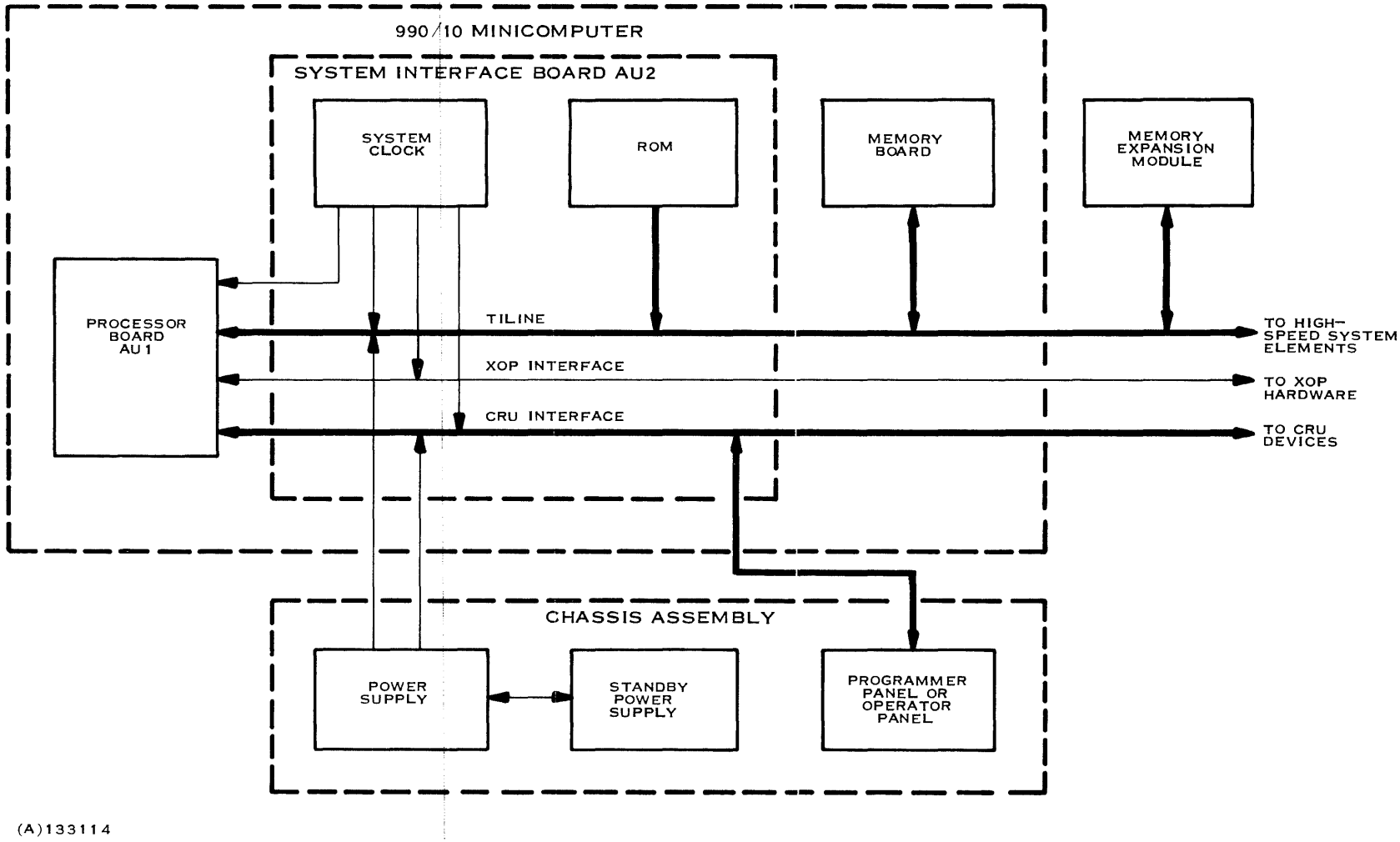


Figure 1-2. Model 990/10 Minicomputer System Block Diagram

1.3.1 **990/10 MINICOMPUTER.** The 990/10 minicomputer as implemented on three printed circuit boards provides the following features.

- 1K 8-bit bytes of PROM installed on system interface board for programmer panel, loader, and self-test options
- 16 vectored interrupts (in 13-slot chassis), 13 external
- Real time clock interrupt input
- TILINE bus interface to memory, memory expansion, and high-speed direct memory access device controllers
- Communication register unit (CRU) interface for communications link with a variety of external serial and parallel data transfer devices
- One CRU interface for the programmer panel (or operator panel)
- Error interrupt logic
- Extended Operations (XOP) hardware interface
- Processor capability for access to 64K 8-bit bytes of memory (extended to 2048K bytes with mapping feature option).

1.3.1.1 **Arithmetic Unit Board.** The arithmetic unit board, designated the AU1 board, is a two-sided printed circuit board that contains the TTL devices to process instructions from the memory and to sequence CRU input/output operations. The AU1 board will be referred to as the processor in this manual. The processor installs into slot 2 of either the 6-slot or 13-slot chassis and connects to the system interface/memory mapping board by two ribbon cable jumpers across the top edges of the two boards. The interface to the power supply for required voltages and the power reset signal is at the edge of the board that installs into the backpanel at slot 2. The AU1 board has three special 16-bit registers that have defined uses. These registers are the program counter (PC), workspace pointer (WP), and the status register (ST) registers. Additional locations called workspace registers exist in memory as defined by the workspace pointer register. The PC and WP always contain an even address (address bit 15 = 0). The program counter contains the address of the instruction following the current instruction being executed, the workspace register contains the beginning address of 16 consecutive memory locations that are actively being used as workspace registers, and the status register contains information about the state of the processor.

1.3.1.2 **System Interface/Memory Mapping Board.** The system interface/memory mapping board, designated AU2A (without mapping feature) or AU2B (with mapping feature), contains the TILINE bus interface, the CRU interface, interrupt logic, 1024 bytes of TTL programmable read-only memory, the system clock, programmer panel interface, and (optionally) the memory mapping feature. The system interface/memory mapping board installs into slot 1 of either the 6-slot or 13-slot chassis. The interface with the power supply, memory, and with peripheral devices is at the edge of the board that installs into the backpanel. As described in paragraph 1.3.1.1, the interface to the AU1 board is by means of ribbon cables and the interface to the programmer panel is also by means of a smaller ribbon cable. Connectors are also provided on the board for XOP hardware and a breakpoint interrupt device.

1.3.1.3 990/10 RAM Memory Board. The 990/10 memory board is the third of the printed circuit boards of the 990/10 minicomputer and is normally installed into chassis slot 3 of either the 6-slot or 13-slot chassis. The memory board is available in a number of optional configurations. Four options of the board consist of a memory controller with 16K, 24K, 32K or 40K bytes of memory. Each of these four different capacity boards may be obtained with a factory-installed parity generation/checking feature for a total of eight separate options.

Memory capacity of the minicomputer can be expanded by either 16K, 24K, 32K or 40K bytes by installing additional memory boards in chassis slots. Expansion beyond 65K bytes of memory requires that the AU2B board (with mapping feature) be installed in chassis slot 1.

Additionally, three different configurations of a memory board with a memory controller and error checking and correcting circuitry (ECC) are available. In the first of these configurations, memory is implemented through the use of TMS 4060 memory chips. The TMS 4060 chip is organized as 4096 one-bit words housed in a 22-pin dual-in-line package. This configuration consists of a memory board with a memory controller and 16K bytes of memory with ECC installed. This board also contains the necessary memory control logic to drive one memory add-on module with 16K, 32K or 48K bytes of memory with ECC for a maximum of 64K bytes per set of two boards. Assuming the minicomputer is equipped with the memory mapping feature, expansion beyond 64K bytes of memory is achieved through the use of additional pairs of these boards. In the second of these configurations, memory is implemented through the use of TMS 4116 memory chips. The TMS 4116 chip is organized as 16,384 one-bit words housed in a 16-pin dual-in-line package. This configuration consists of a memory board with a memory controller and up to 96K bytes of memory with ECC installed. This board also contains the necessary memory control logic to drive up to four memory add-on modules each with up to 256K bytes of memory with ECC for a maximum memory size of 1M bytes. In the third of these configurations, the memory board is a cache controller. The cache controller contains all memory control logic as well as the storage elements for 64K bytes of primary memory and 2K bytes of cache memory. Primary memory in this controller is also implemented through use of the TMS 4116 chip and the controller contains the necessary control logic to drive up to four of the memory add-on modules each with up to 256K bytes of memory. In this controller, the cache technique is used to improve the effective operating speed of primary memory.

1.3.2 CHASSIS ASSEMBLY. The Model 990/10 Minicomputer System may be implemented in a 6-slot or a 13-slot chassis assembly. The 6-slot and 13-slot chassis may be equipped with either an operator panel or a programmer panel. The features and options available in each of the chassis assemblies are discussed in the following paragraphs.

1.3.2.1 6-Slot Chassis. The 177.04-millimetre (6.97-inch), 6-slot chassis consists of a chassis and backpanel that will accommodate 6 full-sized logic boards, a 20-ampere power supply, and either a programmer panel or an operator panel. Optionally, the user may select a standby power supply. When selected, the standby power supply mounts on and connects to the 20-ampere power supply. The standby power supply provides memory power both during power failure and normal ac operation. The standby power supply also maintains a charge on the 12-volt battery supply that is part of the standby power supply. The backpanel is wired to accept the AU2A (or AU2B) printed circuit board in slot 1, the AU1 board in slot 2, and the memory board in slot 3. The other three slots are wired to accept 3 full-sized logic boards or as many as six half-sized logic boards. An air filter and fans provide filtered air cooling for the chassis.

1.3.2.2 13-Slot Chassis. The 310.39-millimetre (12.22-inch), 13-slot chassis is an enlarged version of the 6-slot chassis used when the need to handle a larger number of logic boards exists. The 13-slot chassis is used either as the main chassis for the minicomputer or as a CRU expansion chassis. To accommodate the larger system requirement, the 13-slot chassis assembly consists of a chassis with

backpanel that has slots for 13 full-sized logic boards, a 20- or 40-ampere power supply, and either a programmer panel or an operator panel. As with the 6-slot chassis, the standby power supply is an available option. The backpanel is wired to accept the AU2A (or AU2B) printed circuit board in slot 1, the AU1 board in slot 2, and the memory board in slot 3. The other ten slots are wired to accept ten full-sized logic boards or as many as 20 half-sized logic boards.

1.3.3 MEMORY EXPANSION MODULE. Memory expansion beyond that memory capacity contained on the memory board that is installed as an integral part of the 990/10 minicomputer as described in paragraph 1.3.1.3 is achieved simply by installing additional memory boards. Options available for memory expansion are fully described in paragraph 1.3.1.3. An in-depth description of each of the boards is provided in paragraph 3.3.

SECTION 2

INSTALLATION

2.1 GENERAL

This section provides information and procedures for unpacking the computer from its shipping container, installing it in either a tabletop or a rackmounted configuration, and checking the operation of the newly installed computer system. The section also includes a procedure for modifying the interrupt structure of the computer. The procedures assume that the user has a fundamental knowledge of basic handtools and cabling techniques, but they do not require a detailed understanding of computer hardware or software. This section does not cover installation of any of the peripheral devices that may accompany the computer shipment. Installation instructions for those devices are included in the Installation and Operation manual that is shipped with each peripheral device. To aid in planning to meet the installation requirements for the computer, table 2-1 summarizes the specifications and requirements of the available chassis for the computer.

2.2 UNPACKING/PACKING (6- AND 13-SLOT CHASSIS)

The computer is shipped in a corrugated cardboard container together with the circuit boards and interconnecting cables required to install the system. Upon receipt of the container, inspect to ensure that no signs of physical damage are present. Following preliminary inspection, perform the following steps to remove the computer from its container and ready it for operation. Figure 2-1 illustrates the required steps.

NOTE

Save shipping carton and all packing materials for use in reshipment of the unit.

1. Position container so that the address label is right-side up.

2. Open top of container and remove cushioning material from corners.

NOTE

If the computer has the table top enclosure (6-slot chassis only) no foam block is required to secure circuit boards in chassis.

3. Remove cardboard inner sleeve and foam block (rackmount configurations) from shipping container.

WARNING

Use proper lifting techniques to avoid backstrain when lifting computer chassis.

4. Remove computer and attached shipping pallet from container. When lifting assembly, lift from under the assembly to avoid undue strain on the chassis assembly.

Table 2-1. Computer Chassis Specifications

Characteristic	6-Slot Chassis	13-Slot Chassis
Height	177.04 mm (6.97 in.)	310.39 mm (12.22 in.)
Width	419.10 mm (16.50 in.)	419.10 mm (16.50 in.)
Depth	584.20 mm (23.00 in.)	584.20 mm (23.00 in.)
Ambient Temperature		
Operating[1]	0° to 50°C (32° to 122°F)	0° to 50°C (32° to 122°F)
with Low Speed Fan	0° to 35°C (32° to 95°F)	0° to 35°C (32° to 95°F)
Storage	-40° to 70°C (-40° to 158°F)	-40° to 70°C (-40° to 158°F)
Humidity[2]	0% to 95%	0% to 95%
Altitude	0 to 3048 m (0 to 10,000 ft.)	0 to 3048 m (0 to 10,000 ft.)
Heat Load		
Full Card Slot	50 watts	50 watts
Power Supply	170 watts	170 watts
Exhaust Temperature	65°C (maximum) (149°F)	65°C (maximum) (149°F)
External Power Requirements		
Standard	100 or 115 Vac ± 10% 47 to 63 Hz 3-wire service (hot, neutral, gnd)	100 or 115 Vac ± 10% 47 to 63 Hz 3-wire service (hot, neutral, gnd)
Optional	200 or 230 Vac ± 10% 47 to 63 Hz 3-wire service (hot, neutral, gnd)	200 or 230 Vac ± 10% 47 to 63 Hz 3-wire service (hot, neutral, gnd)

Notes:

[1] Lower upper operating limit by 2°C (3.6°F) for every 762 metres (2500 feet) increase in altitude.
[2] No condensation is allowed.

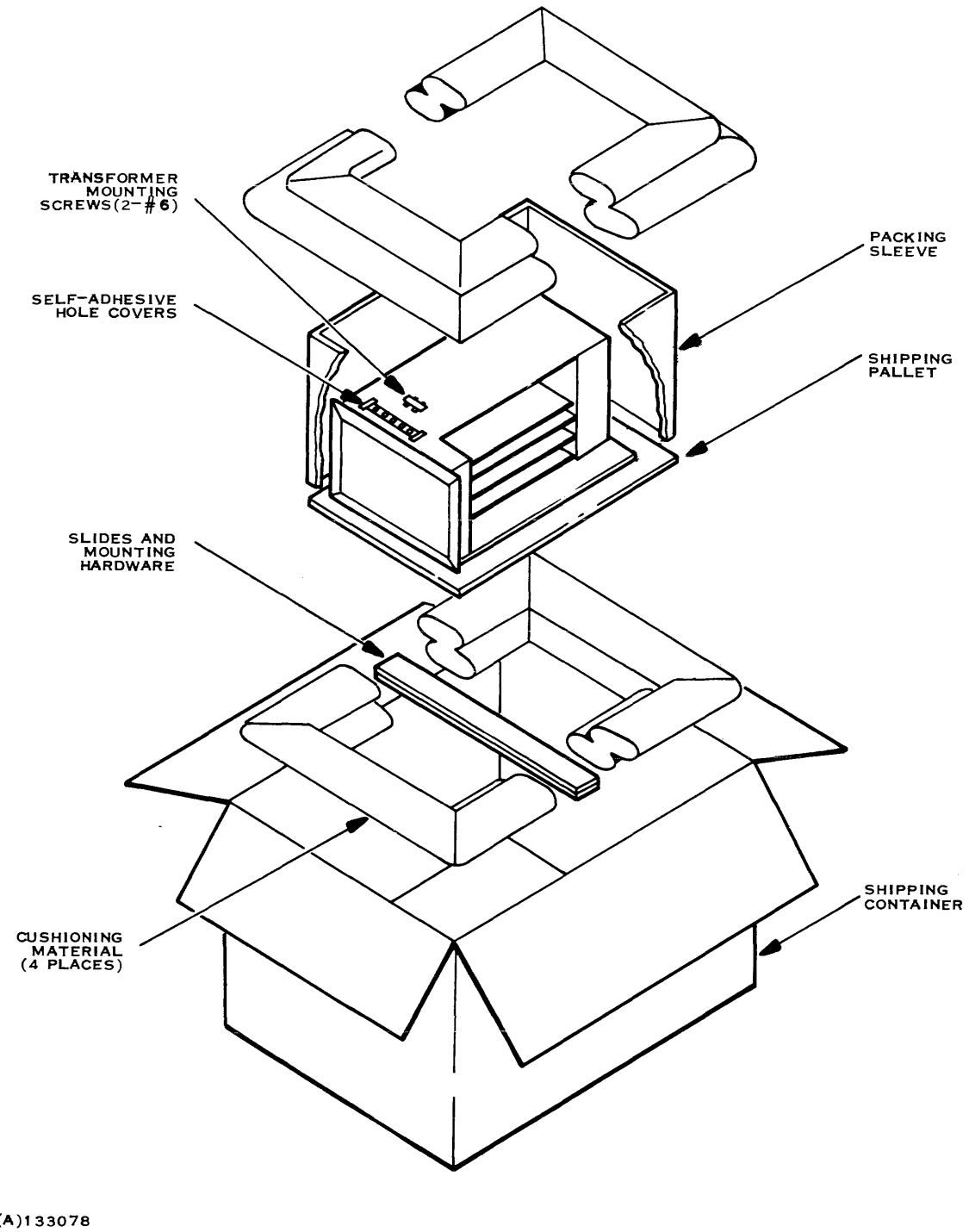


Figure 2-1. Computer Shipping Packaging

CAUTION

To prevent the mounting screws on the underside of the shipping pallet from scratching table surface, place a shielding material (the packing sleeve removed in step 3 makes an excellent shield) on the table before setting the assembly on the table.

5. Place the removed assembly on a convenient, protected work surface.

NOTE

For rackmount configurations, the slides are packed in the bottom of the shipping container.

6. Remove the rackmount slides (if present) and the interface cables from the bottom of the shipping container.

CAUTION

In the following steps, do not allow the unit to overhang the work surface so far that it will fall off of the surface.

7. Position the computer and shipping pallet assembly so that the front edge of the assembly overhangs the edge of the work surface to reveal two (2) #10 mounting screws that secure computer to shipping pallet. See figure 2-2 for location of all mounting screws.

8. Use a straight blade screwdriver to remove the two screws and their associated washers and lock washers. Save the screws and washers for reshipment.

9. Reposition the computer and shipping pallet assembly so that the rear edge of the assembly overhangs the edge of the work surface to reveal three (3) #10 mounting screws that secure computer to shipping pallet.

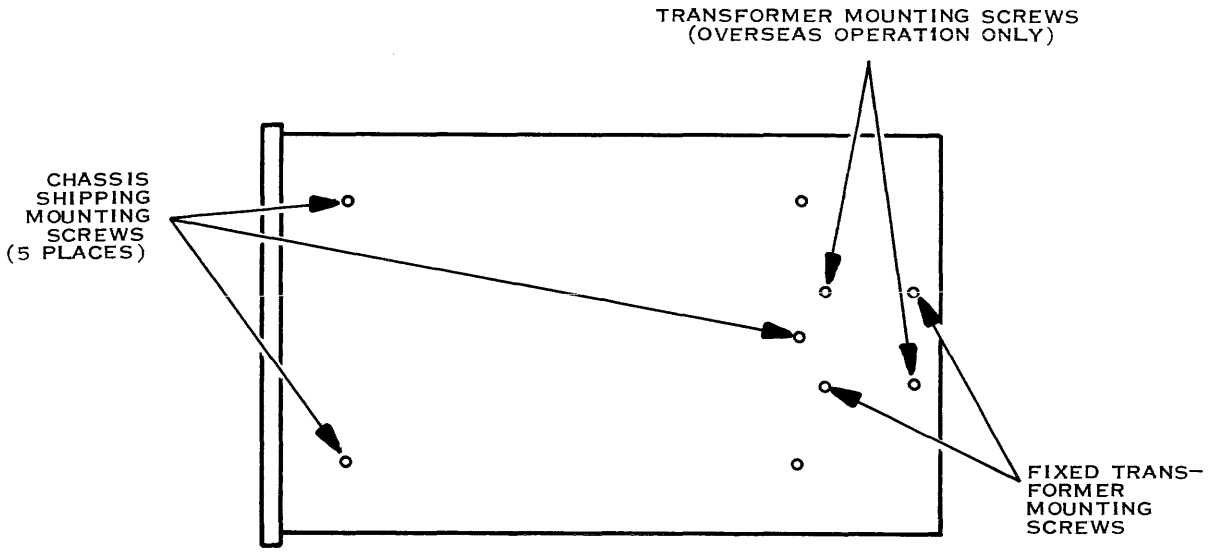
10. Remove the three screws, washers and lockwashers and save for reshipment.

NOTE

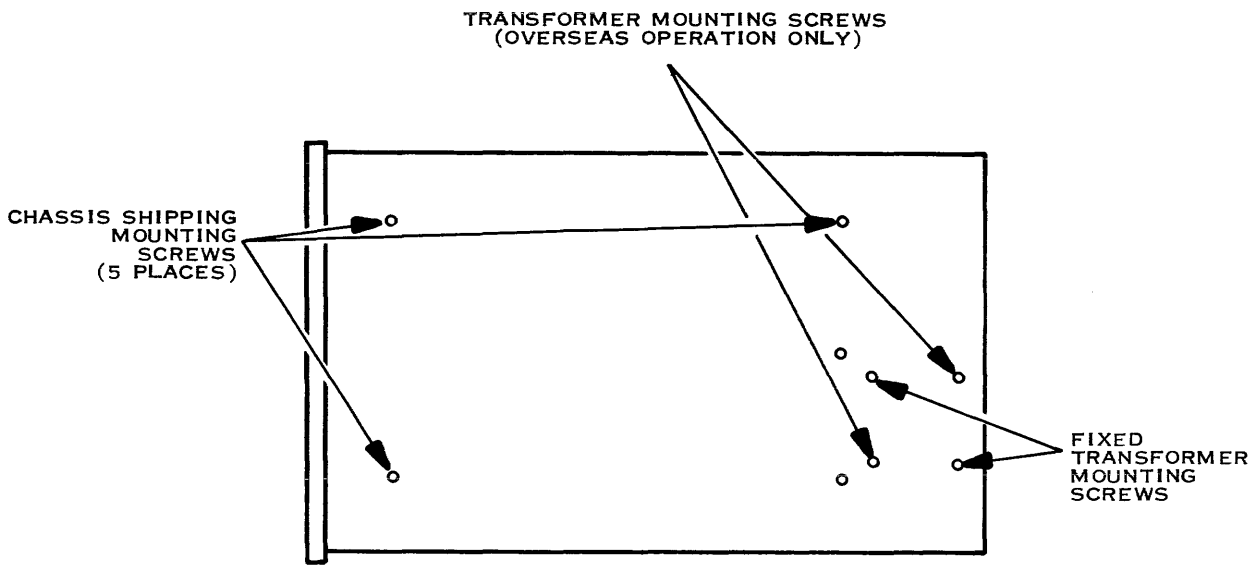
If the computer was ordered for overseas operation, two (2) additional mounting screws are visible on the underside of the shipping pallet. These screws secure the transformer to the shipping pallet. If these screws are not included on the unit being installed, skip step 11.

11. Remove two (2) #6 transformer mounting screws and their associated washers and lockwashers and save for reshipment.

12. Lift computer chassis from shipping pallet and place it on the work surface such that the rear of the unit overhangs the work surface to reveal the holes for the removed mounting screws.



(A) 6-SLOT AND TABLE TOP CHASSIS BOTTOM VIEW



(B) 13-SLOT CHASSIS BOTTOM VIEW

(A)133079

Figure 2-2. Location of Chassis Shipping Pallet Mounting Screws

NOTE

If the unit being installed did not have the two #6 mounting screws (see step 11), skip the following step.

13. Remove two (2) #6 screws taped to the top of the computer chassis and insert them in the holes vacated by the two #6 mounting screws removed in step 11. Tighten the two new screws to secure the transformer to the chassis.

14. Remove the strip of self-adhesive hole covers that are taped to the top of the computer chassis. Use three of the hole covers to cover the three mounting screw holes along the rear of the chassis.

15. Reposition the computer chassis such that the front edge overhangs the work surface to reveal the mounting holes for the front mounting screws.

16. Use the remaining two (2) self-adhesive hole covers to cover the front mounting screw holes.

17. Set the computer chassis in a safe position on the work surface to continue with the remaining portions of the installation procedure.

18. Pack all shipping materials into the original shipping container and store the container for use in reshipment of the unit.

19. Inspect the computer chassis and included components for signs of damage that may have occurred during shipment. If damage has occurred, notify the carrier immediately.

To repack the unit, reverse the above procedure using the original packing material.

2.3 INSTALLATION (TABLETOP CHASSIS)

The tabletop chassis is a 6-slot chassis configuration contained in an attractive enclosure. The unit is shipped fully assembled to ensure that all components arrive safely. However, before operating the computer, the enclosure must be removed to connect the computer to the system peripheral devices. The following procedure describes the steps required to completely integrate the new computer into its operating environment.

1. Set unpacked chassis assembly in the approximate installation position.

NOTE

The chassis enclosure is secured to the chassis by three (3) oval-head screws on each side of the chassis and one oval-head screw at the rear of the assembly as illustrated in figure 2-3.

2. Remove seven (7) oval-head screws and their associated finishing washers that secure the chassis enclosure to the chassis. Save screws and washers for reinstallation of enclosure.

3. Carefully lift enclosure up from chassis and set enclosure in safe place. Remove shipping brackets that hold logic boards in place and save for reuse at a later date.

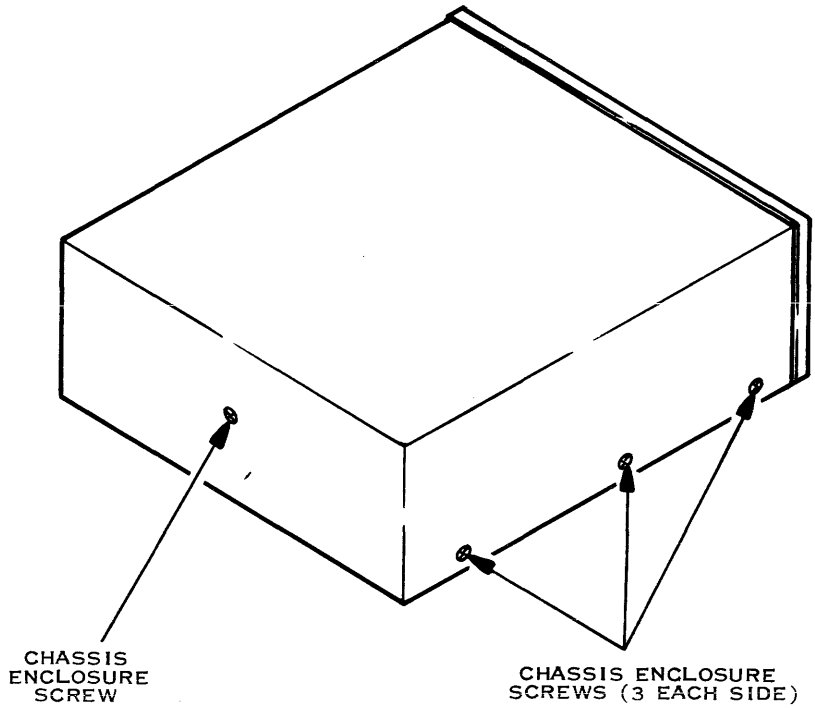


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Figure 2-3. Location of Chassis Enclosure Screws

NOTE

The chassis is shipped from the factory with interrupts installed in predetermined locations as illustrated in figure 2-4. CRU addresses are fixed and cannot be changed.

4. Determine the chassis location and interrupt assignments for each peripheral interface in the system. If the interrupt assignments do not match the factory installed interrupts, or if additional interrupt assignments are required, perform the Interrupt Installation procedure in this section of the manual.

5. Verify that the interface modules, memory boards and the processor boards are firmly seated in their correct positions in the chassis.

6. Install the peripheral device interface cables on the proper interface module in the computer chassis as described in the Installation and Operation manual included with the peripheral device. All interface cables should be routed through the cable clamps at the rear of the chassis and should exit at the rear of the chassis.

7. Connect the ac power cord to a source of ac power with the specifications applicable to the equipment being installed.

8. Turn the key switch on the front panel to the ON (or UNLOCK) position. Observe that the POWER indicator (and the RUN indicator) on the front panel light and that the fans operate.

	P1 (FRONT OF CHASSIS)			P2 (REAR OF CHASSIS)		
	FIXED CRU BASE ADDRESS	CIRCUIT BOARD	INTER-RUPT LEVEL	FIXED CRU BASE ADDRESS	CIRCUIT BOARD	INTER-RUPT LEVEL
1	N/A	990/10 AU2	N/A	N/A	990/10 AU2	N/A
2	0120	990/10 AU1	N/A	0100	990/10 AU1	N/A
3	00E0	MEMORY	3*	00C0	MEMORY	3*
4	00A0	FLOPPY DISC CONTROLLER	7	0080	FLOPPY DISC CONTROLLER	7
5	0060	LINE PRINTER		0040	CARD READER	4
6	0020	PROM PROGRAMMER		0000	733 ASR/KSR	6

NOTE: UNUSED DEVICE INTERFACE LOCATIONS CAN BE USED FOR EXPANSION MEMORY OR OTHER DEVICE INTERFACES (WITH INTERRUPT MODIFICATION).

* INTERRUPT 3 WIRED HERE BUT NOT USED.

(A)133081

Figure 2-4. Pre-Wired Configuration for 6-Slot Chassis

9. Perform the System Checkout Procedure specified in paragraph 2.12.

10. Slip the chassis enclosure over the chassis and align it so that it mates properly with the front panel and the mounting screw holes.

11. Secure chassis enclosure to chassis using seven oval-head screws and finishing washers removed in step 2.

12. Position computer in final installation site.

13. Perform system software installation procedures for the operating system to be used with the computer. For Texas Instruments supplied software, this information is provided in the System Operation Guide for the specific software package.

2.4 INSTALLATION (RACKMOUNT CHASSIS)

Either the 6-slot or the 13-slot chassis can be ordered for mounting in a 482.60-millimetre (19-inch) equipment rack. The chassis is shipped with all circuit boards installed in the chassis; the rack-mounting hardware is packed in the same carton as the chassis. After performing the unpacking procedure, perform the following steps to install the computer in the rack:

NOTE

The following procedure requires access to the rear of the installation rack after the computer chassis is mounted in the rack.

1. Set unpacked chassis assembly on a convenient work surface near the equipment rack in which the computer will be installed.

WARNING

Ensure that the power cord is not connected to a source of ac power before continuing with procedure. Failure to observe this precaution could result in severe electrical shock.

2. Remove six (6) screws that secure air filter and rear access plate to rear of chassis. It is not necessary to remove air filter from access plate.

3. Install two clip nuts in predrilled holes in chassis as illustrated in figure 2-5.

4. Reinstall rear access cover/air filter assembly using the six mounting screws removed in step 2.

5. Inspect the front and rear mounting supports in the rack (or desk) to ensure that the distance between the front and rear supports is 615.95 ± 6.35 millimetres (24.25 ± 0.25 inches) as illustrated in figure 2-6.

6. Determine the desired vertical position of the bottom edge of the computer front panel. When using an EIA standard vertical support, the bottom edge of the front panel must be centered between two holes that are 12.70 millimetres (0.5 inch) apart as illustrated in figure 2-7. Using that figure, locate the position of the two slide mounting holes on each of the four mounting supports. These holes are 16.51 millimetres (0.65 inch) and 32.385 millimetres (1.275 inches) above the bottom edge of the front panel.

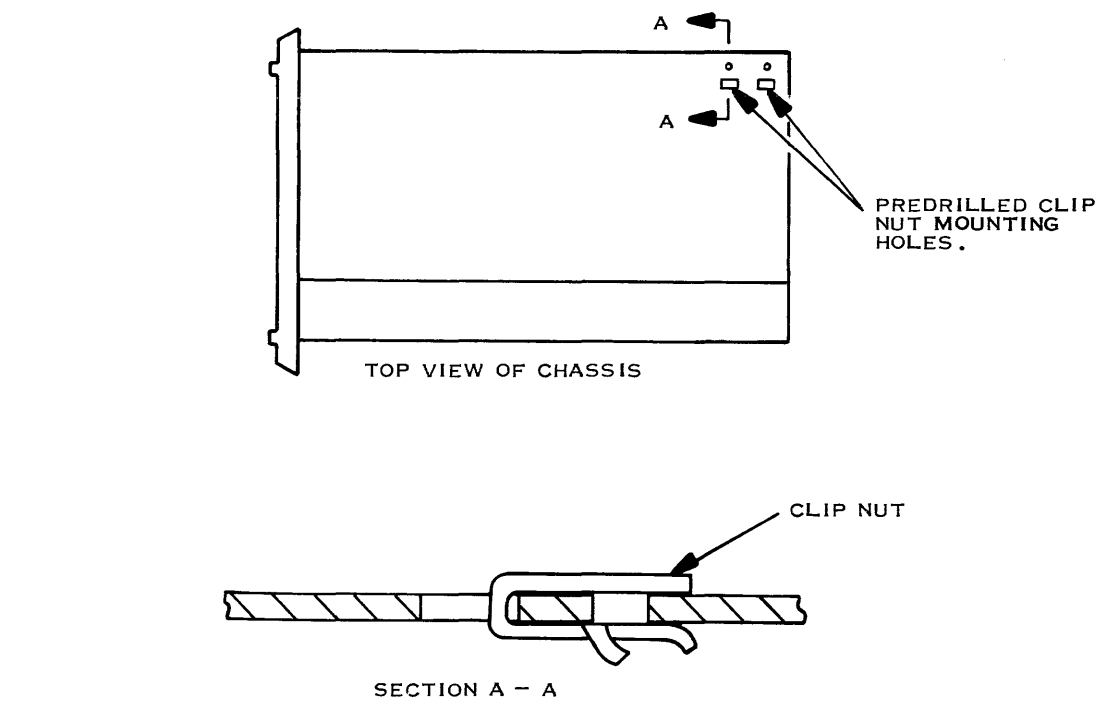


Figure 2-5. Clip Nut Installation

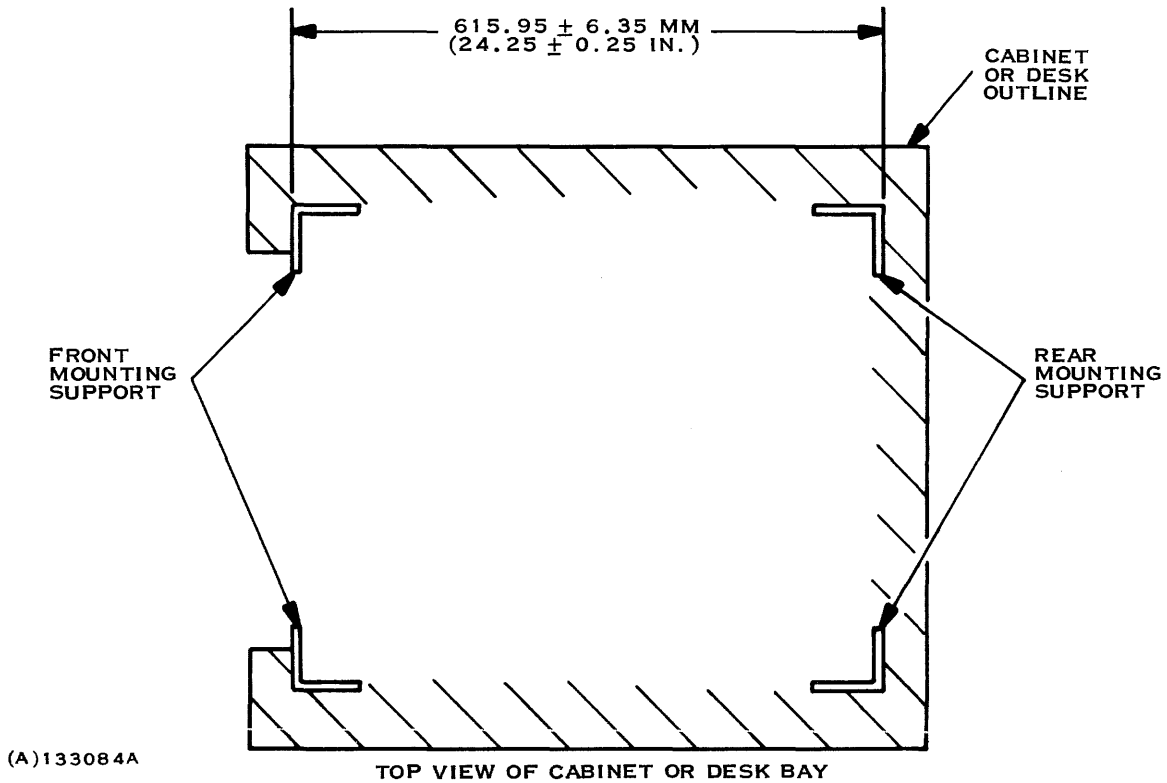


Figure 2-6. Mounting Cabinet Depth Specification

7. Loosely install eight (8) 10-32 X 1/4 mounting screws and their associated flat washers and lock washers in the eight selected holes in the mounting supports (front and rear). Screws are installed from the inside of the enclosure as illustrated in figure 2-8.

8. Loosely assemble rear mounting brackets to slides using hardware provided with slides. Finger-tighten rear mounting bracket screws.

9. Position left slide against front and rear mounting supports such that the slide mounting brackets fit between the washers of the mounting screws and the mounting supports. Finger-tighten the four mounting screws to hold the slide in place.

10. Adjust the slide so that the distance from the center of the cabinet mounting screws to the innermost point of the slide assembly is 38.10 millimetres (1.50 inches) as illustrated in figure 2-9.

11. Ensure that the slide assembly is square with the cabinet mounting supports and tighten the four (4) slide mounting screws and the rear bracket mounting screws.

12. Repeat steps 9 through 11 with the right slide.

13. Extend both slides and release the disconnect mechanism to remove the inner slide member from the slide assemblies.

14. Attach the inner slide members to the left and right underside of the computer chassis using 6-32 X 1/4 and self-tapping screws. Do not overtighten screws.

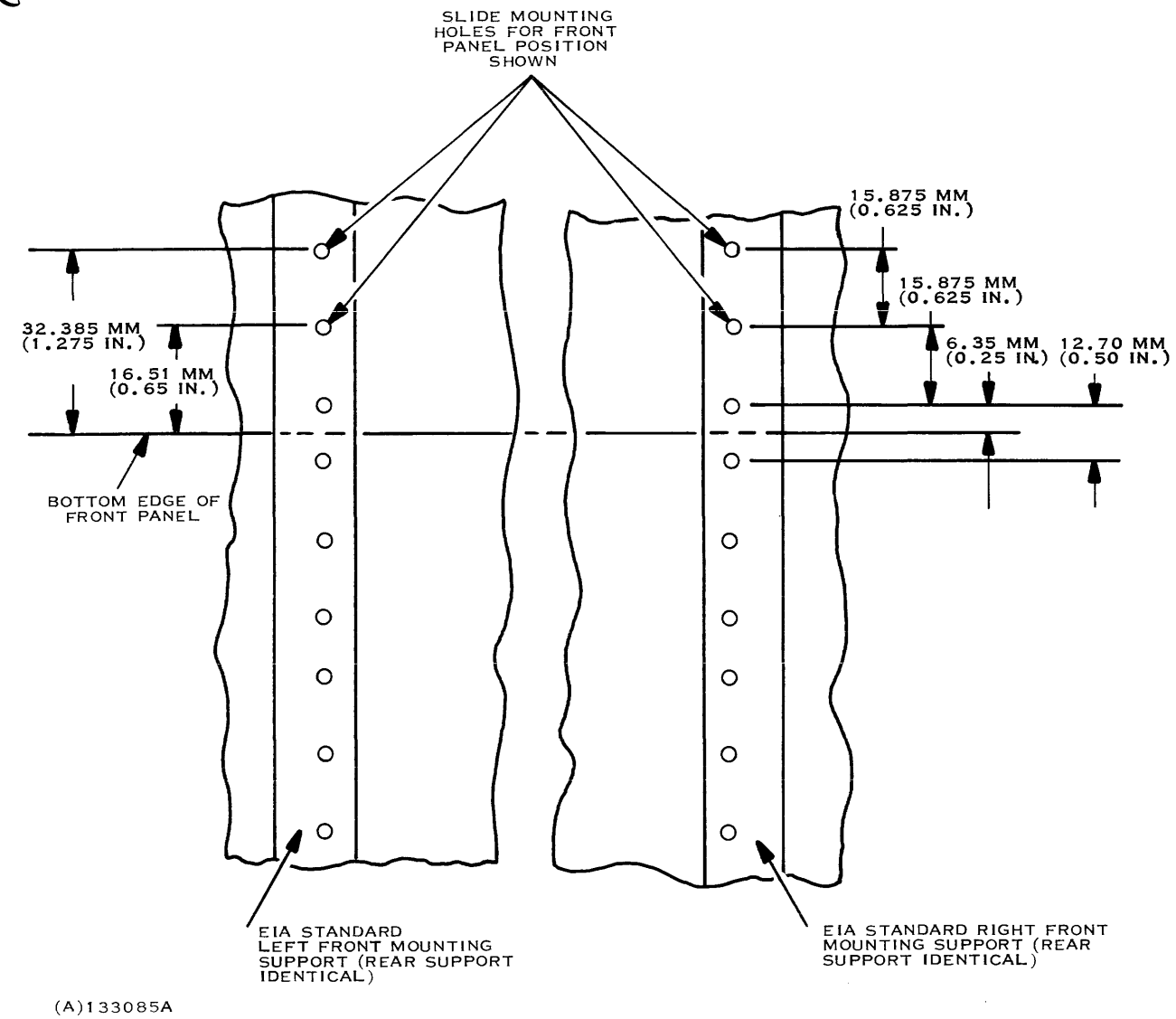


Figure 2-7. Mounting Hole Positioning

15. Mount ball stud to ball stud carrier bar using a 6-32 nut and lock washer as illustrated in figure 2-10.

16. Loosely install ball stud carrier bar to the top of the computer chassis using 6-20 screws and flat washers inserted into the clip nuts installed in the chassis in step 3.

17. Insert chassis into mounted slides and reseat the disconnect mechanism. Push chassis into the rack. During the last 25 millimetres (inch) of travel, lift the front of the chassis to ensure correct slide mating.

18. Assemble ball stud receptacle to stop plate using mounting hardware provided.

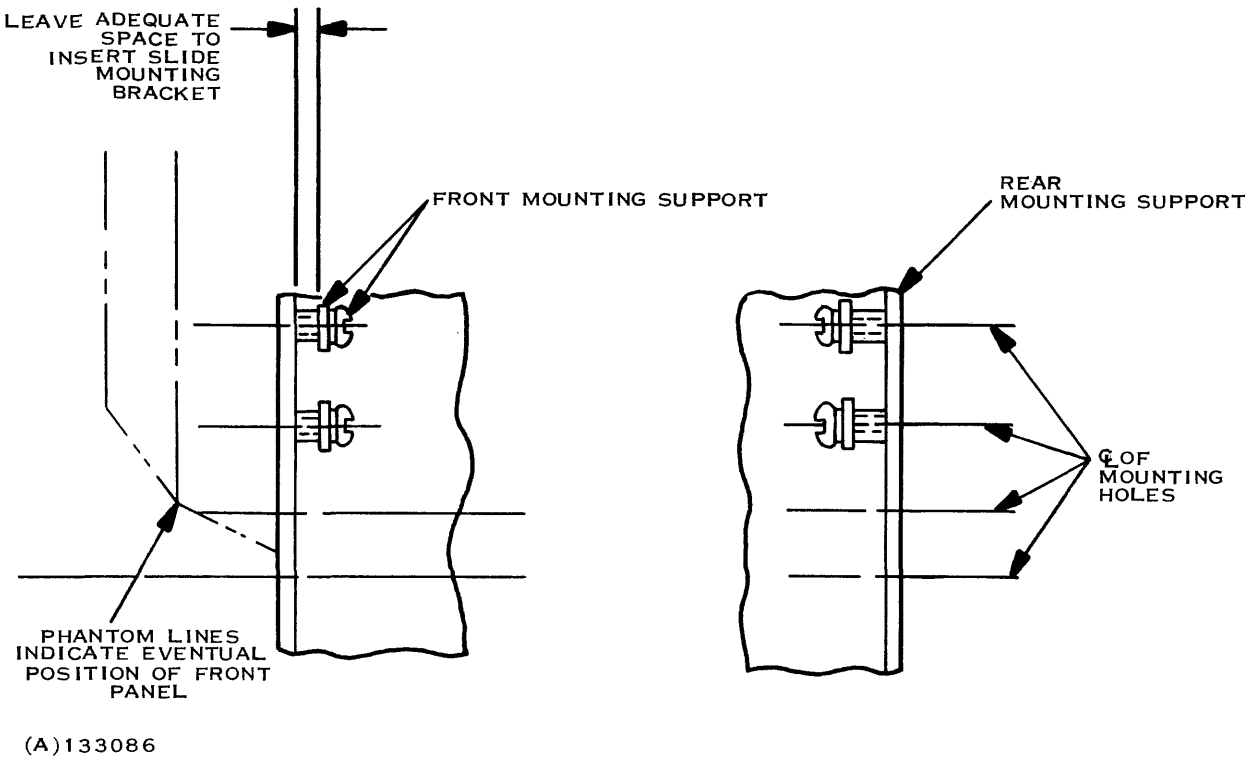


Figure 2-8. Mounting Screw Installation

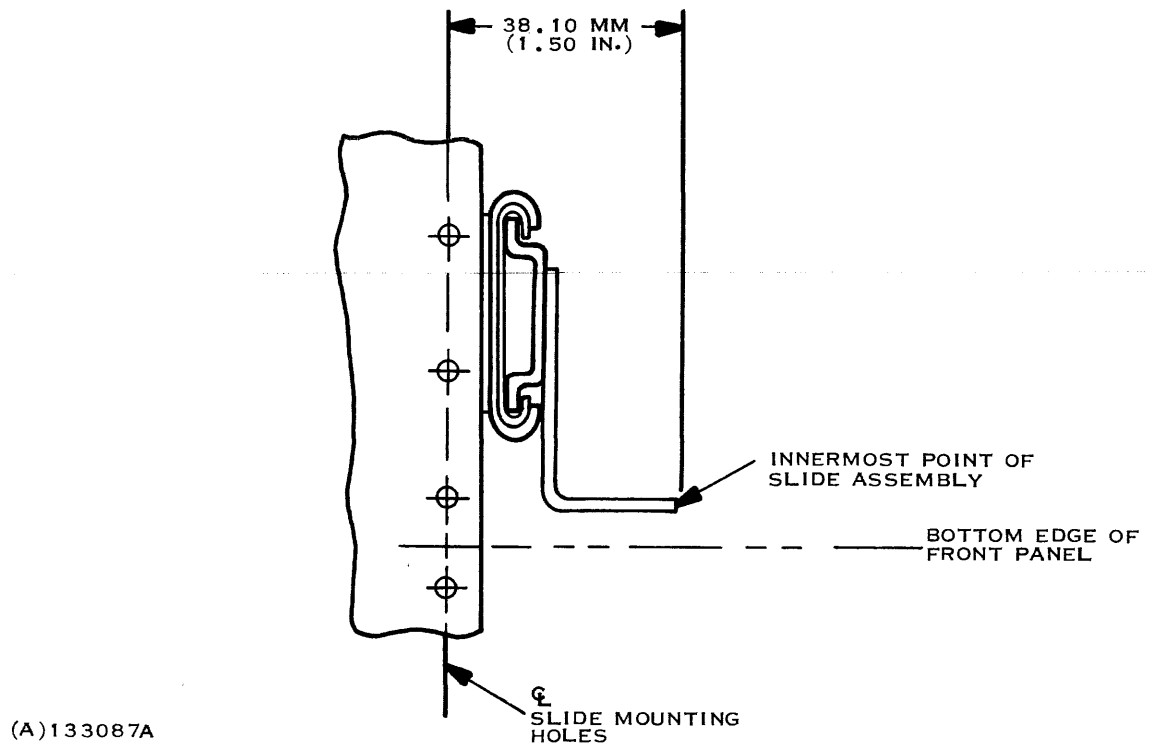


Figure 2-9. Chassis Slide Positioning

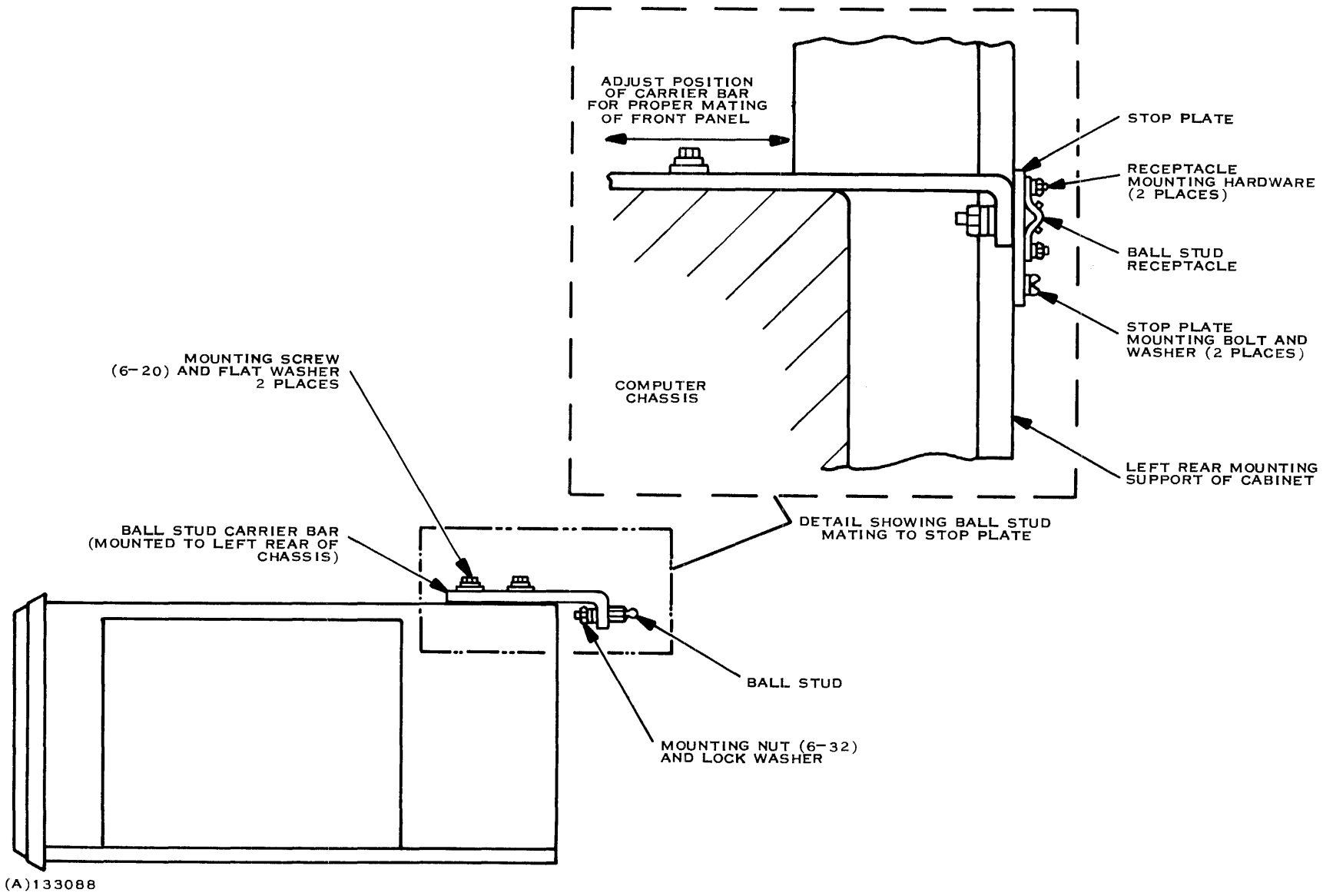


Figure 2-10. Installation of Ball Stud and Stop Plate

19. Install stop plate assembly to the back edge of the left rear mounting support of the cabinet at a height such that the ball stud receptacle mates with the ball stud of the computer chassis.

20. Adjust the forward-backward position of the ball stud carrier bar on the computer chassis such that the chassis stops and the ball stud latches into the receptacle when the back of the front panel is between 0.79 to 1.59 millimetres (0.03 to 0.06 inch) from the front mounting support of the cabinet.

21. Slide computer chassis in and out of the cabinet several times to ensure smooth operation and good alignment of all parts. Readjust as required.

22. Connect power cord from back of computer chassis to the ac power distribution system of the cabinet. Do not apply power at this time.

23. Slide the chassis out from the cabinet to expose the circuit boards mounted within the computer chassis. Remove shipping brackets that hold logic boards in place.

NOTE

The chassis is shipped from the factory with interrupts installed in predetermined locations. Figure 2-11 illustrates these assignments for the 13-slot chassis; 6-slot chassis assignments are identical to those previously described for the tabletop chassis. CRU addresses shown in the figure cannot be changed.

24. Determine the chassis location and interrupt assignments for each peripheral interface in the system. If the interrupt assignments do not match the factory installed interrupts, or if additional interrupt assignments are required, perform the Interrupt Installation procedure in this section of the manual.

25. Verify that the interface modules, memory boards, and processor boards are firmly seated in their correct positions in the chassis. If the memory installed includes a memory controller and expansion boards, ensure that the interconnections between the two boards are as shown in figure 2-12 or 2-13. The ribbon cables used to expand memory for the 96KB memory controller or the 64KB cache controller must be the type designed for the exact number of add-on memory boards to be installed in the chassis. Note that figure 2-13 illustrates the ribbon cable pair designed to accommodate four add-on memory boards.

26. Install the peripheral device interface cables on the proper interface module in the computer chassis as described in the Installation and Operation manual included with the peripheral device. All interface cables should be routed through the cable clamps at the rear of the chassis and should exit at the rear of the chassis.

27. Turn the key switch on the front panel to the ON (or UNLOCK with programmer panel) position. Observe that POWER indicator (and RUN indicator) on the front panel light and that the fans operate.

28. Perform the System Checkout Procedure specified later in this section of the manual.

29. Slide computer into cabinet to complete final installation of computer.

30. Install blank panels (if supplied) to fill open spaces in cabinet or rack.

31. Perform system software installation procedures for the operating system to be used with the computer. For Texas Instruments supplied software, this information is provided in the System Operation Guide for the specific software package.

SLOT NUMBER	P1 FIXED CRU BASE ADDRESS	P1 CIRCUIT BOARD	P1 INTER-RUPT LEVEL	P2 FIXED CRU BASE ADDRESS	P2 CIRCUIT BOARD	P2 INTER-RUPT LEVEL
1	N/A	990/10 AU2	N/A	N/A	990/10 AU2	N/A
2	02E0	990/10 AU1	N/A	02C0	990/10 AU1	N/A
3	02A0	MEMORY	N/A	0280	MEMORY	N/A
4	0260	MEMORY	N/A	0240	MEMORY	N/A
5	0220	MEMORY	N/A	0200	MEMORY	N/A
6	01E0	MEMORY	N/A	01C0	MEMORY	N/A
7	01A0	DS31/32 DISC CONTROLLER	13	0180	DS31/32 DISC CONTROLLER	13
8	0160	TAPE CONTROLLER	9	0140	TAPE CONTROLLER	9
9	0120	CRT 2 OR CRU EXPANDER	8	0100	CRT 2 OR CRU EXPANDER	10
10	00E0	CRT 1	12	00C0	CRT 1	11
11	00A0	FLOPPY DISC CONTROLLER	3	0080	FLOPPY DISC CONTROLLER	7
12	0060	LINE PRINTER	14	0040	CARD READER	4
13	0020	PROM PROGRAMMER	15 (NOT USED)	0000	733 ASR/KSR	6

(A)133089

Figure 2-11. 13-slot Chassis Pre-wired Configuration

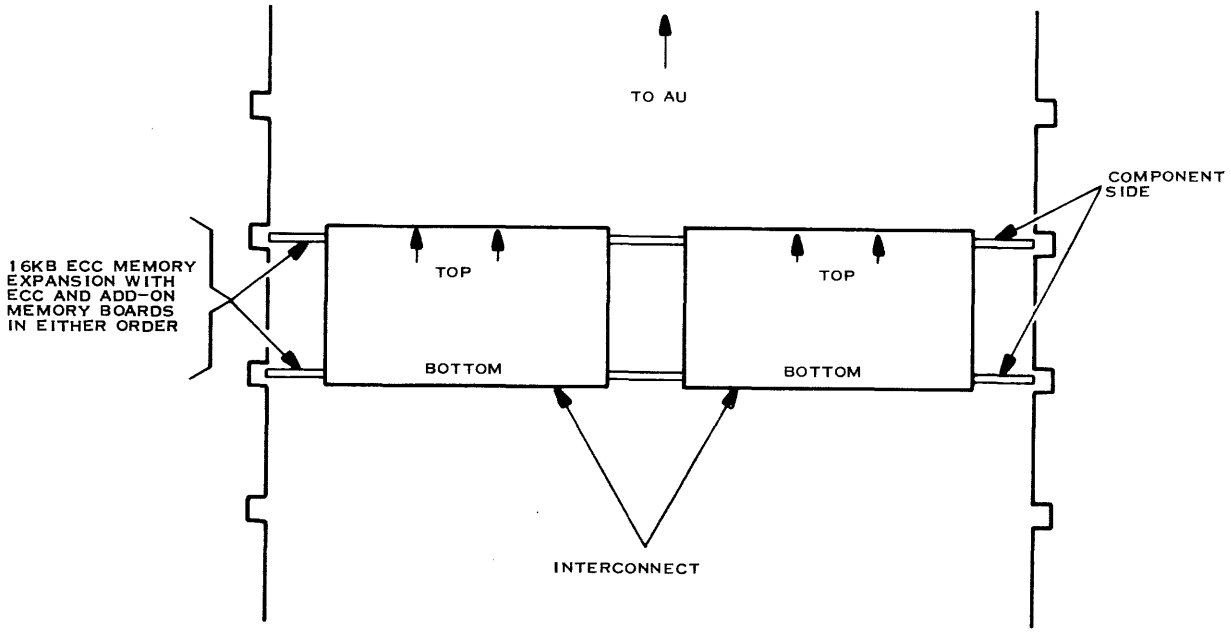


Figure 2-12. Interconnect Diagram for 16KB Memory Expansion with ECC and Add-on Memory Modules

2.5 INTERRUPT INSTALLATION

The computer chassis is shipped from the factory with predetermined interrupts installed. These interrupt assignments are listed in the installation procedure for the particular chassis elsewhere in this section. If the interrupts do not meet the requirements of the system being installed, they may be easily modified. Wiring in the backplane of the chassis brings the interrupts from each connector to a pair of jumper plugs located on the backplane above the AU2 circuit board. Similarly, backplane connections bus the interrupt inputs to the processor to the jumper plug connections. Installing jumper wires in the jumper plugs connects the interrupts from the modules in the chassis to the appropriate interrupt level input to the processor. Modification of the predetermined interrupt configuration is a three part procedure consisting of:

- Preparation and planning
- Modification of jumper plug
- Reinstallation of system

NOTE

Modification of the predetermined interrupt configuration may cause standard system software packages to fail without apparent cause.

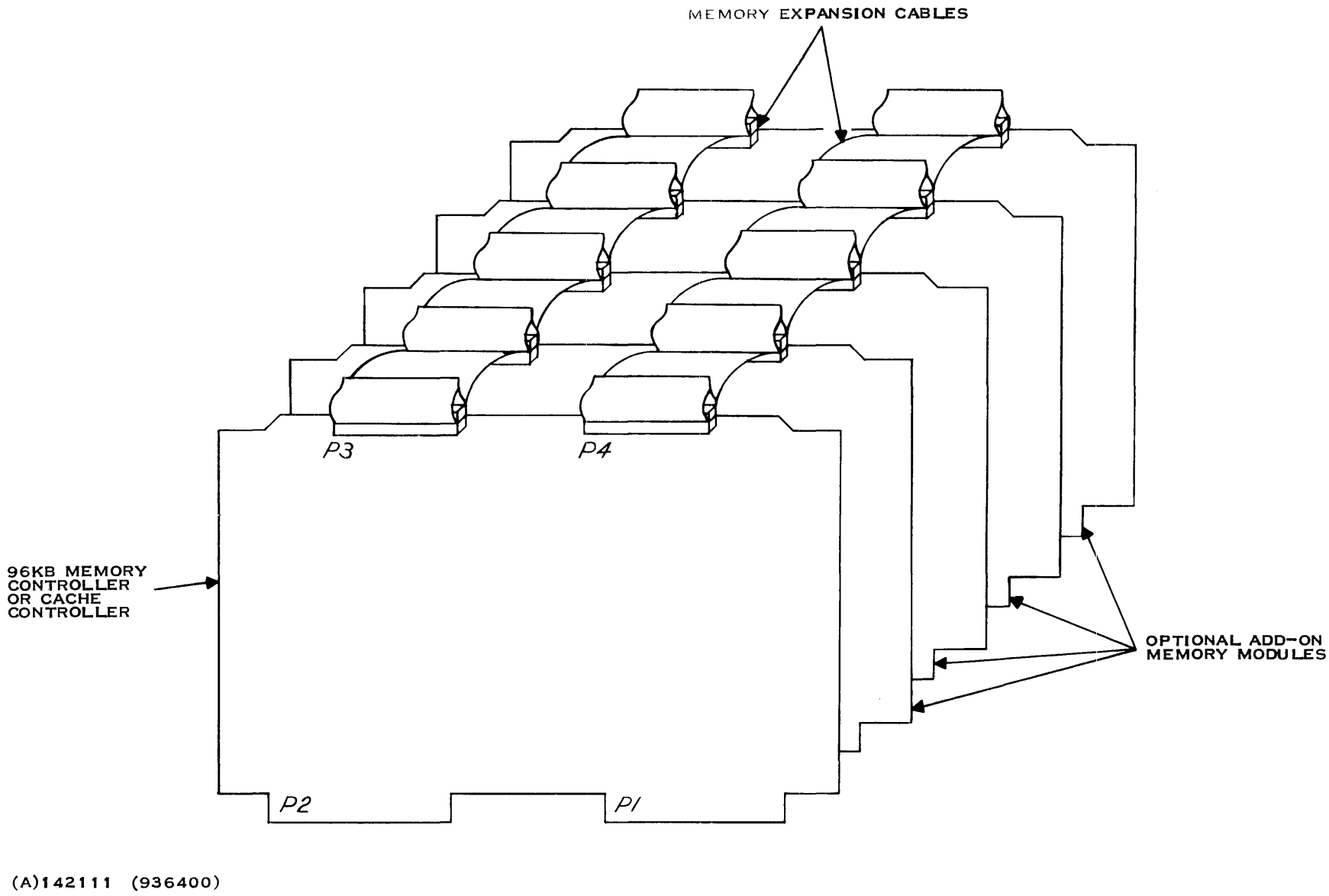


Figure 2-13. Memory System Interconnect, 16K RAM

2.5.1 **PREPARATION AND PLANNING.** To ensure that the interrupt configuration is correctly installed and does not upset the operation of the software system that will control the system, proper planning of the chassis configuration is required. To aid in this planning, figure 2-14 provides a chassis configuration chart for each type of chassis that should be completed with the information for the system being installed. The following steps outline the procedure to prepare for modifying interrupts in either chassis:

1. Fill-in the locations in the chassis configuration chart with the modules that comprise the system to be installed. Observe the following restrictions:

   a. The processor circuit board(s) must occupy the topmost slot(s) in the chassis (990/10 AU1 in slot 2 and AU2 in slot 1).

   b. The memory circuit boards should occupy the slots immediately below the processor.

   c. CRU addresses for interface modules that are assigned by the system software must correspond to the CRU address of the chassis slot in which the module is installed. Texas Instruments supplied software expects the modules to be located in the slots designated in the chassis installation procedures in this section.

2. Determine the interrupt level that each interface module or controller will be assigned and enter those assignments in the "Interrupt Level" column of the chassis configuration chart. More than one module may be assigned to a particular interrupt level if the interrupt service routine for that level interrupt can determine the source of the active interrupt.

CAUTION

Ensure that the key switch on the front panel of the chassis is turned off before removing circuit boards from the chassis. Failure to observe this caution could result in damage to circuit board components.

3. Remove enough circuit boards from the chassis to enable free access to the interrupt jumper plug as illustrated in figure 2-15. Typically, this operation requires removal of the boards in at least locations A1 through A5.

4. Remove the two jumper plugs from the backplane by pulling firmly out on the plugs. Do not twist or bend the plug during removal.

2.5.2 **MODIFICATION OF JUMPER PLUG.** The jumper plugs are molded plastic connectors with two rows of square holes for inserting jumper wires. The jumper plug for the 6-slot chassis has 10 holes in each row; the jumper plug for the 13-slot chassis has 24 holes in each row. Each hole has a plastic detent that holds the jumper wire in place when it is completely inserted into the hole. Figure 2-16 illustrates the mating of the jumper wire with the plastic jumper plug. Notice that the brass connector on the jumper wire must be oriented properly when inserted into the jumper plug so that the plastic detent can engage the slot in the top of the jumper wire brass connector. The jumper wire can be removed from the jumper plug by lifting up on the plastic detent to free the jumper wire brass connector to slide out the rear of the jumper plug. The spring force of the detent is slight enough that only a fingernail is required to lift it up to release the jumper wire.

SLOT NUMBER	P1 (CHASSIS FRONT) FIXED CRU BASE ADDRESS	CIRCUIT BOARD	INTER-RUPT LEVEL	P2 (CHASSIS REAR) FIXED CRU BASE ADDRESS	CIRCUIT BOARD	INTER-RUPT LEVEL
1	N/A	990/10 AU2	N/A	N/A	990/10 AU2	N/A
2	02E0	990/10 AU1	N/A	02C0	990/10 AU1	N/A
3	02A0			0280		
4	0260			0240		
5	0220			0200		
6	01E0			01C0		
7	01A0			0180		
8	0160			0140		
9	0120			0100		
10	00E0			00C0		
11	00A0			0080		
12	0060			0040		
13	0020			0000		

13-SLOT CHASSIS

	FIXED CRU BASE ADDRESS	CIRCUIT BOARD	INTER-RUPT LEVEL	FIXED CRU BASE ADDRESS	CIRCUIT BOARD	INTER-RUPT LEVEL
1	N/A	990/10 AU2	N/A	N/A	990/10 AU2	N/A
2	0120	990/10 AU1	N/A	0100	990/10 AU1	N/A
3	00E0			00C0		
4	00A0			0080		
5	0060			0040		
6	0020			0000		

6-SLOT CHASSIS

(A)133095

Figure 2-14. Chassis Configuration Charts

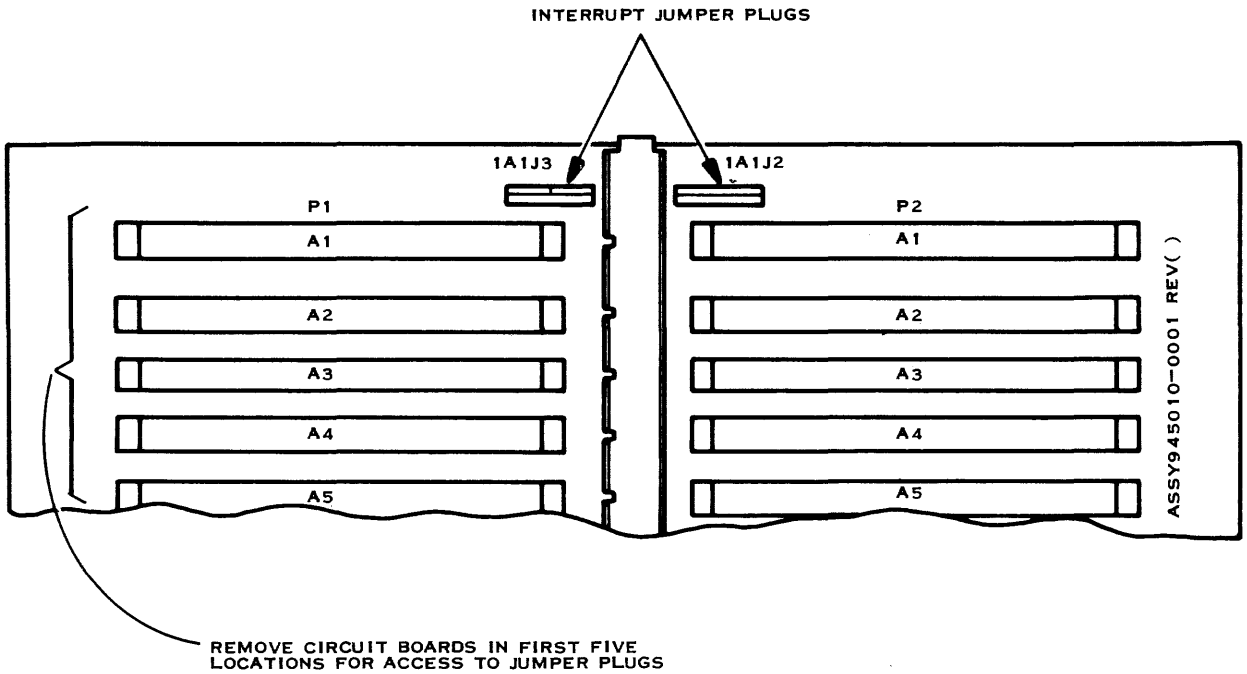


Figure 2-15. Location of Interrupt Jumper Plugs (6- and 13-Slot Chassis)

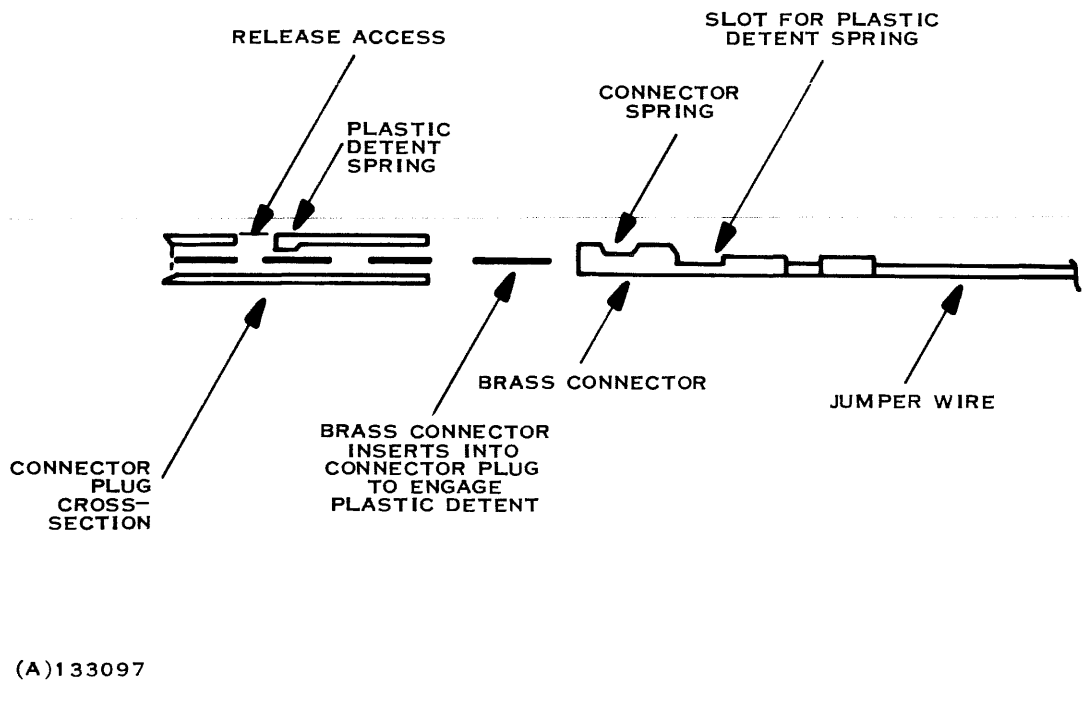


Figure 2-16. Interrupt Jumper Wire Installation

NOTE

There are two configurations of interrupt jumper connections for the 13-slot chassis. One configuration has two rows of jumper pins that connect to the individual half-sized chassis slots with a third row of pins that connect to the 15 interrupt levels. Connections and daisy-chaining for this configuration are made in the same manner as described in paragraph 2.5.2 except that no jumper plug is provided and the jumper wires are individually connected to the chassis jumper pins.

Figures 2-17 and 2-18 illustrate the position assignments on the interrupt plugs for the 6- and the 13-slot chassis, respectively, as seen from the jumper wire side. The "X" marks identify jumper plug positions which have no corresponding pins on the header. The "O" marks identify jumper plug positions which have no corresponding pins on the early production header. Notice that each interrupt generated by a module has two positions on the plug assigned to it. This configuration allows interrupts that will be recognized on the same level to be daisy-chain linked to each other. For example, if the interrupts generated by the modules in locations 6P1, 5P2 and 4P2 are to be level 7 interrupts, the chain would be connected as follows:

1. Insert one end of a jumper wire in the hole assigned to Level 7 and the other end of that jumper wire into one of the two holes assigned to 4P2.

2. Insert one end of a second jumper wire into the second hole assigned to 4P2, and the other end of that jumper wire into one of the two holes assigned to 5P2.

3. Insert one end of a third jumper wire into the second hole assigned to 5P2, and the other end of that jumper wire into one of the two holes assigned to 6P1.

The resulting jumper configuration would appear as illustrated in figure 2-19.

To install the jumper configuration for the system being modified, refer to the chassis configuration chart and perform the following steps:

1. Determine if any of the factory installed jumper wires are still valid interrupt assignments for the modified system, and remove the factory installed jumper wires that are not valid.

2. Determine all locations that generate an interrupt for one of the active priority levels and connect them together similar to the method used in the example.

3. Repeat step 2 for all active interrupt levels.

2.6 REINSTALLATION OF SYSTEM

When the jumper plugs have been modified to suit the interrupt configuration required for the system, perform the following steps to reconstruct the system:

1. Insert the reconfigured jumper plugs into their proper positions on the backplane of the computer chassis. Ensure that they are oriented correctly with the interrupt connections along the top edge and the generated interrupts along the bottom edge.

2. Consult the chassis configuration chart that was filled out for the modified system and install the circuit boards into the chassis according to those assignments. Ensure that the component side of the circuit boards faces up.

3. Return to the chassis installation procedure for the specified chassis in this section and ensure that all steps in that procedure have been properly performed.

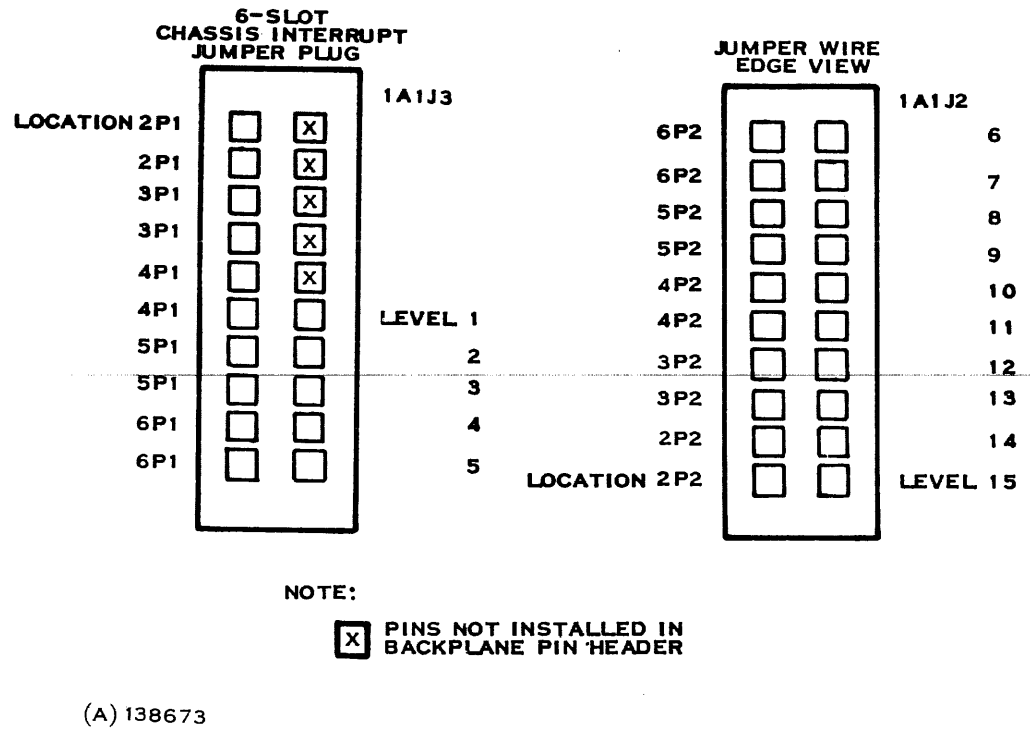


Figure 2-17. Interrupt Jumper Plugs for 6-Slot Chassis

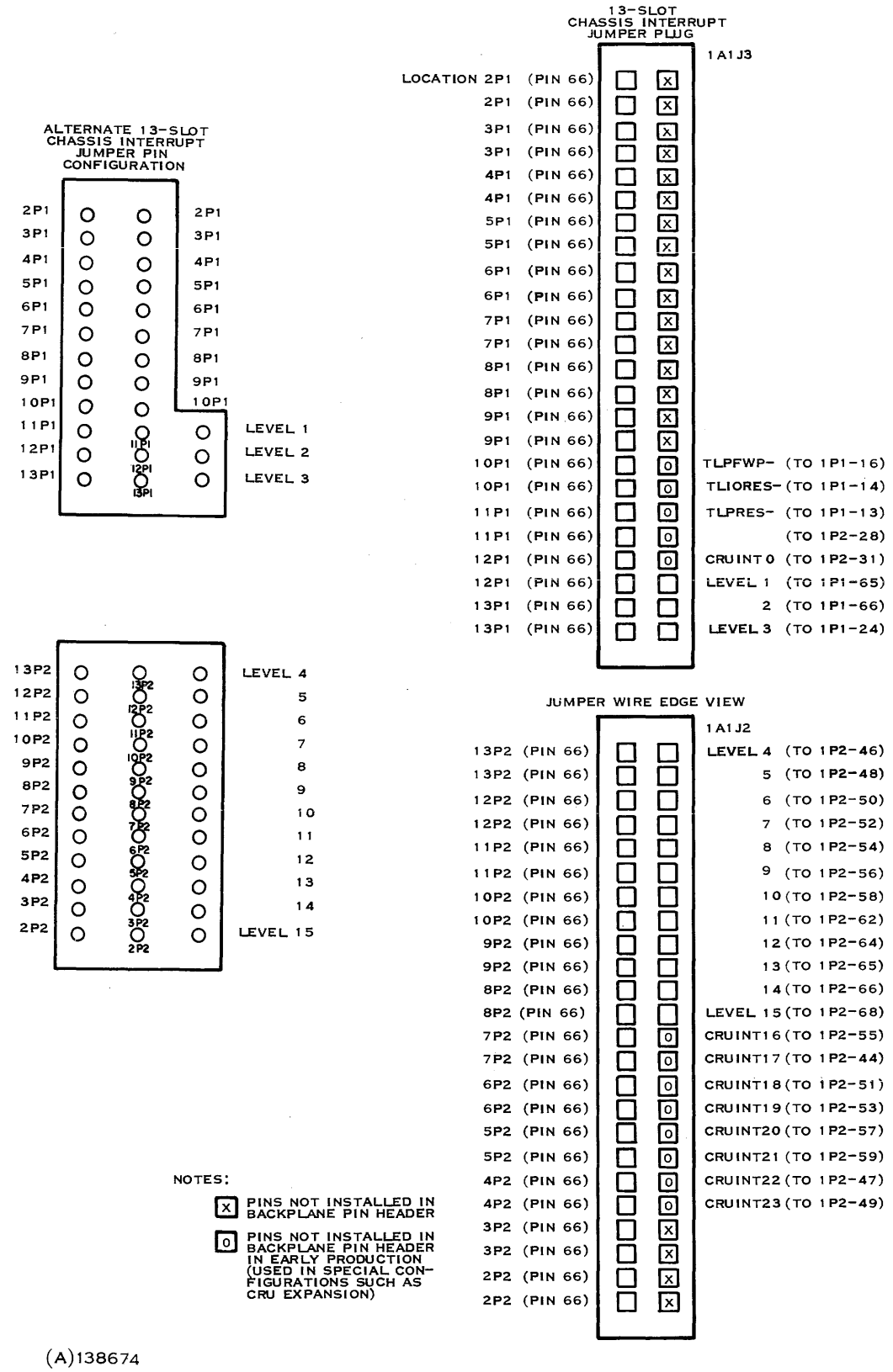
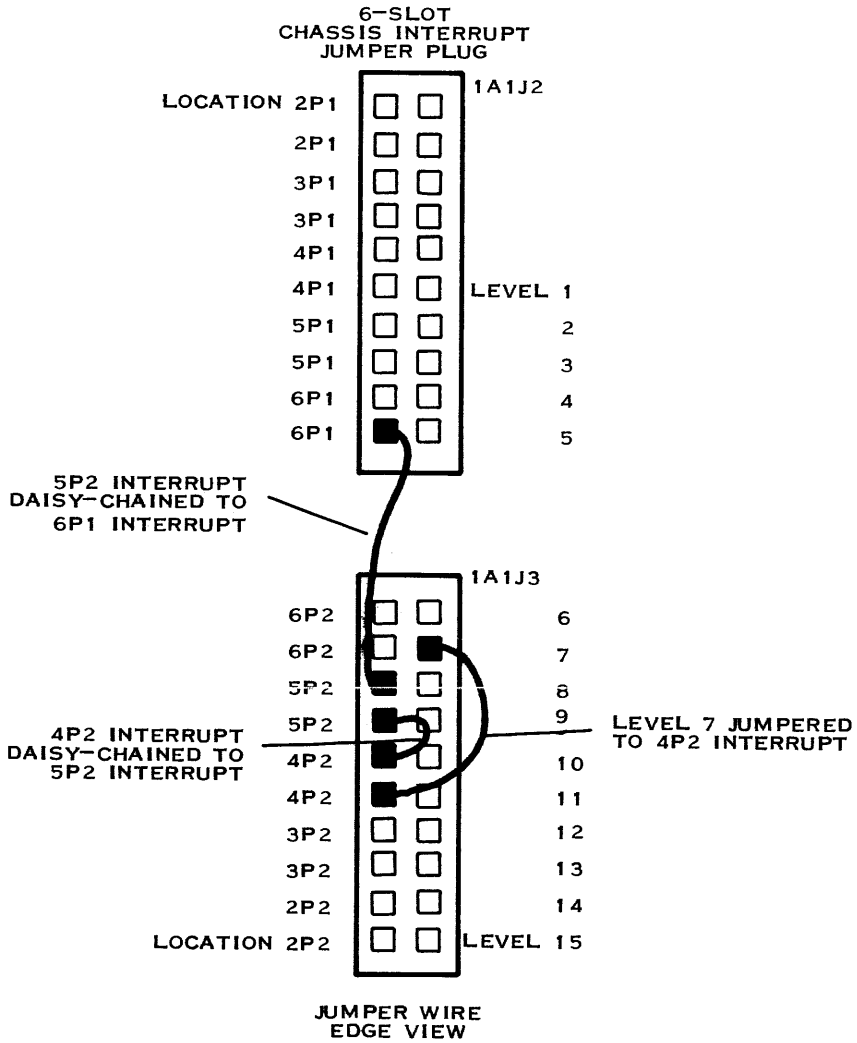


Figure 2-18. Interrupt Jumper Plugs for 13-Slot Chassis



(A)133100

Figure 2-19. Jumper Plug Daisy-Chain Sample Connection

4. If additional CRU expansion chassis are being used, refer to the CRU expansion installation requirements (paragraph 2.9).

5. Inspect all memory boards for proper jumper wiring (paragraph 2.8).

6. If additional TILINE expansion chassis are required, refer to paragraph 2.10 for additional instructions.

7. Install boards in accordance with paragraph 2.11.

8. Refer to applicable peripheral installation and operation manuals (see Preface) and install all peripheral interface modules and module to peripheral cabling.

9. Perform system checkout in accordance with paragraph 2.12.

2.7 ARITHMETIC UNIT

The central processor can be directed to one of two vectors when a power-up condition occurs. The normal setting is to the load vector in ROM code at addresses $FFFC_{16}$ and $FFCE_{16}$. This can be changed to direct the central processor to the interrupt level 0 vector by installing a jumper between terminals E1 and E2 on the printed circuit board for arithmetic unit assembly 944930, revision R and later (see figure 2-20). This jumper option is not available on earlier versions of the printed circuit board nor on any revision level of the multiwire arithmetic unit assembly 946625.

2.8 MEMORY CONFIGURATION

The starting address associated with each RAM or EPROM memory board is normally set up at the factory. For changes to the standard memory system, refer to the memory board address settings provided in Section 3 of this manual.

2.9 CRU EXPANSION INSTALLATION REQUIREMENTS

Up to seven I/O expansion chassis may be connected to the main chassis when configuring larger 990/10 Systems. The electrical interconnection between the main chassis backpanel and the expansion chassis is accomplished via the CRU expansion board which is installed in an unused card slot in the main chassis. The CRU expansion board contains seven top-edge connectors designated P3 through P9 (see figure 2-21), each of which contains all necessary data, address, interrupt and interrupt identification lines required to link an external chassis to the main chassis.

Typically, the plugs are assigned to expansion chassis as follows:

- P3 – expansion chassis 1 (buffer board in slot 1 of the expansion chassis must also be programmed for the chassis 1 ID).
- P4 – expansion chassis 2

  ⋮
- P9 – expansion chassis 7

2.9.1 CRU EXPANSION BOARD JUMPER OPTIONS. The jumper options on the CRU expansion board include:

- Jumper-wire selection of either power-up reset signal (TLPRES–) from the power supply or IORES– from the AU board in the main chassis. Typically, the IORES– signal is used which includes an OR of the main chassis power supply power-on reset and the software CLR instruction (jumper connected between terminals E3 and E4, and terminals E1 and E2 are both open).
- Interrupt section enable option. If four or less expansion chassis are being used, interrupt Section A should be enabled (jumper wire between E5 and E6). If five or more chassis are being installed, both sections must be enabled.

These jumper options are shown in figure 2-21 and summarized in table 2-2.

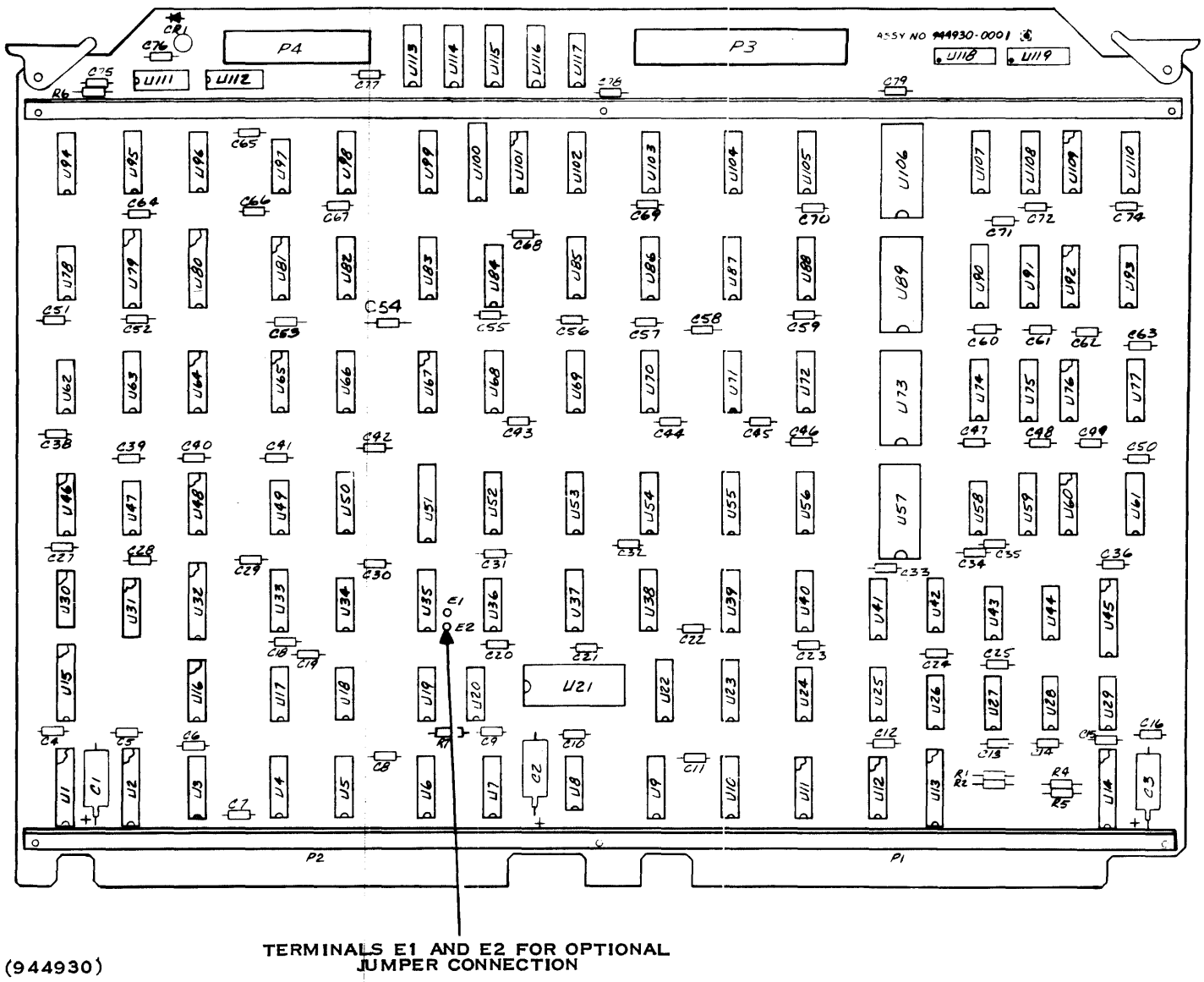


Figure 2-20. AU Board, Part Number 944930, Revisions R and Later

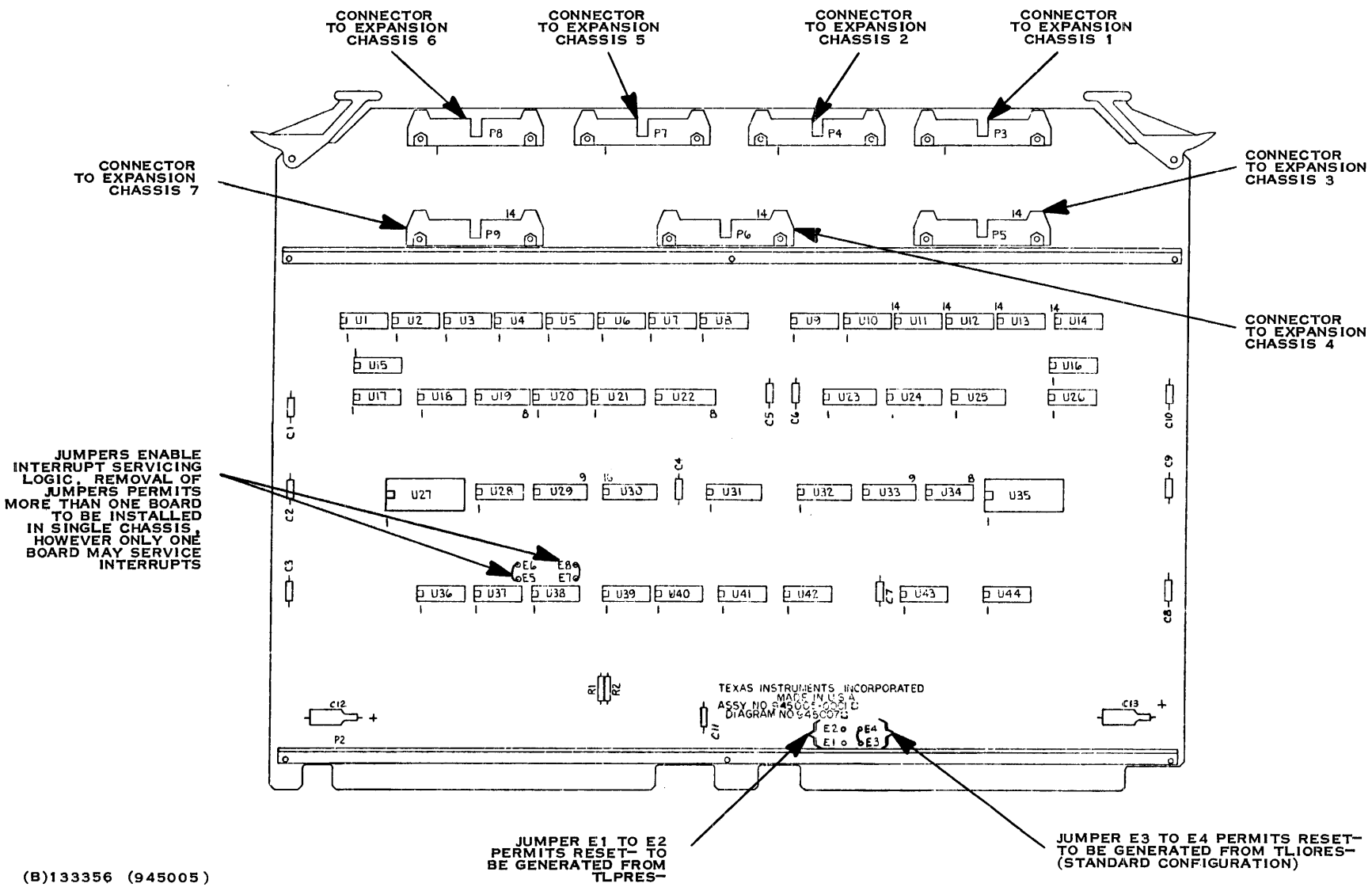


Figure 2-21. CRU Expansion Board Options

Table 2-2. CRU Expansion Board Jumper Options

Reset Source	Jumper Required
TLPRES–	Jumper E1 to E2, E3 and E4 OPEN
IORES–	Jumper E3 to E4; E1 and E2 OPEN

Interrupt Section Enable Option	Jumper Required
Interrupt Section A enabled	Jumper E5 to E6
Interrupt Section B enabled	Jumper E7 to E8

2.9.2 CRU BUFFER BOARD JUMPER OPTIONS. The CRU buffer board in each expansion chassis must be programmed with the proper chassis ID. In the standard configuration, the chassis which is cabled to P3 on the CRU expansion board in the main chassis is designated chassis 1, and the expansion chassis connected to J9 is designated chassis 7 (in numerical order). The chassis ID must then be programmed on the CRU buffer board which is installed in slot 1 of each expansion chassis. The chassis ID is set up by installing plug P4 in the selected position 1 through 7 (see figure 2-22).

The CRU buffer board also contains provisions for bypassing the interrupt scanner for interrupt level 1 when a peripheral requiring fast interrupt response time is implemented in an expansion chassis. In this case, J1 is installed in DI1 and DI2. For normal interrupt scanner processing of interrupt level 1, J1 is installed in DI3 and DI4.

For normal operation, the internal clock disable jumper must not be installed between terminals E1 and E2. For maintenance purposes, the internal clock may be disabled by installing this jumper. An external clock source may be connected to the board via terminal E3, and the scan counter may be cleared by temporarily applying a ground to terminal E4. The CRU buffer board jumper options are summarized in table 2-3.

Table 2-3. CRU Buffer Board Jumper Options

Chassis ID Select	Jumper Required
1	P4 in position 1 of J2
2	P4 in position 2 of J2
.	.
.	.
.	.
7	P4 in position 7 of J2

Internal Clock Option	Jumper Required
Normal operating system	E1 and E2 open
User supplied interrupt	E1 to E2
Scanner clock	External clock to E3

Vectored/Direct Interrupt Option	Jumper Required
Level 1 vectored	J1 in DI3, DI4
Level 1 direct	J1 in DI1, DI2

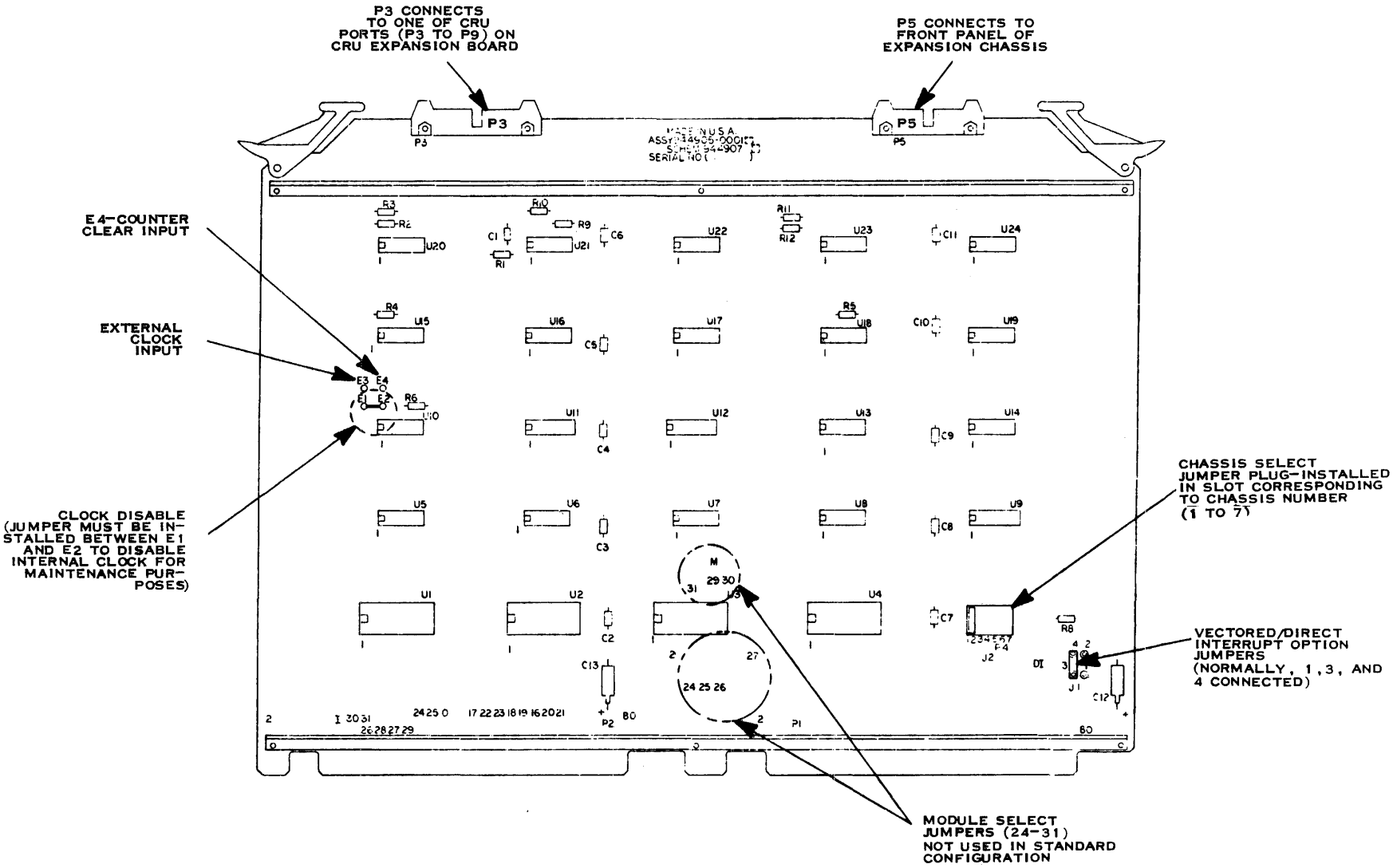


Figure 2-22. CRU Buffer Board Options

2.9.3 EXPANSION CHASSIS INTERRUPT WIRING. The interrupt wiring for each expansion chassis is performed in a similar fashion to that used in the main chassis.

2.10 TILINE EXPANSION

Multiple TILINE chassis to accommodate expansion memory and/or TILINE controllers may be installed on a 990/10 system. The TILINE electrical interconnections between the main chassis backpanel and the backpanel of a 990 expansion chassis are accomplished by installing a TILINE coupler module in the main chassis and a similar TILINE coupler in a 990 expansion chassis. The two couplers are interconnected via two 3.66-metre (12-foot), 60-ohm, shielded, ribbon cables (one 40-conductor cable and a 20-conductor cable). The cabling configuration is shown in figure 2-23.

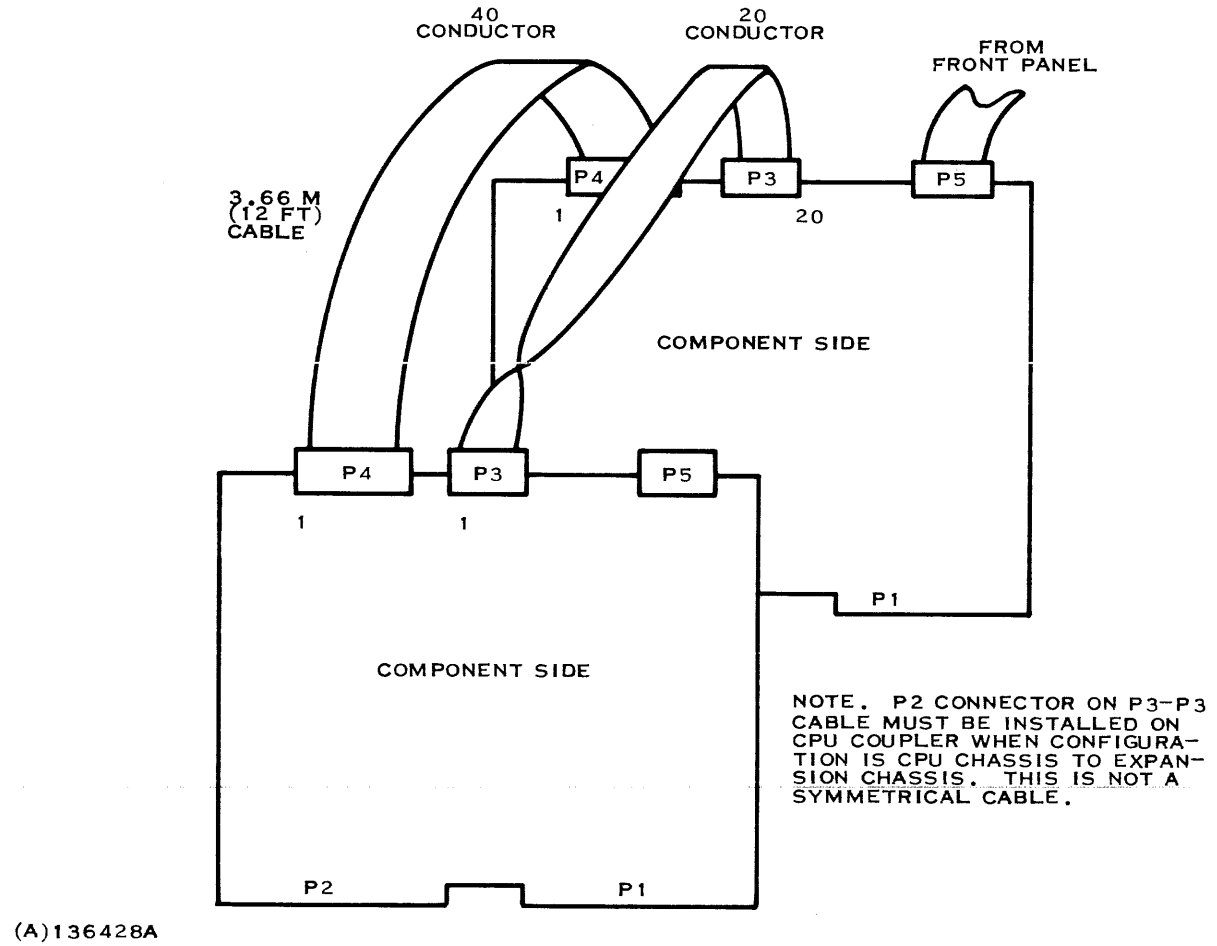


Figure 2-23. TILINE Expansion Cabling

The functions of the TILINE couplers include:

- Address and data buffering between TILINEs
- Address translation for remote memory mapping
- Resolution of timing conflicts in multiprocessor systems
- Providing intersystem interrupt capability and power status via the CRU.

There are two major types of TILINE devices, masters and slaves. TILINE masters, such as a 990/10 processor, may initiate data transfer operations on the TILINE. Slave devices, such as an expansion memory, are commanded by a master to accept or to transmit data. Some TILINE peripherals, such as a disc controller, can operate either as masters or slaves.

Each TILINE coupler module contains both a TILINE master controller and a TILINE slave controller. When the master controller requests TILINE access, it competes with other TILINE masters in that chassis in the same manner as any other master. Thus all chassis considerations for TILINE master controllers (i.e., TLAG jumper must be removed) must be observed.

In order to resolve conflicts between multiple masters contending for TILINE control, a positioned priority scheme is used. The TILINE access granted signal which establishes positional priority among masters is wired along the P2 side of the chassis. The TILINE master installed in the highest numbered slot has the highest priority, with priority decreasing with each slot toward the central processor location (or slot 1).

The TILINE access granted signal from a higher priority master enters each master on P2, pin 6. The signal leaves the master on P2, pin 5. Logic on the master allows it to block the output to lower priority masters. Jumpers are installed on the backplane to assure line continuity across slots not occupied by TILINE masters. Additional TILINE masters may be inserted at slot positions of higher or lower priority by removing the jumper between P2-5 and P2-6 (TILINE access granted) at the selected slot location.

Installing a board with TILINE master logic requires that:

- The TILINE access granted jumper (P2-5 to P2-6) must be removed from the chosen slot.

- Continuity of the TILINE access granted lines between the highest priority master and the central processor board must be preserved. This means that if an intermediate slot is assigned to a TILINE master, that master must be installed to preserve continuity and to allow the priority system to function.

2.10.1 PREPARING A SLOT LOCATION FOR A TILINE CONTROLLER. Current production assemblies have the TILINE access granted jumpers accessible from the connector side of the motherboard when all boards are removed from the chassis. These jumpers are shown in figures 2-24 and 2-25. Simply remove the jumper plug (or cut the jumper, if the jumper is a wire) for the selected TILINE controller slot, and reinstall all circuit boards in their proper location. As noted previously, the continuity of the TILINE access granted line from the highest TILINE master to the central processor must be preserved. Therefore:

1. All slots other than those containing TILINE master controllers must have the TILINE access jumper installed.

2. All master controllers must be installed in their proper location.

If the chassis is an early production version (i.e., it does not have jumpers as shown in figures 2-24 and 2-25), it is necessary to remove the back cover and power supply to gain access to the TILINE access granted jumpers. For these chassis, the following steps should be followed:

1. Turn off power and unplug the ac line cord.

WARNING

Lethal voltages are exposed when the access cover is removed. Power supply capacitors may retain charges long after ac power is removed.

2. Remove the left access cover (as viewed from the front of the chassis). The cover is fastened by four or six hex head machine screens.
3. If the chassis is a 13-slot unit with a 20-amp power supply, slots 1 through 6 are visible above the power supply. To work on them, jump to step 5.
4. Remove the power supply as follows:
   a. Disconnect color-coded connectors from the component side of the power supply board.
   b. Unscrew the machine screws and standoffs which secure the power supply to the frame and to the motherboard.
   c. Carefully pull the power supply board straight forward until the connector at the bottom center of the power supply board is disengaged from the pins protruding from the motherboard. Lift the power supply board out of the chassis.
5. The rear of the motherboard is now exposed. The P2 connectors are at the left side, closest to the fan. Refer to figure 2-26 which gives detailed views of the left end of the P2 connector in a 13-slot and a 6-slot chassis.

   In a 13-slot chassis, the TILINE access granted jumpers (P2-5 to P2-6) are wire loops soldered to the connector pins, as shown in view A.

   In a 6-slot chassis, the jumpers are part of the printed circuit board etch, as shown in view B. Note that pins 1 and 2 are concealed by the ground plane.

   To remove a jumper in the 13-slot chassis, clip the wire loop in two places and remove the excess wire. To remove a jumper in the 6-slot chassis, cut the jumper etch at two points with an X-acto* knife and lift or scrape away the excess conductor.

   To install a jumper, solder a short length of #26 AWG wire between P2-5 and P2-6.

*X-acto is a registered trademark of X-acto Corporation

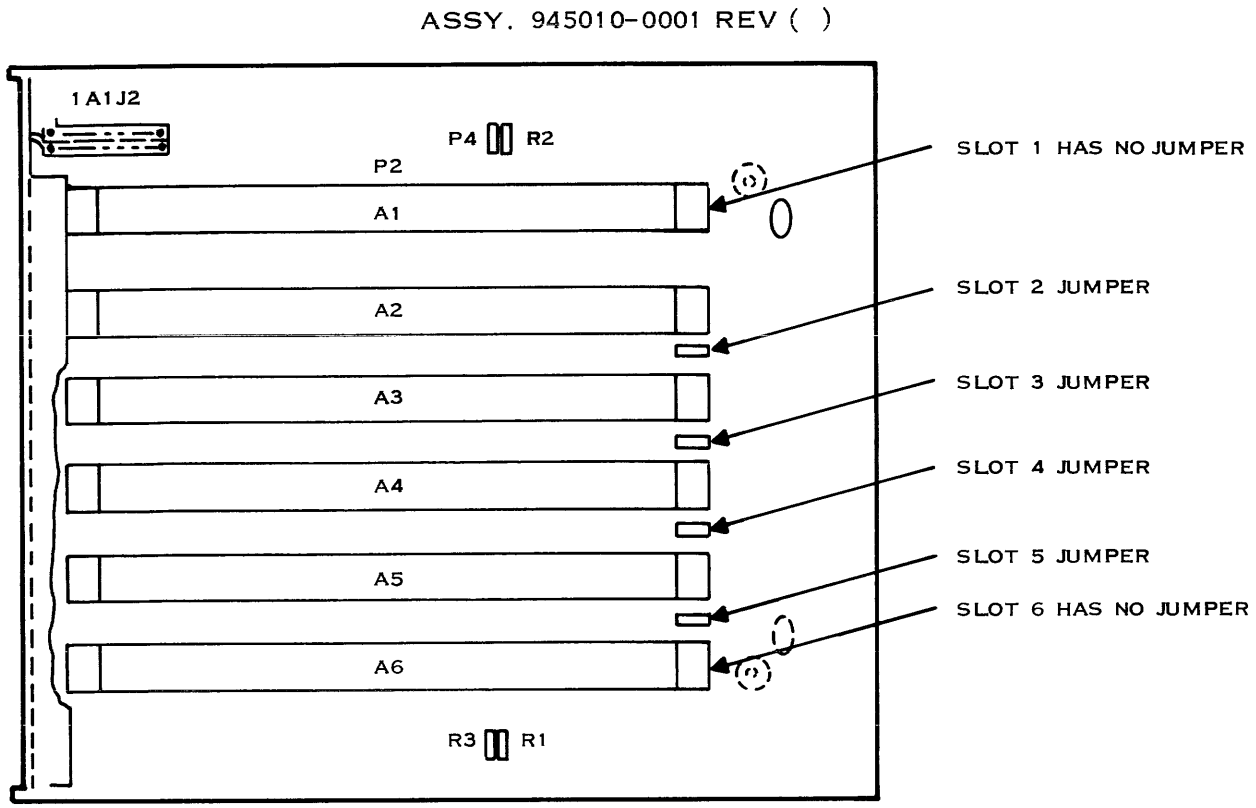


Figure 2-24. TILINE Access Granted Jumper Locations for 6-Slot Chassis (Current Production)

6. To reinstall the power supply, proceed as follows:

CAUTION

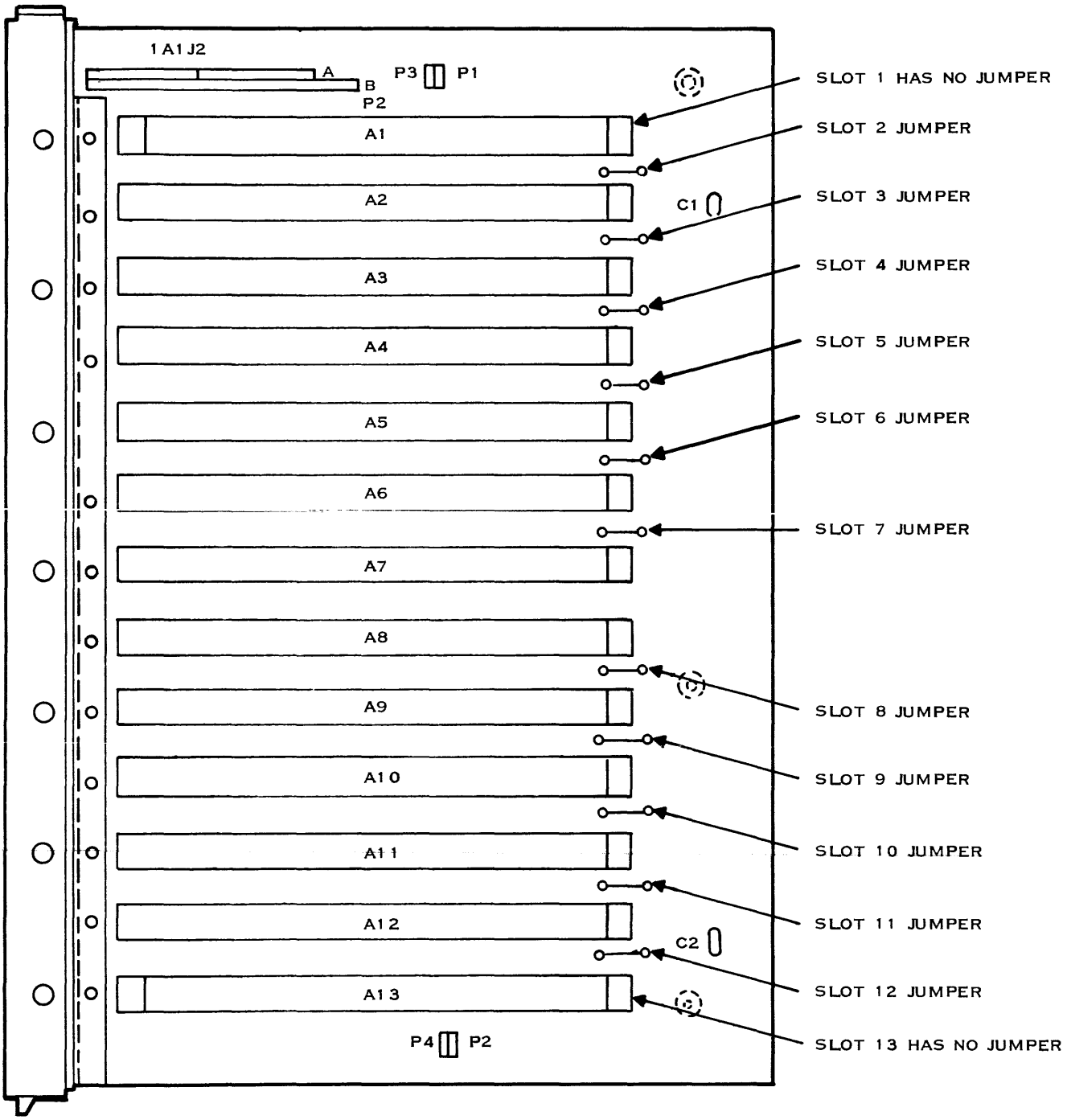
The male pins protruding from the lower center of the motherboard are subject to bending if the mating connector on the power supply is not properly aligned with these pins.

a. Slip the power supply over the cable harness and into the side of the chassis. The metal-shell jumper connector (for the standby power supply) should appear at the bottom center of the power supply board.

b. Align the power supply circuit boards on the two alignment pins and *carefully* slide the board straight back so that the pins protruding from the motherboard slip into the connector on the power supply circuit board. View of these pins is blocked by the power supply board.

c. Reinstall the machine screws and standoffs which hold the power supply in place. Do not omit the lockwashers, as both mechanical and electrical connections are made by the machine screws and standoffs.

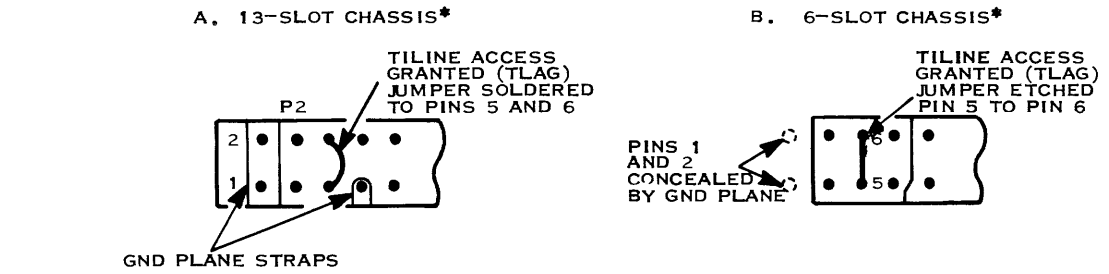
ASSY. 945015-0001 REV (R)



NOTE: JUMPER MAY BE EITHER A REMOVABLE JUMPER PLUG OR A WIRE WHICH MUST BE CUT.

(A) 138672

Figure 2-25. TILINE Access Granted Jumper Locations for 13-Slot Chassis (Current Production)



*NOTE THESE ARE REAR VIEWS OF THE 990 MOTHERBOARD, I.E., VIEWS FROM THE POWER SUPPLY SIDE.

(A) 133946A

Figure 2-26. TILINE Access Granted Jumpers on the 990/10 Motherboard

d. Reconnect the power supply to the wiring harness by installing the color-coded plastic connectors.

7. Replace the access cover.

2.10.2 TILINE COUPLER ADDRESS OPTIONS. The TILINE coupler contains three sets of switches that permit the user to assign a memory map for remote addresses. The address space recognized by the local coupler may be changed in 4K increments from 0 to 1 million words using two of the three sets of eight slide switches (figure 2-27). A bias value between 0 and 1020K (in 4K increments) may also be added to the local TILINE address before it is sent to the remote coupler. The bias value is programmed on the coupler using the third set of eight switches.

2.10.2.1 Address Recognized By Coupler. The lower bound switches are used to select the lowest address that will be recognized by the coupler. The decimal equivalent of the binary number set up by these switches is the number of the lowest 4K bank that will be recognized.

Similarly, the upper bound switches are used to enter a binary value whose decimal equivalent reflects the highest 4K bank that will be recognized. Table 2-4 contain several examples of address space and associated switch settings.

2.10.2.2. Address Bias Options. The third set of 8 slide switches permits the user to select an 8-bit bias value that may be added to the eight most significant bits of the 20-bit TILINE address before the address is passed on to the remote coupler. This bias feature allows a single block of memory or single TILINE peripheral to be shared among several CPUs. Each CPU may use a different address which is biased to the actual TILINE address by the coupler. Table 2-5 shows several examples of biasing using the bias switches on the coupler.

NOTE

If the TILINE address is within the TILINE peripheral control space ($\geq FFC00_{16}$), whether or not the bias value is added to the address is a jumper option as described in paragraph 2.10.6.

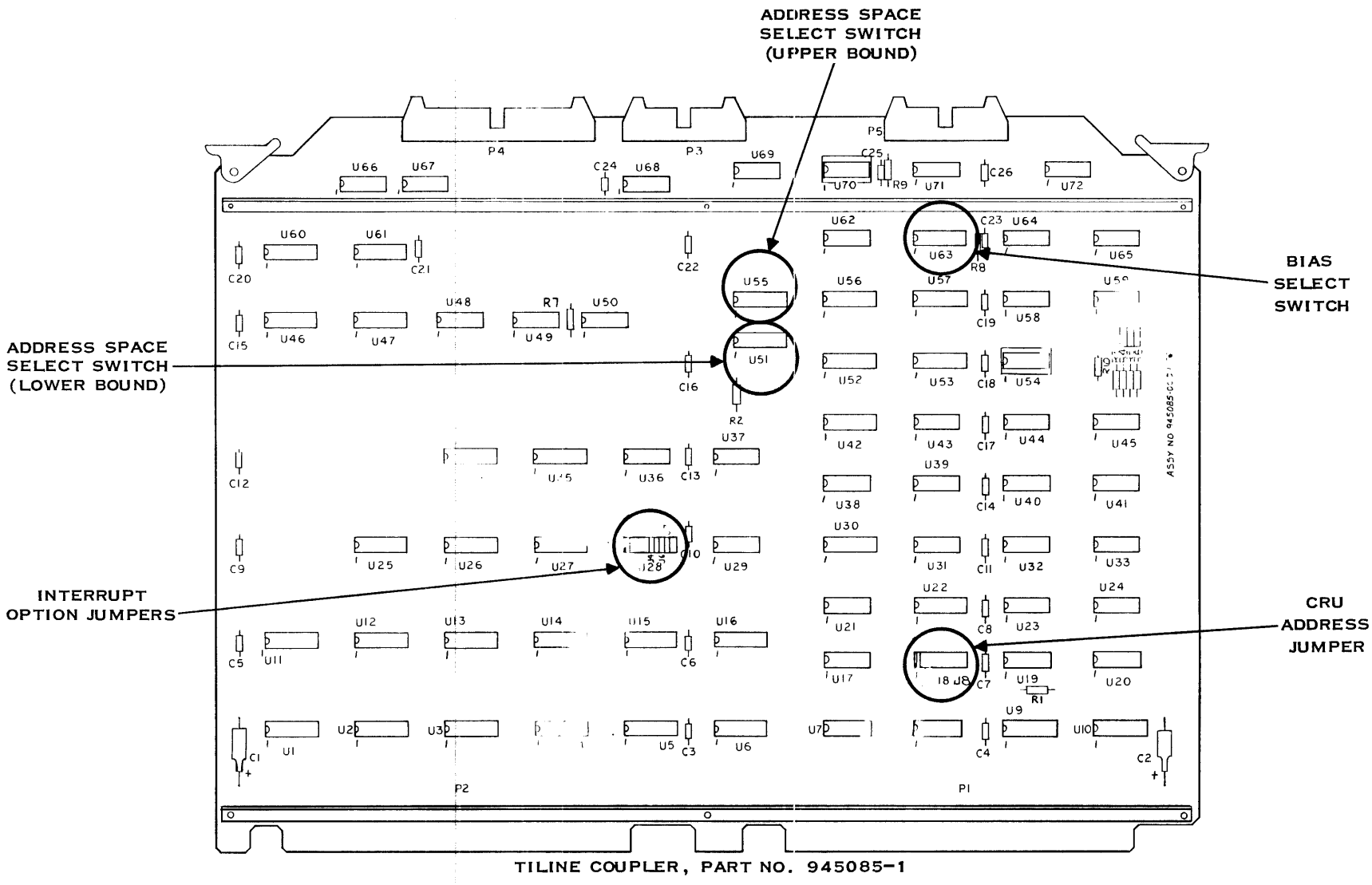


Figure 2-27. TILINE Coupler Options

Table 2-4. Examples of TILINE Coupler Address Space Switch Settings

DECIMAL	ADDRESS SPACE RECOGNIZED ADDRESSES (HEX)	LOWER BOUND SWITCH (MSB) 1 2 3 4 5 6 7 8 (LSB)	UPPER BOUND SWITCH (MSB) 1 2 3 4 5 6 7 8 (LSB)
0-4K	00000-00FFF	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0
4K-8K	01000-01FFF	0 0 0 0 0 0 0 1	0 0 0 0 0 0 0 1
8K-12K	02000-02FFF	0 0 0 0 0 0 1 0	0 0 0 0 0 0 1 0
12K-16K	03000-03FFF	0 0 0 0 0 0 1 1	0 0 0 0 0 0 1 1
0-8K	00000-01FFF	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 1
0-16K	00000-03FFF	0 0 0 0 0 0 0 0	0 0 0 0 0 0 1 1
0-20K	00000-04FFF	0 0 0 0 0 0 0 0	0 0 0 0 0 1 0 0
8K-16K	02000-03FFF	0 0 0 0 0 0 1 0	0 0 0 0 0 0 1 1
32K-64K	08000-0FFFF	0 0 0 0 1 0 0 0	0 0 0 0 1 1 1 1
64K-320K	10000-4CFFF	0 0 0 1 0 0 0 0	0 1 0 0 1 1 0 0
0	NONE	0 0 0 0 0 0 0 1	0 0 0 0 0 0 0 0

SWITCH POSITION
1 = OFF, 0 = ON

Table 2-5. Examples of TILINE Coupler Bias Switch Settings

LOCAL TILINE ADDRESS	BIAS	BIAS SWITCH 1 2 3 4 5 6 7 8 (MSB) (LSB)	REMOTE TILINE ADDRESS
00000	16K	0 0 0 0 0 1 0 0	04000
032CF	4K	0 0 0 0 0 0 0 1	042CF
02F10	1016K (-8K)	1 1 1 1 1 1 1 0	00F10
04000	992K	1 1 1 1 1 0 0 0	FC000
FFC40	1016K (-8K)	1 1 1 1 1 1 1 0	FFC40 (J7 removed) FDC40 (J7 installed)

SWITCH POSITION
1 = OFF, 0 = ON

2.10.3 TILINE COUPLER INTERRUPT OPTIONS. Each coupler includes a CRU interface for a maskable interrupt feature in which two input and two output bits are implemented, and a non-maskable interrupt that they may be jumpered as an incoming or outgoing interrupt.

2.10.3.1 CRU Dedicated Start Address Option. The coupler's CRU section may be assigned a dedicated address beginning at one of eight different addresses controlled by the position of jumper J8 as indicated in table 2-6.

Table 2-6. TILINE CRU Address Jumpers

JUMPER POSITION (J8)	CRU ADDRESS	EQUIVALENT BASE ADDRESS
1	FA0	1F40
2	FA2	1F44
3	FA4	1F48
4	FA6	1F4C
5	FA8	1F50
6	FAA	1F54
7	FAC	1F58
8	FAE	1F5C

2.10.3.2 Optional Interrupt Configurations. In addition to the CRU starting address jumper, four other jumpers (J1-J4) may be used to set up a wide variety of interrupt configurations.

Jumpers J1 through J4, when inserted, perform the following functions:

- J1 – sends direct nonmaskable interrupt out
- J2 – brings direct nonmaskable interrupt in
- J3 – sends direct maskable interrupt out
- J4 – sends CRU maskable interrupt out.

Coupler's interrupt circuitry is shown in figure 2-28. In this example, the following conditions exist:

- Disc A can directly interrupt CPU B
- CPU A can interrupt CPU B via the CRU
- CPU B can mask the interrupt from CPU A
- Disc B can interrupt CPU B
- CPU B can interrupt CPU A via the CRU.

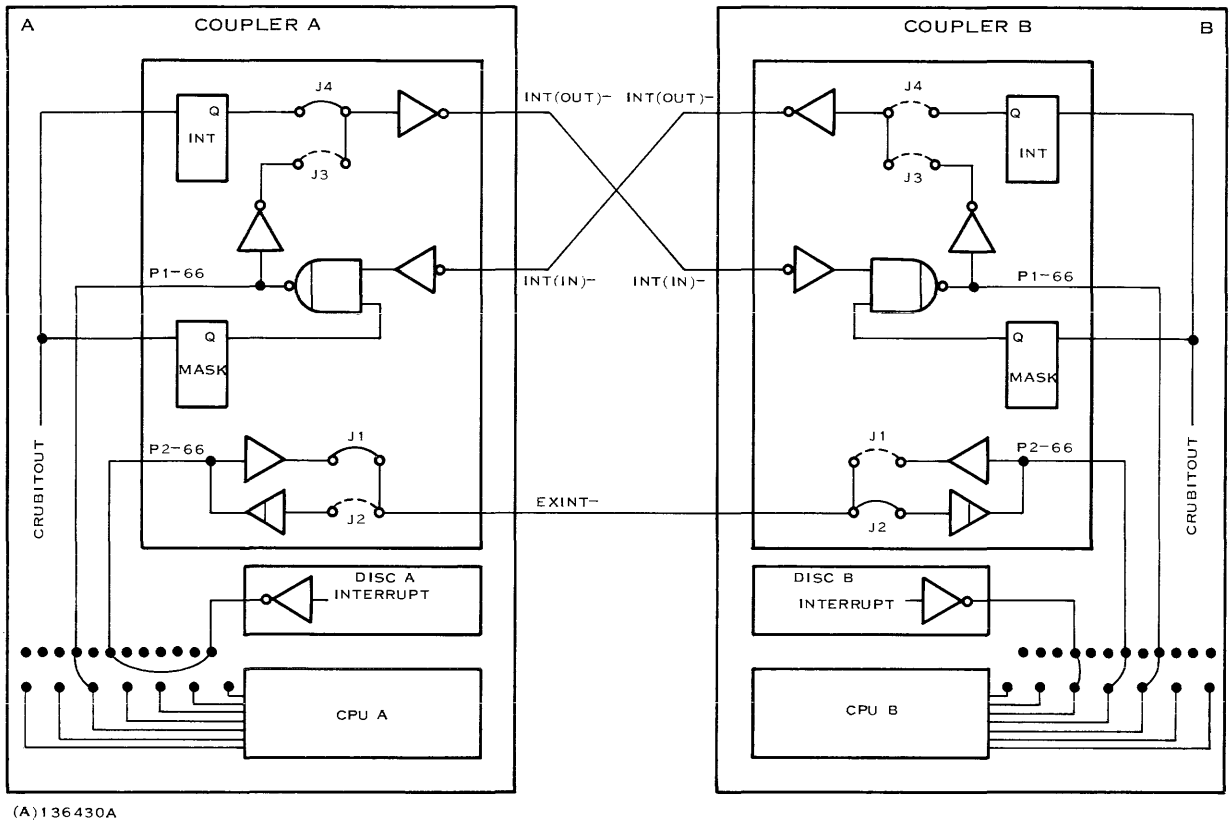


Figure 2-28. TILINE Coupler Interrupt Circuitry, Functional Block Diagram

2.10.4 IORESET JUMPER OPTION. IORESET may be propagated to the remote TILINE. Propagation of IORESET is disabled by removing jumper J5 at the originating coupler.

2.10.5 WRITING TO REMOTE SLAVE OPTION. The data path between two couplers may be assigned as read-only in one or both directions. Removal of jumper J6 at the originating coupler disables a coupler from writing to a remote slave.

2.10.6 PERIPHERAL CONTROL SPACE ADDRESS OPTION. By inserting jumper J7, the circuitry used to detect an address in the TILINE peripheral control space address is disabled. If the jumper is used, all addresses sent to the remote coupler have the bias value added in. If the jumper is removed, all addresses except those in the TILINE peripheral control space address have the bias value added.

2.11 LOGIC BOARD INSTALLATION PROCEDURES

Before installing a logic board in the main chassis or one of the expansion chassis, the chassis map located on top of the chassis should be consulted. If adding a new board to the system, consult the Preparation and Planning paragraph in this section to ensure that the interrupt and CRU addressing requirements of the system are being met. If adding a TILINE controller to the system, consult the TILINE Expansion paragraph in this section. In general, logic boards are either half-sized or full-sized boards. The half-sized boards require the addition of a center card guide into the selected card slot prior to the installation of the logic board.

Procedures for installing both types of logic boards are provided in the following paragraphs.

2.11.1 FULL-SIZED LOGIC BOARD INSTALLATION. The following procedure should be used to install a full-sized logic board into a 990 chassis:

1. Set the key switch on the chassis front panel to the OFF position.

CAUTION

Failure to shut off power to the chassis when installing or removing a logic board may result in damage to the board due to temporary misalignment of board and connector pins.

2. Insert the board into the selected slot of the chassis with the component side of the board facing upward.

3. Ensure that the slots in the circuit board mate properly with the alignment comb on the backpanel connector.

4. Press the board firmly into place, and ensure that the board is properly seated.

5. For a CRU interface board, refer to the associated Installation and Operation manual for cabling information.

6. The board may be removed from the chassis by removing the interface cable and lifting the plastic, pivoted tabs (card ejectors) to free the board from the chassis backpanel.

2.11.2 HALF-SIZED LOGIC BOARDS. Half-sized logic boards may be installed in a 990 chassis using the following procedure:

1. If a center card guide is installed in the desired slot, proceed to step 7. If the center card guide is *not* installed, proceed to step 2.

2. Disconnect the chassis ac power cord from its ac power source.

WARNING

The Center Card Guide Installation procedure requires exposure to dangerous ac voltages unless the chassis is disconnected from the ac power source.

3. If the card guide is being installed on a 6-slot or 13-slot chassis, the left-side access panel and the power supply board(s) must be removed. The standby power supply (when used) is mounted piggyback over the main power supply board. To remove the standby supply board, disconnect cable connector plugs 1A6P1 and 1A6P2, and remove five holding screws. To remove the main power supply board, disconnect cable connectors 1A3P1 and 1A3P2, and remove four holding screws and three standoffs from the center of the board.

4. Examine the card comb located between the two rows of connectors on the front side of the motherboard. If a screw is located between the two connectors in the position where the card guide is to be installed, remove the screw and associated hardware from the motherboard, and install in an adjacent hole either above or below the original location.

5. Install the center card guide, TI Part Number 945226-0001, using a flat washer and screw as shown in figure 2-29. Inspect the card guide to ensure that it is not rotated with respect to the card comb. Correct if misaligned.

NOTE

If two half-sized logic cards are being installed in the same full-sized chassis slot, center the card guide. If only one card is being installed, mount the card guide toward the side of the chassis where the logic card is being installed.

6. Replace the main power supply board and the standby power supply board (if used). Ensure that all screws and standoffs are snug and that all connectors are properly installed. Replace the side access panel.

7. Insert the logic board into the selected half-slot chassis location with the component side of the board facing upward.

8. Ensure that the slots in the circuit board mate properly with the alignment comb on the backpanel connector. Press the board firmly into position.

9. Refer to the associated Installation and Operation manual for the CRU logic card type for additional cabling information.

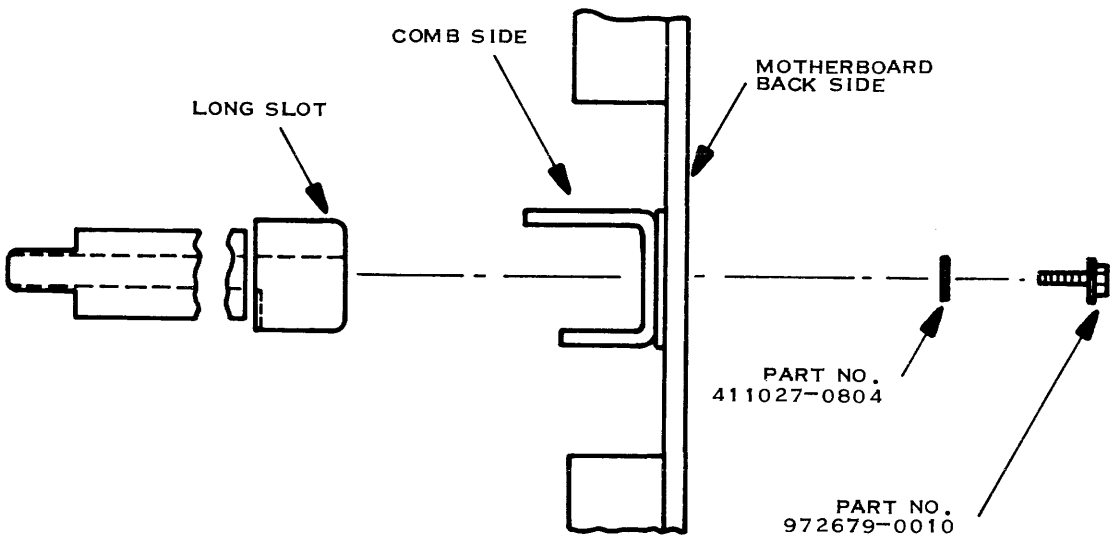


Figure 2-29. Center Card Guide Installation Diagram

2.12 SYSTEM CHECKOUT PROCEDURE

System checkout for the computer consists of loading and executing processor diagnostic tests to ensure that the computer is operating within specifications, and then loading and executing a set of hardware demonstration tests to verify that all system peripheral devices are connected properly to the computer. Refer to the Model 990 Computer Diagnostics handbook for a listing of the diagnostic tests for the 990/10 computer. This handbook also contains:

- A list of all the 990 diagnostics
- A description of the loaders and loading devices that are available and how to use them
- A description of what a standalone test is and how to run one
- A description of the available Verb packages and how to use them
- A brief description of each test.

SECTION 3

PRINCIPLES OF OPERATION

3.1 GENERAL

This section provides a block diagram level discussion for each of the three major hardware units (see figure 1-2) of the 990/10 minicomputer system including those units that are optional.

3.2 990/10 MINICOMPUTER

Three printed circuit boards; a processor board AU1, a system interface board AU2, and a memory board perform as a complete computer when installed in a chassis and provided proper power. As shown in the block diagram of figure 3-1, the interface between the central processor, the memory board, and devices external to the minicomputer is implemented with TTL installed on the system interface board. A discussion of the characteristics and capabilities of the central processor is provided in paragraph 3.2.1. Also provided are the pin assignments and functions of the interface signals between circuit boards AU1 and AU2. A description of the memory board is provided in paragraph 3.2.10 with a detailed description of the memory board as used as an integral part of the minicomputer and as used as an expansion module provided in paragraph 3.3.

The TILINE is a high-speed, bidirectional 16-bit data bus that with associated control lines is used to transfer data between all high-speed system elements that include the central processor, memory, and other rapid data transfer devices such as disc files and magnetic tape transports. The TILINE also serves as a computer-to-computer link.

Up to 512 words of on-board programmable read-only memory (PROM) may be implemented on the system interface board. Data as addressed by memory address bits MA6 through MA14 from the processor is accessed from the PROM and placed on the data input bus to the processor.

Serial data transfer between the processor and interfaces for external CRU devices is effected through CRU interface logic with control and signal lines brought to connectors P1 and P2 on the system interface board.

The programmer panel is a CRU device and separate CRU interface logic provides control and signal lines at connector P7 through which the interface to the programmer panel is made.

The system clock provides timing signals for the processor and system interface board logic. A 120-Hz signal input to the system interface board from the power supply serves as a real-time clock. Up to 13 priority-vectored external interrupt levels (levels 3 through 15) may be applied to the system interface board at connector P1. Provisions are made on the system interface board for extended operation (XOP) hardware modules that perform certain complex arithmetic and logical operations with greater efficiency than can be done with software.

3.2.1 990/10 CENTRAL PROCESSOR UNIT (CPU). The 990/10 CPU as implemented with TTL MSI logic on the AU1 circuit board incorporates the features of the Texas Instruments 990 series minicomputers and generates a 20-bit address and a 16-bit data bus. The 990 concept features multiple register files (16 registers) that reside in memory. The advanced architecture of the 990/10 CPU permits efficient programming with bit, byte, and word addressing capability and the use of multiple register files allows rapid context switching. Characteristics of the 990/10 CPU are as shown in table 3-1.

3.2.1.1 **Architecture.** The memory word of the CPU is 16 bits long. Each word is also defined as 2 bytes of 8 bits each. The instruction set of 990/10 permits both word and byte operands. Thus, all memory word locations are on even byte address boundaries. Byte instructions can address either the even or odd byte. The memory space without mapping is 65536 bytes or 32768 words. Word and byte formats are as shown in figure 3-2.

Registers and Memory. The 990/10 processor employs an advanced memory-to-memory architecture. Blocks of memory designated as workspace replace internal hardware registers as program data registers. The 990/10 memory map is shown in figure 3-3. The first 32 words are used for 16 interrupt trap vectors with the first six words used for internal interrupts and the remaining 26 words used for 13 external equipment interrupts. The next contiguous block of 32 memory words is used by extended operation (XOP) instruction for trap vectors. Those addresses in the range $F800_{16}$ through $FBFE_{16}$ (512 words) are mapped to the TILINE peripheral control space ($FFC00_{16}$ through $FFDFF_{16}$) and the last 512 words (addresses $FC00_{16}$ through $FFFE_{16}$) are preempted to address the TTL P/ROM. The remaining memory is then available for programs, data, and workspace registers. If desired, any of the special areas may also be used as general memory. Three internal registers are accessible to the user. The program counter register (PC) contains the address of the instruction following the current instruction being executed. This address is referenced by the processor to fetch the next instruction from memory and is then automatically incremented. The status register (ST) contains the interrupt mask level and status information pertaining to the instruction operation. Each bit position in the register signifies a particular function or condition that exists in the processor. Figure 3-4 illustrates the bit position assignments. Some instructions use the status register to check for a prerequisite condition, others affect the values of the bits in the register, and others load the entire status register with a new set of parameters. A description of the instruction set contained in the *Model 990 Computer Assembly Language Programmer's Guide* details the effect of each instruction on the status register.

The workspace pointer register (WP) contains the address of the first word in currently active set of workspace registers. A workspace register file occupies 16 contiguous memory words in the general memory area (see figure 3-3). Each workspace register may hold data or addresses and function as operand registers, accumulators, address registers, or index registers. Some workspace registers take on special significance during execution of certain instructions. Table 3-2 lists each of these dedicated workspace registers and the instructions that use them. During instruction execution, the processor addresses any register in the workspace by adding the register number to the contents of the workspace pointer as shown in figure 3-5.

The workspace concept is particularly valuable during operations that require a context switch (a change from one program to another or to a subroutine, as in the case of an interrupt). Such an operation using a conventional multiregister arrangement requires that at least part of the contents of the register file be stored and reloaded. A memory cycle is required to store or fetch each word. By exchanging the contents of the program counter, status register, and workspace pointer the processor accomplishes a complete context switch with only three store cycles and three fetch cycles. After the switch the workspace pointer contains the starting address of a new 16-word workspace in memory for use in the new routine and the contents of the WP, PC, and ST registers from the previous routine have been saved in new workspace registers 13, 14, and 15, respectively. A corresponding saving in time occurs when the original context is restored. Instructions in the processor that result in a context switch include: Branch and Load Workspace Pointer (BLWP), Return from Subroutine (RTWP), and Extended Operation (XOP).

Device interrupts, TLPRES–, TLPFWP–, and RESTART– also cause a context switch by forcing the processor to trap to a service routine.

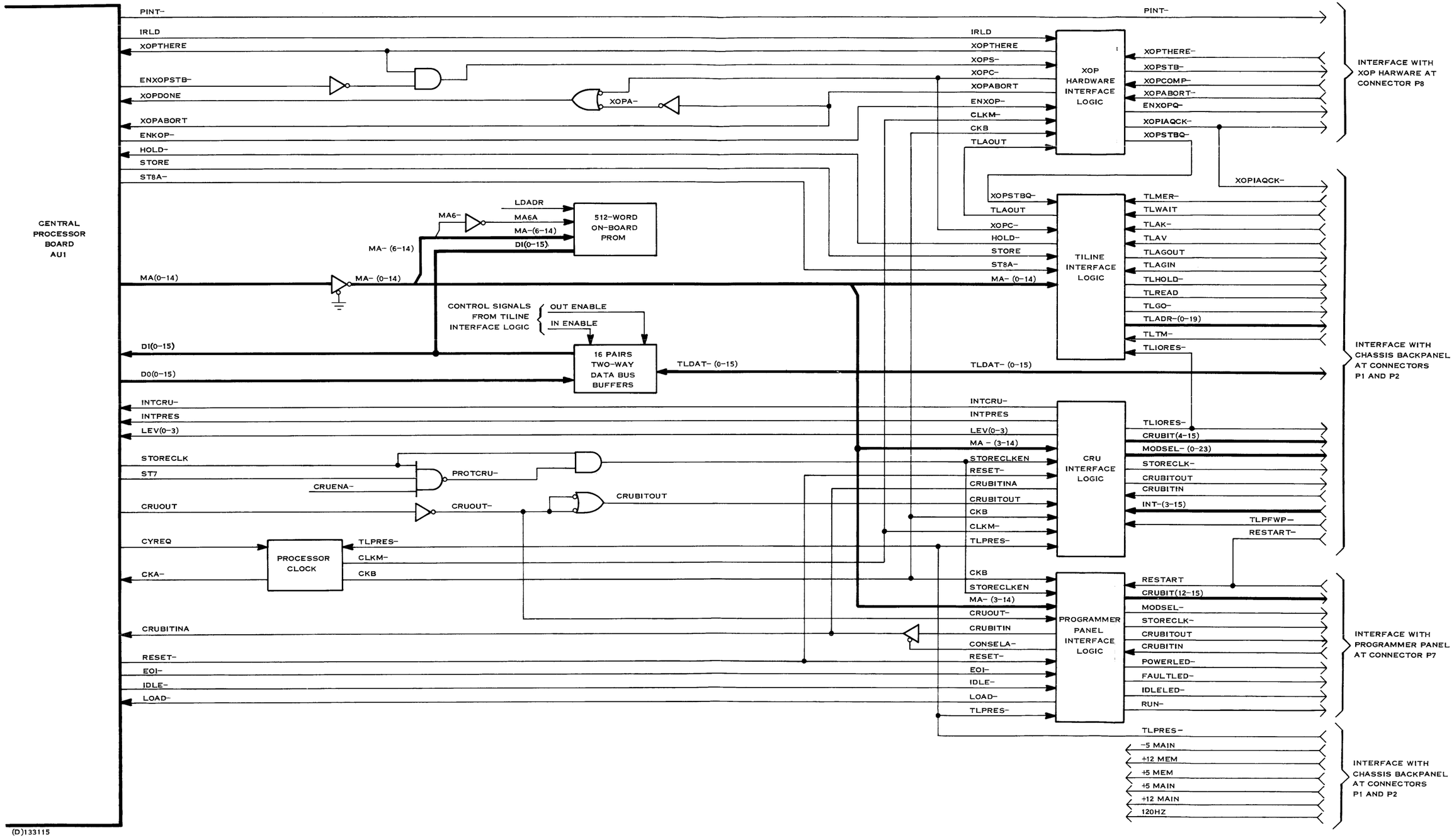


Figure 3-1. Block Diagram of System Interface Board

Table 3-1. 990/10 CPU Characteristics

Item	Characteristics
Word size	16 bits
Maximum memory addressing capability	64K bytes (without mapping), 2M bytes with mapping
Clock rate	Approximately 4 MHz
Addressing modes	Immediate
	Workspace register
	Workspace register indirect
	Symbolic memory (direct)
	Indexed memory
	Workspace register indirect autoincrement
	Program counter relative
	CRU relative
Interrupts	16 interrupts (in 13-slot chassis), 13 external
Input/output	Direct (CRU) and Direct Memory Access
Address bus	15 bits (Internal processor), 20 bits (TILINE)
Data bus	16 bits
Power	+12 vdc, ±5 vdc
Board size	274.32 by 361.95 mm (10.80 by 14.25 in.)

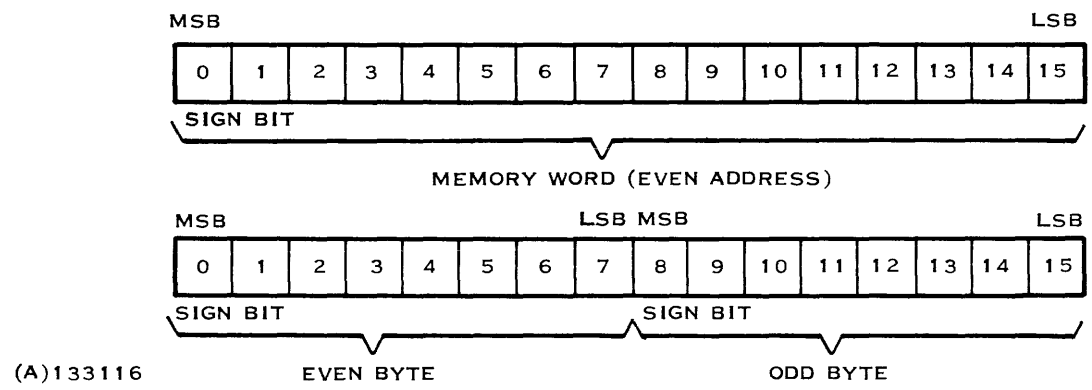


Figure 3-2. Processor Word and Byte Format

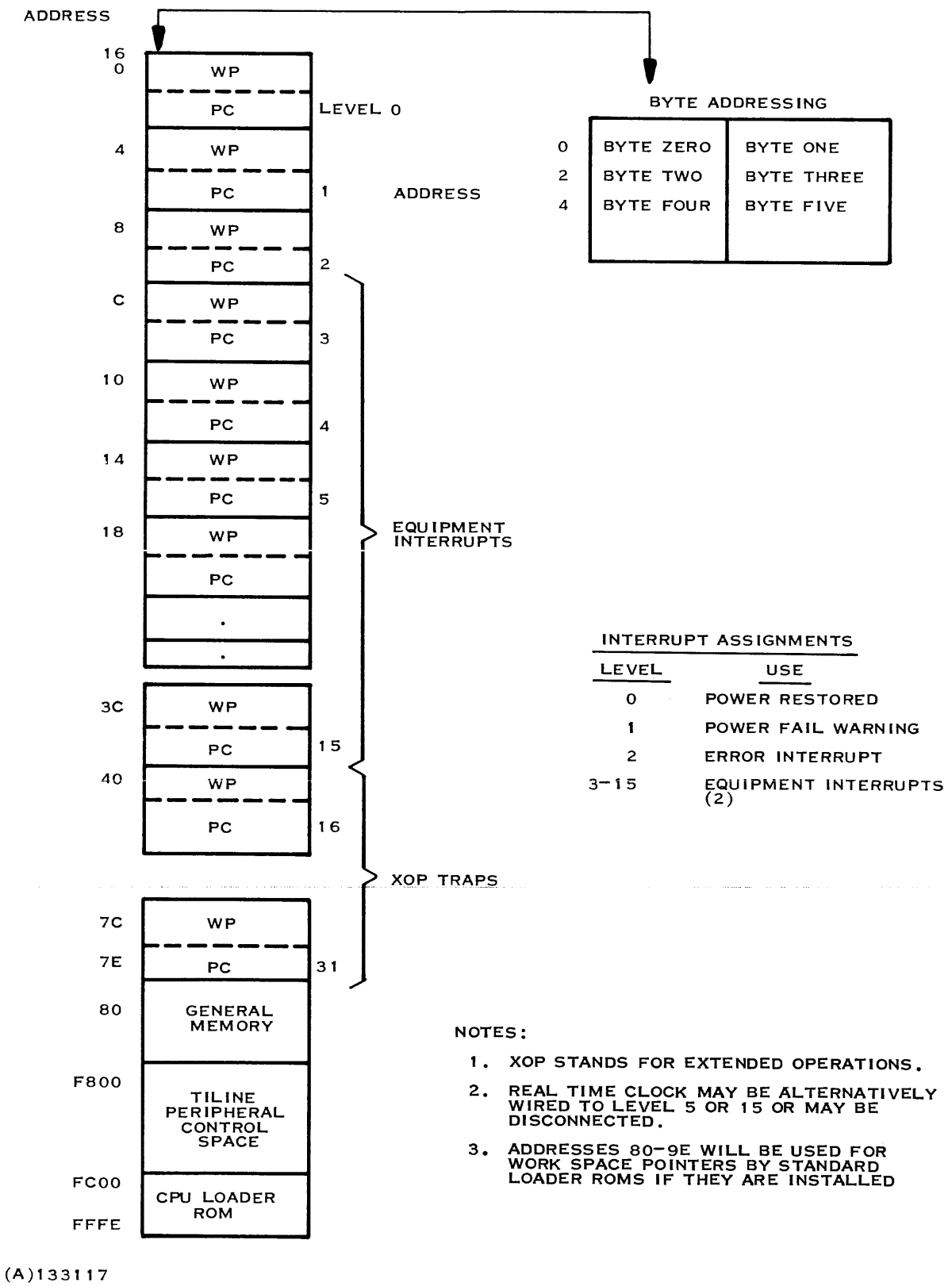


Figure 3-3. 990/10 Processor Memory Map

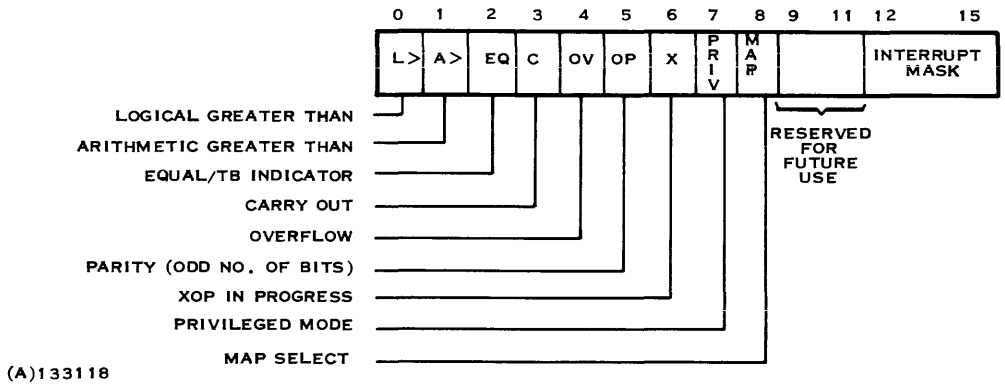


Figure 3-4. Status Register Bit Assignments

Table 3-2. Dedicated Workspace Registers

Register No.	Contents	Used During
0	Shift count (optional)	Shift instructions (SLA, SRA, SRC and SRL)
11	Return address	Branch and Link Instruction (BL)
	Effective address	Software implemented Extended Operation (XOP)
12	CRU base address	CRU instructions (SBO, SBZ, TB, LDCR and STCR)
13	Saved WP register	Context switching (BLWP, RTWP, software XOP, recognized interrupt, LOAD, and RESET)
14	Saved PC register	Context switching (BLWP, RTWP, software XOP, recognized interrupt, LOAD, and RESET)
15	Saved ST register	Context switching (BLWP, RTWP, software XOP, recognized interrupt, LOAD and RESET)

Interrupts. Sixteen priority-vectored interrupt levels are implemented in the 990/10 minicomputer. The interrupts generated by extended operation codes (XOPs) are not a part of the priority structure. When an interrupt is recognized by the hardware (interrupt pending at level not masked by status register mask), a BLWP instruction is forced using the words stored at the trap address for the recognized interrupt level for the workspace pointer and program counter. An RTWP instruction is used to exit from an interrupt subroutine and the prior operating environment is completely restored by the RTWP.

Each of the interrupts has a priority level assigned that ranges from level 0 through level 15. Level 0 has the highest priority and level 15 has the lowest priority. Each priority level has two consecutive memory words with absolute trap addresses reserved for it (see processor memory map, figure 3-3). The first location contains a new workspace pointer and the second location contains a new program counter. Interrupts are enabled at a given level and of higher priority as specified by the four-bit field in the interrupt mask of the status register. Level 0 is the only level that cannot be disabled.

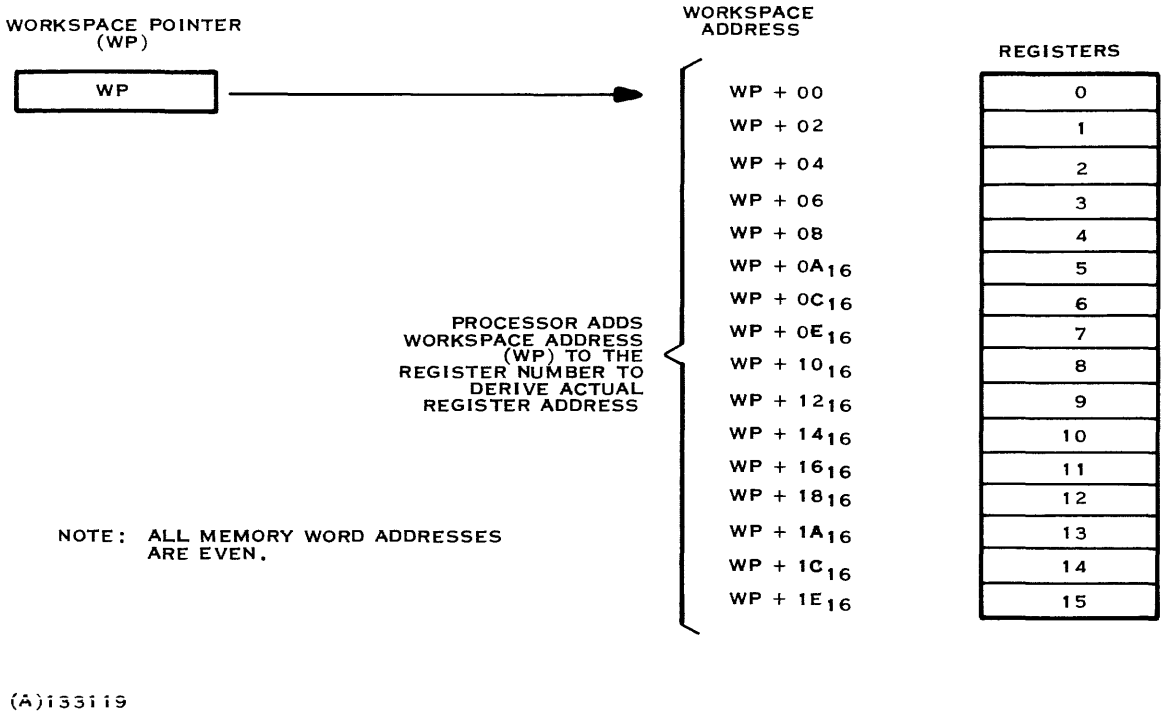


Figure 3-5. Workspace Pointer and Registers

The processor continuously compares the interrupt code (LEV0 through LEV3) with the interrupt mask contained in status register bits 12 through 15. When the level of the pending interrupt is less than or equal to the enabling mask level (higher or equal priority interrupt), the processor recognizes the interrupt and initiates a context switch following completion of the currently executing instruction. The processor fetches the new context WP and PC from the interrupt vector locations. Then, the previous context WP, PC, and ST are stored in workspace registers 13, 14, and 15 of the new workspace. The processor then forces the interrupt mask to a value that is one less than the level of the interrupt being serviced, except for the level 0 interrupt that loads 0 into the mask. This allows only interrupts of higher priority to interrupt a service routine. The processor also inhibits interrupts until the first instruction of the service routine has been executed so that program linkage is preserved should a higher priority interrupt occur. All interrupt requests remain active until recognized by the processor in the device-service routine. The individual service routines must reset the interrupt requests before the routine is complete. If a higher priority interrupt occurs, a second context switch is made to service the higher priority interrupt. When that routine is complete, a return instruction (RTWP) restores the first service routine parameters to the processor to complete processing of the lower priority interrupt. All interrupt subroutines should terminate with the return instruction to restore original program parameters.

The three highest priority level interrupts are reserved for internal interrupts. The highest of these, level 0, is the power restored interrupt. Any time ac power is restored to the CPU chassis, program execution will begin using the program counter and workspace pointer that were previously stored at the level 0 trap locations. The mask field of the status register is set to 0. This disables all interrupts except level 0. Level 0 interrupt cannot be disabled.

When the 990/10 power supply senses that a loss of ac power is imminent, an interrupt is generated and the processor has 7.0 milliseconds of program time before the system is reset for the power-loss state. This function is wired to the level 1 interrupt. The third internal interrupt is a merging of a number of error conditions. The error conditions are:

- Error (parity/error correcting) from TILINE memory (TLMER)
- Illegal operation (ILLOPSET)
- Privileged instruction fetch (PRIVOPSET) with privileged mode off (status register bit 7 = 1)
- TILINE timeout
- Memory mapping error (if memory mapping option implemented)

The error interrupt function is wired to the level 2 interrupt. Interrupt levels 3 through 15 are reserved for externally requested equipment interrupts. The reserved trap addresses for these levels are as shown in figure 3-3. The interrupt requests from the external devices (or from internal interrupt functions) may be wired to any of the thirteen interrupt request lines (INT3– through INT15–) on the edge connector of the system interface board (AU2). The lines form 13 separate wired-or interrupt buses. A 1-kilohm pull-up resistor is supplied on the board for each line and each interrupt request signal should be an active low signal driven by an open-collector TTL gate. The request signal should remain on the respective interrupt bus until it is reset by software communication. The request signal should be reset at some time before the interrupt service program executes RTWP or the processor will repeat the trap.

TILINE Peripheral Control Space (TPCS). The TILINE peripheral control space (TPCS) consists of those central processor addresses in the range $F800_{16}$ through $FBFE_{16}$ (see memory map, figure 3-3). The addresses ($F800_{16}$ through $FBFE_{16}$) are modified before presentation to the TILINE. Five address bits are appended to the left (most significant bit side) of each address in order to form a 20-bit TILINE word address. In other words, addresses 0000 to $F800_{16}$ are passed through to the TILINE so as to address the first 31K words of the 1024K words of TILINE address space. Addresses $F800_{16}$ through $FBFE_{16}$ are mapped to addresses $FFC00_{16}$ through $FFDFF_{16}$ of the 1024K-word address space. Memory commands associated with locations $FC00_{16}$ through $FFFE_{16}$ address the TTL PROM loader on the system interface board (AU2).

Input/Output. The 990/10 minicomputer uses a versatile direct command-driven I/O interface designated as the Communications Register Unit (CRU). The CRU provides up to 4096 directly addressable input bits and 4096 directly addressable output bits. Both input and output bits can be addressed individually or in fields of from 1 to 16 bits. The processor employs three dedicated I/O pins (CRUBITIN, CRUBITOUT, and STORECLK–) and 12 bits (CRUBIT4 through CRUBIT15) of the address bus at the interface to the CRU system. The processor instructions that drive the CRU interface can set, reset, or test any bit in the CRU array or move data between memory and CRU data fields.

Because of its extremely flexible data format, the CRU interface can be used effectively for a wide range of control and data transaction operations. These applications can be divided into two broad categories: those involving a single control bit transfer, and those requiring input or output of several data or status bits.

The processor performs three single-bit CRU functions: test bit (TB), set bit to one (SBO), and set bit to zero (SBZ). To identify the bit to be operated upon, the processor develops a CRU-bit address and places it on the address bus, CRUBIT4 through CRUBIT15.

For the two output operations (SBO and SBZ), the processor generates a STORECLK– pulse that indicates to the CRU device that the operation is one of output and places bit 7 of the instruction word on the CRUBITOUT line to accomplish the specified operation (bit 7 is a ONE for SBO and a ZERO for SBZ). The test bit instruction is an input operation that transfers the addressed CRU bit from the CRUBITIN input line to bit 2 (equal bit, see figure 3-4) of the status register.

The processor develops a CRU-bit address for the single-bit operations from the CRU base address contained in workspace register 12 (W12) and the signed displacement contained in bits 8 through 15 of the instruction. The displacement allows two's complement addressing from base minus 128 bits through base plus 127 bits. The base address from W12 (in bits 3-14) is added to the signed displacement specified in the instruction and the result is loaded onto the address bus. Figure 3-6 illustrates the development of a single-bit CRU address.

The processor performs two multiple-bit CRU operations: store communications register (STCR) and load communications register (LDCR). Both operations perform a data transfer from the CRU-to-memory or from memory-to-CRU as illustrated in figure 3-7. Although the figure shows a full 16-bit transfer operation, any number of bits from 1 to 16 may be involved. The LDCR instruction fetches a word from memory and right-shifts it to serially transfer it to CRU output bits. If the LDCR involves 8 or fewer bits, those bits come from the right-justified field within the addressed byte of the memory word. If the LDCR involves 9 or more bits, those bits come

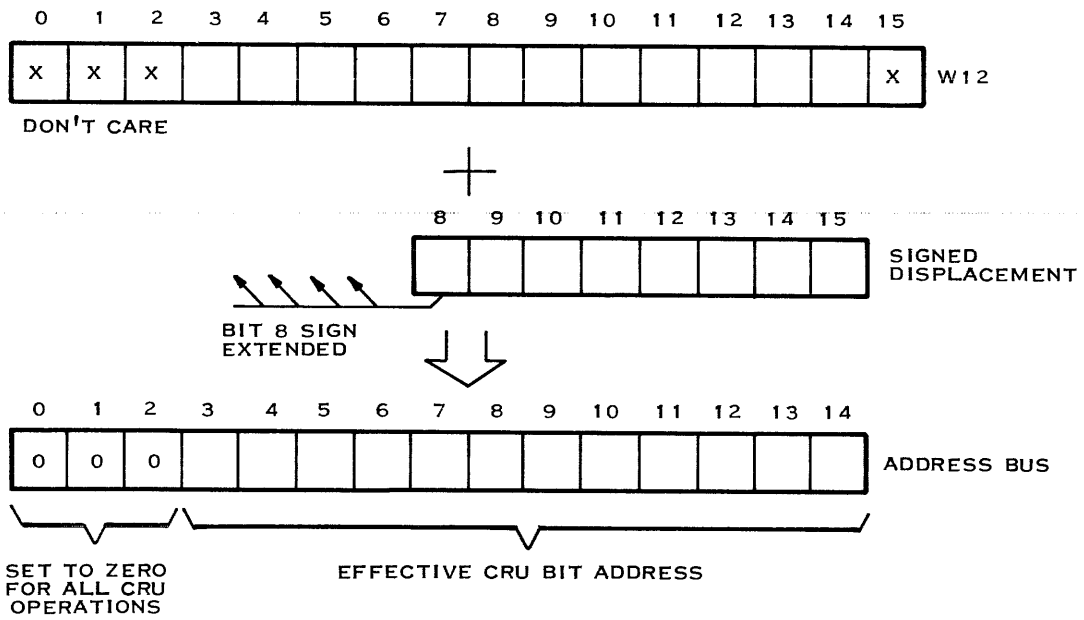


Figure 3-6. 990/10 Single-Bit CRU Address Development

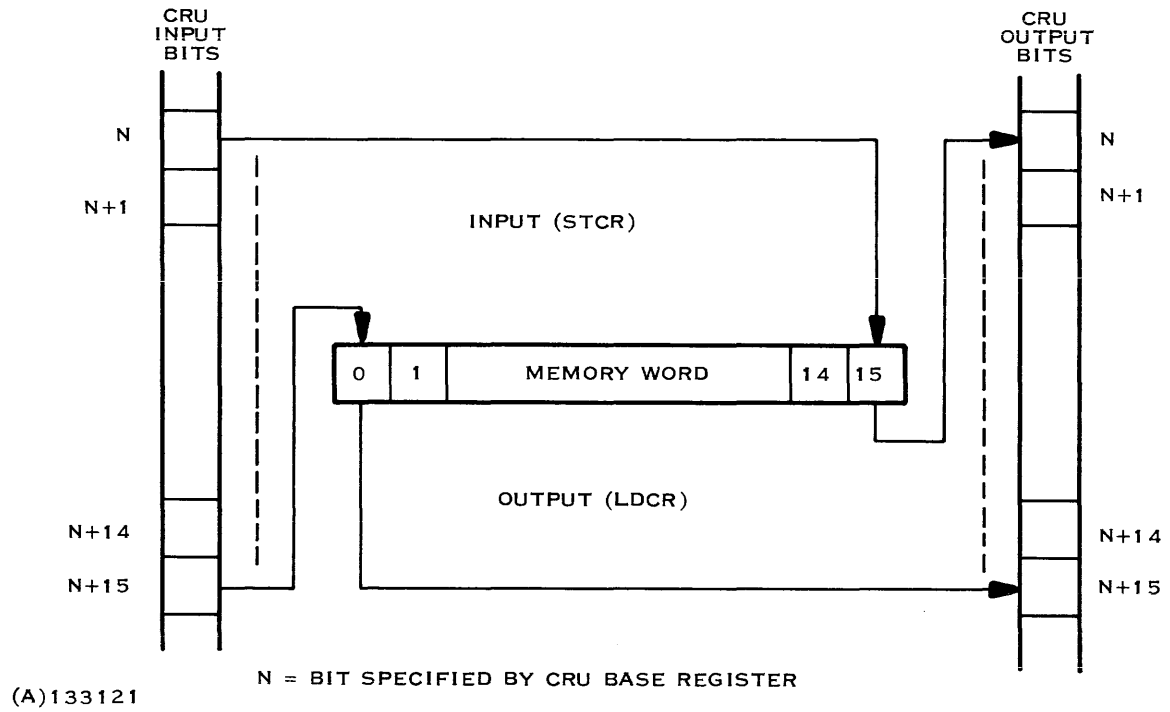


Figure 3-7. 990/10 LDCR/STCR Data Transfers

from the right-justified field within the whole memory word. As the bits are transferred to the CRU interface, the CRU address is incremented for each successive bit. This addressing mechanism results in an order reversal of the bit; that is, bit 15 of the memory word (or bit 7) becomes the lowest addressed bit in the CRU and bit 0 becomes the highest addressed bit in the CRU field.

An STCR instruction transfers data from the CRU to memory. If the operation involves a byte or less transfer, the transferred data will be stored right-justified in the memory byte with leading bits set to zero. If the operation involves 9 to 16 bits, the transferred data is stored right-justified in the memory word with leading bits set to zero. When the input from the CRU device is complete, the first bit from the CRU is in the least significant bit position in the memory word or byte.

Load Function. The RESTART– signal permits cold-start ROM loaders and front panel routines to be implemented for the processor. When active, RESTART– causes the processor to initiate a trap immediately following the instruction being executed. RESTART– is an unmaskable interrupt that traps to the TTL PROM loader location $FFFC_{16}$ to obtain the trap vector (WP and PC). The old PC, WP, and ST are loaded into the new workspace and the interrupt mask is set to zero. Then, program execution resumes using the new PC and WP. The RESTART– signal comes into the system interface board either from the backpanel or from the programmer panel connector. The load function can also be initiated by execution of an LREX instruction or through the programmer panel single-instruction (SIE) function.

Privileged Instructions. Certain machine instructions of the 990/10 are treated as privileged instructions and will execute only when the computer is in the privileged mode (bit 7 of the status register equals 0). The attempt to execute a privileged instruction when the computer is not in the privileged mode causes an error condition and a trap through interrupt level 2 (except for instruction RTWP). The privileged instructions are: LIMI, LMF, LDS, LDD, LREX, RSET, CKON, CKOF, IDLE, and RTWP. When any interrupt trap is taken, bit 7 of the status register is cleared to 0 to allow proper interrupt processing. The instruction RTWP executes normally except that during the workspace register 15 to status register transfer, bits 7, 8, and 12 through 15 are not loaded.

Additionally, the addressing of CRU output bits at address $\geq E00_{16}$ (CRU base address $1C00_{16}$) is privileged.

Illegal Operation Codes. When the processor acquires an instruction from memory that cannot be executed it generates a level 2 error interrupt. A detailed description of error interrupts and illegal operation codes is provided in paragraph 3.2.5.

Real Time Clock. A line frequency synchronized oscillator on the power supply is an input to the central processor. On every cycle of the oscillator, the real time clock interrupt function is generated. This function may be connected with jumper wires to interrupt level 5 or interrupt level 15 or may be disconnected. The CKON and CKOF instructions are used to enable and disable the real time clock interrupt function independent of the status register mask. This function is normally cleared in the "clock interrupt service routine" with CKOF, CKON instructions sequence.

XOP Hardware. As a performance enhancement, the 990/10 provides an interface to customer-supplied external hardware modules that execute customer defined instructions while the processor waits for the results. If the external modules are not attached, the processor traps to emulation subroutines instead. A detailed description of the XOP hardware interface logic as implemented on the 990/10 is provided in paragraph 3.2.6.

Programmer Panel Interface. The 990/10 provides an interface to a programmer panel. The programmer panel is a CRU device that is addressed at CRU base address $1FE0_{16}$. A detailed description of the programmer panel interface is provided in paragraph 3.2.7 and a description of the programmer panel is contained in paragraph 3.6. Tables 3-28 and 3-29 provide the CRU bit assignments for base address $1FE0_{16}$. The following programmer panel functions are implemented directly by the 990/10.

- Power LED – Power reset is inverted and supplied to the programmer panel connector through a 180-ohm resistor.

- Fault LED – An SBO instruction to CRU bit 11 causes the FAULT light on both the programmer panel and the system interface board (AU2) to light. The fault indicator flip-flop is buffered to drive both lamps. An I/O reset or an SBZ instruction turns off the fault lamps. A power reset turns the lamps on. The FAULT signal is supplied to the programmer panel through a 180-ohm resistor.

- Run LED – An SBO or SBZ instruction to CRU bit 10 causes the RUN indicator on the programmer panel to illuminate. A power reset also illuminates the RUN indicator. The RUN function is automatically cleared by a RESTART– signal or by setting the single-instruction execute function (programmer panel CRU output bit 14). The RUN signal is supplied to the programmer panel through a 180-ohm resistor.

- Memory error interrupt clear – An SBO or SBZ instruction to CRU bit 12 clears a memory error interrupt.

- Single Instruction Execute (SIE) – An SBO or SBZ instruction to CRU bit 14 causes the load function to be executed after two additional instructions.

- Idle LED – The IDLE– signal from the processor is buffered and provided to the programmer panel connector through a 390-ohm resistor as the IDLELED– signal.

3.2.1.2 **Processor Board to System Interface Board Signals.** The interface between the processor board (AU1) and the system interface board (AU2) consists of the following functions:

- Mapping option (on AU2B board only)

- XOP (hardware)

- Data and Address Busses

- CRU interface

- Interrupts

- Clock/clear

The interface is made between the two boards with two short ribbon cables connected to connectors P5 and P6 near the top edge of each board. Pin assignments are the same for both boards. Pin assignments and interface signal functions are as described in table 3-3. The input/output (I/O) column of the table is in reference to the AU1 circuit board.

3.2.2 **TILINE.** The 990/10 computer uses a high-speed, bidirectional 16-bit data bus called the TILINE that with associated control lines serves to transfer data between all high-speed system elements. These elements include the central processor, the memory, and other rapid data transfer devices such as disc files and magnetic tape transports. The TILINE also serves as a computer-to-computer link and is the backbone of multiprocessor systems.

The TILINE operates asynchronously and the speed of data transfers over the TILINE is governed by distance between and the speed of the devices connected to the TILINE. Consequently, system performance can be tailored to the application by suitable choice of devices and can be upgraded easily as needed.

The devices connected to the TILINE compete for access to the bus through a positional priority system. High-speed peripherals are usually assigned highest priority and the central processor is assigned the lowest priority. In operation, an efficient cycle-stealing action occurs. The overhead time required for switching from central processor access to another device is overlapped with the data transfer. This permits a very high rate of device switching without sacrificing overall data bandwidth.

Table 3-3. Processor/System Interface Board Interface Pin Assignments and Functions

Signature	Pin	I/O*	Description
MA0(MSB)	P5-38	OUT	MA0 through MA14 comprise the address bus.
MA1	P5-36	OUT	
MA2	P5-30	OUT	
MA3	P5-41	OUT	
MA4	P5-43	OUT	
MA5	P5-45	OUT	
MA6	P5-47	OUT	
MA7	P5-50	OUT	
MA8	P5-48	OUT	
MA9	P5-49	OUT	
MA10	P5-39	OUT	
MA11	P5-40	OUT	
MA12	P5-42	OUT	
MA13	P5-44	OUT	
MA14(LSB)	P5-46	OUT	
DI0(MSB)	P5-35	IN	DI0 through DI15 comprise the memory read data bus.
DI1	P5-25	IN	
DI2	P5-15	IN	
DI3	P5-13	IN	
DI4	P5-31	IN	
DI5	P5-29	IN	
DI6	P5-19	IN	
DI7	P5-7	IN	
DI8	P5-37	IN	
DI9	P5-23	IN	
DI10	P5-17	IN	
DI11	P5-11	IN	
DI12	P5-33	IN	
DI13	P5-27	IN	
DI14	P5-21	IN	
DI15(LSB)	P5-9	IN	
DO0(MSB)	P5-5	OUT	DO0 through DO15 comprise the memory write data bus.
DO1	P5-3	OUT	
DO2	P5-32	OUT	
DO3	P5-4	OUT	
DO4	P5-12	OUT	
DO5	P5-10	OUT	
DO6	P5-8	OUT	
DO7	P5-6	OUT	
DO8	P5-20	OUT	
DO9	P5-18	OUT	
DO10	P5-16	OUT	
DO11	P5-14	OUT	
DO12	P5-28	OUT	
DO13	P5-26	OUT	
DO14	P5-24	OUT	
DO15(LSB)	P5-22	OUT	

*Input/output is in reference to the processor board.

Table 3-3. Processor/System Interface Board Interface Pin Assignments and Functions (Continued)

Signature	Pin	I/O*	Description
CYREQ	P6-19	OUT	When active (high) indicates that the present clock period is for a memory cycle.
STORE	P5-34	OUT	When high indicates that the memory cycle request is for a write cycle.
HOLD–	P6-27	OUT	A TILINE control signal that suspends control contention during the processing of an ABS instruction so that the effective address can be read, tested, and changed before another master device can have access to memory. This is to assure the validity of global software interlocks in multiprocessor systems.
INTPRES	P6-10	IN	Interrupt present. When active (high) indicates that an interrupt is requested. If INTPRES is active, the processor loads the data on the interrupt-code input lines LEV0 through LEV3 into an interrupt-code storage register. The code is compared to the interrupt bits of the status register. If equal or higher priority than the enabled interrupt level (interrupt code equal to or less than status register bits 12 through 15) the processor interrupt sequence is initiated. If the comparison fails, the processor ignores the request. INTPRES remains active and the processor will continue to sample LEV0 through LEV3 until the program enables a priority low enough to accept the requested interrupt.
LEV0(MSB) LEV1 LEV2 LEV3(LSB)	P6-26 P6-24 P6-22 P6-20	IN IN IN IN	Interrupt codes. LEV0 is the MSB of the interrupt code that is sampled when INTPRES is active. When LEV0 through LEV3 are LLLH, the highest priority interrupt is being requested and when HHHH, the lowest priority interrupt is being requested.
STORECLK	P6-9	OUT	CRU clock enable. When active (high) and ANDed with system clock, develops signal that indicates to addressed CRU device that data on CRUBITOUT should be sampled.
CRUBITINA	P6-15	IN	CRU data in. When the processor executes an STCR or TB instruction, it samples CRUBITINA for the level of the CRU input bit specified by the address bus (MA3 through MA14).
CRUOUT	P6-28	OUT	CRU data out. Serial data appears on the CRUOUT line when an LDCR, SBZ, or SBO instruction is executed. The data on CRUOUT is sampled by external I/O interface logic at the CRU interface on the positive-going edge of STORECLK–.
INTCRU–	P6-33	IN	When low indicates to processor that CRU address is in the main chassis and that CRU input data can be processed at the 4-MHz rate.
ST8A–	P6-29	OUT	When ST8A– is high (status register bit 8 is low) indicates that MAP0 is to be used during a nonlong distance memory reference.
IRLD	P6-21	OUT	Indicates that the current memory request is an instruction fetch. Signal is used to develop the XOP hardware interface signal XOPIAQCK–.
XOPTHERE	P6-31	IN	Input signal to processor to indicate that a hardware module is available to perform the indicated XOP function.

*Input/output is in reference to the processor board.

Table 3-3. Processor/System Interface Board Interface Pin Assignments and Functions (Continued)

Signature	Pin	I/O*	Description
XOPDONE	P6-30	IN	Input signal to processor developed by either a XOPABORT– or a XOPCOM– signal from an XOP hardware module to indicate that an operation was aborted before completion or was successfully completed.
XOPABORT	P6-32	IN	Input signal to processor developed by XOPABORT– signal from an XOP hardware module to signify that the module has terminated an operation before completion.
ENXOPSTB–	P6-13	OUT	Output signal from the processor that develops the XOPSTB– signal to the XOP hardware module to indicate that the effective address has been calculated and is available on the address bus.
ENXOP–	P6-14	OUT	Signal from the processor that develops the ENXOPQ– signal to the hardware module to permit the module to start processing.
CKA–	P5-2	IN	Clock signal generated on AU2 (the system interface board) used to drive AU1 (processor board).
RESET–	P6-18	OUT	Signal generated during the execution of the RSET instruction.
PRIVOPSET–	P6-4	OUT	Signal generated by processor to indicate a privileged instruction fetch attempt when not in privileged mode (status register bit 7 = 1).
ILLOPSET–	P6-6	OUT	Signal generated by processor to indicate that an illegal operation code has been decoded.
PINT–	P6-23	OUT	A low active signal from the processor to indicate to an XOP hardware module the presence of an interrupt.
IR10A	P6-16	OUT	Instruction register bit 10 – high for a CKON instruction to enable the real time clock; set low for a CKOF instruction to disable the real time clock.
ST7	P6-25	OUT	Status register bit 7. Privileged instructions will execute only when register bit 7 is set to 0.
IDLE–	P6-8	OUT	A signal from the processor to the system interface board indicating processor idle mode.
120HZMSK	P6-11	OUT	A signal from the processor that masks the real time clock so that once an interrupt has been generated, a CKOF, CKON instruction sequence is required to generate a second interrupt.
LOAD–	P6-34	IN	A low active signal to the processor indicating that a restart trap has been requested.
LDMAP–	P6-7	OUT	A low active signal from the processor indicating that map-load data is present on internal data lines (applicable to 990/10 with map option).
LDMAPID–	P6-5	OUT	A signal from the processor indicating whether map 0 or map 1 is designated for loading (applicable to 990/10 with map option).
MAP2–	P6-12	OUT	A signal from the processor that indicates when active (low) that ST8A– should be overridden and map 2 be used instead of map 0 or map 1 (applicable to 990/10 with map option).

*Input/output is in reference to the processor board.

Table 3-3. Processor/System Interface Board Interface Pin Assignments and Functions (Continued)

Signature	Pin	I/O*	Description
EOI–	P6-3	OUT	A signal from the processor indicating the last state of an instruction.
HALT–	P6-17	IN	A breakpoint input signal to the processor.

*Input/output is in reference to the processor board.

3.2.2.1 **TILINE Applications.** The TILINE is fully implemented on high capability Model 990 Computers, including the 990/10 minicomputer, where it is utilized as the sole path of data communication between all high-speed system elements. The central processor, the main memory, and all high-speed peripheral devices such as disc files and magnetic tape transports are directly connected to the TILINE. Slower peripheral devices, such as EIA-compatible devices, are connected to the 990/10 minicomputer through the communications register unit (CRU). The interface to the minicomputer system of either a CRU or TILINE device is effected by installing either device into a slot of the chassis backpanel since the CRU and TILINE share the same backpanel but use different pin positions.

3.2.2.2 **MASTER-SLAVE Concept.** There are two classes of devices that connect to the TILINE: TILINE MASTER devices that control data transfers, and TILINE SLAVE devices that generate or accept data in response to some MASTER device. Data transfers in either direction always occur between one MASTER and one SLAVE. The central processor is an example of a MASTER device and a memory module is an example of a SLAVE device. All SLAVE devices recognize a specific address and are activated only when addressed. For example, a memory module is activated when some MASTER device performs a read operation from an address within the bounds of its address. The configuration of the system must be such that only one SLAVE device recognizes any particular address. For memory modules, pencil switches on the modules are set to provide the desired starting address and size of the module.

Peripheral controllers are both MASTER and SLAVE devices. Special registers addressed as specific memory addresses near the high end of memory constitute the SLAVE part of the peripheral controller. The registers are loaded by the central processor with memory-to-memory move instructions. The registers specify the parameters of a peripheral data transfer. In the case of a disc, they specify disc address, the number of sectors of data to be transferred, the memory address to which the data is to be transferred and whether the data is to be read or written. One register in each peripheral controller is a status register for that controller. The bits in the register indicate information such as "operation complete", "read error", "rewind complete", and "illegal command". Other bits in the peripheral controller status register are set by the central processor to command the peripheral to start, stop, clear its interrupt, or reset. All of these registers are addressed by the central processor as consecutive words of memory at some specific address. Pencil switches are used to set the address of the registers for each peripheral controller. When a peripheral controller is started by the central processor, it transfers data between memory and the peripheral device by cycle-stealing with the central processor and any other MASTER devices that may be active. When a peripheral controller needs to transfer a word of data over the TILINE, the MASTER device part of the peripheral controller must gain access to the TILINE and then may address a SLAVE (such as a memory module) and read from or write to it.

3.2.2.3 **TILINE Interface Signals.** There are 48 TILINE interfaces signals that perform the addressing, data transfer, and control functions of the TILINE. Figure 3-8 illustrates and table 3-4 defines the TILINE interface signals and gives their assigned connector pin numbers at the chassis packpanel. The signals are functionally grouped and described in the three subparagraphs that follow.

Data Transfer Operations. There are 40 TILINE interface signals that are used exclusively for data transfer operations on the TILINE. As shown in figure 3-8, 36 of these signals consist of the 20 address bits and 16 data bits with the remaining 4 signals used primarily for control of the actual data transfer operation. These 4 signals are: TLGO–, TLREAD, TLTM–, and TLMER–. All signals are transmitted and received between a TILINE MASTER device and a TILINE SLAVE device during a transfer of data. A description of both a read and write data transfer are described herein.

Timing for the TILINE MASTER to SLAVE write cycle is as shown in figure 3-9 and is referenced in the following discussion. When a TILINE MASTER device has access to the TILINE it may accomplish a memory (SLAVE) write cycle as follows. The MASTER asserts TILINE GO (TLGO–) and at the same time asserts the write command TILINE READ (TLREAD) by setting both signals low. The MASTER at this time also generates valid write data on the data bus (TLDAT–) and a valid 20-bit address (TLADR–) on the address lines. All SLAVE devices on the TILINE receive the TILINE GO transmitted by the MASTER. The SLAVE devices must decode the address to determine which SLAVE is being addressed. The SLAVE generates a delayed GO signal (using a timer circuit) and uses that signal to strobe for a valid address decode. In the case of a memory module, a delayed GO and a valid address decode generate a memory start signal. It is the responsibility of the SLAVE device to delay GO for a time sufficient to accommodate the worst case address decode time and the worst case TILINE skew, with TILINE skew defined as 20 nanoseconds maximum. When the SLAVE device has delayed GO and decoded the address as valid it performs the write cycle and then asserts the TILINE TERMINATE (TLTM–). At the time the SLAVE device asserts TLTM– it must be finished with the TLDAT–, TLADR–, and TLREAD signals from the TILINE. The action just described occurs during "time 1" as shown in figure 3-9. This time is defined as the SLAVE access time and must be less than 1.5 microseconds for all TILINE SLAVES except the TILINE coupler. When the TILINE MASTER receives the asserted TLTM–, it must release TLGO–, TLREAD, TLADR–, and TLDAT– within 120 nanoseconds. This occurs during "time 2" shown in figure 3-9. At this time the MASTER device may relinquish the TILINE to another MASTER device. When the SLAVE receives the release of TLGO–, it must release TLTM– within 120 nanoseconds as shown in "time 3" of figure 3-9. When the MASTER device receives the release of TLTM–, it may begin a new cycle if it has not relinquished the TILINE to another MASTER device. This is shown as "time 4" in figure 3-9.

Timing for the TILINE MASTER to SLAVE read cycle is as shown in figure 3-10 and is referenced in the following discussion. When a TILINE MASTER device has access to the TILINE it may accomplish a memory (SLAVE) read cycle as follows. The MASTER asserts TLGO– and at the same time generates a valid address signal (TLADR–) and TLREAD signal. All SLAVE devices on the TILINE receive the TILINE GO transmitted by the MASTER. The SLAVE devices delay the GO signal and decode the address as is done for a write cycle. As in the write cycle, it is the responsiblity of the SLAVE device to delay GO for a time sufficient to accommodate the worst case TILINE skew (defined as 20 nanoseconds maximum) and worst case address decode time. When this has been done and the address is decoded as valid, the SLAVE device begins to generate read data. In the case of a memory module this means starting a read cycle. When read data is valid, the SLAVE device asserts TLTM– and at this time must have finished using TILINE signals TLADR– and TLREAD. If a read error is detected during a read cycle, the READ ERROR (TLMER–) signal is asserted by the SLAVE. This signal must

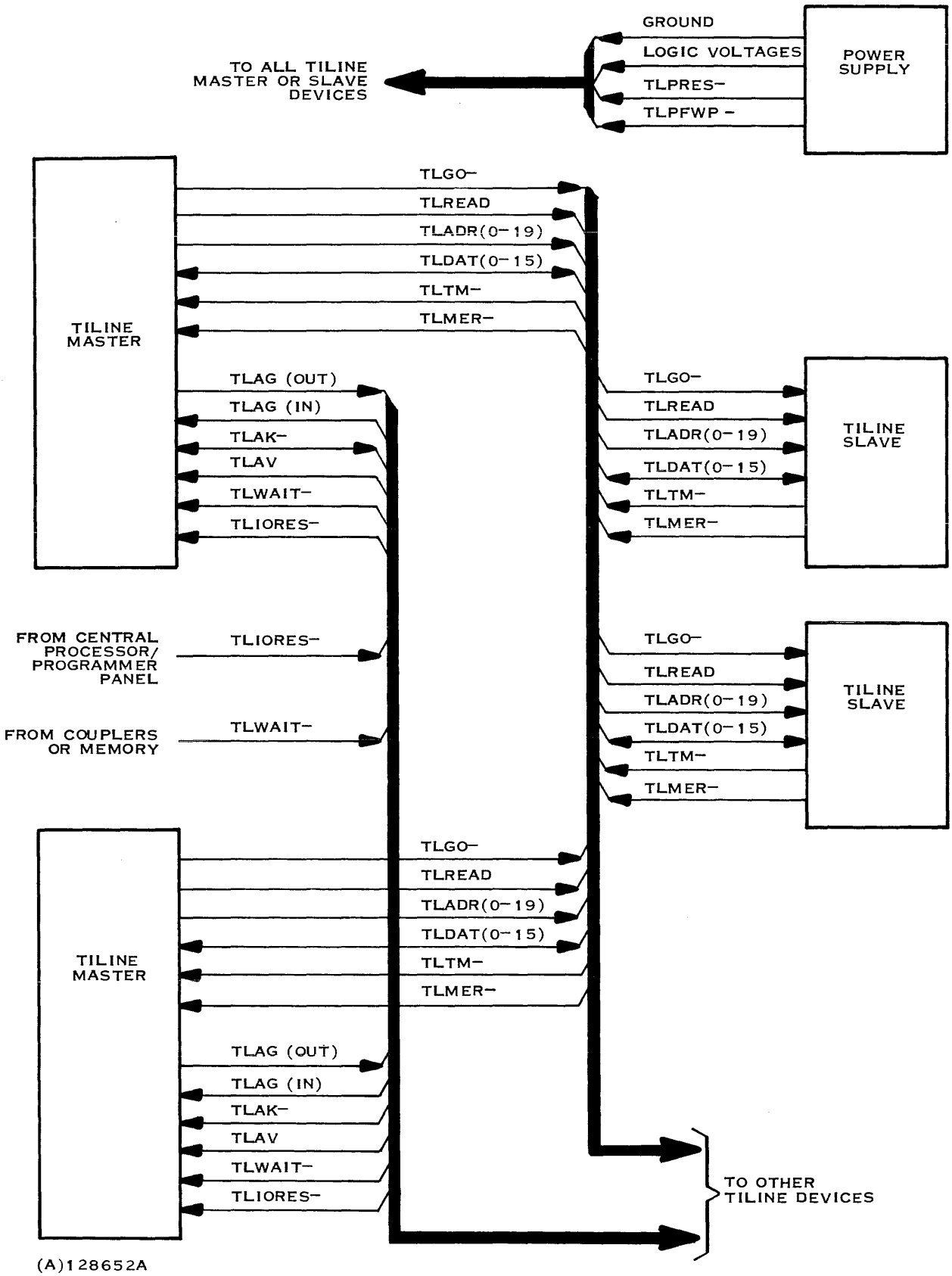


Figure 3-8. TILINE Interface Signals

Table 3-4. TILINE Signal Definitions

Signature	Pin No.	Definition
TLGO–	P1-25	TILINE Go: Initiates all data transfers when transition from high (3.0V) to low (1.0V) occurs. See note 1.
TLREAD	P1-11	TILINE Read: When high (3.0V) designates a read from SLAVE operation; when low (1.0V) designates a write to SLAVE operation. See note 1.
TLADR00–	P2-55	TILINE Address to define the location of data during a fetch or store operation. When high (≥2.0V) the corresponding address bit is a zero; when low (≤0.8V) the corresponding address bit is a one. See note 2.
01–	P2-44	
02–	P2-51	
03–	P2-53	
04–	P2-57	
05–	P2-59	
06–	P2-47	
07–	P2-49	
08–	P2-17	
09–	P2-19	
10–	P2-10	
11–	P2-12	
12–	P2-11	
13–	P2-15	
14–	P2-8	
15–	P2-9	
16–	P2-29	
17–	P2-27	
18–	P2-25	
TLADR19–	P2-31	
TLDAT00–	P2-67	TILINE Data: Bidirectional data lines that when high (≥2.0V) represent zero data bits, and when low (≤0.8V) represent one data bit. See note 2.
01–	P2-69	
02–	P2-35	
03–	P2-37	
04–	P2-61	
05–	P2-63	
06–	P2-43	
07–	P2-45	
08–	P2-21	
09–	P2-33	
10–	P2-23	
11–	P2-20	
12–	P1-27	
13–	P1-28	
14–	P1-30	
TLDAT15–	P1-31	
TLTM–	P1-20	TILINE Terminate: When low (1.0V) indicates that the SLAVE device has completed the requested operation. See note 1.

Note 1: Received by SN75138; driven by 36 milliampere, minimum, open-collector driver.
Note 2: Received by one, maximum, standard SN74- load per card slot; driven by SN74LS367/8.

Table 3-4. TILINE Signal Definitions (Continued)

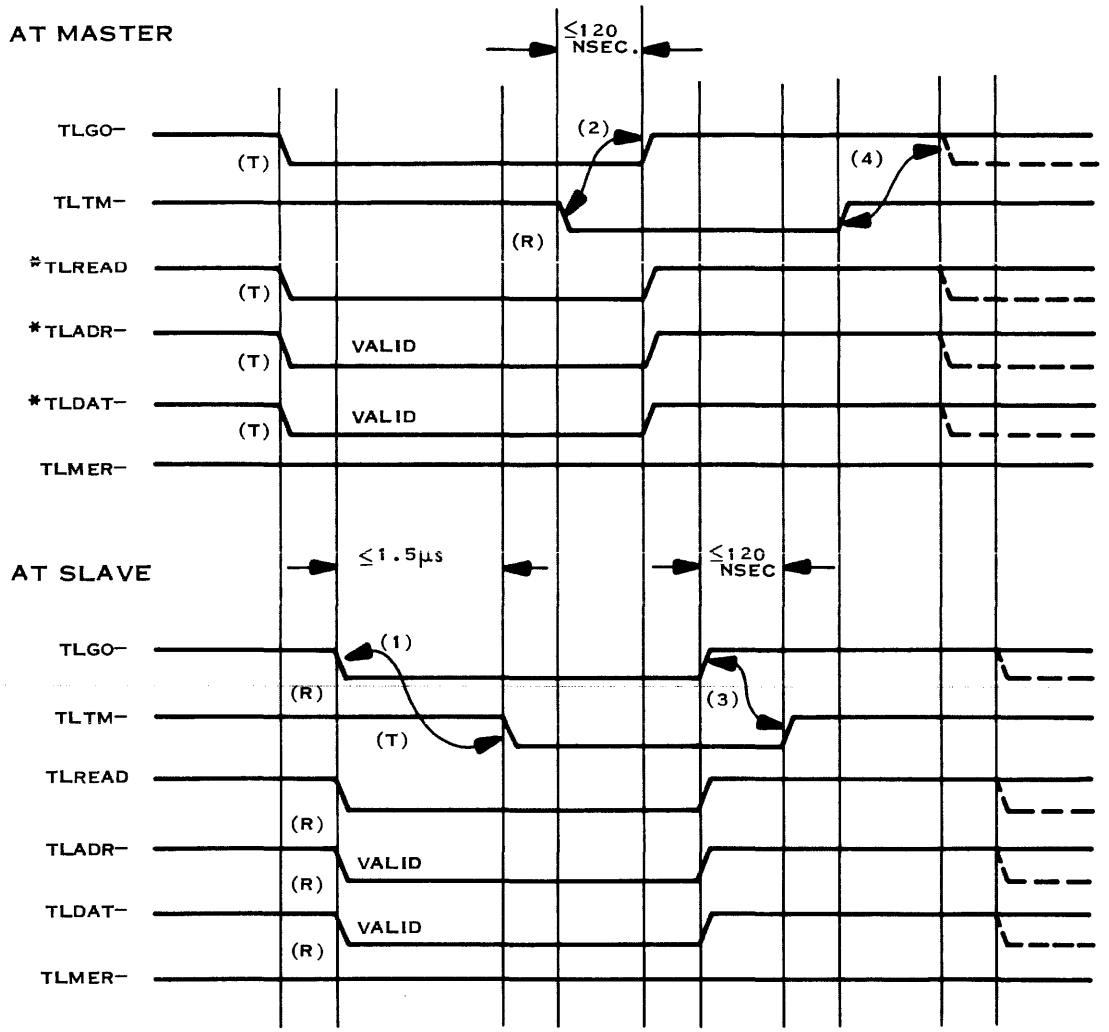
Signature	Pin No.	Definition
TLMER–	P1-55	TILINE Memory Error: When low (≤0.8V) indicates that a nonrecoverable error has occurred during a memory read operation. See note 2.
TLAG (in)	P2-6	TILINE Access Granted: When high (≥2.0V), this signal indicates that no higher priority device has requested use of the TILINE. When low (≤0.8V), this signal prevents the receiving device from gaining access to the TILINE bus.
TLAG (out)	P2-5	TILINE Access Granted: When high (≥2.0V), this signal indicates that neither the sending device nor any higher priority device is requesting use of the TILINE. When low (≤0.8V), this signal indicates that either the sending device or some higher priority device is requesting use of the TILINE bus and prevents all lower priority devices from gaining access to the bus.
TLAK–	P1-71	TILINE Acknowledge: When high (3.0V), this signal indicates that no TILINE device has been recognized as the next device to use the TILINE. When low (1.0V), this signal indicates that some TILINE device has requested access, has been recognized, and is waiting for the bus to become available. See note 1.
TLAV	P1-58	TILINE Available: When high (3.0V), this signal indicates that no TILINE device is using the bus. When low (1.0V), this signal indicates that the TILINE bus is busy. See note 1.
TLWAIT–	P1-63	TILINE Wait: A normally high (3.0V) signal that when low (1.0V), temporarily suspends all TILINE MASTER devices from using the TILINE bus. This signal is generated by bus couplers to allow them to use the bus as the highest priority user. See note 1.
TLIORES–	P1-14 P2-14	TILINE I/O Reset. A normally high (≥2.0V) signal that when low (≤0.8V), halts and resets all TILINE I/O devices. This signal is a 100 to 500 nanosecond pulse generated by the RESET switch on the control console or by the execution of a Reset (RSET) instruction by a CPU. Driven by SN7437; received by 2, maximum, standard SN74- loads per slot.
TLPRES–	P1-13 P2-13	TILINE Power Reset: A normally high (≥2.0V) signal that goes low (≤0.8V) to reset all TILINE devices and inhibit critical lines to external equipment. The signal is generated by the power supply at least 10 microseconds before dc voltages begin to fail during power-down, and until dc voltages are stable during power-up. Driven by 80-milliampere open-collector driver (160 milliamperes with 40-ampere power supply).
TLPFWP–	P1-16 P2-16	TILINE Power Failure Warning Pulse: A 7.0 millisecond pulse preceding TLPRES–. When low (≤0.8V), this signal indicates that a power-down sequence is in progress, allowing the CPU to perform its power failure interrupt subroutine. Driven by SN7437; received by two, maximum, standard SN74- loads per card slot.

Note 1: Received by SN75138; driven by 36 milliampere, minimum, open-collector driver.
Note 2: Received by one, maximum, standard SN74- load per card slot; driven by SN74LS367/8.

Table 3-4. TILINE Signal Definitions (Continued)

Signature	Pin No.	Definition
TLHOLD–	P2-26	TILINE Hold Signal: A normally high (3.0V) signal that goes low (1.0V) to assert that a central processor is executing an ABS instruction. TILINE Hold prevents interference from another processor on the TILINE while the first processor is performing the ABS instruction. This signal is used and propagated by TILINE COUPLERS in multi-processor systems. See note 1.

Note 1: Received by SN75138; driven by 36 milliampere, minimum, open-collector driver.
Note 2: Received by one, maximum, standard SN74- load per card slot; driven by SN74LS367/8.



NOTES: NUMBERS IN PARENTHESES DENOTE TIME PERIODS REFERENCED IN TEXT.
(TILINE DELAY IS EXAGGERATED FOR CLARITY)
(T) = TRANSMITTED
(R) = RECEIVED
*TLREAD, TLADR–, AND TLDAT– MUST BE STABLE AT THE TIME (OR BEFORE) TLGO– IS ASSERTED.

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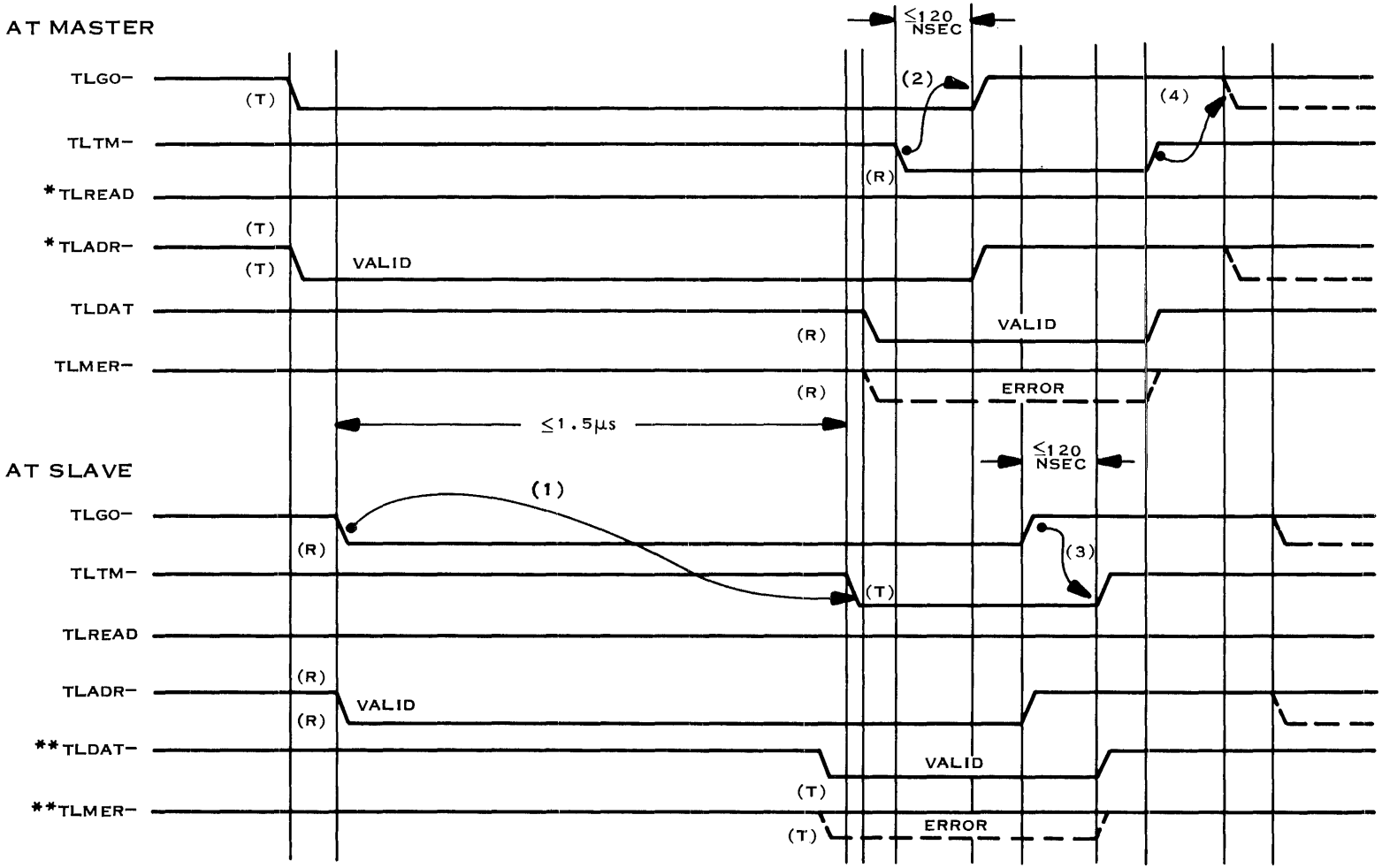
Figure 3-9. TILINE MASTER to SLAVE Write Cycle Timing Diagram



NOTES: NUMBERS IN PARENTHESES DENOTE TIME PERIODS REFERENCED IN TEXT. (TILINE DELAY IS EXAGGERATED FOR CLARITY)
(T) = TRANSMITTED (R) = RECEIVED
*TLREAD AND TLADR– MUST BE STABLE AT THE TIME (OR BEFORE) TLGO– IS ASSERTED
**TLDAT– AND TLMER– MUST BE STABLE AT THE TIME (OR BEFORE) TLTM– IS ASSERTED

(A)133123

Figure 3-10. TILINE MASTER to SLAVE Read Cycle Timing Diagram

have the same timing that the read data would have had and this action occurs during "time 1" as shown in figure 3-10. "Time 1" is defined as the SLAVE access time and must be less than 1.5 microseconds for all TILINE SLAVES except the TILINE coupler. When the MASTER devices receive the asserted TLTM–, it must delay at least for worst case TILINE skew (20 nanoseconds, maximum) and then release TLGO– and TLADR– signal lines. At the time the MASTER device releases TLGO– it must have finished using the TLDAT– and the TLMER– signals. This action occurs during "time 2" of figure 3-10 and must not require more than 120 nanoseconds. At this time the TILINE MASTER device may relinquish the TILINE to another MASTER device. When the SLAVE device receives the release TLGO–, it must release TLTM– and TLDAT– signals. This action occurs during "time 3" as shown in figure 3-10 and must not be a greater time period than 120 nanoseconds. When the MASTER device receives the released TLTM– it may begin a new cycle if it has not relinquished the TILINE to another MASTER device. This is shown as "time 4" of figure 3-10.

MASTER Device TILINE Acquisition. The three TILINE signals; TILINE Access Granted (TLAG), TILINE Acknowledge (TLAK–), and TILINE Available (TLAV) are used by MASTER devices to schedule the next TILINE MASTER during the last data transfer operation of the present TILINE MASTER. All TILINE MASTER devices are connected to the TILINE in a positional priority system with that TILINE device installed into the highest numbered chassis slot receiving the highest priority. Priority ranking decreases with each chassis slot location toward that chassis slot occupied by the central processor, which has the lowest priority. Figure 3-11 illustrates the connections between TILINE MASTER devices that establish the priority system. In the 990/10 chassis family backplane, TLAGIN is jumpered to TLAGOUT for all TILINE card slots except slot 7 which is, by convention, the slot used for the first TILINE MASTER device controller. Additional TILINE MASTER device controllers may be inserted in other TILINE card slots at higher or lower priority if the jumper plug between pins P2-5 and P2-6 is removed in the slot where the controller is installed.

The access controllers for each of the TILINE MASTER devices are identical. A flowchart of the operation of the access controllers is provided in figure 3-12 and is referenced in the following discussion.

When a TILINE MASTER device is inactive or reset, its access controller is in the IDLE state. In this state, TILINE Access Granted (TLAG) is passed on to lower priority MASTER devices and the access controller monitors for a Set Device Access Request signal from the device.

As soon as the device generates a Set Device Access Request signal indicating that it wants to obtain TILINE access, the access controller changes from the IDLE state to the DEVICE ACCESS REQUEST (DAR) state.

In the DAR state the access controller monitors TILINE Access Granted (TLAGIN) and TILINE Acknowledge (TLAK–). The access controller also disables TLAGOUT to the lower priority devices. After TLAGIN has been high for at least 100 nanoseconds and after the access controller has been in the DAR state for at least 100 nanoseconds, a high TLAK– causes the access controller to change to the DEVICE ACKNOWLEDGE (DAK) state.

In the DAK state the access controller continues to disable TLAG to lower priority MASTER devices and pulls TILINE Acknowledge (TLAK–) low. In this state the access controller monitors TILINE Available (TLAV) and when TLAV is high the access controller changes to the DEVICE ACCESS (DACC) state.

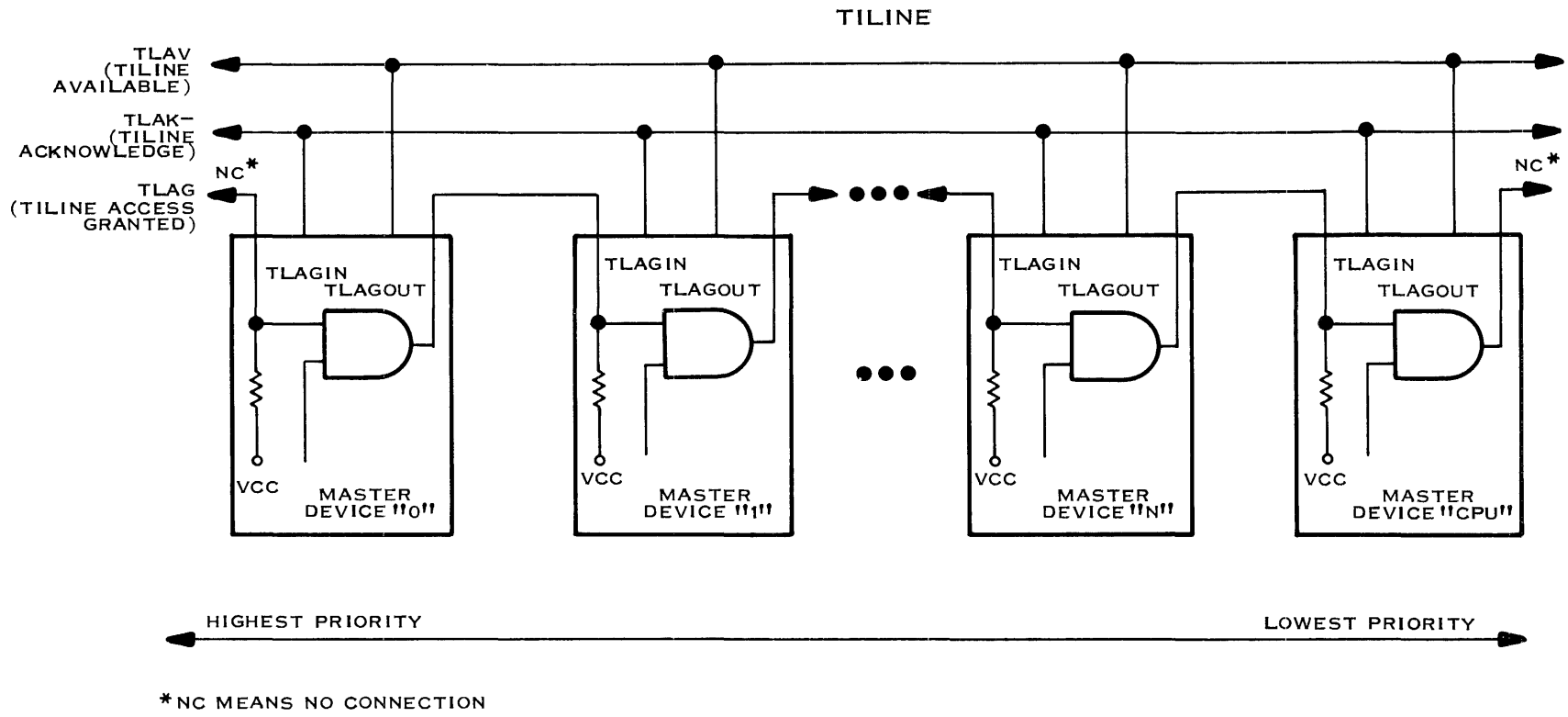


Figure 3-11. TILINE MASTER Devices Priority Interconnections

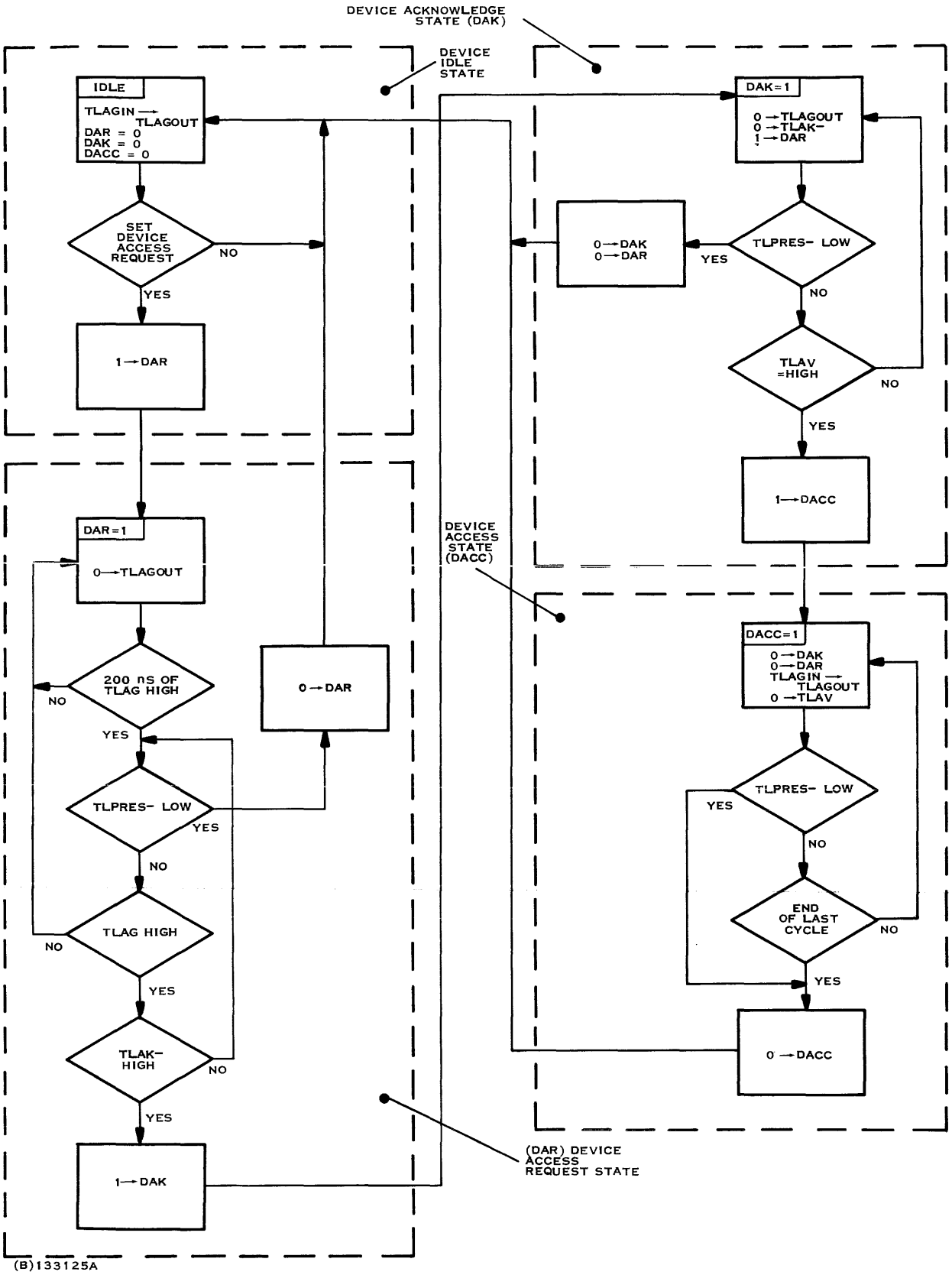


Figure 3-12. TILINE Master Device

In the DACC state the TLAG signal is passed on to lower priority MASTER devices and the access controller pulls TLAV low. While in the DACC state the MASTER device has access to the TILINE and may perform data transfers as described previously under data transfers. During the last data transfer the MASTER device performs, it must generate a Last Cycle signal that clears DACC and causes the access controller to return to the IDLE state at the end of the data transfer. Most TILINE device controllers are designed to steal only one TILINE cycle at a time and the Last Cycle control is wired permanently high.

TILINE Special Purpose Functions. In addition to the TILINE signals associated with data transfers and those that establish priority for TILINE access, there are five special function signals. These signals are TILINE I/O Reset (TLIORES–), TILINE Power Failure Warning Pulse (TLPFWP–), TILINE Power Reset (TLPRES–), TILINE Wait (TLWAIT–), and TILINE Hold (TLHOLD–).

The TILINE I/O Reset (TLIORES–) signal is generated by the central processor during execution of its I/O Reset Instruction or in response to the programmer panel RESET switch. TLIORES– is a 100- to 500-nanosecond low pulse on a normally high line. TLIORES– is also asserted whenever TLPRES– is asserted. TLPRES– is available to all devices connected to the TILINE. TLIORES– functions to halt and reset all TILINE I/O devices. The devices should reset in an orderly fashion in response to TLIORES– and any memory cycle in progress should be completed normally. For example, if a tape write is in progress an end of record sequence should occur. When a device is reset while active it must report abnormal completion status.

The TILINE Power Failure Warning Pulse (TLPFWP–) signal is generated by the power supply to indicate that a power shutdown is imminent. The signal is a low pulse that occurs at least 7.0 milliseconds before TILINE Power Reset (TLPRES–) occurs. The negative-going edge of this pulse causes the central processor to trap to the power failure trap location and the effect of the negative-going edge of TLPFWP– on connected TILINE I/O devices is the same as that of TLIORES–. TLPFWP– remains low until TILINE Power Reset is asserted.

The TILINE Power Reset (TLPRES–) is a normally high signal that goes low at least 10 microseconds before any dc voltage level from the power supply begins to fail due to normal shutdown or because of ac power failure. TLPRES– is generated by the power supply. TLPRES– remains low during and after a power failure. During ac power turn-on, TLPRES– remains at a low level until all dc voltages from the power supply are up and are stable. The purpose of TLPRES– is to reset all device controllers and the central processor during power failure and to directly inhibit all critical lines to external equipment that are powered by a separate power supply. For example, it is TLPRES– that prevents a tape deck from getting a rewind pulse when the central processor is powered up and down. During the power-up sequence, the TLPRES– resets all I/O controllers to their IDLE state and clears any device status information. As TLPRES– goes high indicating that power is up and stable, the central processor performs the power-up interrupt trap.

The TILINE Wait (TLWAIT–) is a normally high signal generated by TILINE Couplers that is used to resolve certain conflicts that can arise in computer-to-computer communication over the TILINE. The purpose of TLWAIT– is to directly disable (inhibit) the following signals from all TILINE MASTER devices (including central processors): TLGO–, TLREAD, TLADR–, and TLDAT–. Note, that these signals are not inhibited in SLAVE devices. The foregoing signals are disabled within 40 nanoseconds of the time that TLWAIT– is asserted and remain disabled as long as TLWAIT– stays low. This action should cause no state change in MASTER devices and except for its TILINE interface drivers, the MASTER device should be unaware that TLWAIT– has been asserted. TLWAIT– inhibits the MASTER device from "seeing" any TILINE Terminate

(TLTM–) or TILINE Memory Error (TLMER–) signals that occur and also holds the MASTER devices TILINE timeout timer reset. TLWAIT– allows TILINE Couplers to exercise a "higher than any" priority on the TILINE.

The TILINE Hold (TLHOLD–) is a normally high signal that is brought low by a central processor prior to the operand fetch of an ABS instruction. TLHOLD– remains low until the operand store cycle is complete or until the processor determines that the operand store is not needed. ABS is intended to be used as a software interlock. ABS reads a memory word, tests it, and then, if it was negative, subtracts it from zero and restores it to memory in its original location. In the use of ABS as a software interlock in multiprocessor systems it is possible for one processor to modify a memory word while another processor is performing an ABS instruction on that word. This interference would ruin the usefulness of ABS as a software interlock. The asserted TLHOLD– prevents this interference by holding TILINE access for the processor performing ABS. TLHOLD– is used and propagated by TILINE Couplers in multiprocessor systems.

3.2.2.4 TILINE Coupler. The TILINE coupler is a full-size 990 PWB used to provide direct memory communications between independent TILINEs in a multiple TILINE system. A TILINE coupler is installed in the main chassis or expansion TILINE chassis and a similar coupler is installed in the addon TILINE expansion chassis. Within this configuration, the coupler performs the following functions:

- Provides address and data buffering between the existing and addon TILINE
- Performs address translation so that remote memory may be mapped
- Resolves timing conflicts resulting from simultaneous data transfer requests in multiprocessor systems
- Provides intersystem interrupt capability and reports power status information via a CRU interface.

Coupler Functional Description. Figure 3-13 contains a functional block diagram of two TILINE couplers. The operation of the coupler based on this figure is presented in the following subparagraphs. For a typical write cycle from TILINE master to a remote slave, the following sequence occurs:

1. The appropriate address is placed on the TILINE (by the master) and TLGO– is asserted.
2. The local coupler delays TLGO– until it has had sufficient time to decode the TILINE address and add the bias. If the coupler recognizes the TILINE address then "ADDRESS OK" is sent to the slave control logic.
3. Delayed TLGO– is then used to set the START latch. At this time the address and data lines are turned on toward the remote coupler and START(OUT)– is sent.
4. At the remote coupler START(OUT)– is received by the master control logic as START(IN)–. This signal sets the DEVICE ACCESS REQUEST latch.

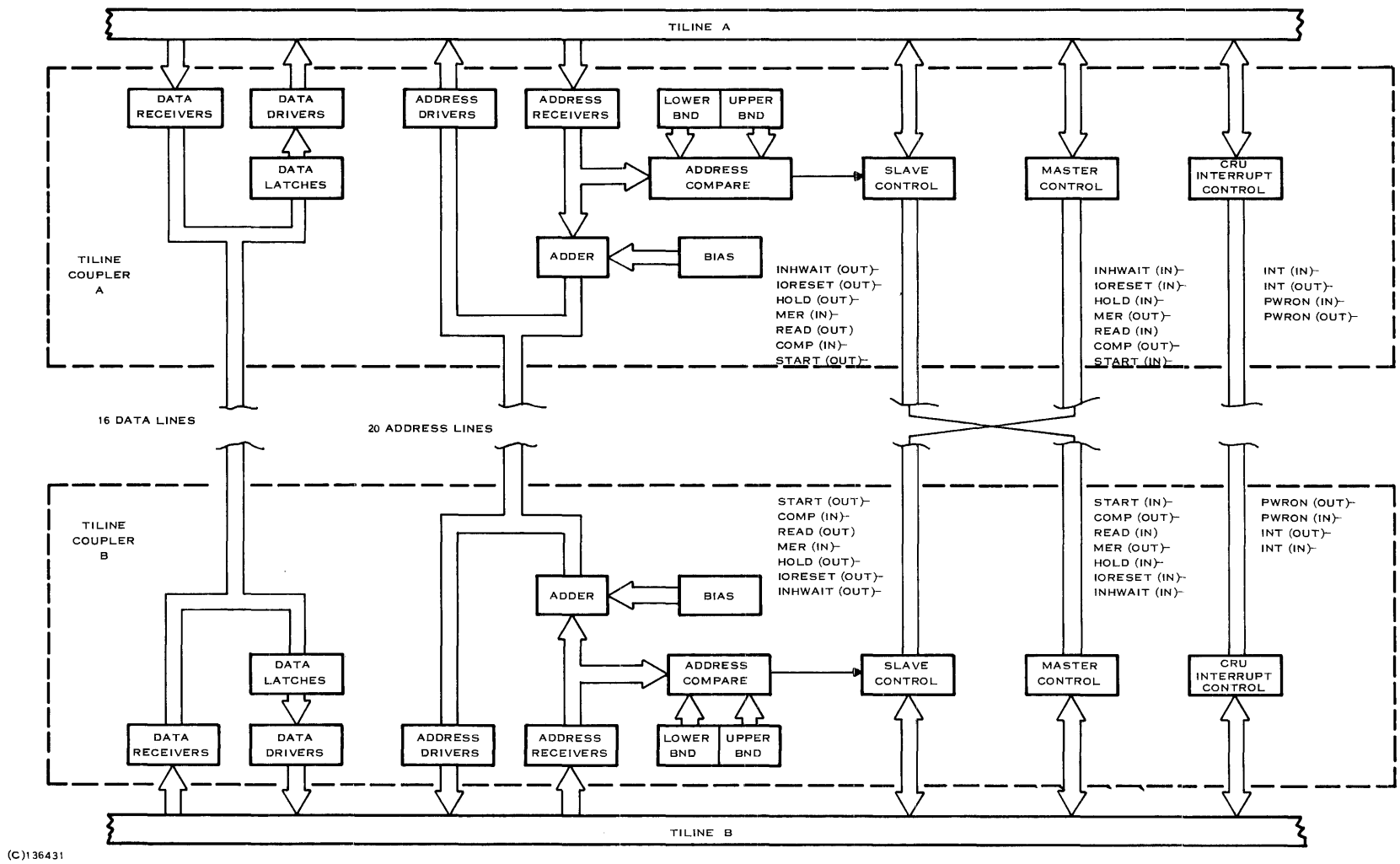


Figure 3-13. TILINE Coupler Functional Block Diagram

5. The remote coupler vies for access to the TILINE in the normal manner.

6. When access is achieved the address and data drivers are turned onto the TILINE.

7. As soon as TLTM– is released by the previous master then the coupler asserts TLGO–.

8. When TLTM– is received from the target slave a COMP(OUT)– is sent to the local coupler.

9. COMP(OUT)– is received by the local coupler's slave control as COMP(IN)–. This forces the START(OUT)– signal OFF and asserts TLTM–.

10. The remote coupler disengages as a result of START(IN)– being released.

11. When TLGO– is released by the master then the local coupler drops TLTM– and the write cycle is complete.

A timing diagram for the TILINE coupler write cycle is shown in figure 3-14.

When a TILINE master wants to perform a data read from a remote slave, the following sequence occurs:

1. The appropriate address is placed on the TILINE, by the master, and TLGO– is asserted.

2. The local coupler delays TLGO– until it has had sufficient time to decode the TILINE address and add the bias. If the coupler recognizes the TILINE address "ADDRESS OK" is sent to the slave control logic.

3. Delayed TLGO– is then used to set the START latch. At this time the address lines are turned on toward the remote coupler and START(OUT)– is sent.

4. At the remote coupler START(OUT)– is received by the master control logic as START(IN)–. This signal sets the DEVICE ACCESS REQUEST LATCH.

5. The remote coupler vies for access to the TILINE in the normal manner.

6. When access is achieved the address drivers are turned onto the TILINE.

7. As soon as TLTM– is released by the previous master the coupler asserts TLGO–.

8. When TLTM– is received from the target slave the data drivers are turned onto the cable and COMP(OUT)– is sent to local coupler.

9. When COMP(IN)– is received by the local coupler the data on the cable is held in a set of data latches, the START(OUT)– line is released and TLTM– is asserted.

10. The remote coupler disengages.

11. When TLGO– is released by the master then the local coupler releases TLTM– and the data read cycle is complete.

A timing diagram for a TILINE coupler read cycle is shown in figure 3-15.

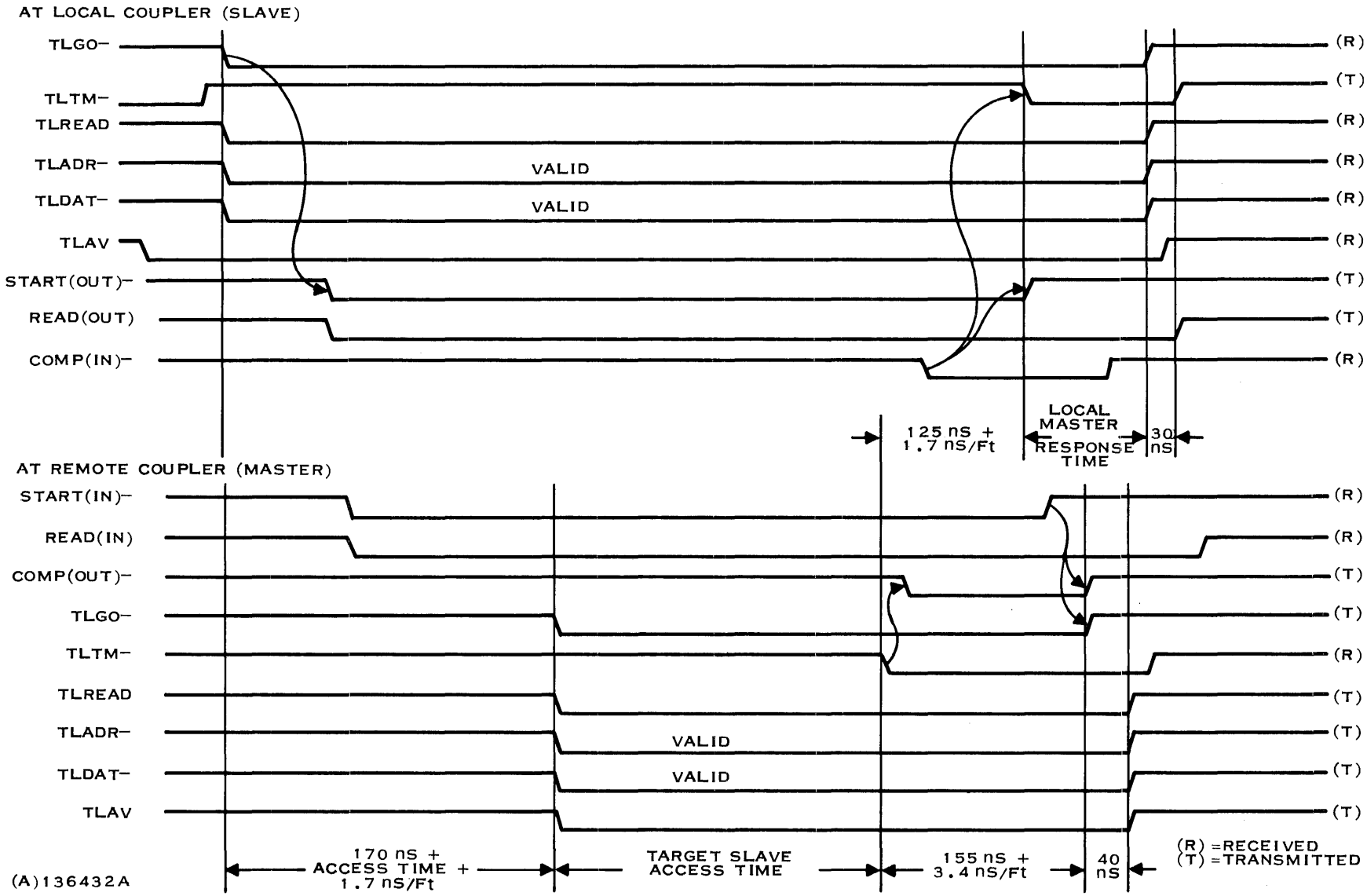


Figure 3-14. TILINE Coupler Write Cycle Timing Diagram

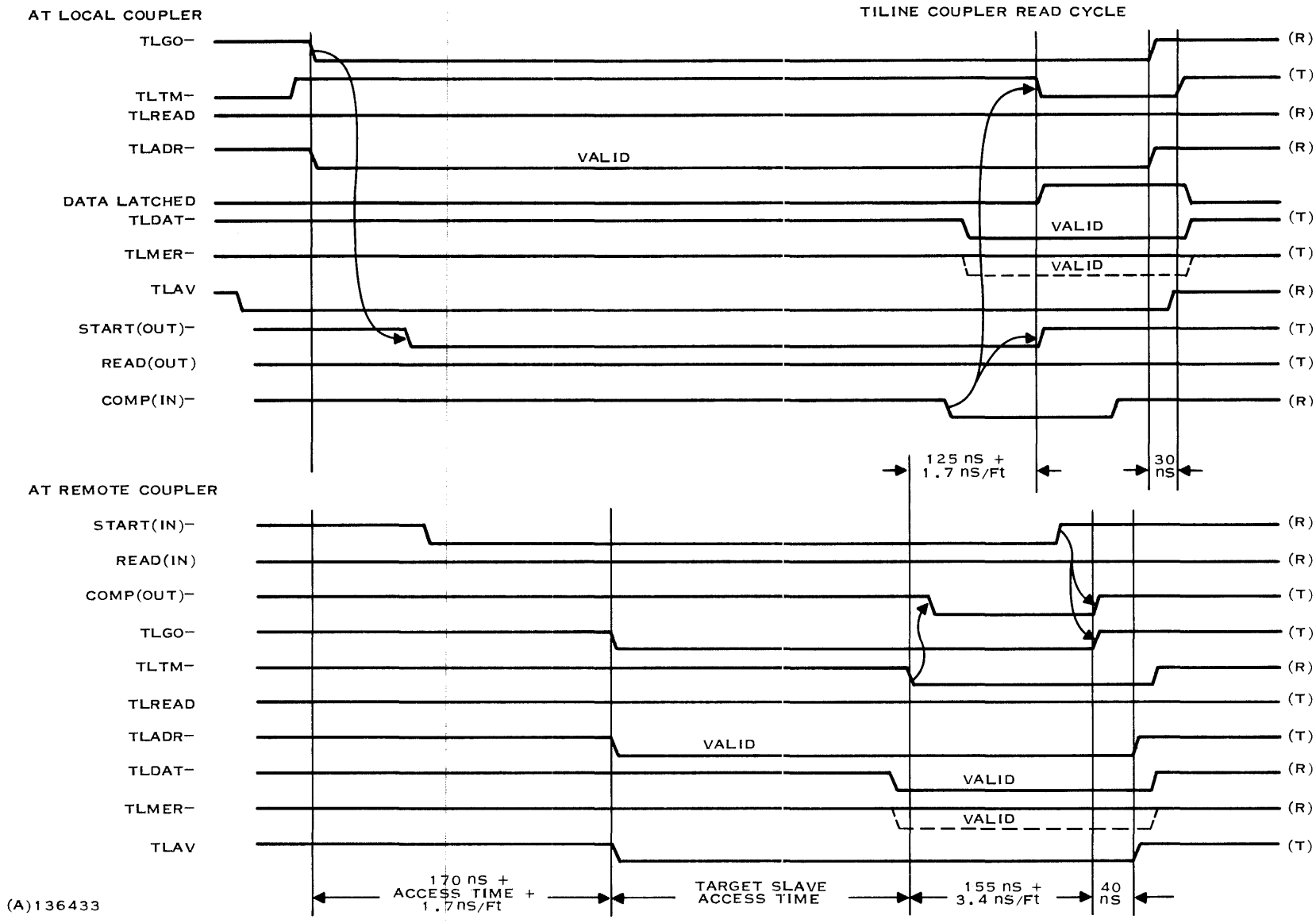


Figure 3-15. TILINE Coupler Read Cycle Timing Diagram

In multiprocessor systems there is a very high probability that two CPUs attempt a data transfer across the coupler simultaneously. In order to resolve this conflict the couplers recognize a "preferred" direction. The coupler which has master responsibility in the preferred direction issues a TLWAIT– signal. This is a signal to all other TILINE masters to relinquish control of the bus immediately pending a high priority data transfer from a coupler. The coupler now goes ahead and performs its data transfer. When TLWAIT– is released, then the master which had to release the bus may continue. This action causes no state change in master devices, and with the exception of its TILINE drivers, the master device does not realize that TLWAIT– has been asserted. The "preferred" direction for data transfer is established by the control cable. It may be viewed as a vector pointing in the preferred direction.

The ABS instruction is intended to be used as a software interlock. ABS reads a memory word and then, if it is negative, writes the 2's complement of it back in the same location. In multiprocessor systems it would be possible for one processor to modify a memory location between the read and write cycles of another CPUs ABS instruction.

In order to prevent this, the 990/10 CPU issues TLHOLD–. It is used and propagated by TILINE couplers in order to maintain the effectiveness of ABS as a software interlock. TLHOLD– will prevent couplers from releasing access to the TILINE during an ABS instruction thus insuring that no other CPU can modify the ABS target memory location.

Typical System Configuration. Figure 3-16 shows an example of a multiprocessor system using TILINE couplers. In this system:

- Each CPU can address all 48KB.
- As long as each CPU addresses local memory it does not interfere with the other systems.
- When a CPU addresses remote memory it steals cycles from the remote CPU.
- Each CPU can interrupt or be interrupted by the other CPUs.
- Couplers are designed to be self-isolating when powered down. If a chassis is powered down, or if the control cable is disconnected, then "TILINE TIMEOUT" interrupts will occur in the CPU attempting to use that link. Otherwise, the system will work normally.

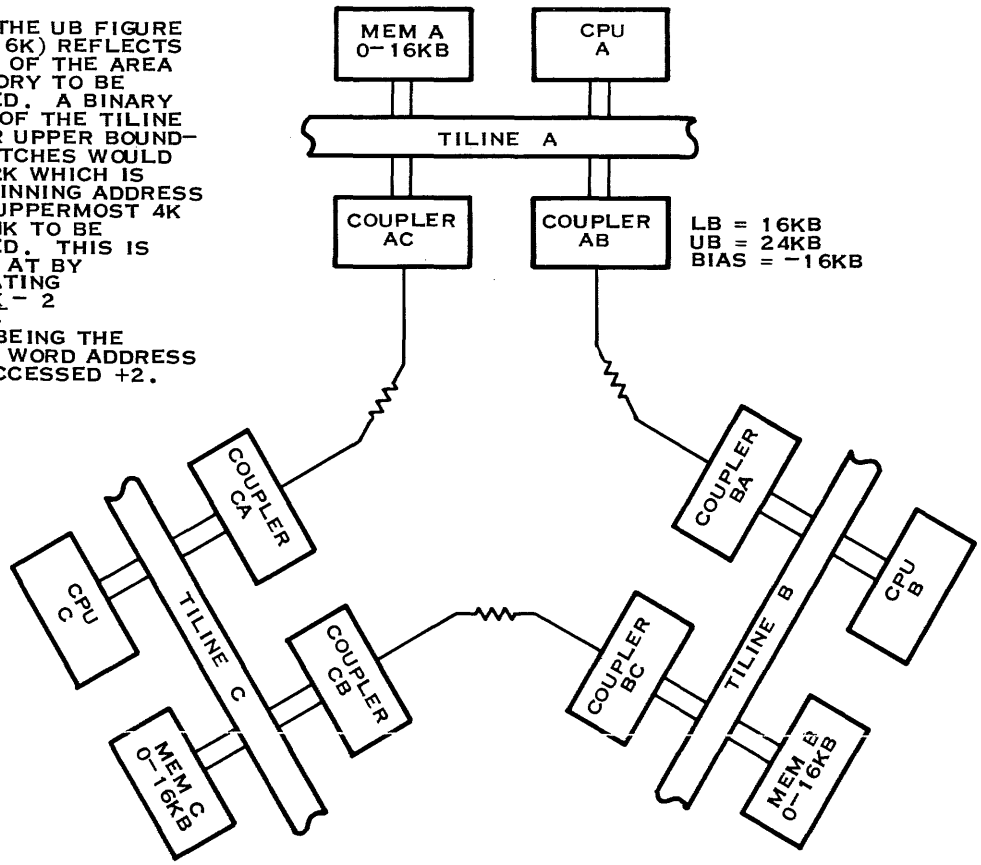
Illegal Configurations. There are few limitations to the number of processors or network geometry in multiprocessor systems using TILINE couplers. However, a TILINE bus addressing itself over couplers is not allowed. For example, in figure 3-16, CPU A cannot be allowed to address memory A through TILINES B and C. If it were to make this attempt, coupler AC could not acquire access and the system is locked up. After 10 microseconds a TILINE timeout will occur and unlock the system.

Interface Description. There are two cables which connect TILINE couplers. One cable is a 40-conductor, 65 ohm, shielded ribbon cable which carries the 16-bit data word, the 20-bit data address and the nonmaskable interrupt line. This cable connects to P4 on the TILINE coupler PCB which is a 40-pin header. The cable is connected so that PIN number 1 on one coupler goes to PIN number 1 on the other coupler as shown in figure 2-22. The pinout for this cable is given in figure 3-17.

NOTE: THE UB FIGURE GIVEN (16K) REFLECTS THE TOP OF THE AREA OF MEMORY TO BE ACCESSED. A BINARY DECODE OF THE TILINE COUPLER UPPER BOUNDARY SWITCHES WOULD SHOW 12K WHICH IS THE BEGINNING ADDRESS OF THE UPPERMOST 4K RAM BANK TO BE ACCESSED. THIS IS ARRIVED AT BY CALCULATING

$$\frac{X}{4} - 2$$

WITH X BEING THE HIGHEST WORD ADDRESS TO BE ACCESSED +2.



MEMORY MAP

	CPU A	CPU B	CPU C
MEM A	0-16KB	32KB-48Kb	16KB-32KB
MEM B	16KB-32KB	0-16KB	32KB-48KB
MEM C	32KB-48KB	16KB-32KB	0-16KB

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Figure 3-16. Typical Multiprocessor System Block Diagram

The remaining cable is a 20-conductor, 65 ohm, shielded ribbon cable which carries the coupler control signals. This cable connects to P3 on the PCB which is a 20-pin header. In order to establish the cable vector, pin 11 is removed from the cable connector at the end pointed to by the vector prior to assembly. The cable is assembled so that PIN number 1 at one end is PIN number 20 at the other. The pinout for this cable is given in figure 3-18.

The pinout for the two bottom edge connectors (P1 and P2) is given in figure 3-19.

If a TILINE coupler is implemented in a chassis with no CPU then the 20-pin header P5 provides a place to hook up the front panel cable. Its function is simply to provide power for the "POWER" LED. (See figure 3-20 for pinout.)

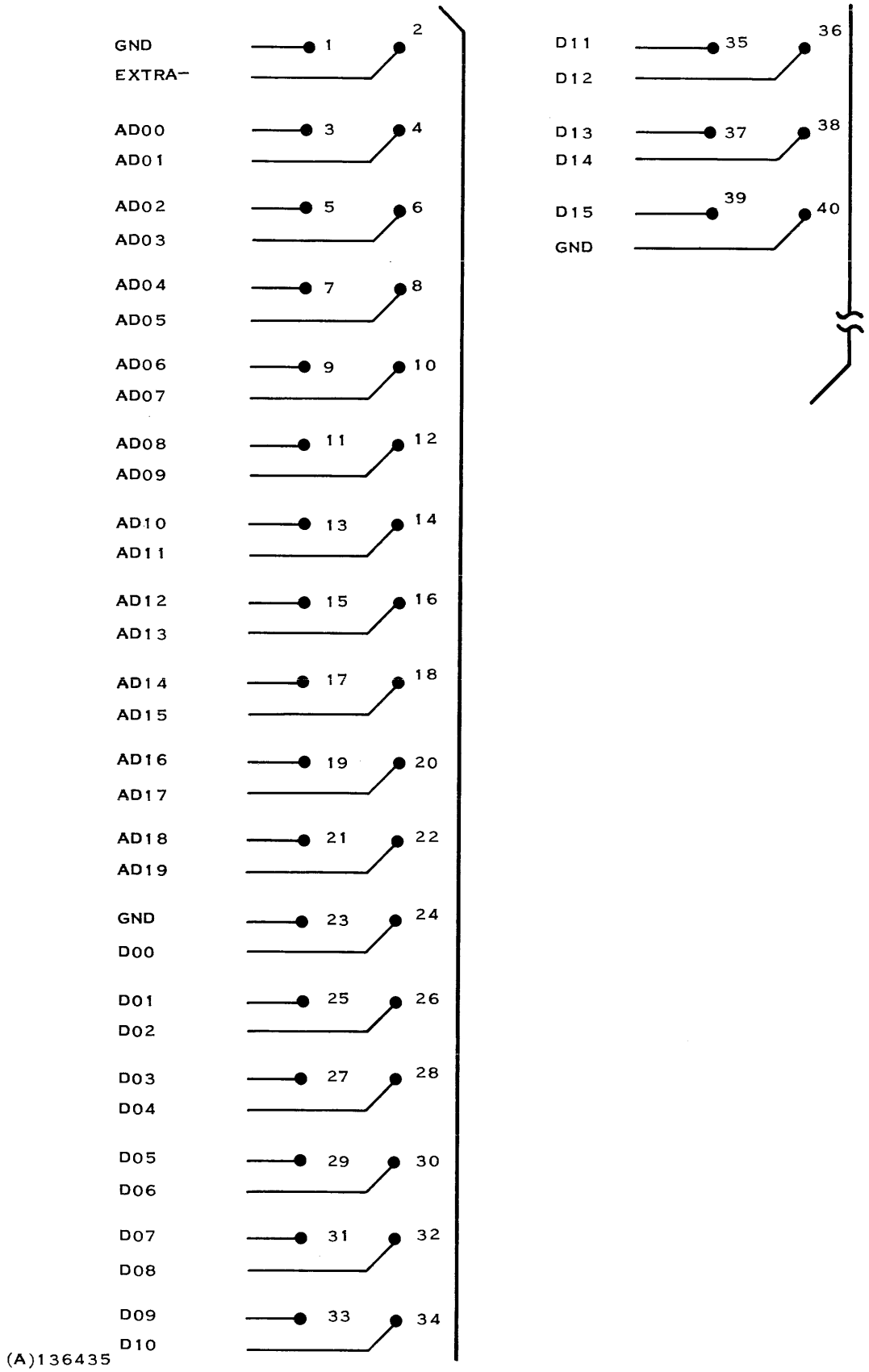


Figure 3-17. Data Address Cable Pinout

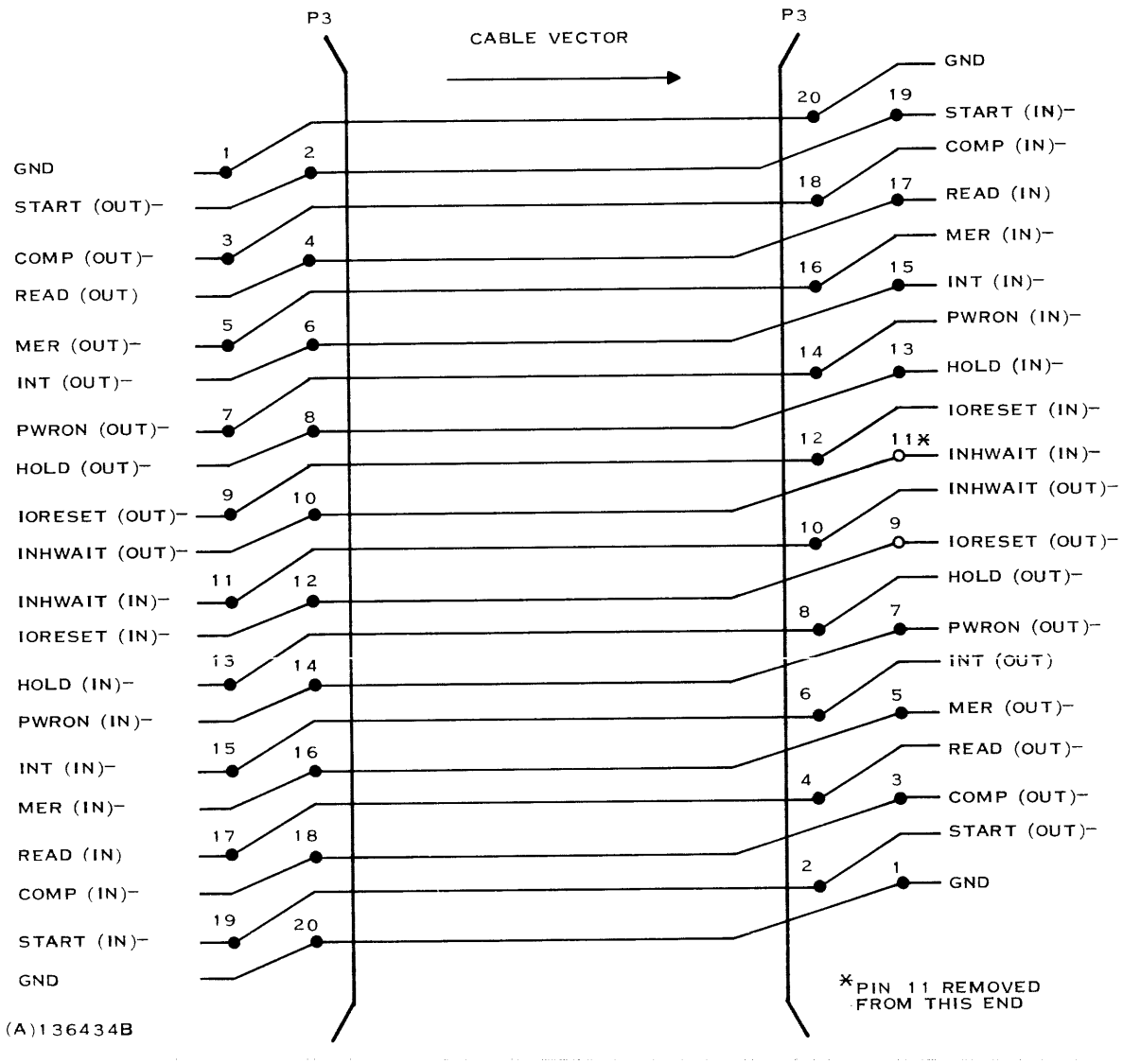


Figure 3-18. Control Cable Pinout

P1				P2			
GND	1	2	GND	GND	1	2	GND
+5 MAIN	3	4	+5 MAIN	+5 MAIN	3	4	+5 MAIN
	5	6		TLAG(OUT)	5	6	TLAG(IN)
	7	8		GND	7	8	TLADR14-
	9	10		TLADR15-	9	10	TLADR10-
TLREAD	11	12	GND	TLADR12-	11	12	TLADR11-
	13	14		TLPRES-	13	14	TLIORES-
GND	15	16		TLADR13-	15	16	
GND	17	18	CRUBITOUT	TLADR08-	17	18	
GND	19	20	TLTM-	TLADR09-	19	20	TLDAT11-
GND	21	22	STORECLK-	TLDAT08-	21	22	
	23	24	GND	TLDAT10-	23	24	GND
TLGO-	25	26	GND	TLDAR18-	25	26	TLHOLD-
TLDAT12-	27	28	TLDAT13-	TLADR17-	27	28	
	29	30	TLDAT14-	TLDAR16-	29	30	
TLDAT15-	31	32	CRUBIT13	TLDAR19-	31	32	
	33	34	CRUBIT15	TLDAT09-	33	34	
	35	36	CRUBIT12	TLDAT02-	35	36	
	37	38	CRUBIT15	TLDAT03-	37	38	
	39	40			39	40	
	41	42			41	42	
	43	44		TLDAT06-	43	44	TLADR01-
	45	46		TLDAT07-	45	46	
	47	48		TLADR06-	47	48	
	49	50	CRUBIT7	TLADR07-	49	50	
	51	52	CRUBIT6	TLADR02-	51	52	
	53	54	CRUBIT5	TLADR03-	53	54	
TLMER-	55	56	CRUBIT4	TLADR00-	55	56	
GND	57	58	TLAV	TLADR04-	57	58	GND
GND	59	60	CRUBITIN	TLADR05-	59	60	
	61	62	CRUBIT8	TLDAR04-	61	62	
TLWAIT-	63	64	CRUBIT9	TLDAT05-	63	64	
	65	66	INTA-		65	66	EXINT-
	67	68	CRUBIT10	TLDAT00-	67	68	
	69	70	CRUBIT11	TLDAT01-	69	70	
TLAK-	71	72	GND		71	72	
	73	74	GND		73	74	
	75	76			75	76	
+5 MAIN	77	78	+5 MAIN	+5 MAIN	77	78	+5 MAIN
GND	79	80	GND	GND	79	80	GND

(A)136436

Figure 3-19. Bottom Edge Connector Pinout

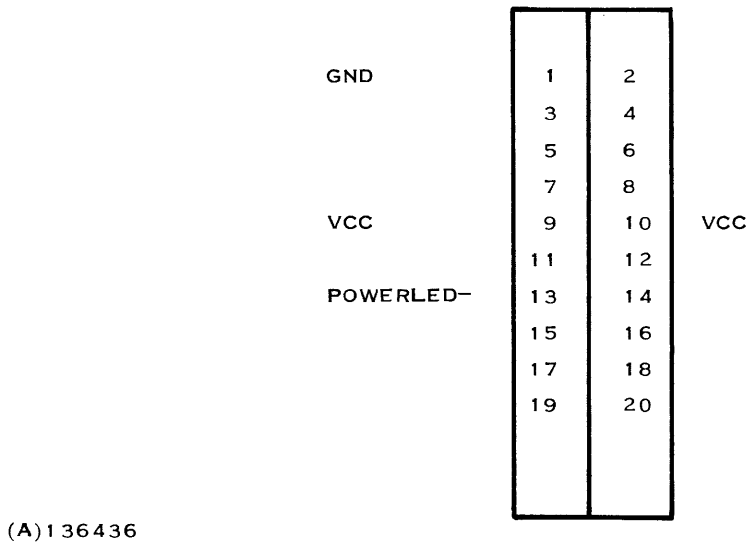


Figure 3-20. Front Panel Connector Pinout

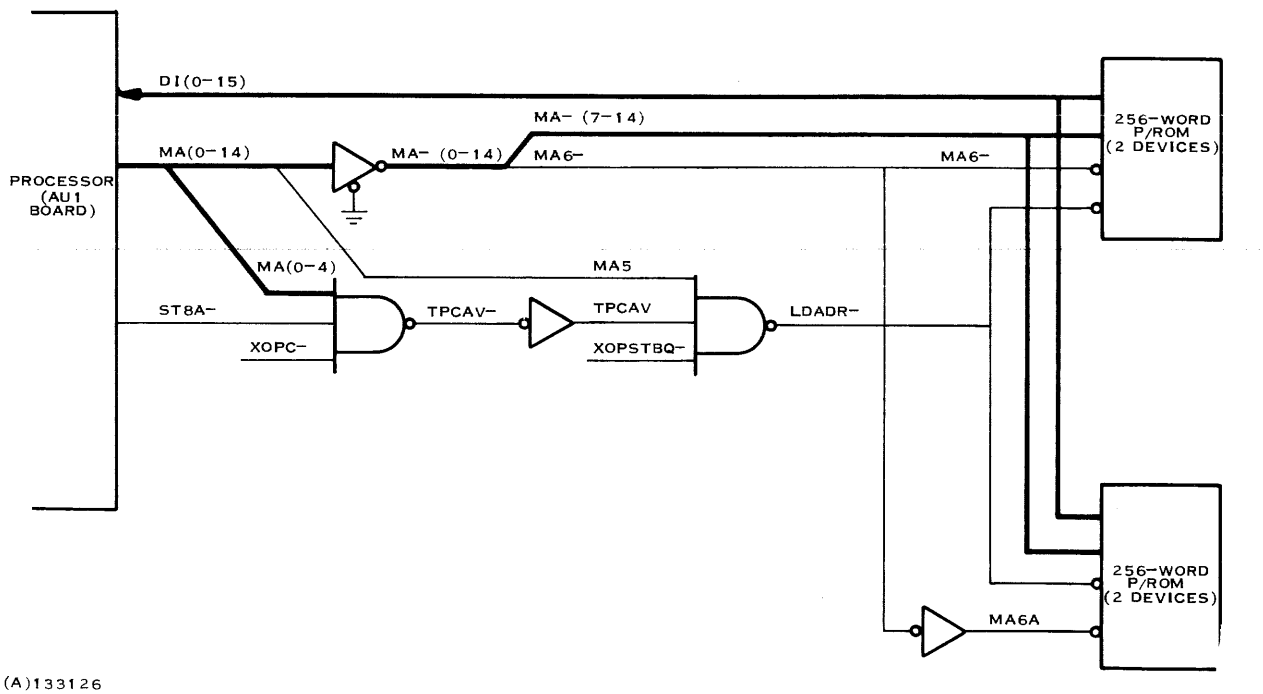


Figure 3-21. Simplified Functional Block Diagram P/PROM

3.2.3 **PROGRAMMABLE READ-ONLY MEMORY.** Up to 1K bytes of TTL programmable read-only memory (PROM) in 512-byte increments may be implemented on the system interface board by installing two 512-byte by 8-bit PROM devices in the four sockets provided. The TTL PROM may be implemented in one of several loaders options with or without a self-test feature. The PROM devices are the Texas Instruments SN74S471s that can be electronically permanently programmed and may be furnished to the user unprogrammed to permit development by the user of a custom loader. A low level signal is required at both of two chip-select pins of the PROM device to enable the device. When not enabled, the high-impedance three-state output of the device permits direct interface with the internal 990/10 data bus.

The 1K bytes of TTL PROM is addressed at central processor addresses $FC00_{16}$ to $FFFF_{16}$. As shown in the functional block diagram of the TTL PROM, figure 3-21, a low loader-addressed signal, LDADR–, is applied as one enabling signal to each of the devices. For the loader address to be developed, memory address bits MA0 through MA5 must all be high. Additionally, status register bit 8 must be cleared by software (ST8A– = 1) and no hardware implemented XOP instructions may be in progress (XOPC– and XOPSTBQ– both high). With LDADR– low and applied as an enabling signal to each PROM device, memory address bit 6 (or its complement) applied to the other chip-select pin enables one or the other of the two 512-byte groups of PROM. With both chip-select pins enabled, the memory word as addressed by memory address bits 7 through 14 is placed on the data bus for input to the processor.

3.2.4 **SYSTEM CLOCK.** Timing and control for the processor on the AU1 circuit board, for control and interrupt logic on the system interface board, and timing for the CRU interface and for the TILINE are derived from the system clock that is located on the system interface board.

In a computer system such as the 990/10 where the speed of the asynchronous memory devices approaches that of the system clock rate if a commonly used method of clocking the input from memory into a flip-flop using a synchronous system clock is employed at the interface, then on the average half a system clock period is wasted. In effect, memory is slowed by 50 percent. To avoid this inefficiency, the 990/10 uses a memory-speed dependent clock wherein during a memory read or write cycle the asynchronous "memory complete" (TLTM–) signal fires a pulse generator that is used as the system clock.

The basic element of the system clock is the timer circuit (or pulse generator) as shown in figure 3-22. The delay from input to output of the timing circuit is established by the RC time constant of resistor R and capacitor C. By selecting temperature-stable components, the ability to repeat pulse width is typically better than ± 5 percent over maximum temperature and power voltage ranges. The central processor is designed to operate with a system clock rate no faster than 250 nanoseconds. With 5 percent accuracy, the clock rate is set for a nominal rate of 263 nanoseconds to ensure that the 250 nanosecond-rate is not exceeded. This 5 percent loss in speed occurs, however, only when the clock is free-running (which does not often occur).

As shown in figure 3-23, the system clock consists of three timer circuits and associated TTL logic. The clock operates in either one of two modes: one where it generates a clock for a memory state and the other where it generates a clock for a run state as established by the cycle request signal CYREQ from the processor. A high CYREQ signals that the operation in progress is a memory cycle state and the clock operates in the memory state mode. When CYREQ is low, the clock operates in the run state mode.

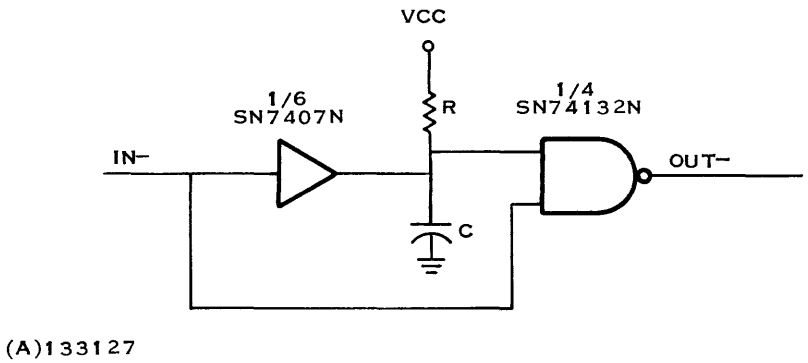


Figure 3-22. Timer Circuit Schematic

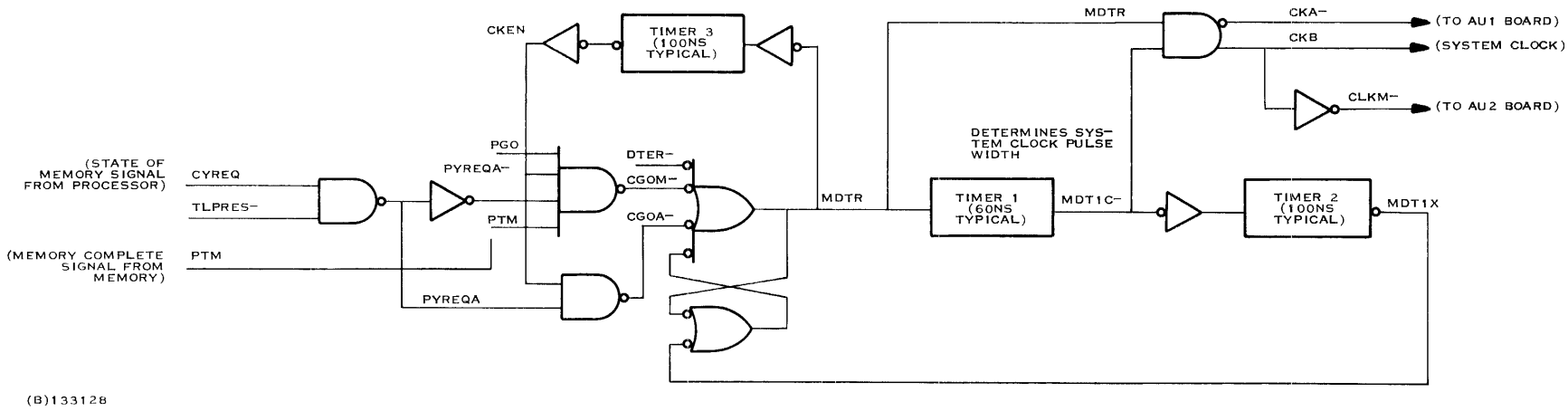


Figure 3-23. Simplified Functional System Clock Diagram

For a memory state cycle, the clock operates as follows. As CYREQ goes high, the high PYREQA– developed is applied as one input to a NAND gate. ANDed with PYREQA– is the clock enable signal, CKEN, that goes high as TIMER 3 times-out to indicate that the previous clock cycle is complete. Then as memory complete signal PTM goes high, a low CGOM– at the output of the NAND gate starts a new clock cycle as clock signals CKA– and CLKM– go low and CKB goes high. After TIMER 1 time-out completion, the clocks change state and the processor transitions to the next microcontrol state. TIMER 2 and TIMER 3 must time-out before a new clock start is enabled as signalled by the high CKEN signal at the output of TIMER 3. If the new state is to be another memory cycle, the previously described operation is repeated with the start of the clock keyed to the receipt of a memory complete signal.

If the new state is not a memory cycle, the low CYREQ signal from the processor provides a high PYREQA signal that is ANDed with CKEN and the start of the clock is now caused by the low CGOA– signal as the system clock is no longer memory-dependent but simply waits for completion of the previous clock cycle.

3.2.5 **INTERRUPTS.** The 990/10 computer uses sixteen priority-vectored interrupt levels. A priority ranking system assigns numbers from 0 (highest priority) to 15 (lowest priority) to the levels so that interrupt conflicts can be resolved. Interrupt inputs are synchronized with the system clock on the system interface board, are encoded, and presented to the processor along with an interrupt request, INTPRES. The interrupt levels are vectored for rapid reaction to recognized interrupts. That is, corresponding to each interrupt level is a 2-word vector located in low-order memory (addresses 00 through 3E, hexadecimal). When the processor recognizes an interrupt, it loads the vector for that level into the workspace pointer register (first vector word) and program counter register (second vector word) to define the new workspace pointer and program starting point for the interrupt servicing routine. The old values of PC, WP, and ST are saved in the new workspace. When the interrupt routine is complete, the processor returns to the program that was executing when the interrupt occurred by restoring the original values to the PC, WP, and ST registers. Should a higher priority interrupt occur while an interrupt service subroutine is executing, the processor honors the interrupt after completing the current instruction. The processor enters the higher priority interrupt subroutine and preserves the linkage to the earlier interrupt in the same manner described for the first interrupt. Thus, many interrupts can occur simultaneously with the processor maintaining an orderly linkage between the interrupt programs. Table 3-5 lists the interrupt levels, assignments, vector location, and mask information. The level 0 interrupt is reserved for the power-up interrupt and seven other interrupt conditions (eight for computers with memory mapping feature) are implemented by the 990/10 computer that are internal to the operation of the computer as described in the following paragraph.

A power failure warning pulse (TLPFWP–) generated by the power supply is brought into the system interface board at pin 16 of P1 and applied to the input of a priority interrupt level encoder so as to generate a level 1 interrupt. Four internal central processor error functions are implemented by logic on the system interface board so that if any one of the four error conditions occur, a level 2 error interrupt is generated. These conditions are: memory data error (MEMER–), illegal operation (ILLOPSET–), device/TILINE timeout (DTER–), and privileged instruction violation (PRIVOPSET–). Additionally, if the system interface board includes the memory mapping feature, a memory mapping error signal (ERRORL–) also generates a level 2 interrupt.

Table 3-5. Interrupt Level Data

Interrupt Level	Vector Location (Trap Address)	Device Assignment	Enabling Mask Values
0	00	Power up	0 through F
1	04	Power failure	1 through F
2	08	Error	2 through F
3	0C	Open	3 through F
4	10	Card reader	4 through F
5	14	Real time clock	5 through F
6	18	733 ASR	6 through F
7	1C	Floppy disc	7 through F
8	20	Open	8 through F
9	24	CRT No. 3	9 through F
10	28	CRT No. 2 or CRU expansion	A through F
11	2C	CRT No. 1	B through F
12	30	Open	C through F
13	34	Diablo disc	D through F
14	38	Line printer	E and F
15	3C	PROM programmer	F only

Interrupt levels 3 through 15 are available for assignment to external devices. The 990 Family System Software supports peripherals at specified interrupt levels as shown in table 3-5. Interrupt jumpers are configured at the factory for 990/10 standard systems. Users may reconfigure interrupts easily to suit specific applications.

3.2.5.1 **Masking.** The processor uses a 4-bit field in the status register to determine the lowest priority interrupt that will be recognized during a program operation and also to ensure that an interrupt service routine will not be halted due to another interrupt of equal or lower priority. At the start of a program, the mask field in the status register is loaded with the mask value. The processor compares this value with any interrupts that occur. If the level of the interrupt is equal to or less than the mask value (equal or greater priority), then the processor recognizes the interrupt and calls the service routine for that interrupt level. When the processor sets up for the service routine, it loads a value into the mask field that is one less than the interrupt level being serviced, thereby disabling interrupts from devices of equal or lower priority. The enabling mask values for the different interrupt levels are as shown in table 3-5.

3.2.5.2 **TTL Logic for Interrupt Implementation.** The TTL logic for implementing interrupt levels 1 through 15 is located on the system interface board and consists, in main, of three SN74174s and two SN74148s along with flip-flop circuits for setting and resetting those interrupts generated on the circuit board itself. Figure 3-24 is an extraction from the logic diagram for the system interface board and has been reproduced here for convenience. The SN74174s each contain six D-type flip-flops with single-rail outputs with only two of the flip-flops of the third SN74174 in use for a total of 14 flip-flop circuits. The 14 interrupts (TLPFWP–, and I3- through I15-) are applied as D-inputs to the SN74174s and are transferred to the Q-outputs on the positive transition of the CLKM-clock signal. Here they are applied as inputs to the two cascaded SN74148 8-line-to-3-line priority encoders. Also applied to the input of the SN74148s is the level 2 error interrupt signal, INTINT–. The encoders provide a binary coded interrupt level at signals LEVO through LEV3 that corresponds to the highest priority interrupt level input. An interrupt, at any level, causes a high INTPRES signal to be generated and applied to the processor along with signals LEVO through LEV3.

Power Failure Interrupt. When ac power begins to fail, a sensor in the power supply generates a low TLPFWP– pulse that is applied to the system interface board. TLPFWP– is applied as an input to an SN74174 and is encoded as a level 1 interrupt. At this point, the computer has 7.0 milliseconds of program time before a power supply reset (TLPRES–) halts operation. This interrupt sets the interrupt mask in the status register to 0.

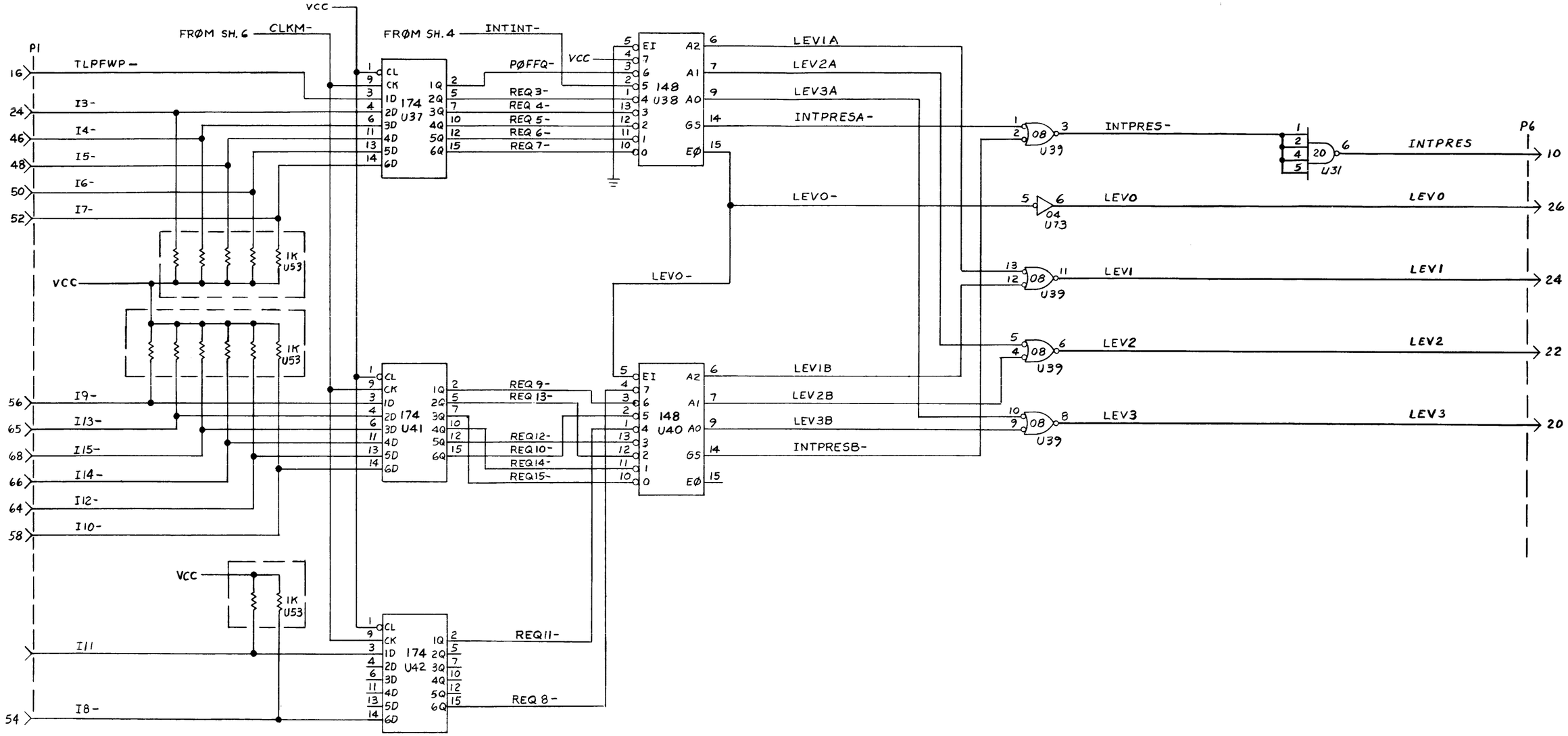
Error Interrupt. Logic to generate a level 2 interrupt in the event a system error occurs is included on the system interface board as shown in figure 3-25. The error interrupt is a merging of all system errors. Each error is stored on the system interface board and is read and/or cleared through the CRU interface and additionally is cleared by either an I/O reset or master clear.

The processor develops a CRU bit address from the CRU base address contained in workspace register 12 added to the signed displacement contained in bits 8 through 15 of the three single-bit CRU instructions: Test Bit (TB), Set Bit to One (SBO), and Set Bit to Zero (SBZ). The CRU base address loaded into workspace register 12 to address the error interrupt logic either to read or clear is hexadecimal 1FCO. The memory mapping error is cleared by addressing CRU output bit 4 at CRU base address hexadecimal 1FAO. The CRU input and output bit assignments that address the error interrupt logic are as shown in table 3-6.

Illegal operation codes that generate the ILLOPSET– signal are as shown in table 3-7.

Each of the stored error condition signals is applied as one input to an SN74151 data selector/multiplexer and as one input to a NOR gate. Any error condition results in the generation of a low internal interrupt INTINT– signal that is applied to the priority interrupt level encoder to generate a level 2 interrupt. A single-bit CRU instruction to read the error interrupts generates a high INTSEL signal and a low INTESL– signal. The error signal input to the data selector/multiplexer as addressed by memory address bits MA12- through MA14- is selected for output to the processor as the CRUBITINA signal. Memory address bits MA12- through MA14- also address an SN7442 BCD-to-decimal decoder to generate a low that clears the addressed error signal on the next CLKMA– clock pulse.

Real Time Clock Interrupt. The power supply contains a line frequency synchronized clock that generates the 100 or 120 Hz signal. The real time clock interrupt logic is implemented on the system interface board (see figure 3-17). A signal is generated every 8.33 or 10.0 milliseconds to provide a level 5 interrupt request. The interrupt is enabled by a high IR10A from the processor that is generated by the control instruction CKON. The interrupt is cleared by either a low IR10A signal generated by a CKOF instruction or IORES– generated by a RSET instruction. IORES– is also generated by the TLPRES– power-up sequence from the power supply. Though the real time clock is normally wired for level 5 interrupt it may be wired for level 15 interrupt. When the level 5 interrupt is taken, the processor sets the interrupt mask to 4.



(B) 133129

Figure 3-24. Priority Interrupt Level Encoder

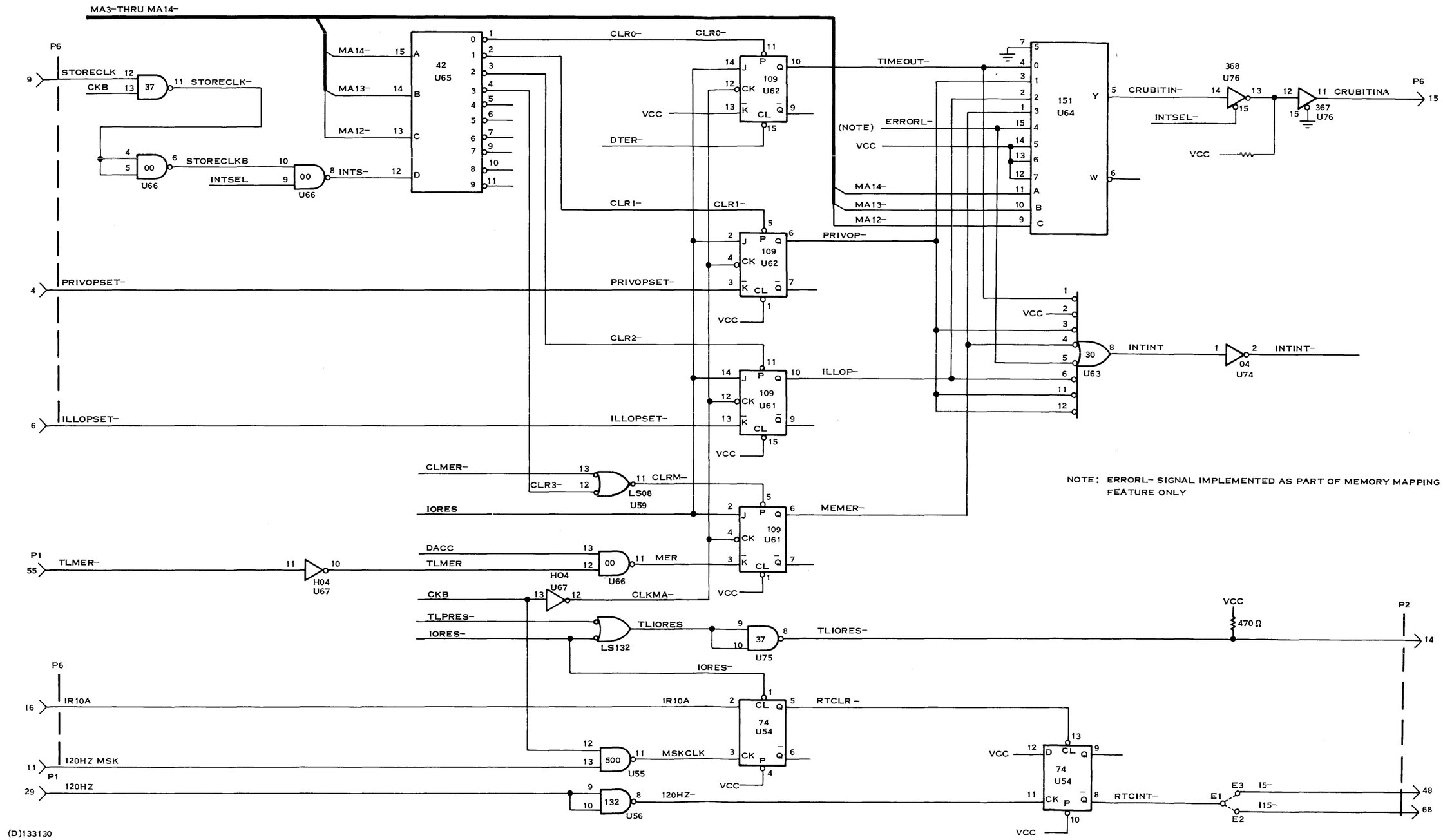


Figure 3-25. Error Interrupt and Real Time Clock Interrupt Logic

Table 3-6. Error Interrupt Logic CRU Bit Assignments (CRU Base Address $1FC0_{16}$)

Input Bit	Output Bit	Error Condition
11		Memory Mapping Error
12	12	Error from TILINE memory (parity/error correcting)
13	13	Illegal Operation
14	14	Privileged instruction fetch with privileged mode off
15	15	TILINE timeout

Table 3-7. Illegal Operation Codes

BIT	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	0	0	0	0	1	1	X	X	X	X	X	X	X	X	X	X
	0	0	0	0	0	0	1	1	1	X	X	N	N	N	N	N
	0	0	0	0	0	0	1	1	0	1	X	N	N	N	N	N
	0	0	0	0	0	0	1	1	0	0	0	N	N	N	N	N
	0	0	0	0	0	0	1	0	1	1	1	N	N	N	N	N
	0	0	0	0	0	0	1	0	1	1	0	N	X	X	X	X
	0	0	0	0	0	0	1	0	1	0	X	N	X	X	X	X
	0	0	0	0	0	0	1	0	0	X	X	N	X	X	X	X
	0	0	0	0	0	0	0	X	X	X	X	X	X	X	X	X

X = DON'T CARE

N = ILLEGAL IF NOT ZERO

External Interrupts. Interrupt requests from external devices or from internal central processor interrupt functions may be wired to any of thirteen interrupt request lines (I3- through I15-) on the card-edge connector of the system interface board. The lines form 13 separate wired-or interrupt buses. A 1K pull-up resistor is located on the circuit board for each interrupt line. Each request signal must be an active low signal driven by an open-collector TTL gate. The request signal must remain active until it is reset by software communication. The request signal should be reset at some time before the interrupt service program executes RTWP or the central processor will repeat the trap.

NOTE

System software is highly dependent on the interrupt structure of the computer. Any deviations from standard interrupt configurations must be brought to the attention of the system programmer before or during software installation.

3.2.6 **XOP HARDWARE INTERFACE.** As a performance enhancement, the 990/10 provides an interface at connector P8 on the system interface board that permits connection of hardware modules to perform complex arithmetic and logical operations with greater efficiency than can be achieved with a software subroutine. The extended operation (XOP) feature is an integral component of the software XOP instruction. When the processor begins execution of an XOP instruction, a check is made to determine if a hardware module for that function is included in the chassis. Only if the hardware module is not included does the processor call the software subroutine for that function from memory. The following paragraphs describe the operation of the XOP interface.

3.2.6.1 **XOP Interface Signals.** The XOP hardware interface uses six exclusive signals, plus five signal types used by the TILINE and other devices, to control actions of an XOP circuit board. Figure 3-26 shows the interface lines connecting the XOP module to the system interface board. Table 3-8 defines these signals and lists the system interface board pin numbers for each signal.

3.2.6.2 **XOP Hardware Operation.** An XOP module processes a set of data to produce an end product that is either stored in memory as data, reported to the AU through status bits, or a combination of the two methods. In addition, the module continuously monitors the instructions sent to the AU when the module is not active. An extended operation cycle begins when the AU reads an XOP instruction from memory. Figure 3-27 illustrates the timing of interface signals during the entire XOP cycle using a hardware module. The following subparagraphs describe the operation.

Instruction Monitoring and Acquisition. Each time that the AU fetches a new instruction from memory and receives the termination indication from memory, the AU produces a clock pulse (XOPIAQCK–) to the XOP module, allowing the module to capture the op code and D field portions of the instruction from the TILINE data bus. The module then decodes that portion of the instruction to determine if the module will process that instruction. If the module cannot perform the requested function, the module does nothing and waits for another instruction to be acquired. However, if the module can perform the operation, it activates XOPTHERE– to indicate to the AU that the hardware module is present and active. This signal must be active within 200 nanoseconds of the instruction acquisition clock (XOPIAQCK–) and must remain active until the AU recognizes its presence by transmitting the operand address to the XOP module.

Address Transfer. The XOP instruction may use the TS field of the instruction to modify the source address for the XOP data. In this case, the S field of the instruction does not contain the true, effective address of the XOP data, and the AU must modify that value before it can be used by the XOP module. For this reason the XOP module does not capture the TS and S fields during the instruction acquisition phase. Instead, the module holds XOPTHERE– active until the AU has determined the effective address. At that point (500 nanoseconds minimum delay), the AU issues XOPSTB– and places the effective address on the TILINE address lines. The address remains on the lines and the strobe remains active until the XOP module returns TLTM– to indicate that it has captured the address in its address register. The AU's time out function clears the address and strobe lines if the XOP module fails to respond. If the XOP module desires data from the effective address rather than the address itself, the module may assert TLGO– to fetch an operand at the address. The addressed memory responds with TLTM– to indicate the end of the data transfer.

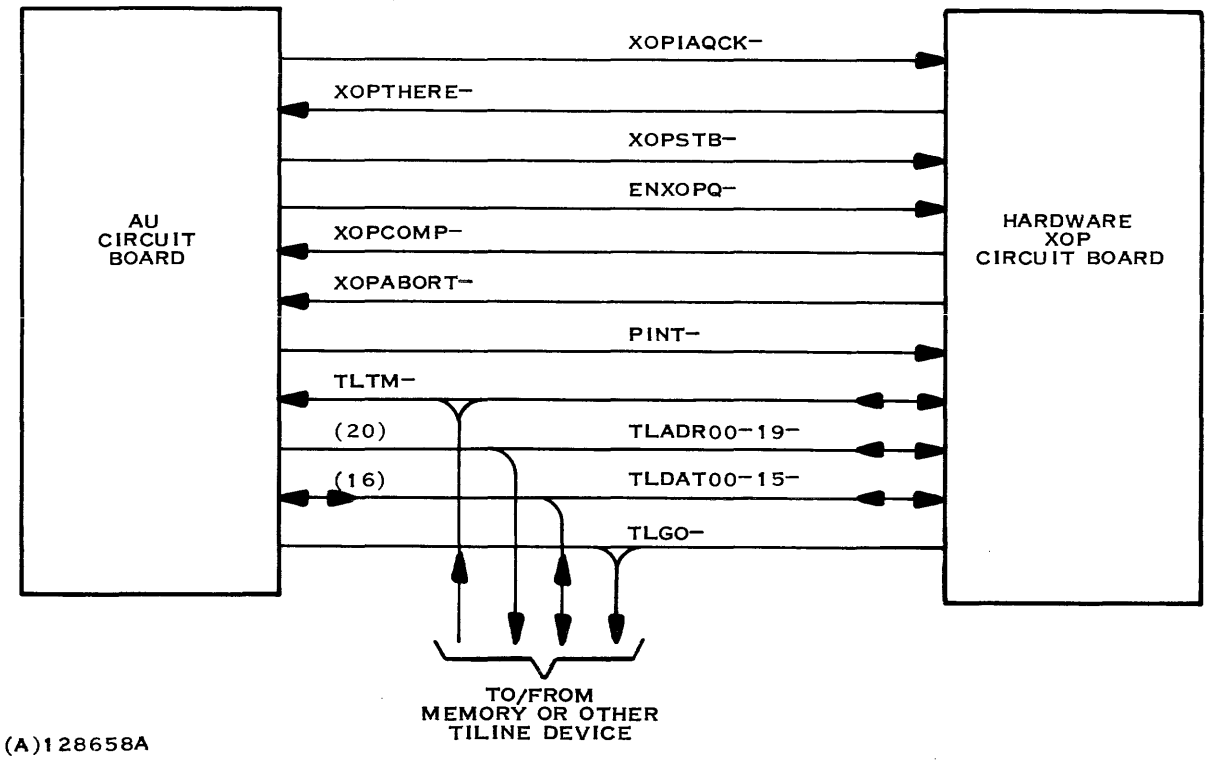


Figure 3-26. XOP Hardware Interface Signals

Operation Execution. When the AU has received TLTM– from the XOP module (or memory), it generates an enable signal to the module (ENXOPQ–) to initiate execution of the prescribed operation. This signal remains active until the module completes or terminates the operation. The hardware within the module must be able to function independently to fetch operands from memory, perform the required manipulations, and return the operands to memory in the location specified by the effective address stored in its address register. Operand size and length of operation are a function of the XOP module design.

Operation Completion. When the XOP module has completed its operation and stored the results in the specified memory location, it issues a signal to the AU to indicate that the operation has completed normally (XOPCOMP–), and places status information on the TILINE data line. When the AU has received the status information, it loads it into the status register for program monitoring, and responds to the XOP module by deactivating ENXOPO–. The XOP module then removes the XOPCOMP– indicator and status information from the interface lines. The extended operation is complete.

Operation Aborted. The XOP module may respond to an AU interrupt by terminating the extended operation before completion. The AU generates a pending interrupt signal (PINT–) when it receives an unmasked interrupt from one of the peripheral TILINE or CRU devices. Since the operation being performed in the XOP module may continue for a long time, the user may choose to checkpoint or terminate that operation so that the AU may service the interrupt. If the XOP module is designed to respond to a processor interrupt, it terminates or otherwise halts the operation in progress and returns XOPABORT- to the AU. Concurrent with the abort signal, the XOP module places its status information on the TILINE data bus for sampling by the AU. After the AU stores the status in the status register, it drops ENXOPQ- to the XOP

Table 3-8. XOP Hardware Interface Signals

Signature	Pin No.	Definition
XOPIAQCK–	P8-2	XOP Instruction Acquisition Clock: a 60 nanosecond low active pulse that enables the XOP circuit boards to capture the data currently on the TILINE data lines. That data is an instruction to be inspected by the XOP module.
XOPTHERE–	P8-3	XOP Hardware Present: a low active signal generated by the XOP module within 200 nanoseconds following XOPIAQCK–. This signal indicates to the AU that a hardware module is available to perform the indicated XOP function and that no software subroutine need be started. This signal must be present until acknowledged by XOPSTB–.
XOPSTB–	P8-9	XOP Strobe: a low active enable signal generated by the AU to the XOP board at least 500 nanoseconds following XOPIAQCK–. This signal indicates to the XOP module that the effective address has been calculated and is available on the TLADR lines.
ENXOPQ–	P8-4	Enable XOP: a low active signal generated by the AU to allow the XOP module to begin processing. The signal remains active during the entire process and is cleared when the AU receives status at the completion of the XOP.
XOPCOMP–	P8-5	XOP Complete: a low active signal that is issued by the XOP module to indicate that it has successfully completed the required operation. While this signal is active, the TLDAT lines contain status bits from the completion of the operation for transfer to the AU status register.
XOPABORT–	P8-7	XOP Aborted: a low active signal from the XOP module to indicate that the module will suspend the operation in progress so the processor may service a pending interrupt. While the signal is active, the TLDAT lines contain status bits from the module to indicate the condition at time of termination.
PINT–	P8-10	Pending Interrupt: a low active signal from the AU indicating that an active interrupt is pending.
TLTM–	P1-20	TILINE Terminate: a low active signal from any TILINE device or the XOP module to indicate the end of a particular data transfer. The XOP module uses TLTM– to indicate receipt of the effective address from the AU.
TLADR00– to TLADR19	See TILINE description	TILINE Address: a 20-bit address from the AU to the XOP module that designates the starting address of the data for the extended operation. This address is available to the XOP module when XOPSTB– is asserted. The module may store the address until completion of the routine or may assert TLGO– to fetch an operand at the address.
TLDAT00– to TLDAT15	See TILINE description	TILINE Data: bidirectional data lines that carry the XOP instruction to the XOP module, the XOP data and results between the XOP module and memory, and the status bits from the module to the AU.

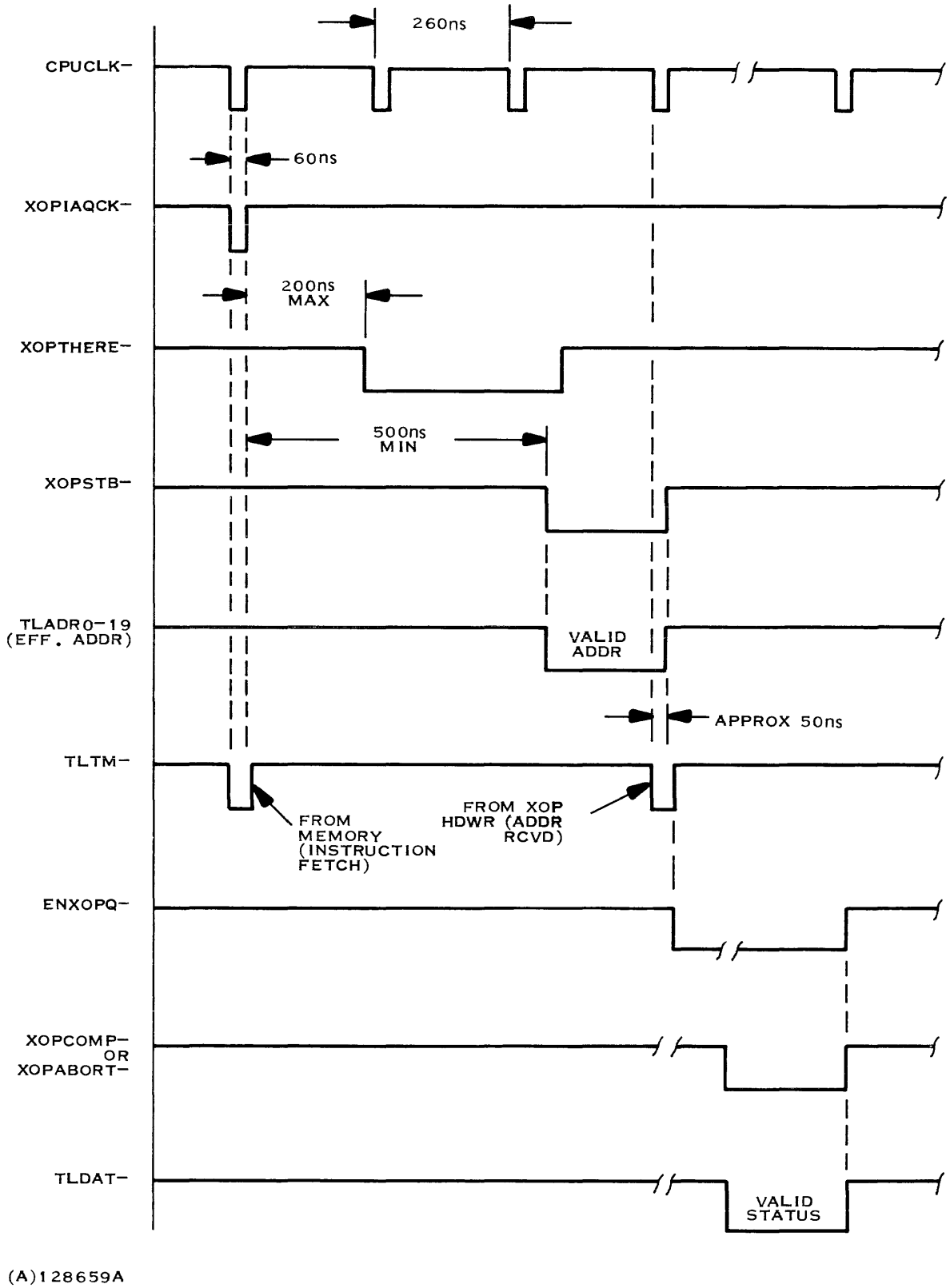


Figure 3-27. XOP Interface Timing Diagram

module to end the operation. If the extended operation is aborted, the AU does not increment the address in the program counter, so that when the AU returns from servicing the interrupt, it initiates the extended operation again.

3.2.7 **PROGRAMMER PANEL INTERFACE.** The programmer panel interface is comprised of TTL devices mounted on the 990/10 system interface board that serve as the interface between the processor on the AU1 circuit board and the programmer panel. Thirteen signal lines plus 5 volts main power and ground are brought to a 20-pin male connector at the top edge of the system interface board (AU2) at plug P7 where the interface to the programmer panel is completed through a 20-conductor ribbon cable. The interface signals are as shown in figure 3-28. The following description of each of the signals and how they are implemented is keyed to the simplified logic diagram of figure 3-29.

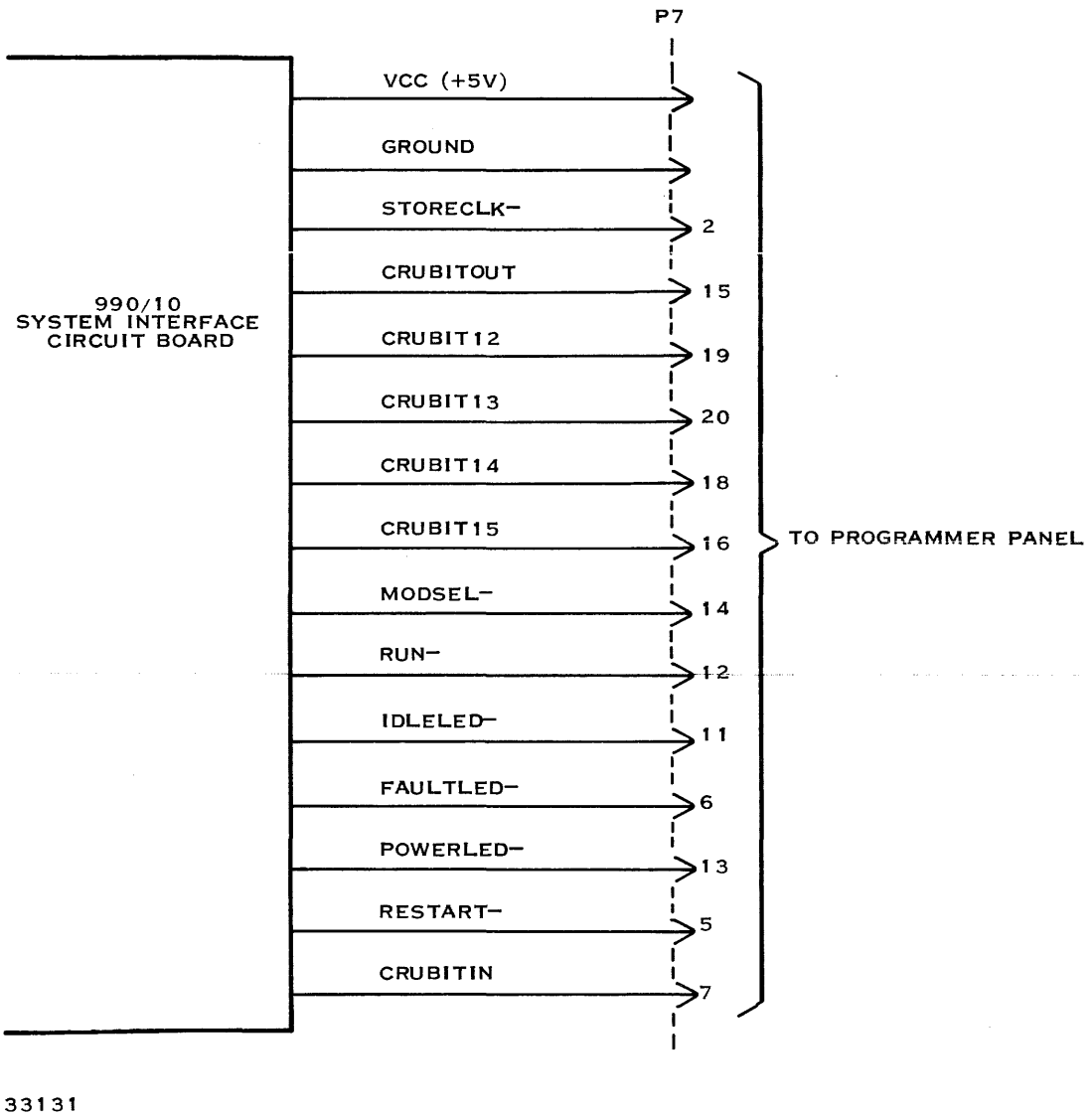


Figure 3-28. Programmer Panel Interface Signals

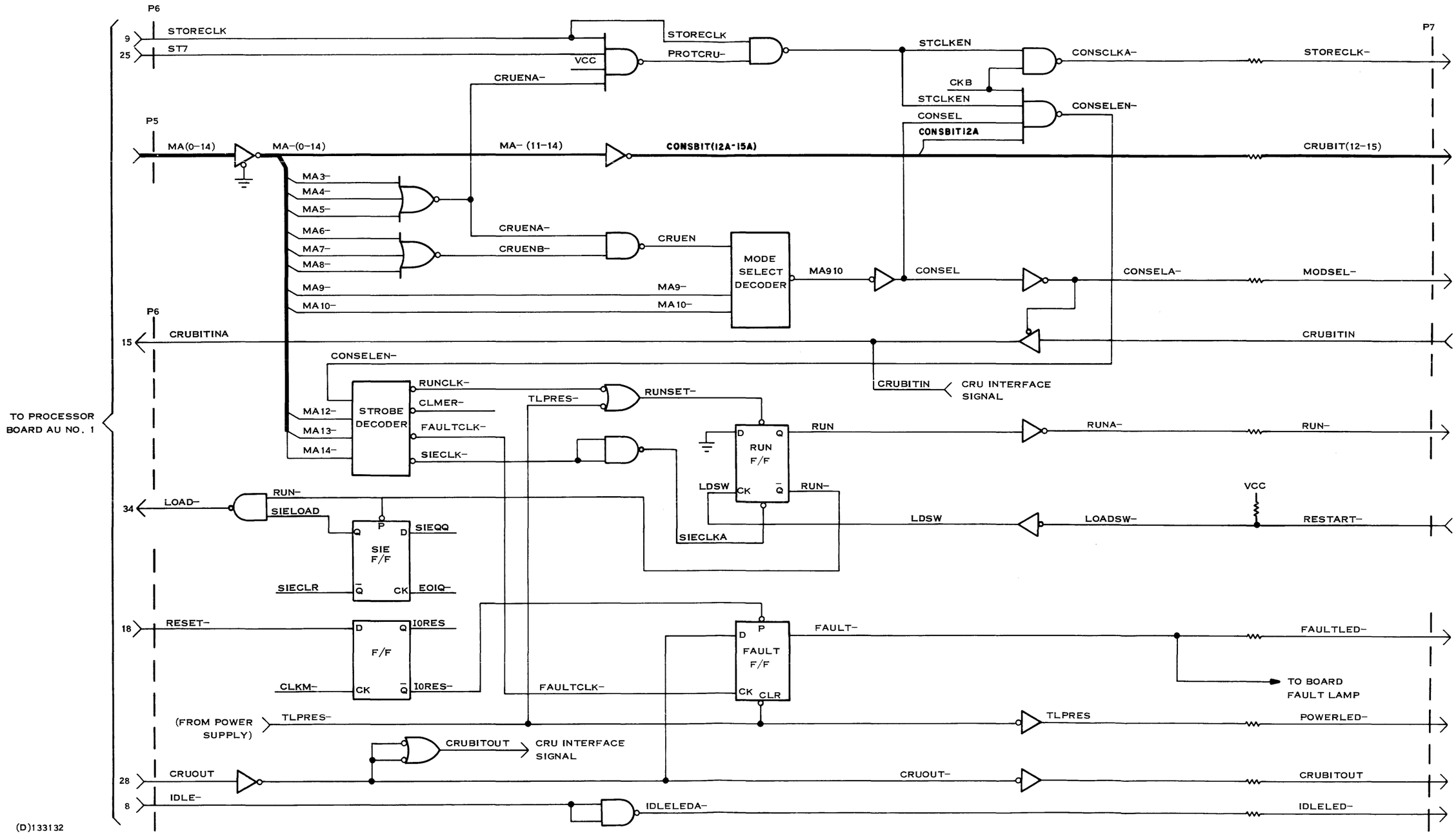


Figure 3-29. Simplified Logic Diagram of Programmer Panel Interface

3.2.7.1 **CRU Bit Select Bits.** The CRU bit select bits, CRU bits 12 through 15, are developed from bits of the processor address bus as follows. Address bus signals MAO through MA14 are brought into the system interface board at plug P5 and applied to bus drivers where signals MAO– through MA14– are generated at the inverted output of the drivers. CRU bits 12 through 15 are the CRU bit select field of the CRU 12-bit address word and as shown in figure 3-29 are developed from memory address bits MA11– through MA14–. During a read operation, the bit select field bits applied to the programmer panel select a particular bit for input to the processor whereas during a write operation the bits are used to generate control strobes in the programmer panel.

3.2.7.2 **STORECLK– Signal.** The STORECLK– signal is active when low to generate control strobe enable or write enable logic in the programmer panel. When a CRU device such as the programmer panel is being addressed by the processor, the STORECLK signal from the processor on the AU1 board goes high and is ANDed with a protect CRU (PROTCRU–) signal on the system interface board. If the processor is not in the privileged instruction mode and ST7 = 0, PROTCRU– is high to generate a high STCLKEN signal. When the central processor clock signal (CKB) that is ANDed with the STCLKEN goes high, the low STORECLK– output of the NAND gate is provided at the programmer panel interface.

3.2.7.3 **MODSEL– Signal.** A low MODSEL– signal at the programmer panel interface signifies to the programmer panel that it has been selected by the computer as the addressed module. Memory address bits MA3 through MA10 received from the central processor are all high when the programmer panel is the addressed module and as a consequence MA3– through MA10– are low. Low input signals MA3– through MA6– applied to two triple input positive NOR gates hold both CRUENA– and CRUENB– signals high. CRUENA– and CRUENB– applied to a NAND gate generate a low CRUEN enabling signal to the mode select decoder. With low MA9– and MA10– signals applied to the enabled decoder, a low MA910 signal is developed at the output of the decoder. The low MA910 is applied to one inverter to develop a high CONSEL signal and when inverted a second time develops the low CONSELA– signal. The low CONSELA– signal is applied through a resistor as the low MODSEL– signal at the programmer panel interface. Note that CONSEL is applied as an enabling input to a strobe decoder and that CONSELA– enables a three-state driver in the CRUBITIN serial data line.

3.2.7.4 **Serial Data Lines CRUBITOUT and CRUBITIN.** CRUOUT serial data from the central processor is applied through one inverter to produce a CRUOUT– signal and through a second inverter and resistor to the programmer panel interface as the CRUBITOUT signal that is sampled by the programmer panel when the STORECLK– input to the panel goes low. CRUBITIN serial input data from the programmer panel is applied to a three-state driver that is enabled by the low CONSELA– signal when the programmer panel is the addressed module. The output of the three-state driver is applied through a driver as the CRUBITINA input to the central processor.

3.2.7.5 **POWERLED– Signal.** A normally high TLPRES– signal supplied by the computer is applied to an inverter that is applied through a resistor to provide the normally low POWERLED– signal at the programmer panel interface. The low POWERLED– signal illuminates the POWER LED on the programmer panel to indicate that the system power supply is on.

3.2.7.6 **FAULTLED– Signal.** The FAULTLED– signal is a programmable low output signal generated by the central processor to illuminate the FAULT LED on the programmer panel to indicate the result of a processor test. A logic ONE on the central processor CRUOUT serial data line addressed to the programmer panel CRU output bit 11 lights the panel LED. As shown in figure 3-29, a logic ONE at CRUOUT develops a low CRUOUT- at the input to a flip-flop. This low is clocked out of the flip-flop as a low FAULT- signal by the FAULTCLK- strobe. The FAULTCLK- strobe is generated at the output of a strobe decoder when memory address bits MA11 through MA14 from the central processor are set to hexadecimal 11. The low MA11-address bit applied to an inverter develops a high CONSBIT12A signal that in turn is ANDed with the high SOTRECLK, CKB, and CONSEL signals when the programmer panel is the addressed module to generate a low CONSELEN- signal. CONSELEN- and inverted memory address bits MA12 through MA14 applied to the strobe decoder select the FAULTCLK- output of the strobe decoder. The low FAULT- signal that generates the low FAULTLED- signal at the programmer panel interface is also connected to a FAULT lamp on the 990/10 system interface board. Both FAULT lamps are illuminated following a power-up and are turned off by the user's software or by the self-test option. A set-bit-to-zero instruction addressed to programmer panel CRU output bit 11 or a RSET instruction extinquishes both lamps. A set-bit-to-one instruction can turn on the FAULT lights.

3.2.7.7 **RUN– Signal.** The RUN– signal is an active-when-low signal at the programmer panel interface that is generated by the computer while in the RUN mode. The low illuminates the RUN LED on the programmer panel. As shown in figure 3-29, either a low TLPRES– or a low RUNCLK– signal sets a flip-flop to provide a high RUN signal that is inverted and applied at the programmer panel interface through a series resistor as the RUN– signal. Since TLPRES– is initially low during a power-up, the RUN– signal is always generated when power is applied. The low RUNCLK– signal is programmable and is generated with an SBO instruction addressed to CRU output bit 10 of the programmer panel. As long as RUN is held high, the LOAD– signal (generated from RESTART or SIE) to the central processor is inhibited by the Q– output of the RUN flip-flop.

3.2.7.8 **RESTART– Signal.** RESTART– is a low signal generated at the programmer panel interface by pressing the HALT/SIE switch on the programmer panel when the front panel key switch is in the UNLOCK position. On the system interface board, RESTART– is inverted and applied to the clock of the RUN flip-flop and the Q output of the flip-flop goes low. The RUN– signal at the programmer panel interface goes high and the programmer panel moves into its active (HALT) mode of operation.

As the Q– output of the RUN flip-flop goes high in response to the RESTART– signal, the Q– output ANDed with the high SIELOAD signal causes a low LOAD– signal to be generated. The low LOAD– signal applied to the processor causes a trap to memory address $FFFC_{16}$. The low SIECLR output at the Q– output of the SIE flip-flop clears a flip-flop that permits a low SIEQQ to be clocked into the SIE flip-flop by the end-of-instruction signal EOIQ– and as SIELOAD goes low the LOAD– signal returns high. The RUNLED– signal to the panel is supplied through a series resistor to light the RUN indicator.

3.2.7.9 **IDLELED– Signal.** A low IDLELED– signal at the programmer panel interface illuminates the IDLE LED on the panel as an indication of processor inactivity. When the processor executes an IDLE instruction it causes a low IDLE– signal to be applied to the system interface board AU2. On the system interface board, IDLE– applied to a driver generates a low IDLELED– signal that is applied to the programmer panel interface through a series resistor. The low IDLE– signal from the processor changes state when program execution resumes due to an interrupt, load, or reset.

3.2.8 **COMMUNICATIONS REGISTER UNIT (CRU) INTERFACE.** The direct command driven input/output interface for the processor is called the CRU. The CRU provides for up to 4096 directly addressable input bits and up to 4096 directly addressable output bits, Input and output operations can address each of the bits individually or in fields of from one to sixteen bits. The processor instructions that drive the CRU can set, reset, or test any bit in the CRU array, or the microprocessor instructions can move data between memory and the CRU data fields.

Logic for the CRU is mounted on the system interface circuit board and this logic exerts control over the interface data and control lines. These lines are available to all main chassis locations except for the two slot locations used by the processor board AU1 and the system interface board itself. Twenty four module select signals are decoded by CRU interface logic and are made available to 11 chassis locations when the 13-slot chassis is used. Only eight of the module select signals are used for the four available chassis locations used in the 6-slot chassis. Each chassis location (full-sized slot) accomodates one double-connector circuit board or two single-connector circuit boards.

3.2.8.1 **Main Chassis Implementation.** The minimum CRU implementation can be effected by installing an AU1 and an AU2 circuit board into a 990 family chassis/power supply assembly. This combination is defined as a main chassis and can be implemented with either a 177.04-millimetre (6.97-inch) chassis that has a maximum of four available full-sized slots or with a 310.39-millimetre (12.22-inch) chassis that has a maximum of 11 available full-sized slots. Each full-sized slot has the capability to implement a maximum of 32 input/output bits using the module select decodes provided. Main chassis CRU addresses begin at 000_{16} and extend to a maximum of $09F_{16}$ for the 177.04-millimetre (6.97-inch) chassis and to a maximum of $17F_{16}$ for the 310.39-millimetre (12.22-inch) chassis. If the main chassis contains a memory circuit board, the number of available full-sized CRU chassis slots is reduced accordingly.

3.2.8.2 **Standard CRU Expansion Implementation.** If a computer system requires more CRU slots than are available in the main chassis, then from one to seven 13-slot CRU expansion chassis can be added. A CRU address map for the standard expansion implementation is shown in figure 3-30. The hardware required for the standard CRU expansion implementation is as shown in figure 3-31. One 26-conductor ribbon cable is required to connect each expansion chassis. The chassis and backpanels used in the expander chassis are identical to those used for the 12-inch main chassis. The expander board installed in the main chassis contains line drivers and receivers for the expansion cables. The buffer board installed in each expansion chassis decodes module select signals, contains buffers and receivers for the CRU address and data, and additionally generates clock signals for the expander chassis cards. The buffer board also implements an interrupt scanner for up to 32 interrupts per expansion chassis. Software can use the interrupt scanner to construct vectored interrupts for each slot of the expander chassis and eliminate the need to poll devices to determine the source of the interrupt.

3.2.8.3 **CRU Applications.** Because of its extremely flexible data format, the CRU interface can be used effectively for a wide range of control and data operations. These applications can be divided into two broad categories: those involving a single control bit transfer, and those requiring input or output of a word of several data or status bits.

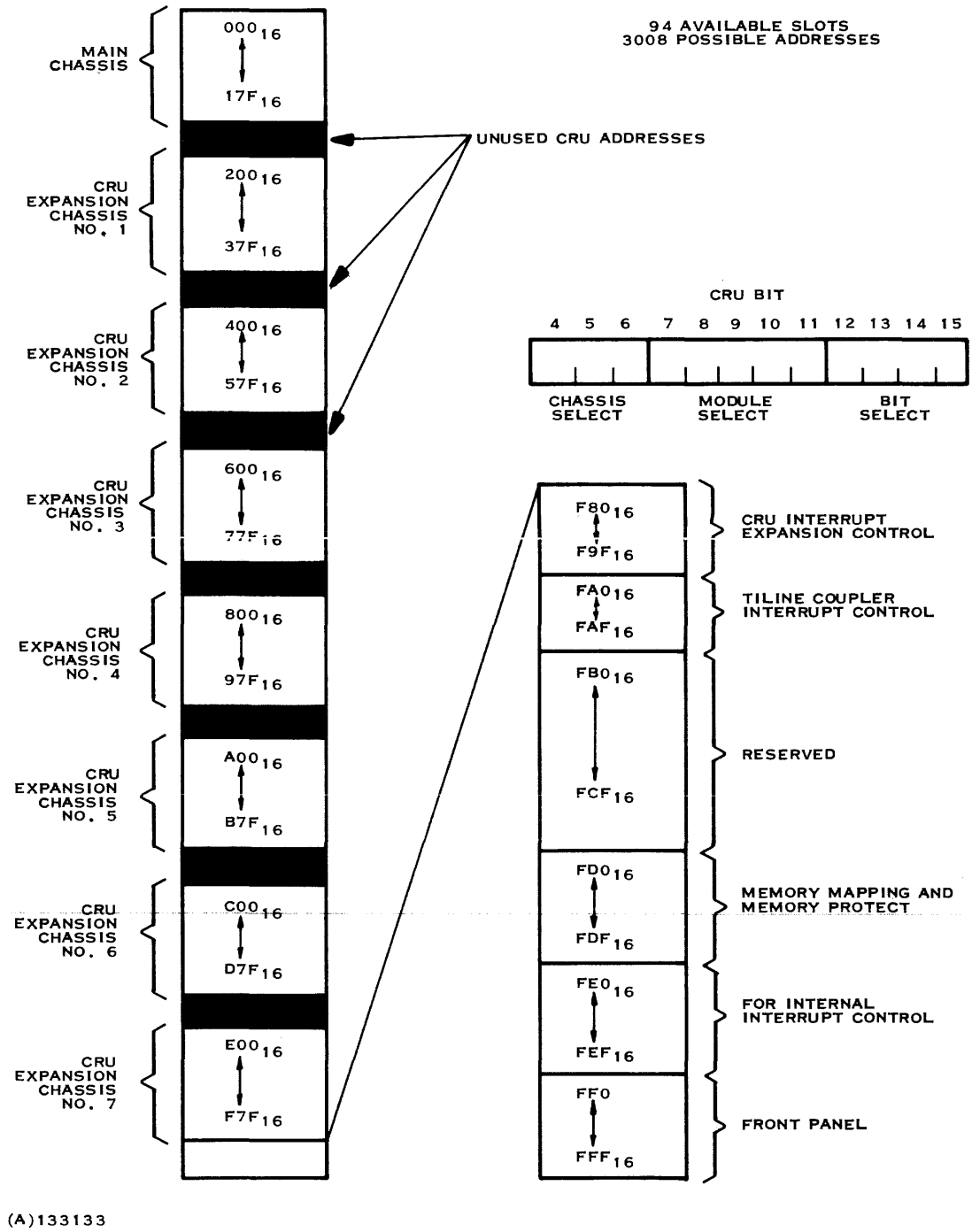


Figure 3-30. CRU Address Map for Standard Expansion Implementation Using 13-slot Chassis

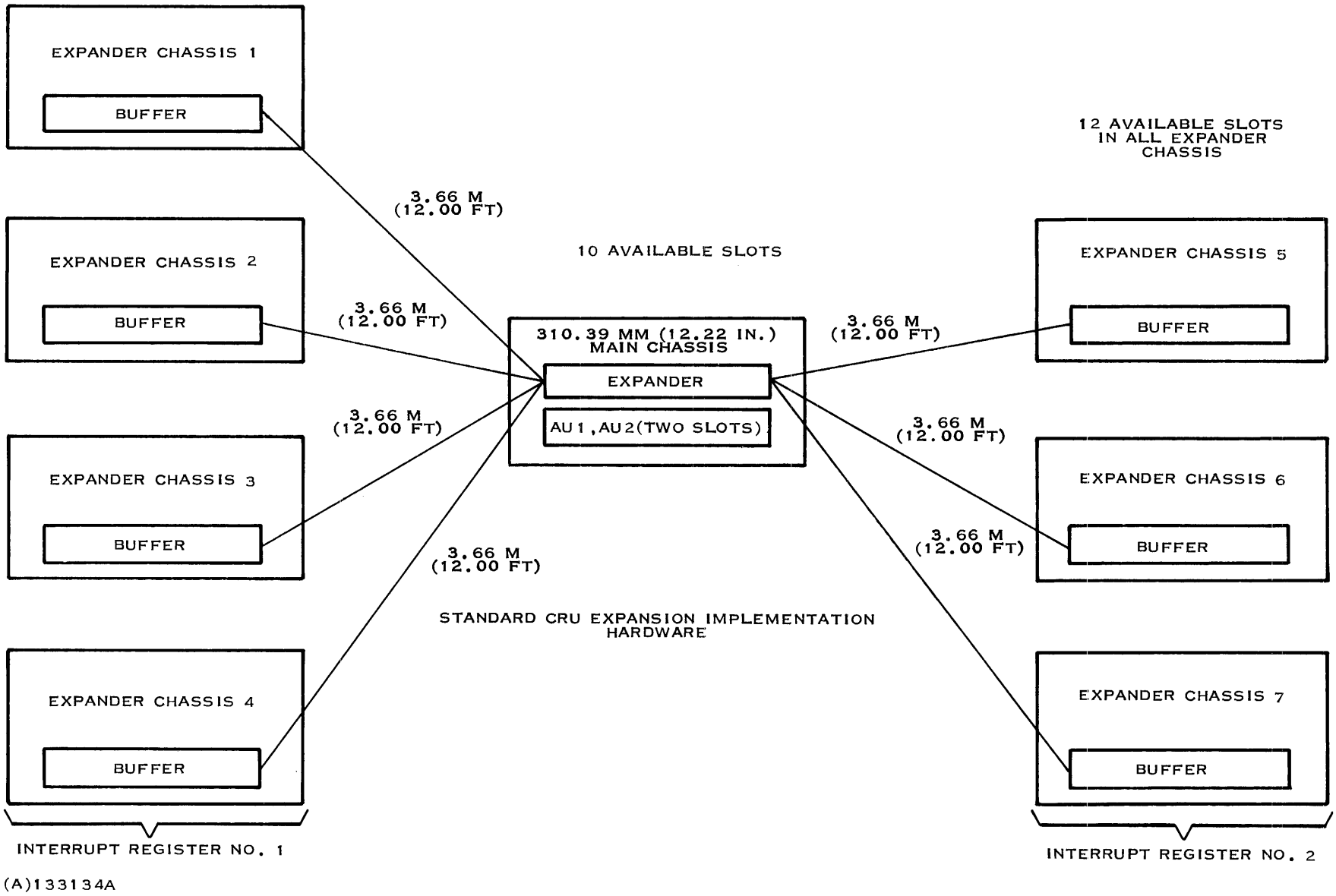


Figure 3-31. Standard CRU Expansion Implementation Hardware

Single-Bit Operations. Single-bit operations typically involve the computer sampling a status bit. When the status bit sets, the computer responds by setting a control bit or by transferring to a different set of instructions. This operation is exemplified by a communications interface unit that generates a single interrupt for one of several reasons such as output complete, input complete, or line status change. An output or input complete requires a transfer to instructions that perform another output or input operation. A line status change might require the setting of a control output or the transfer to instructions that handle the change in other ways.

Multiple-Bit Operations. Multiple-bit operations typically involve a data input device such as a keyboard or card reader, or an output device such as a display or card punch. An interrupt from the device causes the microprocessor to perform a store communications register (STCR) instruction to read data from the CRU device and store it into memory. Similarly, to output data to the device the processor executes a load communications register (LDCR) instruction to fetch data from memory and transfer it to the CRU device.

3.2.8.4 **CRU Interface Signals.** Logic on the system interface board implements a dedicated CRU interface for the programmer panel as was described in paragraph 3.2.7 and also the standard CRU interface for the main chassis. The interface signals to the main chassis are effected at the bottom edge connectors, P1 and P2, of the system interface board. A simplified logic diagram of the CRU interface that shows the interface signals to the main chassis is provided in figure 3-32. Table 3-9 provides the function of each of the CRU interface signals, the pin numbers of the signals on the system interface board that installs in main chassis slot designated slot 1, and the pin numbers of the signals as they appear on the backpanel chassis slots of either the main chassis or an expansion chassis. These chassis slots are designated slots 2 through 6 for a 6-slot chassis and 2 through 13 for a 13-slot chassis. Both connectors in each chassis slot are furnished with the CRU bit select bits (CRUBIT 12-15) and other CRU interface signals that permit each connector to address 16 bits of the CRU. Connector P1 in a chassis slot receives one module select signal corresponding to one 16-bit register whereas connector P2 receives two module select signals and thus may address up to 32 bits of the CRU. Connector P1 also receives the eight most significant bits of the CRU address thus permitting the chassis slot to be used for a CRU expansion driver or for modules that ignore module select signals to directly decode their own CRU address.

3.2.8.5 **CRU Power Supply Requirements.** The chassis power supply provides three regulated voltages for use of the CRU, provides power status signals to the CRU, provides signal isolation from the power line or earth ground, and provides ground fault protection for logic signals.

Chassis Power Supply CRU Interface Signals. The chassis power supply interface signals that are implemented in the chassis/power supply assembly are described in table 3-9 along with the pin numbers of the signals at the system interface board and also at the chassis backpanel. The description that follows is a description of the signals in greater depth than that provided in the table.

The chassis power supply generates a low Power Fail Warning Pulse (TLPFWP–) to warn of imminent power supply failure. The TLPFWP– pulse connects to the system interface board and to all CRU connectors. TLPFWP– has a duration of at least 7.0 milliseconds. Figure 3-33 shows the timing relationship between signals furnished by the power supply and main voltages of the power supply.

The chassis power supply generates a Power Reset (TLPRES–) to indicate that power supply voltages are unstable. The TLPRES- signal is connected to the system interface board and to all the CRU connectors. TLPRES- is low true.

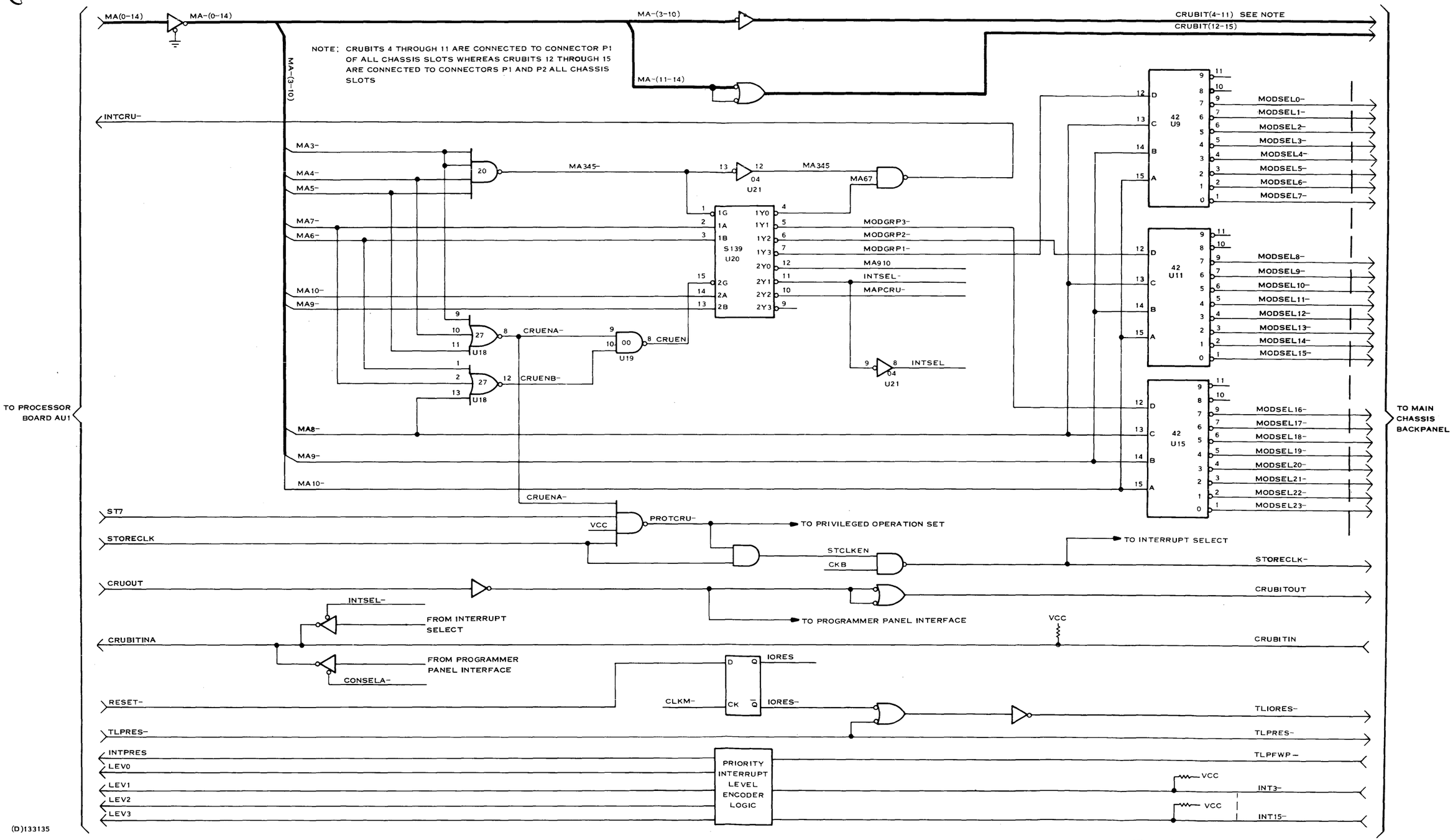


Figure 3-32. Simplified Logic Diagram of CRU Interface Implementation

Table 3-9. CRU Interface Signals

Signature	System Interface Board Pin Number	Main or Expansion Chassis Backpanel Pin Number	Function
CRUBIT4	P1-56	P1-56	Address bits generated by the microprocessor to select a particular chassis (bits 4-6), a 16-bit module within that chassis (bits 7-11), and a particular bit from that module (bits 12-15). CRUBITS 4-11 are capable of driving at least 12 normalized TTL loads, CRUBITS 12-15 are capable of driving 30 normalized TTL loads.
CRUBIT5	P1-54	P1-54	
CRUBIT6	P1-52	P1-52	
CRUBIT7	P1-50	P1-50	
CRUBIT8	P1-62	P1-62	
CRUBIT9	P1-64	P1-64	
CRUBIT10	P1-68	P1-68	
CRUBIT11	P1-70	P1-70	
CRUBIT12	P1-36	P1-36, P2-36	
CRUBIT13	P1-32	P1-32, P2-32	
CRUBIT14	P1-38	P1-38, P2-38	
CRUBIT15	P1-34	P1-34, P2-34	
CRUBITOUT	P1-18	P1-18, P2-18	Serial data line for transfer of data from the processor to the addressed CRU bit(s). This line is active only when STORECLK- goes low. (This line will drive 30 normalized TTL loads.)
CRUBITIN	P1-60	P1-60, P2-60	Serial data line for transfer of data from the addressed CRU bit(s) to the processor. This line must be driven by an open collector gate and only when the module is selected. A 470-ohm pull-up resistor is mounted on the AU2 circuit board for this line.
STORECLK-	P1-22	P1-22, P2-22	An active-when-low pulse that indicates to the selected CRU module that the operation is a write (Set Bit or LDCR) operation. This pulse transfers the data on the CRUBITOUT line into a holding flip-flop that is the CRU bit. (Will drive 30 TTL loads.)
TLIORES-	P1-14	P1-14, P2-14	I/O Reset: A normally high signal that, when low, resets all connected devices. This signal is a minimum 250 nanoseconds pulse that is generated by a RSET instruction in the processor. This signal is also low until dc power is up and stable. (Will drive 30 TTL loads.) loads.)
TLPFWP-	P1-16	P1-16, P2-16	Power Failure Warning Pulse: A low signal of at least 7.0 milliseconds duration that indicates that a power failure is imminent. (Will drive 30 TTL loads.)

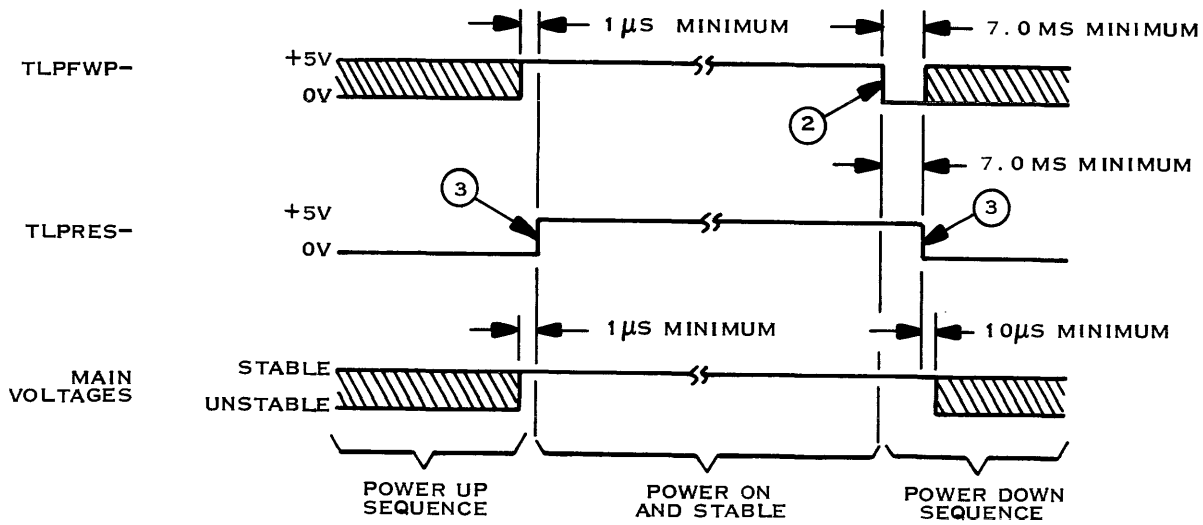
Table 3-9. CRU Interface Signals (Continued)

Signature	System Interface Board Pin Number	Main or Expansion Chassis Backpanel Pin Number	Function
TLPRES-	P1-13	P1-13, P2-13	Power Reset: A normally high signal that goes low to reset connected devices at least 10 microseconds before dc voltages begin to fail during power-down. During power-up, this signal is low until all voltages are stable. This line will drive 60 TTL loads (20 ampere power supply) and 120 TTL loads (40 ampere power supply).
MODSEL0-	P1-23	Slot 13, P2-48	Module select signals generated by the processor from address bits 6-10 (CRUBITS 7-11) for use within the main or an expansion chassis. Note that P1 in each slot of the backpanel receives one module select signal whereas P2 receives two module select signals. This configuration permits P2 to use 32 bits of the CRU. Note that pin 48 of successive P2 connectors in the chassis slots are connected to even-numbered module select signals and at the CRU circuit board level carries a MODSELA- signature. Pin 46 of successive P2 connectors in the chassis slots are connected to pin 48 of P1 of that slot and then to an odd-numbered module select signal and carries a signature of MODSELB-. Pin P1-48 is not used when a full-sized CRU circuit board is implemented in a chassis slot. MODSEL signal lines will drive 10 TTL loads.
MODSEL1-	P1-35	Slot 13, P1-48 and P2-46	
MODSEL2-	P1-37	Slot 12, P2-48	
MODSEL3-	P1-43	Slot 13, P1-48 and P2-46	
MODSEL4-	P1-44	Slot 11, P2-48	
MODSEL5-	P1-45	Slot 11, P1-48 and P2-46	
MODSEL6-	P1-46	Slot 10, P2-48	
MODSEL7-	P1-47	Slot 10, P1-48 and P2-46	
MODSEL8-	P1-48	Slot 9, P2-48	
MODSEL9-	P1-49	Slot 9, P1-48 and P2-46	
MODSEL10-	P1-51	Slot 8, P2-48	
MODSEL11-	P1-53	Slot 8, P1-48 and P2-46	
MODSEL12-	P1-61	Slot 7, P2-48	
MODSEL13-	P1-67	Slot 7, P1-48 and P2-46	
MODSEL14-	P1-69	Slot 6, P2-48	
MODSEL15-	P1-71	Slot 6, P1-48 and P2-46	
MODSEL16-	P2-38	Slot 5, P2-48	
MODSEL17-	P2-36	Slot 5, P1-48 and P2-46	
MODSEL18-	P2-34	Slot 4, P2-48	
MODSEL19-	P2-32	Slot 4, P1-46 and P2-46	
MODSEL20-	P2-22	Slot 3, P2-48	
MODSEL21-	P2-18	Slot 3, P1-48 and P2-46	
MODSEL22-	P2-16	Slot 2, P2-48	
MODSEL23-	P2-13	Slot 2, P1-48 and P2-46	

Table 3-9. CRU Interface Signals (Continued)

Signature	System Interface Board Pin Number	Main or Expansion Chassis Backpanel Pin Number	Function
INT1-*	P1-65		Each side of each full-sized chassis slot is furnished a pin (P1-66 and P2-66) through which a CRU circuit board may interrupt the processor. These pins are connected to interrupt levels by jumpers in accordance with assigned priorities.
INT2-*	P1-66		
INT3-	P2-24		
INT4-	P2-46		
INT5-	P2-48		
INT6-	P2-50		
INT7-	P2-52		
INT8-	P2-54		
INT9-	P2-56		
INT10-	P2-58		
INT11-	P2-62		
INT12-	P2-64		
INT13-	P2-65		
INT14-	P2-66		
INT15-	P2-67		

*INT1 and INT2 are sometimes implemented on the processor board and are not available for CRU use.



NOTES:
1. SHADED AREAS INDICATE UNDEFINED VOLTAGES.
2. THE FALL TIME OF TLPFWP- SHALL NOT EXCEED 50NS.
3. THE RISE AND FALL TIME OF TLPRES- SHALL NOT EXCEED 100NS. THERE SHALL BE NO OSCILLATIONS ON EITHER EDGE OF TLPRES-.

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Figure 3-33. Chassis Power Supply Timing

The chassis power supply furnishes three separate supply voltages to all connectors on the chassis backpanel; +5 MAIN, +12 MAIN, and -12 MAIN. The + 5 MAIN supply is +5±.15 volts referenced to logic ground and has the capacity for 20 amperes if mounted in a 6-slot chassis and 40 amperes if mounted in a 13-slot chassis. Note that to determine the power available to CRU devices the current drain of the AU1 board and the AU2 board must be subtracted from the above currents. The +12 MAIN supply is +12±.36 volts referenced to logic ground and has the capacity for 2 amperes in the 6-slot chassis and for 4 amperes if mounted in the 13-slot chassis. The -12 MAIN supply is -12±.72 volts referenced to logic ground and has the capacity for 1 ampere in the 6-slot chassis and for 2 amperes when mounted in the 13-slot chassis. All power supply voltages and logic levels are referenced to logic ground. Additionally, the backpanel in the chassis contains a logic ground plane on the connector side of the backpanel to minimize crosstalk and noise problems for CRU signals. Logic ground is electrically isolated from chassis or earth ground to minimize ground loop problems when two chassis of slightly different earth ground potentials must interconnect. Fault protection capacitors between earth and logic ground are provided to perform two functions. First, the capacitors bleed off high frequency noise on logic ground that would interfere with the operation of high frequency analog devices such as CRT displays and second, the capacitors provide protection for the user when voltages greater than 30 volts dc or 15 volts ac exist between earth and logic ground as the fault protection capacitors will short to trip the users circuit breaker to prevent a potential shock hazard. Earth ground is supplied from the ground prong on the chassis power cord. Earth ground is connected to all exposed metal parts of the chassis but is not made available to any CRU circuit board.

3.2.8.6 **CRU Circuit Board Mechanical Requirements.** The chassis/power supply assembly is able to accept CRU (or other) circuit boards with the dimensions specified in figure 3-34 without clearance problems. Maximum power load for each full-sized slot is 50 watts.

3.2.8.7 **CRU Addressing.** The processor issues a 12-bit address (CRUBIT4 through CRUBIT15) to address up to 4096 individual bits. The 12-bit address is used for both input and output operations. Figure 3-35 illustrates the field assignments for the 12-bit CRU address. The four least significant bits, CRUBIT12 through CRUBIT15, select one of sixteen possible bits from a particular module select. The next five bits, CRUBIT 7 through CRUBIT 11, have the capability of generating 32 module select signals but only 24 module select signals are implemented on the system interface circuit board since this is the maximum number of CRU modules that can be installed in the 13-slot chassis. The three most significant bits identify the chassis containing the addressed module. Chasis 0 is by definition the main chassis. All CRU address bus signals are high true.

3.2.8.8 **Processor CRU Output Timing.** The processor conforms to minimum CRU output timing restrictions as defined by figure 3-36. The figure shows the timing sequence for a LCDR R1, 2 instruction followed by a SBZ 15 instruction. Minimum timing restrictions are the same for both instructions. CRU addresses and module selects are defined only during the execution of CRU output or CRU input instructions. CRUBITOUT and STORECLK- are held high when the processor is not executing a CRU output instruction. The CRU device clocks the CRUBITOUT line using the positive edge of the STORECLK- pulse.

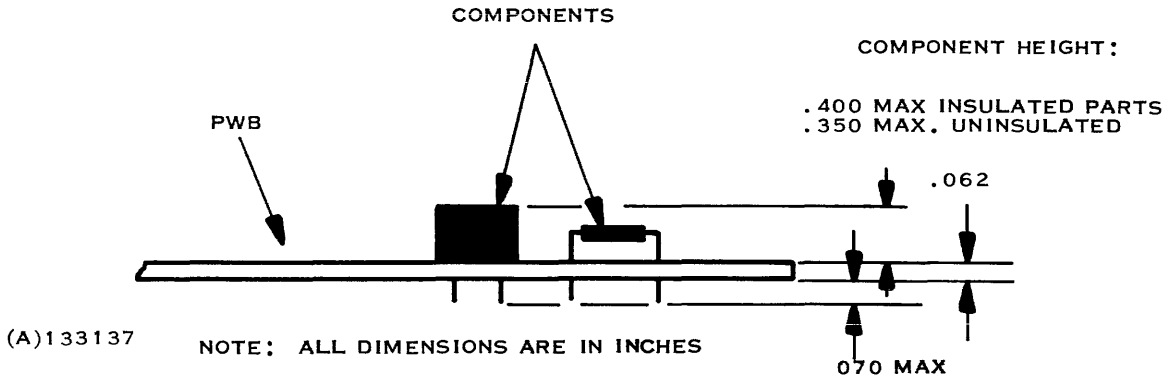

Figure 3-34. 990/10 Circuit Board Dimension Requirement

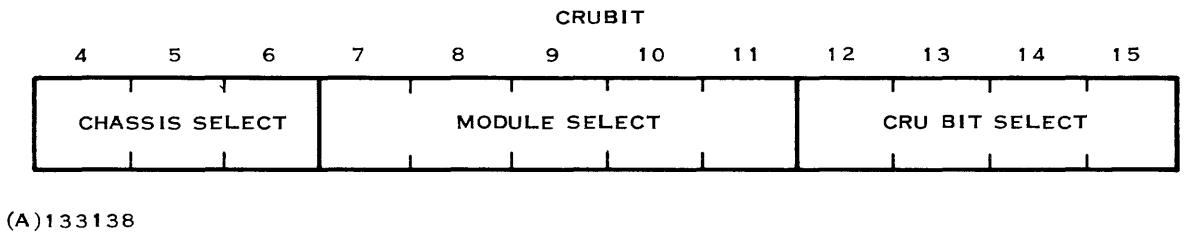

Figure 3-35. CRU Address Field Assignments

3.2.8.9 **Processor CRU Input Timing.** The processor conforms to minimum CRU input timing restrictions as defined by figure 3-37 for CRU addresses 000_{16} to $17F_{16}$ and to the same minimum CRU input timing restructions for CRU addresses from 200_{16} to FFF_{16} even though the delay between when the processor presents the CRU address and when the processor samples CRU data is increased by 250 nanoseconds for CRU expansion addresses, 200_{16} to FFF_{16} to allow for propagation delay through the interconnecting cables. The figures show the timing sequences for STCR R1, 2 instruction followed by an SBZ 15 instruction. Minimum timing restrictions are the same for both instructions. CRU addresses and module selects are defined only during the execution of CRU input or CRU output instructions. CRUBITIN is defined only during the execution of a CRU input instruction. The CRU device decodes the CRU address and places the appropriate data on the CRUBITIN line. The CRU module drives the CRUBITIN line with an open collector or three-state gate that is enabled only when that module is selected. Timing restrictions shown in figure 3-37 are based on a clock period of 250 nanoseconds.

3.2.8.10 **CRU Circuit Board Requirements.** Texas Instruments offers CRU interface modules that plug into CRU slots to act as the interface between the minicomputer and external devices. The 16 I/O EIA Data Module, TI part number 945140-0001 provides a general purpose 16-bit input and output interface between the minicomputer and any external device that requires EIA voltage levels at the interface. The 16 I/O TTL Data Module with Interrupt Option, TI part number 945145-0001, provides a two-way communication path between the minicomputer and devices which are operated by or generate discrete signals. Sixteen input and sixteen output lines are provided with each line capable of being manipulated as a single independent line or as a member of a group of lines. For the customer that has special requirements and wishes to implement a special CRU circuit board, the following information is provided.

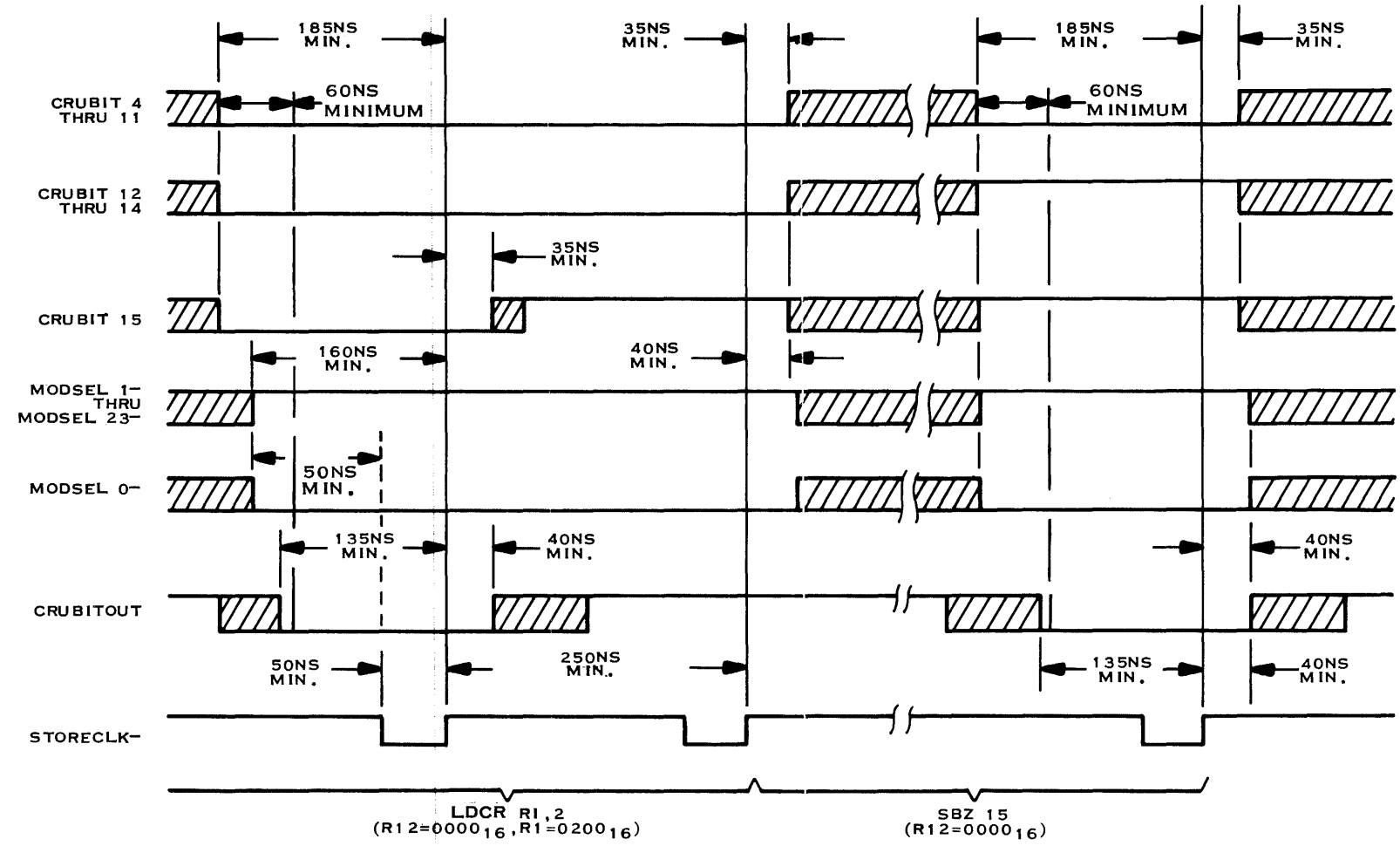

Figure 3-36. CRU Output Timing, Minimum Restrictions

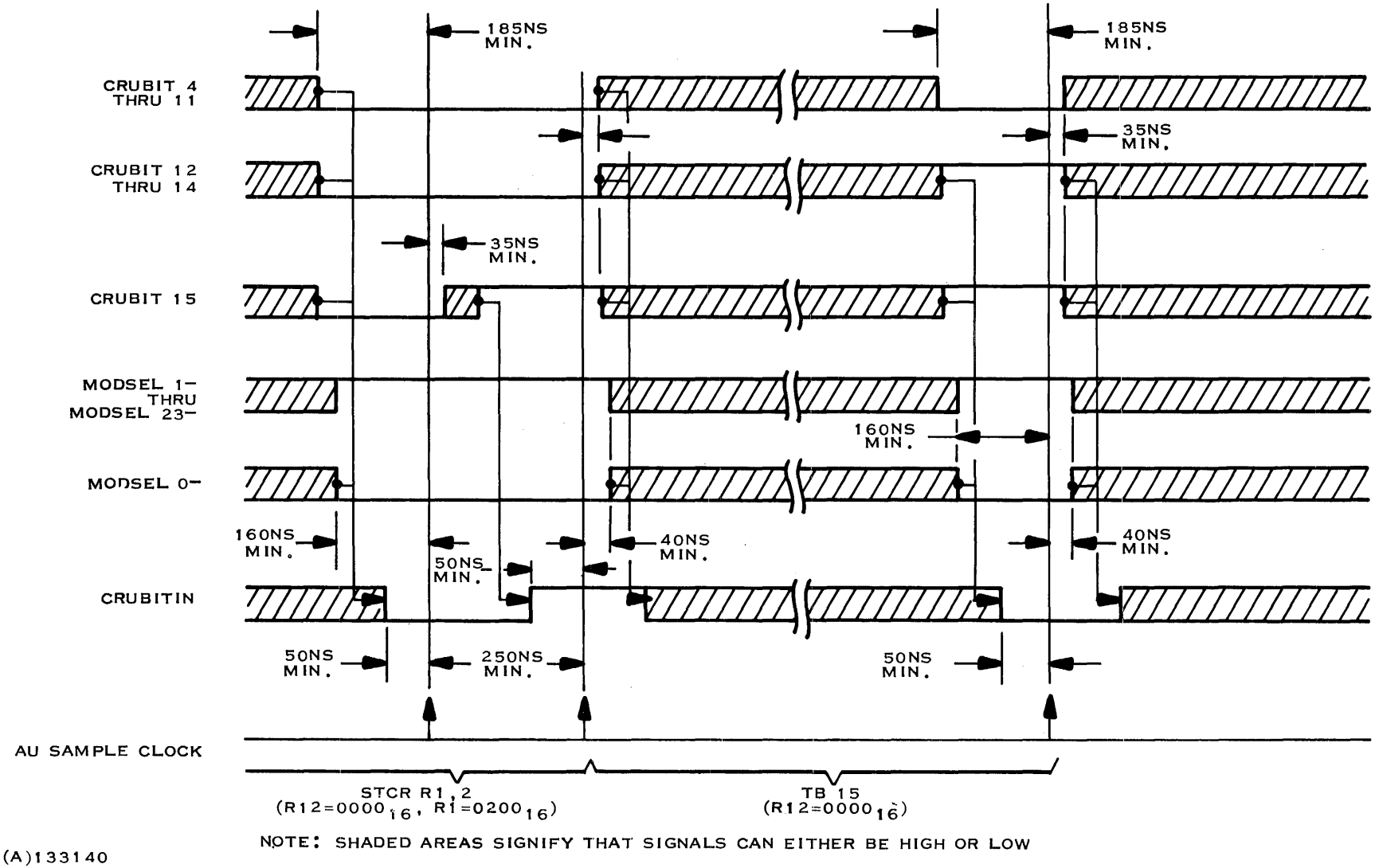

Figure 3-37. CRU Input Timing, Minimum Restrictions

CRU circuit boards may be implemented as either full-sized or half-sized circuit boards. Full-sized boards may implement a maximum number of two interrupt vectors and 32 input/output bits along with two module select signals. Half-sized boards may implement one interrupt vector and as many as 32 input/output bits (16 for P1 connectors). A CRU circuit board may be implemented as a standalone peripheral such as an interval timer or may be part of a peripheral kit such as a CRT controller. As part of a peripheral kit, the CRU circuit board interconnects to the CRU peripheral device using a cable.

All CRU signals with the exception of interrupts and module select signals are implemented on the same pins of both connectors P1 and P2 of the chassis backpanel so that the half-sized CRU circuit boards may be installed in either side of a chassis slot. Table 3-10 shows the pin number of these interface signals and figure 3-38 is a logic diagram of a 16 I/O TTL data module that is provided as an example of a CRU interface module. The data module inputs and outputs are negative logic levels that switch between zero and some positive voltage level. Each output is an open-collector transistor capable of sinking up to 50 milliamperes at up to 30 volts. Pads are available on the module for installing pull-up resistors or resistor divider networks at each input of the module. Pads for input filter capacitors are also available on the module.

Interrupts. Each side of a chassis slot is provided with a pin through which a CRU circuit board may interrupt the processor. Full-sized boards have two interrupts available. Jumper wires on the backpanel are used to assign interrupt priority levels.

When the CRU circuit board requests an interrupt, the interrupt pin should be driven low with an open-collector TTL gate on the CRU circuit board. This signal should be held low until the processor, using a CRU output operation, clears the interrupt. This signal should be forced clear by TLIORES- and should always be high or floating after a power-up.

Module Select A- (MODSELA-). MODSELA- is the primary or lowest address module select of a full-sized chassis slot and is the only module select available on connector P1. MODSELA-, depending on the CRU circuit board's location in the chassis, is connected to one of the module selects generated by the system interface circuit board by way of the chassis backpanel. MODSELA- is low true and CRU circuit board loading should not exceed 5 normalized TTL loads.

Module Select B- (MODSELB-). MODSELB is the secondary or highest address module select of a full-sized chassis slot. MODSELB- is not implemented on connector P1. MODSELB- on connector P2 is the same signal as MODSELA- on connector P1. This is done so that two half-sized CRU circuit boards can be installed into one full-sized slot. Other characteristics and requirements for the MODSELB- signal are the same as those for the MODSELA- signal.

CRU Address Bits 12 Through 15 (CRUBIT 12-15). The function of CRU bits 12 through 15 is the same as that described in table 3-9. Each signal should be high true and CRU circuit board loading should not exceed one normalized TTL load per connector.

CRUBITOUT. The function of CRUBITOUT is as described in table 3-9. CRUBITOUT should be high true and CRU circuit board loading should not exceed one normalized TTL load per connector.

Store Clock (STORECLK-). The function of STORECLK- is as described in table 3-9. CRU circuit boards should use the positive edge of STORECLK- to clock CRU data into edge-triggered or master-slave flip-flops. STORECLK- may be combined with a CRU address to set or reset a latch. CRU addresses and module selects are valid only during CRU operations and therefore they cannot be used reliably to perform output operations without STORECLK-. CRU circuit board loading on STORECLK- should not exceed one normalized TTL load per connector.

Table 3-10. CRU Circuit Board Signals

Signature	Connector	Pin Number
INTP2A– (INTA–**)	P2	66
INTP1A– (INTA–**)	P1	66
MODSELA–	P2 (wired to an even-numbered MODSEL)	48
	P1 (wired to an odd-numbered MODSEL)	48*
MODSELB–	P2 (wired to the same MODSEL as P1-48)	46
CRUBIT12	P2, P1	36
CRUBIT13	P2, P1	32
CRUBIT14	P2, P1	38
CRUBIT15	P2, P1	34
CRUBITOUT	P1, P2	18
STORECLOCK–	P2, P1	22
CRUBITIN	P2, P1	60
TLIORES–	P2, P1	14
TLPFWP–	P2, P1	16
TLPRES–	P2, P1	13

** Half sized circuit board signature

* This signal should not be used when implementing a full sized CRU circuit board.

CRUBITIN. The function of CRUBITIN is as described in table 3-9. CRUBITIN is high true and should be driven by either an open collector or three-state gate on the CRU circuit board. CRUBITIN should be allowed to go low only when the CRU circuit board has been addressed by a module select signal.

TILINE I/O Reset (TLIORES-). The function of TLIORES- is as described in table 3-9. TLIORES- shall be used by the CRU circuit board to clear and mask all interrupts and shall also be used to reset any state controllers to the start or power-up state. TLIORES- should be low true and CRU circuit board loading should not exceed one normalized TTL load per CRU connector.

TILINE Power Fail Warning Pulse (TLPFWP–). The function of TLPFWP– is as described in paragraph 3.2.8.5. TLPFWP- should be low true and CRU circuit board loading should not exceed one normalized TTL load per CRU connector.

TILINE Power Reset (TLPRES-). The function of TLPRES- is as described in paragraph 3.2.8.5. TLPRES- should be used without buffering to inhibit critical control and data lines to peripheral devices so that erratic operation of the peripheral does not occur when the chassis power is cycled. TLPRES- is a low true signal and CRU circuit board loading should not exceed ten loads per connector. Total loading for the 6-slot chassis is 50 TTL loads maximum and for the 13-slot chassis is 100 TTL loads maximum.

CRU Circuit Board Output Timing. All CRU circuit boards shall operate in conformance with output timing specified in figure 3-36. Additionally, the CRU circuit board should not delay STORECLK- more than two gate delays or 30 nanoseconds with respect to CRU data out. High speed logic should be used when gating STORECLK- to ensure minimum delay.

CRU Circuit Board Input Timing. All CRU circuit boards should operate in conformance with input timing specified in figure 3-37. Additionally, CRUBITIN should be stable within 90 nanoseconds after address or module select signals become stable.

CRU Circuit Board Power-up, Power-down Sequence. All CRU circuit boards should use the signals described in the timing diagram of figure 3-33 to inhibit any glitches on control or data lines from the CRU circuit board to the CRU peripheral device so that the CRU peripheral device does not receive any false data or control commands during a power-up or power-down sequence. Also the signals should be used to reset all control and data storage elements to the desired state during the power-up sequence. This includes resetting the interrupt and the interrupt mask.

Loopback Test Feature. All CRU circuit boards that operate with CRU peripheral devices should contain a loopback function on the CRU device interface connector for all data and control lines so that when the device cable is removed and a test enable bit is set the CRU circuit board can be exercised to determine whether it is defective or not.

Production Testing. All CRU circuit boards should be checked in a main chassis of a 990 computer or equivalent to ensure that it conforms to high speed CRU operation.

CRU Circuit Board Peripheral Device Interface. CRU peripheral device interface connections to CRU circuit boards should be made with low cost ribbon cable whenever possible. The interface connector that connects to an RS232 CRU peripheral device, such as a modem, auto dialer, teleprinter, or 912 CRT, should be a right-angle subminiature 25-pin connector (AMP HDP-20 or equivalent).

All TTL drivers on the CRU peripheral device interface should be discrete TTL gates or transistors. The output of these drivers should not be loaded by any devices on the CRU circuit board. All TTL receivers on CRU circuit boards should place no more than one normalized TTL load on the CRU peripheral device interface.

In order to prevent ground loops, no signal on the CRU peripheral device interface should be connected directly to earth ground by the peripheral device. All CRU peripheral devices shall be tested to make sure that the resistance between chassis ground and logic ground exceeds 5000 ohms.

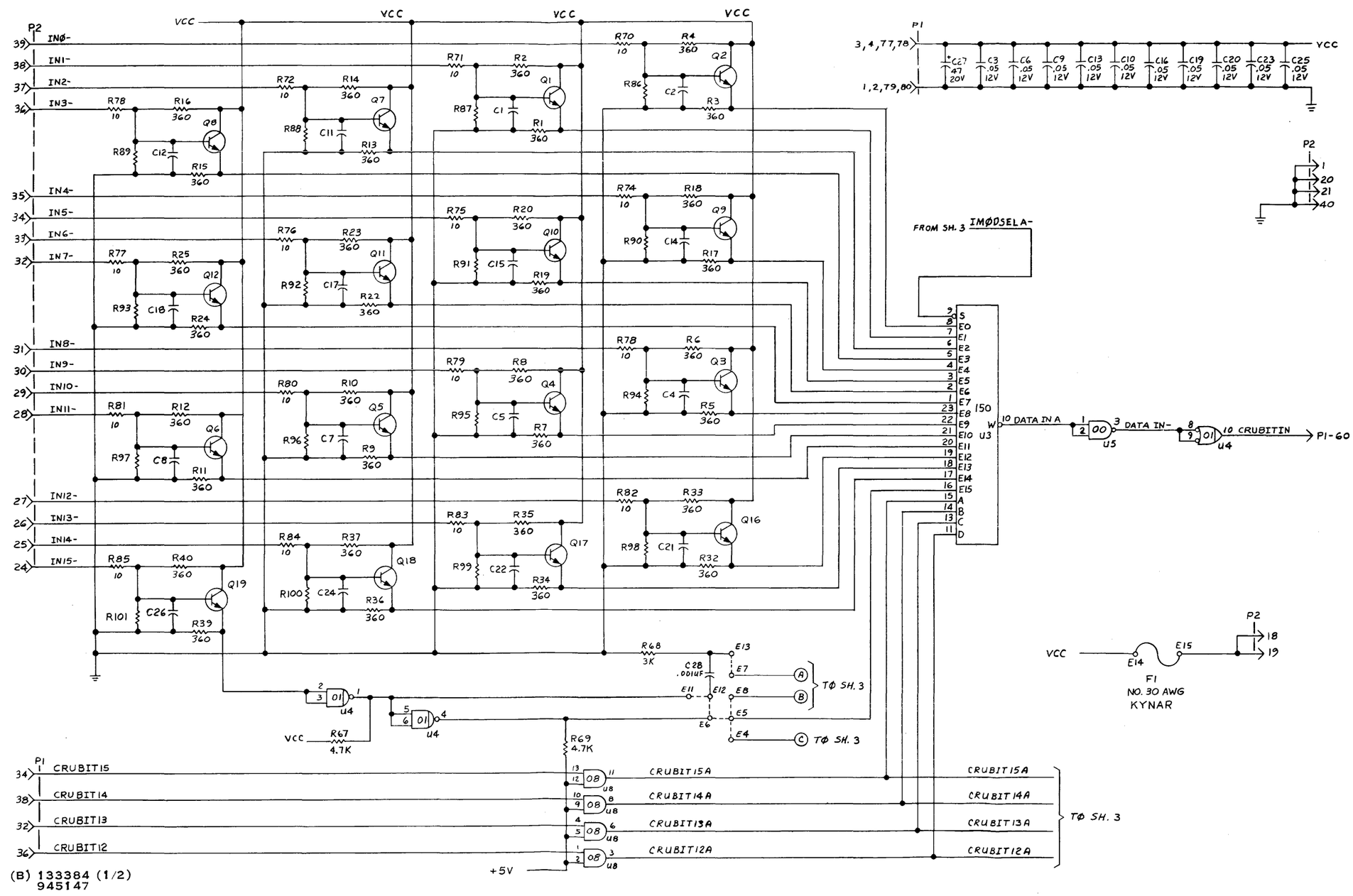

Figure 3-38. Logic Diagram of 16 I/O TTL Data Module (Sheet 1 of 2)

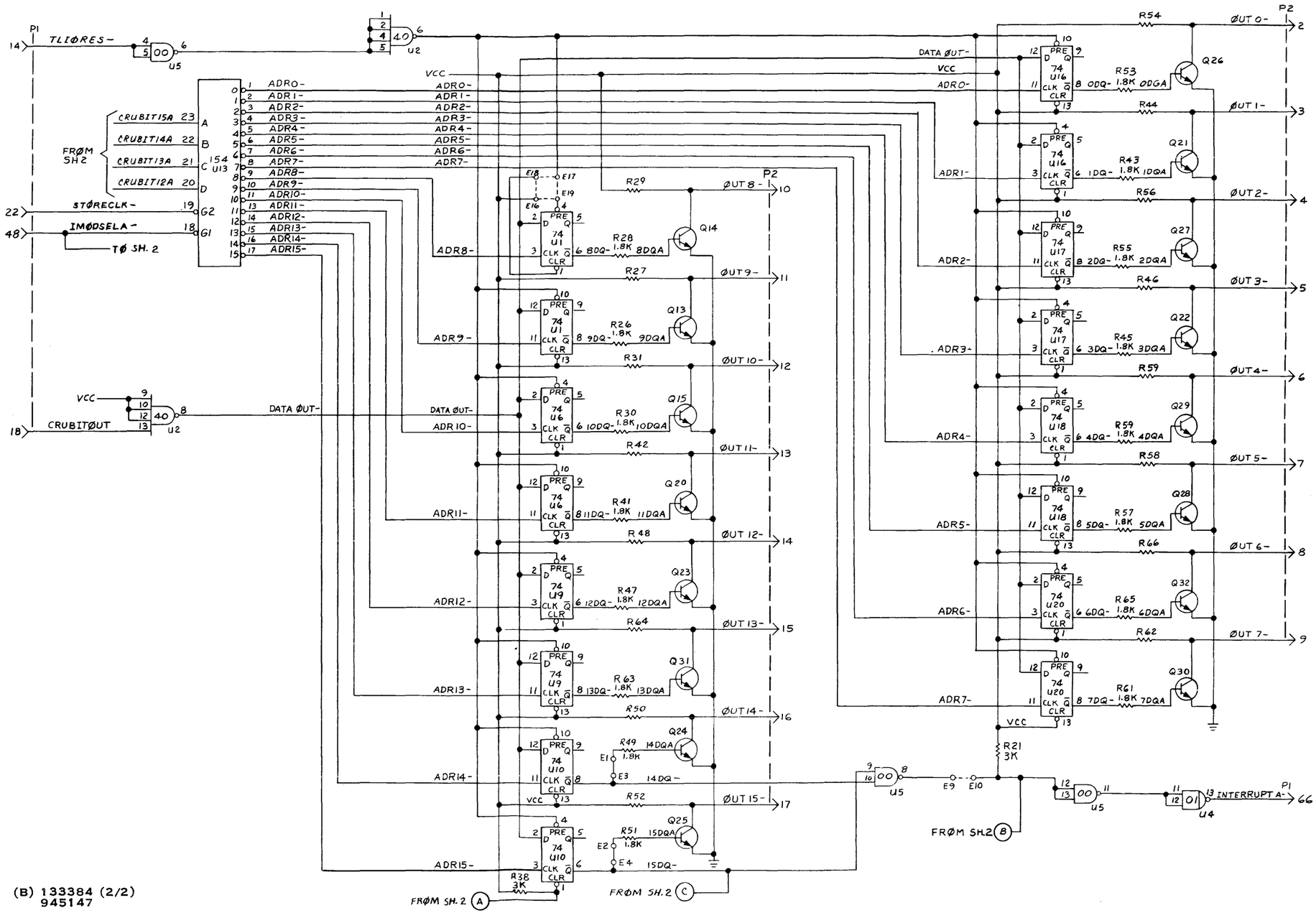

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Figure 3-38. Logic Diagram of 16 I/O TTL Data Module (Sheet 2 of 2)

CRU Circuit Board Software Requirements. All CRU circuit boards should implement interrupts as shown in figure 3-39. Interrupts are enabled only after the user program sets the interrupt mask flip-flop. When the CRU circuit board requests an interrupt it sets the interrupt request flip-flop and an interrupt is generated by the open-collector gate. Once the interrupt request is set it must remain set until it is cleared by either an interrupt acknowledge or an I/O reset. The interrupt ID CRU input bit is implemented so the user program can poll CRU circuit boards connected to the same interrupt to determine which board caused the interrupt. Once the user program has finished servicing the interrupt it clears the interrupt request flip-flop by addressing the interrupt acknowledge CRU output strobe. The interrupt request flip-flop and the interrupt acknowledge flip-flop should be reset after a power-up or whenever a RSET instruction is executed.

Corresponding input and output bits that are used by the LDCR and the STCR instructions shall have the same CRU addresses so that driving software does not have to change the CRU base address between input and output operations.

Dedicated CRU Circuit Boards. Dedicated CRU circuit boards are full-sized circuit boards that decode the full 12-bit CRU address instead of using module selects. Dedicated CRU circuit boards should have dedicated CRU addresses at the high end of the CRU address space. Dedicated CRU boards will operate in any main chassis or I/O expansion chassis without software modifications. Dedicated CRU circuit boards should be implemented when more than 32 bits are required on a full-sized CRU circuit board. Dedicated CRU circuit boards have the same requirements as regular CRU circuit boards except that loading on CRU bits 3 through 11 should not exceed one normalized TTL load.

3.2.8.11 System Interface Board CRU Interface Implementation. The CRU interface as implemented on the system interface board is comprised of TTL devices that serve as the interface between the processor on AU1 board and external CRU devices. The CRU interface signals are brought to two 80-pin male connectors, P1 and P2, at the bottom edge of the system interface board. When the circuit board is installed in full-sized chassis slot 1 of the main chassis, the interface signals are connected to each of the chassis slots through backpanel wiring. The following description of the interface signals and how they are implemented is keyed to the simplified logic diagram of figure 3-32.

CRU Bits 4 through 15. CRU bits 4 through 15 are developed from bits of the processor address bus as follows. Address bus signals MA0 through MA14 from the processor are applied to inverted data three-state bus drivers that are held enabled on the system interface board to develop memory address bus signals MA0- through MA14-. Memory address bits MA3- through MA10 are applied through inverters to develop CRUBITS 4 through 11 for application to connector P1. Each of memory address bits MA11- through MA14- is applied to both inputs of a positive NAND buffer to develop CRUBITS 12 through 15 for application to pins of connectors P1 and P2. See table 3-9 for pin numbers.

Module Select Signals. Memory address bits MA3- through MA10- are applied to an SN74S139 2-to-4 line decoder and three SN7442 BCD-to-decimal decoders to develop module select signals MODSELO– through MODSEL23–. Memory address bits MA3- through MA5-, that correspond to chassis select address field bits CRUBIT4 through CRUBIT6, are applied to a NAND gate to develop an enabling signal, MA345-, for one-half of the SN74S139 and when all are high (MA3 through MA5 are low) one of three main chassis module group signals as selected by memory address bits MA6- and MA7- is low and one of the three BCD-to-decimal decoders is enabled. Memory address bits MA8- through MA10- are decoded by the enabled BCD-to-decimal decoder to develop the module select signal for the addressed module. The module select signals are

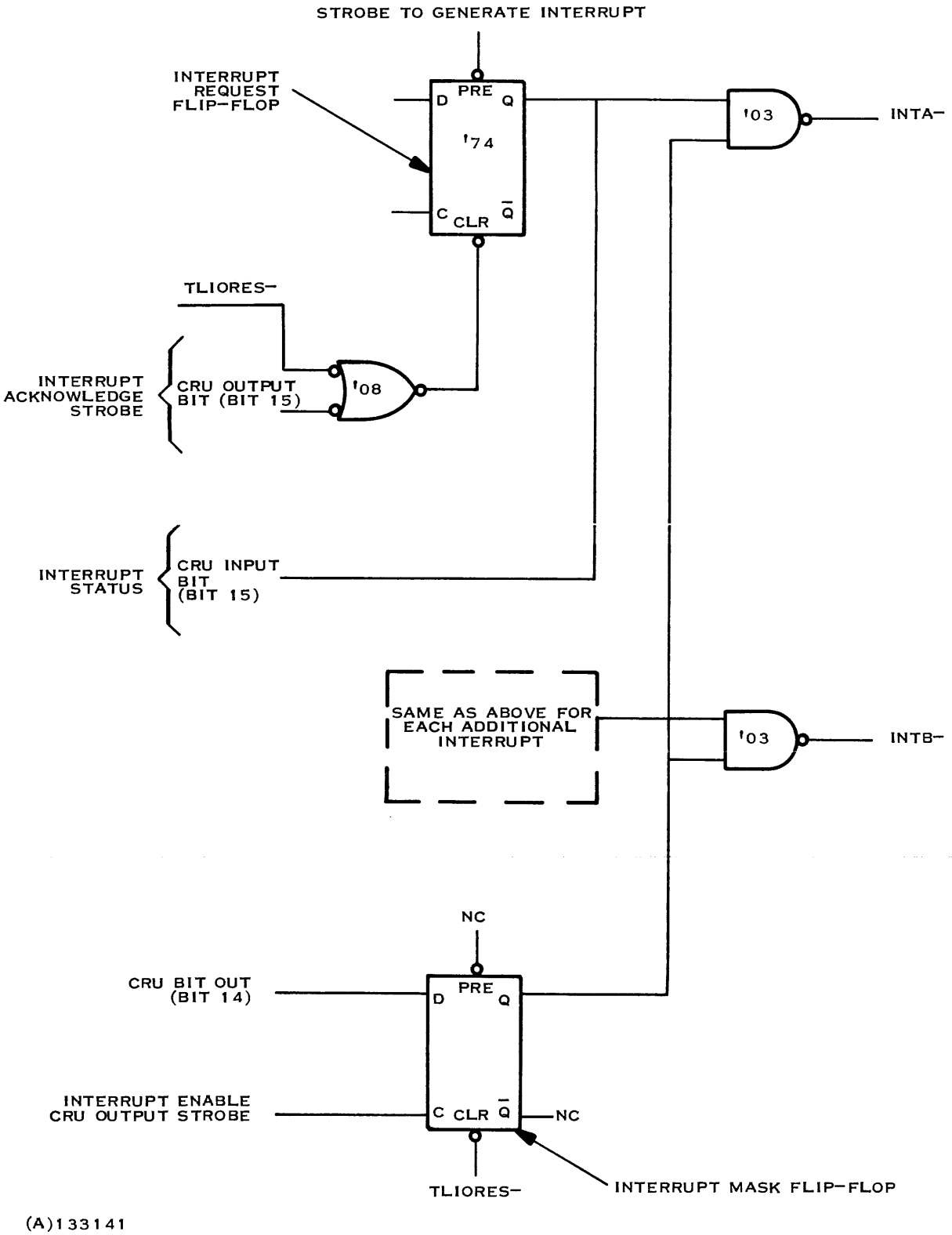


Figure 3-39. CRU Interrupt Implementation

applied to connectors P1 and P2 with pin numbers as shown in table 3-9. Note that when a module on the main chassis is addressed, a low INTCRU– signal advises the processor not to introduce delay to compensate for signal propagation time to an expansion chassis.

Store Clock (STORECLK–). The processor provides a high STORECLK signal to the system interface board to indicate data is available on the CRUOUT line. On the system interface board, STORECLK is ANDed with a protect CRU signal, PROTCRU–. When PROTCRU– is high, the AND gate generates a high STCLKEN that is applied as one input to a NAND gate. A system clock signal, CKB, goes high to generate the low STORECLK– signal at the output of the NAND gate.

The low STORECLK– signal cannot be generated in the absence of a high PROTCRU– signal. Note that when the processor is in the privileged mode of operation (status register bit 7, ST7, equals 0) CRU instructions execute normally but when ST7=1 (nonprivileged mode) a CRU instruction directed to an effective CRU address equal to or greater than $E00_{16}$ generates a low PROTCRU– to cause an error interrupt and the instruction is not executed.

Serial Data Lines. The serial CRU data out line from the processor, CRUOUT, is applied to an inverter on the system interface board. The CRUOUT– output of the inverter is applied to a positive NAND buffer to develop the CRUBITOUT signal at pin 18 of connector P1. Serial data in to the processor is brought in from external CRU devices to system interface board pin 60 of connector P1 as CRUBITIN. The signal is developed across a resistor and applied to the processor as CRUBITINA.

Interrupts. Thirteen external interrupt levels (INT3- through INT15-) are brought to the system interface board at connector P1 with pin numbers as shown in table 3-9. Paragraph 3.2.5 contains detailed information on interrupt logic implementation.

TILINE Power Failure Warning Pulse (TLPFWP–). The TLPFWP– signal is brought into the system interface board at pin 16 of connector P1 and applied as an input of the priority interrupt level encoder to generate a level 1 interrupt to the processor.

TILINE Power Reset (TLPRES–). The normally high TLPRES– signal generated by the power supply goes low at least 10 microseconds before dc voltages begin to fail during power-down and is used to reset connected devices. TLPRES– is brought to both the AU1 and AU2 boards at pin 13 of connector P1.

TILINE I/O Reset (TLIORES–). TLIORES– is a normally high signal that, when low, resets all connected devices. TLIORES– is generated by a RSET instruction in the processor and goes low for a duration of 100 to 500 nanoseconds. TLIORES– is held low by TLPRES– until dc power is up and stable. TLIORES– is applied to external devices at pin 14 of connector P1 or P2.

3.2.9 MEMORY MAPPING OPTION. Memory mapping is an available option with the 990/10 minicomputer that expands the addressing capability of the 990/10 from 64K bytes to 2M bytes. The CPU-TILINE address space without mapping is as shown in figure 3-40 and the address space as expanded with mapping is as shown in figure 3-41.

The addressing expansion is accomplished by relocating the 15-bits of address generated by the processor within blocks of memory defined by preloaded displacement values. The mapping circuits contain three sets of mapping registers (Map 0, Map 1, and Map 2) for use by the operating system, user programs, and long distance instructions, respectively. Each set can define three displacement values for use with the programs using that map. The total memory available

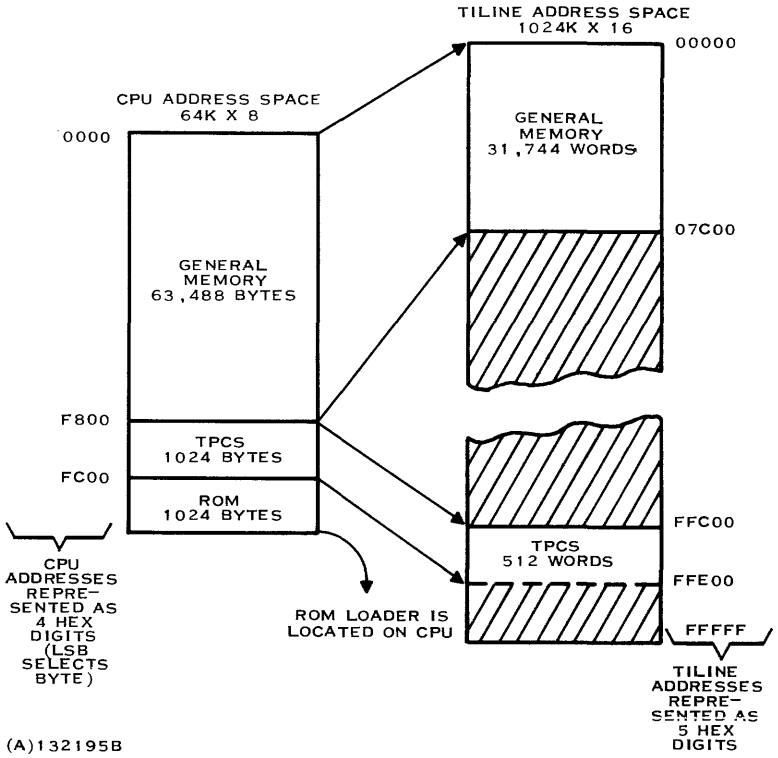


Figure 3-40. 990/10 CPU-TILINE Address Space without Map Option

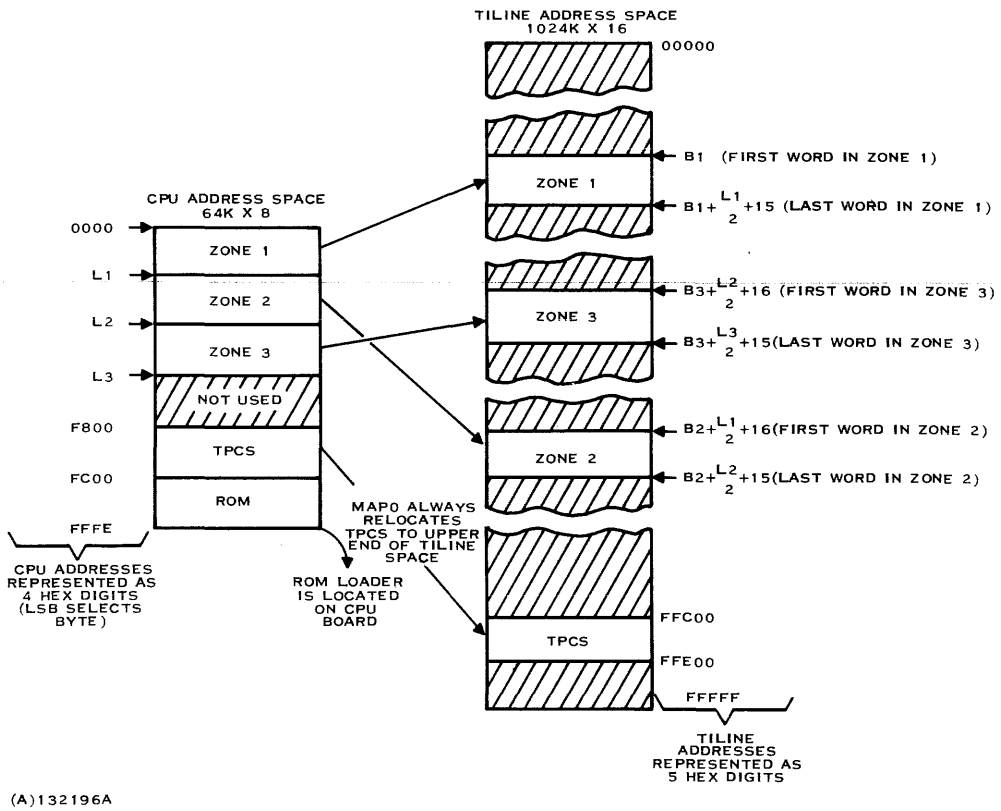


Figure 3-41. 990/10 CPU-TILINE Address Space with Map Option

using one set of map registers is 64K bytes. However, by changing the parameters within the map (with a Load Map File instruction) addresses in the entire 2M byte range can be accessed. In addition to the expanded addressing capability, the memory mapping option provides the following features:

- Error detection logic that generates an interrupt and prevents further memory write operations if a program attempts to access memory above its defined area.
- A diagnostic feedback interface (implemented through the CRU) that allows examination of the contents of any register in the mapping circuitry.
- An output address register that latches the address that produced a memory access error for inspection through the diagnostic interface. This register can also capture an address within a mapping range as requested by the diagnostic interface.
- Automatic detection of accesses to TILINE peripheral controllers and mapping of those accesses to the high order addresses when operating under Map 0 only (the operating system map).

The mapping option is implemented on the AU2B circuit board. If the computer is initially delivered without the mapping option installed, mapping may be added to the system by replacing the original AU2A circuit board with an AU2B circuit board containing the mapping circuitry. Figure 3-42 illustrates the data, address and control paths within the mapping circuitry. The following paragraphs describe the operations performed by the mapping option.

3.2.9.1 **Address Development.** Figure 3-43 illustrates the process that creates a 20-bit address from a 15-bit address. If mapping has been selected, the mapping circuits transfer the four least significant bits of the incoming address to the output address without change. Then the most significant 11 bits (the remaining bits) of the incoming address are added to the least significant 11 bits of the base address register with any resulting carry propagated up through the remaining bits of the base address register. The result of this addition is placed in the 16 most significant bits of the output address to complete the 20-bit address. If mapping is not enabled, a pass-through path (not shown in figure) places the incoming address in the 15 least significant bits of the output address without modification.

3.2.9.2 **Base Register Selection.** Since there are three base registers that can be used for address development in each set of map registers, the mapping circuits must decide which base address register to use for a particular operation. To make this selection, the incoming address is compared to three separate values contained in limit registers L1, L2 and L3. These registers contain the one's complement value of an upper bound address for specified ranges of incoming addresses. Adding each of these complement values to the incoming address (binary subtraction of the true limit values) and then monitoring the carry-out bit from each addition determines the range that contains the incoming address value. If any of the additions do not produce a carry-out, then the incoming address is less than the true value of the corresponding limit register. The three carry-out bits are examined by a priority encoding network to eliminate coincident conditions. For example, if the incoming address is less than the L1 value, then it will also be less than the values in L2 and L3. The priority encoder recognizes only the lowest limit register and generates a gating code to select the base register addition process that corresponds to the recognized limit register. Therefore, an incoming address that is less than or equal to the true value of L1 will be added to the value in base register B1; an address that is greater than L1 but less than or equal to L2 will be added to the value of B2; and an address that is greater than L2 but less than or equal to L3 will be added to the value of B3. Incoming addresses that are greater than all three limit registers are not mapped and generate an error signal to the processor. A fourth input to the priority encoder circuit generates a code to select the pass-through path for the incoming address if mapping is not selected.

The address development and the limit comparison processes occur simultaneously for each of the base registers and the limit registers. Therefore, the output of the limit comparison selects the result of one of the address development processes, rather than enabling the process itself. This construction greatly increases the speed of the mapping process to provide a mapped address as soon as the comparison is complete.

3.2.9.3 **Map Selection.** The map file option contains three sets of map registers that are used for the following functions:

- Map 0: This set of map registers is reserved for use by the operating system so that its area of memory can be segregated from that used by programs running in the system.
- Map 1: This set of map registers is used by programs running under the operating system.
- Map 2: This set of map registers is used exclusively by the long distance instructions and cannot be accessed with any other instructions.

Two signals from the AU1 circuit board determine which of the maps will be used for a particular map loading operation: MAP2– and LDMAPID–. MAP2– enables the long distance instruction map (Map 2) by generating a map select code (RA0 and RA1) equal to a binary 11. This signal is generated by the instruction microcode on the AU1 circuit board when it encounters a long distance instruction. LDMAPID– selects either Map 0 or Map 1 by generating a map select code equal to either a binary 00 or a binary 10, respectively. This signal is developed in the AU1 circuit board from bit 11 of the instruction word (Map code of the format 10 instruction). If this incoming signal is a 1, it selects Map 0; if the signal is a 0, it selects Map 1 to be loaded.

During regular use of the map file (when not loading), a third signal from the AU1 circuit board, ST8A–, determines which map file will be used for the program under execution. This signal is developed on the AU1 circuit board from bit 8 of the status Register. If this signal is a 1 (ST8 = 0), then Map 0 will be used; if this signal is a 0 (ST8 = 1) then Map 1 will be used.

3.2.9.4 **Map File Loading.** During a Load Map File (LMF) operation, the AU1 circuit board activates the LDMAPA– interface signal to set a flip-flop in the map file control circuits that indicates that a load operation is in progress. Simultaneously, an address is placed on the input address lines from AU1. This address indicates the starting memory address of the map file parameters to be loaded. After passing through the address mapping circuits, the address is passed to memory to fetch the first parameter word, and is also stored in the Latched Memory Address Register. The Load Map signal then performs two functions. It disables output from the memory mapping circuits to the memory and enables the output from the Latched Memory Address Register to the memory bus. In addition, the Load Map signal enables the Load Map Counter to increment with each succeeding clock pulse. Since the counter is initially at zero, it generates a gating signal (GWO) to transfer the first parameter from memory into Limit Register 1. Subsequent memory cycles increment the counter so that the incoming data is distributed to the registers in the selected map file in the following order:

1. Limit Register 1 (GWO)
2. Base Register 1 (GW1)
3. Limit Register 2 (GW2)
4. Base Register 2 (GW3)
5. Limit Register 3 (GW4)
6. Base Register 3 (GW5)

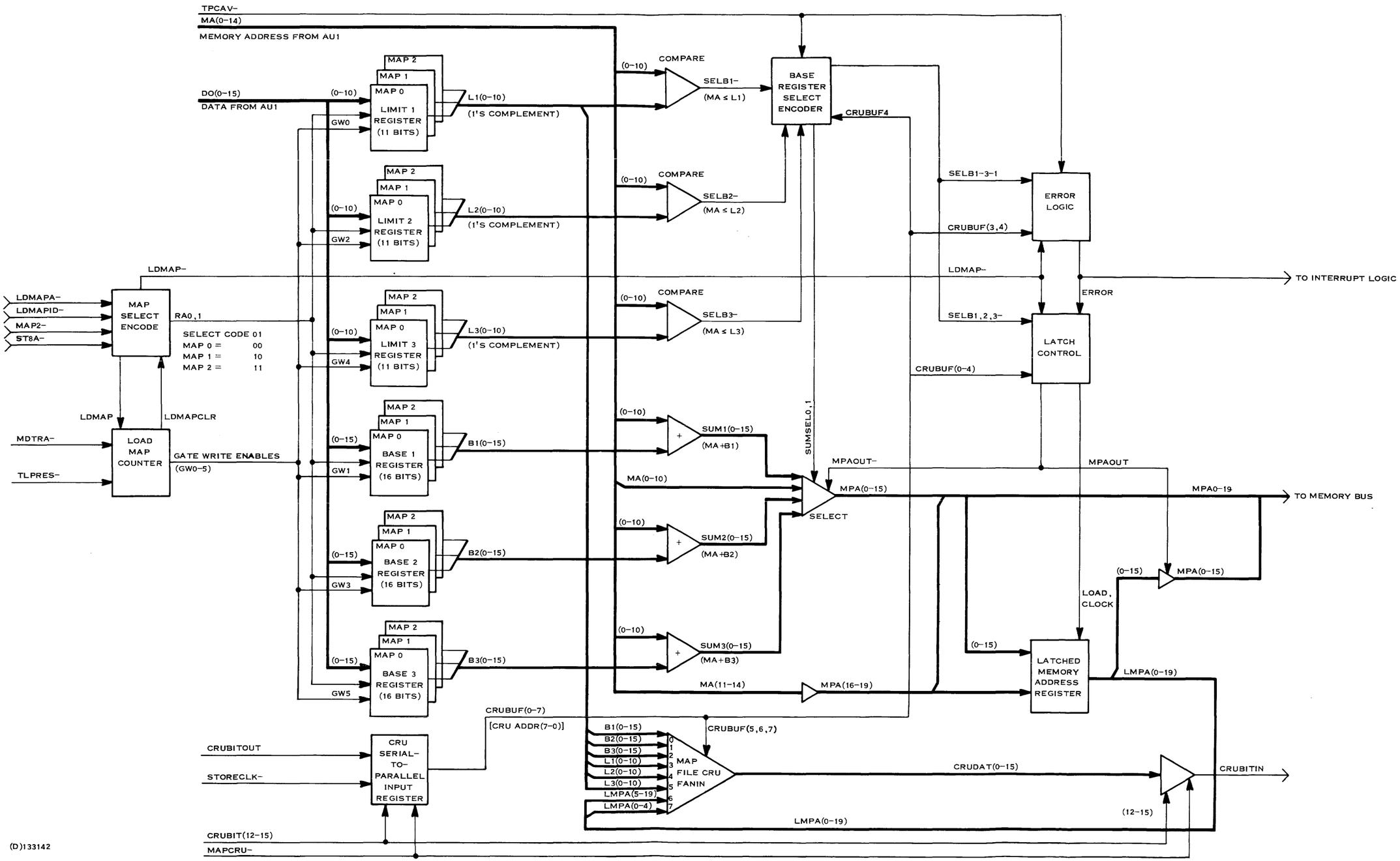


Figure 3-42. Memory Map Option, Detailed Block Diagram

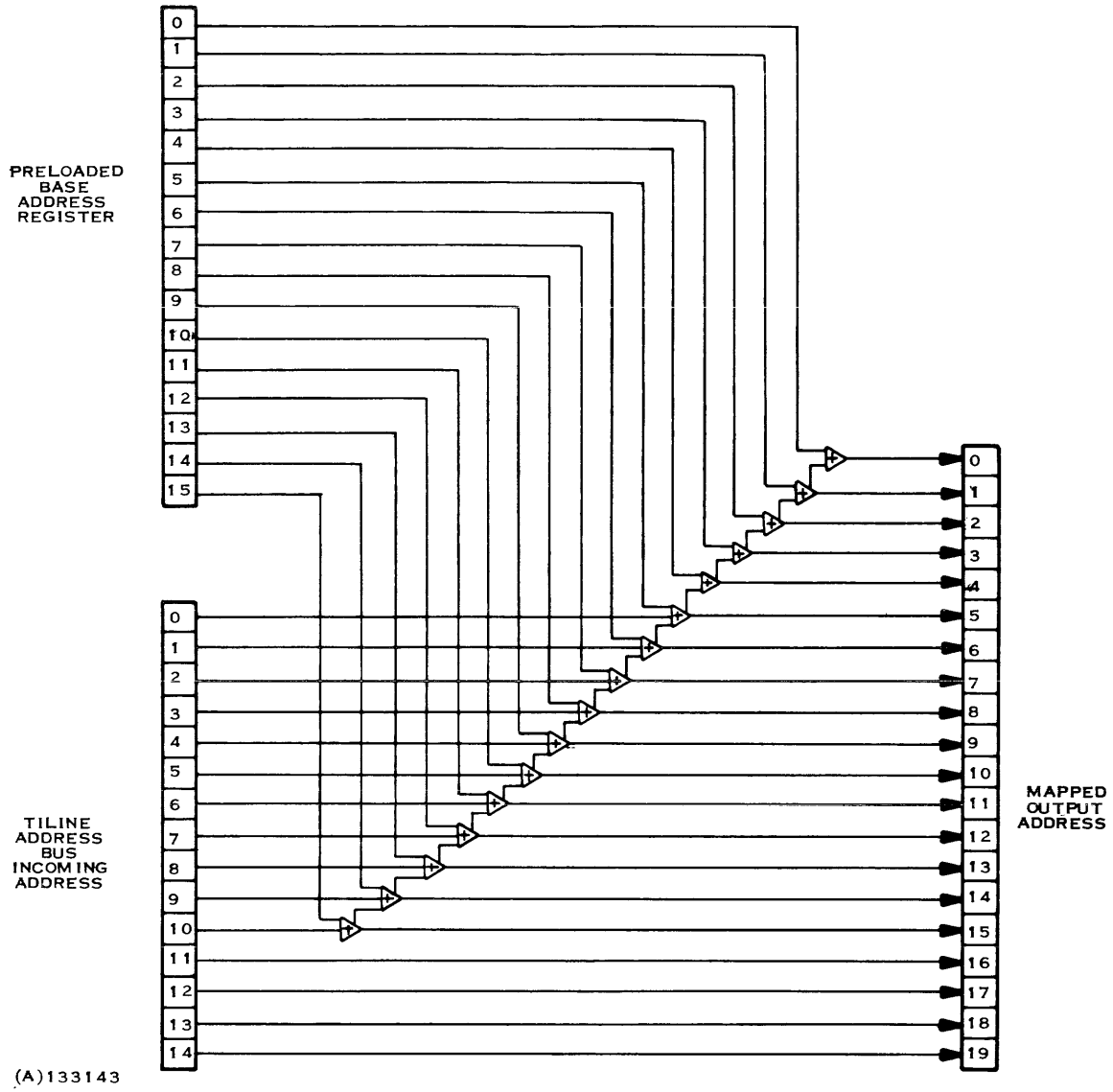


Figure 3-43. Mapped Address Development

To access the parameters from memory, AU1 generates successive memory addresses and sends them to the mapping circuits. The lowest 4 bits pass through the mapping circuits unchanged and are combined with the 16-bit output from the Latched Memory Address Register to form the mapped 20-bit address sent to memory. However, if the initial value of the least significant 4 bits of the address was B_{16} or greater, incrementing the address through the six locations produces a carry-up to the next hexadecimal group of the address. This next group is not passed through the map logic. To allow for this condition, the 20-bit Latched Memory Address Register (only the 16 MSBs are used for output) is incremented with each memory cycle. Any carry produced in the counting process adjusts the value placed on the memory bus so that six contiguous words of memory are accessed.

Because of the sequence used in accessing the mapping parameters and the manner in which the data is loaded from the data bus into the map file registers, the data must be formatted correctly in memory before the load operation begins. Figure 3-44 illustrates the proper format for the parameters. All parameters must be in contiguous memory locations in the order that they will be loaded. In addition, the values must be left-justified within the memory word since the 5 least significant bits are ignored when loading the limit registers. Also, due to the method of comparison of the limit registers to incoming address, the true values of the limit registers must be in ascending order; i.e., L1<L2<L3.

3.2.9.5 Map File CRU Interface. The map file implements a CRU interface to the processor for diagnostic purposes. The CRU interface allows the diagnostic program to read the contents of any of the map file registers into memory for inspection. In addition, the interface provides for disabling mapping operation and for control of the error and mapping flags. Figure 3-45 illustrates the CRU output interface to the map file circuitry; table 3-11 defines the bit assignments for this output interface. Figure 3-46 illustrates the CRU input interface from the map file circuitry. The bit assignments for the input interface are determined by the 3-bit Read Register Select code that is defined in the output interface. The input interface provides access to the map file register contents for the map (Map 0, Map 1 or Map 2) that is currently selected. To read the contents of a different set of map file registers, the map select code (RA0 and RA1) must be changed. Refer to the discussion of Map Selection earlier in this section. The map file CRU interface responds to base address $1FA0_{16}$.

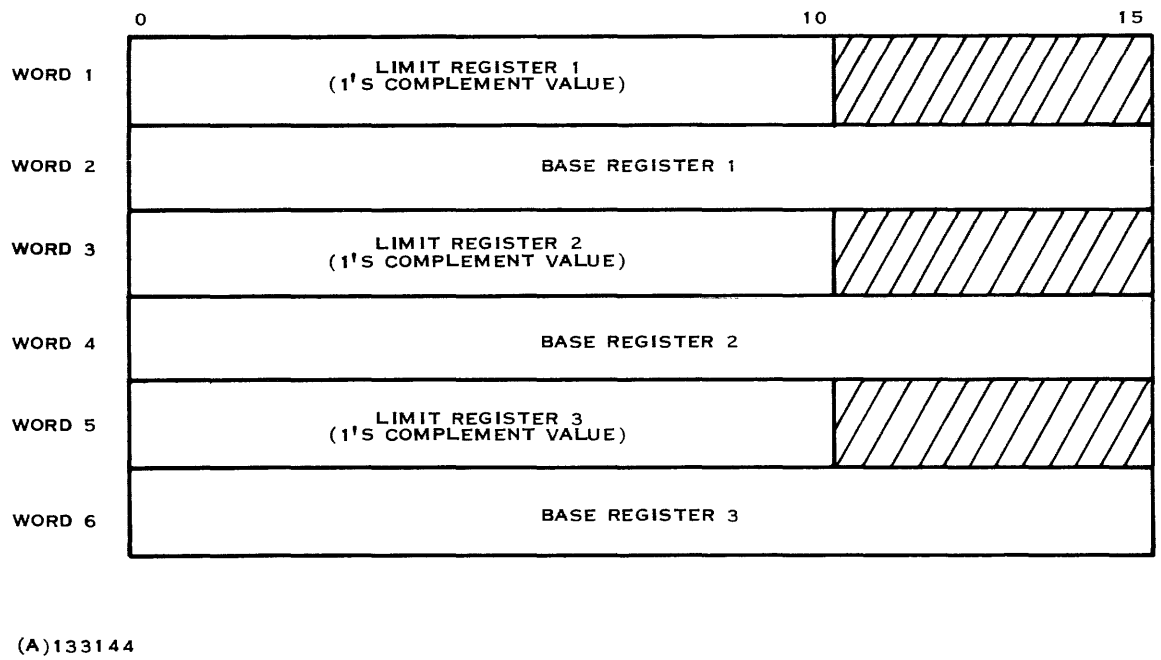


Figure 3-44. Memory Format of Mapping Parameters

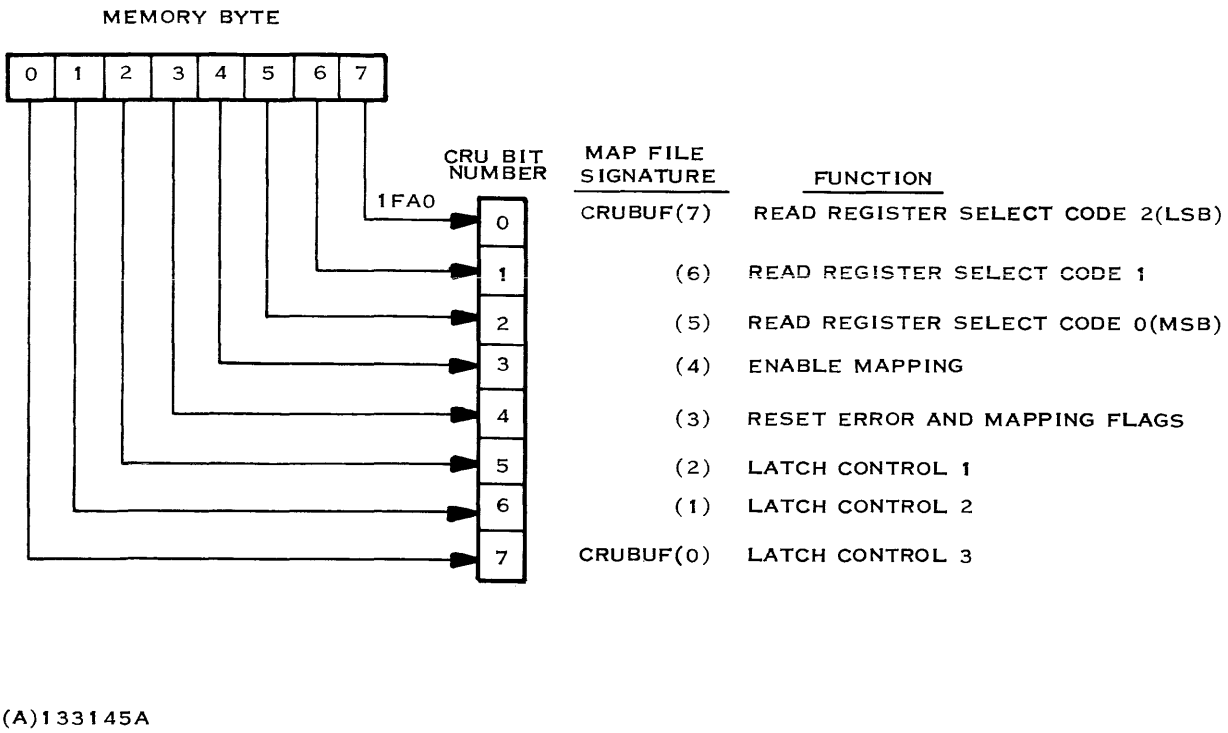


Figure 3-45. Memory Map File CRU Output Interface

3.2.9.6 **Latch Control and Error Logic.** The error circuitry monitors the three limit register comparisons to determine if the current address is within legal limits for the selected set of map registers. If the incoming address exceeds the value in all three limit registers, an error signal is generated. The error signal in turn sets two latches, Capture Address Latch and Error Flag.

The error flag sets when the limit error is detected. The output of this flag generates an interrupt to the processor and sets another error latch that prevents memory write cycles. This second error latch remains set until the currently executing instruction is completed to prevent any further memory requests from storing data in an unauthorized location. When the instruction is complete, the processor traps to the interrupt routine. To allow the processor to perform the context switch, memory write cycles are again enabled by the cleared second error latch. The first error flag remains set until cleared by a CRU instruction in the interrupt service routine.

The capture address latch sets when the limit error is detected. The output of this latch disables clock inputs to the Latched Memory Address Register so that the current memory address (the one that produced the error) is held in that register. Memory addresses continue to be mapped and sent to memory, but they are not clocked into the Latched Memory Address Register. The address that produced the error is therefore held in the register until the interrupt service routine clears the capture address latch with a CRU instruction. This allows the service routine to read the contents of the Latched Memory Address Register through the CRU input interface to determine the nature of the mapping error.

Table 3-11. Map File CRU Output Bit Assignments

CRU Bit Number	Function
0 (LSB) through 2 (MSB)	Read Register Select Code 2 (LSB) through 0 (MSB): This 3-bit code selects which of the map file registers in the currently selected map will be fanned-in for sampling on the CRU input interface. The code bits are decoded as follows:

Code Bit 0	1	2	Register Selected
0	0	0	Base Register 1
0	0	1	Base Register 2
0	1	0	Base Register 3
0	1	1	Limit Register 1
1	0	0	Limit Register 2
1	0	1	Limit Register 3
1	1	0	Latch Memory Address Register (5-19)
1	1	1	Latch Memory Address Register (0-4)

Enable Mapping: When set to a 1, this bit turns on the mapping circuitry; when this bit is cleared, mapping is disabled.

Reset Flags: Setting this bit to a 1 clears the error flag and the capture address latch, and prevents them from being set again; clearing this bit enables operation of the two latches.

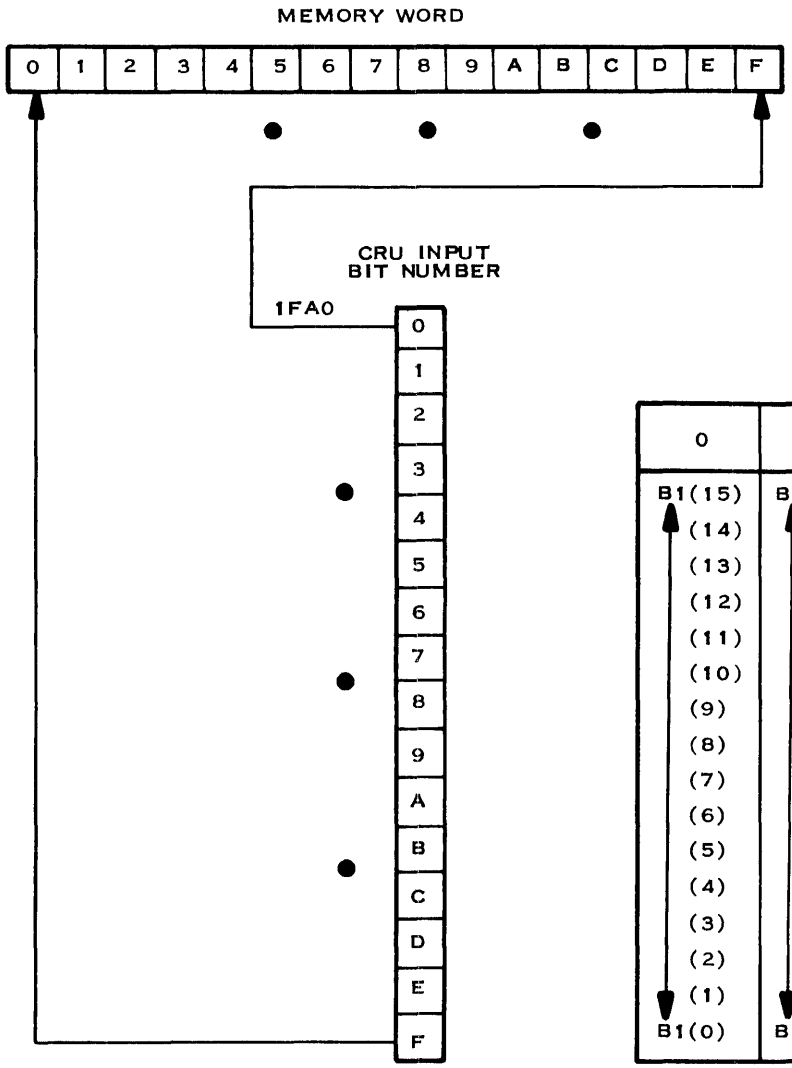
Latch Control 1: When set, this bit instructs the mapping circuits to capture the first address that uses base register 1. The resulting mapped address will be captured in the Latch Memory Address Register.

Latch Control 2: When set, this bit instructs the mapping circuits to capture the first address that uses base register 2. The resulting mapped address will be captured in the Latch Memory Address Register.

Latch Control 3: When set, this bit instructs the mapping circuits to capture the first address that uses base register 3. The resulting mapped address will be captured in the Latch Memory Address Register.

In addition to a limit error, the capture address latch also sets during a load map file operation and when an address is processed that uses any of the three base registers specified in the Latch Control bits of the CRU Output interface. Again, the current mapped address is held in the Latched Memory Address register when the capture address latch is set. During a load map file operation this address is then incremented with each new memory cycle. When used in the Latch Control function, the contents of the Latched Memory Address Register should be read through the CRU input interface for diagnostic inspection. In either case, the capture address latch should be reset as soon as possible in case any new mapping errors occur.

3.2.9.7 **TILINE Peripheral Control Space (TPCS).** The TILINE Peripheral Control Space (TPCS) is a range of TILINE addresses reserved for assignment to peripheral device controllers. The address range is 512 words. This range of addresses extends from TILINE word address $FFC00_{16}$ through $FFDFF_{16}$. The processor, whether with or without the mapping option, maps CPU addresses $F800_{16}$ through $FBFF_{16}$ to the TPCS (see figures 3-40 and 3-41). This particular mapping occurs (for both the mapping and nonmapping options) only when map file zero is invoked (status register bit 8 = 0).



READ REGISTER SELECT CODE (0,1,2)

0	1	2	3	4	5	6	7
B1(15)	B2(15)	B3(15)	-0-	-0-	-0-	-0-	LATCH(4)
(14)	(14)	(14)	-0-	-0-	-0-	LATCH(19)	① (3)
(13)	(13)	(13)	-0-	-0-	-0-	① (18)	(2)
(12)	(12)	(12)	-0-	-0-	-0-	(17)	(1)
(11)	(11)	(11)	-0-	-0-	-0-	(16)	LATCH(0)
(10)	(10)	(10)	L1(10)	L2(10)	L3(10)	(15)	-0-
(9)	(9)	(9)	(9)	(9)	(9)	(14)	-0-
(8)	(8)	(8)	(8)	(8)	(8)	(13)	-0-
(7)	(7)	(7)	(7)	(7)	(7)	(12)	-0-
(6)	(6)	(6)	(6)	(6)	(6)	(11)	-0-
(5)	(5)	(5)	(5)	(5)	(5)	(10)	-0-
(4)	(4)	(4)	(4)	(4)	(4)	(9)	-0-
(3)	(3)	(3)	(3)	(3)	(3)	(8)	-0-
(2)	(2)	(2)	(2)	(2)	(2)	(7)	-0-
(1)	(1)	(1)	(1)	(1)	(1)	(6)	-0-
B1(0)	B2(0)	B3(0)	L1(0)	L2(0)	L3(0)	LATCH(5)	-0-

① LATCH = OUTPUT OF LATCH MEMORY ADDRESS REGISTER

Figure 3-46. Memory Map File CRU Input Interface

The computer uses the TPCS to precondition TILINE peripheral controllers to perform data transfers. Each controller is assigned a block of 16 addresses from the TPCS; however, a specific controller may not require all 16 addresses. The TPCS addresses allow the computer to directly access a hardware register file within the Slave portion of the TILINE peripheral controller. By writing into this register file, the computer defines a data transfer operation that the Master portion of the controller will perform. The actual function of each word of the TPCS depends on the particular controller. The computer can also examine the contents of the controller's register file by performing a read operation with the TPCS addresses assigned to that controller. Figure 3-47 illustrates the TPCS concept.

The mapping circuits develop TPCS addresses by monitoring the six most significant bits of the incoming address. If the five most significant bits are set and the sixth most significant bit is clear (CPU address is $F800_{16}$ or greater but less than $FC00_{16}$), status register bit 8 is clear (using Map 0), and for the processor with the mapping option no long distance instruction is being executed (not using Map 2); then the mapping circuits pass the incoming address bits through to the least significant 15 bits of the output TILINE address. To complete the TILINE address, the mapping circuits insert five 1's as the five most significant bits of the TILINE word address. This transposition process is illustrated in figure 3-48.

3.2.10 **990/10 RAM MEMORY BOARD.** The 990/10 memory board is the third of the three printed circuit boards and is available in a number of optional configurations. Refer to paragraph 1.3.1.3 for a discussion of options available. Refer to paragraph 3.3 for an in-depth description of each of the configurations.

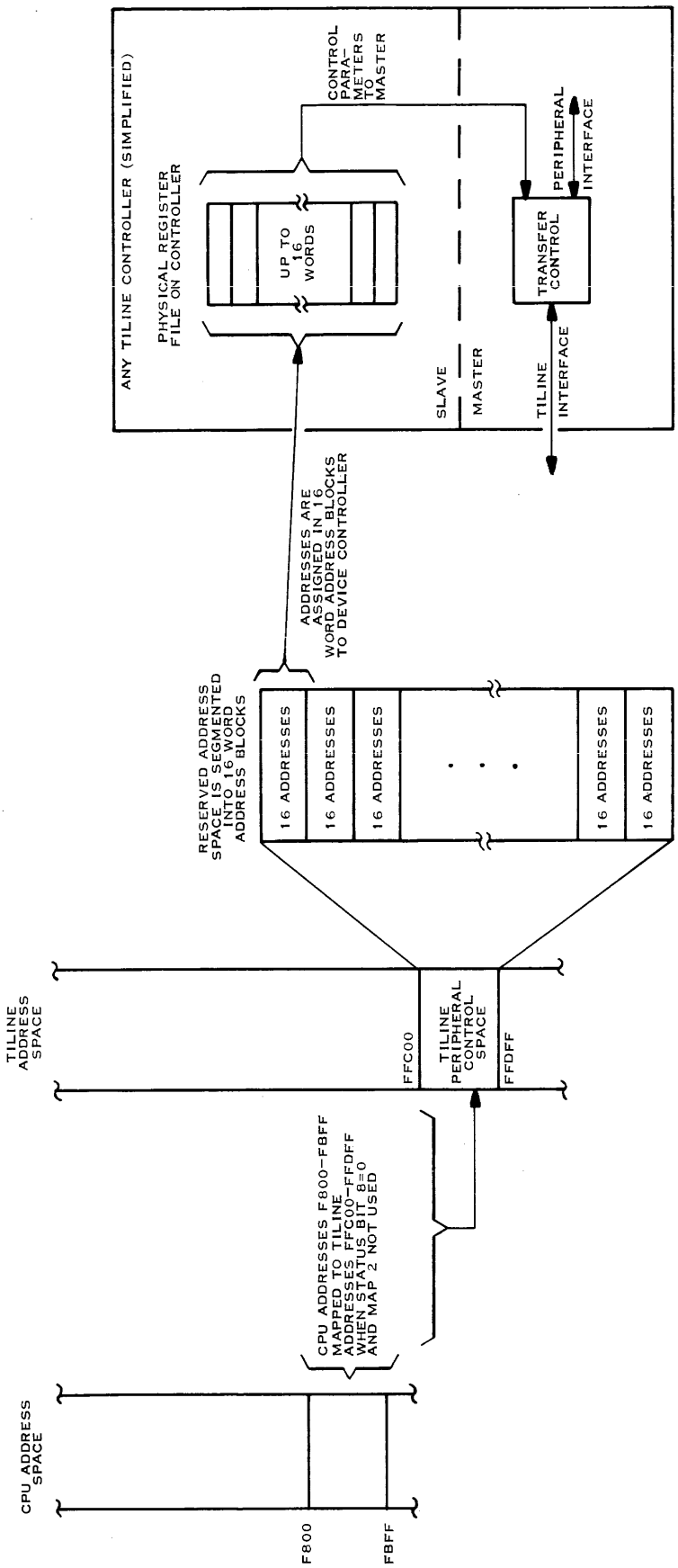
3.3 RAM EXPANSION MEMORY AND OPTIONS AVAILABLE

A number of RAM memory configurations are available in the 990/10 minicomputer system. The relationship between the CPU options and the RAM memory options is illustrated in figure 3-49. The four CPU options available include two with the mapping option and two without the mapping option. The mapping feature is required in order to make it possible for the CPU to address RAM in excess of 64K bytes (permits addressing of up to 2M bytes). Two of the CPU options have no parity error detection but may have parity included as an option. These processors have a memory board that is complete with a memory controller and from 16K to 40K bytes of RAM. A third CPU option without mapping (PN 944920-0001) and a fourth option with mapping (PN 944920-0006) include error checking and correction circuitry (ECC) in the basic 16KB memory on its third (or memory) board.

Memory expansion boards (944945-0002 through 944945-0005) without parity and without error correction are available for expanding the memory of each of the CPU options by 16K, 24K, 32K, or 40K bytes as designated by the appropriate dash number. The expansion memory boards are available with parity installed in part numbers 944945-0007 through 944945-0010.

A 16KB module of RAM with ECC (includes controller - PN 946655-0002) provides the error correcting RAM and controller for the -0001 and -0006 CPUs. This board is also used as an expansion board to interface the CPU with each additional board of Add-On RAM with ECC (PN 945093-xxxx). The Add-On (Array) boards have no controller and provide memory in increments of 16K, 32K and 48K bytes for a total of 64K bytes for each set of boards which includes an ECC 16KB Expansion board and accompanying Add-On board with 48K bytes.

- In standard and fine line versions, the 96KB memory controller (2261980-xxxx) provides up to 96K bytes of memory in increments of 32K bytes. The cache controller (2261990-0001) provides 64K bytes of on-board memory. Each of these controllers uses the TMS 4116 memory device and has the control logic for up to 1M bytes of additional memory on the 256KB add-on memory array boards.


ANY TILINE CONTROLLER (SIMPLIFIED)
PHYSICAL REGISTER FILE ON CONTROLLER
UP TO 16 WORDS
CONTROL PARA-METERS TO MASTER
TRANSFER CONTROL
PERIPHERAL INTERFACE
SLAVE
MASTER
TILINE INTERFACE
ADDRESSES ARE ASSIGNED IN 16 WORD ADDRESS BLOCKS TO DEVICE CONTROLLER
RESERVED ADDRESS SPACE IS SEGMENTED INTO 16 WORD ADDRESS BLOCKS
16 ADDRESSES
TILINE ADDRESS SPACE
FFC00
TILINE PERIPHERAL CONTROL SPACE
FFDFF
CPU ADDRESSES F800-FBFF MAPPED TO TILINE ADDRESSES FFC00-FFDFF WHEN STATUS BIT 8=0 AND MAP 2 NOT USED
CPU ADDRESS SPACE
F800
FBFF
NOTE: TPCS ADDRESSES SPECIFY PHYSICAL REGISTERS IN TILINE DEVICE CONTROLLER SLAVE INTERFACE
(B)133291

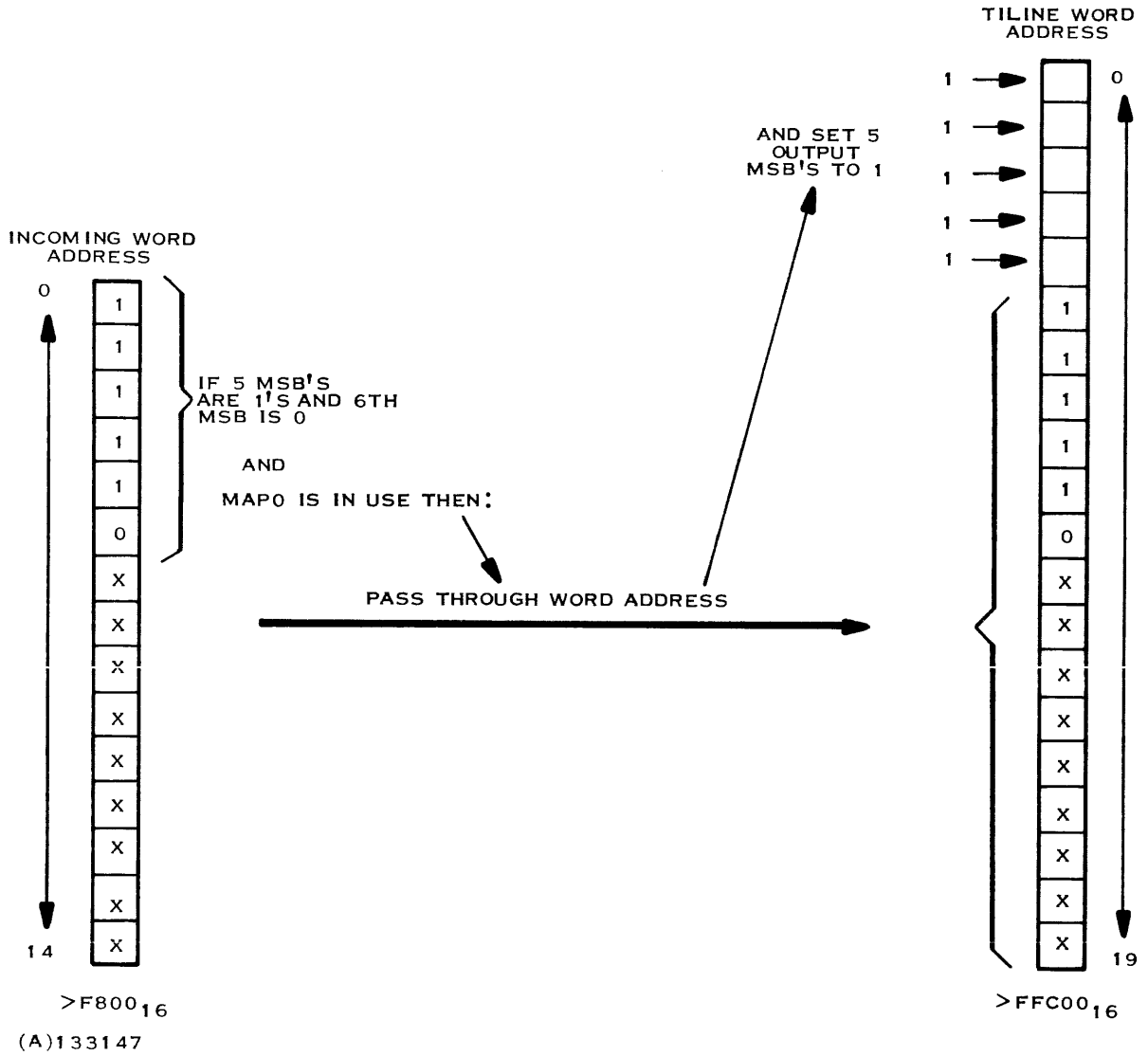


Figure 3-48. Development of TPCS Address

3.3.1 MEMORY EXPANSION BOARD. Details on the physical description, performance specifications, interfaces and memory expansion board control and operation are included in the following paragraphs.

3.3.1.1 **Physical Description – Memory Expansion Board and Chip.** The memory expansion board is a two-sided 160-pin printed circuit board. As shown in figure 3-50, the controller circuitry occupies the lower part of the board. Thirteen bits of the MOS memory chips occupy the upper left part of the board and the remainder of the chips occupy the upper right part of the board. The address buffers are placed between the areas of MOS chips and the clock circuitry appears in the upper right corner of the board. Each 8K byte increment of memory is supplied by a row of 16 TMS 4050 chips with an additional chip in each row if the parity option is implemented on the board. Five rows of MOS chips supply the maximum 40K bytes of memory per board.

The TMS 4050 chip is organized as 4096 one-bit words and is housed in an 18-pin dual-in-line package. The chip is based on N-channel silicon-gate technology and the inputs are TTL compatible.

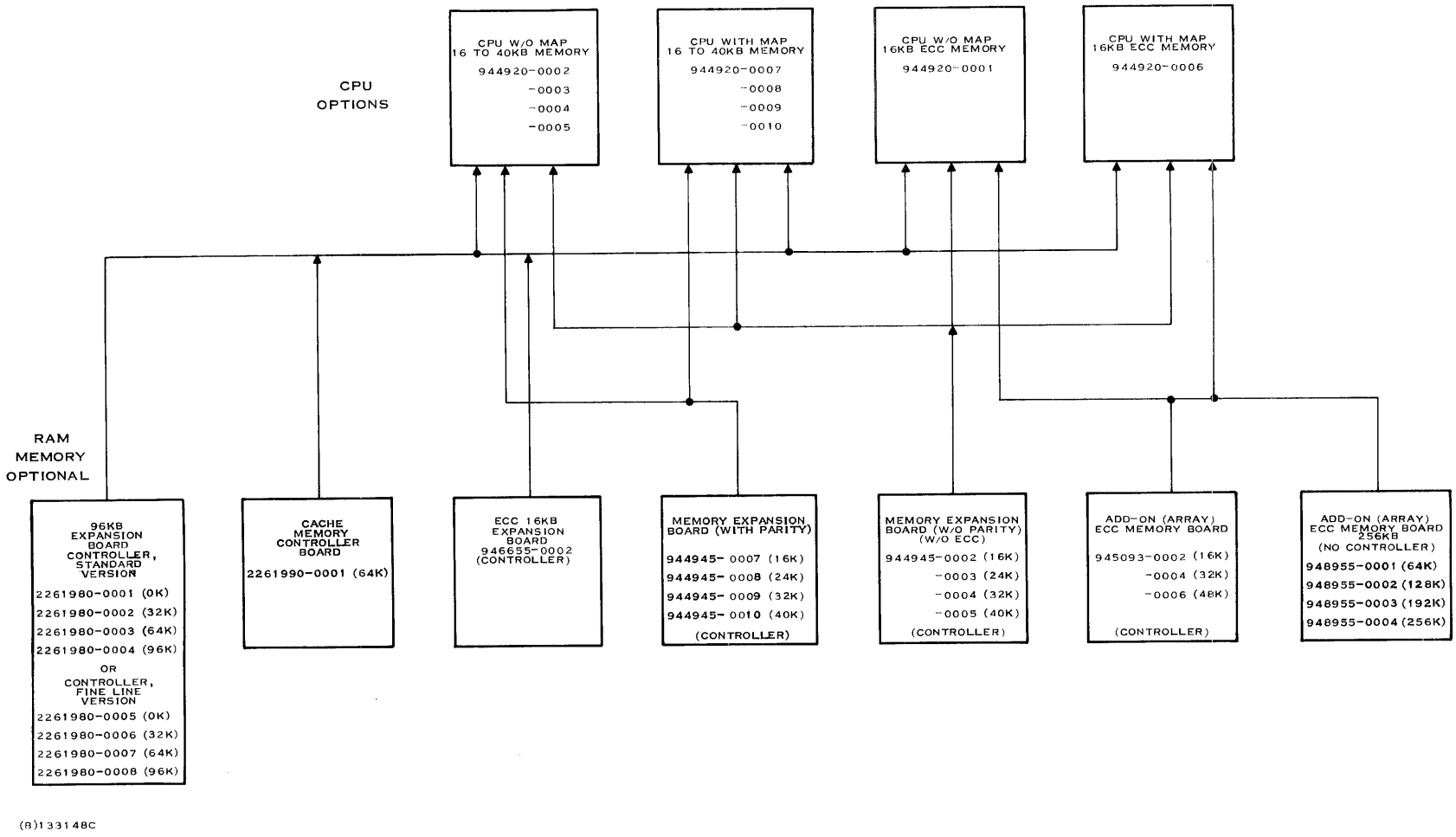


Figure 3-49. Applicability of Memory Options to CPU Options

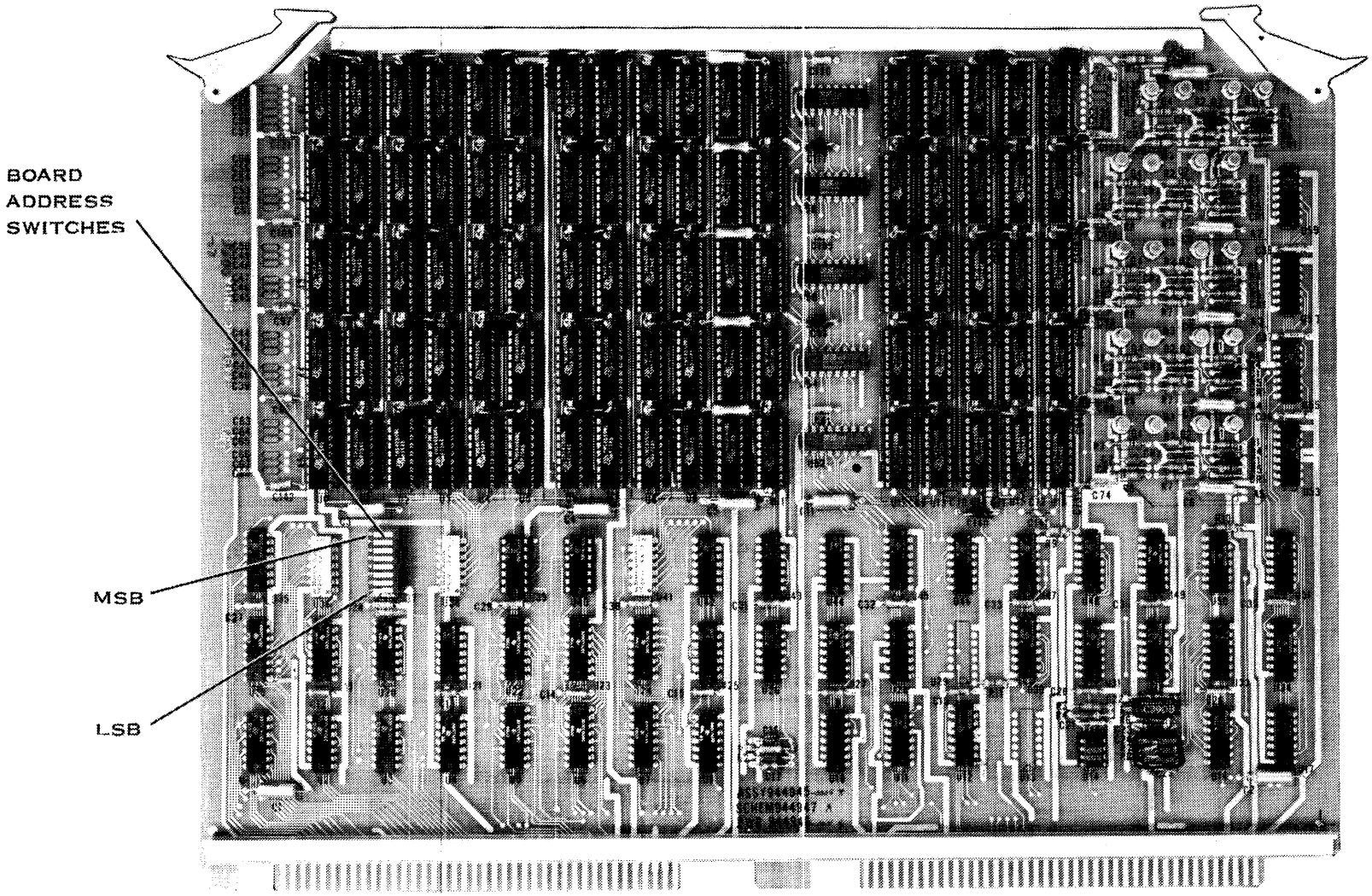


Figure 3-50. Memory Expansion Board

An LED indicator on each memory expansion board provides an indication of a memory parity error on that board. A dual-in-line package containing eight single-pole, single-throw switches is mounted on the board to permit the setting of the starting address of the memory locations within the control of a particular memory expansion board. The address switches correspond to the eight most significant bits of the 20-bit TILINE address, and allow board address selection in 4K-word increments. Switch 1 is the most significant bit of the address; switch 8 is the least significant bit of the address group. All Model 990/10 Computer systems must have a minimum of 8K bytes of dynamic RAM. Since the ROM loader begins loading the memory at TILINE address location 00050_{16}, the board address switches must all be OFF in systems containing only one memory expansion board. Table 3-12 lists the required switch settings for some memory board addresses up to 64K. Addresses greater than 64K can be represented in a similar manner using the eight switches to represent the binary number desired.

Table 3-12. Memory Board Address Settings

Beginning* Address On Board ( )16	Address Switch Setting								Number Of Memory Words Below Board
	1	2	3	4	5	6	7	8	
00000	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	0
01000	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	4,096
02000	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	8,192
03000	OFF	OFF	OFF	OFF	OFF	OFF	ON	ON	12,288
04000	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF	16,384
05000	OFF	OFF	OFF	OFF	OFF	ON	OFF	ON	20,480
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
0F000	OFF	OFF	OFF	OFF	ON	ON	ON	ON	61,440
10000	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	65,536
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
40000	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	262,144
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
F4000	ON	ON	ON	ON	OFF	ON	OFF	OFF	999,424

* The amount of addressable memory for any particular board is dependent on the configuration of the board, i.e. each dash number has a different size of addressable memory.

3.3.1.2 **Memory Expansion Board Performance Specifications.** The typical access time for dynamic RAM memory expansion boards is 500 nanoseconds. The cycle time is system dependent and is typically 725 nanoseconds for 990/10 systems. Access time may be increased to a maximum of 1050 nanoseconds in the presence of an interfering refresh cycle that must be performed at least once every 31 microseconds to ensure retention of stored data. In the event of main power failure, standby power from a battery included in the mainframe prevents loss of stored data for at least 30 minutes. The memory operates within specifications over a temperature range of 0 to 65 degrees Celsius (32 to 149 degrees Fahrenheit) and a humidity range of 0 to 95 percent (noncondensing).

3.3.1.3 **Memory Expansion Board Interfaces.** The power and signal connections interfacing the memory expansion board with the mainframe are made through the printed circuit connector on the bottom edge of the card that mates with the mainframe connector when the board is inserted. The interface includes power connections and signal (TILINE) connections. The memory controller is a slave device on the TILINE.

In addition to a common ground connection, the power supply provides the following voltages to the memory expansion board:

+5V MAIN	Used for TTL logic in memory controller
-5V MEM +5V MEM +12V MEM	Used for MOS RAM (TMS 4050) Modules

The memory expansion board and TILINE interface signals include the following:

FROM MEMORY EXPANSION BOARD TO TILINE

TLTM–	-	active low during external requests if 300 ns have passed since the memory cycle began. Indicates that either read data may be strobed or address, write control and write data may be released for another request. Open Collector Output with no on-board termination. (75138)
TLMER–	-	active low indicates a memory parity error has been encountered during an external read. Open collector 3-state output with no on-board termination. (07)

FROM TILINE TO MEMORY EXPANSION BOARD

TLGO–	-	active low to initiate an external memory request. This line must go inactive between memory requests. 1 internal load (75138)
TLREAD	-	high indicates read, low indicates a write. 1 internal load (75138)

TLIORES– - active low to reset the parity latch which drives the parity LED.
1 internal load (7400)

TLADR (00-19)– - active low to control internal addressing.
1 internal load/bit

TWO-WAY DATA TRANSFER

TLDAT (00-15)– - Two-way data bus driven by 3-state bus drivers (74LS367). Enabled during an external read when the request gets accepted, i.e., EXRQ setting. Uses (74LS367) as receivers.

TLPRES– - active low prior to power down and up cycles. Used to stabilize logic in preparation for standby power condition and power up.
1 load

TLAG - Connections in board merely transfer TLAG signal through the board but do not use it (used by master devices only, memory controller is a slave device on the TILINE).

3.3.1.4 **Memory Expansion Board - Control and Operation.** The memory controller monitors the TILINE, decodes address signals on the bus, and controls the performance of read and write cycles as required by the TILINE master device. In addition, the memory controller provides for refresh cycles of the MOS memory chips to prevent loss of stored data. The parity option, if present on the board, provides an odd parity bit for each 16-bit word stored. The parity checking circuit indicates errors that occur in the storage and retrieval of 16-bit data words. The major functional circuits of the memory expansion board are shown in figure 3-51.

Address Examination. When the memory controller senses TLGO– asserted on the TILINE, it inspects the address on the TLADR lines to determine if the operation is intended for a memory address under its control. To make this determination, the memory controller compares the lower bound address from the board address switches with the TILINE address (bits 0-7) in the address decode logic to determine if the TILINE address is greater than the lower bound address.

If the TILINE address is greater than the lower bound address, the controller determines the upper bound of its memory as follows. The controller adds the memory size, hardwired into each memory board, to the lower bound address and compares the result with the TILINE address to determine if the TILINE address is less than the calculated upper bound address. If the TILINE address is within the specified bounds, the controller initiates the memory cycle requested.

The 12 least significant bits of the TILINE address are sent directly to the memory chips as the address inputs. The address decode logic decodes the 8 most significant bits of the address to generate the bank select and ADROK signals. The bank select signal enables the memory chips in the selected bank to act upon the address signals that are applied to all of the memory chips on the board.

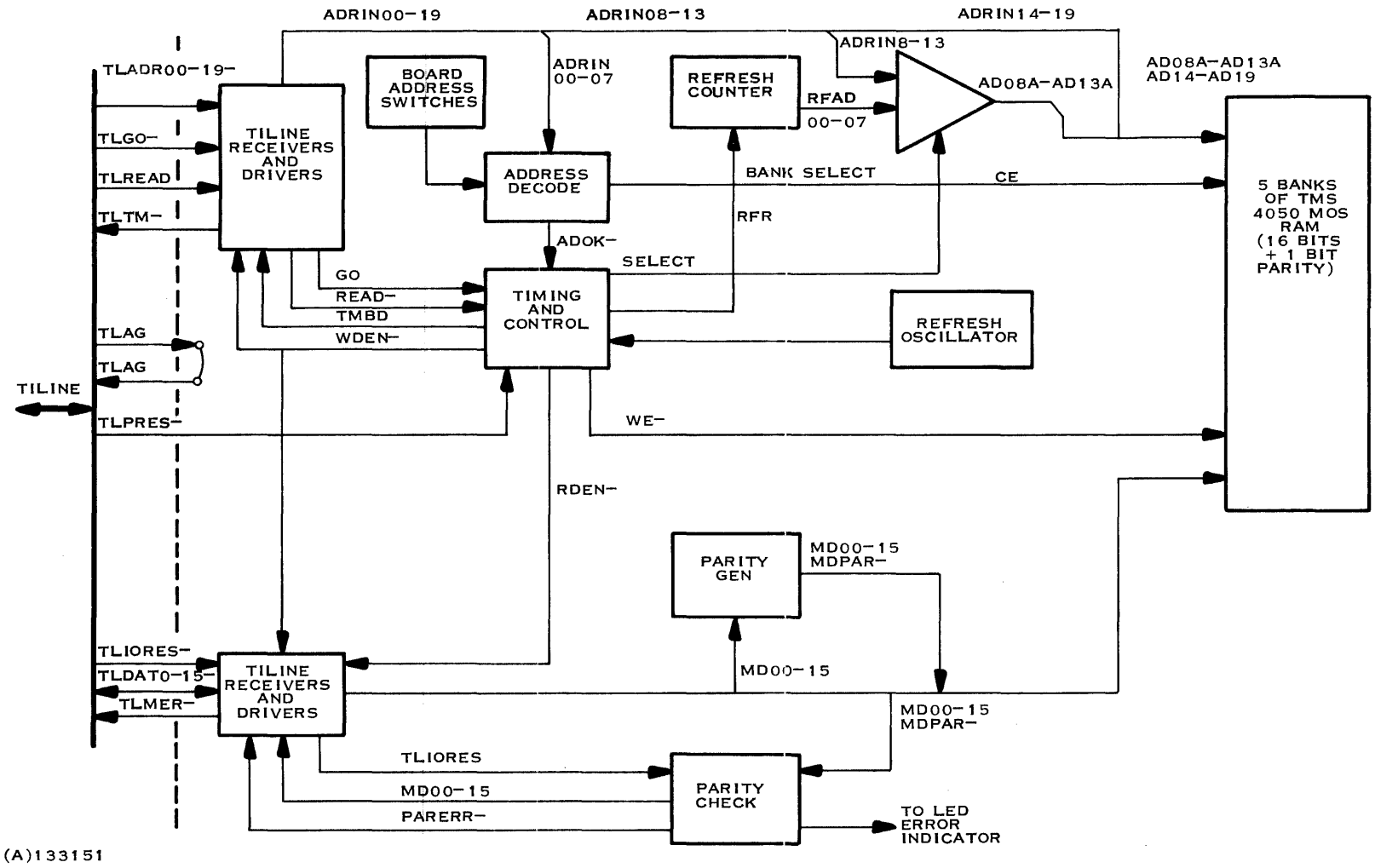


Figure 3-51. Expansion Memory Board, Block Diagram

Write Cycle. When the TLREAD signal line goes low, the controller performs a write cycle by holding the write enable (WE–) line low. The WE– line connects to all of the memory chips on the board. The controller then passes the address from the TLADR lines to the inputs of the memory banks and transfers the data bits from the TILINE to the selected memory chips for storage via the TILINE receivers that are enabled by the controller.

Read Cycle. When the TLREAD signal line goes high, and the controller has determined the address, the controller initiates a read cycle by setting the WE– line high. The memory responds with a data word plus parity bit that are supplied to the parity check logic, if parity option is implemented, as well as to the output.

Refresh Cycle. A refresh cycle is initiated every 31 microseconds to refresh the data stored in each of the 64 rows of RAM storage. This rate provides for complete refresh of the memory in approximately 2 milliseconds. The basic timing of the refresh cycle is provided by the refresh oscillator. The timing and control priority access circuit gives the refresh cycle priority over the memory requests from TILINE users but the refresh operation does not interrupt a normal read or write cycle. During the refresh operation, clock signals are produced by the timing and control circuit. These clock signals are supplied to the 6-bit refresh counter which steps through each of 64 states in order to refresh all 64 rows of memory via the address selector.

Parity Error Detection. The 16-bit word being written is applied to a parity generator (if the parity option is implemented on the board). The parity generator outputs a bit that makes the total parity count for the resulting 17-bit word odd and that bit is stored in a 8K byte chip for each implemented bank of MOS memory. During the Read operation, the parity check logic determines that the odd parity count has been retained in the 17-bit word emerging from memory. If no parity error is found, the 16 data bits are supplied to the TILINE drivers which sends them out on the bus. If a parity error is found by the parity check logic, an error signal TLMER– is sent out on the TILINE and an LED error indicator is energized. A software controlled reset signal TLIORES may be used to reset the error indicator.

3.3.2 16KB MEMORY BOARDS WITH ERROR CHECKING AND CORRECTING CIRCUIT (ECC). As previously described, a 16KB module with ECC is used as the memory board for two optional configurations of the 990/10 minicomputer (one option with mapping and the other without mapping). The same board may also be used for ECC memory expansion. The 16KB memory board with ECC has a memory controller and, whether used as the basic memory board of the minicomputer or as an expansion module, may be augmented with an add-on memory module that may contain an additional 16K, 32K, or 48K bytes of ECC memory. The add-on memory module does not have a controller but operates under control of the 16KB memory board with ECC to give a total capacity of 64K bytes of ECC memory per pair of boards. The add-on memory module includes top edge connectors for the interface to the 16KB memory board with ECC.

Error checking and correction ensures accurate storage and retrieval of data. The memory controller generates a 6-bit code during a store operation that is checked during a read operation on the data. The code enables the controller to detect and correct single-bit errors, and to detect two or more errors in each 16-bit word stored in the memory. The add-on board is shown in figure 3-52. The discussion in the following paragraphs covers physical description, performance specifications, interfaces and operation and control of the ECC memory boards with emphasis on the differences between the 16KB memory board with ECC and the memory expansion board described in paragraph 3.3.1.

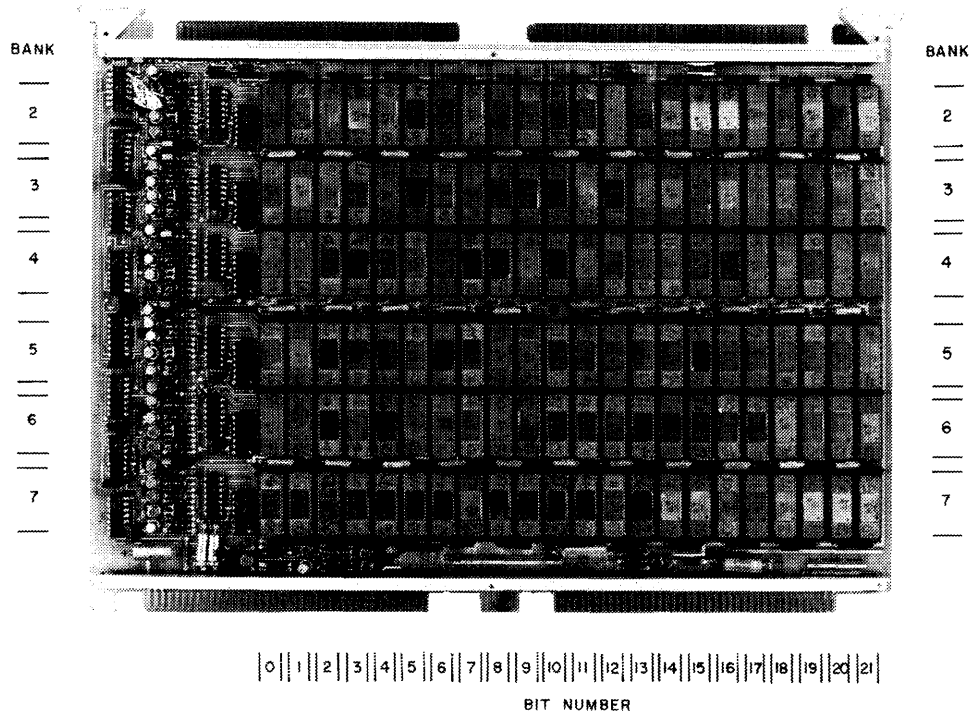


Figure 3-52. Add-on (Array) Board for the ECC Memory

3.3.2.1 **Physical Description - ECC Memory Boards and Chip.** The ECC 16KB Expansion board is a two-sided 160-pin printed circuit board that contains the controller for the 16KB of MOS RAM on the board plus the additional memory (up to 48 bytes) on the associated Add-On Board. The controller circuitry, including the Error Correcting Circuit, is implemented in the DIP packaged TTL logic on the lower part of the board shown in figure 3-53. The 16KB of on-board MOS memory is implemented in two rows of TMS 4060 devices across the top of the board. Each row of devices provides for the storage of the 22 bits required for data and error correction. The TMS 4060 device is similar to the TMS 4050 previously described. It has separate I/O terminals provided on a 22-pin dual-in-line package.

As shown in figure 3-53, the ECC 16KB Expansion Board includes two LED error indicators and two dual-in-line switch packages for controlling the operation of the board. Two light-emitting diodes, mounted next to the ejector tab on all ECC 16KB Expansion boards indicate errors that may occur during a memory cycle. The Correctable Error indicator lights when the error correcting logic detects and corrects an error in data read from memory. This indicator is not operational if the error correcting logic is disabled. The Noncorrectable Error indicator lights when the error detecting logic senses a data error that cannot be corrected (2 or more bits in error), or a data error that is not corrected because the error correcting logic has been disabled.

A dual-in-line package (DIP) containing four single-pole, single-throw switches allows the user to select or disable the error correcting logic. Switches 3 and 4 in this package perform no function. Switches 1 and 2 enable the error correcting logic when both switches are set to the ON position. These switches disable the error correcting logic when both switches are set to the OFF position. In no case should one switch be ON while the other switch is OFF, since this condition produces erroneous indications to the memory controller.

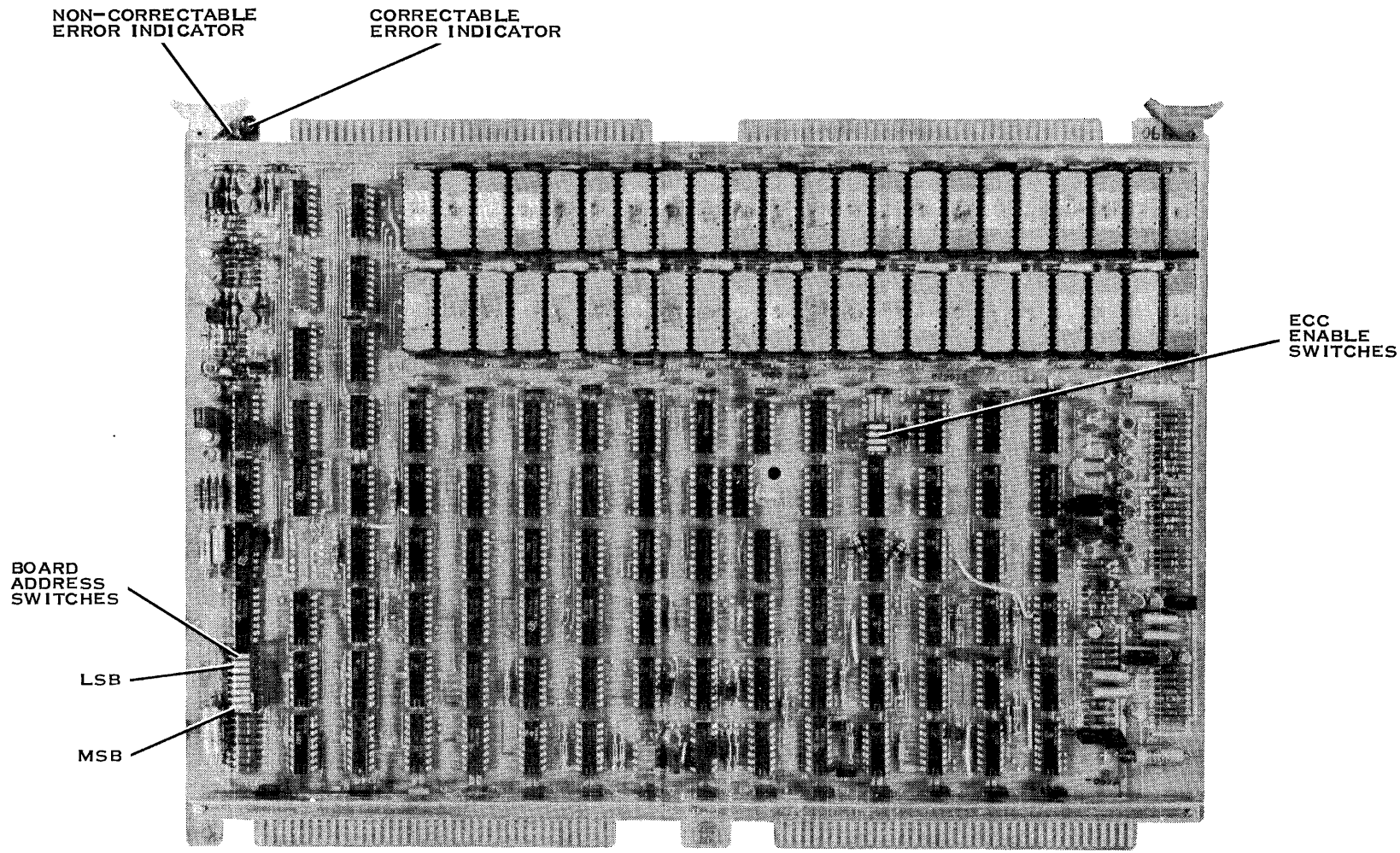


Figure 3-53. ECC 16KB Expansion Board

The starting address of the memory locations is set by switches as described in the previous paragraph on the expansion board. The required settings for the address switches are shown in table 3-13.

Table 3-13. ECC 16KB Expansion Board, Starting Address Switch Settings

Beginning Word* Address On Board ( )$_{16}$	Address Switch Setting								Number Of Memory Words Below Board
	1	2	3	4	5	6	7	8	
00000	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	0
01000	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	4,096
02000	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	8,192
03000	OFF	OFF	OFF	OFF	OFF	OFF	ON	ON	12,288
04000	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF	16,384
05000	OFF	OFF	OFF	OFF	OFF	ON	OFF	ON	20,480
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
0F000	OFF	OFF	OFF	OFF	ON	ON	ON	ON	61,440
10000	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	65,536
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
40000	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	262,144
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
F4000	ON	ON	ON	ON	OFF	ON	OFF	OFF	999,424

* The amount of addressable memory for any particular board is dependent on the configuration of the board, i.e. each dash number has a different size of addressable memory.

3.3.2.2 **ECC Memory Performance Specifications.** The typical access time for the ECC Memory is 600 ns. Access time may be increased to a maximum of 1200 ns in the presence of an interfering refresh cycle that must be performed every 31 microseconds or more often in order to assure the retention of stored data. Cycle time is dependent upon the TILINE MASTER and is typically about 225 ns longer than the memory access time. In the event of main power failure, standy power from a battery included in the mainframe prevents loss of stored data for at least 30 minutes. The ECC Memory operates within specifications over a temperature range of) to 65 degrees Celsius (32 to 149 degrees Fahrenheit) and a humidity range of 0 to 95 percent (noncondensing).

3.3.2.3 **ECC Memory Interfaces.** The ECC 16KB Expansion Board and the Add-On Board interface with the TILINE in the same manner as that described in the previous paragraph on the Memory Expansion Board. The ECC 16KB Expansion Board also interfaces with the Add-On Board if more than 16KB of memory is required of a given set of boards. The Add-On Board in each set receives data, address and control signals from the associated control board through a printed circuit memory interconnect board (PN 944986-0001) that connects the boards together at the top edges. The interface signals between the Add-On and ECC 16KB Expansion boards are described in table 3-14.

3.3.2.4 **ECC Memory Boards - Control and Operation.** A block diagram of the ECC memory system appears in figure 3-54. As may be seen from the figure, the operation of the controller and the on-board 16K bytes of ECC memory is similar to that described earlier for the Memory Expansion Board. The address decoding must take into account the installed capacity of the Add-On Board in determining the address bounds for the set of ECC memory boards as described earlier. Refresh control signals are supplied to the Add-On Board where they perform functions like those performed on the ECC 16KB Expansion Board. The Read and Write cycles are similar to those previously described except that they involve the Error Correcting Circuit in the manner described below.

Write Cycle and Error Correcting Code Generation. The 16-bit data word is applied to the error code generator at the same time that it is written into the MOS dynamic memory. The error code generator supplies a 6-bit code that is a modified Hamming code for error detection and correction that is also written into memory. Each bit in the error correcting code is an odd parity bit for selected bits of the 16-bit data word. As shown in figure 3-55 bit C0 parity checks bit 0 through 8 in the data word. Each bit in the data word is parity checked by three or five bits of the error correcting code.

Read Cycle and Error Detection and Correction. On the Read cycle, the 16-bit data word is again applied to the error code generator which outputs another 6-bit error code as before. If a 1-bit error occurs in the 22-bit word read from memory, the error code generated on the Read cycle does not match that generated (and stored in memory) on the Write cycle. Comparing the error correcting code bits that change permits the location of the bit that is in error. As indicated in figure 3-55, data word errors produce three or five mismatched error code bits. A code bit error is indicated by a single bit mismatch. The 16-bit data word read from memory is applied to the error correction circuit along with an error bit from the error code compare circuit so that single-bit errors are corrected before the data word is supplied to the TILINE. The correctable error LED indicator on the memory board is also energized. If two or more bits are in error, the error cannot be corrected. For even numbers of errors, the memory controller error code compare circuit generates a TLMER– signal that is sent to the TILINE device to indicate the existence of such an error. The noncorrectable error indicating LED is also energized. An

Table 3-14. ECC 16KB Expansion Board to Add-On Board Interface Signals

Signature	Pin No.	Definition
MDO00–	P4-51	Memory read data output from Add-On Board to ECC 16KB Expansion Board
MDO01–	P4-43	
MDO02–	P4-35	
MDO03–	P4-27	
MDO04–	P4-19	
MDO05–	P4-13	
MDO06–	P4-09	
MDO07–	P4-05	
MDO08–	P4-04	
MDO09–	P3-75	
MDO10–	P3-71	
MDO11–	P3-63	
MDO12–	P3-55	
MDO13–	P3-47	
MDO14–	P3-39	
MDO15–	P3-31	
C0OUT–	P3-23	Error correcting code output signals from Add-On Board during Read operation
C1OUT–	P3-17	
C2OUT–	P3-13	
C3OUT–	P3-09	
C4OUT–	P3-05	
C5OUT–	P3-04	
MDI00	P4-53	Memory write data inputs from ECC 16KB Expansion Board to Add-On Board.
MDI01	P4-45	
MDI02	P4-37	
MDI03	P4-29	
MDI04	P4-21	
MDI05	P4-15	
MDI06	P4-11	
MDI07	P4-07	
MDI08	P4-03	
MDI09	P3-77	
MDI10	P3-73	
MDI11	P3-65	
MDI12	P3-57	
MDI13	P3-49	
MDI14	P3-41	
MDI15	P3-33	
C0IN	P3-25	Error correcting code inputs to Add-On Board during write operation.
C1IN	P3-19	
C2IN	P3-15	
C3IN	P3-11	
C4IN	P3-07	
C5IN	P3-03	

Table 3-14. ECC 16KB Expansion Board to Add-On Board Interface Signals (Continued)

Signature	Pin No.	Definition
ADR08 ADR09 ADR10 ADR11 ADR12 ADR13 ADR14 ADR15 ADR16 ADR17 ADR18 ADR19	P4-67 P4-61 P4-69 P4-73 P4-77 P4-75 P4-57 P4-55 P4-59 P4-65 P4-63 P4-71	Least significant 12 bits of address from TILINE bus used as a store or fetch address when accessing a memory location. The most significant 6 bits of this address can also be generated internal to the controller for use during refresh cycles.
DECODEA DECODEB DECODEC	P4-78 P4-76 P4-74	A 3-bit code that indicates which bank (0-7) of memory chips is to be cycled. DECODEA is the least significant and DECODEC is the most significant bit of the code.
XMEM4– XMEM8– XMEM16–	P3-27 P3-29 P3-21	A 3-bit complement code, hardwired in the Add-On Board, that designates to the memory controller the size of the memory contained on the Add-On Board. Valid codes are: XMEM 16- 8- 4- 1 0 1 16KB memory 0 1 1 32KB memory 0 0 1 48KB memory
START	P4-70	Initiates a memory cycle in the Add-On Board
RFACC–	P4-68	When coincident with START, this signal initiates a refresh cycle in the Add-On Board
READ	P4-64	When a logic one, this signal indicates that a read cycle is to be performed from the address on the ADR__ lines. When this line is a logic zero, the Add-On Board performs a write operation.
PWRON	P3-37	When a logic one, this signal applies +5 Vdc to the Add-On Board logic; when a logic zero, this signal removes power from the logic.
PWRONA	P4-66	This signal is a logic zero during power on or off transitions and disables the clock input to the memory chips to prevent voltage spikes from affecting the memory chips. During normal power conditions, this signal is a logic one.
ERROR–	P3-67	A low active signal that indicates a noncorrectable error in data from the Add-On Board and lights an LED on the Add-On Board to indicate that condition.
CERR–	P3-43	A low active signal that indicates a corrected error in data from the Add-On Board. This signal also lights an LED on the Add-On Board to indicate that condition.
DECENB	P4-72	A high active signal that enables the Add-On Board to decode the DECODEA,B,C lines to set an 8KB bank of memory on the Add-On Board.

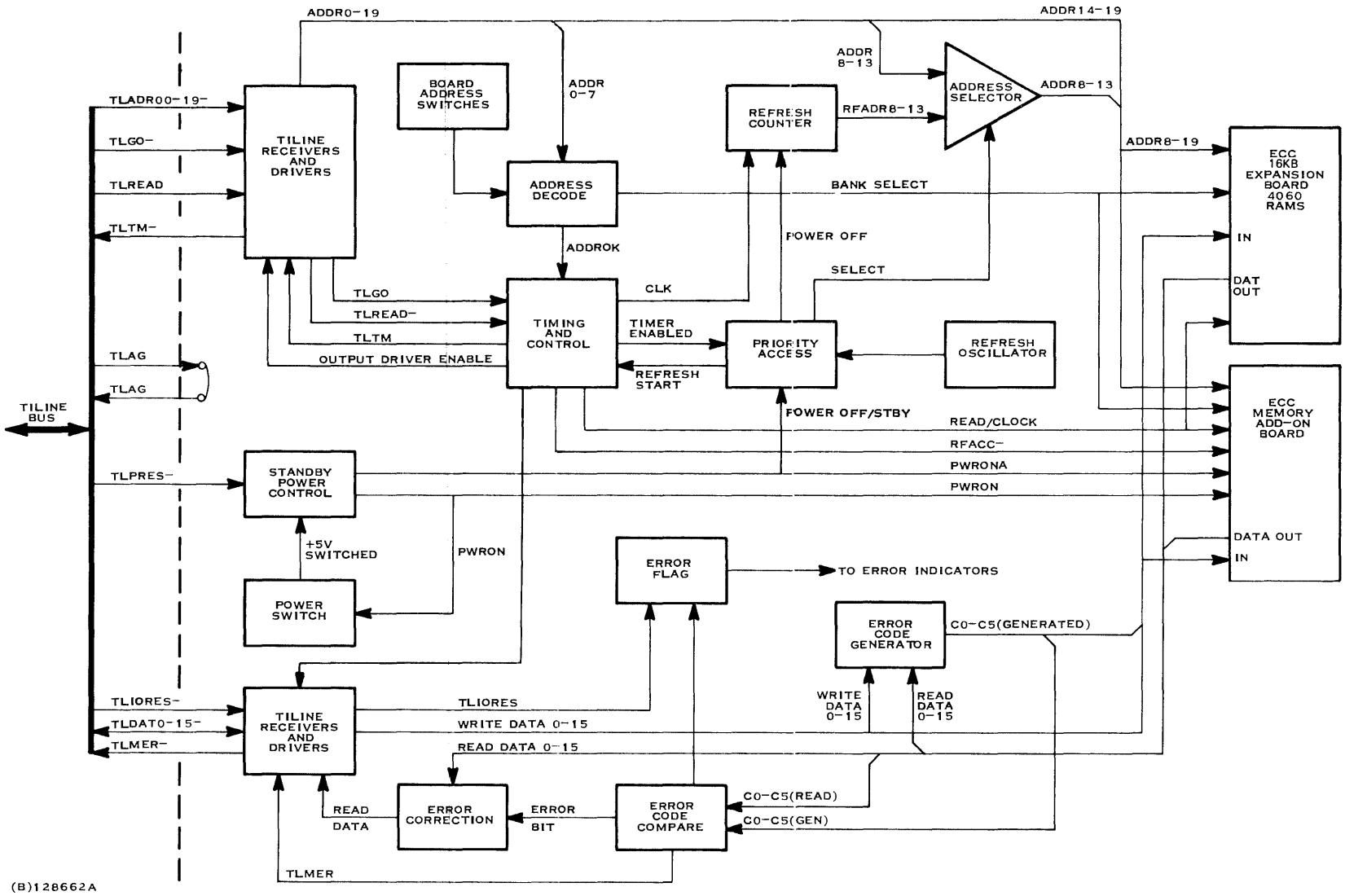


Figure 3-54. ECC Memory System Block Diagram

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DATA BIT / CHECK BIT
							X	X	X	X	X	X*	X	X	X	C0
X		X		X		X	X	X		X		X*		X		C1
X	X			X	X			X	X			X*	X			C2
X	X	X	X					X	X	X	X					C3
X	X	X	X	X	X	X	X								X	C4
X			X		X	X		X			X		X	X	X	C5

*BITS C0,C1, AND C2 MISMATCHED INDICATES DATA BIT 3 IN ERROR.

(A)128663

Figure 3-55. Error Correcting Code Bit Pattern

odd number of errors (greater than 1) produces the same result as a single-bit error except that the errors are not corrected. If the ECC logic is disabled by the switches on the board, every error generates a TLMER– signal and energizes the noncorrectable error indicator.

Standby Operation When Power Fails. The dynamic MOS memory chips lose the data stored in them unless refresh cycles, requiring power, are performed. A battery in the mainframe supplies power to prevent loss of stored data. When main power begins to fail, the priority access circuit resets the refresh counter and, following completion of a memory cycle in progress, begins a series of 64 refresh cycles in succession to ensure that memory data is maintained. When the last refresh cycle is complete, the controller sets a timer and turns off power to all memory control logic to conserve battery power. The timer is temperature-dependent such that at higher temperatures the time span is shorter than at lower (room) temperatures. When the timer times-out, it switches power back to the control circuits, resetting the refresh counter. The controller then initiates another 64 memory refresh cycles, sets the timer at the completion of the refresh period, and shuts off power to the control logic. This process continues until main power returns. When main power returns, the memory control logic is off and the controller does not respond to the return of main power. When the timer times-out, the controller performs 64 refresh cycles. However, TLPRES– from the power supply is now high, indicating that power has been restored. This signal prevents the controller from switching logic power off, so that the controller remains active and ready for the first memory request. The temperature-sensitive timer spaces the refresh cycles during standby to ensure that the memory is maintained without needless refresh cycles (decay rate of the memory is also temperature-dependent in a ratio similar to the timer). The refresh rate decreases from approximately 2 milliseconds at 70 degrees Celsius (158 degrees Fahrenheit) to about 20 milliseconds at room temperature to conserve the standby battery.

3.3.3 MEMORY CONTROLLER, 96KB, WITH ERROR CHECKING AND CORRECTING (ECC) 990/16KR. The 96KB memory controller is a multilayered printed circuit board in standard and fine line versions. It contains the memory control logic and storage elements for up to 96K bytes of MOS RAM on the board, and the control logic for up to 1M bytes of additional memory on associated add-on memory expansion boards. The 96K memory controller functions as a TILINE slave device and generates or accepts data only in response to a TILINE master device.

The board interface to the TILINE bus is effected through the two 80-pin connectors at the bottom edge of the board that installs in the computer or expansion chassis. Two 50-pin connectors at the top edge of the board are used to interface with expanded memory. The TILINE bus and expanded memory interface lines are as shown in figure 3-56. Table 3-15 describes the functions of these interface lines.

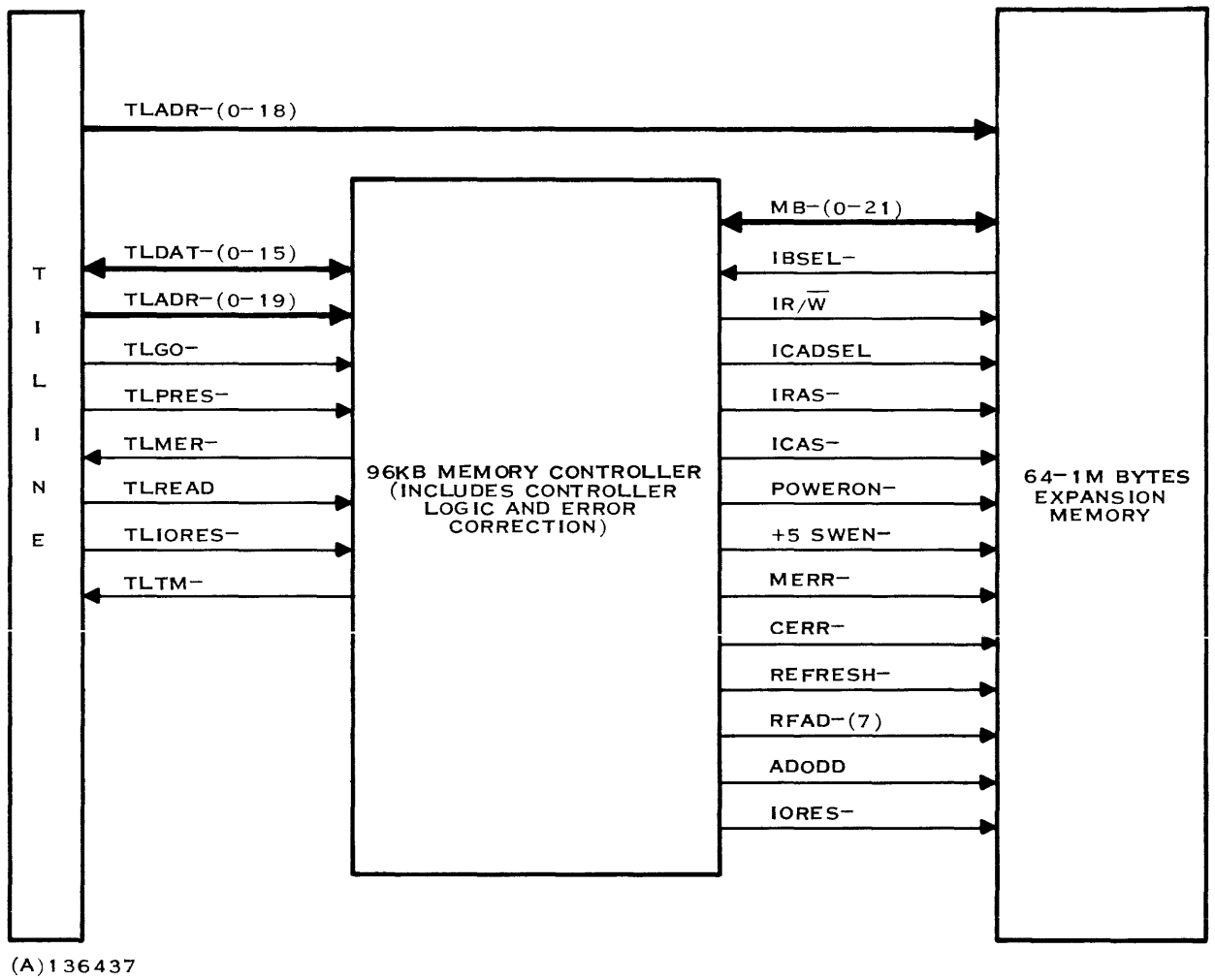


Figure 3-56. ECC 96KB Memory Controller TILINE and Add-on Memory Interface Diagram

Table 3-15. Memory Controller to 256KB Add-On Memory Interface Signals

Signature	Pin No.	Definition
MB00—	P4-1	22-bit bidirectional data bus that transfers read and write data between the two boards (includes six check bits, MB16— through MB21—).
MB01—	P4-3	
MB02—	P4-5	
MB03—	P4-7	
MB04—	P4-9	
MB05—	P4-11	
MB06—	P4-13	
MB07—	P4-15	
MB08—	P4-17	

Table 3-15. Memory Controller to 256KB Add-On Memory Interface Signals (Continued)

Signature	Pin No.	Definition
MB09—	P4-19	
MB10—	P4-21	
MB11—	P4-23	
MB12—	P4-25	
MB13—	P4-27	
MB14—	P4-29	
MB15—	P4-31	
MB16—	P4-33	
MB17—	P4-35	
MB18—	P4-37	
MB19—	P4-39	
MB20—	P4-41	
MB21—	P4-43	
IBSEL—	P3-19	Board Selected Signal. The select signal is sent to the 96KB memory controller when the 256KB add-on memory board decodes a TILINE address that falls in the address space defined by the address switches and memory size jumpers.
IR/W—	P3-21	Read-Write control. The read-write control line to the 256KB add-on memory board specifies either a read or write operation.
ADODD	P3-29	Odd-Word Address. The address odd line operates in conjunction with the read-write control line to enable both rows in a selected bank during a read operation or to enable only the required odd or even row during a write operation.
IRAS—	P3-13	Row-Address Strobe. The row-address strobe clocks seven row-address bits into the memory chips.
ICADSEL	P3-7	Column-Address Select. The column-address select line causes the second seven address bits to be applied to the memory chips.
ICERR	P3-9	Correctable Error, One-Bit Error Detected. The correctable error signal is generated by the control logic of the 96KB memory controller during a read cycle to indicate that a one-bit error has occurred and sets the error indication lamp on the selected 256KB add-on memory board.
ICAS—	P3-15	Column-address Strobe. Column-address strobe clocks the seven column-address bits into the memory chips.
RFAD0—	P3-27	Refresh Address Lines. Refresh address lines provide the row address to the memory chips during a refresh operation.
RFAD1—	P3-33	
RFAD2—	P3-17	
RFAD3—	P3-35	
RFAD4—	P3-25	
RFAD5—	P3-23	
RFAD6—	P3-31	

Table 3-15. Memory Controller to 256KB Add-On Memory Interface Signals (Continued)

Signature	Pin No.	Definition
REFRESH—	P3-5	Refresh Cycle in Progress. The refresh control line causes the refresh address lines to be applied to the memory chips that are then strobed into the memory chips by the IRAS— pulse.
+5SWEN—	P3-1	5-volt Switch Enable. Turns on 5 volts of power to 256KB add-on memory whenever main power is on, or during a refresh operation when in standby operation.
POWERON—	P3-11	Power-On. Power-on is true after 5 volts is stable. When false, this signal inhibits extraneous strobes to the memory chips.
IORES—	P3-37	I/O Reset. The reset line resists the error indication lamps after initial power-up and in response to a front panel reset or execution of a reset instruction.
IMERR—	P3-3	Memory Error, Multibit Error. Memory is generated by the control logic of the 96KB memory controller during a read cycle and sets the error indication lamp on the selected 256KB add-on memory board.

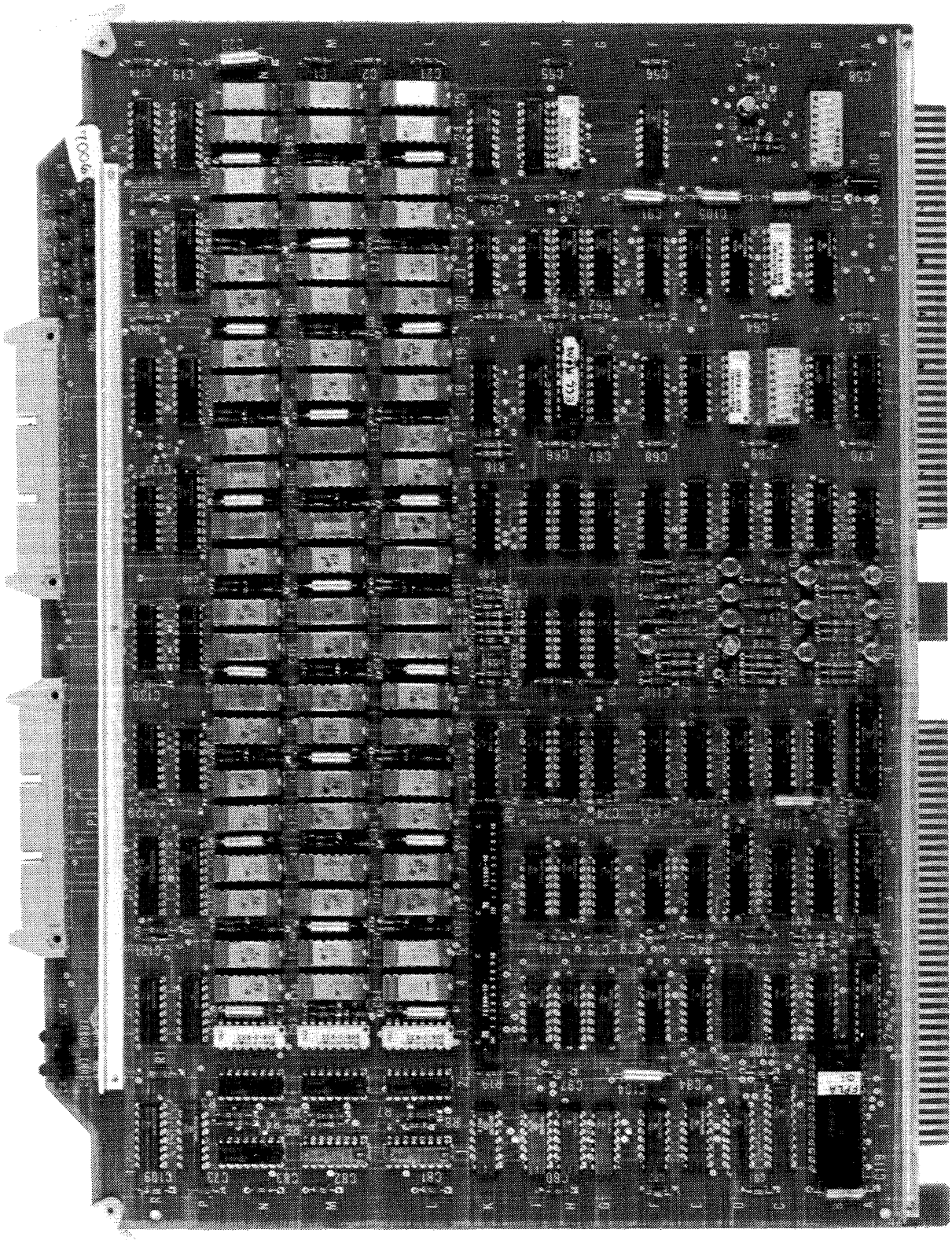
Memory capacity can be expanded by an additional 1M bytes with the addition of four 256K byte add-on memory expansion boards.

The control logic consists of TILINE interface logic, timing and memory refresh control circuits, and error checking and correction circuits. The memory array consists of from zero to three banks (rows) of memory chips with 22 memory chips in each bank. Each memory word consists of 16 data bits and six check bits. During normal operation, only the data bits are processed on the TILINE data bus. The 96KB memory controller may be operated in a diagnostic mode through its user-selected TILINE Peripheral Control Space (TPCS) address. In the diagnostic mode, the six check bits are processed over the data bus and the MSB of the data word is stored in the check bit area.

Cycle control and refresh control for the add-on memory expansion boards are provided by the 96KB memory controller but the add-on memory expansion boards interface directly with the TILINE for address selection.

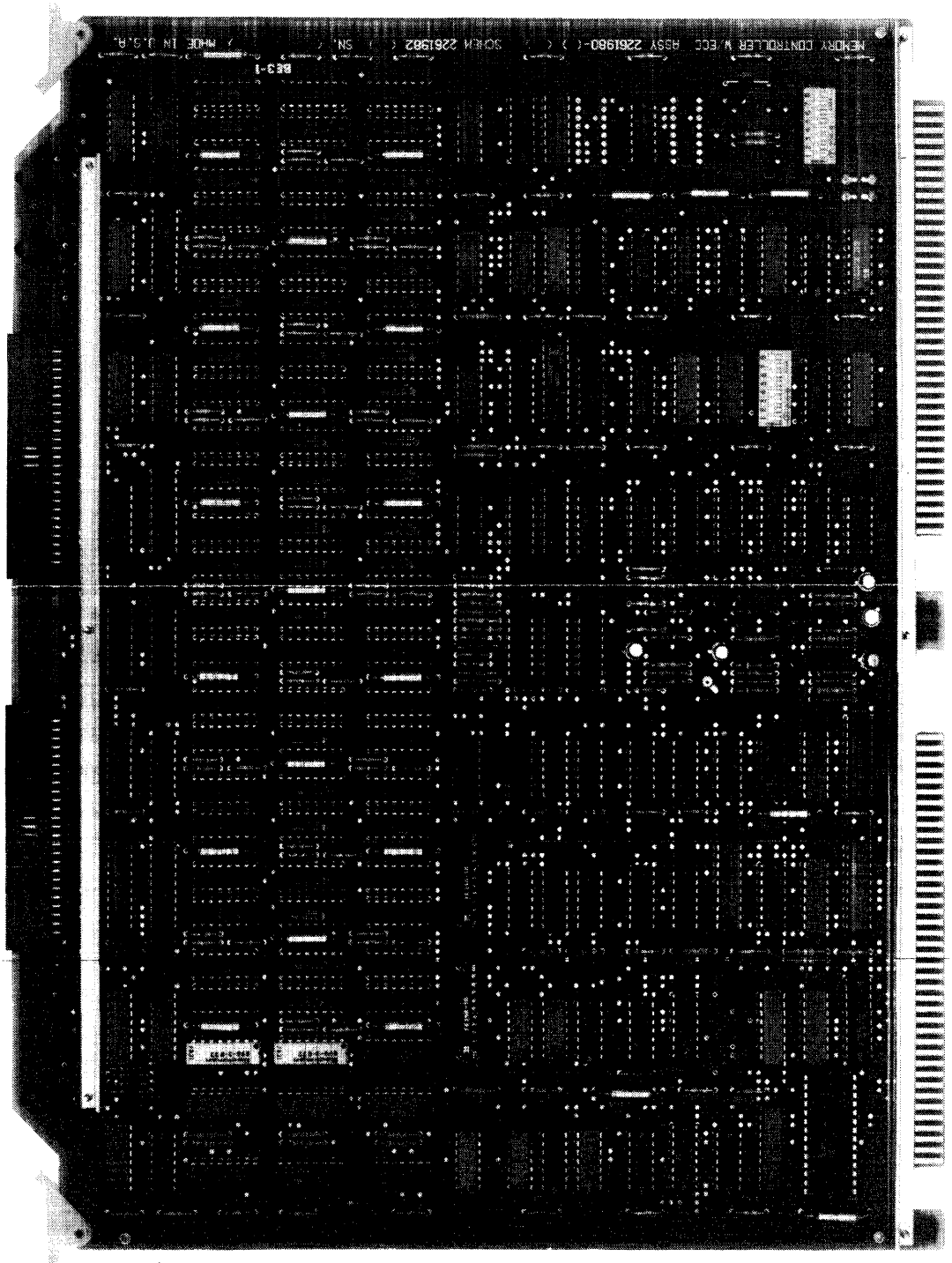
3.3.3.1 96KB Memory Controller Physical Description. The 96KB memory controller circuitry, including the error checking and correcting circuits, is implemented in TTL devices on the lower half of the board as shown in figure 3-57. The 96K bytes of on-board MOS memory consist of three rows of TMS 4116 devices across the top of the board. Each row includes the 22 devices required for the storage of 16 data bits and the six error checking bits. The TMS 4116 chip is organized as 16,384 one-bit words housed in a 16-pin dual-in-line package. The chip is based on N-channel silicon-gate technology and the inputs and outputs are TTL compatible.

As shown in figure 3-57, the 96KB memory controller includes two light emitting diode (LED) error indicators, eleven LED chip failure indicators, and two dual-in-line switch packages. The two error indicating LEDs indicate that a one-bit (correctable) error or a multibit (uncorrectable) error has occurred on this board. The correctable error LED lights when the error correcting logic detects and corrects an error in data read from memory. The memory error LED lights when the error detecting logic senses a data error that cannot be corrected (two or more bits in error).



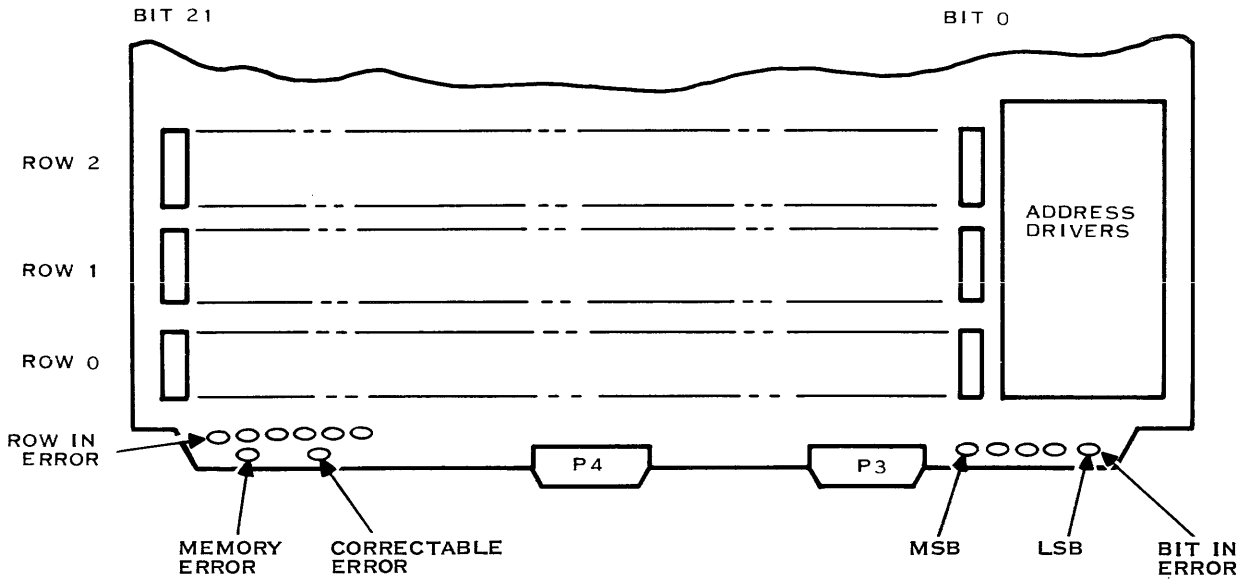
(A)140377

Figure 3-57. 96KB Memory Controller Board, Standard Version

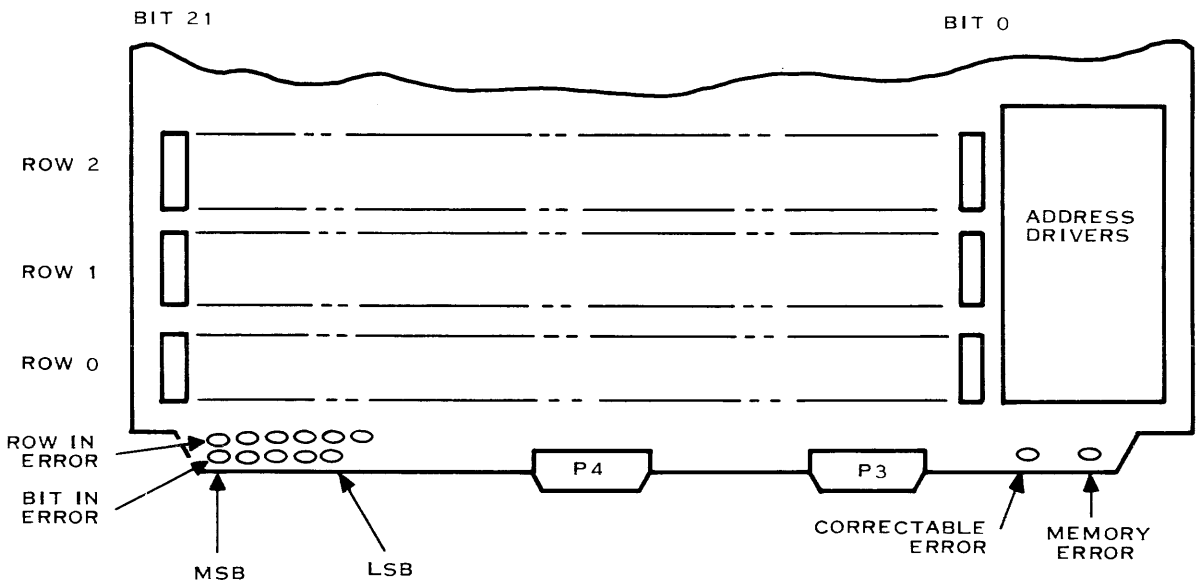


(A)143784

Figure 3-57A. 96KB Memory Controller Board, Fine Line Version



FINE LINE VERSION



STANDARD VERSION

(A)143783

Figure 3-58. 96KB Memory Board Error Indicators

These lamps are set on the first occurrence of the respective error stimulant and remain set until the board is powered down or until an I/O reset instruction is issued.

The additional eleven chip failure indicators pinpoint the memory chip that caused the first single-bit error. The eleven chip failure indicators are divided into two groups as shown in figure 3-58. A group of five form a binary code that identifies the bit that failed. The remaining six LEDs form a binary code that identifies the row that contains the failing chip. Additional errors do not affect these indicators but are recorded by the two error indicators located on each add-on memory expansion board. Table 3-16 summarizes the error indicators and their functions.

Each of the dual-in-line switches consists of eight single-pole, single-throw, push-type switches. One switch package is used to set the 96KB memory controller on-board memory starting address. The other switch contains the TPCS address of the board.

The memory starting address switches correspond to the eight most significant bits of the 20-bit TILINE address and permit board starting address selection in 8K-byte increments. Switch 1 is the most significant bit of the address and switch 8 is the least significant bit of the address. Table 3-17 lists the required switch settings for memory board beginning word addresses. Addresses other than those shown can be represented in a similar manner using the eight switches to represent the binary number. Since each of the three rows of memory devices represents 32K bytes of memory, the memory capacity is either 0, 32K, 64K, or 96K bytes. Memory size is set by connecting jumpers across the terminals of J9 and J10 as shown in table 3-17. The diagnostic mode pencil switches correspond to address bits 11 through 18 of the 20-bit TILINE address bus and select the TPCS address that is used to operate the controller in the diagnostic mode. Switch 1 is the most significant bit and switch 8 is the least significant bit of the TPCS address segment. This permits 512 addresses to be selected that fall between hexadecimal F800 and FBFE inclusive in the 15-bit address form and between hexadecimal FFC00 and FFDFF inclusive in the 20-bit address form. The 20-bit address is generated in the address development process as described in paragraph 3.2.9.1. Table 3-18 lists several example TPC addresses and corresponding switch settings.

Table 3-16. Description and Function of 96KB Memory Board Error Indicators

Indicator	Description	Display Convention
Bit In Error	Hexadecimal Code 00 = Bit 0 . . 0F = Bit 15 . . 15 = Bit 21	LED On: Bit = 1
Row In Error	Hexadecimal Code 00 = Row 0 01 = Row 1 02 = Row 2 . . 22 = Row 34	LED On: Bit = 1
Memory Error	Multibit error on this board	LED On: Error
Correctable Error	Single bit error on this board	LED On: Error

3.3.3.2 **TMS 4116 Memory Chip.** The TMS 4116 memory chip is a monolithic, high-speed, dynamic, 16,384-bit MOS RAM organized as 16, 384 one-bit words. All inputs and outputs are compatible with TTL logic including the clocks: Row Address Strobe (RAS–) and Column Address Strobe (CAS–). The seven address lines and the data-in (DI) lines are latched on the chip to simplify system design. The data out (DO) line is unlatched to allow greater system flexibility. To decode 1 of 16,384 storage cell locations, 14 address bits are required. To achieve this, seven row-address bits are set up on the seven address lines and latched onto the chip by RAS–. Then in this system, a column address select (CADSEL–) signal applies the seven column address bits to the seven address lines. The CAS– strobe latches the column address bits onto the chip. A refresh operation must be performed at least every two milliseconds to retain data. Each of 128 row addresses is strobed with RAS– to cause all bits in each row to be refreshed. Since the output buffer is in the high-impedance state unless CAS– is applied, the RAS– only refresh sequence avoids any output during refresh. CAS– remains high (inactive) for this refresh sequence, thus conserving power.

Table 3-17. Address Switch Settings and Memory Size Jumpers for 96KB Memory Controller

Beginning Word Address On Board ( )$_{16}$	1	2	3	4	5	6	7	8	Number of Memory Words Below Board
00000	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	0
01000	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	4,096
02000	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	8,192
03000	OFF	OFF	OFF	OFF	OFF	OFF	ON	ON	12,288
04000	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF	16,384
05000	OFF	OFF	OFF	OFF	OFF	ON	OFF	ON	20,480
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
0F000	OFF	OFF	OFF	OFF	ON	ON	ON	ON	61,440
10000	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	65,536
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
40000	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	262,144
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
F4000	ON	ON	ON	ON	OFF	ON	OFF	OFF	**999,424**

Memory Size	Jumper J9	Jumper J10
0	OFF	OFF
32KB	OFF	ON
64KB	ON	OFF
96KB	ON	ON

Table 3-18. Example TPCS Address Switch Settings and Their Corresponding TPCS Addresses TPCS Addresses

CPU ADDRESS	TPCS ADDRESS	SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8
F800-02	FFC00-01	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
F804-06	FFC02-03	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
F81C-1E	FFC0E-0F	OFF	OFF	OFF	OFF	OFF	ON	ON	ON
F820-22	FFC10-11	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
F9FC-FE	FFCFE-FF	OFF	ON	ON	ON	ON	ON	ON	ON
FA00-02	FFD00-01	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
FBFC-FE	FFDFE-FF	ON	ON	ON	ON	ON	ON	ON	ON

3.3.3.3 **Control and Operation.** The 96KB memory controller monitors the TILINE, decodes addresses on the TILINE address bus, and directs the performance of read and write cycles under control of a TILINE MASTER device to addressed memory. This addressed memory can be on board or located on add-on expansion boards. The following functional description is keyed to the block diagram for the memory board (figure 3-59).

Memory Timer. Pulses used to control the timing and sequence of operation during memory read and write operations are provided by the memory timer. This includes timing for the memory refresh cycle that is a memory read operation. The memory timer consists of two resistance/capacitance timers and two 250-nanoseconds delay lines along with associated TTL logic. Each 250-nanoseconds delay line has 10 output taps that are separated from each other in time by 25 nanoseconds. An input signal to the delay line is propagated down the line and is reproduced at each output tap with each progressive tap introducing an additional 25 nanoseconds of delay to the input signal. The delayed by 250-nanoseconds output of the first delay line is the input to the second delay line providing a total delay of 500 nanoseconds.

Reference is made to the simplified functional diagram for the memory timer in the following discussion of the operation of the timer (figure 3-60). When the 96KB memory controller is not busy with a previous memory operation nor a refresh operation, the asserted TLGO– from the MASTER device provides a high BTLGO to trigger the two RC timers that in turn generate the GO120 and GO170 pulses at approximately 120 and 170 nanoseconds after the asserted TLGO–. GO120 clocks a flip-flop to generate the row address strobes for both on-board use and for add-on memory expansion board use. With either the 96KB memory controller or add-on memory addressed, the low board selected signal, BSEL–, is clocked by GO170. A high BSEL– signal produces the low ENDCYC– signal to abort the cycle. Assuming a valid address is presented to the local memory or to an add-on memory expansion board, as BUSY goes high (at time T170 after TLGO– is asserted), a high pulse is clocked into the input of the first of the two delay lines. At the time T270, a pulse that is delayed by 100 nanoseconds from GO170 is used to reset the flip-flop at the input to the delay line. This 100-nanoseconds wide pulse propagates down the delay lines providing the various delayed pulses as shown in figure 3-60.

Address Examination. The TILINE address, consisting of address bits TLADR00– through TLADR19–, is presented to the 96KB memory controller at the time TILINE GO (TLGO–) is asserted by the TILINE MASTER device. The eight most significant bits, TLADR00– through TLADR07–, are applied to an adder circuit where the starting address of the board as set by the start address switches on the board is in effect subtracted and resultant output bits ADR00– through ADR07– are generated. With the board not busy (CADSEL– is high), address bits ADR00– through ADR05–, and the output of two memory size jumpers are enabled as inputs to the board/bank address decoder. A valid address presented to the board/bank address decoder (that is, a preprogrammed logic array) develops a low board selected signal, SEL–, and a high at one of the three BANK signals. At approximately 170 nanoseconds after TLGO– is asserted and with the board selected, the GO170 output from the board timer clocks BUSY high and the memory read or write cycle operation is continued. If the address is not valid for the board nor for any add-on memory board, BUSY remains low and a high BSEL– signal ANDed with GO170 produces a low ENDCYC– to abort the cycle as previously described. Output bits of the address subtractor ADR06– and ADR07– along with TILINE address bits TLADR08– through TLADR12– are applied as the row address inputs to the row/column address select circuit. Address bits TLADR13– through TLADR19– are the column address inputs to the row/column address select circuit. With no refresh operation in progress, the row address inputs are latched onto the memory chips in the addressed bank as the row address strobe, RAS, is clocked high by the GO120 output from the memory timer. The GO170 output from the memory timer clocks CADSEL– low and the column address inputs to the row/column address select are selected for output to the memory chips. The T220 output from the timer clocks the column address strobe CAS high to latch the column address bits onto the memory chips in the address bank.

Memory Write Cycle. To execute a write to memory cycle, the TILINE master device asserts TLGO– and at the same time asserts the write command TILINE READ (TLREAD) by setting both signals low. TLREAD causes the read/write input to the memory devices to go low thereby placing the board in the write mode. The MASTER also generates valid write data on the data bus (TLDAT–) and a valid 20-bit address (TLADR–) on the address lines. The asserted TLGO– triggers the memory timer and after 120 nanoseconds GO120 is generated to clock row address strobe (RAS) high and to also provide the row address strobe, IRAS–, for the add-on memory expansion boards. RAS is ANDed with the selected bank signal to provide a low row address strobe that latches the seven row address bits onto the selected bank of memory devices. A delayed strobe output from the memory timer, GO170, is used to interrogate the results of address decoding on the 96KB memory controller and on the add-on expansion boards. With a valid address decoded, the low BSEL– clocked by GO170 generates a high BUSY signal. The high BUSY signal clocks a 100-nanoseconds wide pulse that is applied to the input of a 500-nanosecond delay line. The effect is that the delay line is activated at time T170 (nanoseconds) after TLGO– is asserted.

At time T170, column address select signal CADSEL– is clocked low and the column address bits are selected for application to the addressed bank of memory devices. The column address strobe, CAS, is clocked high by T220 to strobe the column address bits, the 16 data bits, and the six check bits that are generated by check logic on the board into the selected memory bank. Also generated at this time is the column address strobe for add-on memory, ICAS–. For a memory write cycle, the T345 output from the memory timer ANDed with a high READ– signal generates the TILINE terminate signal TLTM– for transmission to the TILINE interface. The time from receipt of the asserted TLGO– to the transmission of TLTM– is typically 370 nanoseconds. However, the time for a memory write cycle, the time from the beginning of a write cycle until a new memory cycle can begin, is typically 450 nanoseconds. TLGO– can be asserted by the master device before then but will be ignored until the memory busy signal is released. The positive transition of TCYC generated by the memory timer occurs at time T470 to signal the completion of the memory write cycle by changing the state of the flip-flop that generates the BUSY signal.

Memory Read Cycle. To execute a memory read cycle, the TILINE master device asserts TLGO– low and TLREAD high. TLREAD generates a high at the read/write input to the memory devices thereby placing the memory board in the read mode.

The master also generates a valid address on the address lines. The address is decoded and interrogated, the row address strobe (RAS), column address select (CADSEL–), and the column address strobe (CAS) are generated and used in the same manner as was described for the memory write cycle. With the memory board addressed and in the read mode, the low RSEL– signal enables the 16 output data bits from the addressed memory through three-state buffers and latches. Each data bit is applied as one input to an exclusive-OR gate. Similarly, RSEL– enables six check bits to the error detect logic. RENAB–, clocked low by time T370 pulse output from the memory timer, enables the 16 data bits onto the data bus. However, data is not valid to the master device until TLTM– is asserted by the memory board. With no error detected, at time T445 the TACC output from the memory timer ANDed with the high ERROR– signal asserts TLTM– low. The master device accepts data as valid and releases TLGO–. A detected and correctable error generates an output from the error detect logic that is applied to the other input of the exclusive-OR gate for the data bit in error to change the sense of that data bit thereby correcting the error. At the same time the ERROR– signal driven low inhibits the assertion of the valid data signal, TLTM–, the MASTER device. After an appropriate delay to permit data correction, the positive transition of the TCEER output from the memory timer at time T520 to assert TLTM– to the master device.

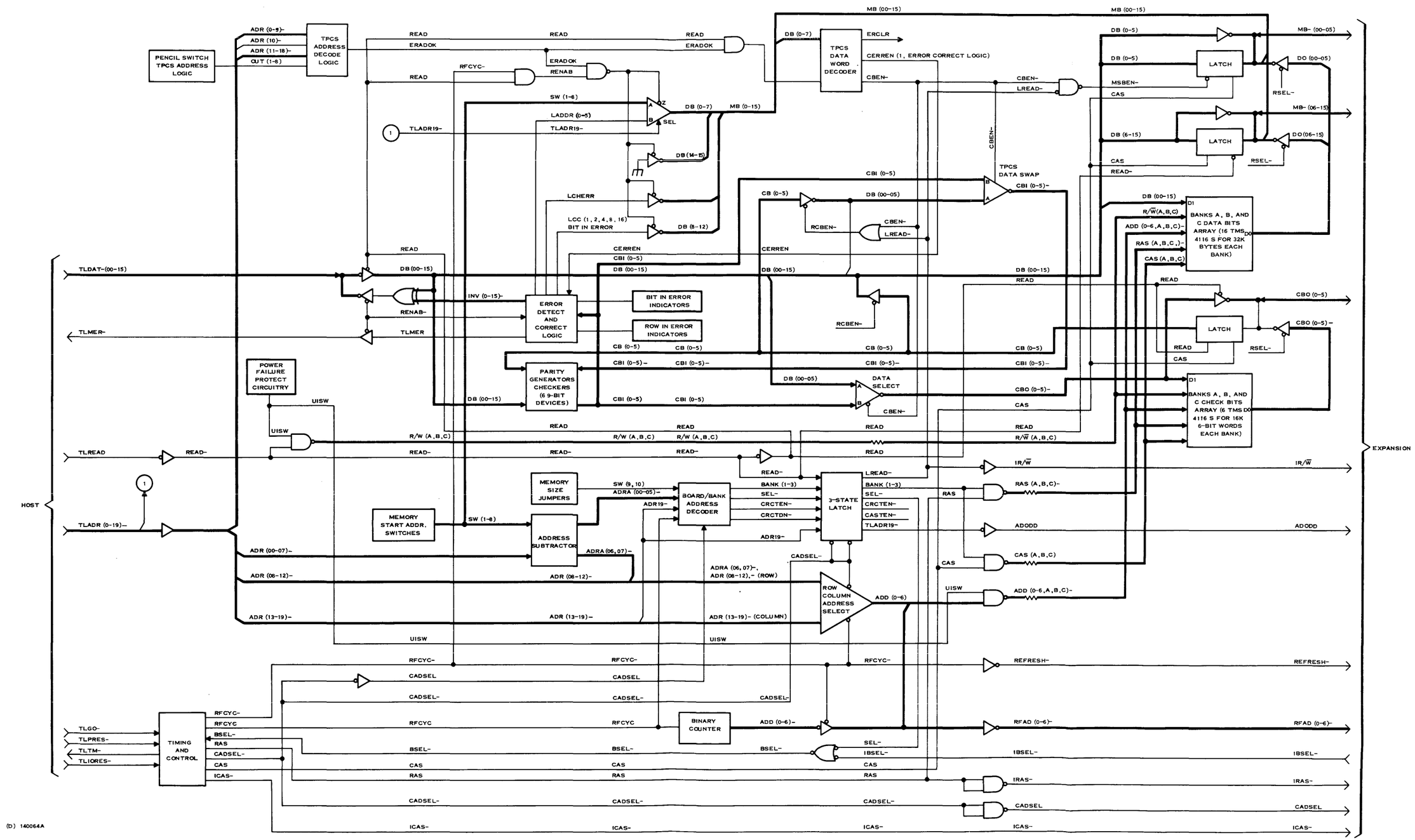


Figure 3-59. 96KB Memory Controller Block Diagram

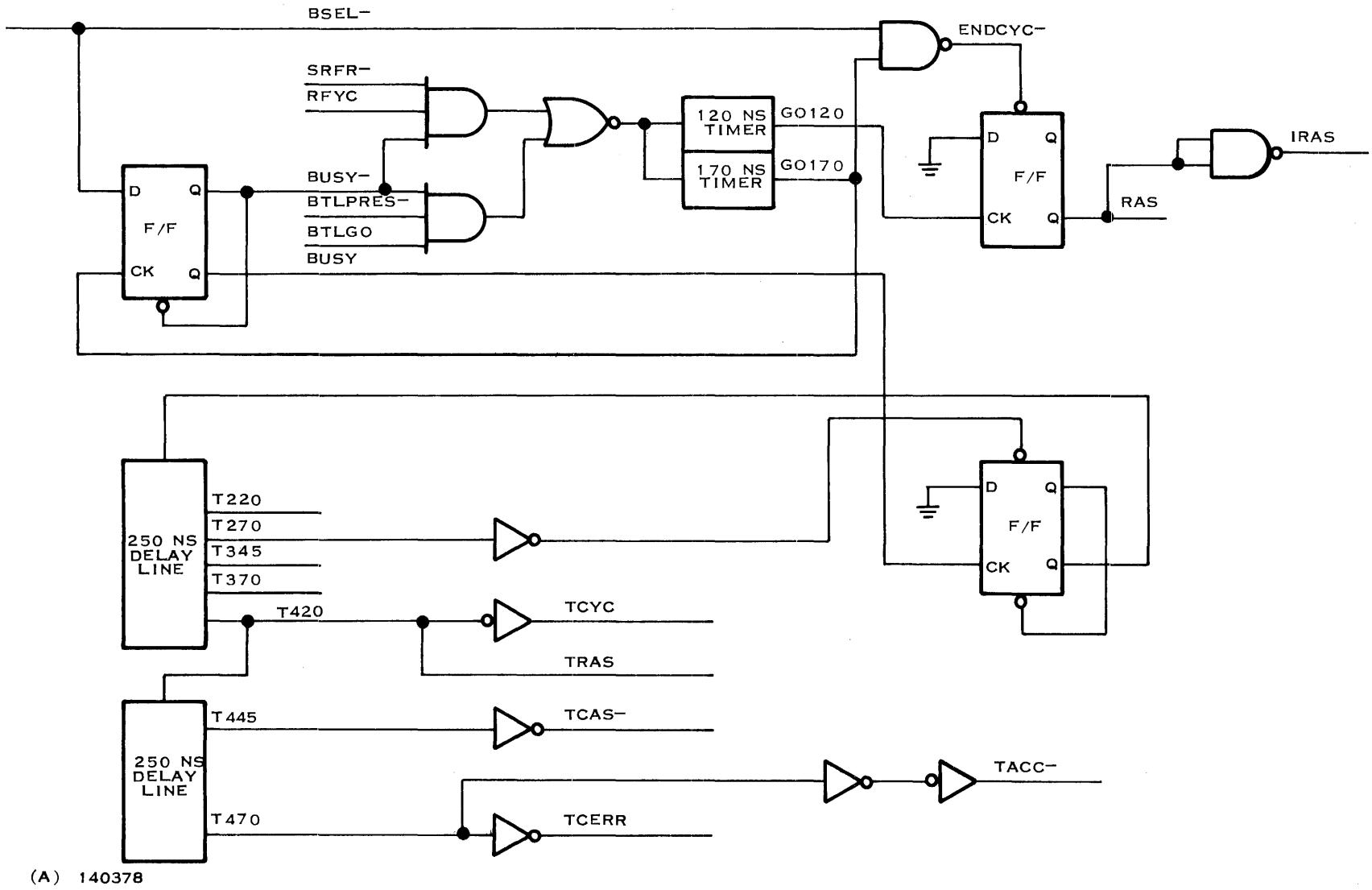


Figure 3-60. 96KB Memory Board Memory Timer Functional Diagram

Memory Refresh Controller. A refresh of the memory cell matrix is accomplished by performing a memory cycle at each of the 128 row addresses every two milliseconds to preserve data that is stored in the dynamic MOS memory storage cells. The refresh address lines at the output of the refresh controller replace the normal row and column address lines to refresh 1/128th of the memory during a refresh cycle. Refresh cycles are synchronized with memory requests and begin immediately following the first memory cycle that occurs after the refresh request is made. In the event that no memory requests are made before a second refresh request occurs, a refresh cycle is forced at the time of the second refresh request. When main power is removed from memory, the memory is said to be in the standby mode. While in this standby mode, only that circuitry required to maintain the integrity of the refresh controller is powered by the power supply battery. Refresh requests are generated at the same rate as when main power is on. When a refresh request occurs the required address and control logic is switched on and the refresh cycle is executed. The address and control logic power is switched off at the completion of each single cycle. The refresh controller consists of a free-running oscillator, four flip-flops, and a binary counter. (Figure 3-61 is a simplified functional diagram of the refresh controller.) The output of the oscillator is ANDed with PWRON to generate 128 refresh clock pulses, labelled RFCLK, every two milliseconds. RFCLK clocks a high RFREQ to the inputs of refresh flip-flop 2 and of forced refresh flip-flop. If a memory cycle is in progress or if a memory cycle occurs before the next RFCLK pulse is issued, the column address strobe CAS clocks the high through to the input of refresh flip-flop 3. At the end of the memory cycle, the positive-going RAS– signal clocks the high through this flip-flop to generate the RFCYC and RFCYC– signals. RFCYC is used to increment the 128-count binary counter by one for each refresh cycle. The output of the counter is selected during a refresh cycle to address each of the 128 rows of the memory devices in turn, one row for each refresh cycle. The high RFCYC is applied at the input to the board/bank address decoder to enable all banks of memory during a refresh cycle. In the absence of normal memory cycles, CAS and RAS– are not available to clock the flip-flops in the method just described and an alternate method of forcing refresh cycles is used. As before, the first RFCLK pulse clocks a high RFREQ to the inputs of two separate flip-flops. The flip-flop normally clocked by CAS remains static in the absence of a memory cycle and the next RFCLK pulse generated clocks RFREQ through the forced refresh flip-flop as a high input to a NAND gate. With a memory cycle not in progress, the other two inputs to the NAND gate (RTLGO– and BUSY–) are high. The low SRFR– output of the NAND gate sets refresh flip-flop 3 to generate the RFCYC and RFCYC– signals. Since refresh flip-flop 1 is not reset by the ANDed outputs of refresh flip-flops 2 and 3, REFREQ at the input to the forced refresh flip-flop stays high and all ensuing RFCLK pulses generate forced refresh cycles in the absence of normal memory cycles.

Error Checking and Correction. The error correction code is a modified Hamming code that allows for correction of any single-bit error and detection of any double-bit error. A three-bit or greater number of errors causes erroneous operation of the checking logic. The gross error condition wherein all 0's or all 1's are returned from memory is detected as an error. During a write cycle, the 16 data bits are applied to a check bit generator that provides the six check bits, CBI0 through CBI5, at the same time that the data word is written into memory. The check bit generator consists of six 9-input odd/even parity generators/checkers. During a write cycle, eight data bits are applied as inputs to each of the six parity generators/checkers with the pattern as shown in figure 3-62.

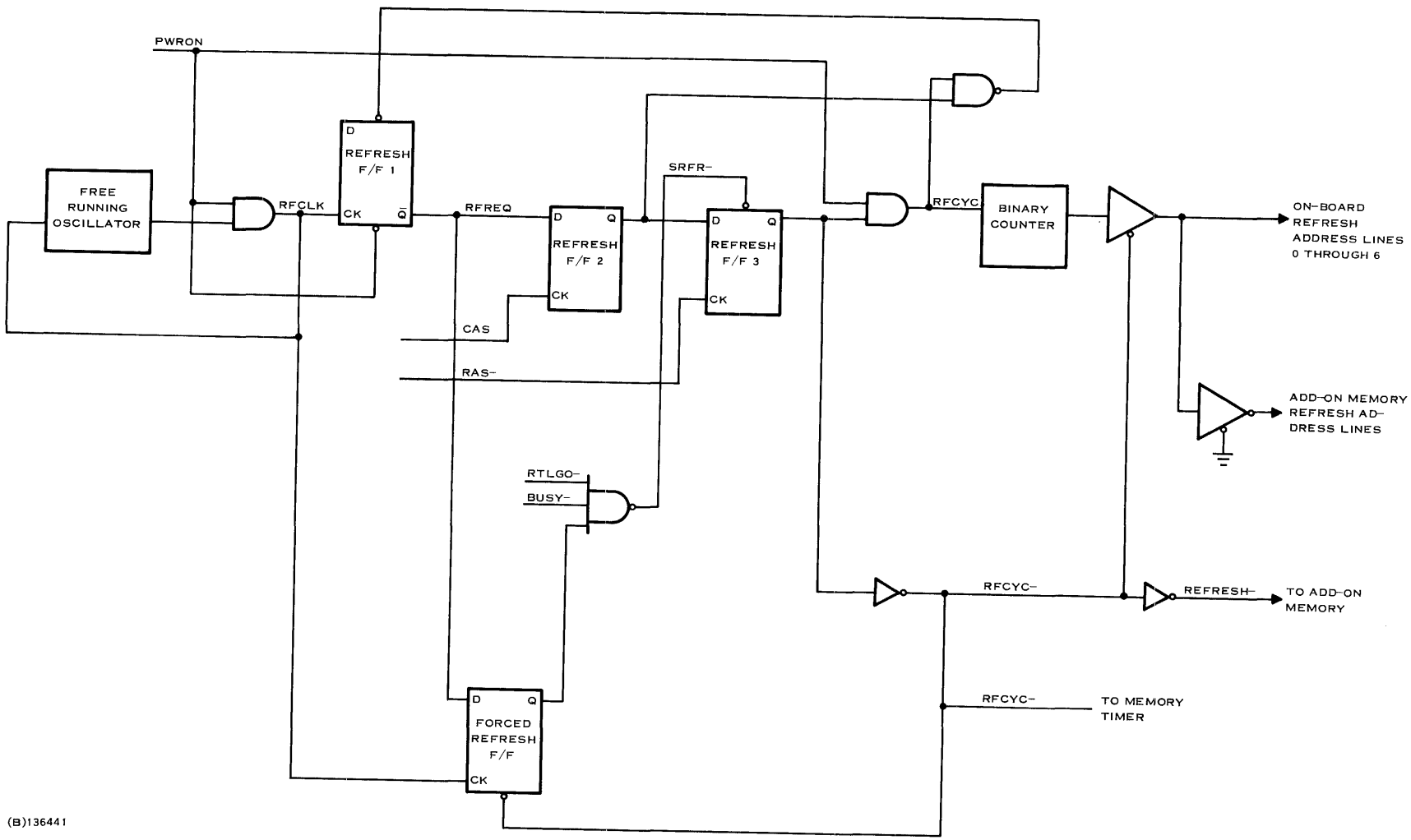


Figure 3-61. 96KB Memory Controller Refresh Logic Simplified Functional Diagram

CHECK BIT \ DATA BIT	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CB0	X	X		X	X				X	X	X			X		
CB1	X		X	X		X	X		X			X			X	
CB2		X	X		X	X		X		X			X			X
CB3	X	X	X				X	X			X	X	X			
CB4				X	X	X	X	X						X	X	X
CB5									X	X	X	X	X	X	X	X

Figure 3-62. Error Correcting Code Bit Patterns

The six check bits generated are stored in memory along with the 16 data bits. During a read cycle the six check bits are read out of memory as CB00– through CB05– along with the data bits. The check bits along with their corresponding data bits are applied to the parity generators/checkers that are acting as 9-input devices. If the parity of all six groupings of data and check bits are correct the assumption is made that no error has occurred. Note that the sense of two of the check bits (bits 0 and 1) is inverted to assure that the gross error condition of all 0's or all 1's is detected. If the parity of one or more of the check groups is incorrect, an error has occurred and the correction logic is enabled. The correction logic looks at the output of the six parity generators/checkers as a 6-bit code. Any single data bit error will change the sense of exactly three check bit lines and generate a code unique to that bit. The correction logic decodes this unique code, determines that the error is correctable, and inverts the specified data bit. Any single check bit error will change the sense of exactly one check bit line and generate a code unique to that bit. The correction logic will decode this unique (code) and pass the data with no modification. Any bit error will change the sense of an even number of check bit lines and generate codes that are not unique to any given error combination; therefore, a memory error is signaled and the data is not modified. Three or more bit errors generate codes that may indicate either no error, a correctable error, or an uncorrectable error, but in each instance an erroneous result is produced.

3.3.3.4 **TILINE Software Diagnostic Feature.** The 96KB memory controller may be placed in a diagnostic mode to allow testing of all on-board memory banks and add-on expansion memory banks. The diagnostic mode is activated when the proper 20-bit TILINE address is placed on the TILINE address bus. The user selects an assigned TPCS address using a set of eight pencil switches mounted on the 96KB memory controller board. These switches can be set to select any address that falls within the TILINE Peripheral Control Space (TPCS). Table 3-19 shows typical TPCS assignments for the 96KB memory controller and other peripherals.

Table 3-19. TPCS Locations for the 96KB Memory Controller

Typical Assignments for Peripherals	Device
F800	Primary Disk
F810	Secondary Disk
F820	Primary or Secondary Disk
F830	Disk
F840	Disk
F880	Mag Tape

Typical Assignments for Memory Devices	Device
FB00	1st 96KB Memory Controller
FB04	2nd 96KB Memory Controller

When the proper TPCS address is found to be present on the TILINE address lines, the controller examines the data bits present on the TILINE data bus for instructions on how to conduct the self-test. As shown in figure 3-63, bits 0-3 specify which of the four areas of memory on which to administer the test. That memory which is mounted on the 96KB memory controller board is divided into Bank A, Bank B, and Bank C. Additional memory boards are considered as expansion. Bank A addresses fall between the base address plus 16384_{10} (16K). Bank B includes the sum of Bank A plus 16K. Bank C addresses fall similarly, starting with the uppermost boundary for Bank B and continuing for another 16K.

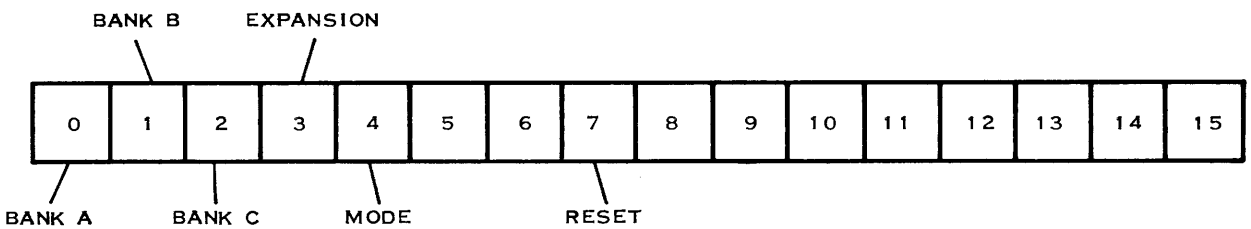
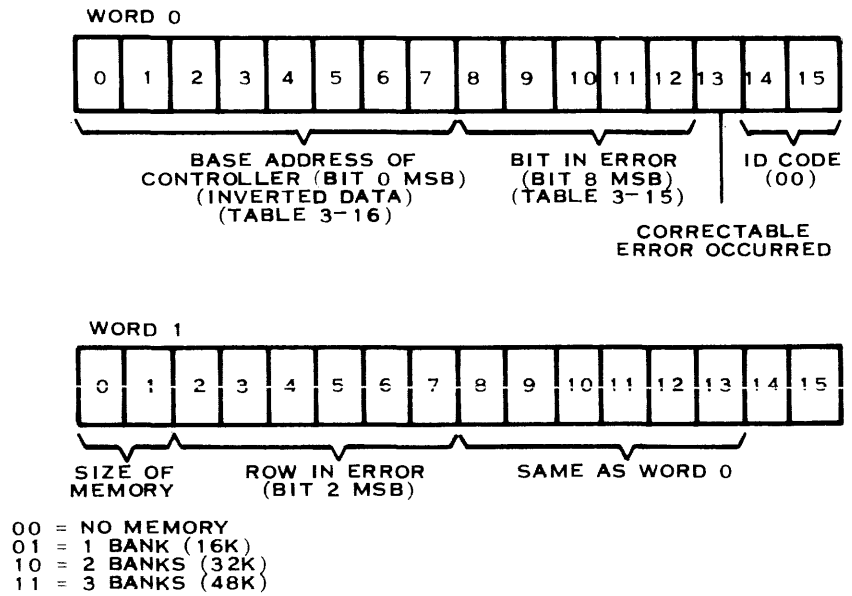


Figure 3-63. TPCS Data Word Assignments

Bit 4 controls the mode of the data placed on the TILINE data bus. When bit 4 is zero, the error correction is disabled and data is passed on to the master unchanged. When bit 4 is set to one, the six check bits are exchanged for the most significant data bits. This allows the user to directly access the check bits generated by the ECC logic and to monitor their validity. Bit 7 clears the diagnostic mode from the controller when set to one, restoring the memory board to normal operation. The following discussion of the operation of the TILINE diagnostic feature is keyed to figure 3-59.

Eight pencil switches with outputs OUT (1-8) are set by the user to establish a TPCS address for the 96KB memory controller. This address can be switched to form an address anywhere between FFC00 and FFDFF inclusive. When the TILINE address falls between these boundaries, the user selected address is compared to the TILINE address. If the two addresses match, the address decode logic enables the diagnostic mode with the ERADOK signal. In the diagnostic mode, the host 990 computer can read two data words from the TPCS. Word 0 and Word 1 are placed on the data bus when TLADR19– is high and then low, respectively. In other words, the 96KB memory controller TPCS logic is enabled by two consecutive addresses: the even address selects Word 0, and the odd address selects Word 1. Figure 3-64 shows the contents of Word 0 and Word 1.



(A) 140376A

Figure 3-64. Word 0 and Word 1 Placed on the TILINE Data Bus by the 96KB Memory Controller When in the Diagnostic Mode During a Read Operation

Bits 8-15 of both TPCS output contain these data:

- The address of the bit in error
- Whether the error was correctable
- The ID code, 00.

The bit in error address is provided to the output words through lines connected directly to the bit in error LEDs, LCC (1,2,4,8,16). A line tied directly to the correctable error LED, LCHERR, is connected to bit 13 of both words. Bits 14 and 15 are both grounded to provide the ID code 00.

Word 0 bits 0-7 contain the base address of the memory controller's memory. This information is provided to the output word through pencil switch lines sw(1-8). Word 1 bits 0-7 are divided into these data:

- Size of computer memory
- Row in error address.

Bits 0 and 1 indicate the size of the computer memory with information provided through lines tied to memory size jumpers SW9 and SW10. Bits 2-7 of Word 1 form the row in error address. This information is composed of lines tied directly to the row in error LEDs, LADDR(0-5).

After being placed in the diagnostic mode, DB(0-7) of the TILINE data word is examined by the diagnostic logic when a TILINE write operation is attempted, i.e., when READ– goes high.

The user can form this data word to control these features:

- Selection of a portion of memory on which to perform the diagnostic test
- Selection of the diagnostic mode
- Clearing of the diagnostic feature to restore the memory controller to normal operation.

Expansion memory cannot be modified into banks. Data bits 0-3 select one or all of the banks and/or the expansion. Data bit 4 selects the mode under which the diagnostic should be run. When this bit is zero, CERREN is high and the error detection and correction is disabled in the specified banks. When data bit 4 is one, CBEN– goes low and the most significant data bits of the word are swapped through the multiplexer with the six error checking bits in the banks or memory area specified. When Bit 7 is one, the data word decoder issues an ERCLR command that clears all latches and disables all three-state TPCS devices, restoring the controller to normal operation.

3.3.4 CACHE CONTROLLER. The cache controller is a multilayer printed circuit board that contains all memory control logic as well as the storage elements for 64K bytes of primary memory and 2K bytes of cache memory and the control logic for up to 1M bytes of additional memory on associated add-on memory expansion boards. The cache controller uses a cache technique to improve the effective operating speed of primary memory. Under the cache concept, frequently used data is copied from the relatively slow primary memory into a small, fast cache memory. Subsequent calls to data residing in the cache can be honored faster than data from primary memory. The cache controller interface to the TILINE bus is made through the two 80-pin connectors at the bottom edge of the board that installs into the chassis slot. Two 50-pin connectors at the top edge of the board are used to interface with expanded memory.

As was true for the 96KB memory controller, up to four of the 256KB add-on memory array boards may be controlled by the cache controller. Cycle control and refresh control for the add-on array boards are provided by the cache controller, but the add-on boards interface directly with the TILINE for address selection.

The cache controller circuits, including the error checking and correcting circuits, are implemented in TTL devices on the lower half of the board as shown in figure 3-65. The 64K bytes of on-board MOS primary memory consist of two rows of TMS 4116 devices across the top of the board. Each row includes the 22 devices required for the storage of 16 data bits and the 6 error checking bits. The TMS 4116 chip is organized as 16,384 one-bit words housed in a 16-pin, dual-in-line package. The 2K bytes of cache memory consist of two banks of memory devices grouped in the center of the lower edge of the board. Each bank includes the 14 devices required for the storage of the 16 data bits, 2 data parity bits, a data error bit, 11 address bits, 2 address parity bits and 1 validity bit.

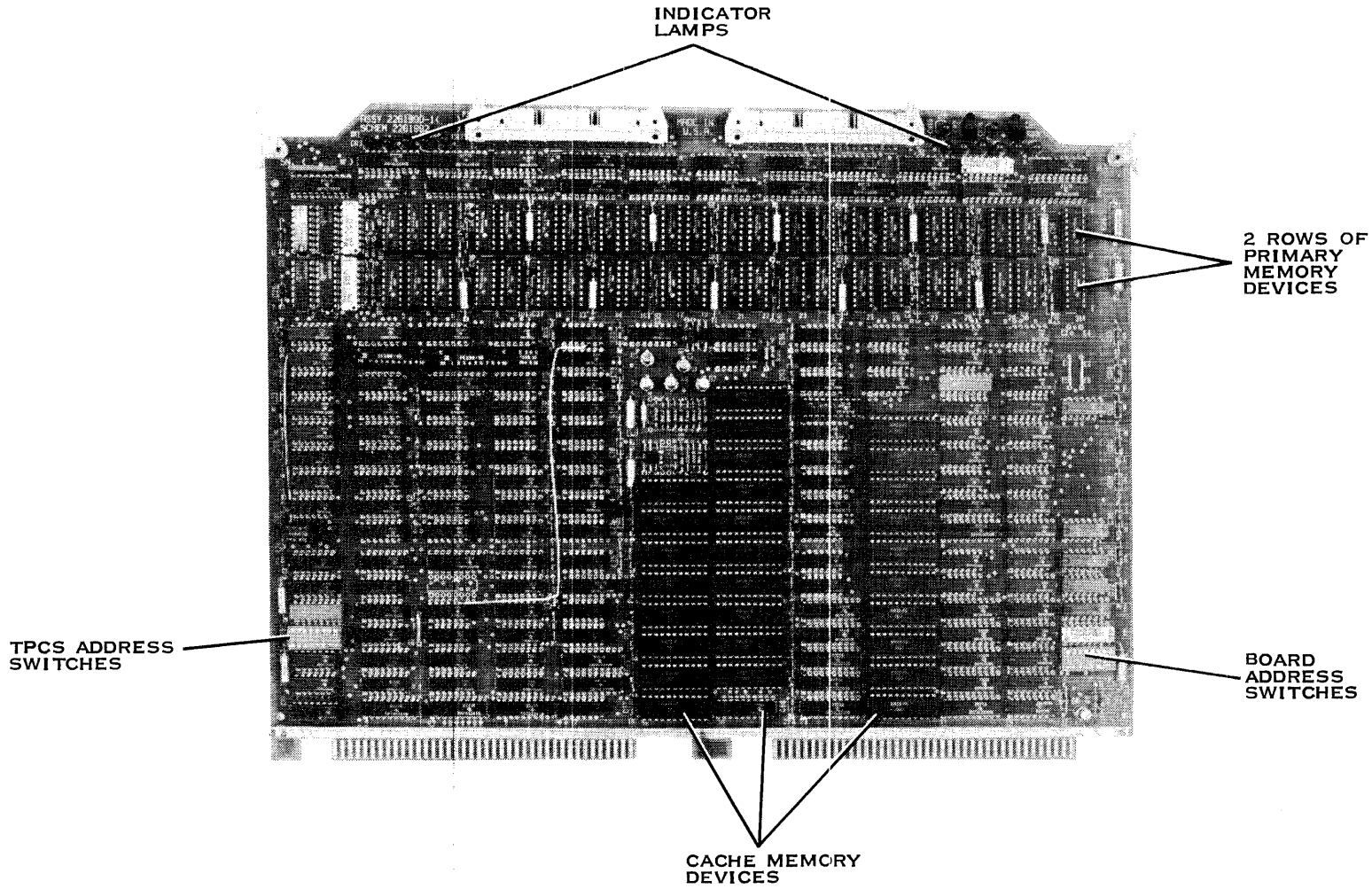


Figure 3-65. Cache Controller

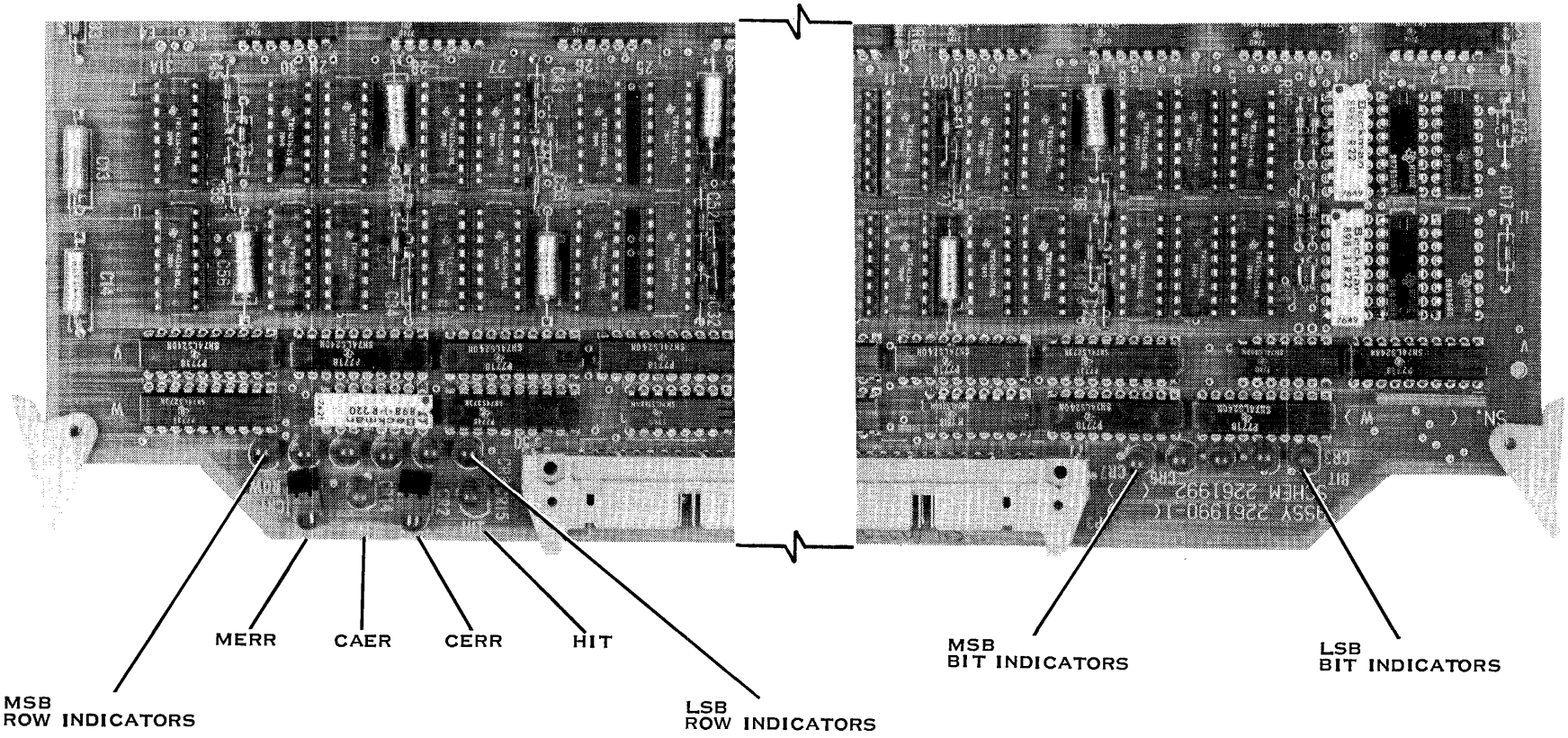


Figure 3-66. Cache Controller Indicators

As shown in figure 3-66, the cache controller includes 3 LED error indicators, an LED HIT indicator, and 11 LED chip failure indicators. The three error-indicating LEDs are dedicated to the following functions:

- An indication that a one-bit correctable primary memory error has been detected and corrected (CERR).
- An indication that a multibit, uncorrectable primary memory error has been detected and placed on the data bus unmodified (MERR).
- An indication that a parity error has occurred in either the cache data or the cache data address. No change is made to data when this type of error occurs (CAER).

The error-indicating LEDs are set on the first occurrence of the respective error stimulant and remain set until the board is powered down or until a reset instruction is issued.

The additional 11-chip failure indicators pinpoint the memory chip that caused the first single-bit error and are divided into two groups as shown in figure 3-66. A group of five forms a binary code that identifies the bit that failed. The remaining six LEDs form a binary code that identifies the row that contains the failing chip. Additional errors do not affect these indicators but are recorded by the two error indicators located on the add-on memory expansion board where the error occurred.

The HIT indicator lights whenever the addressed word in a memory read or write operation resides in cache memory. Table 3-20 summarizes the indicators and their functions.

Table 3-20. Description of Cache Controller Indicators

Indicator	Function
ROW	These six LEDs indicate in hexadecimal the row that sustained a data recovery error. Refer to table 3-16.
BIT	These five LEDs indicate in hexadecimal the bit determined to be in error. Refer to table 3-16.
CAER	An uncorrectable cache error has occurred.
CERR	A correctable primary data error has occurred.
MERR	An uncorrectable primary memory data error has occurred.
HIT	Indicates that the addressed word in a read or write operation resides in cache memory.

Each of the dual-in-line switches consists of eight single-pole, single-throw, push-type switches. As shown in figure 3-65, one switch package is used to set the cache controller on-board memory starting address. The other package selects the TPCS address of the board. The memory starting address switches correspond to the 8 most significant bits of the 20-bit TILINE address and permit board starting address selection in 8K-byte increments. Switch 1 is the most significant bit of the address, and switch 8 is the least significant bit. Operation of these address switches is identical to that of the 96KB memory controller. The starting address switch settings for the cache controller are set in the same manner that they were set for the 96KB memory controller (see table 3-17). Addresses other than those shown can be represented by using the eight switches to establish the binary number.

The diagnostic mode pencil switches correspond to address bits 11 through 18 of the 20-bit TILINE address bus and select the TPCS address that is used to operate the controller in the diagnostic mode. Switch 1 is the most significant bit and switch 8 is the least significant bit of the TPCS address segment. This permits 512 addresses to be selected that fall between $F800_{16}$ and $FBFE_{16}$, inclusive, in the 15-bit address form. The 20-bit address is generated in the address development process. Table 3-18 of the 96KB memory controller lists several examples of TPCS addresses and their corresponding switch settings. These settings operate identically for the cache controller. The recommended TPCS addresses for cache controllers are shown in table 3-21. Software provided by Texas Instruments expects these values to be used.

Table 3-21. Recommended TPCS Settings for One or More Cache Controllers

CPU Address	TILINE Address	Module
FB10	FFD88	1st Cache Controller
FB14	FFD8A	2nd Cache Controller
FB18	FFD8C	3rd Cache Controller
.	.	.
.	.	.
.	.	.
etc.	etc.	etc.*

*Additional controllers placed every four bytes (CPU address).

3.3.4.1 Cache Operation. The cache controller is able to make the primary memory appear to operate faster by storing copies of often-used memory word pairs in a small, fast access memory. The scheme used by the cache controller is to store in cache the contents of the last 512 odd/even memory word pairs requested by a TILINE master device. An odd memory word is a word with an address in which the least significant bit is one. An even memory word is a word in which the least significant bit is zero. A pair of data words whose addresses are identical except for the sense of the least significant bit is called an odd/even word pair. When a primary memory word is requested by the TILINE master device, the cache logic searches the collection of data words in the fast memory (cache memory) to see if the requested word is present. If the requested word is not present, the

cache logic adds the new word to the cache memory along with the other member of the odd/even word pair. With the cache option enabled, these possibilities may occur during a read or write operation.

1. A valid memory address is decoded but is not present in the cache memory. If the memory operation is a read operation, the requested word and the other member of the odd/even pair are fetched from primary memory and copied to the cache memory. If the memory operation is a write operation, the specified word is updated in primary memory only and no action is taken by the cache controller to add this word to the cache memory.

2. A valid memory address is decoded and is present in the cache memory. If the memory operation is a read operation, the requested word is copied from the fast cache memory onto the TILINE data bus. If the memory operation is a write operation, both the cache memory and the primary memory are updated.

3. A nonvalid memory address is found on the TILINE address bus. The cache controller takes no action and the TILINE is relinquished after a specified time-out period.

4. The cache controller board is busy with either a memory refresh cycle or with a memory cycle with another master device. The master device encountering the busy indication must wait for the cache controller board to become free.

The cache for the cache controller is enabled via the TPCS write word addressed to the cache controller. Addressing the cache controller's selected TPCS in a write operation with bit 9 of the word low enables the cache. Similarly, setting this bit high disables the cache option and the board functions only as a primary memory controller. The cache controller is equipped with error detection and correction circuits that generate error prevention data. The error prevention information is stored with other cache data that is organized as shown in figure 3-67. When the cache controller board is powered-up or when an instruction is issued through the TPCS, an initialization sequence is executed on the cache controller. Initialization consists of setting all validity bits low and clearing all error logic. Validity bits are then generated and stored with all cached data word addresses. The sense of the validity bit is high when the cache is operating normally and low during initialization or when an error condition is experienced. When a data word is fetched from the cache memory, the validity bit is checked along with the associated parity bits. If the validity bit is high, the fetched data word is treated normally. If the sense of the validity bit is low, the cache version of the requested word is discarded and the fetch is made from primary memory instead.

3.3.4.2 Memory Read Cycle. In a memory read cycle, a master device gains control of the TILINE by issuing a TILINE GO (TLGO–) signal. At the same time, the master asserts a read command and places a valid 20-bit address on the TILINE address bus. When the cache controller interface circuits receive the TLGO–, the board starting address as set in the pencil switches is subtracted from the address present on the TILINE address bus in preparation for a normal primary memory read cycle. At the same time, the asserted TLGO– causes the cache circuits to begin comparing the TILINE address to the cached data addresses to determine if the requested word resides in the cache. A read is performed on the cache address memory at the location specified and the 14 output bits from the addressed cache memory location are applied to an address comparison logic. The 14 output bits consist of 11 bits of cache address information, 2 associated parity bits and a validity bit. The sense of the validity bits is checked. If the validity bit is high, operation of the cache continues; otherwise, the cache cycle aborts and the cache controller continues with a normal primary memory read. The cache address logic and the TILINE address logic on the board are both interrogated at 100 nanoseconds after TLGO– is asserted. If the requested word is present in the cache memory, a valid

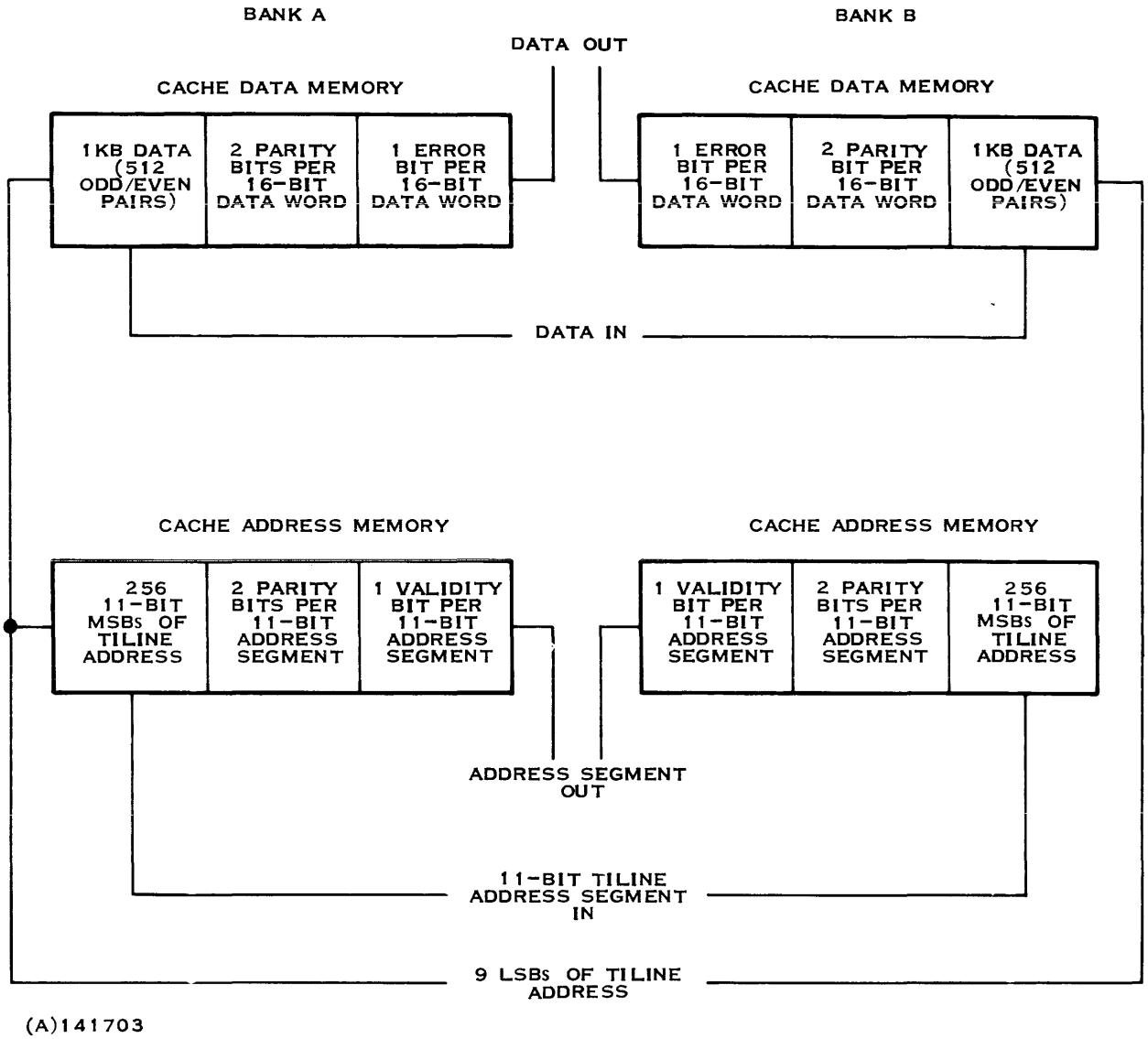


Figure 3-67. Organization of Cache Data

cache address signal is generated and the parity and error bits of the cached word are tested. Any discrepancy in the cache data parity or error bits aborts the cache operation and a normal primary read operation occurs. If the cache data parity and error bits are in order, a cache hit (HIT) signal is generated and the output buffers of the appropriate cache address are enabled. The HIT signal causes the TILINE terminate signal to be generated, signaling to the master device that valid data is present on the TILINE data bus.

If the requested word is not present in the cache memory and a valid address is not decoded by the TILINE address logic on the board, an end of cycle signal is generated and the operation is aborted. If the requested word is not present in the cache and a valid address is decoded by the TILINE address logic, 16 data bits and 6 ECC bits at the addressed location are strobed into latches. The 6 ECC bits that were stored in primary memory are compared with 6 new ECC bits generated from the retrieved data bits. If no discrepancy is detected from this comparison, the TILINE terminate signal is generated to indicate to the master device that valid data is present on the TILINE data bus. If an error is detected by the ECC, the error logic then determines if the error is correctable. If the error is uncorrectable, the fetched data is not modified and an error signal is generated to the master device along with the TILINE terminate signal. If the error is correctable, the ECC modifies the bit in error and the corrected data word is placed on the TILINE data bus and the TILINE terminate signal is asserted. During this time, the cache logic places a copy of the fetched word in cache memory so that subsequent read operations at the associated address will result in a cache HIT. The cache controller also fetches and stores the other member of the odd/even address pair associated with the data word just read into cache memory. Subsequent read requests to either of the two memory locations will result in a cache HIT until more frequently requested data is written into cache.

If an ECC discrepancy occurs on the second word of this double-word read, the error bit at the cache memory location for the second word is set and the cache sequence aborts. Subsequent reads to the first of the two cache memory locations will result in a HIT, but reads from the second word location will result in a MISS and the word will be fetched from primary memory.

3.3.4.3 Memory Write Cycle. In a memory write cycle, a master device gains control of the TILINE by issuing a TLGO- signal. At the same time, the master asserts a write command and presents valid write data and a valid 20-bit address to the TILINE. When the cache controller interface circuits receive the TLGO-, the cache address logic and the TILINE address logic on the board decode the address to determine if the board is being addressed and if the addressed word resides in cache. If a valid address is not decoded, an end of cycle signal is generated. If a valid address is decoded, the sequence continues. If the address is found to reside in cache, the HIT signal goes high to generate the CACHE BUSY signal. The CACHE BUSY signal causes the data bits and two bits of parity to be stored in the cache bank that caused the HIT signal. If the address is not found to reside in cache, or if at the completion of cache storage the address is found to be in cache, the 16 write data bits and the 6 check bits generated by the memory check logic are stored in the addressed portion of primary memory.

Table 3-22 summarizes the sequence of actions taken by the cache controller during memory operations.

Table 3-22. Summary of Cache Controller Memory Operations

Condition	Action
READ CYCLE:	
Cache enabled Cache HIT	The requested word is provided from high speed cache memory.
Cache enabled Cache MISS	The requested word is provided from slower primary memory.
Cache disabled Cache HIT	No cache action occurs; the requested word is provided from primary memory.
Cache disabled Cache MISS	No cache action occurs; the requested word is provided from primary memory.
WRITE CYCLE:	
Cache enabled Cache HIT	The controller writes into both primary and cache copies of the specified word.
Cache enabled Cache MISS	The controller writes into the specified primary memory location only.
Cache disabled Cache HIT	The controller writes into both primary and cache copies of the specified word.
Cache disabled Cache MISS	The controller writes into the specified primary memory location only.

3.3.4.4 TPCS Mode Operation. A master device gains access to the control logic of the cache controller through use of the TPCS for purposes of monitoring the operation of the cache controller or to control the performance of the cache controller. The TPCS can be used to enable the cache operation, to control error latches, and to operate the cache controller in the diagnostic mode.

The cache controller is placed in the TPCS mode by placing the correct TPCS address on the TILINE address lines while executing a write operation. This address must fall between FFC00 and FFE00 hexadecimal (see table 3-21), and must match the address set in the TPCS pencil switches on the cache controller board. The operation of the cache controller while in the TPCS mode is controlled by the data present on the TILINE data bus. Figure 3-68 illustrates the cache controller TPCS write word. Refer to table 3-23 for an explanation of the function of each write data bit while the cache controller is in the TPCS mode.

When the cache controller is placed in the diagnostic mode, tests on either primary memory or the cache memory of the controller may be performed. The following diagnostic functions can be performed on primary memory:

1. The six check bits generated on a write cycle that are normally stored in the primary memory can be swapped with the six most significant data bits, 0 to 5.

2. The six check bits returned from primary memory on a read cycle can be manipulated to replace data bits 0 to 5. Under this mode of operation, the error circuitry will detect and indicate any errors using the appropriate indicator lamp, but correction of the error is inhibited and the data are not modified.

3. The controller may be instructed to inhibit the data error detection and correction circuitry so that uncorrected data may be read from the memory.

4. The error indication circuits can be reset by setting the primary memory reset bit (bit 7) in the TPCS write word.

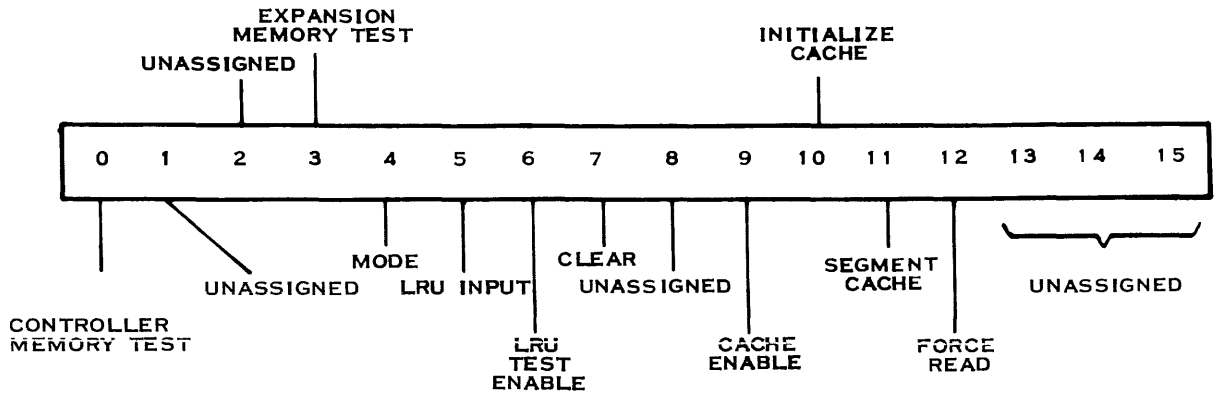


Figure 3-68. TPCS Write Word to Cache Controller

Table 3-23. Description of Bit Assignments for TPCS Write Word to Cache Controller

Bit	Description
0	When high, all read and write operations to the first 64K bytes of the primary memory on the cache board are modified as determined by bit 4.
1	Unassigned
2	Unassigned
3	When high, access to all expansion memory boards is modified as described for bit 0.
4	Mode bit, when low, error correction is disabled on banks in the areas of primary memory as specified by setting bits 0 and 3. When high, the six most significant data bits are swapped with the ECC field.

Table 3-23. Description of Bit Assignments for TPCS Write Word to Cache Controller (Continued)

Bit	Description
5	When enabled by bit 6, this bit controls the sense of the least-recently-used (LRU) bank flip-flop. When high, the LRU is forced high, and the next word added to the cache memory will be stored in bank B. When low, the LRU is forced low, and the next word added to the cache memory will be stored in bank A.
6	When high, the least-recently-used (LRU) bank flip-flop will be forced to the sense of bit 5. This test allows a diagnostic check to control the bank of the cache memory to which new words are added.
7	When high, primary and cache memory error logic and the associated error indicator LEDs are cleared. This bit must be reset to reenable the primary memory error logic.
8	Unassigned
9	When low, the cache logic is enabled, that is, the cache controller will begin processing primary memory references through the cache memory. When high, the cache logic is completely disabled, and all primary memory references are made directly to primary memory.
10	When toggled (set to 1, then 0), the cache memory is initialized; that is, all validity bits are set to false. All cache HITS will be disregarded unless the data was stored in the cache memory following the initialization.
11	When high, the controller will store data in the cache memory only from references made to the upper 32K bytes of primary memory, that is, no data will be stored in the cache memory if a MISS occurs with a primary memory address located in the lower 32K bytes of the on-board primary memory, or located on any expansion board.
12	When high, this bit causes the cache to answer if an address match occurs. This bit is used to read cache addresses with parity errors.
13	Unassigned
14	Unassigned
15	Unassigned

The following diagnostic functions can be performed on the cache memory:

1. The cache operation can be inhibited so that no cache operation will occur. Primary memory words residing in the cache will not be read during read cycles and cache data will not be updated during write cycles.

2. The cache operation can be restricted to the upper 32K bytes of the controller primary memory. This provides the capability to enter a diagnostic routine in the lower 32K bytes of the controller memory and prevent its execution from filling up the cache.

3. The cache can be totally initialized by resetting all validity bits.

4. The bank used by the cache to store new data can be preselected.

When in the TPCS mode, the cache controller places data words on the TILINE data bus when a read operation is made. The data words read are even and odd forms of the TPCS address as set in the TPCS pencil switches. Figure 3-69 shows the format of the two data words read from the cache controller. Table 3-24 provides an explanation of the function of each read data bit while the cache controller is in the TPCS mode.

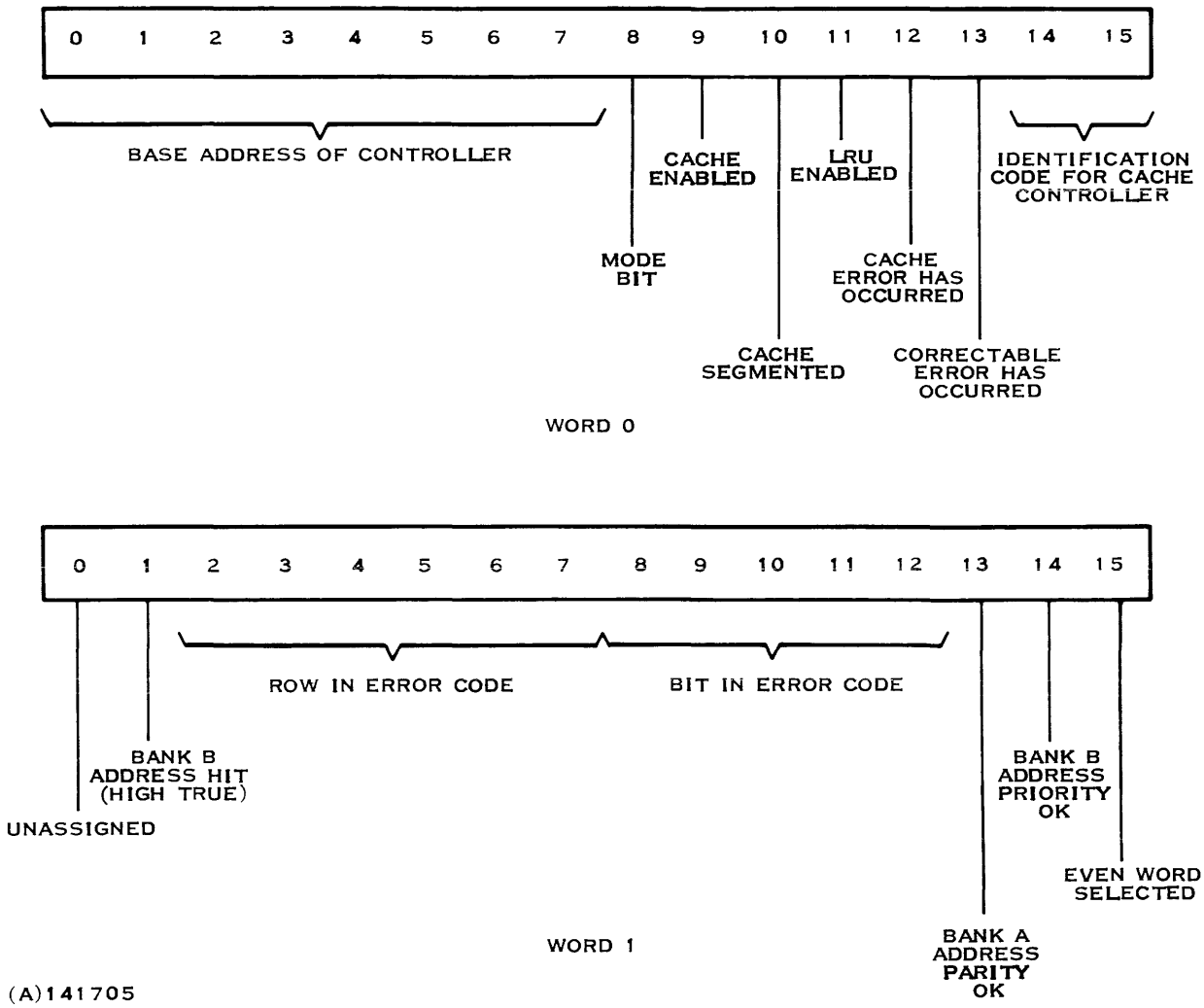


Figure 3-69. Data Words Output to TILINE During Read Operation in Cache TPCS Diagnostic Mode

Table 3-24. Bit Assignments for Read Words from Cache TPCS Diagnostic Mode

Bit	Description
WORD 0	
0 - 7	These eight bits indicate the setting found on the cache primary memory starting address pencil switches.
8 - 11	These bits echo the diagnostic state of the controller as follows; bit 8 = mode, bit 9 = cache enabled, bit 10 = cache segmented, and bit 11 = LRU enabled.
12	When high, a parity, validity, or error bit fault has occurred during a cache operation. An ECC error will also set this bit high.
13	When high, a single-bit ECC error has been detected and corrected in a fetch from primary memory.
14 - 15	These bits are permanently set to form the cache controller identity code, 01.
WORD 1	
0	This bit is unassigned and is always set low.
1	When high, an address match has occurred in cache memory Bank B.
2 - 7	The sense of these bits corresponds to the row in error information found on the error LEDs.
8 - 12	The sense of these bits corresponds to the bit in error information found on the error LEDs.
13	When high, the parity bits associated with the address fetch from cache memory Bank A were good.
14	When high, the parity bits associated with the address fetch from cache memory Bank B were good.
15	When high, an even word from cache memory has been selected. When low, an odd word has been selected.

3.3.5 MEMORY ADD-ON MODULE, 256KB, WITH ECC, 990/16KR. The expansion memory board used with the 96KB memory controller and cache controller hereinafter referred to as the 256KB add-on memory, contains the storage elements, address decoding logic, and control and data buffers for up to 256K bytes of MOS RAM on the board. The 256KB add-on memory board used in conjunction with the memory controllers provides high density main memory for the 990/10 central processors that communicate over the TILINE. Up to four of the 256KB add-on memory boards may be controlled by one memory controller. The 256KB add-on memory interface to the TILINE consists of the TILINE address lines and power lines and is effected through two 80-pin connectors at the bottom edge of the board that installs into the computer or expansion chassis. Two 50-pin connectors at the top edge of the board provide the data path and control signals needed to interface with the 96KB memory controller, as shown in figure 3-56. The TILINE address lines interface to the 256KB add-on memory is also shown in figure 3-56. Memory on the 256KB add-on memory board consists of from one to four banks of memory chips. Each bank consists of two rows of 22 memory chips, one row for even and one row for odd word addresses. Double word read and single word write cycles are implemented for use with a cache-type controller.

3.3.5.1 256KB Add-On Module Physical Description. As shown in figure 3-70, the 256KB add-on memory array address decoding logic and the control and data buffers are implemented in TTL devices located on one side of the board. Figure 3-71 shows component layout and reference designators for the 256KB add-on array. The eight rows (or four banks) of TMS 4116 MOS memory devices extend across the rest of the board with row and bank designations as shown in figure 3-72. Also installed on the board are two LED error indicators and dual-in-line switch package that is used to set the starting address of the board. The two error indicating LEDs indicate that a one-bit (correctable) error or a multibit (uncorrectable) error has occurred on this board. These lamps are set on the first occurrence of the respective error stimulant and remain set until the system is powered down or until an I/O reset instruction is issued. The dual-in-line switch consists of eight single-pole, single-throw address switches. The address switches correspond to the eight most significant bits of the 20-bit TILINE address and permit board starting address selection in 8K-byte increments. Switch 1 is the most significant bit of the address with switch 8 the least significant bit of the address. The required switch settings for the 256KB add-on memory array are the same as that for the 96KB memory controller board as provided in table 3-17. The memory capacity may be set in increments of from one to four banks of memory. Since each bank of memory represents 64K bytes of memory, the memory capacity available is either 64K, 128K, 192K, or 256K bytes. Memory size is set by connecting jumpers across the terminals of E9 and E10 as shown in table 3-25.

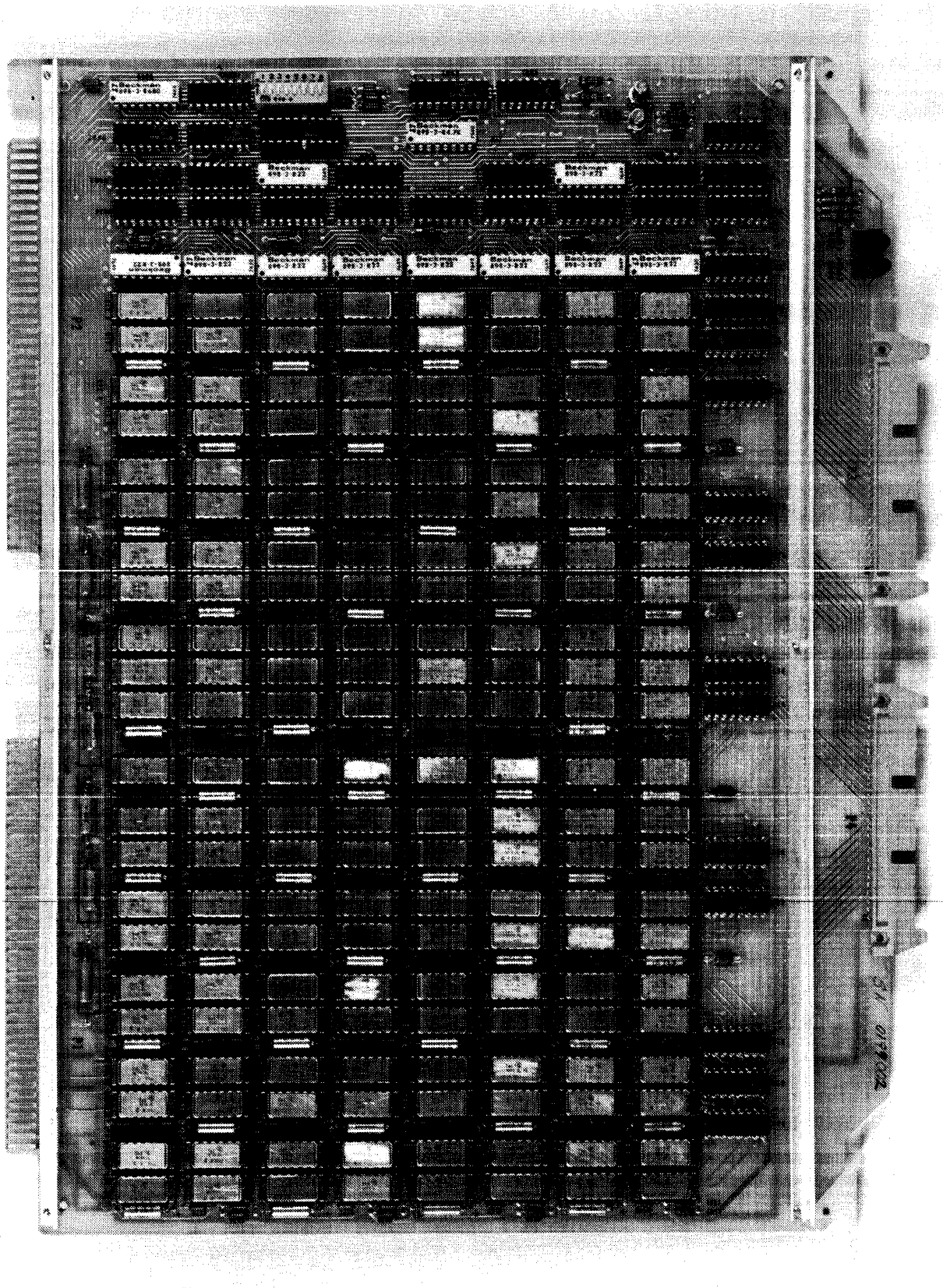


Figure 3-70. 256KB Add-On Memory Array Board

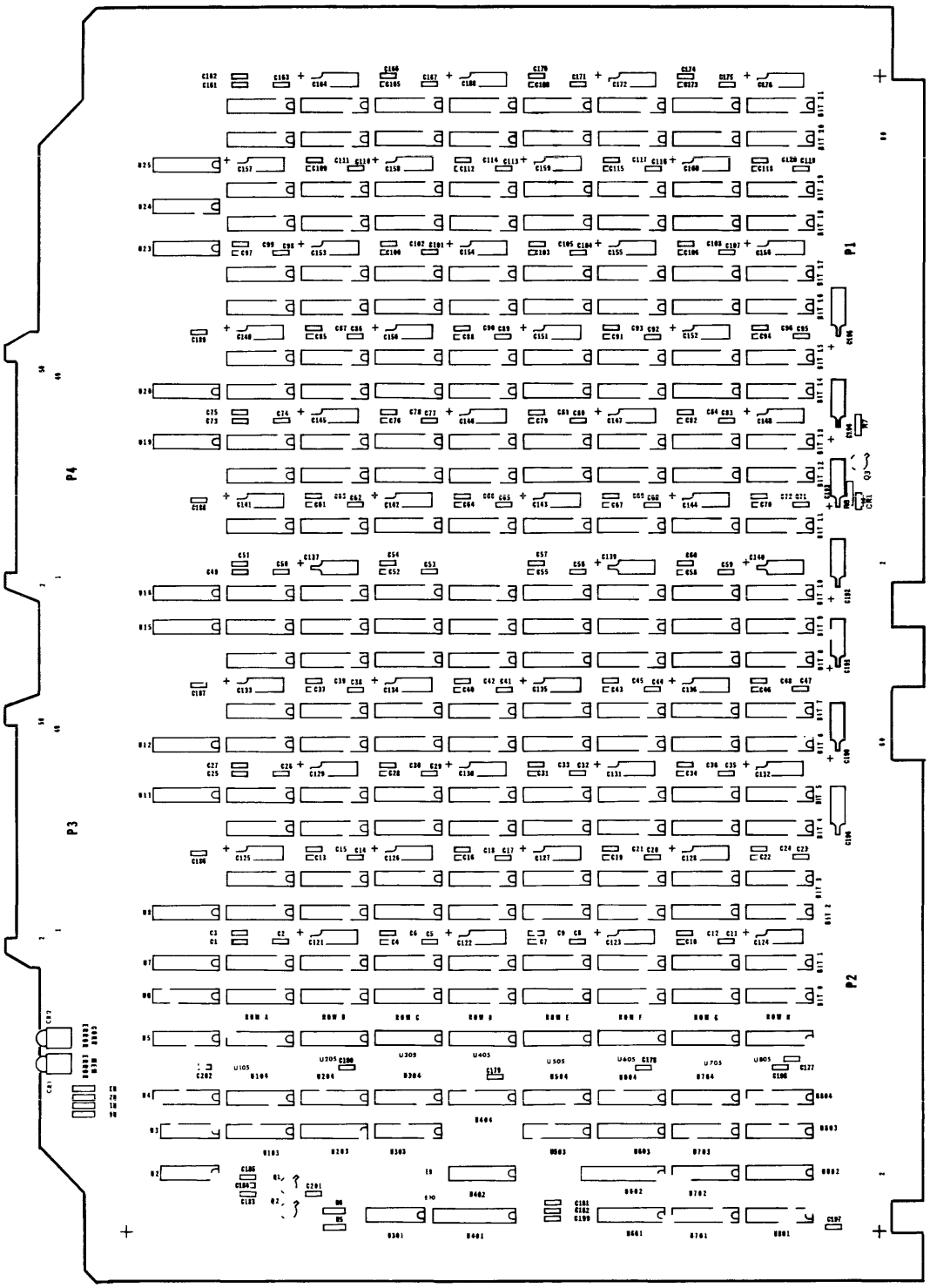
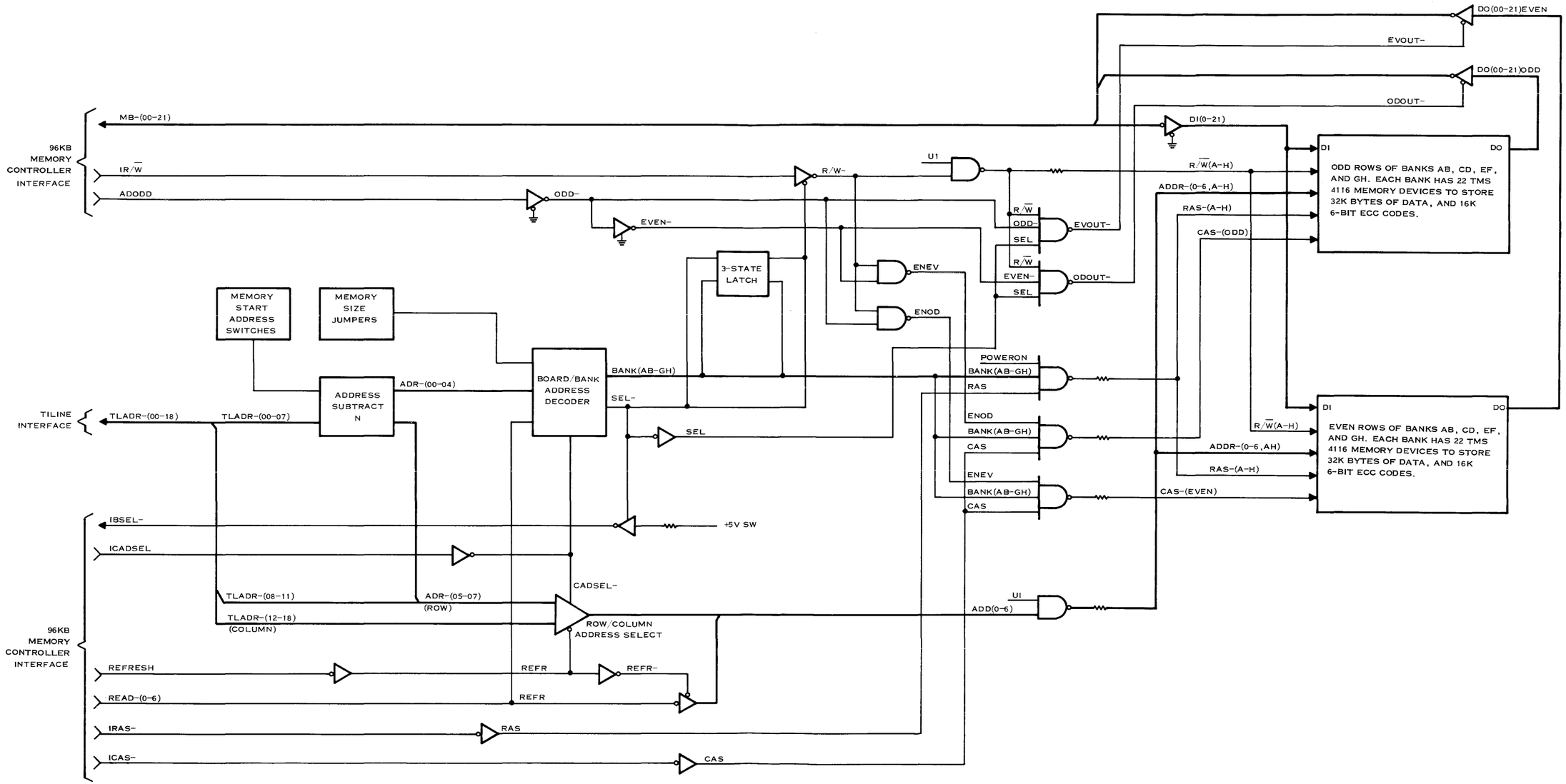


Figure 3-71. 256KB Add-On Memory Board Component Layout with Reference Designators



(D)136442A

Figure 3-72. 256KB Add-On Memory Array Board Block Diagram

Table 3-25. Memory Size Jumpers for 256KB Add-On Memory Array Board

Memory Size	Jumper E9	Jumper E-10
64KB	OFF	ON
128KB	ON	OFF
192KB	ON	ON
256KB	OFF	OFF

Memory Write Cycle. To execute a write memory cycle, the TILINE master device asserts TLGO– and at the same time asserts the write command TILINE READ (TLREAD) by setting both signals low. The master also generates valid write data on the data bus (TLDAT–) and a valid 20-bit address (TLADR–) on the address lines. The memory interface circuits on the 96KB memory controller receive the TLGO– as the 256KB add-on memory board decodes the address to determine if the address is valid for that board (as set on the memory start address switches and memory size jumpers). The asserted TLGO– triggers the memory timer on the 96KB memory controller that produces a delayed strobe to interrogate the results of the address decoder. If no valid address is decoded on the 96KB memory controller nor on any 256KB add-on memory board, a cancel signal is produced that aborts the cycle. When a valid address is decoded on the 256KB add-on memory, the memory timer on the 96KB memory controller generates the following interface signals to the 256KB add-on memory board in this sequence:

- Row address strobe (IRAS–) to strobe seven address bits into the selected memory banks
- Column address select (ICADSEL) to select the second set of seven address bits
- Column address strobe (ICAS–) to strobe the second set of address bits, the 16 data bits, and the six check bits generated by the 96KB memory controller check logic in the selected memory bank. The memory timer also generates the TILINE terminate (TLTM–) to the TILINE bus.

The data word is steered to either the odd or even row of the selected bank by the ADODD signal that is generated by the 96KB memory controller from the least significant TILINE address bit, TLADR19–. The time from receipt of TLGO– to transmission of TLTM– is typically 370 nanoseconds.

Memory Read Cycle. To execute a memory read cycle, the TILINE master device asserts TLGO– low and TLREAD high. The master also generates a valid address on the address lines. The address is decoded and interrogated. The row address strobe (RAS–), column address select (ICADSEL), and the column address strobe (ICAS–) are generated and used in the same manner described for the memory write cycle. Both the odd and even rows of the selected bank are accessed. The data word that is returned to the 96KB memory controller is specified by the ADODD control line as it generates either of two enabling signals, EVOUT– or ODOUT–. This line may be toggled after the first data word has been latched to provide the alternate word for cache storage. The odd-even words are contiguously addressed, with the odd word always being the next higher word addressed. The time from receipt of TLGO– to transmission of TLTM– is typically 445 nanoseconds if no error is detected in the data accessed from memory, and 570 nanoseconds if an error is detected and error correction logic is enabled. If the correction logic on the 96KB memory controller determines that the error is not correctable, the accessed data is not modified and TILINE memory error (TLMER–) is asserted in addition to TLTM–.

Memory Refresh. Refresh timing for the 256KB add-on memory is controlled by the 96KB memory controller that must produce 128 refresh cycles for each refresh period. For each refresh cycle, the 96KB memory controller provides the refresh address (RFAD0 through RFAD6), the REFRESH signal, and the row address strobe (IRAS–). The REFRESH signal applied to the board/bank address decoder on the 256KB add-on memory board in turn generates the board selected IBSEL– signal that is sent to the 96KB memory controller. All the memory banks on the memory array are refreshed simultaneously. While in standby mode, only the circuitry required to maintain the integrity of the refresh logic is powered by the power supply battery. Refresh requests are generated at the same rate as when main power is on. When a request occurs, the required address and control logic is switched on and the cycle is executed. The address and control logic is switched off at the completion of each single cycle.

3.4 EPROM EXPANSION MEMORY OPTION

An optional EPROM (erasable programmable read only memory) expansion memory board is also available for use in 990/10 systems. The EPROM module contains the control/interface circuitry and IC sockets to accommodate from 2K to 16K of 8-bit bytes (field expandable) of additional memory. Each 2KB of memory requires 2 INTEL 2708 1024 by 8-bit EPROM chips. These EPROM chips may be removed from the board and programmed using a Model 990 PROM Programmer.

3.4.1 EPROM MEMORY MODULE JUMPER OPTIONS. The computer type (990/10 or 990/4), board starting address, and amount of memory must be set up on the board as described in figures 3-73 and 3-74.

3.4.2 EPROM MEMORY MODULE FUNCTIONAL DESCRIPTION. The EPROM module consists of four major sections including:

- Memory Addressing Section
- Memory Timing and Control
- -5V Regulator Section
- EPROM Memory Banks

The operation of these circuits is described in the following paragraphs.

3.4.2.1 Memory Addressing Section. A simplified logic diagram of the EPROM module's address section is shown in figure 3-75. As shown in the figure, the ten most significant bits of the TILINE address are inverted and routed to one of the two inputs in a network of adder chips (functioning as subtracters). The adjustable board starting address for the module is set up in one's complement form using switches S1 and S2 (figures 3-73 and 3-74). The chips U17, U28 and the U19 gates compare each TILINE address with the starting address bits and produce the logic-high signals TLGTEMIN1 and TLGTEMIN2 when the memory address is greater than or equal to the board's programmed starting address.

The memory capacity is also programmed on the board via jumper straps on terminals E1 through E9 as listed in figure 3-74.

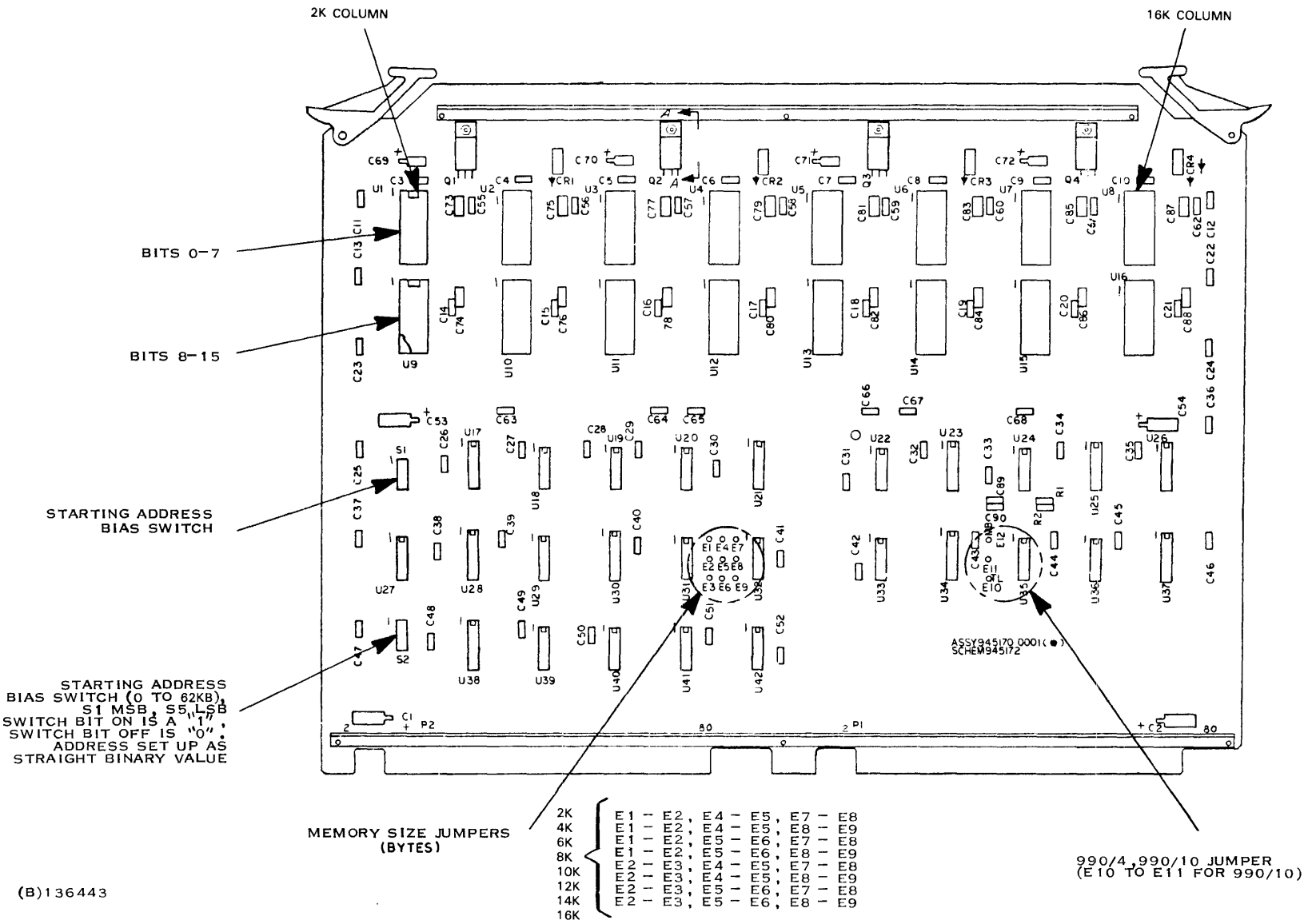


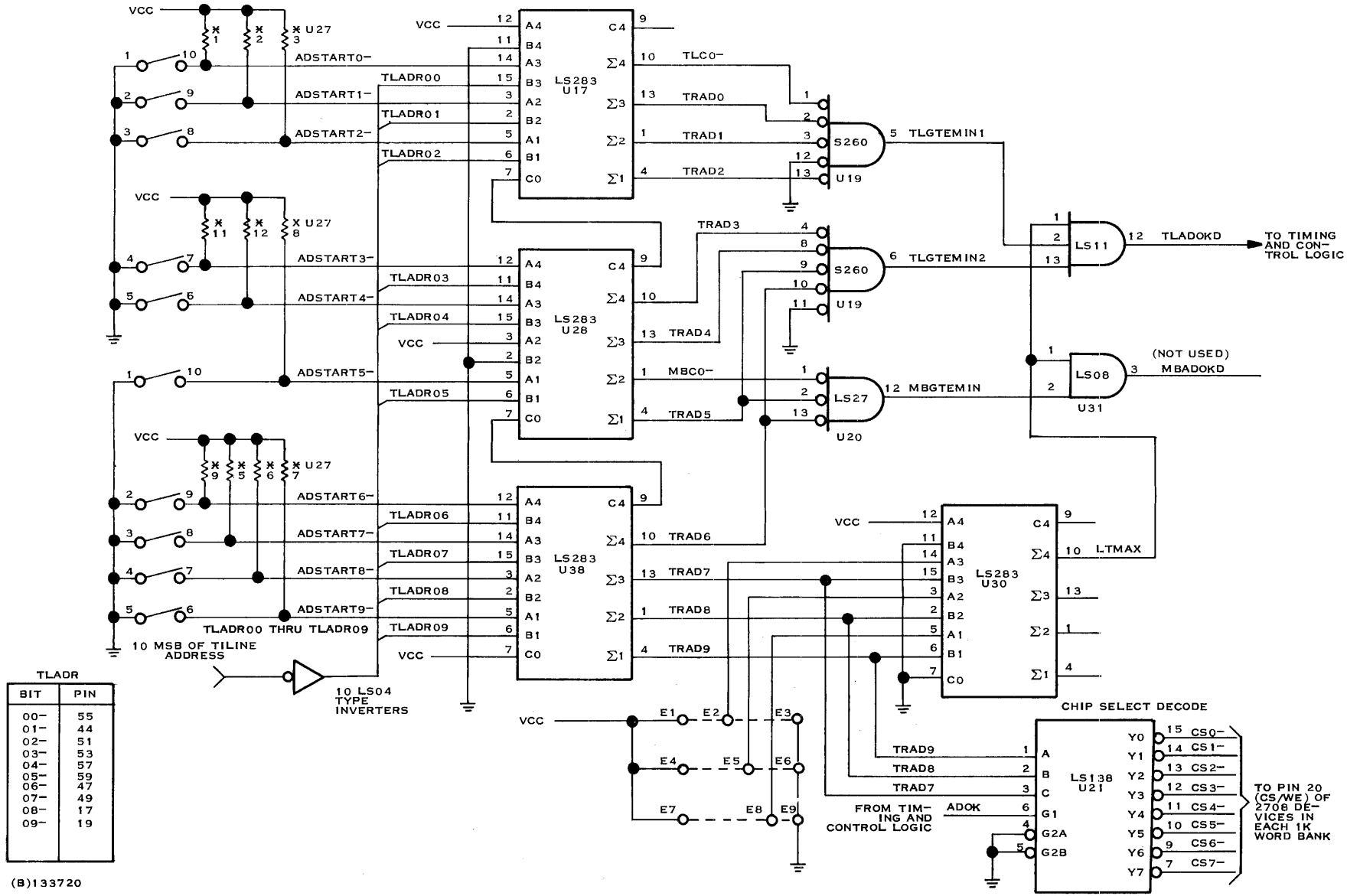
Figure 3-73. EPROM Memory Module Options

Starting Address (Hex Byte Addresses)		Bias Switch Setting S1	S2	S3	S4	S5	Starting Address (Hex Byte Addresses)		Bias Switch Setting S1	S2	S3	S4	S5
0000	(0)	off	off	off	off	off	9000	(18K)	on	off	off	on	off
0800	(1K)	off	off	off	off	on	9800	(19K)	on	off	off	on	on
1000	(2K)	off	off	off	on	off	A000	(20K)	on	off	on	off	off
1800	(3K)	off	off	off	on	on	A800	(21K)	on	off	on	off	on
2000	(4K)	off	off	on	off	off	B000	(22K)	on	off	on	on	off
2800	(5K)	off	off	on	off	on	B800	(23K)	on	off	on	on	on
3000	(6K)	off	off	on	on	off	C000	(24K)	on	on	off	off	off
3800	(7K)	off	off	on	on	on	C800	(25K)	on	on	off	off	on
4000	(8K)	off	on	off	off	off	D000	(26K)	on	on	off	on	off
4800	(9K)	off	on	off	off	on	D800	(27K)	on	on	off	on	on
5000	(10K)	off	on	off	on	off	E000	(28K)	on	on	on	off	off
5800	(11K)	off	on	off	on	on	E800	(29K)	on	on	on	off	on
6000	(12K)	off	on	on	off	off	F000	(30K)	on	on	on	on	off
6800	(12K)	off	on	on	off	on	F800	(31K)	on	on	on	on	on
7000	(14K)	off	on	on	on	off							
7800	(15K)	off	on	on	on	on							
8000	(16K)	on	off	off	off	off							
8800	(17K)	on	off	off	off	on							

Memory Size (Bytes)	Jumpers Required
2K	E1 to E2; E4 to E5; E7 to E8
4K	E1 to E2; E4 to E5; E8 to E9
6K	E1 to E2; E5 to E6; E7 to E8
8K	E1 to E2; E5 to E6; E8 to E9
10K	E2 to E3; E4 to E5; E7 to E8
12K	E2 to E3; E4 to E5; E8 to E9
14K	E2 to E3; E5 to E6; E7 to E8
16K	E2 to E3; E5 to E6; E8 to E9

Computer Type	Jumper Required
990/4	E11 to E12; E10 open
990/10	E10 to E11; E12 open

Figure 3-74. EPROM Memory Module Jumper Options



TLADR BIT	PIN
00–	55
01–	44
02–	51
03–	53
04–	57
05–	59
06–	47
07–	49
08–	17
09–	19

(B)133720

Figure 3-75. Address Examination and Decoding Simplified Logic

The signals produced by that strapping are supplied to adder U30 that also receives output signals (TRAD7-TRAD9) from adder U38 representing the difference between the TILINE address bits and the board starting address. If the highest board memory address exceeds the relative input address from U38, adder U30 supplies a high LTMAX (less than max) output signal. An incoming TILINE address within the board's range of addresses thus produces simultaneous high signals at the input of the U41 AND gate. AND gate U41 then produces a high TLADOKD (TILINE address OK – delayed) signal for the timing and control logic.

3.4.2.2 Timing and Control Circuits. A simplified logic diagram for the EPROM Expansion Board timing and control appears in figure 3-76. Two signatures are used on some lines; the first for TILINE operation and the second for 9900 bus operation. The U34 transceiver serves to interface the slave device logic on the board with the TILINE. Delay network DLY1 delays GO for 95 ns to permit the examination of the TILINE address by the address examination logic and the generation of a stable TLADOKD signal. D type FF U33 (reset by GO) receives the delayed DGO as a clocking input for freezing the TLADOKD input to produce the TLADOK signal. TLADOK is applied to another delay network DLY2 that produces the termination (TM) signal after a delay of 405 ns. These signals, along with TLREAD obtained from a U22 D-type FF, are applied to the inputs of the data selector U23. Connecting a jumper from E11 to E10 adapts the board for TILINE (990/10) operation by grounding the SEL input so that the A inputs are passed through to the Y outputs as indicated. The TM output of U23 is applied to transceiver U34 that supplies the TLTM– signal to the TILINE. The ADOK and READ signals are applied to a U43 NAND gate to produce a low VLDADOK– output that drives sixteen 3-state drivers. The drivers send valid data from the EPROM devices to the TILINE.

The READ signal also drives a U40 inverter that produces READ–. If an attempt is made to write at a valid EPROM Expansion Board address, READ– and ADOK are both high, setting the interrupt FF and ultimately generating the interrupt signal INTA–. The interrupt FF is later reset under software control from the CPU via the IORESET signal derived from the TLIORES signal. Since READ is low for a write attempt, VLDADOK– is not generated and no data from the EPROM devices is transmitted to the TILINE.

3.4.2.3 -5V Regulators. Four LM320 negative voltage regulators provide the -5V inputs required by the 2708 devices. A diagram of one of the regulator circuits appears in figure 3-77.

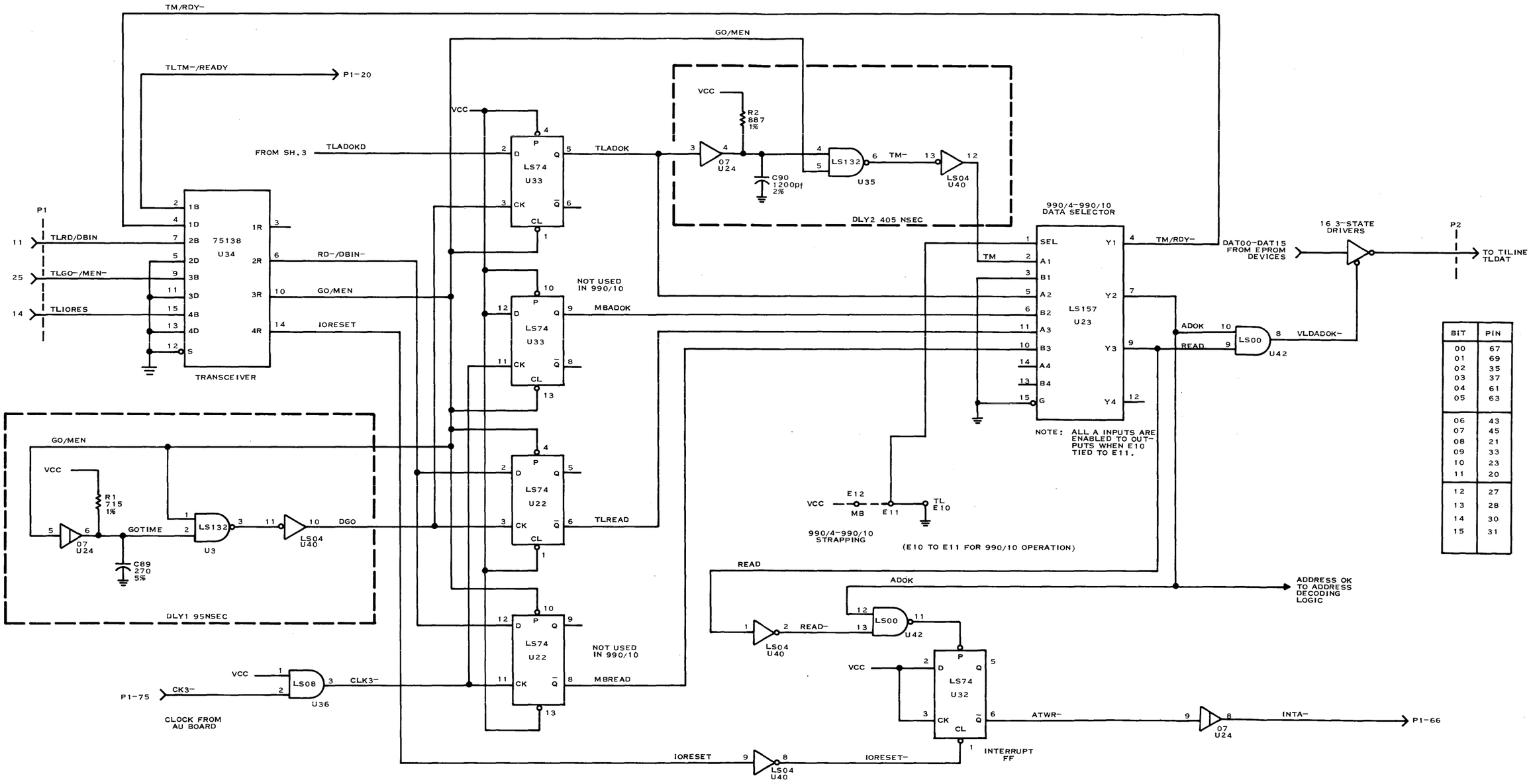
The output of the -12-volt section of the power supply is applied to the regulator circuits via the indicated terminals on P1 and P2. Diode CR1 is back biased by normal circuit polarities but conducts to prevent the development of a damaging reverse voltage across the regulator Q1 (due to voltage across capacitors C73-C76) when the -12-volt input is removed.

3.5 990/10 CHASSIS

The three printed circuit boards of the 990/10 minicomputer may be installed in either the six-slot chassis or the thirteen-slot chassis. The configurations of each chassis are discussed in the paragraphs that follow.

3.5.1 SIX-SLOT CHASSIS. The 6-slot chassis provides full support that includes backplane wiring, power, and cooling air for six full-sized logic boards. Two half-sized logic boards may be substituted for one full-sized board in any slot except the initial slot that is wired to accept the AU2 circuit board.

The 6-slot chassis is available in two different configurations; one configuration is supplied with an operator front panel assembly and the other with a programmer front panel assembly. The operator front panel assembly is basically a blank panel with indicators and switch as shown in figure 3-78. The programmer front panel is intended for use in applications requiring software troubleshooting. Panel controls may be locked out by a key-operated switch to prevent inadvertent use of the controls. A detailed description of the programmer panel is provided in paragraph 3.7.



BIT	PIN
00	67
01	69
02	35
03	37
04	61
05	63
06	43
07	45
08	21
09	33
10	23
11	20
12	27
13	28
14	30
15	31

Figure 3-76. Timing and Control, Simplified Logic Diagram

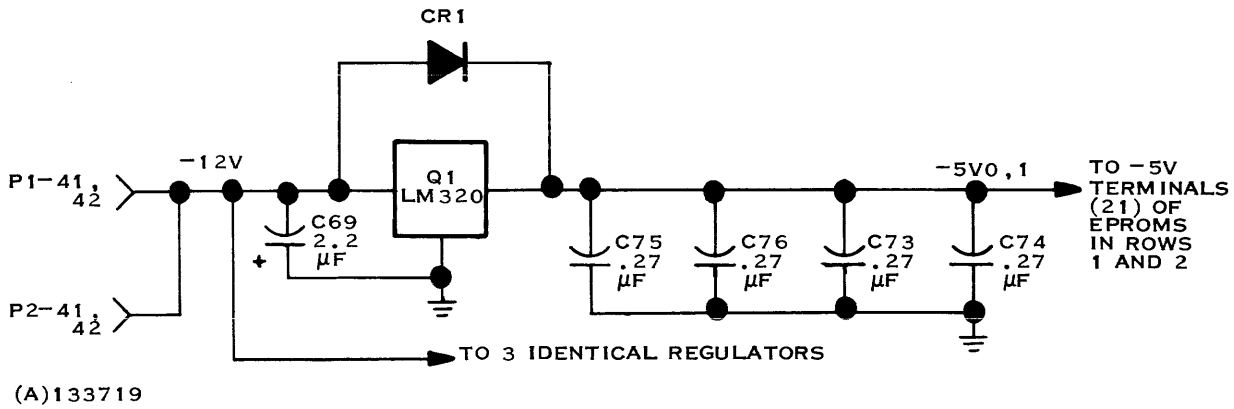


Figure 3-77. Circuit of Typical -5V Regulator on EPROM Expansion Board

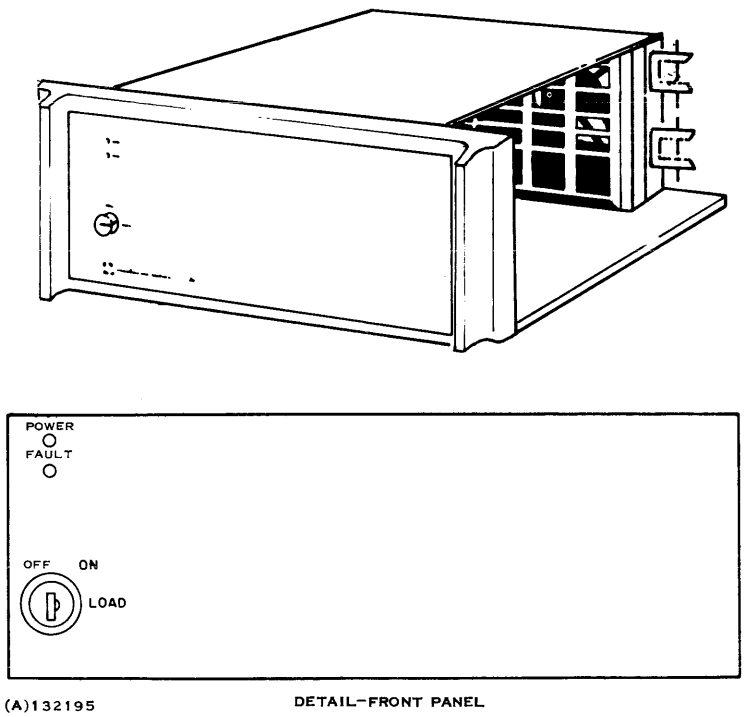


Figure 3-78. Operator Front Panel, 6-Slot Chassis

The CRU and TILINE signals are distributed to the individual chassis slots on backplane wiring.

The 6-slot chassis includes the card support and backpanel for the 6 slots, an ac power converter, a 20-ampere power supply, and two fans for cooling. The chassis will support a 170-watt heat load in the power supply area and a 50-watt heat load for each full-sized board position. The maximum temperature of exhaust air is designed to be 65 degrees Celsius (149 degrees Fahrenheit) for manufacturing and office installations.

A chassis slide kit or table top chassis option are available. The chassis slide kit consists of chassis slides and hardware for mounting the chassis in a standard 482.60-millimetre (19-inch) RETMA rack. The table top chassis option consists of a table top enclosure cover with mounting brackets to provide a dust proof enclosure for desk or table top operation.

A 230 VAC option kit consisting of a transformer and necessary hardware permits the chassis to be operated from 100V, 200V, or 230V ac line voltages.

A standby power supply to provide standby power for volatile memory protection in the event of a primary power failure is available as an option. The standby power supply consists of batteries and a standby power supply/charger that installs in either the 6-slot or 13-slot chassis in the area behind the backpanel reserved for the power supply. The unit supplies +5 MEM, +12 MEM, and -5 MEM power. A detailed description of the standby power supply is provided in paragraph 3.8.3. The 20-ampere power supply is an offline ringing choke (sometimes referred to as flyback) dc to dc converter. A detailed description of the power supply is provided in paragraph 3.8.2.

The ac power converter full-wave rectifies the primary ac input to the chassis to provide 160-volt dc input power to the 20-ampere power supply and to the standby power supply (if that option is implemented). A second full-wave rectifier develops a 120-Hz pulse that is optically coupled to the 20-ampere power supply where it is further refined and furnished as the line frequency synchronized real time clock interrupt signal to the system interface board. A detailed description of the ac power converter is provided in paragraph 3.8.1. The physical configuration and dimensions of the 6-slot chassis are as shown in figure 3-79. Chassis wiring for the 6-slot chassis is as shown in figure 3-80.

3.5.2 THIRTEEN-SLOT CHASSIS. The thirteen-slot chassis is basically an enlarged version of the six-slot chassis and will provide full support (backplane wiring, power, and cooling) for thirteen full-sized logic boards. Two half-sized boards may be substituted for one full-sized board in all but the initial three slots reserved for the AU1, AU2, and memory boards. The thirteen-slot chassis is also available in either the operator front panel or programmer front panel configuration but is not available in the table top chassis option. Other characteristics of the thirteen-slot chassis are as described for the six-slot chassis in paragraph 3.5.1.

The physical configuration and dimensions of the 13-slot chassis are as shown in figure 3-81. Chassis wiring for the 13-slot chassis is as shown in figure 3-82.

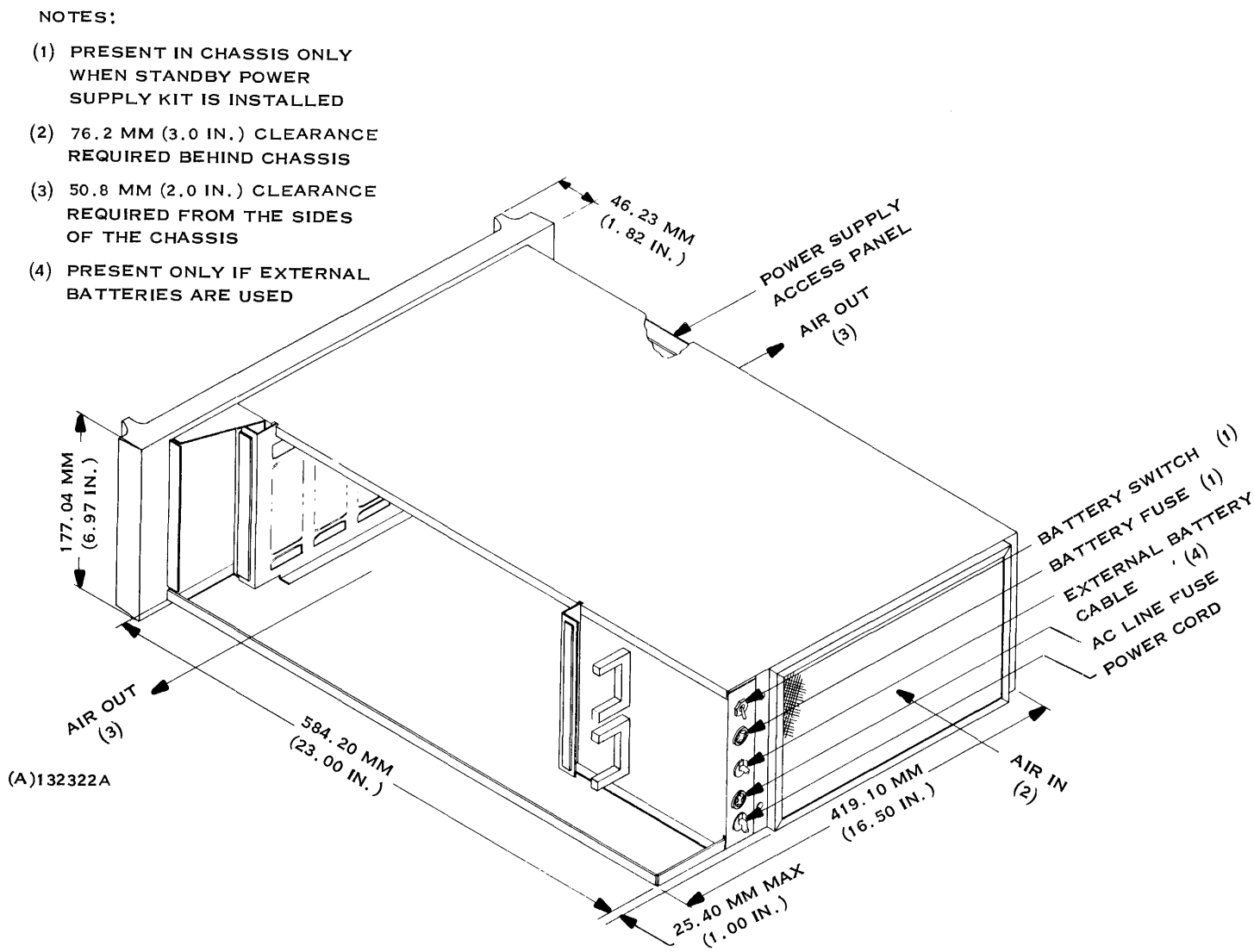


Figure 3.79. Physical Configuration for 6-Slot Chassis

3.6 CRU EXPANSION

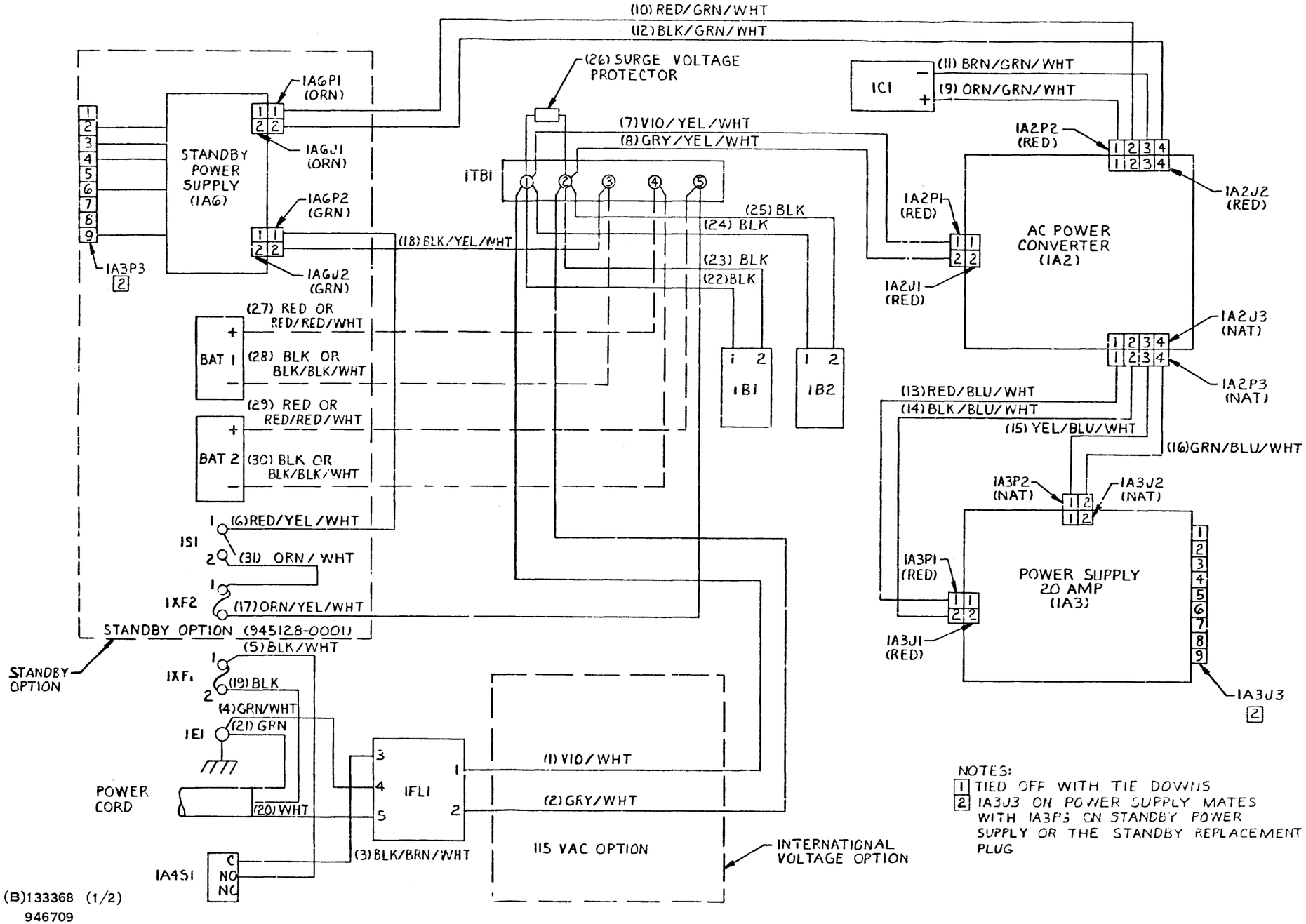
From one to seven 990 I/O expansion chassis may be added to a 990 system when the main chassis does not contain enough board slots to house all of the required CRU interface boards. The chassis used as an I/O expansion chassis is identical to the main computer chassis except that it contains an operator panel instead of a programmer panel and slot 1 of the expansion chassis houses a CRU buffer board instead of an AU2 board. Also, the interrupt wiring for the expansion chassis is accomplished through jumper plugs on the backpanel board identical to that for the main chassis. The dc power supplies in the expansion chassis are identical to the power supply used in the main chassis except that a standby supply is not used with an expansion chassis.

The operator panel on the expansion chassis contains a key switch which controls ac power to the chassis and a POWER LED which indicates when the power supplies are functioning properly. The interconnection between the operator panel and the CRU buffer board is accomplished through a 26-pin ribbon cable and connector which attaches to connector plug P5 on the top edge of the buffer board. The interface between the main chassis and the expansion chassis is accomplished through a 3.66 metre (12-foot) ribbon cable (Part Number 945001-1) which attaches to one of the seven ports on the CRU expansion board in the main chassis (P3 through P9, depending on chassis number) and attaches to plug P3 on the top edge of the CRU buffer board in the expansion chassis. A simplified block diagram of the CRU expansion system is shown in figure 3-83.

3.6.1 EXPANSION CHASSIS INTERRUPT SCHEME. A simplified block diagram of the interrupt system associated with a fully expanded 990/10 system is shown in figure 3-84. As indicated in this figure, interrupts from each half-board slot in a given expansion chassis are wired to the interrupt jacks J2 and J3 on the backpanel board. These interrupt lines are then jumpered to selected interrupt levels 1 through 15 using wire jumpers on the backpanel board. The 15 interrupt levels are routed to an interrupt scanner on the CRU buffer board which is located in slot 1 of the expansion chassis. If an interrupt is received on any of the 15 interrupt levels, the CRU buffer board issues an interrupt present to the CRU expander board in the main chassis. The CRU expander board then responds to the interrupting chassis (having highest priority) with an ID enable signal. This enable is used to gate the four ID bits (which represent the binary value of the interrupt level) back to the CRU expander board. In response to an interrupt request from any of the seven chassis, the CRU expander board issues either an interrupt A (interrupt present in chassis 1-4), an interrupt B (interrupt present from chassis 5 through 7) or an interrupt C (direct interrupt present from interrupt chassis 1 through 7).

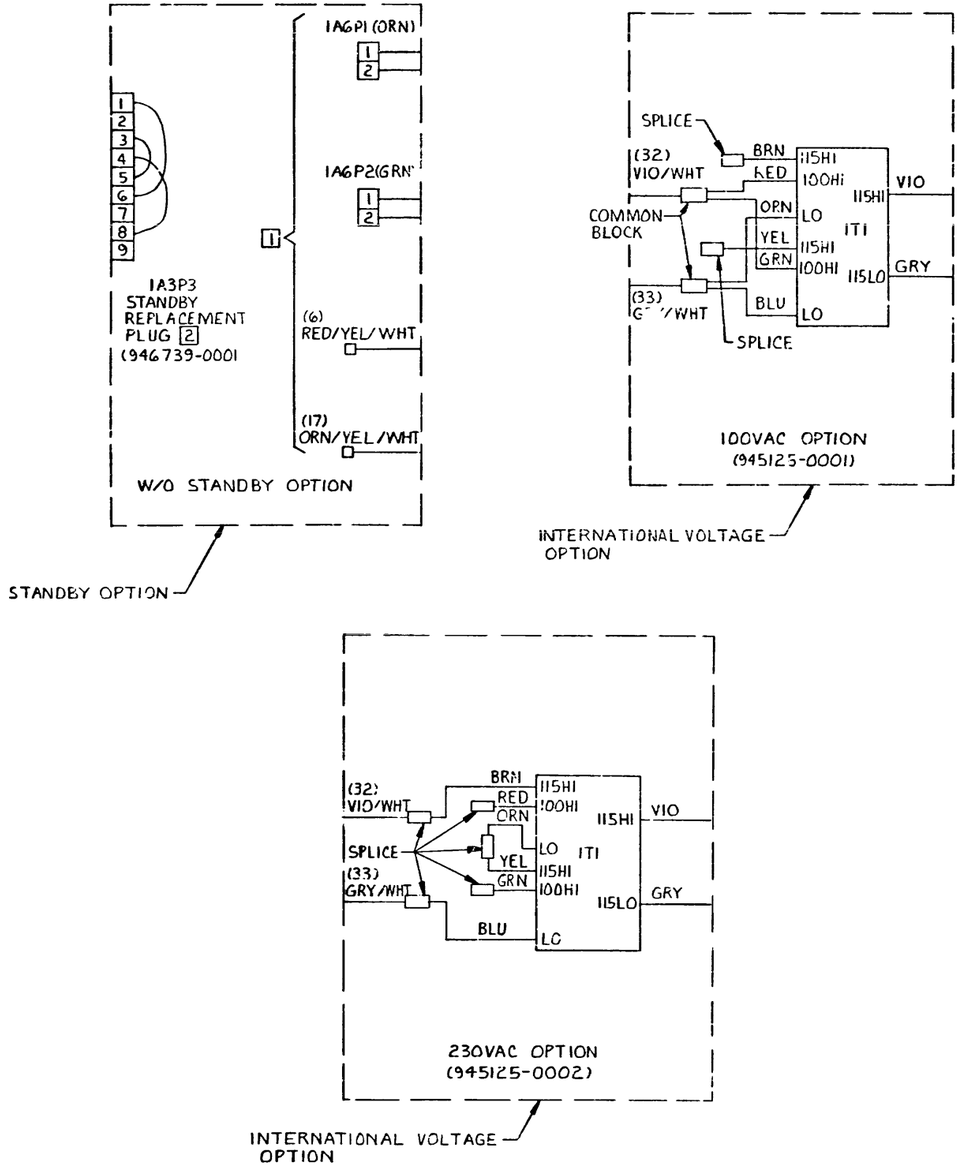
Interrupts A and B are used to activate the expander interrupt servicing routine in the microcomputer which, in turn, addresses the appropriate interrupt servicing section (A or B) with a store CRU instruction addressed to either $F80_{16}$ (interrupt A) or $F90_{16}$ (interrupt B). As a result of the store CRU instruction, a 16-bit interrupt vector is sent back to the microprocessor. As shown in figure 3-85, the interrupt vector contains the ID of the originating unit (developed by the CRU buffer board in the interrupting chassis), the ID of the expansion chassis (developed in the CRU expander board) and the status of the expansion chassis associated with the reporting interrupt section (chassis 1-4 associated with interrupt section A and chassis 5-7 associated with section B). The interrupt vector is then used to select the proper device interrupt servicing routine associated with the interrupting board.

If a direct interrupt (INT C–) is generated, the interrupt is processed more speedily since the expansion interrupt servicing routine is bypassed and the microprocessor traps directly to the board-level interrupt servicing routine. This interrupt scheme is used when peripherals requiring rapid response to interrupts are located in the expansion system.



NOTES:
[1] TIED OFF WITH TIE DOWNS
[2] 1A3J3 ON POWER SUPPLY MATES WITH 1A3P3 ON STANDBY POWER SUPPLY OR THE STANDBY REPLACEMENT PLUG

Figure 3-80. Wiring Diagram for 6-Slot Chassis (Sheet 1 of 2)



(B)133368 (2/2)
946709

Figure 3-80. Wiring Diagram for 6-Slot Chassis (Sheet 2 of 2)

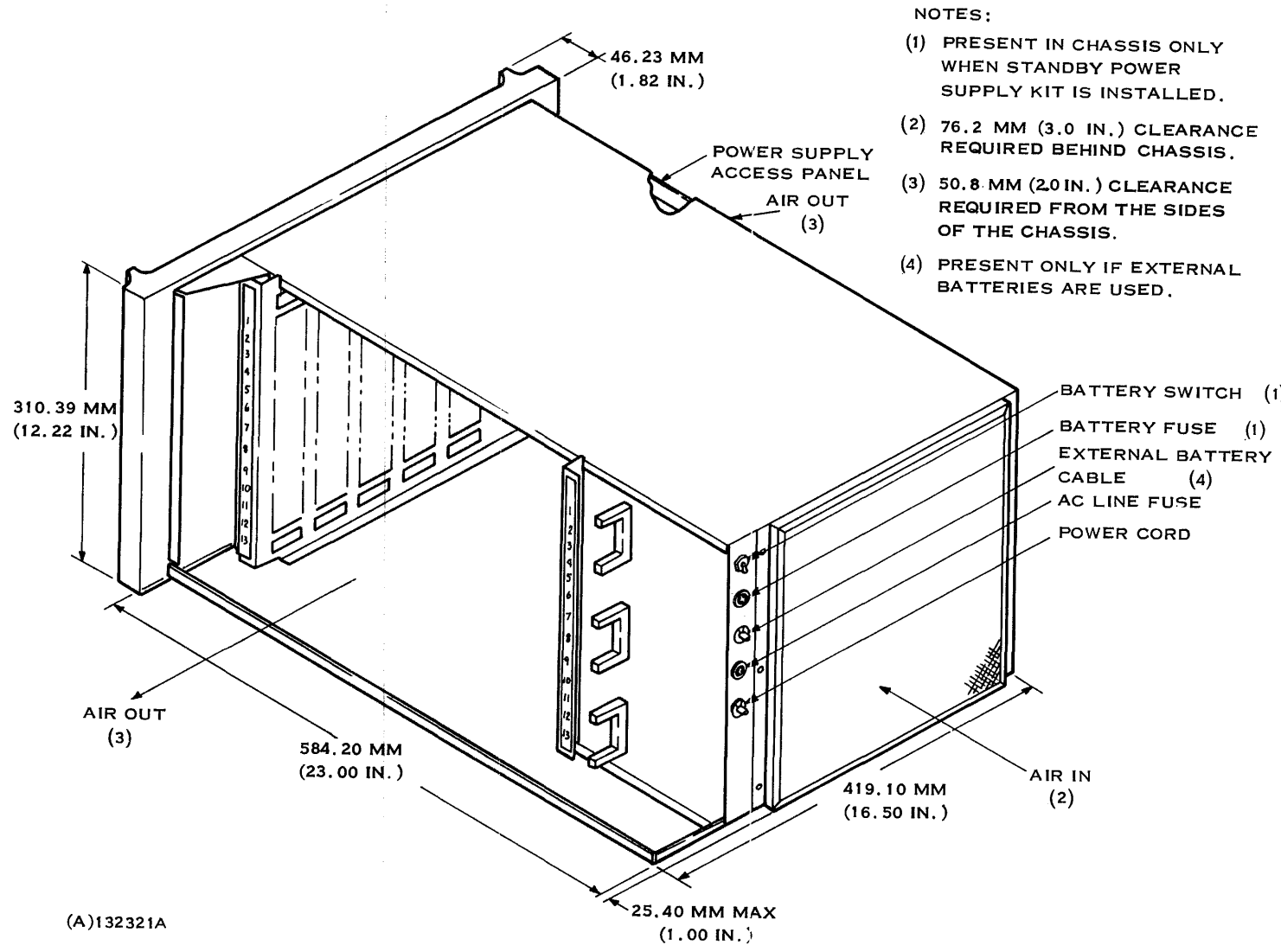
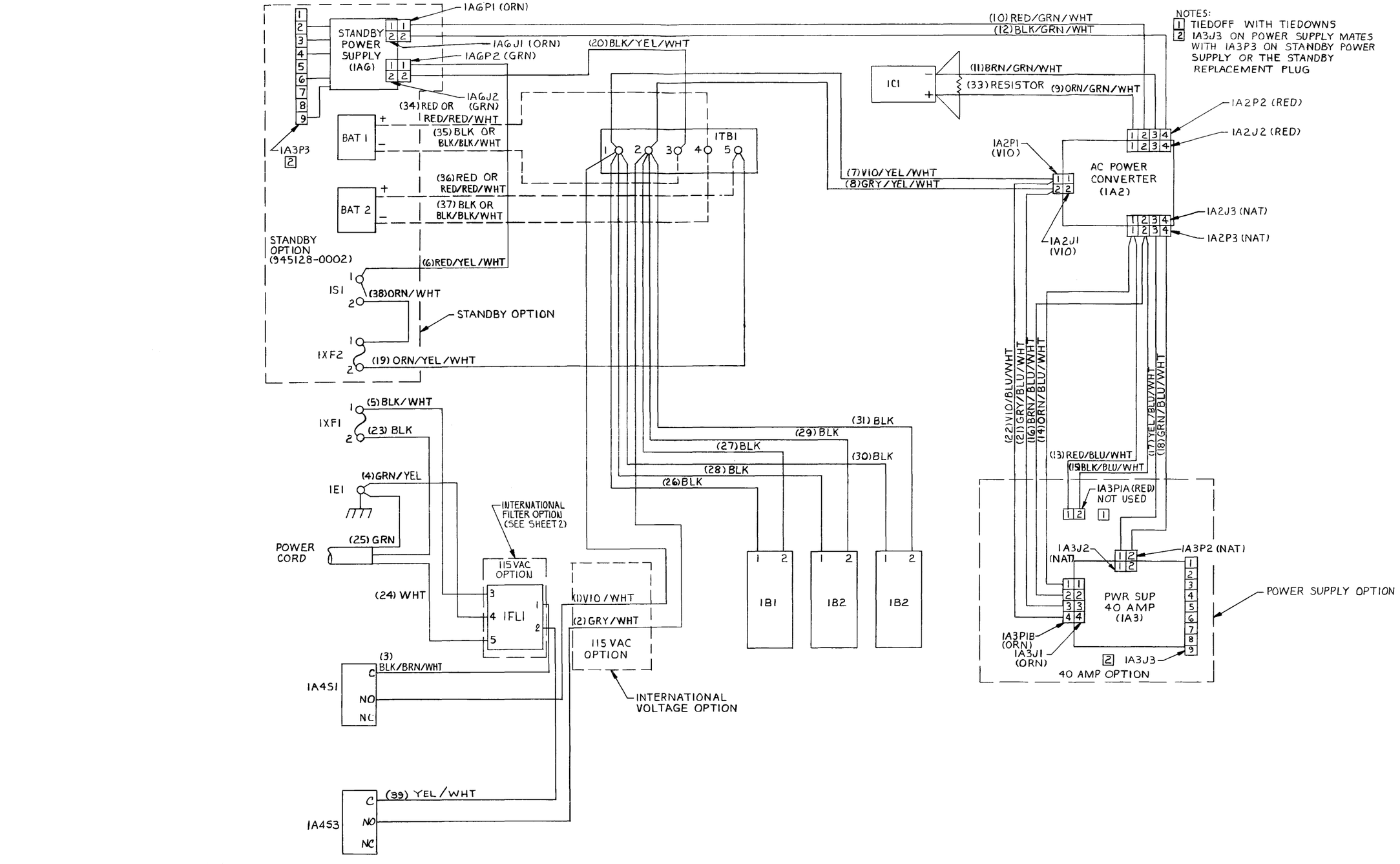
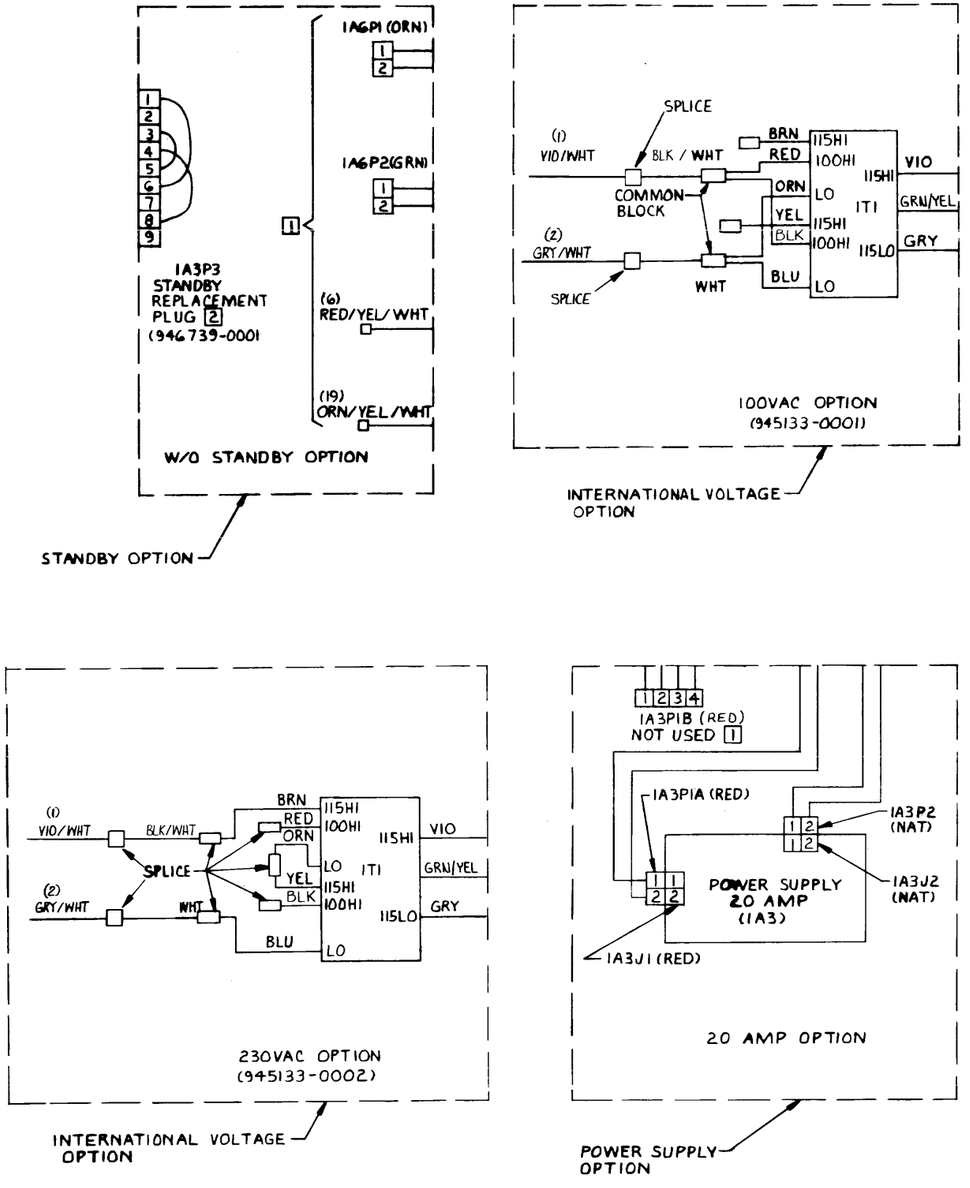


Figure 3-81. Physical Configuration for 13-Slot Chassis



(B)133195A (1/2)
946736

Figure 3-82. Wiring Diagram for 13-Slot Chassis (Sheet 1 of 2)



(B)133195A (2/2)
946736

Figure 3-82. Wiring Diagram for 13-Slot Chassis (Sheet 2 of 2)

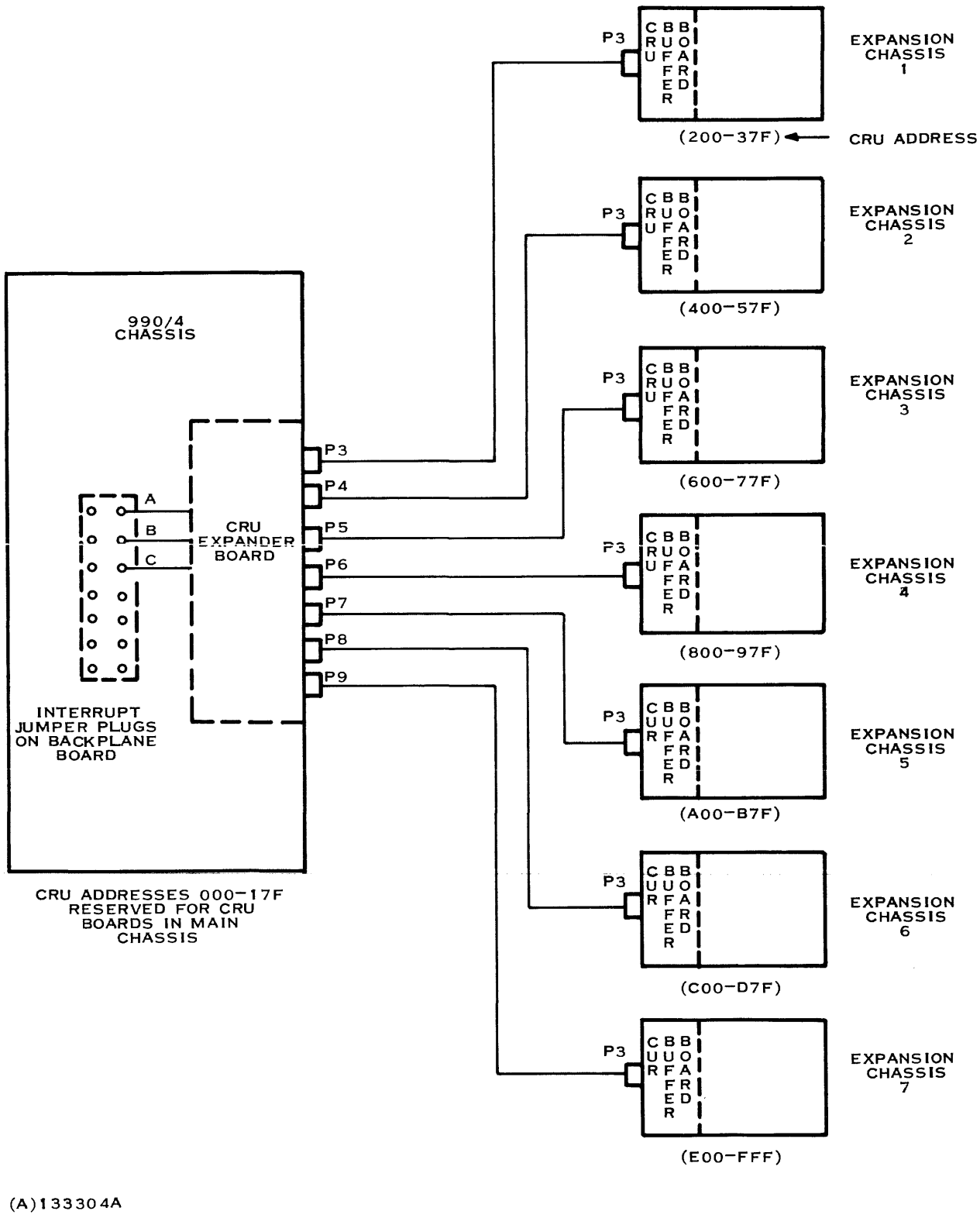


Figure 3-83. CRU Expansion, Simplified Block Diagram

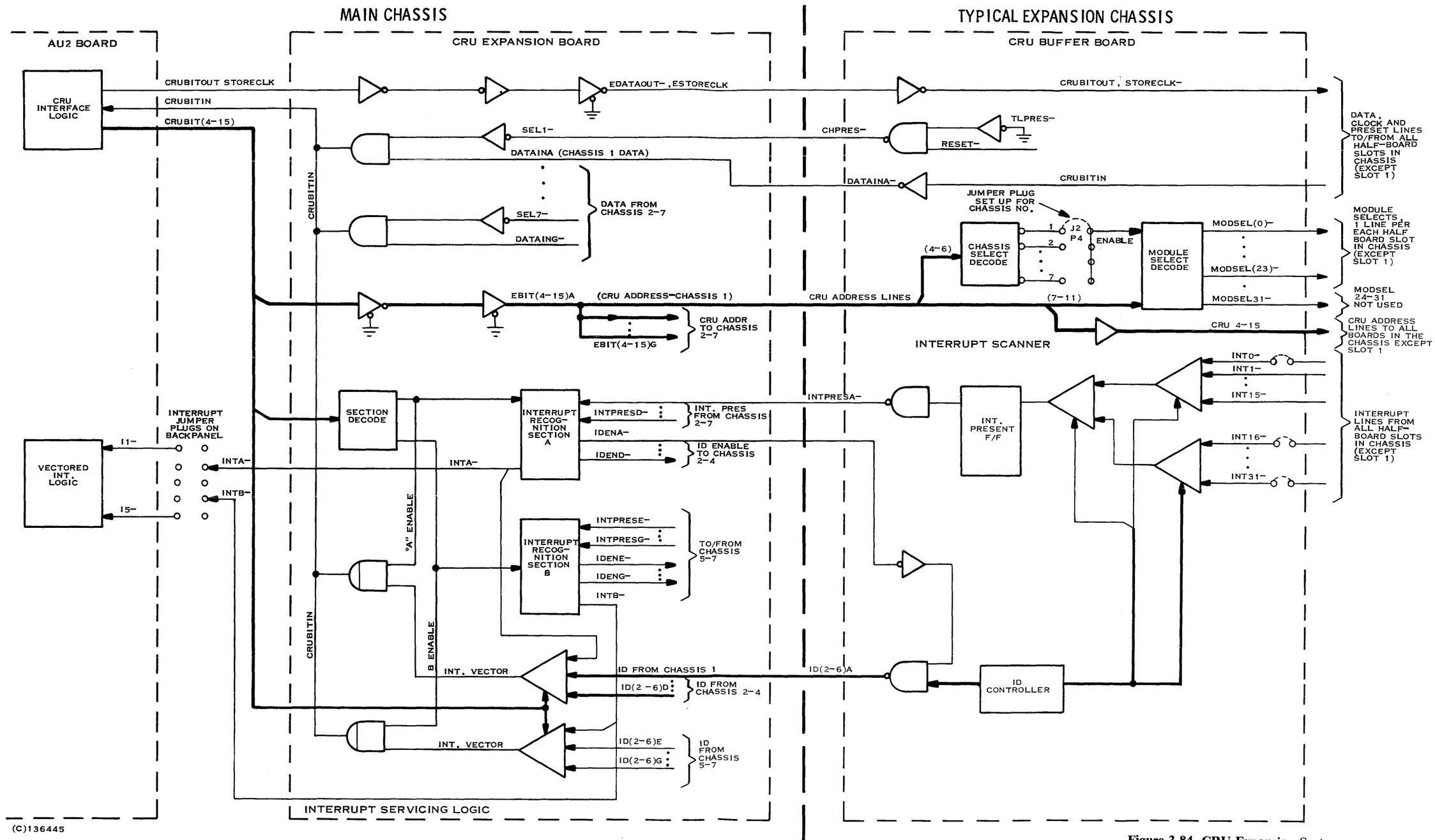


Figure 3-84. CRU Expansion System, Functional Diagram

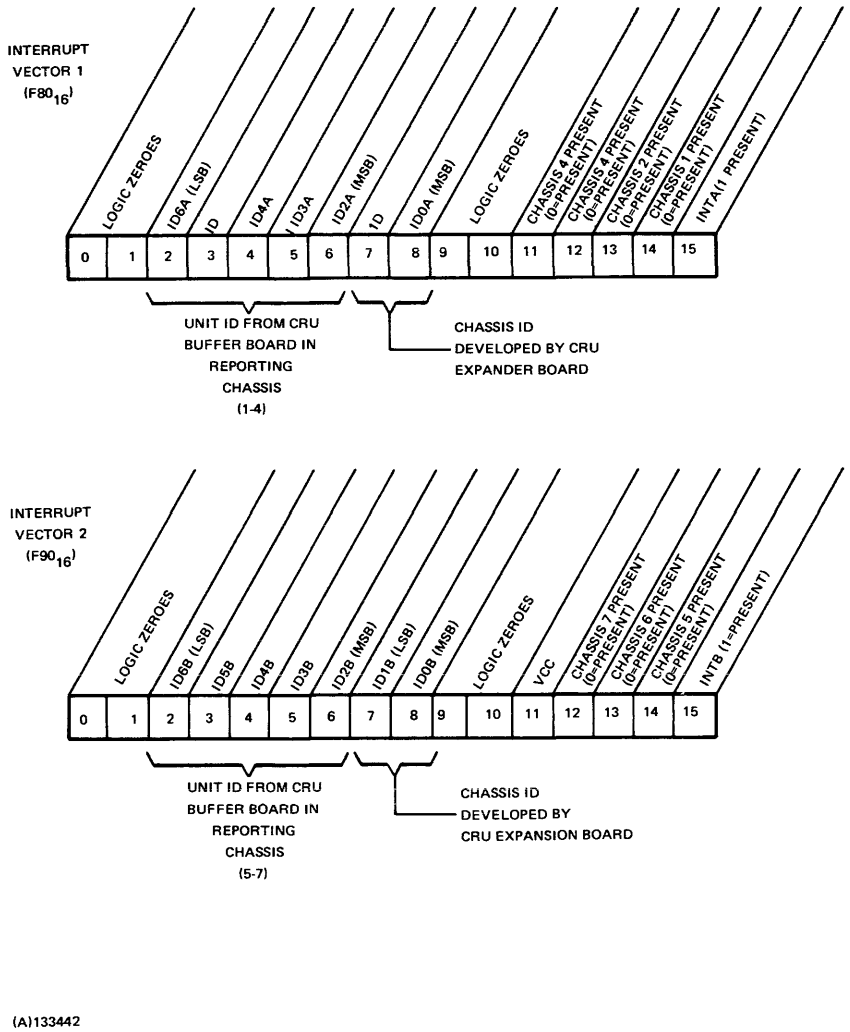


Figure 3-85. Expansion Interrupt Vector Format

3.6.2 CRU EXPANSION ADDRESS SCHEME. A CRU address map for the standard fully expanded system is shown in figure 3-30. As indicated in this figure, each chassis is assigned a band of location-dependent CRU addresses which are used to address the CRU interface boards implemented within a given chassis. The chassis number (1 to 7) which is assigned to each chassis is determined by an ID plug on the CRU buffer board.

3.6.3 CRU EXPANSION BOARDS. The CRU expansion system requires two board types including the CRU expander board and the CRU buffer board. These two boards are briefly described in the following paragraphs.

3.6.3.1 CRU Expander Board. The CRU expander board, part number 945005-1, basically expands the CRU present at the main chassis backpanel to drive up to seven expansion chassis. The board is equipped with buffer/drivers for fanout of data and control lines and contains interrupt processing logic to report interrupts to the microprocessor.

A functional block diagram of the CRU expander board, complete with inteface pin numbers, is shown in figure 3-86. As indicated in this diagram, the CRU expander consists of two major sections including:

- CRU Fanout Logic
- Interrupt Recognition Logic

CRU Fanout Logic. The CRU expansion board provides a 1 by 7 fanout of the following CRU interface signals:

- TLIORES– (or TLPRES– using jumper option)
- CRUBITOUT
- CRUBIT (4-15)
- STORECLK–

Each of these signals, with the exception of STORECLK–, is buffered and series terminated. STORECLK– is driven by a power gate which requires parallel termination in the CRU buffer board in the receiving chassis.

Interrupt Recognition Logic. The interrupt recognition logic on the CRU expansion board is functionally divided into two sections, A and B. Section A monitors the interrupt lines from chassis 1-4 and reports interrupts to the computer over the INTA– line. Section B monitors the interrupts from expansion chassis 5-7 and reports interrupts over the INTB– line.

The interrupt request lines (INTREQ–) from all chassis are wire-ORed together, buffered and sent to the computer as INTC–. The direct interrupt feature is used when faster interrupt processing response time is required by a peripheral in an external chassis.

When an interrupt present (INTPRES–) is detected by one of the two interrupt recognition sections, it develops a 2-bit binary word (ID(0,1)) which corresponds to the highest priority interrupt present. This binary word is decoded to send a logic-low ID enable signal (IDEN–) to the selected requesting chassis. The ID enable is a request for the external chassis's CRU buffer board to send back the ID word (ID(2-6)) which identifies the board in the external chassis that initiated the interrupt.

In a similar fashion, Section B of the interrupt recognition logic monitors and processes the interrupts from chassis 5 through 7. Provisions are incorporated on the board to permit software to address either the A or B interrupt section via an STCR addressed to either $F80_{16}$ (section A) or $F90_{16}$ (section B). Then by manipulating the CRU address lines 12-15, software is able to serially transfer a full 16-bit interrupt vector from either interrupt section to computer memory via the CRUBITIN data line. The interrupt vector format is shown in figure 3-85.

Note that the vector includes the encoded binary word (ID(0,1)) developed by the interrupt sections, the ID word returned from the external chassis and the chassis present (SEL–) lines from each expansion chassis (if a chassis is connected, its associated SEL– line will be a logic 0 level).

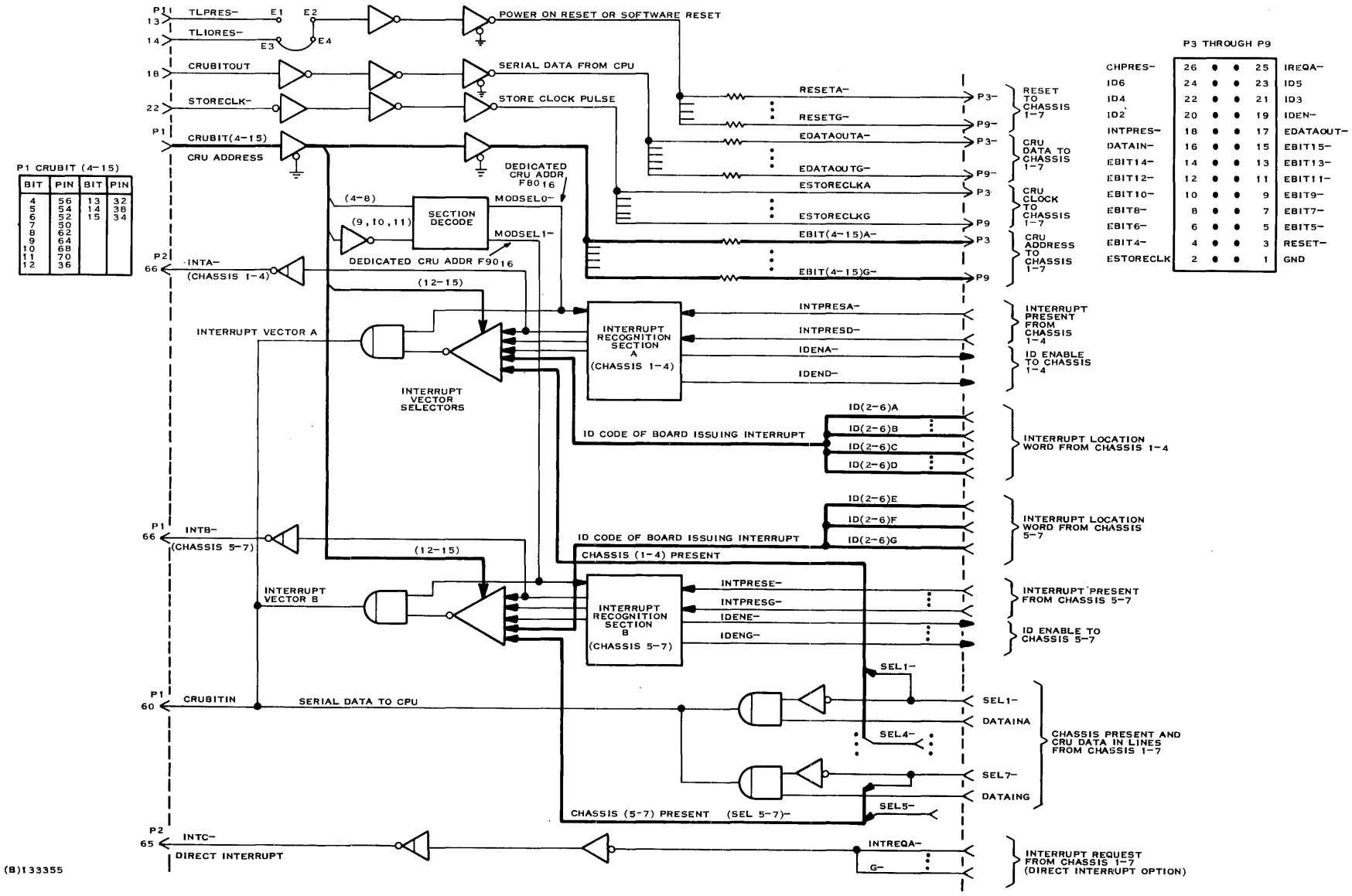


Figure 3-86. CRU Expander Board Block Diagram

3.6.3.2 CRU Buffer Board. Each expansion chassis is equipped with a CRU buffer board in slot 1. Basically, the CRU buffer board performs a module select decode and CRU fanout/fanin function similar to that performed by the CRU interface logic on the AU2 board. The buffer board decodes CRU address lines from the main chassis (via the 990 CRU expansion board) to generate the low-active Module Select signals for the CRU interface boards within the expansion chassis.

The board also buffers the CRUDATAOUT, CRUSTORECLK, TLIORES– and CRUBITOUT lines between the main chassis and all CRU slots in the expansion chassis.

An interrupt scanner circuit on the buffer board (figure 3-87) continuously monitors for the presence of interrupts from any of the CRU buffer boards in the chassis and issues an Interrupt Present (INTPRES—) if an interrupt is detected on any line. The buffer board then enables the ID word (ID(2-6)) which identifies which board in the expansion chassis issued the interrupt when ID Enable signal (IDENA) is received from the CRU expansion board.

Interrupt Scanner Logic. The CRU buffer board contains provisions for encoding up to 32 interrupts onto a single interrupt line to the CRU expander board and supplying the expander board, on request, the ID of the board which originated the interrupt. However, in the present 13-slot chassis, only the first 15 interrupt lines (INT(1-15)–) are actually connected to the scanner circuitry.

The interrupt scanner consists of a clock oscillator stage (U21, U10 plus R1 and C1), a 5-bit counter (U11 and U12), two 16-bit multiplexer stages U1 and U2, a multiplexer selector U17, interrupt present flip-flop stage U22, and output driver stage U15.

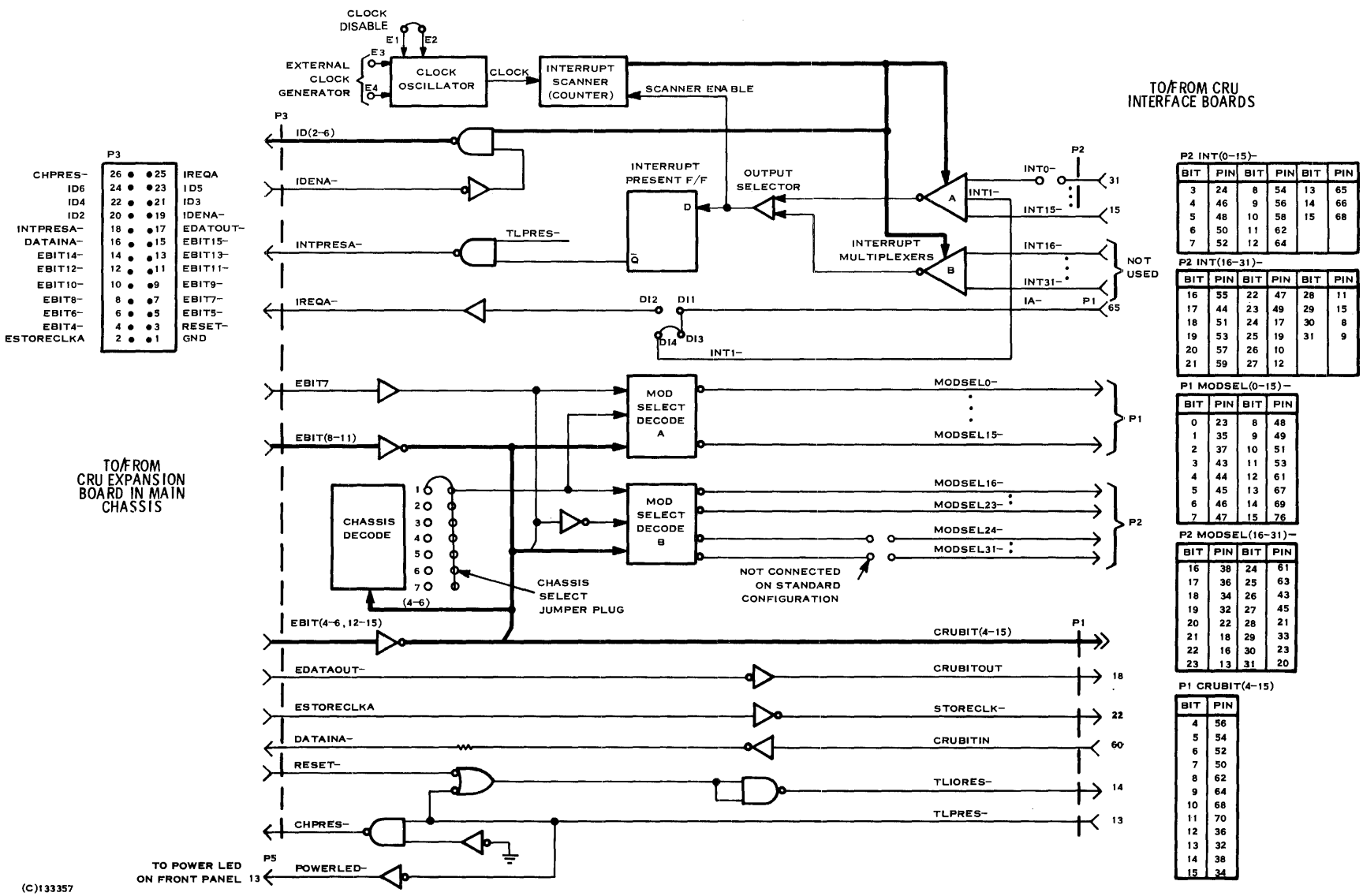
The scanner oscillator, which is disabled when jumper E1 is connected to E2, develops a 250-nanosecond pulse train used to advance the 5-stage scan counter. The four least significant counter outputs (U11, pins 14, 13, 12 and 11) are used to address the two interrupt multiplexer stages U1 and U2. The most significant counter output bit (and its complement) is used to control the multiplexer selector stage U17. The output of the selector is also routed back to the counter inputs which permit the counter to be inhibited when an interrupt is detected by either of the multiplexers.

The output of the multiplexer selector stage U17 (INTPRES–) is clocked into the interrupt present flip-flop stage U22 and routed to the CRU expansion board in the main chassis.

When the ID enable is received from the expansion board, the outputs from all five stages of the scan counter are sent to the CRU expansion board for use by software in constructing the interrupt vector which identifies which chassis and which board slot issued the interrupt.

The interrupt logic on the CRU buffer board also includes an option to bypass the scanner for interrupt 1 (IA–). In this case, the interrupt is wired to the interrupt request gate U15 and used to generate a low-active IREQA– signal. This signal is wire-ORed on the CRU expansion board with the IREQ– signals from all seven CRU buffer boards. The direct interrupt option is used when a peripheral requiring more rapid interrupt processing time is implemented in an expansion chassis.

The interrupt scanner section also contains provisions for disabling the internal interrupt scanner clock and using an external pulse generator to advance the counter. Provisions are also included for clearing the counter manually. The jumper connections associated with the maintenance options are described in Section 2 of this manual.



P2 INT(0-15)-

BIT	PIN	BIT	PIN	BIT	PIN
3	24	8	54	13	65
4	46	9	56	14	66
5	48	10	58	15	68
6	50	11	62		
7	52	12	64		

P2 INT(16-31)-

BIT	PIN	BIT	PIN	BIT	PIN
16	55	22	47	28	11
17	44	23	49	29	15
18	51	24	17	30	8
19	53	25	19	31	9
20	57	26	10		
21	59	27	12		

P1 MODSEL(0-15)-

BIT	PIN	BIT	PIN
0	23	8	48
1	35	9	49
2	37	10	51
3	43	11	53
4	44	12	61
5	45	13	67
6	46	14	69
7	47	15	76

P2 MODSEL(16-31)-

BIT	PIN	BIT	PIN
16	38	24	61
17	36	25	63
18	34	26	43
19	32	27	45
20	22	28	21
21	18	29	33
22	16	30	23
23	13	31	20

P1 CRUBIT(4-15)

BIT	PIN
4	56
5	54
6	52
7	50
8	62
9	64
10	68
11	70
12	36
13	32
14	38
15	34

Figure 3-87. CRU Buffer Board Block Diagram

Module Select Decoding. The module select decode function performed by the CRU buffer board is similar to the function provided in the main chassis by the AU2 board. To set up the chassis address to correspond to the CRU expansion board connector (which may be connected to any connector from P3 to P9), a single jumper wire is installed on the 14-pin socket P4. Then if the incoming CRU address lines (EBIT4-11) indicate an address within the chassis address space, one of the 24 module select lines (MODSEL(0-23)–) goes low. This signal is routed to the appropriate CRU board slot via the chassis backpanel board.

The CRU buffer board has provisions for decoding up to 32 module selects but the option is not wired up on the conventional system.

CRU Buffer Options. The following jumper options are available on the CRU buffer board:

- Option to wire interrupt level 1 either directly to the CRU expansion board in the main chassis or through the interrupt scanner. If J1, pins 1 and 2 are connected, the interrupt is sent directly; if J1, pins 3 and 4 are connected, the interrupt uses the scanner circuitry (normal configuration).

- Module select decodes 24 through 31 — To enable module select decodes 24 through 31; install jumpers on the CRU buffer board between M24 and P2-61, M25 and P2-63, M26 and P2-43, M27 and P2-45, M28 and P2-21, M29 and P2-33, M30 and P2-23, and M31 and P2-20 (see figure 2-21).

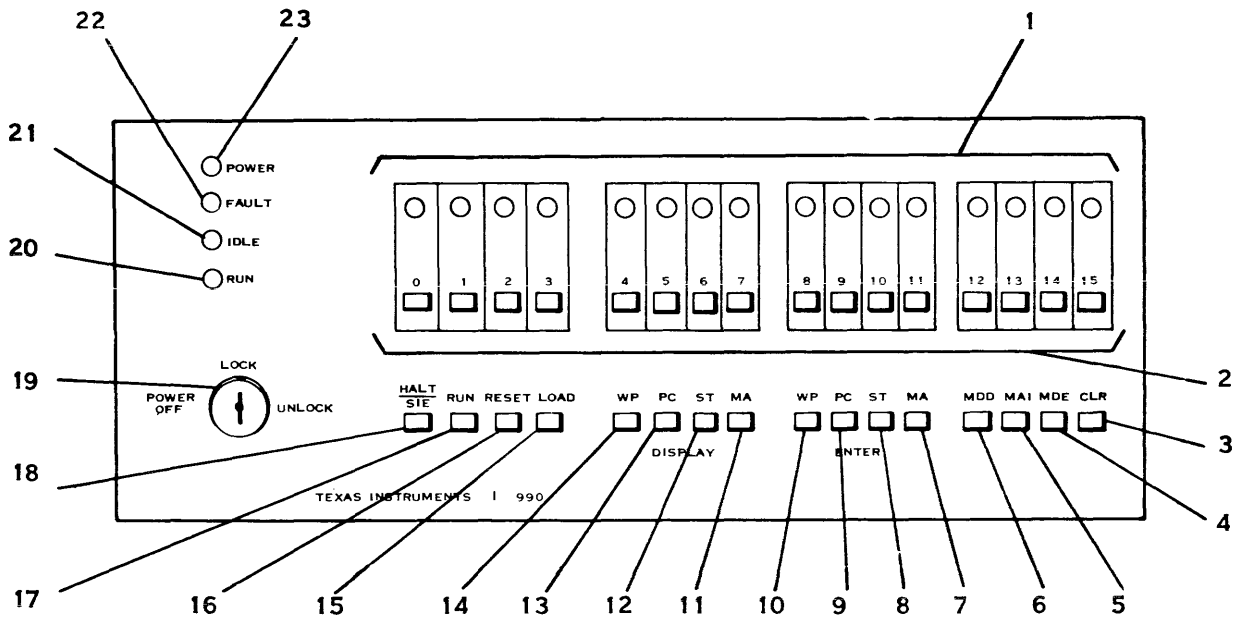
- Chassis select – A single jumper is installed on the 14 pin socket P4 as follows:

Expander Connector	Jumper Pins on P4	Chassis Number
P3	1, 14	1
P4	2, 13	2
P5	3, 12	3
P6	4, 11	4
P7	5, 10	5
P8	6, 9	6
P9	7, 8	7

3.7 PROGRAMMER PANEL

The 990 programmer panel operates as a CRU device with the Model 990/10 Computer. The programmer panel contains logic, switches and indicators that provide for manual control and operator observation of the operation of the computer. The switches are used for data entry and, along with light emitting diodes (LEDs), provide for display of data at the panel. Logic for the programmer panel is contained on a printed circuit board installed just to the rear of the panel. Interface signals between the programmer panel and the AU2 board are routed through a 20-conductor cable that leads from the programmer panel to a connector plug P3 at the top edge of the AU2 circuit board. The panel can be installed on the front of either the 6-slot or 13-slot chassis. A 127-millimetre (5-inch) filler panel adapts the programmer panel for use with the 13-slot chassis.

3.7.1 PROGRAMMER PANEL CONTROLS AND INDICATORS. The programmer panel controls indicators are shown in figure 3-88, which is keyed to table 3-26.



(A)133607

Figure 3-88. 990 Programmer Panel Controls and Indicators

3.7.2 PROGRAMMER PANEL MODES OF OPERATION. The programmer panel may function in any one of two modes including:

- Run Mode
- Halt Mode

Run Mode. In the Run mode of operation (RUN LED lit), all programmer controls are inoperative except for the HALT/SIE switch which may be enabled by setting the key switch to the UNLOCK position. If the key switch is in the LOCK position, all panel controls are disabled.

Halt Mode. If the key is inserted into the key switch and rotated to the UNLOCK position, the HALT/SIE switch is enabled. At this time, a Restart signal can be issued to the 990/10 AU1 board if the HALT/SIE switch is pressed. The Restart signal causes the minicomputer to trap to location $FFFC_{16}$ in ROM and begin executing the panel software. As a result, the minicomputer is taken out of the Run mode and the RUN LED on the programmer panel is extinguished. At this time, the scan counter on the programmer panel logic board is advanced under software control and the programmer panel switch outputs are monitored by software (see figure 3-89). Notice that the software being executed determines the function of each switch. The following discussions are based on the standard front panel (ROM) software.

If an indication is received that one of the panel switches has been pressed, the software utility activates a 10-millisecond debounce timer on the programmer panel board via an SBO or SBZ instruction addressed to bit 8 (CRUBIT12-15 encoded with 8_{16}). The resulting START TIMER– signal activates a debounce timer. Since the output of the timer is also routed to the CRUBITIN line via the multiplexer, software can determine when 10 milliseconds have elapsed. At this time, the software monitors the column containing the pressed key to ensure that the key is still

Table 3-26. Programmer Panel Controls and Indicators

Reference Number	Control or Indicator	Function
1	DATA LEDs	In the RUN mode of operation, all DATA LEDs light except when the computer halts. At this point, the contents of the CPU's program counter is displayed. A lit LED denotes a logic 1, an extinguished indicator denotes logic 0. The LSB is displayed on the far right of the LEDs. In the HALT mode, the LEDs display a computer register contents, memory contents or a value entered into computer memory via the data entry switches depending on which switches are pressed (see reference 5, 7, 9, 11, 13, 15).
2	DATA entry switches	Used in conjunction with the ENTRY switches on the panel to enter data and addresses into selected computer registers and memory locations (active only when the panel is in the HALT mode of operation). In the HALT mode, the data LED located immediately above each data entry switch lights as each switch is pressed. The value indicated by the DATA LEDs is then stored in the register or memory address selected by the entry switches.
3	CLR switch	When pressed, this switch clears the DATA LED displays.
4	MDE switch	This switch is pressed to transfer a value displayed on the DATA LEDs to the memory location defined by the contents of the memory address (MA) register in the computer.
5	MAI switch	The memory address increment (MAI) switch is pressed to increment the value stored in the CPU's memory address register by a value of 2.
6	MDD switch	When pressed, this switch causes the contents of the memory location defined by the contents of the memory address register to be displayed on the DATA DISPLAY LEDs.
7	ENTER MA switch	When pressed, this switch causes the value displayed by the DATA LEDs to be entered into the computer's memory address register.
8	ENTER ST switch	When pressed, the value displayed on the DATA LEDs is entered into the computer's status register.
9	ENTER PC	When pressed, the value displayed on the DATA LEDs is loaded into the computer's program counter.
10	ENTER WP	When pressed, the value displayed on the DATA LEDs is loaded into the computer's workspace pointer register.
11	DISPLAY MA	When pressed, the value stored in the computer's memory address register is displayed on the DATA LEDs.
12	DISPLAY ST	When pressed, the contents of the computer's status register is displayed on the DATA LEDs.
13	DISPLAY PC	When pressed, the contents of the computer's program counter is displayed on the DATA LEDs.
14	DISPLAY WP	When pressed, the contents of the computer's workspace pointer register is displayed on the DATA LEDs.

Table 3-26. Programmer Panel Controls and Indicators (Continued)

Reference Number	Control or Indicator	Function
15	LOAD switch	When the panel is in the HALT mode, pressing this switch causes the computer to branch to the ROM loader starting address.
16	RESET switch	Pressing the RST switch results in an IORESET– pulse being generated which resets all units in the system.
17	RUN switch	When the computer is halted (programmer panel is active), pressing the RUN switch returns the computer to the RUN mode of operation and deactivates the panel.
18	HALT/SIE switch	When the computer is in the RUN mode (RUN LED is lit), pressing the HALT/SIE switch causes the computer to halt and begin processing the front panel software if the key switch is set to the UNLOCK position. Pressing the switch when the computer is not in the RUN mode causes the computer to execute a single instruction at the present PC (program counter) address. The contents of the program counter are incremented by two and displayed on the DATA LEDs.
19	Key switch	The key switch (OFF/LOCK/UNLOCK) switch prevents unauthorized computer turnon or program intervention. In order to apply ac power to the chassis, the key must be inserted into the switch and the switch set to the LOCK position. At this point, power is applied to the computer, but the programmer panel is locked out. In the UNLOCK position, the computer may be halted by pressing the HALT/SIE switch. The key may be removed from the switch in either the OFF or LOCK position.
20	RUN LED	The RUN LED lights when a low-active RUN– signal is generated by the computer indicating the computer is in the RUN mode. When this LED is lit, all switches on the panel except the HALT/SIE switch are disabled and the DATA LEDs are driven under program control. When the RUN LED is extinguished, the panel controls are active.
21	IDLE LED	Lights when the computer is executing an idle instruction (indication of computer inactivity for most interrupt driven software).
22	FAULT LED	The FAULT LED lights when the computer has detected a diagnostic test failure. The LED is extinguished by executing a RSET instruction or an SBO or SBZ addressed to panel bit 11.
23	POWER LED	Lights when power is applied to the unit (key switch on the panel set to the LOCK or UNLOCK position).

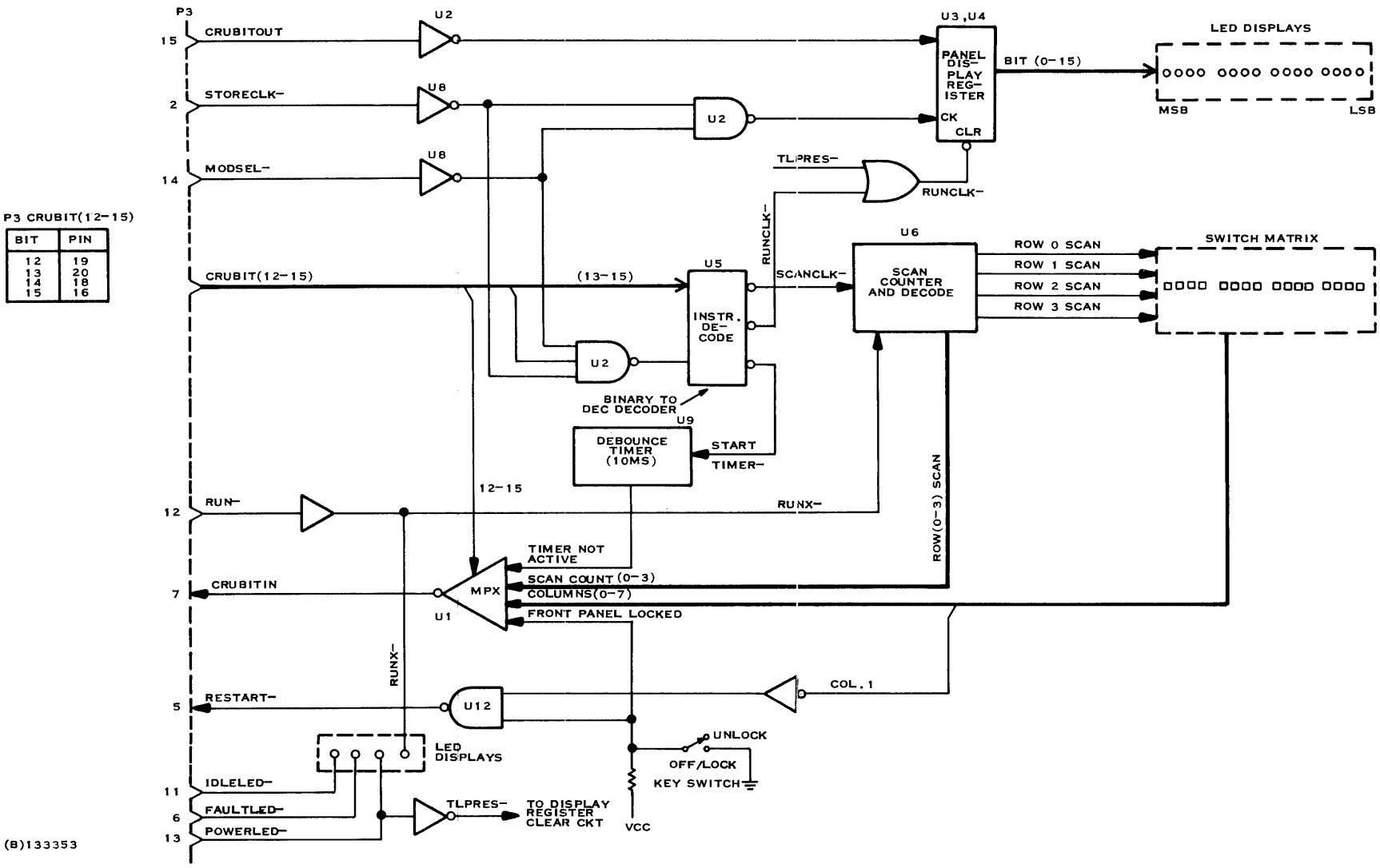


Figure 3-89. Programmer Panel Functional Block Diagram

pressed (see figure 3-90). If so, the software determines whether the key is a data key or function key. If it is a function key, panel software branches to the appropriate instruction in the program which executes the specified function. If it is a data key, the data bit is complemented (if previously a 1, changed to a zero and vice versa). The complemented bit is also stored in the data display register on the programmer panel board and applied to the corresponding DATA LED. A logic 1 is indicated by a lighted LED, and a logic 0 is indicated by an extinguished LED.

3.7.3 INTERFACE SIGNALS. Figure 3-91 shows the interface connections between the programmer panel and the programmer panel interface of the computer. The function of each interface line is described in table 3-27.

3.7.4 PROGRAMMER PANEL ADDRESSING. The programmer panel as a CRU interface device has 16 directly addressable input bits and 16 directly addressable output bits. Input and output operations can address each of the bits individually or in fields of from 1 to 16 bits. The computer instructions that drive the CRU interface can set, reset or test any bit and can move data between memory and the programmer panel.

3.7.4.1 Address Format. The 12-bit CRU address format with field assignments used by the computer is as shown in figure 3-35. The module select bits are decoded internally by the computer to generate a Module Select (MODSEL—) signal to address the programmer panel. The bit select field (CRUBIT 12-15) is the only portion of the CRU address that the programmer panel uses. When enabled by the hard-wired MODSEL— line, the programmer panel must decode the bit select field to determine which of its bits is affected by the operation.

3.7.4.2 Bit Address Development. The computer develops a CRU bit address from the CRU base address contained in workspace register 12 added to the signed displacement contained in bits 8 through 15 of the three single-bit CRU instructions: Test Bit (TB), Set Bit to One (SBO) and Set Bit to Zero (SBZ). The CRU base address loaded into workspace register 12 for the programmer panel is hexadecimal 1FE0. Individual CRU input bit address assignments for the programmer panel are as shown in table 3-28. The CRU output bit address assignments are provided in table 3-29.

3.7.5 THEORY OF OPERATION. The programmer panel operates in either the RUN mode or the HALT mode. The description that follows discusses each mode of operation separately and is based on the block diagram for the programmer panel as shown in figure 3-89.

3.7.5.1 RUN Mode. As the computer powers up in preparation to carry out its task of normal processing, the POWER LED— interface signal between the computer circuit board and the programmer panel goes low and is applied to a complementary output element on the panel. The low output from the element lights the POWER lamp on the panel, and the complementary output from the element, TLPRES—, goes high to remove the CLEAR signal from the data display register thus enabling the data display register for data entry. TLPRES has been low during computer power-down condition to hold the 16 data display lamps on the panel to logic ONE's (illuminated). The level 0 power-up interrupt is taken by the computer and the computer comes up in its RUN mode of operation. An SBO instruction addresses CRU output bit 10 of the panel causing the RUN— interface signal from the computer circuit to go low. Additionally, the strobe decoder is addressed and a low RUNCLK— is generated by the strobe decoder during one STORECLK period. The low RUNCLK— clears the data display register and the 16 data display lamps light. The low RUN— interface signal lights the RUN lamp on the programmer panel and also is applied to the two flip-flops of the scan counter to hold the scan counter to a 10_2 scan count. This scan count holds one side of

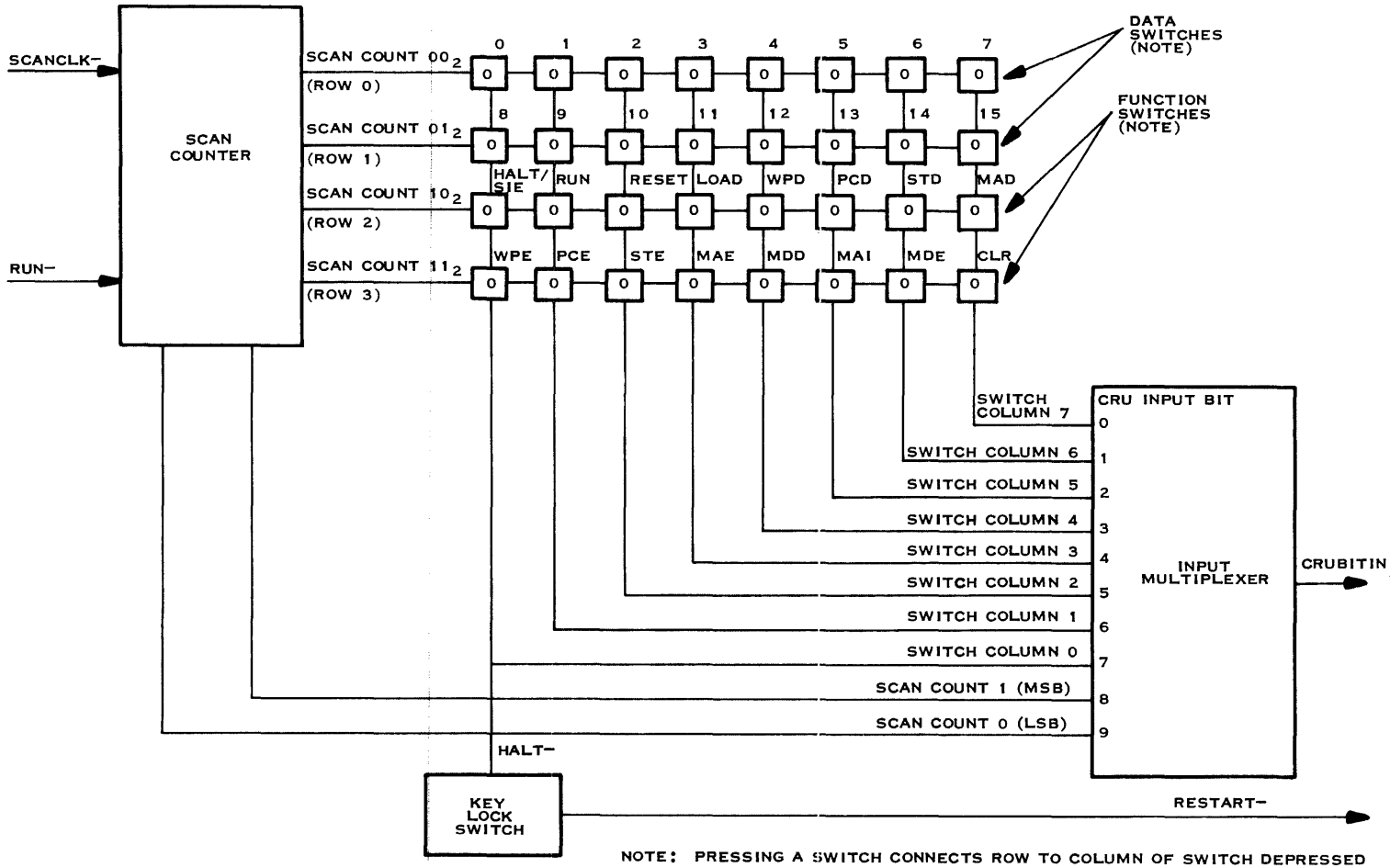


Figure 3-90. Switch Scanner Block Diagram

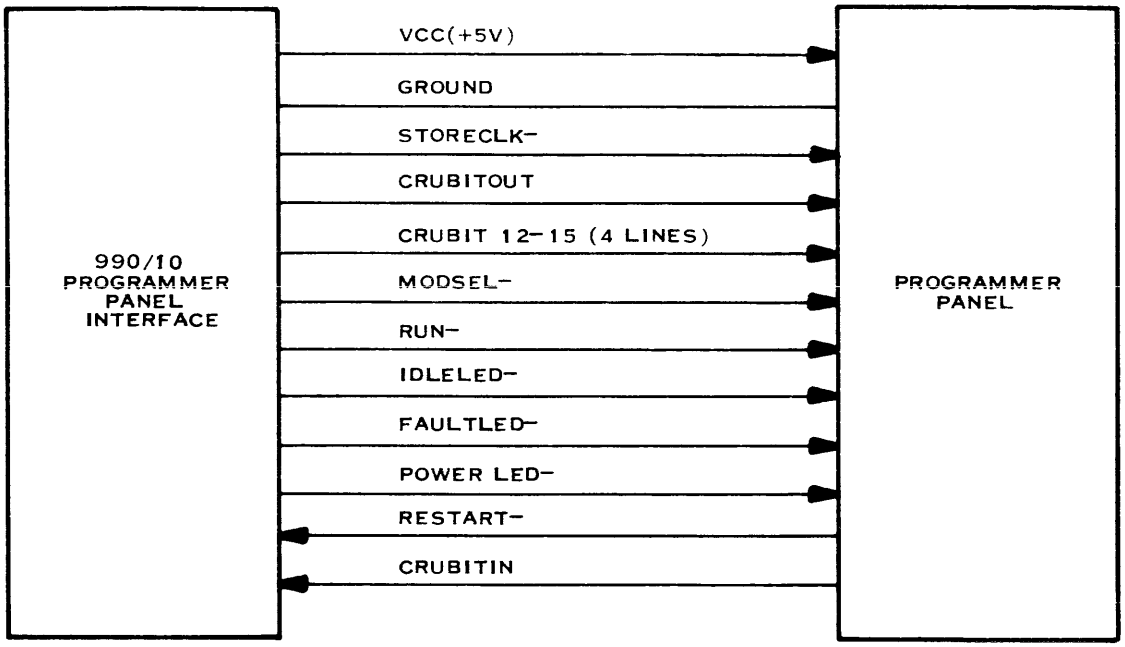


Figure 3-91. Programmer Panel Interface Diagram

the row 2 switches (left-side function switches as viewed from front panel and refer to figure 3-90) low. All switches on the panel with the exception of the HALT/SIE switch are inhibited and the panel is inactive while in the RUN mode. However, the data display register and data display lamps may be used by the computer to display program data by issuing LDCR instructions. Pressing the HALT/SIE switch while the computer is in the RUN mode causes the computer to stop processing and to execute programmer panel software. When activated, the HALT/SIE switch transfers the low at the row 2 scan side of the switch through the key lock switch (in UNLOCK position) as a low RESTART— interface signal to the computer circuit board to cause the RUN— interface signal to the panel to go high. The RUN lamp is extinguished and the hold on the scan counter is relinquished so that it may respond to the SCANCLK— signal generated by the strobe decoder while the panel is in the HALT mode. The RESTART— interface signal also causes a trap through $FCCC_{16}$ and the computer begins to execute programmer panel software making the panel switches and lights active in the HALT mode of operation.

3.7.5.2 HALT Mode. As previously described, when the HALT/SIE switch is pressed while the panel is in the RUN mode the low RESTART— interface signal to the computer circuit board causes the RUN— interface signal to go high to extinguish the RUN lamp on the panel and release the hold on the scan counter. The computer performs the RESTART— trap and the two-word vector at memory address $FFFC_{16}$ is loaded in to the workspace pointer register (first vector word) and program counter register (second vector word) to define the workspace and program starting point and the software for the programmer panel initializes and begins to execute. A test is made to see if the user has initiated an SIE instruction. If yes, the SIE register is cleared, the programmer panel is enabled and a branch is made to the user's program. If no SIE instruction has been initiated, a test is made of the Front Panel Present bit, CRU input bit 11. If the test shows the programmer panel is not present, the program jumps to a loader function. If the panel is present, the program displays the contents of the program counter at the panel data display lamps and the program moves to a main scan loop to determine if any panel switch is depressed.

Table 3-27. Programmer Panel Interface Connections

INTERFACE LINE	FUNCTION
Vcc (+5 volts)	Power for programmer panel furnished by computer power supply.
Ground	System ground.
STORECLK-	A low clock pulse that indicates to the programmer panel that the operation is a write operation. The pulse transfers the data on the CRUBITOUT line into the 16-bit parallel-out serial shift data display register of the programmer panel.
CRUBITOUT	Serial data line for transfer of data from the CPU to the addressed CRU bit(s) of the programmer panel. This line is active only when STORECLK- goes low.
CRUBIT 12 through 15	During a read operation, CRUBIT 12 through 15 applied to the input multiplexer of the programmer panel select a particular bit for input to the CPU. During a write operation, CRUBIT 12 through 15 applied to the strobe decoder of the programmer panel generate the SCANCLK-, RUNCLK-, and START TIMER strobes.
MODSEL-	Module select signal. When MODSEL- is low, the programmer panel has been selected by the computer as the addressed module.
RUN-	A low active signal generated by the computer when in the RUN mode. The low signal through a series resistor illuminates the RUN LED on the programmer panel. The low is also applied to the scan counter that in turn holds one side of the HALT/SIE switch low. Pressing the HALT/SIE switch transfers the low through the POWER OFF, UNLOCK, LOCK key switch (when in the UNLOCK position) to generate a low RESTART- signal to the computer.
IDLELED-	A low signal generated by the computer when in the IDLE mode. The low signal, through a series resistor, illuminates the IDLE LED on the panel.
FAULTLED-	A low signal generated by the computer that through a series resistor, illuminates the FAULT LED on the panel to indicate the result of a CPU test.
POWERLED-	A low signal generated by the computer that, through a series resistor, illuminates the POWER LED on the panel to indicate that the system power supply is on.
RESTART-	A low signal generated by pressing the panel HALT/SIE switch when the key switch is in the UNLOCK position. The low causes the CPU to stop processing and to start executing panel software.
CRUBITIN	Serial data line for transfer of data from the addressed CRU bit(s) at the input multiplexer of the programmer panel to the CPU.

Table 3-28. Programmer Panel CRU Input Bit Assignments

BIT	DESCRIPTION	FUNCTION
0	Switch column 7	CRU input bits 0 through 7 are assigned to switch columns 7 through 0 respectively. An 8-bit Store Communications Register (STCR) instruction from the computer stores the value of a row of eight switches as defined by the scan counter. A switch that has been depressed and has stopped bouncing is stored into memory as a logic ONE.
1	Switch column 6	
2	Switch column 5	
3	Switch column 4	
4	Switch column 3	
5	Switch column 2	
6	Switch column 1	
7	Switch column 0	
8	Scan Count 1	A logic ONE on CRU input bit 8 indicates that the scan counter is in the function (row 2 or row 3) group of switches.
9	Scan Count 0	A logic ONE on CRU input bit 9 indicates that the scan counter is in the least significant byte (row 1 or row 3) of either the data or the function group of switches.
10	Timer Active	A logic ONE on CRU input bit 10 indicates that the debounce timer has finished timing out.
11	Front Panel Not Present Or Locked	A logic ONE on CRU input bit 11 indicates that the panel is not connected to the computer or that the programmer panel key switch is in the LOCK position.
12 and 13	Not Used	
14	Maintenance Unit Not Present	A logic ZERO on CRU input bit 14 indicates that the 990 maintenance unit is connected to the computer rather than the standard programmer panel.
15	Not Used	

function. If the panel is present, the program displays the contents of the program counter at the panel data display lamps and the program moves to a main scan loop to determine if any panel switch is depressed.

As shown in the block diagram for the switch scanner, figure 3-90, the 32 data and function switches are part of a 4-row by 8-column matrix. As previously described, when the programmer panel is in the RUN mode the low RUN- signal input to the scan counter holds the scan count output of the scan counter at 10_2 and row 2 is held low. The HALT/SIE switch in row 2 is active and when pressed generates the low RESTART- signal through the unlocked key lock switch. In the HALT mode, the scan counter is incremented by the SCANCLK- signal through its binary count, 00_2 through 11_2, and rows 0 through 3 are brought low in turn. Pressing a switch transfers the low output of the scan counter to the input of the input multiplexer at the CRU input bit position that corresponds to the switch column of that switch. Though the switch column position can be determined simply by detecting CRU input bit position, the row position of the pressed switch also needs to be ascertained. To check the condition of the switches, the computer issues a byte-length STCR instruction to the programmer panel. Data switches in row 0 and function switches in row 2 are treated by soft-

Table 3-29. Programmer Panel CRU Output Bit Assignments

BIT	DESCRIPTION	FUNCTION
0 through 7	Data Display Lamps 0 through 15	A 16-bit word is transferred to the lamps for display by executing two 8-bit Load Communication Register (LDCR) instructions on the word to be displayed in a most significant byte, least significant byte order.
8	Increment scan	A Set Bit to ONE (SBO) or SBZ instruction addressed to CRU output bit 8 increments the scan counter. For example, if the scan counter is at count 11_2 then it will increment to count 00_2 after execution of the SBO. The scan counter is set to 10_2 when the RUN bit is set.
9	Not Used	CRU output bit 9 not used in the programmer panel.
10	Run	An SBO instruction addressed to CRU output bit 10 illuminates the RUN LED, sets the DATA LEDs to logic ONEs, sets the scan counter to 10_2, and enables the interrupt. The foregoing actions are effected by programmer panel ROM software when the RUN switch is pressed while in the HALT mode. Following a power-up, the RUN bit is set to a logic ONE.
11	Fault	The FAULT output bit is connected to an LED on both the programmer panel and the computer. A logic ONE to output bit 11 illuminates both LEDs. A zero clears both LEDs.
12	Clear internal interrupts	An SBO or SBZ instruction addressed to CRU output bit 12 clears the error interrupt flag in the computer. This action is performed by the CPU and is not a function of the programmer panel.
13	Start Timer	An SBO or SBZ instruction addressed to CRU output bit 13 starts the debounce timer. CRU input bit 10 monitors the timer output.
14	Single Instruction Execute (SIE)	An SBO or SBZ instruction addressed to CRU output bit 14 enables the computer to execute two more instructions before trapping to the programmer panel ROM. By addressing this bit and following with an RTWP, panel software can perform the SIE function. This action is performed by the CPU and is not a function of the panel.
15	Not Used	CRU output bit 15 not used in the programmer panel.

ware as the least significant byte of a two-byte word and the data switches in row 1 and the function switches in row 3 are handled as the most significant byte of the 16-bit word. By checking the scan count inputs to the input multiplexer at CRU input bit positions 8 and 9 a determination is made as to which row a pressed key is located. First, CRU input bit 9 (SCAN COUNT 0-) is tested to determine whether the least significant byte (rows 0 and 2) or the most significant byte (rows 1 and 3) is the location of the pressed key. If the location is determined to be in the most significant byte position the software executes SWPB instruction to reposition the CRU input bits as stored in computer memory so that they will be representative of either row 1 or row 3. A test is then made of CRU input bit 8 (SCAN COUNT 1-) to determine whether the pressed key is data switch (rows 0 and 1) or a function switch (rows 2 and 3).

In the main scan loop, the programmer panel is exercised as follows. CRU output bit 13 is addressed to start the debounce timer. After approximately 3 milliseconds delay and with the debounce timer no longer active, a read instruction is issued to see if a switch is depressed in that row of switches held low by the scan counter. If no switch is depressed this action is repeated two more times and then CRU output bit 8 is addressed to increment the scan counter to check the next row of switches three times. This scanning continues until a depressed key is detected. When a depressed key is detected, two more delayed passes are made using the debounce timer to ensure that the key is really depressed and is not noise. When the decision is made that the key is depressed, the test of CRU input bit 9 is made to see if the switch is represented by the least significant byte or the most significant byte of the word. If it is the most significant byte then the swap byte position instruction is issued. A test is then made of CRU input bit 8 to see if the switch is a data switch or a function switch. If it is a data switch, an exclusive OR instruction is issued which has the effect of changing the data in the data display register and the data display lamp that corresponds to the data switch depressed. If a function switch is depressed, an index table is set up in a workspace register to cause a jump to the instruction in the program that corresponds to the function required of the switch. The programmer panel stays in the HALT mode until the RUN function switch is depressed.

3.8 20-AMPERE POWER SYSTEM

The 20-ampere power system is used to furnish dc power for the 6-slot chassis and for a low-power consumption configuration of the 13-slot chassis. The 20-ampere power system is part of the chassis assembly, unit 1, and consists of input line filter 1FL1, ac power converter 1A2, filter capacitor 1C1, and 20-ampere power supply 1A3. An optional transformer 1T1 is required when the ac input voltage is not 115 volts ac. Also available as an optional addition to the 20-ampere power system is the standby power supply kit. The standby power supply, 1A6, provides power for protection of volatile memory during primary line failure and consists of batteries and a power supply/battery charger. The standby power supply, when implemented, provides memory power during normal ac operation as well as during a primary line power failure and maintains a charge on the 12-volt battery supply. When the standby power supply option is not implemented as a part of the 20-ampere power system, a jumper plug is installed across pins of jack 1A3J3 of the 20-ampere power supply and memory power is then derived from the 20-ampere power supply.

The 20-ampere power supply provides dc power to the computer backpanel as shown in table 3-30. Additionally +12MEM and +5MEM are either supplied by jumper wires from the +12MAIN and +5MAIN outputs respectively of the 20-ampere power supply or from the standby power supply when that option is implemented.

Table 3-30. 20-Ampere Power Supply DC Power Output

SUPPLY	VOLTAGE	CURRENT MAX
+5 MAIN	5 ± 3%	20A
+12 Main	12 ± 3%	2A
-12 Main	-12 ± 6%	1A
-5 Mem	-5 ± 6%	0.05A

Three control signals are generated on the 20-ampere power supply and are provided to the computer system via the backpanel. The signals are TLPRES-, TLPFWP-, 120HZ. TLPRES- remains at logic ZERO until all supply voltages are stable and then goes to logic ONE. The warning pulse, TLPFWP-, is generated when ac power failure is imminent. The 120HZ signal is the real time clock signal provided to the processor and is a series of logic level pulses synchronized with the ac line frequency. Timing for control signals are as shown in figure 3-33.

A block diagram discussion of the elements of the 20-ampere power system is provided in the following paragraphs.

3.8.1 AC POWER CONVERTER AND FILTERS. The ac power converter and filters as shown in the block diagram of figure 3-92 transform primary ac power into a 160-volt dc output and a 120-Hz output. The 160-volt dc output is applied to either a 20-ampere or 40-ampere power supply and also to the standby power supply when that option is in use. Refer to chassis wiring diagram figure 3-80 as well as to the block diagram for the ac power converter and filters as shown in figure 3-92 during the following description.

Primary power is applied through fuse 1F1 and the key lock switch on the programmer panel (or operator panel) to line filter 1FL1. The filtered ac is applied to terminals 1 and 2 of terminal board 1TB1. Note that transformer 1T1 is in the circuit only when its use is required to adapt the power system to 100-volt, 200-volt, or 230-volt ac input operation. Both chassis cooling fans are across the ac input at terminals 1 and 2 of the terminal board 1TB1 and the ac input is connected to the input of the ac power converter at pins 1 of 2 of jack 1A2J1.

The ac input to the power converter is applied to a bridge rectifier through two 5-ohm thermal resistors. The thermal resistors prevent excessive current through the rectifiers at power turn-on and are labeled soft start on the block diagram. The 160-volt dc output of the ac power converter is applied across filter capacitor 1C1 and to the input of both the 20-ampere power supply and, when implemented, the standby power supply.

The ac input to the ac power converter is applied to another bridge rectifier circuit through four 2700-ohm current-limiting resistors. The 120-Hz full-wave output of the rectifier is optically coupled to pins 3 and 4 of jack 1A2J3 where it is wired to the input of the main power supply.

3.8.2 20-AMPERE POWER SUPPLY. The 20-ampere supply (see figure 3-93) is a ringing choke, sometimes referred to as flyback, dc-to-dc converter. The primary ac input is converted to approximately 160 volts dc by the ac power converter and applied to the input of the 20-ampere power supply. To this point no electrical isolation between input and output voltages has been achieved unless optional transformer 1T1 is in use. The primary voltage reference circuit is adjusted so that when the dc input voltage to the 20-ampere power supply rises to approximately 130 volts dc, the voltage threshold comparator switches in to drive an optical coupler that permits the reset to be removed from the TLPRES- and TLPFWP- circuits. The voltage threshold comparator switches off when the input dc voltage drops to about 120 volts dc.

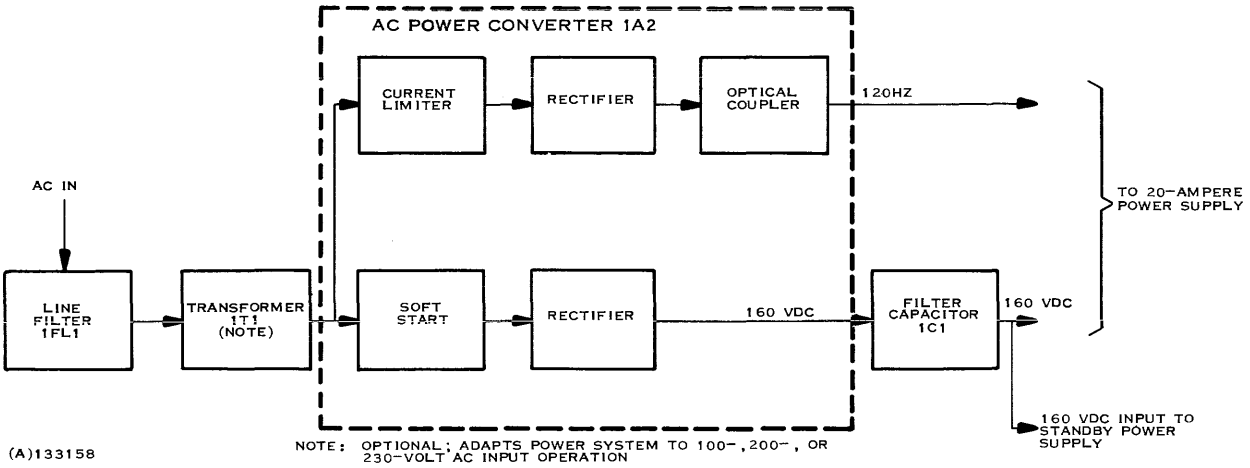


Figure 3-92. Block Diagram of AC Power Converter and Filters

The flyback control circuit causes the flyback switch to turn off and on at a frequency much higher than the 50 to 60 Hz input frequency. The flyback switch stores energy in the transformer through the primary winding. The flyback control circuit regulates the energy transfer from the input to the outputs by varying the frequency of operation of the flyback switch. This high frequency of application of the dc voltage to the isolation transformer reduces core size requirements of the transformer. Three secondary windings of the transformer develop multiple output voltages that are applied to their separate rectifier and filter circuits. The +5 MAIN output of the +5 volt rectifier is sensed and compared to a +5 volt reference level applied to the +5 volt regulator control circuit. A signal from the +5 volt regulator control circuit is optically coupled to the flyback control circuit and the flyback switch "on" time is varied to regulate to +5 volts. The other two output voltages applied to the rectifier and filter circuits for the +12 MAIN and -12 MAIN outputs are thus slaved to the +5 MAIN output. The outputs of the two rectifier and filter circuits are actually at approximately 16 volts in amplitude and each requires a 12-volt series regulator to provide +12 MAIN and -12 MAIN outputs. Another series regulator provides the -5 MEM output from either the -12 MAIN output or from the -12 MEM input from the standby power supply if implemented. The +12 MEM and +5 MEM outputs are patched from the +12 MAIN and +5 MAIN outputs respectively if a standby power supply is not used.

As shown in figure 3-93, an overvoltage condition at any of the power supply output voltages or an over current of the 5-volt output causes generation of a signal that is optically coupled to the flyback control circuit to shut down the power supply and power must be cycled to restart the power supply. This nondestructive shutdown also occurs when the average current in the primary winding is greater than approximately 2.5 amperes or when the temperature of the heatsink for the transistor in the flyback switch is approximately 105 degrees Celsius (221 degrees Fahrenheit).

Optical couplers are used to maintain isolation between input and output voltages of the power supply. Additionally the power supply receives a 120-Hz signal input from the ac power converter, shapes the signal, and provides the signal as the real time clock input to the AU2 circuit board. The TLPFWP- pulse output of the power supply is provided as a warning pulse prior to the loss of any output voltages and a TLPRES- reset signal is provided as an accurate status of all output power even during power-up, power-down, or total loss of power.

3.8.3 STANDBY POWER SUPPLY. The standby power supply is an optional power supply system consisting of a standby power supply assembly (mounted "piggy back" on the main supply), and a set of storage batteries which provide the regulated voltages used in the 990/10 memory. In the event of an ac power failure, the supply automatically switches to battery power to prevent loss of data in the dynamic memory of the computer. The standby power supply will support a maximum of 32K words of memory.

During normal ac power conditions, the standby power supply derives its input power from the +160 volt dc output from the power converter assembly in the main power supply. The standby supply then converts the unregulated dc input into the regulated ±12 and +5 volts dc voltages required by the RAM memories used in the computer. The standby supply also contains a battery charger circuit used to provide charging current for the storage batteries.

In the 13-slot chassis the standby voltages are distributed to slots 1 through 7; memory voltages for the remaining slots are powered from the main power supply. Since the standby power supply can support a maximum of 32K words of memory, memory expansion greater than 32K must be located in slots 8 through 13. Obviously, memory located in these slots 8 through 13 will not be retained during a power failure.

The standby power supply automatically switches to battery operation any time the +160-volt output from the ac power converter fails to deliver adequate power. The standby power supply generates UV- to notify the main power supply of the status of the output voltages from the standby power supply. The low voltages signal (UV-) is used by the main power supply to generate the computer power reset (TLPRES-) signal sent to the computer circuit board. When the batteries discharge to the minimum functional voltage level, the standby power supply shuts down.

When normal ac power is restored, the standby supply develops an equalizing voltage until the charge current drops to the trickle charge level. The supply then switches to a float voltage to maintain the batteries at full charge. The standby power supply also has provisions for preventing battery operation unless ac power is first applied to the system (+160 volts dc output of the ac power converter is within tolerance).

Another feature of the standby power supply is an overvoltage protection circuit which disables the standby supply and blows the battery fuse in the event that any of the memory voltages exceed predetermined values.

Functionally, the standby power supply consists of the following major circuits:

160-volt to 20-volt converter

12-volt converter

Regulator control

5-volt regulator

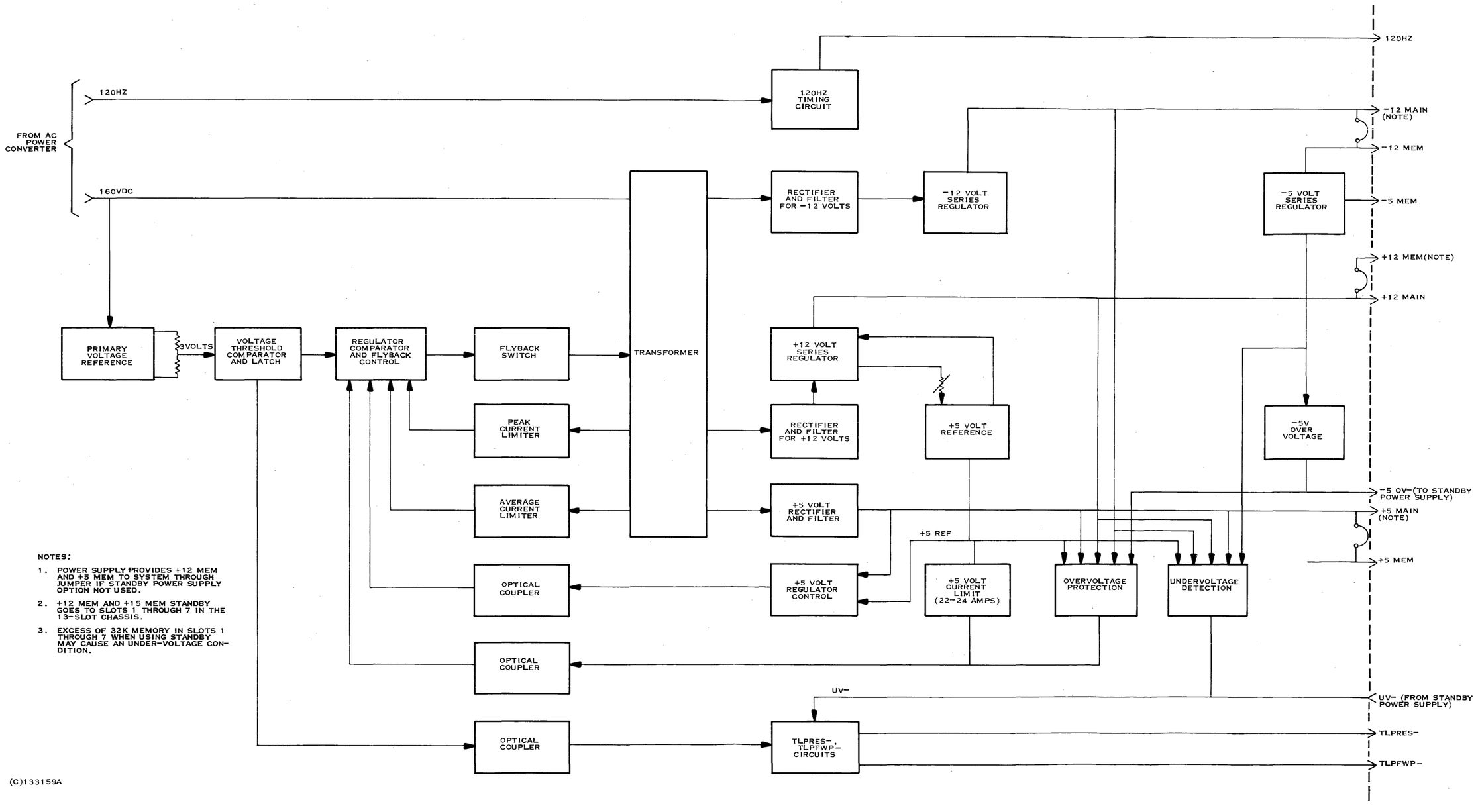
12-volt overvoltage protection circuit

5-volt overvoltage protection circuit

Battery charger circuit

Battery circuit

A simplified block diagram of the standby power supply is shown in figure 3-94. The operation of the circuits is briefly described in the following paragraphs.



NOTES:

1. POWER SUPPLY PROVIDES +12 MEM AND +5 MEM TO SYSTEM THROUGH JUMPER IF STANDBY POWER SUPPLY OPTION NOT USED.
2. +12 MEM AND +15 MEM STANDBY GOES TO SLOTS 1 THROUGH 7 IN THE 13-SLOT CHASSIS.
3. EXCESS OF 32K MEMORY IN SLOTS 1 THROUGH 7 WHEN USING STANDBY MAY CAUSE AN UNDER-VOLTAGE CONDITION.

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Figure 3-93. Block Diagram of 20-Ampere Power Supply

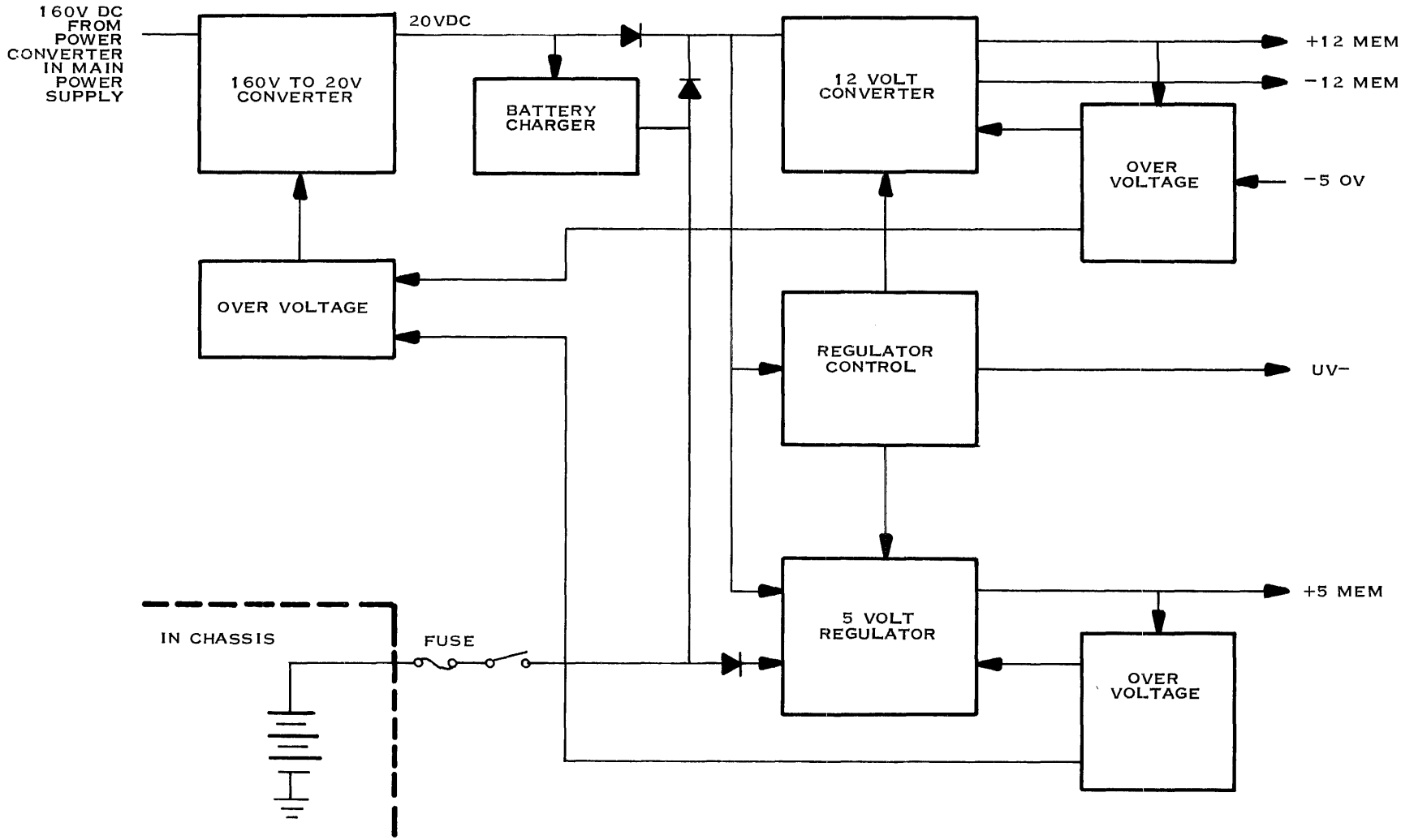

Figure 3-94. Standby Power Supply, Simplified Block Diagram

3.8.3.1 160-Volt to 20-Volt Converter. The 160-volt to 20-volt converter is a flyback type dc-dc converter similar to the converters used in the main power supply. The converter steps down the unregulated +160-volt (nominal) output of the power converter in the main supply to an unregulated +20 volts dc used by the battery charger and by the 12-volt and 5-volt regulators during normal operation. The converter is automatically shut down if an overvoltage condition is detected on any of the memory supply voltage lines (±12 or 5 volts dc).

3.8.3.2 12-Volt Converter. The 12-volt converter is also of the flyback converter type that operates from the unregulated +20 volts dc output of either the 160-volt to 20-volt converter (normal operation) or from the standby batteries (power fail condition). The 12-volt converter also contains provisions for shutting down in the event of an over-voltage condition at the converter output.

3.8.3.3 5-Volt Regulator. The 5-volt regulator is a series regulator used to develop the reference +5 volts dc memory voltage. The overvoltage associated with the 5-volt regulator shuts down the 160-volt to 20-volt converter and causes the battery fuse to open in the event that the output of the +5-volt regulator rises above a predetermined value.

3.8.3.4 Battery Charger Circuit. The battery charger circuit is a series regulator that develops either a float voltage (batteries at full charge) or an equalizing voltage (batteries discharged).

3.8.3.5 Regulator Control. The regulator control circuit monitors the memory supply voltage lines (+12 volts and +5 volts) and generates a logic low UV- until the supplies are up. The regulator control circuit also disables the 12-volt converter and the 5-volt regulator if the battery switch is turned on before the ac switch is turned on. After the system is initialized, the regulators will function properly from battery power if ac power is lost.

3.9 40-AMPERE POWER SYSTEM

The 40-ampere power system is used to furnish dc power for the 13-slot chassis configuration. The 40-ampere power system is a part of the chassis assembly and consists of input line filter 1FL1, ac power converter 1A2, filter capacitor 1C1 and 40-ampere power supply 1A3. An optional transformer 1T1 which is supplied in the voltage kit (TI part number 945133) is required when the ac input voltage is not 115 volts ac. Also available as an optional addition to the 40-ampere power system are two sizes of standby power supply kits, a small standby power supply kit (TI part number 945128-1) or a large standby power supply kit (TI part number 940024-1). The standby power supply provides power for the protection of volatile memory during a primary line failure and consists of batteries and a power supply/battery charger. The standby power supply, when implemented, provides memory power during normal ac operation as well as during a primary line power failure and maintains a charge on the 12-volt battery supply. When the standby power supply option is not implemented as a part of the 40-ampere power system, a jumper plug is installed across the pins of jack 1A3J3 of the 40-ampere power supply and memory power is derived from the 40-ampere power supply.

The 40-ampere power supply provides dc power to the computer backpanel as shown in table 3-31. Additionally +12 MEM and +5 MEM are either supplied by jumper wires from the +12 MAIN and +5 MAIN outputs respectively of the 40-ampere power supply or from the standby power supply when the option is implemented.

Table 3-31. 40-Ampere Power Supply Dc Power Output

Supply	Voltage	Current Maximum
+ 5 MAIN	+ 5 ± 3%	40A
+12 MAIN	+12 ± 3%	4A
−12 MAIN	−12 ± 6%	2A
− 5 MEM	− 5 ± 6%	0.10A

Three control signals are generated on the 40-ampere power supply and are provided to the computer system via the backpanel. The signals are TLPRES–, TLPFWP–, and 120Hz. TLPRES– remains at logic zero until all supply voltages are stable and then goes to logic one. The warning pulse, TLPFWP–, is generated when ac power failure is imminent. The 120Hz signal is the real time clock signal provided to the signal processor and is a series of logic level pulses synchronized with the ac line frequency. Timing for control signals is as shown in figure 3-33.

A block diagram discussion of the 40-ampere power supply keyed to figure 3-95 is provided in the following paragraphs. The ac power converter used in the 40-ampere power system is the same as that used in the 20-ampere system described in paragraph 3.8.1. For convenience, the elements of the ac power converter are repeated as part of the block diagram for the 40-ampere power system.

The 40-ampere power supply contains two types of switching circuits. The +12 MAIN and −12 MAIN supplies use a flyback dc-dc converter and the +5 MAIN uses a forward converter configuration. The primary ac input is converted to approximately 160 volts dc by the ac power converter and is applied to the input of the 40-ampere power supply. To this point, no electrical isolation between the input and output voltages has been achieved unless optional transformer 1T1 is in use.
The primary voltage reference circuit is set so that when the dc input voltage to the 40-ampere power supply rises to approximately 130 volts dc, the voltage threshold comparator switches into an emitter follower that drives an optical coupler to permit the reset to be removed from TLPRES– and TLPFWP– circuits. The voltage comparator switches off when the input dc voltage drops to about 120 volts dc.

The +12 MAIN and −12 MAIN flyback converter switch and the +5 MAIN forward converter switch are driven by the same clock generator. The converters are alternately gated on and then forced to turn off, thus providing pulse width modulation to maintain voltage regulation.

The +12 MAIN and −12 MAIN flyback control circuit causes the flyback switch to turn on and off at a frequency much greater than the 50 or 60 Hz input line frequency. The flyback switch stores energy in a transformer through its primary winding. The flyback control circuit regulates the energy transfer from the input to the output by varying the "on" time pulse width of a flyback switch. This high-frequency application of the 160 volts dc to the isolation transformer reduces the core size requirements of the transformer. Two secondary windings of the transformer develop multiple output voltages that are applied to their separate rectifier and filter circuits.

The +12 MAIN output of the +12 rectifier is sensed and compared to the +5 reference level applied to the +12 regulator control circuit. A signal from the +12 voltage regulator control circuit is optically coupled to the flyback control circuit that controls the flyback switch "on" time that varies to regulate the +12 MAIN voltage.

The other output voltage applied to the rectifier and filter circuit for the −12 MAIN is approximately 16 volts in amplitude and requires a −12 volt series regulator circuit to provide the −12 MAIN output voltage. The −5 volts is developed by a −5 volt series regulator connected to the −12 MAIN or to the −12 MEM.

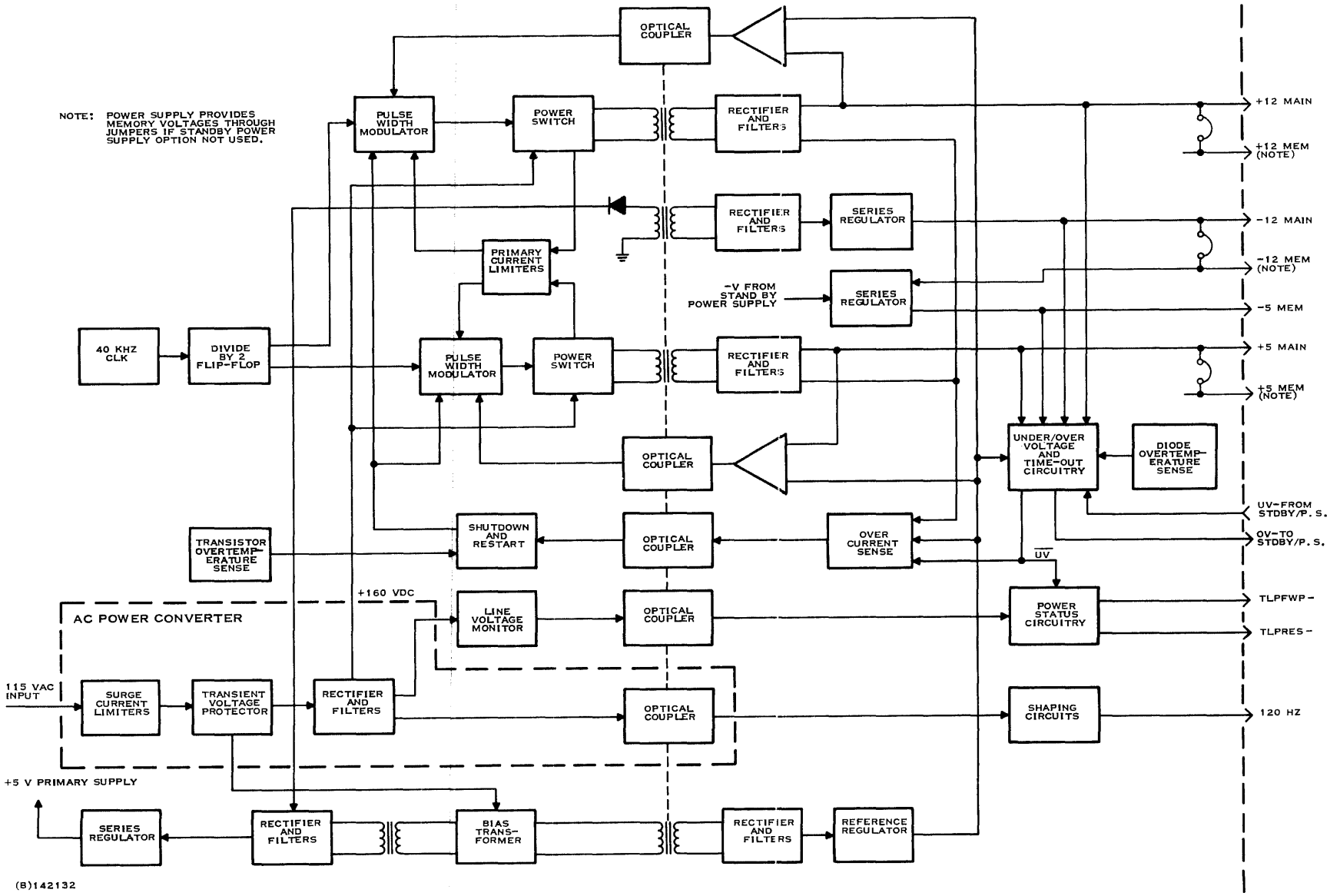

Figure 3-95. Block Diagram of 40-Ampere Power System

The +5 MAIN forward converter control circuit causes the forward switch to turn on and off at the same frequency as the +12 MAIN and -12 MAIN converter switch. This high-frequency application of the 160 volts dc through the primary transfers energy through the transformer to the secondary winding. The secondary voltage is rectified and fed to a filter consisting of an inductor-capacitor network and a commutating diode that is connected between the output of a rectifier and ground. Essentially, the secondary portion of this circuit performs like a buck-switching regulator.

The +5 MAIN voltage is sensed and compared to the +5 reference supplied to the control circuit and is optically coupled to the +5 MAIN forward switch regulator control circuit. The switch "on" time is varied to regulate the +5 volts.

As shown in figure 3-95, an overvoltage at any of the power supply voltages or an overcurrent of the +5 MAIN, +12 MAIN and −12 MAIN output voltages causes generation of a signal that is optically coupled to the flyback and forward control circuits to shut down the power supply. When an over-current occurs, a restart circuit tries several times to power up. If the over-current continues to exist during the restart cycles, the power supply will shut down. Input ac power must be momentarily removed and reapplied in order to get the power supply to reset. A separate protection on the primary switch transistors is obtained by sensing peak currents through a common emitter resistor. If the peak current in the primary windings is greater than approximately 7 amperes, the drive for the switch is terminated for that cycle. Temperature sensors on the heatsink for the switch transistors and the heatsink for the diode rectifiers for the +5 MAIN supply are provided that shut the system down if the heatsink temperatures exceed approximately 105° C (221° F). Optical couplers are used to maintain isolation between input and output voltages of the power supply.

Additionally, the power supply receives a 120 Hz signal from the ac power converter (1A2). This signal is shaped to provide the signal used as the real time clock input to the AU2 circuit board via the backpanel.

The TLPFWP- output pulse of the power supply is provided as a warning pulse prior to the loss of any output voltage.

The TLPRES- reset signal is provided as an accurate status of output power even during power-up, power-down, or total loss of power (see figure 3-33 for chassis power supply timing).

3.10 LARGE STANDBY POWER SUPPLY

The large Standby Power Supply Kit (TI part number 940024-0001) contains an optional power supply system that consists of a standby power supply assembly (to be mounted "piggyback" on the main 40-ampere power supply) and a set of storage batteries that provide the regulated voltages used in the 990 memory. In the event of ac power failure, the supply automatically switches to battery power to prevent loss of data in the dynamic memory of the computer.

During normal ac power conditions, the standby power supply derives its input power from the 160-volt dc output from the ac power converter assembly 1A2 in the main power supply. The standby power supply then converts the unregulated dc input into isolated regulated +12 MEM, +5 MEM and an unregulated −12 volts to drive the −5 MEM regulator on the MAIN supply. These voltages are required by the RAM memories used in the computer. The standby supply also contains a battery charger circuit used to provide charging current for the storage batteries.

In the 13-slot chassis, the standby voltages are distributed to slots 1 through 7; memory voltages for the remaining slots are powered from the main power supply. Memory located in slots 8 through 13 will not be retained during a power failure.

When the standby power supply is operating from ac power, it generates a low-voltage signal (UV–) to notify the main power supply of the status of the output voltages from the standby power supply. The low voltages signal is used by the main power supply to generate the computer power reset (TLPRES–) signal which is sent to the computer.

When operating under ac power, the standby battery charge circuit develops an equalizing voltage until the charge current drops to the trickle charge level. The supply then regulates at a float voltage to maintain the batteries at full charge. When the batteries discharge to the minimum functional voltage level (approximately 9.5v), the standby power supply will shut down. The standby power supply also has provisions for preventing battery operation unless power first applied to the system (+160 volts dc) is within tolerance.

Functionally, the standby power supply consists of the following major circuits:

1. 160-volt to 15-volt converter
2. Boost switching regulator and 12-v series regulator
3. 5-volt converter
4. Overvoltage control circuit
5. Undervoltage control circuit
6. Battery charger circuit
7. Battery circuit

A simplified block diagram of the standby power supply is shown in figure 3-96. The operation of the circuits is briefly described in the following paragraphs.

3.10.1 160-VOLT TO 15-VOLT CONVERTER. The 160-volt to 15-volt converter is a flyback type of dc-dc converter using a regulating pulse width modulator that operates in a slave-driven mode. The pulse width modulator drives switch transistors to switch 160 volts through a transformer. The transformer also provides isolation between the primary circuits and the secondary circuits. The transformer also steps down the unregulated 160 volts (nominal) output of the ac power converter (1A2) that is rectified and filtered to a regulated 15 volts dc output that is used as an input voltage by the +12 MEM and +5 MEM regulators and the battery charger. The ac power converter will shut down if an overvoltage condition is detected on the memory supply voltage lines (+12 or +5 MEM). Primary current limiting is achieved by sensing the current in the switch transistors. An optical coupler provides isolation from primary to secondary control circuits. The 15-volt regulator load current is sensed by a transistor and resistor. The primary and secondary load current sense voltage is connected to the pulse width modulator to provide current limiting.

3.10.2 BOOST SWITCHING REGULATOR AND +12-VOLT SERIES REGULATOR. During normal ac operation, the boost switching regulator circuit remains off as long as the +15-volt regulator output is greater than 14.5 volts dc. During this condition, the +15 volts is steered to the input of the 12-volt series regulator. If ac power is lost causing the 15-volt regulator to be off, the boost switching regulator begins to switch because the battery voltage is less than 14.5 volts dc. The boost regulator voltage is steered to the input of the 12-volt series regulator to provide the +12 MEM output.

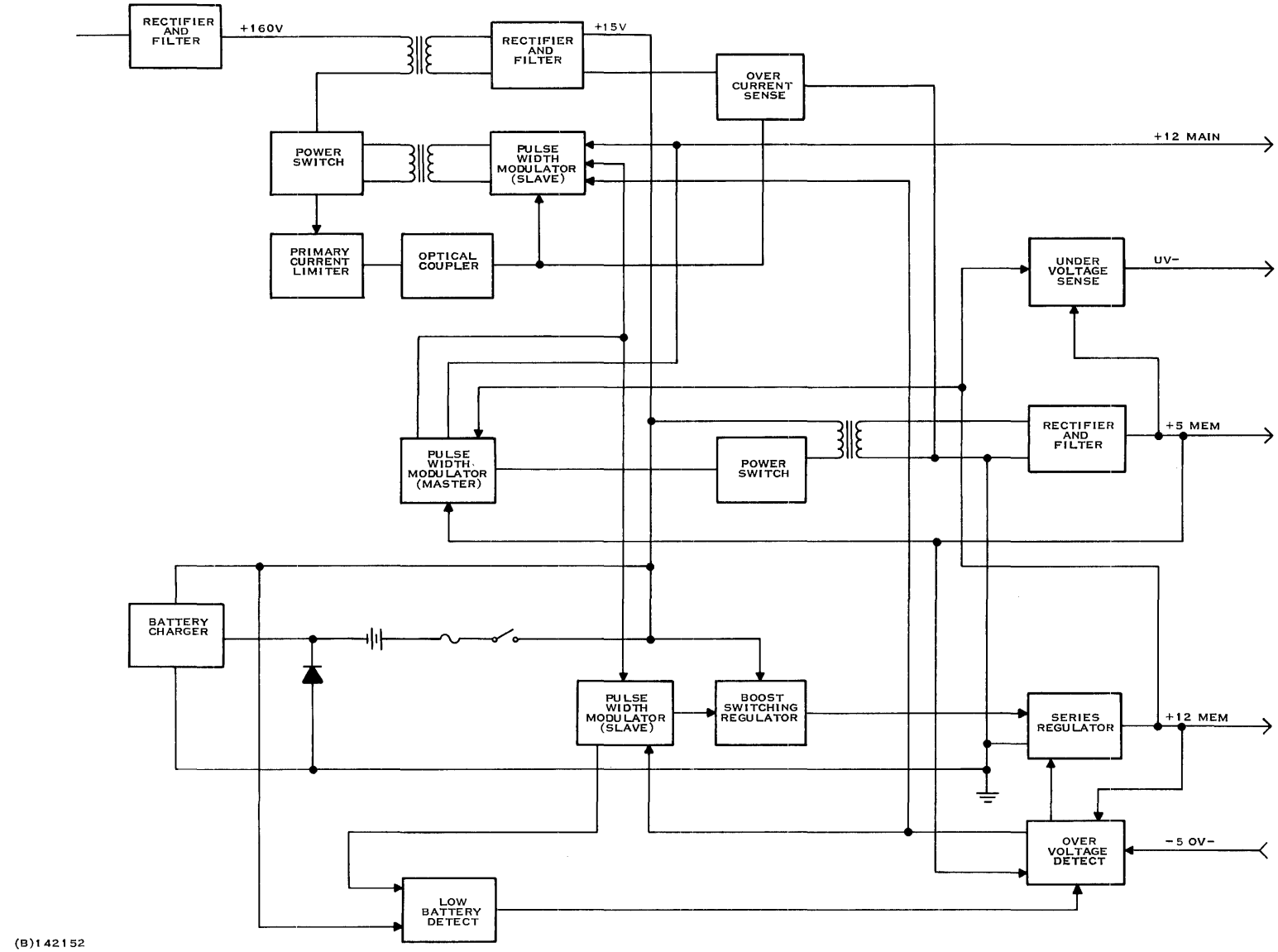

Figure 3-96. Large Standby Power Supply, Simplified Block Diagram

In standby operation and when the battery voltage begins to decrease, the boost switching regulator will regulate at 13.8 volts dc to the + 12-volt series regulator until the battery voltage decreases to 9.5 volts dc. At this voltage, the standby power supply will shut down and remain off until ac power comes up and power is recycled.

3.10.3 5-VOLT CONVERTER. The 5-volt power supply is a flyback type dc-dc converter using a regulating pulse width modulator that operates in a free-running mode. The pulse width modulator drives switch transistors to switch the + 15 volts or the battery voltage through a transformer. The transformer steps down either the + 15 volts or battery voltage for the + 5 MEM voltage. The transformer also has a second winding to provide unregulated − 12 volts. Primary current limiting for the switch transistor is sensed by a resistor and transistor as is the − 12-volt load current sensed in the secondary of the transformer. Both sensed voltages are connected to the pulse width modulator to provide current limiting. This pulse width modulator acts as a master oscillator to provide drive to the other two slave pulse width modulators for high-frequency synchronism. This converter will shut down if an overvoltage condition is detected on the memory supply voltage lines or if low battery voltage occurs.

3.10.4 OVERVOLTAGE CONTROL CIRCUIT. The overvoltage control circuit monitors the memory supply voltage lines (+ 12 and + 5 volts) and generates a low signal to shut down the power supply.

3.10.5 UNDERVOLTAGE DETECT CIRCUIT. The undervoltage detect circuit monitors the memory supply voltage lines (+ 12 and + 5 volts) to generate a low voltage signal (UV–) to the main power supply. The low-voltage signal is used by the main power supply to generate the computer power reset signal (TLPRES–) that is sent to the computer circuit boards.

3.10.6 BATTERY CHARGER CIRCUIT. The battery charger circuit is a series regulator configuration that develops either a float voltage (battery at full charge) or an equalizing voltage (battery discharged). The battery charger regulates the battery negative return line.

3.10.7 BATTERY CIRCUITS. The battery circuit consists of two 6-volt storage batteries connected in series, a fuse and a battery switch.

ALPHABETICAL INDEX

INTRODUCTION

The following index lists key words and concepts from the subject material of the manual together with the area(s) in the manual that supply major coverage of the listed concept. The numbers along the right side of the listing reference the following manual areas:

- Sections - References to Sections of the manual appear as "Section x" with the symbol x representing any numeric quantity.
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  Tx-yy

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  Fx-yy

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RD: 101080 TRH, NT, TI H/W MANUAL (EXPANDED TABLE)

WORD ADDRESS ON BOARD	SWITCH SETTING 1	2	3	4	5	6	7	8	NUMBER OF MEMORY WORDS BELOW BOARD	NUMBER OF MEMORY BYTES BELOW BOARD
>00000	0	0	0	0	0	0	0	0	0 (0) KW	0 (0) KB
>01000	0	0	0	0	0	0	0	1	4,096 (4) KW	8,192 (8) KB
>02000	0	0	0	0	0	0	1	0	8,192 (8) KW	16,384 (16) KB
>03000	0	0	0	0	0	0	1	1	12,288 (12) KW	24,576 (24) KB
>04000	0	0	0	0	0	1	0	0	16,384 (16) KW	32,768 (32) KB
>05000	0	0	0	0	0	1	0	1	20,480 (20) KW	40,960 (40) KB
>06000	0	0	0	0	0	1	1	0	24,576 (24) KW	49,152 (48) KB
>07000	0	0	0	0	0	1	1	1	28,672 (28) KW	57,344 (56) KB
>08000	0	0	0	0	1	0	0	0	32,768 (32) KW	65,536 (64) KB
>09000	0	0	0	0	1	0	0	1	36,864 (36) KW	73,728 (72) KB
>A0000	0	0	0	0	1	0	1	0	40,960 (40) KW	81,920 (80) KB
>B0000	0	0	0	0	1	0	1	1	45,056 (44) KW	90,112 (88) KB
>C0000	0	0	0	0	1	1	0	0	49,152 (48) KW	98,304 (96) KB
>D0000	0	0	0	0	1	1	0	1	53,248 (52) KW	106,496 (104) KB
>E0000	0	0	0	0	1	1	1	0	57,344 (56) KW	114,688 (112) KB
>F0000	0	0	0	0	1	1	1	1	61,440 (60) KW	122,880 (120) KB
>10000	0	0	0	1	0	0	0	0	65,536 (64) KW	131,072 (128) KB
>11000	0	0	0	1	0	0	0	1	69,632 (68) KW	139,264 (136) KB
>12000	0	0	0	1	0	0	1	0	73,728 (72) KW	147,456 (144) KB
>13000	0	0	0	1	0	0	1	1	77,824 (76) KW	155,648 (152) KB
>14000	0	0	0	1	0	1	0	0	81,920 (80) KW	163,840 (160) KB
>15000	0	0	0	1	0	1	0	1	86,016 (84) KW	172,032 (168) KB
>16000	0	0	0	1	0	1	1	0	90,112 (88) KW	180,224 (176) KB
>17000	0	0	0	1	0	1	1	1	94,208 (92) KW	188,416 (184) KB
>18000	0	0	0	1	1	0	0	0	98,304 (96) KW	196,608 (192) KB
>19000	0	0	0	1	1	0	0	1	102,400 (100) KW	204,800 (200) KB

>1A000	0	0	0	1	1	0	1	0	106,496	(104)	KW	212,992	(208) KB
>1B000	0	0	0	1	1	0	1	1	110,592	(108)	KW	221,184	(216) KB
>1C000	0	0	0	1	1	1	0	0	114,688	(112)	KW	229,376	(224) KB
>1D000	0	0	0	1	1	1	0	1	118,784	(116)	KW	237,568	(232) KB
>1E000	0	0	0	1	1	1	1	0	122,880	(120)	KW	245,760	(240) KB
>1F000	0	0	0	1	1	1	1	1	126,976	(124)	KW	253,952	(248) KB
>20000	0	0	1	0	0	0	0	0	131,072	(128)	KW	262,144	(256) KB
>21000	0	0	1	0	0	0	0	1	135,168	(132)	KW	270,336	(264) KB
>22000	0	0	1	0	0	0	1	0	139,264	(136)	KW	278,528	(272) KB
>23000	0	0	1	0	0	0	1	1	143,360	(140)	KW	286,720	(280) KB
>24000	0	0	1	0	0	1	0	0	147,456	(144)	KW	294,912	(288) KB
>25000	0	0	1	0	0	1	0	1	151,552	(148)	KW	303,104	(296) KB
>26000	0	0	1	0	0	1	1	0	155,648	(152)	KW	311,296	(304) KB
>27000	0	0	1	0	0	1	1	1	159,744	(156)	KW	319,488	(312) KB
>28000	0	0	1	0	1	0	0	0	163,840	(160)	KW	327,680	(320) KB
>29000	0	0	1	0	1	0	0	1	167,936	(164)	KW	335,872	(328) KB
>2A000	0	0	1	0	1	0	1	0	172,032	(168)	KW	344,064	(336) KB
>2B000	0	0	1	0	1	0	1	1	176,128	(172)	KW	352,256	(344) KB
>2C000	0	0	1	0	1	1	0	0	180,224	(176)	KW	360,448	(352) KB
>2D000	0	0	1	0	1	1	0	1	184,320	(180)	KW	368,640	(360) KB
>2E000	0	0	1	0	1	1	1	0	188,416	(184)	KW	376,832	(368) KB
>2F000	0	0	1	0	1	1	1	1	192,512	(188)	KW	385,024	(376) KB
>30000	0	0	1	1	0	0	0	0	196,608	(192)	KW	393,216	(384) KB
>31000	0	0	1	1	0	0	0	1	200,704	(196)	KW	401,408	(392) KB
>32000	0	0	1	1	0	0	1	0	204,800	(200)	KW	409,600	(400) KB

RE: MEMORY SIZE JUMPERS FOR 96KB MEMORY CONTROLLER

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0	OFF	OFF
32 KB	OFF	ON
64 KB	ON	OFF
96 KB	ON	ON

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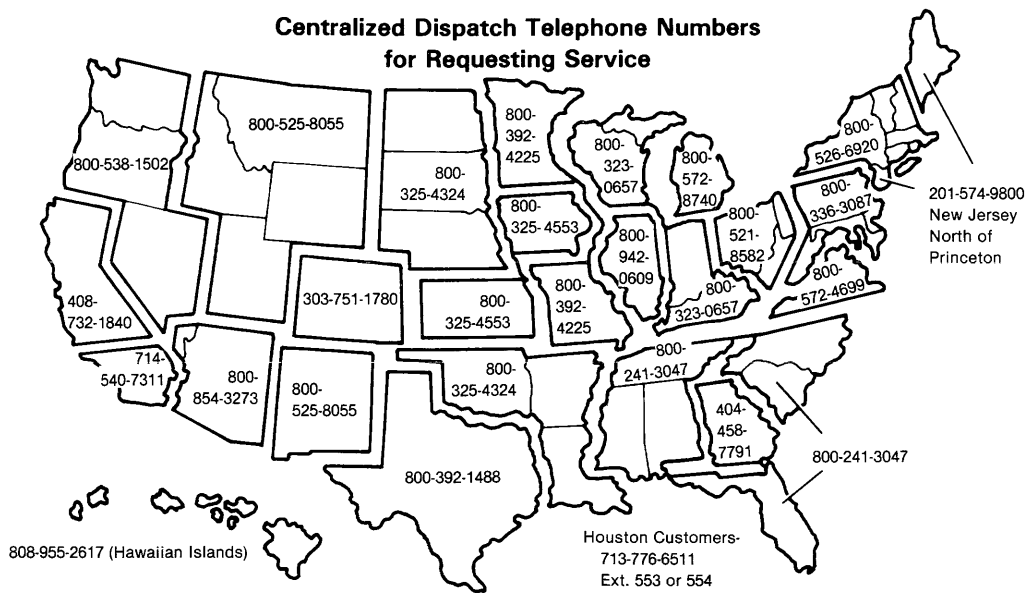

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