UNIT DIAGNOSTICS HANDBOOK

Diagnostics for 990 Communications Interfaces

Part No. 945400-9706 *J
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Volume 6

TEXAS INSTRUMENTS

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The computers, as well as the programs that TI has created to use with them, are tools that can help people better manage the information used in their business; but tools—including TI computers—cannot replace sound judgment nor make the manager's business decisions.

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Preface

Volume 6, Diagnostics for 990 Communications Interfaces, explains the diagnostic tests for the communications interfaces associated with Texas Instruments 990 computers. The manual is intended as a reference for systems analysts, customer representatives, factory service personnel, and other technical users.

Volume 6 is one of seven volumes comprising the Unit Diagnostics Handbook. Volume 1 contains information applicable to all the unit diagnostic tests. Volumes 2 through 7 contain operational and supplemental information for the specific diagnostic tests, which are grouped by volume according to equipment similarity. The test descriptions in each volume are arranged in alphabetical order by the mnemonic name of the test. The seven volumes are as follows:

Volume	Part Number	Volume Title
1	945400-9701	General Diagnostic Information
2	945400-9702	Diagnostics for 990 Processors and Memories
3	945400-9703	Diagnostics for 990 Mass Storage Devices
4	945400-9704	Diagnostics for 990 Printers, Terminals, and Interface Modules
5	945400-9705	Diagnostics for 990 Industrial Systems
6	945400-9706	Diagnostics for 990 Communications Interfaces
7	945400-9707	Diagnostics for 990 AMPL Systems

Refer to Volume 1 for a cross-reference of diagnostics contained in each volume.

ACUTST

AUTOMATIC CALL UNIT TEST

AUTOMATIC CALL UNIT TEST (ACUTST)

ACUTST

Automatic Call Unit Test

1.1 INTRODUCTION

ACUTST, the Automatic Call Unit Test, verifies the correct operation of the input, output, status, and interrupt lines of the automatic call unit (ACU) module.

1.2 TEST REQUIREMENTS

The following equipment is required to operate ACUTST:

* A Model 990 Computer with a minimum of 20K bytes of memory
* An automatic call unit module (part number 945163-0001)
* An interactive terminal
* A loading device

1.3 TEST CHARACTERISTICS

ACUTST operates under the control of DOCS. Refer to Volume 1 of the Unit Diagnostics Handbook for inforation about DOCS operation.

ACUTST consists of five parts:

Part	Title
1	State transitions test
2	Digit test
3	ACU timing test
4	Tone frequency test
5	Number dialing test

In addition to the verbs supplied by DOCS, ACUTST uses the following test execution verbs:

Test Execution Verb	Function
EA	Execute all parts
E1-E5	Execute parts 1 through 5 individually one time
LA	Loop continuously on all parts
L1-L5	Loop continuously on parts 1 through 5 individually
LD	Loop on digital sequence

You can also use the Initialize Test (IT) verb to reinitialize the ACUTST initialization parameters.

2.1 TEST INITIALIZATION

ACUTST must be loaded and initialized by DOCS before you can begin testing. Volume 1 of the Unit Diagnostics Handbook explains the loading procedure. When DOCS has loaded the ACUTST module, the name and version of the test appears:

ACUTST AUTOMATIC CALL UNIT TEST VERSION # JJJ/YY XX

where:

JJJ is the Julian Date.

YY is the year.

XX is the revision letter.

Then DOCS executes the IT verb with the following prompts:

ACU CRU BASE DEFAULT = 0000 -
The ACU communications register unit (CRU) base is the identification number of the chassis slot where the ACU board is installed. Enter the correct CRU base or accept the default.

DO YOU WANT TO USE INTERRUPTS? DEFAULT = 0 -
If you do not want to use interrupts during testing, accept the default (no). Otherwise, enter 1 (yes). When you enter 1, the following prompt appears:

ACU INTERRUPT LEVEL DEFAULT = 0 -

The ACU interrupt level is determined by the back panel wiring and is indicated in a label on the chassis.

CPU CLOCK RATE (1 = 120, 0 = 100) DEFAULT = 1 -
The central processing unit (CPU) clock rate is determined by the AC line frequency (120 for 60 Hz and 100 for 50 Hz). If the clock rate is 120, accept the default. Otherwise, enter 0.

After you respond to the initialization prompts, DOCS displays the following prompt:

EXECUTE EA VERB? (DEF=1) -

If you accept the default (yes), parts 1 through 3 execute. If you are running with interrupts, part 1 subtest 1-4 is skipped. If you are running without interrupts, part 1 subtest 5-8 is skipped. If you enter 0 (no), the following prompt is displayed:

```
VERB? -
```

You can then execute any part of ACUTST by entering the appropriate test verb.

If errors occur during a test, you should reexecute the test. Use the appropriate verb to determine the cause of the errors. The following messages appear when ACUTST executes without errors:

```
PART 1 - STATE TRANSITIONS TEST
SUBTEST 5-8 COMPLETE
SUBTEST 9-12 COMPLETE

PART 1  COMPLETE

PART 2 - DIGIT TEST
SUBTEST 1   COMPLETE
SUBTEST 2   COMPLETE
SUBTEST 3   COMPLETE
SUBTEST 4   COMPLETE
SUBTEST 5   COMPLETE

PART 2  COMPLETE

PART 3 - ACR TIMING TEST

PART 3 COMPLETE
```

2.2 TEST VERBS

ACUTST contains the following test verbs:

Test Execution Verb	Function
EA	Execute parts 1-3
E1-E5	Execute parts 1 through 5 individually one time
LA	Loop continuously parts 1-3
L1-L5	Loop continuously on parts 1 through 5 individually
LP	Loop on digital sequence

You can also use the Initialize Test (IT) verb to reinitialize the ACUTST initialization parameters. The following paragraphs discuss the test verbs.

2.2.1 Execute All Parts (EA) Verb

The EA verb executes parts 1 through 3 consecutively one time.

2.2.2 Execute Parts 1 Through 5 Individually One Time (E1-E5) Verbs

The E1 through E5 verbs execute parts 1 through 5 individually. The selected test is executed one time.

2.2.3 Loop Continuously on All Parts (LA) Verb

The LA verb causes continuous execution of parts 1 through 3 consecutively.

2.2.4 Loop Continuously on Parts 1 Through 5 Individually (L1-L5) Verbs

The L1 through L5 verbs cause parts 1 through 5 to execute individually and continuously until you press the @ key.

2.2.5 Loop on Digital Sequence (LP) Verb

The LP verb causes the continuous execution of a digital sequence that you specify. Select the digital sequence by responding to the following prompts:

RUN WITH INTERRUPTS? DEFAULT = 00

If you want to execute the test with interrupts enabled, enter 1. Otherwise, accept the default.

DIALING TECHNIQUE (0 = PULSE, 1 = TONE) DEFAULT = 00

If you want to use the pulse (rotary) dialing technique, accept the default. If you want to use tone (push-button), enter 1.

INPUT DIGITS (ENTER FF TO TERMINATE) -

Enter a string of hexadecimal digits one at a time, pressing the RETURN key after you enter each digit. When you have entered the complete digital sequence, enter FF and press the RETURN key.

The LP verb executes the digital sequence and checks the status of the ACU. Execution continues until you press the @ key.

2.3 TEST DESCRIPTIONS

ACUTST consists of five parts:

Part	Title
1	State transitions test
2	Digit test
3	ACR timing test
4	Tone frequency test
5	Number dialing test

The following paragraphs describe each test.

2.3.1 Part 1 -- State Transitions Test

Part 1 checks all state transitions of the ACU module by outputting the digits, control codes, and CRU bits necessary to exercise all states of the ACU. Part 1 also tests pulse and tone dialing, and verifies interrupts. The following messages are displayed at the start and completion of part 1:

PART 1 - STATE TRANSITIONS TEST

PART 1 COMPLETE

Part 1 consists of 12 subtests, which are described in the following paragraphs.

2.3.1.1 Subtest 1. Subtest 1 of part 1 dials digits 1 and 2 using pulse dialing without interrupts enabled. This subtest verifies that the correct number of pulses are output for pulse dialing. It also makes a status check at each state where the ACU waits for a control bit to be set. If a status line is in error, the following message is displayed:

STATUS ERROR EXPECTED = XXXX RECEIVED = XXXX

Table 1 is a summary of the CRU input/output (I/O) bit assignments:

Table 1 CRU I/O Bit Assignments

CRU Bit	Output Bit Assignment	Input Bit Assignment
0	ANB1 - Digit bit 2**0	PND - Present next digit
1	ANB2 - Digit bit 2**1	DLO - Data line occupied
2	ANB3 - Digit bit 2**2	DSS - Data set status
3	ANB4 - Digit bit 2**4	ACR - Abandon call and retry
4	DPR - Digit present	PWI - Power indication
5	CRQ - Call request	INT SUM - Interrupt summary
6	INTONF - Interrupt on/off	CCTDIS - Coupler cut through disable
7	PNDIEN - PND interrupt enable	DTDET - Dial tone detect
8	DTSIM - Dial tone simulate	DPRFF - Digit present F/F
9	ATSIM - Answer tone simulate	OH - Off hook
10	TSIM - Tone simulate	PE - Pulse enable
11	TNOT - tone/pulse	DDC - Digit dial complete
12	SINTON - single tone	SB0 - State bit 0
13	CMPLCR - clear	SB1 - State bit 1
14	Unused	SB2 - State bit 2
15	Unused	SB3 - State bit 3

2.3.1.2 Subtest 2. Subtest 2 of part 1 outputs a second dial tone required code and dials digit 1 using pulse dialing without interrupts enabled. Then it makes a status check at each state where the ACU waits for a control bit to be set.

2.3.1.3 Subtest 3. Subtest 3 of part 1 dials digit 1 followed by the end-of-number code for pulse dialing without interrupts enabled.

2.3.1.4 Subtest 4. Subtest 4 of part 1 issues an answer tone using pulse dialing without interrupts enabled.

2.3.1.5 Subtests 5 Through 8. Subtests 5 through 8 of part 1 perform the same functions as subtests 1 through 4, respectively, but use pulse dialing with interrupts enabled.

2.3.1.6 Subtests 9 Through 12. Subtests 9 through 12 of part 1 perform the same functions as subtests 1 through 4, respectively, but use tone dialing with interrupts enabled.

2.3.2 Part 2 -- Digit Test
Part 2 checks all digits and control codes by outputting these digits and codes using both pulse and tone dialing with interrupts enabled. It also makes a status check at each state where the ACU waits for a control bit to be set. The following start and completion messages are displayed:

PART 2 - DIGIT TEST

PART 2 COMPLETE

Part 2 consists of five subtests, which are discussed in the following paragraphs.

2.3.2.1 Subtest 1. Subtest 1 of part 2 tests the pulse dialer by sending digits 0 through 9 to the ACU.

2.3.2.2 Subtest 2. Subtest 2 of part 2 tests the tone dialer by sending digits 0 through 9 to the ACU.

2.3.2.3 Subtest 3. Subtest 3 of part 2 issues a second-dial-tone-required code and dials digit 1 using pulse dialing.

2.3.2.4 Subtest 4. Subtest 4 of part 2 outputs digit 1 and an end-of-number code using pulse dialing.

2.3.2.5 Subtest 5. Subtest 5 of part 2 outputs codes >A and >B followed by an end-of-number code using tone dialing.

NOTE

A value preceded by a right angle bracket (>) indicates a hexadecimal value.

2.3.3 Part 3 -- ACU Timing Test
Part 3 checks the timing for the abandon-call-and-retry status. It issues a call request to the ACU and then waits up to 45 seconds for an abandon-call-and-retry status to be reported. The following start and completion messages are displayed:

PART 3 - ACU TIMING TEST

PART 3 COMPLETE

2.3.4 Part 4 -- Tone Frequency Test.
Part 4 checks the frequencies of various tones generated by the ACU tone circuitry. The following messages are displayed:

PART 4 - TONE FREQUENCY TESTS

INPUT DIGIT

Enter the number (0 through 9) that you want to test. The ACU then outputs a continuous tone that can be monitored by either a frequency counter or an oscilloscope. Press the RETURN key to halt the tone. The following completion message is displayed:

PART 4 COMPLETE

2.3.5 Part 5 -- Number Dialing Test
Part 5 dials a phone number using the communications interface and a modem connected to the ACU. The number can be either local or long distance. When part 5 begins execution, the following message is displayed:

PART 5 - NUMBER DIALING TEST

The following prompts are displayed next:

COMM I/F CRU BASE DEFAULT = 0000
Enter the CRU base of the communications interface.

DIALING TECHNIQUE (0 = PULSE 1 = TONE) DEFAULT=00
If you want to use pulse (rotary) dialing, enter 0. If you want to use tone (push-button) dialing, enter 1.

INPUT DIGITS
Enter the number you wish to dial. You are restricted to 22 (base 10) characters. The following are the only valid ones:

The digits 0-9
(A dash has no effect)
X number terminator must be the last character before the carriage return.

For example: entering 946-7736X dials the number 946-7736.

When the test has dialed this number, it displays the following message:

PART 5 COMPLETE

Part 5 is a functional test only and indicates whether the unit as a whole is operational. If a connection is made with the dialed number, a DOCS reset (.RS) should be executed to disconnect the line.

3.1 ERROR MESSAGES

The following errors can occur during execution of ACUTST:

Error Number	Error Message
1	UNEXPECTED ACU INTERRUPT
2	UNKNOWN INTERRUPT
3	EXPECTED INTERRUPT DID NOT OCCUR
4	STATUS ERROR EXPECTED = /RESERVE BLOCK 3 /RESERVE BLOCK 3 REC
5	PULSE ENABLE NOT SET
6	PULSE TIMING ERROR
7	PULSE ENABLE DID NOT RESET
8	ACR NOT REPORTED
9	DDC NOT REPORTED
A	PND NOT SET
B	DSS NOT SET
C	PND NOT RESET
D	DSR NOT SET

BCAIMT

BCAIM COMMUNICATIONS CONTROLLER TEST

BCAIM COMMUNICATIONS CONTROLLER TEST (BCAIMT)

BCAIM Communications Controller Test (BCAIMT)

1.1 INTRODUCTION

Utilizing its on-board self-test and communications software, the BCAIM Communications Controller Test (BCAIMT) performs the following functions:

* Assures full performance of the BCAIM Communications Controller (part number 2261964-0001) hardware.
* Assures full performance of the X21 BCAIM Communications Controller (part number 2303085-0001) hardware.
* Isolates any hardware faults to a field-replaceable component or to a section of logic that may be causing the failure.
* Provides software tools to assist in the installation and check-out of modems and data access arrangements (DAA) supplied by Texas Instruments.

The Diagnostic Control System (DOCS) normally loads and controls this BCAIMT diagnostic. By specifying the external equipment connected to the BCAIM communications controller, you exercise indirect control over the tests to be performed. You can test BCAIMT with no external equipment connected, or you can attach a loopback connector, an asynchronous modem, or a synchronous modem. BCAIMT skips tests that cannot be performed and displays a message to indicate the unexecuted tests. The following is a list of titles of related documents and their associated part numbers.

Title	Part Number
BCAIM Communications Controller Installation and Operation Manual	2263886-9701
BCAIM Communications Controller Maintenance Manual	2263887-9701

Title	Part Number
BCAIM Communications Controller Specification	2265169-9901
X21 BCAIM Communications Controller Installation and Operation Manual	2263883-9701
X21 BCAIM Communications Controller Maintenance Manual	2263884-9701
X21 BCAIM Communications Controller Specification	2303089-9901
Model 990 Computer Unit Diagnostic Handbook, Volume 1, General Unit Diagnostic Information	945400-9701

1.2 TEST REQUIREMENTS

The following paragraphs list the minimum equipment and software configurations needed to execute BCAIMT.

1.2.1 Equipment Requirements

BCAIMT runs on any Model 990 Computer with at least 48K bytes of memory- and with the following equipment installed on the system:

* A BCAIM communications controller
* An appropriate interactive device

The following hardware is optional:

* A loopback connector (part number 2265197-0001). The connector fits into the 18-pin connectors in the P2 and P3 slots.
* A loopback assembly (part number 2303065-0001). The assembly mates with the 25-pin connector on the modem cable.
* A modem

1.2.2 Software Requirements

The BCAIMT diagnostic runs under control of DOCS. Refer to Volume 1 of the Unit Diagnostics Handbook for detailed explanations of the different versions of DOCS and their operation.

1.3 TEST CHARACTERISTICS

You should run all of the tests in the BCAIMT diagnostic to see if the hardware under test is functioning properly. If a failure occurs, run tests >01 through >09 to make sure the CPU interface is working properly. After making sure the interface controller is functioning correctly, you should then follow a general diagnostic isolation procedure. Assume that the failure was caused by equipment farthest away from the CPU. For example, if you run test >B with an asynchronous modem attached (the modem is in analog loopback) and the test fails, assume the modem is bad rather than the controller.

After making your assumption, select a channel test configuration that uses all the hardware except that of the isolated equipment. If the test that previously failed runs without errors from that configuration, the malfunction then lies in the isolated equipment. Using the above example, you should test all the hardware except that of the modem. In choosing test initialization parameters, set the channel test configuration to select for the EIA loopback connector. If test >B completes without errors, you have isolated the problem to the modem.

2.1 TEST EXECUTION AND CONTROL

Refer to Volume 1 of the Unit Diagnostics Handbook for information on start-up and initialization of DOCS.

2.2 LOADING

Refer to Section 3 of Volume 1 of the Unit Diagnostics Handbook for procedures to load diagnostics from all available media.

2.3 INITIALIZATION

After the test module is loaded into memory, the following message appears:

```
BCAIMT
BCAIM COMMUNICATIONS CONTROLLER DIAGNOSTIC
VERSION = *X  mm/yy
```

In this message, X represents the revision level and mm/yy represents the date of the latest release of the diagnostic.

DOCS then automatically displays prompts for the IT verb, which are described in paragraph 2.5.1. Upon receiving all of your responses, DOCS automatically executes the verb, initializing the test.

2.4 EA VERB EXECUTION

DOCS then asks you if you would like to execute the EA verb:

```
EXECUTE EA VERB?  (DEF=1) -
```

To respond to the prompt, select 1 (yes) or 0 (no). The EA verb causes all available tests to execute one time. Note that the BCAIMT diagnostic may skip some tests, depending on the test configuration selected. Upon completion, the diagnostic writes out the following prompt:

```
VERB? -
```

You may then execute any of the test verbs.

2.5 TEST VERB DESCRIPTIONS

The BCAIMT diagnostic provides the following special verbs for testing various sections of the BCAIM Communications Controller:

Verb	Function
IT	Initialize Test
ET	Execute Test
LT	Loop Test
EA	Execute All Tests One Time
LA	Loop on All Tests
DS	Display Status
PE	Display Error Count
TD	Test DAA
RC	Read Channel Interface Status
WC	Write Channel Interface
RD	Read ROM Release Date
ID	Read ID Switches
TH	Display Test History
PV	Print Verbs

Subsequent paragraphs explain their use.

2.5.1 Initialize Test (IT) Verb

The IT verb allows you to configure the diagnostic to test the BCAIM. You should consider the test configuration carefully in relation to the current system environment, as the BCAIMT diagnostic skips tests that cannot be performed in the specific test configuration. You must enter the following initialization information:

ENTER BCAIM CRU BASE ADDRESS: (DEF = XXXX)

Enter the CRU base for the chassis slot where you inserted the BCAIM board.

ENTER BCAIM INTERRUPT LEVEL: (DEF = X)

Enter the interrupt level associated with the chassis slot where you inserted the BCAIM board.

UUT TYPE X.21 BCAIM: (0=NO, 1=YES. DEF=X)

Enter 1 if the unit under test (UUT) is an X.21 BCAIM board. Otherwise, enter 0.

```
CHANNEL TEST CONFIGURATION,
  0 = NO CONNECTOR
  1 = EIA LOOPBACK CONNECTOR
  2 = LOCAL LINE / X21 LOOPBACK CONNECTOR
  3 = SYNCHRONOUS INTERNAL MODEM OR EXTERNAL
      MODEM IN ANALOG LOOPBACK
  4 = ASYNCHRONOUS INTERAL MODEM OR EXTERNAL
      MODEM IN ANALOG LOOPBACK
  5 = X.21 SWITCHED LINE, EXTERNAL DCE IN ANALOG
      LOOPBACK (LOOP T2)
( DEF = X )
```

Select the channel configuration that you want to use during execution of the diagnostic.

```
SELECT EXTERNAL ASYNCHRONOUS MODEM BAUD RATE
0 = 300BPS    1 = 1200BPS
( DEF = X )
```

This prompt appears only if you chose to a use a modem in response to the CHANNEL TEST CONFIGURATION prompt. Select the baud rate for the modem you want to use.

DO YOU WANT TO RUN THE TEST WITH INTERRUPTS? (DEF = X)

Enter 1 if you want to execute the diagnostic with interrupts. Otherwise, enter 0.

ENTER COMPUTER LINE FREQ: (0= 50, 1=60. DEF = X)
Select the line frequency used by the CPU. If you are using an S200 or S300 computer, enter 0.

FACTORY TEST MODE: (0= NO, 1=YES. DEF = X)
Enter 1 only if you are executing the diagnostic in the factory; otherwise, enter 0.

NOTE

If the default value shown by an IT verb prompt is correct, press RETURN to select that value. If it is not correct, enter the desired value.

2.5.2 Execute Test (ET) Verb

After you enter the ET verb, a prompt asks you to enter the hexadecimal number of the test to be performed.

CAUTION

When you exit a test through abnormal termination (pressing the @ key, for example), BCAIMT outputs the message TEST ABORTED. At this time, the state of the BCAIM is unknown and you cannot run any more tests without properly restarting the controller. To restart, run the Self-Test (Test >02) and the BCAIM CRU Interface Test (Test >03) in sequence.

2.5.3 Loop Test (LT) Verb

The LT verb allows continuous looping of any test. To terminate looping of a test, press the @ key, the 911 VDT CMD key, or the 913 VDT HELP key. The loop count of the number of test executions is continuously output to the front panel. In addition, if any errors have occurred in the tests, the error count appears on the interactive device.

2.5.4 Execute All Tests (EA) Verb

The EA verb causes all available tests to execute one time. Note that the BCAIMT diagnostic might skip some tests, depending on the test configuration selected.

2.5.5 Loop on All Tests (LA) Verb

The LA verb causes continuous looping of the EA test sequence. The displayed loop count equals the number of times the EA sequence has executed. The error count also appears. You can terminate this verb the same way you terminate the LT verb.

2.5.6 Display Status (DS) Verb

The DS verb displays the status of the BCAIM in the following format, where XXXX is the status word as read from the BCAIM CRU interface.

```
BCAIM INTERFACE STATUS: XXXX
```

Consult the Installation and Operation Manual for the type of BCAIM communications controller you are using for the definition of these bits.

2.5.7 Display Error Count (PE) Verb

The PE verb displays the current error count in the following format, where XXXX is the current error count.

```
BCAIMT ERRORS = XXXX
```

2.5.8 Test DAA (TD) Verb

The TD verb monitors the modem signal ring indicator (RI) for an incoming call. After selecting the verb, the following message appears:

```
ANSWER INCOMING CALL
```

During the monitoring period, the following message appears every ten seconds to let you know that the verb is active:

```
..WAITING FOR RING SIGNAL FROM MODEM..
```

When the ring signal is received, the verb sets a data terminal ready (DTR) flag. The following message appears on the interactive terminal:

```
* * RING RECEIVED!  DTR NOW SET.
          BEGIN 10 SEC WAIT FOR DSR.
```

The presence of a DTR causes the modem/DAA pair to answer the incoming call, transmit the answerback tone (about two and one half seconds), and set the DSR (Data Set Ready). If the modem sends out a DSR within ten seconds, the test completes and the following message appears:

```
DTR RESET TO DISCONNECT LINE
```

If it does not detect a DSR, the following message appears:

```
*** TIMEOUT ERROR! DSR NOT SET.
```

2.5.9 Read Channel Interface Status (RC) Verb

The RC verb reads the channel status and displays the status of the modem interface signals available. The format depends on whether the unit under test is a BCAIM or an X.21 BCAIM. For each, an X under the name of the signal represents the true state; a blank indicates the false state. The following format appears for BCAIM:

DCD	RING	SDCD	EIAEN	CTS	DSR

In addition to the above signals, the following appears for X.21 BCAIM:

RS422	X21LL	X21II	X21RI	X21NIT	X21NRI	X21CLK

2.5.10 Write Channel Interface (WC) Verb

The WC verb allows you to modify all of the control bits associated with a BCAIM communication channel. You must respond to the following questions:

```
TRANSMIT BIT RATE SELECT  (0 TO F)  X
RECEIVE BIT RATE SELECT  (0 TO F) X
DATA TERMINAL READY (PIN 20)
REQUEST TO SEND (PIN 4) X
SECONDARY REQUEST TO SEND (PIN 11 19) X
ANALOG LOOP BACK (PIN 13) X
CLOCK SELECT (1=INTERNAL ) X
OUTPUT CLOCK SELECT (PIN 24) (1 = INTERNAL) X
DISABLE DEADMAN TIMER  X
SELECT FULL DUPLEX  X
SELECT LOCAL LINE  X
```

If you are not familiar with any of these prompts, refer to the BCAIM Installation and Operation Manual for details.

Next, a command is generated, using the data that you supplied. The command instructs the BCAIM to modify the control bits on the channel interface.

2.5.11 Read ROM Release Date (RD) Verb

The RD verb reads the release date stored in the BCAIM ROM and displays it in the following format, where yy is the year and JJJ is the Julian date for the ROM installed in the BCAIM that is under test.

```
READ BCAIM ROM RELEASE DATE
ROM DATE = yy.JJJ
```

For example, a ROM date of January 2, 1980, reads as follows:

```
ROM DATE = 80.002
```

If you entered 1 (yes) in response to the FACTORY TEST MODE prompt, the ROM release data read from the BCAIM is compared to the ROM release data stored in the diagnostic. Any discrepancy in the comparison results in an information message appearing. The message is dependent upon the factory patch in use at the time.

2.5.12 Read ID Switches (ID) Verb

The ID verb reads the BCAIM ID switches and displays them in the following format, where XX represents the two-digit hexadecimal ID code.

```
READ BCAIM ID SWITCHES:
ID = XX
```

If the factory test flag is set, the value read from the BCAIM ID switches is compared to >00. Any failure in this comparison causes an error message to appear.

2.5.13 Display Test History (TH) Verb

The TH verb allows you to review all commands processed during testing once the test series completes. It records the status returned by the BCAIM for each commmand. First, the verb asks you if you want to print the test history. If you select the print option and the error message device is a printer, the complete history of the last test performed prints out. If you do not select the print option, the interactive device displays each test command block (TCB). You can then press the RETURN key to display the next TCB.

TCBs comprise several classes, each displayed with an appropriate format. All TCBs have four words of overhead which are displayed at the beginning of each TCB. The command code of the TCB is expanded on the next line of the display. The test driver control commands use the following format:

```
TCB ADDRESS = qqqq     TCB LINK WORDS = rrrr  ssss
TCB COMMAND = tttt     TCB STATUS = uuuu
(a line of  expanded TCB command code appears in this space)
```

If an error is indicated, the following message also appears:

```
* * * * *   ERROR IN THIS TCB   * * * * *
```

In this format, rrrr is a pointer to the next TCB used in the test and ssss is a pointer to the previous TCB. The TCB status (uuuu) is zero if the TCB reports no errors. When uuuu is a nonzero number, an error is associated with the TCB and the error status is expanded after the TCB command code expansion.

Commands that initialize or compare test data buffers also display part of the associated buffer and other information associated with the command.

The BCAIM has two command formats. The first has commands without data and displays the following block:

```
TIME OUT = xxxx   REMAINING TIME = yyyy
BCAIM COMMAND       B0      B1&B2   B3&B4    ST
COMMAND ISSUED      aaaa    aaaa    aaaa
STATUS RETURNED     bbbb    bbbb    bbbb     bbbb
```

The second has commands with data. This format uses the preceding block in addition to the following messages that indicate the returned status and expected status of the commands:

```
STATUS MASK         cccc    cccc    cccc     cc
STATUS EXPECTED     dddd    dddd    dddd     dd
```

The BCAIM commands that have data display the following:

```
BUFFER ADDRESS     eeee
```

Each BCAIM command TCB has a time-out xxxx, which is copied and decremented each clock tick (8.33ms for a 60 Hz line frequency and 10.0 ms for a 50 Hz line frequency). When the command is complete, the decremented copy is displayed as the remaining time.

2.5.14 Print Verbs (PV) Verb

The BCAIMT diagnostic provides the PV verb for information only, displaying the following one-line descriptions of the verbs:

IT - INITIALIZE TEST
ET - EXECUTE TEST
LT - LOOP TEST
EA - EXECUTE ALL TESTS (ONCE)
LA - LOOP ALL TESTS (FOREVER)
DS - DISPLAY STATUS
PE - DISPLAY ERROR COUNT
TD - TEST DAA
RC - READ BCAIM CHANNEL INTERFACE STATUS
WC - WRITE BCAIM CHANNEL INTERFACE
RD - BCAIM ROM RELEASE DATE
ID - READ BCAIM ID SWITCHES
TH - TEST HISTORY

2.6 TEST DESCRIPTIONS

The BCAIMT diagnostic comprises a series of numbered tests. Each uses the logic tested by its predecessors so that each test uses as little untested hardware as possible. When tests are executed in ascending order, the BCAIMT begins testing hardware at the CRU interface and progresses until it reaches the communication channel EIA interface. Those tests which target the communication channel execute only if you have selected the proper initialization parameters. If you do not properly define the channel configuration during initialization, the BCAIMT diagnostic skips the test. Table 1 defines which tests are executed or skipped in a particular configuration. Each test checks out one part of the hardware at a time in incremental steps, from the processor to the EIA channel interface to the connected modem. The following table specifies the channel connector configurations that are available to you. Each entry in the table has two parts: The part to the left of the "/" mark applies if you are running the diagnostic on the BCAIM board; the part to the right of the "/" mark applies if you are running the diagnostic on the X.21 BCAIM board.

Table 1 Test Configurations

Test Number (Hex)	No Loop-back	EIA Loop-Back	Local Line Loop-back	SYNC MDM	ASYNC MDM	X.21 DCE
	BCM/X21	BCM/X21	BCM/X21	BCM/X21	BCM/X21	BCM/X21
>01	X / X	X / X	X / X	X / X	X / X	X / X
>02	X / X	X / X	X / X	X / X	X / X	X / X
>03	X / X	X / X	X / X	X / X	X / X	X / X
>04	X / X	X / X	X / X	X / X	X / X	X / X
>05	X / X	X / X	X / X	X / X	X / X	X / X
>06	X / X	X / X	X / X	X / X	X / X	X / X
>07	X / X	X / X	X / X	X / X	X / X	X / X
>08	X / X	X / X	X / X	X / X	X / X	X / X
>09	X / X	X / X	X / X	X / X	X / X	X / X
>0A	S / S	X / X	X / S	S / S	S / S	S / S
>0B	S / S	X / X	S / S	S / S	X / X	S / S
>0C	S / S	X / X	S / S	S / S	S / S	S / S
>0D	S / S	X / X	S / S	X / X	S / S	S / S
>0E	S / S	X / X	S / S	X / X	S / S	S / S
>0F	S / S	X / X	S / S	S / S	S / S	S / S
>10	S / S	S / S	X / S	S / S	S / S	S / S

BCM - BCAIM X.21 - X.21 BCAIM
X - Test is executed S - Test is skipped

Table 1 Test Configurations (Continued)

TEST NUMBER (HEX)	NO LOOP BACK	EIA LOOP BACK	LOCAL LINE LOOP BACK	SYNC MDM	ASYNC MDM	X.21 DCE
	BCM/X21	BCM/X21	BCM/X21	BCM/X21	BCM/X21	BCM/X21
>11	S / S	S / S	X / S	S / S	S / S	S / S
>12	S / S	S / S	X / S	S / S	S / S	S / S
>13	S / S	S / S	S / X	S / S	S / S	S / S
>14	S / S	S / S	S / X	S / S	S / S	S / S
>15	S / S	S / X	S / S	S / X	S / S	S / S
>16	S / S	S / S	S / S	S / S	S / S	S / S

BCM - BCAIM X.21 - X.21 BCAIM
X - test is executed S - test is skipped

2.6.1 Test >01 -- Self-Test Started by TILINE I/O Reset

Test >01 monitors the proper start and completion of the self-test. When the firmware reports errors, the diagnostic expands and displays error messages and a list of possible causes. This test targets the following logic blocks or field-replaceable components.

* BCAIM interface logic
* TMS 9900 microprocessor
* TMS 4732 mask ROMs
* TMS 40L45 static RAMs
* TMS 9901 programmable systems interface
* TMS 9903 synchronous communications controllers

2.6.2 Test >02 -- Self-Test Started by a CRU Set Bit

Test >02 begins by setting the initiate master reset bit (bit 12). Test >02 monitors the proper start and completion of the self-test. Primarily, this test targets the initiate master reset logic and the host CRU output to the BCAIM. After starting up, this test repeats test >01. The targets of test >02 are as follows:

* Slave CRU master reset logic
* All Test >01 targets

2.6.3 Test >03 -- BCAIM CRU Interface Test

This test verifies the capability of the BCAIM to transfer command and status blocks. BCAIM diagnostic commands are used with fixed data patterns in command bytes 1 through 4. When the BCAIM firmware processes a command, the diagnostic verifies the the data and returns it to the status block for BCAIMT to verify. Test >03 targets the following:

* The host CRU data logic
* BCAIM CRU interface and control logic

2.6.4 Test >04 -- Single Word Load and Dump Test

This short test checks the ability of the BCAIM to read and write the on-board RAM. Test >04 targets the following:

* BCAIM to host control logic
* BCAIM to host data logic

2.6.5 Test >05 -- Memory Load and Dump Test

This test writes 256 bytes of data to the BCAIM RAM using the download procedure. The test transfers data back to the host and compares it to the original buffer for any errors that may have occurred. Test >05 targets the BCAIM RAM.

2.6.6 Test >06 -- 9903 Internal Loopback, Synchronous Mode

This test places the TMS 9903 in the internal loopback mode and transmits a block of synchronous data. Test >06 targets the following:

* TMS 9903 synchronous communications controller
* BCAIM slave CRU logic

2.6.7 Test >07 -- 9903 Internal Loopback, Asynchronous Mode

This test is identical to test >06 except that it transmits asynchronous data.

2.6.8 Test >08 -- 9903 Internal Loopback BOP Mode

This test is identical to test >06 except that it transmits bit-oriented protocol (BOP) data.

2.6.9 Test >09 -- 9903 Internal Loopback, BOP NRZI Mode

This test is identical to test >06 except that it transmits bit-oriented protocol nonreturn-to-zero-inverted (BOP NRZI) data.

2.6.10 Test >0A -- Interface Control Test

This test checks EIA modem controls for proper operation. You must place the loopback assembly (part number 2303065-0001) on the communications interface connector or place the loopback connector (part number 2265197-0001) on the modem cable. This test sets a particular modem control lead, checks the looped back signal to ensure that it is on, and checks all other modem leads to ensure they are not affected.

NOTE

This test does not check the EIA clocks and data signals. Test >0B is the first to check the data signals. Test >0D is the first to use the clocks.

Test >0A targets the following:

* EIA drivers and receivers
* Slave CRU decode logic TMS 9901

2.6.11 Test >0B -- EIA Channel Data Path Test, Asynchronous Mode

Using a 1200 bps or 300 bps modem or a EIA loopback connector, this test transfers and compares four blocks of data using an asynchronous data format. In asynchronous mode the baud-rate generator handles all data timing. Test >0B targets the following:

* TMS 9903 data input and output
* TMS 9903 data clocks and clock control I/O
* EIA drivers and receivers for transmit and receive data

2.6.12 Test >0C -- Bit Rate Generator Test

This test transfers sixteen blocks of data, one block for each bit rate, in an asynchronous data format. The test time is thirty seconds. The character count of each block is selected so that the block transfers in approximately one second. The time required to transmit each block is then compared to the upper and lower limits for the selected rate. If the transfer time is outside of the limits, the test reports an error. The target of test >0C is the baud-rate generator control logic.

NOTE

The EIA clocks are not checked in this test. See test >0D.

2.6.13 Test >0D -- EIA Channel Data Path Test, Synchronous Mode

Using an external synchronous modem (in analog loopback) or a loopback connector, this test transfers four blocks of data while in full-duplex mode. If the channel is connected to a modem, that modem sets the bit rate. When the test utilizes a loopback connector, it selects a 9600 bps internal bit-rate clock. At the completion of the data transfer, the test compares the received buffers to the buffers transmitted. Test >0D targets the following:

* TMS 9903 data clocks and control I/O
* EIA drivers and receivers for the modem clocks

2.6.14 Test >0E -- EIA Channel Data Path Test, BOP Mode

This test is identical to test >0D except that it transmits BOP data.

2.6.15 Test >0F -- EIA Channel Data Path Test, BOP NRZI Mode

This test is identical to Test >0D except that it transmits BOP NRZI data. This test does not run with a modem.

2.6.16 Test >10 -- Local Line Data Path Test, BOP NRZI Mode

This test checks operation of the local line interface at 9600 bps, forcing the full-duplex mode so that it can receive transmitted data. Test >10 targets the following:

* Local line data paths
* Local line power supplies

2.6.17 Test >11 -- Local Line Data Path Test, Asynchronous Mode

This test is identical to test >10, except that it transmits asynchronous data.

2.6.18 Test >12 -- Deadman Timer Test

This test checks the ability of the deadman timer to turn off RTS (Request to Send). The test time is thirty seconds. The test transfers a character string with the deadman timer enabled. After the deadman timer times out, the test compares the character count to upper and lower limits. The count of characters determines how long it took the timer to turn off RTS. The test produces an error message if the timer is out of tolerance.

2.6.19 Test >13 -- X21 Interface Test

This test checks EIA modem controls for proper operation. You must place the loopback assembly (part number 2303065-0001) on the communications interface connector. This test sets a particular modem control lead, checks the looped back signal to ensure that it is on, and checks all other modem leads to ensure they are not affected.

Test >13 targets the following:

* X.21 drivers and receivers
* Slave CRU decode logic TMS 9901

2.6.20 Test >14 -- X.21 Data Test, Synchronous Mode

You must use a loopback connector to execute Test >14. This test selects a 9600 bps internal bit-rate clock and transfers four blocks of data while in full-duplex mode. At the completion of the data transfer, the test compares the buffers received to the buffers transmitted. Test >14 targets the following:

* TMS 9903 data clocks and control I/O
* X.21 drivers and receivers

2.6.21 Test >15 -- Clocked NRZI Data Test

You must use a loopback connector to execute Test >15. This test transfers four blocks of data while in full-duplex mode. It selects a 9600 bps internal bit-rate clock and BOP NRZI. At the completion of the data transfer, the test compares the buffers received to the buffers transmitted. Test >15 targets the following:

* TMS 9903 data clocks and control I/O
* X.21 drivers and receivers

2.6.22 Test >16 -- X.21 Switched Line, X.21 DCE Loopback Test

This test transfers four blocks of data. The test selects the synchronous and full-duplex modes. Test >16 does not use a clock; instead it uses the X.21 data communications equipment (DCE) to control the speed at which bits are passed. At the completion of the data transfer, the test compares the buffers received to the buffers transmitted. Test >16 targets the X.21 drivers and receivers.

3.1 MESSAGES

The BCAIMT diagnostic issues two types of messages:

* Informative messages
* Error messages

3.1.1 Informative Messages

These messages indicate the start and the completion of tests, providing you with a brief test description. As each test starts, the BCAIMT diagnostic issues a message in the following general format:

TEST XX (.....test description.....)

When a test begins execution, it checks for a required channel configuration. If the channel is not in the required configuration, the diagnostic skips the test and issues the following message:

**** S K I P P E D ****

At the completion of each test, it issues this message:

TEST XX COMPLETE

3.1.2 Error Codes and Messages

The diagnostic issues these messages as the result of an error condition in a test. They aid you in locating a fault in the unit under test. The following pages list each possible message, along with possible causes for failure.

The BCAIMT diagnostic provides the following error messages:

Hexadecimal Error Number	Error Message
>0001	**** ERROR BCAIM CRU BIT >F IS NOT ZERO **** PROBABLE CAUSES ARE: 1) BCAIM IS NOT INSTALLED 2) BCAIM IS NOT AT THE CRU BASE SPECIFIED 3) BCAIM CRU INTERFACE LOGIC
>0002	**** BCAIM SELF-TEST WAS NOT PROPERLY STARTED **** **** BY TILINE I/O RESET **** PROBABLE CAUSES ARE: 1) BCAIM MASTER RESET LOGIC 2) CLOCK GENERATOR LOGIC 3) TLIORES NOT REACHING THE BCAIM 4) BCAIM CRU INTERFACE LOGIC
>0003	**** BCAIM SELF-TEST WAS NOT PROPERLY STARTED **** **** BY SET BIT ONE TO BIT >B **** PROBABLE CAUSES ARE: 1) BCAIM CRU WRITE INTERFACE LOGIC 2) BCAIM MASTER RESET LOGIC
>0004	**** BCAIM ENCOUNTERED AN ILLEGAL XOP **** BCAIM ERROR CODE >70 PROBABLE CAUSES ARE: 1) FAILURE OF THE TMS9900 2) POSSIBLE BAD FIRMWARE
>0005	**** BCAIM TMS9900 FAILED SELF-TEST **** BCAIM ERROR CODE >71 PROBABLE CAUSES ARE: 1) FAILURE OF THE TMS9900

Hexadecimal Error Number — Error Message

>0006

**** BCAIM FAILED ROM CRC SELF TEST ****
BCAIM ERROR CODE >72
PROBABLE CAUSES ARE:
1) TMS2532 AT LOCATION UXX
(The locations or ROMs on the board are marked with U.)

>0007

**** BCAIM FAILED RAM SELF TEST ****
BCAIM ERROR CODE >73
PROBABLE CAUSES ARE:
1) TMS XXXXX AT UXX
2) TMS9900 DATA OR ADDRESS BUS FAILURE

>0008

**** BCAIM TMS9901 CLOCK SELF TEST FAILURE****
BCAIM ERROR CODE >74
PROBABLE CAUSES ARE:
1) BCAIM CRU DECODE LOGIC.
2) TMS 9901 AT U21
3) BCAIM TTL CLOCK 3

>0009

**** BCAIM TMS9903 SELF TEST FAILURE ****
BCAIM ERROR CODE >75
PROBABLE CAUSES ARE:
1) TMS 9903 AT LOCATION "U35"
2) BCAIM CRU LOGIC.
3) BCAIM TTL CLOCK 3

>000A

**** BCAIM DID NOT COMPLETE ERROR STATUS REPORT ****
PROBABLE CAUSES ARE:
1) HOST CRU READ DATA INTERFACE
2) HOST CRU CONTROL LOGIC

>000B

**** BCAIM SELF-TEST TIME OUT ERROR ****
PROBABLE CAUSES ARE:
1) FAILURE OF BCAIM ROM
2) FAILURE OF BCAIM CLOCK GENERATOR
3) FAILURE OF THE TMS 9900
4) FAILURE OF THE BCAIM RAM

Hexadecimal Error Number	Error Message
>000C	**** ERROR IN CRU INTERFACE TEST **** PROBABLE CAUSES ARE: 1) CRU INTERFACE DATA LOGIC 2) CRU CONTROL LOGIC 3) INTERRUPTS ARE NOT REACHING THE CPU RERUN THE TEST WITHOUT INTERRUPTS
>000D	**** ERROR SINGLE WORD LOAD & DUMP TEST **** PROBABLE CAUSES ARE: 1) CRU INTERFACE DATA LOGIC 2) CRU CONTROL LOGIC
>000E	**** ERROR MEMORY LOAD AND DUMP TEST **** PROBABLE CAUSES ARE: 1) CRU INTERFACE DATA LOGIC 2) CRU CONTROL LOGIC 3) BCAIM RAM
>000F	**** ERROR 9903 INTERNAL LOOPBACK SYNC MODE **** PROBABLE CAUSES ARE: 1) FAILING TMS9903 2) SLOW SIGNAL IN THE BCAIM CRU LOGIC
>0010	**** ERROR 9903 INTERNAL LOOPBACK ASYNC MODE **** PROBABLE CAUSES ARE: 1) FAILING TMS9903 2) SLOW SIGNAL IN THE BCAIM CRU LOGIC
>0011	**** ERROR 9903 INTERNAL LOOPBACK BOP MODE **** PROBABLE CAUSES ARE: 1) FAILING TMS9903 2) SLOW SIGNAL IN THE BCAIM CRU LOGIC

Hexadecimal Error Number — Error Message

>0012

**** ERROR 9903 INTERNAL LOOPBACK BOP NRZI MODE ****
PROBABLE CAUSES ARE:
1) FAILING TMS 9903
2) SLOW SIGNAL IN THE BCAIM CRU LOGIC

>0013

**** ERROR EIA LOOPBACK VERIFICATION ****
PROBABLE CAUSES ARE:
2) EIA LOOPBACK CONNECTOR IS NOT INSTALLED
3) LOCAL LINE LOOPBACK CONNECTOR IS INSTALLED
4) FAILURE OF THE "SRTS" DRIVER OF "SDCD" RECEIVER
5) FAILURE OF THE TTL MODEM CONTROL LOGIC

>0014

**** ERROR EIA MODEM CONTROL ****
PROBABLE CAUSES ARE:
1) FAILURE OF AN EIA DRIVER OR RECEIVER
2) FAILURE OF THE TMS 9903
3) FAILURE OF THE DEADMAN TIMER LOGIC
4) FAILURE OF THE TTL MODEM CONTROL LOGIC

>0015

**** ERROR LOCAL LINE LOOPBACK VERIFICATION ****
PROBABLE CAUSES ARE:
1) LOCAL LINE LOOPBACK CONNECTOR IS NOT INSTALLED
2) FAILURE LOCAL LINE INTERFACE BIT

>0016

**** ERROR LOCAL LINE INTERFACE ****
PROBABLE CAUSES ARE:
2) FAILURE OF AN EIA DRIVER OR RECEIVER
3) FAILURE OF THE TMS 9903
4) FAILURE OF THE DEADMAN TIMER LOGIC
5) FAILURE OF THE TTL INTERFACE CONTROL LOGIC

>0017

**** ERROR CHANNEL DATA TEST ASYNC MODE ****
PROBABLE CAUSES ARE:
1) BIT RATE GENERATOR AT 32X CLOCK
2) THE FAILING TMS 9903
3) FAILURE OF THE EIA XMIT & RCV DATA LOGIC

Hexadecimal Error Number | Error Message

>0018

**** ERROR BIT RATE TIMING ERROR ****
BIT RATE SELECT CODE = XX
UPPER TIME LIMIT = XXXX
LOWER TIME LIMIT = XXXX
TEST TIME = XXXX
PROBABLE CAUSES ARE:
1) THE BIT RATE GENERATOR
2) THE BIT RATE GENERATOR CRYSTAL

>0019

**** ERROR CHANNEL DATA TEST SYNC MODE ****
PROBABLE CAUSES ARE:
1) FAILURE OF EIA CLOCK LOGIC
2) OTHER CHANNEL DATA CLOCK LOGIC
3) FAILURE OF THE TMS 9903

>001A

**** ERROR CHANNEL DATA TEST BOP MODE ****
PROBABLE CAUSES ARE:
1) FAILURE OF THE TMS 9903

>001B

**** ERROR CHANNEL DATA TEST BOP NRZI MODE ****
PROBABLE CAUSES ARE:
1) FAILURE OF THE TMS 9903

>001C

**** ERROR LOCAL LINE DATA BOP NRZI MODE ****
PROBABLE CAUSES ARE:
1) ISOLATED POWER SUPPLIES
2) LOCAL LINE DRIVES OR RECEIVERS
3) TTL DATA SELECT LOGIC

>001D

**** ERROR LOCAL LINE DATA ASYNC MODE ****
PROBABLE CAUSES ARE:
1) LOCAL LINE DRIVES OR RECEIVERS
2) ISOLATED POWER SUPPLIES

Hexadecimal Error Number	Error Message
>001E	**** ERROR DEADMAN TIMER TEST **** PROBABLE CAUSES ARE: 1) NE555 TIMER OR TIMING COMPONENTS 2) TTL 'RST' LOGIC
>001F	**** ERROR X21 LOOPBACK VERIFICATION **** PROBABLE CAUSES ARE: 1) LOOPBACK CONNECTOR IS NOT INSTALLED 2) FAILURE X21 INTERFACE BIT
>0020	**** ERROR X21 BCAIM TYPE DOES NOT MATCH UUT TYPE **** PROBABLE CAUSES ARE: 1) WRONG TYPE SELECTED IN "IT" VERB 2) BCAIM INSTALLED NOT X21 BCAIM
>0021	**** ERROR X21 BCAIM TYPE DOES NOT MATCH UUT TYPE **** PROBABLE CAUSES ARE: 1) WRONG TYPE SELECTED IN "IT" VERB 2) BCAIM INSTALLED NOT X21 BCAIM
>0022	**** ERROR X21 INTERFACE **** PROBABLE CAUSES ARE: 1) FAILURE OF AN RS422 DRIVER OR RECEIVER 2) FAILURE OF THE TMS 9903 3) FAILURE OF THE X21 TTL INTERFACE CONTROL LOGIC
>0023	**** ERROR X21 DATA TEST SYNC MODE **** PROBABLE CAUSES ARE: 1) FAILURE OF AN RS422 DRIVER OR RECEIVER 2) FAILURE OF THE TMS 9903 2) FAILURE OF THE X21 TTL INTERFACE CONTROL

Hexadecimal Error Number	Error Message
>0024	**** ERROR CLOCKED NRZI DATA TEST **** PROBABLE CAUSES ARE: 1) FAILURE OF THE NRZI TTL LOGIC 2) FAILURE OF THE NRZI SELECT LOGIC
>0025	**** ERROR X21 DCE LOOPBACK TEST MODE **** PROBABLE CAUSES ARE: 1) FAILURE OF AN X21 DRIVER OR RECEIVER 2) X21 DCE FAILURE 3) FAILURE OF THE TMS 9903

COM90X

TMS 9902/9903 COMMUNICATIONS IC TEST

TMS 9902/9903 COMMUNICATIONS IC TEST (COM90X)

COM90X

TMS 9902/9903 Communications IC Test

1.1 INTRODUCTION

COM90X, the TMS 9902/9903 communications integrated circuit (IC) test, verifies the correct operation of the Texas Instruments TMS 9902 and TMS 9903 communications controllers. It also verifies the total operation of the communications controller ports for the Model 990 and the Business System computers.

The term port in this diagnostic includes:

* The communications controller itself.
* The additional circuitry required to complete the interface signals to an RS-232 connector.

COM90X tests the TMS 9902/9903 communications controller through an internal loopback facility; it does all other testing through an external loopback connector.

COM90X can test the following:

* Port 1 of a 990/10A CPU
* Ports 1 through 3 of a 990/5 CPU
* Two-channel (CI-421) and four-channel (CI-422) communications option boards for Business System 200, S300, and S300A computers
* Ports 1 and 2 of the 990 CI-402 CRU interface

1.2 TEST REQUIREMENTS

You must have the following equipment to operate the COM90X test:

* A Model 990 or Business System Computer with a minimum of 64K bytes of memory
* A test communications port
* An interactive terminal
* A device to load the test module into the CPU memory

You must use a loopback connector to execute COM90X. The connector can be one of the following:

* 25-pin Engineering Industries Association (EIA) loopback connector (part number 948550-0001, revision C or later). Select this connector when using a 990/5 CPU.
* 25-pin EIA loopback connector for the two-channel communications option board (part number 2230510-0001).
* 25-pin EIA loopback connector for the four-channel communications option board (part number 2528940-0001).
* 18-pin loopback connector (part number 2303065-0001) Select this connector when using a /10A CPU or CI-402.

1.3 TEST CHARACTERISTICS

Familiarize yourself with these characteristics of COM90X before operating the test:

* COM90X operates under the control of DOCS. Information about DOCS operation on a Model 990 Computer is in Volume 1 of the Unit Diagnostics Handbook.

* COM90X consists of four tests and is structured so that you can execute either the complete set of tests or any separate test. These tests are as follows:

Test	Title
1	Timer/interrupt test
2	Data set interface test
3	TMS 9902 communications test
4	TMS 9903 communications test

* COM90X uses a number of test verbs to execute various tests and functions. The EA, ET, LA, and LT verbs are the primary test verbs. You should always execute these verbs first, preferably using a loopback connector. You can use the remaining verbs for testing external equipment such as modems, DAAs, and communications lines. The COM90X verbs are as follows:

Verb	Function
DP	Display port status
EA	Execute all tests one time
ET	Execute individual test
IP	Initialize port
IT	Initialize test
LA	Loop on all tests continuously
LT	Loop on a test continuously
PE	Print errors
PV	Print verbs
RP	Reset port
TD	Test data access arrangement (DAA)

1.4 TEST ENVIRONMENTS

COM90X is designed to test the following equipment environments:

1. Model 990/5 CPU -- Port 1, 2, or 3
2. Model 990/10A CPU -- Port 1
3. Model S200 CPU -- Port 1, 2, 3, 4, 5, or 6
4. Model S300 CPU -- Port 1, 2, 3, 4, 5, or 6
5. Model S300A CPU -- Port 1, 2, 3, 4, 5, or 6
6. Model 990 CI-402 CRU interface - Port 1 or 2 (These ports are referred to as 1 and 2 in the diagnostic but are labelled 0 and 1, respectively, on the hardware.)

Initialization options allow you to select the proper environment. You can set all operating parameters automatically, or you can specify any other arbitrary environment parameters for special test circumstances.

COM90X runs in either internal or external test mode. These three options are provided for the external mode:

* Digital loopback (DI)
* Analog loopback (AL) -- Modem testing on any TMS 9902/9903 port
* Far End loopback (FE) -- Supported on TMS 9903 test only

The test runs in external mode when a loopback connector or modem is installed. It runs in internal mode when none of these devices are present. You cannot run certain tests in internal mode. To run the entire COM90X test, you must select digital loopback mode and use either a 25-pin loopback connector or the 18-pin loopback connector. Refer to Appendix B for an illustration of the portions of the system that are tested in each mode.

COM90X operates if you use one of the ports of a multiport interface as the DOCS interactive terminal; however, it does not test that port. You can use only one port for a DOCS device, and that port must be the interactive terminal.

During test initialization, a DOCS service routine locates where the DOCS interactive device is connected. If DOCS determines that the interactive device is connected to one of the possible test ports, then it writes the following message:

DOCS DEVICE DETECTED. AT CRU ADDR=XXXX SKIPPED.

where:

XXXX is the CRU address of the DOCS device.

To test the interactive terminal port from which DOCS was run, use this procedure:

1. Move the cable to a new port location.
2. On a Business System Computer, power down. On other computers, press the HALT, RESET, and CLEAR keys on the computer front panel.
3. Reconnect the DOCS terminal to a previously tested port.
4. Reload DOCS.

2.1 TEST INITIALIZATION

COM90X must be loaded and initialized by DOCS before you can begin testing. Volume 1 of the Unit Diagnostics Handbook explains the loading procedure. When DOCS has loaded the COM90X module, the name and version of the test appears:

```
COM90X - TMS 9902/03 COMMUNICATION IC TEST. VERSION=XX : JJJ/YY
```

where:

XX is the revision letter.

JJJ is the Julian date.

YY is the year.

Then DOCS executes the IT (Initialize Test) verb by giving you a series of initialization prompts to answer.

DOCS then displays the initialization prompts described in the following paragraphs. Press the RETURN key if the default value displayed with the prompt (shown as DEF=) is the one you want. Otherwise, type a value and press the RETURN key. If you enter a value that is not acceptable, the following message prompts you for a correct response:

```
*** INVALID ENTRY! RE-ENTER DATA:
```

If you want to alter any of the initialization parameters later, reexecute the Initialize Test (IT) verb.

The initialization prompts are as follows:

```
ENTER TEST ENVIRONMENT:
(1=990/5, 2=990/10A, 3=S200, 4=S300/300A, 5=CI-402) DEF=X -
```

Type the number appropriate to the hardware assembly you want to test.

```
RUN WITH INTERRUPTS? ( 0=NO, 1=YES ) DEF=X -
```

Enter 0 if you do not want to test the interrupts; otherwise, enter 1. Your response may depend upon whether a particular environment has the ability for the interrupt to be jumper connected or not.

TEST CI-421 COMM OPTION? (0=NO, 1=YES) DEF=X

This prompt appears only if you are using a Business System computer. Enter 1 if you want to select the 2-channel communications option. If the computer you are using is equipped with a 4-channel communications option board (COB), you can select the 2-channel option or wait for the prompt that follows to select the 4-channel option. However, you must choose one of the communications options. If the computer you are using is equipped with a 2-channel COB, you must enter 1 in response to this prompt.

TEST CI-422 COMM OPTIONS? (0=NO, 1=YES) DEF=X

This prompt appears only if you are using a Business System computer. Enter 1 only if the computer you are using is equipped with the 4-channel COB and you want to select the 4-channel communications option.

ENTER LINE FREQ (0=50HZ, 1=60) DEF=X -

Specify the line frequency of the computer by entering either 1 to select 60 hertz or 0 to select 50 hertz. This prompt is not displayed if you previously selected the either the S200, S300, or S300A environment.

ENTER TEST CRU ADDRESS: DEF=0800 -

This prompt is displayed only if you selected the CI-402 environment. Enter the CRU address of the CI-402 or accept the default (0800). Valid CRU addresses are in the range of >0800 through >1B00.

ENTER INTERRUPT LEVEL: DEF=X -

This prompt is displayed only if you selected the CI-402 environment and are running with interrupts. Enter the interrupt level of the CI-402.

ENTER 990/10A DSR JUMPER: (0=DCD, 1=DSR) DEF=X -

This prompt is displayed only if you selected the 990/10A environment. Respond with 0 for Data Carrier Detect or 1 to designate the DSR jumper connection at the edge of the 990/10A CPU board.

MANUAL OR AUTO PARAMETERS? (0=MAN, 1=AUTO) DEF=X -

If you select automatic mode, COM90X automatically sets all the parameters for the environment you selected in response to the ENTER TEST ENVIRONMENT prompt.

If you select manual mode, individual initialization prompts allow you to select desired parameters, according to the environment you selected in response to the ENTER TEST ENVIRONMENT prompt.

If you want to view all the parameters of a particular environment, select manual mode or use the IP verb. If you use the IP verb, COM90X is automatically switched to manual mode.

The following paragraphs describe the additional initialization prompts for automatic and manual mode.

2.1.1 Automatic Mode Test Initialization Prompts

The following prompts appear:

RUN INTERNAL OR EXTERNAL MODE? (0=INT, 1=EXT) DEF=X -

Select 1 if you want to use a loopback connector. Select 0 if you want to use the IC internal loopback mode instead of a connector. In this mode, COM90X cannot test the external driver/receiver circuits.

NOTE

If you select internal mode and there are external devices connected to the port being tested, you may receive misleading error messages. Therefore, when you select internal mode, disconnect any external devices (including the loopback connector).

If you specify external mode (indicating that one of the loopback conditions is present), COM90X displays the following prompt:

EXT LOOPBACK TYPE? (DI=DIGITAL, AL=ANALOG, FE=FAR END) DEF=DI -

NOTE

If you select AL or FE, you should execute a digital or an internal loopback test mode first to ensure that the TMS 9902/9903 communication integrated circuitry is functioning properly.

The loopback type depends on the test environment. Appendix B illustrates the portions of the system that are tested in each mode. The following table states the type of loopback connector required for each test mode.

Test Mode	Loopback Connector	Modem	Comm Line
DI - Digital loopback	Yes	No	No
AL - Analog loopback	No	Yes	No
FE - Far-End loopback	No	Yes	Yes

The following additional prompts are displayed if you select analog or far-end:

LOOPBACK PLUGS INSTALLED ON ALL PORTS ? DEF = 1 -
Select 1 if a loopback plug is installed on each port; otherwise, select 0. Initialization is complete and the EXECUTE EA VERB prompt appears next.

ENTER PORT NUMBER: (1=1, 2=2, ETC., F=ALL) DEF=X -
If you entered AL or FE in response to the EXT LOOPBACK TYPE? prompt, then this prompt appears. For AL or FE test you must initialize each.

TI INTERNAL MODEM? (0=NO, 1=YES) DEF=X
If you enter AL in response to the EXT LOOPBACK TYPE? prompt, this prompt appears. If you enter 0, indicating that the device is not a TI modem, the following prompt is displayed:

MODEM AL SWITCH ON? (0=NO, 1=YES) -

Confirm that the modem analog switch is in the ON position. If the switch is on, type a 1 (YES). If not, turn it on, then enter a 1.

NOTE

When testing modems, make sure that the CTS line is set on MODEM.

FAR END IN REMOTE LOOPBACK? (0=NO, 1=YES)
If you enter FE in response to the EXT LOOPBACK TYPE? prompt, this prompt appears. Confirm that the far-end connection is in loopback mode and enter a 1.

ENTER 9903 DATA MODE (0=ASYNC, 1=SYNC) DEF=X -

This prompt is displayed if you are testing a TMS 9903 with a modem. Select the data mode, asynchronous or synchronous, for that port.

ENTER MODEM BAUD RATE: (1) 300, (2) 1200, (3) 1800,
(4) 2400, (5) 4800, (6) 9600, DEF=X

This prompt appears if you are testing analog or far-end loopback on external modems. Enter the baud rate associated with the modem.

EXECUTE EA VERB? (0=NO, 1=YES) DEF=X

This prompt follows the initialization prompts. If you want to execute the entire COM90X test, respond with a 1; otherwise, enter a 0.

If you enter a 1 (YES), the port number is requested as follows:

ENTER PORT NUMBER: (1=1, 2=2, ETC., F=ALL) DEF=X -

After you enter the port number, DOCS executes all COM90X tests that can be run in the test environment and mode that you selected.

NOTE

If the Business System computer with 4-channel communication option is selected, port numbers should be chosen according to Table 3 in Section 4.

If the EA verb executes without errors, you can assume that the communications ports that were tested are operating correctly, and you do not need to perform further testing. However, if any error messages are displayed, rerun the test or tests that indicate errors, using the appropriate testing verbs to determine the cause.

NOTE

When any verb displays the instruction "INSTALL LOOPBACK CONNECTOR AT PORT X -", install the connector and then press RETURN.

When the test sequence is completed, DOCS displays the VERB? prompt. You can enter any other DOCS or COM90X test verb.

2.1.2 Manual Mode Test Initialization Prompts

The following prompts appear only if you specified manual mode initialization (you responded 0 in response to the MANUAL OR AUTO PARAMETERS? initialization prompt). Manual mode gives you the following options:

* It allows you to use the testing capabilities of COM90X for a special environment.

* It allows you to test the same port with different parameters (for example, you can run COM90X in both internal and external mode). Familiarize yourself with the parameters in paragraph 4.2 before using this mode.

NOTE

The defaults shown are for the 990/5, port 1.

ENTER PORT NUMBER : (1=1, 2=2 ETC, F=ALL) DEF=X -
Enter the number of the port you want to test. In manual mode, you must initialize each port to be tested individually. Therefore, F is not a valid response.

ENTER DEVICE TYPE: (0=9902, 1=9903) DEF=X -
Enter the number representing the communications IC type that you want to test.

ENTER TEST CRU ADDRESS: DEF=XXXX -
Enter the CRU address, in the range from 0 to >FFFF. The default CRU address is the value used in register 12 for TMS 990X test device addressing.

ENTER PORT CONTROL CRU ADDRESS: DEF=XXXX -
Enter the CRU address, in the range from 0 to >FFFF. The default port control CRU address is the value used in register 12 for control of the port operations.

ENTER INTERRUPT LEVEL: DEF=X -
This prompt appears only if you are in manual mode and you entered 1 (yes) in response to the RUN WITH INTERRUPTS? prompt. Enter an interrupt level number, in the range from 3 to >F.

ENTER INTERRUPT ENABLE BIT: DEF=24 -
This prompt appears only if you are in manual mode and you entered 1 (yes) in response to the RUN WITH INTERRUPTS? prompt. Enter the communications IC interrupt enable bit value, in the range from 1 to >FF. The interrupt enable bit address is relative to the port control CRU address.

ENTER CLOCK FREQ: (0=2.5, 1=3.0, 2=4.0 MHZ) DEF= X
Enter the clock frequency that the communications IC receives.

ENTER EXT COMM ENABLE BIT: DEF=XX -
Enter the communications IC external communications enable bit value, in the range from 1 to >FF. Enter 0 to indicate that there is no external communications enable function.

ENTER DTR BIT: DEF=XX -
Enter the CRU bit value, in the range from 1 to >FF, for the Data Terminal Ready (DTR) signal to the modem. Enter 0 to indicate that the signal is not used.

ENTER ANALOG LOOPBACK BIT: DEF=XX -
Enter the CRU bit value, in the range from 1 to >FF, for the Analog Loopback signal to the modem. Enter 0 to indicate that the signal is not used.

ENTER SRTS BIT: DEF=XX -
Enter the CRU bit value, in the range from 1 to >FF, for the Secondary Request to Send (SRTS) signal from the modem. Enter 0 to indicate that the signal is not used.

ENTER DCD BIT: DEF=XX -
Enter the CRU bit value, in the range from 1 to >FF, for the Data Carrier Detect (DCD) signal from the modem. Enter 0 to indicate that the signal is not used.

ENTER RING BIT: DEF=XX -
Enter the CRU bit value, in the range from 1 to >FF, for the Ring signal from the modem. Enter 0 to indicate that the signal is not used.

ENTER SDCD BIT: DEF=XX -
Enter the CRU bit value, in the range from 1 to >FF, for the Secondary Data Carrier Detect (SDCD) signal from the modem. Enter 0 to indicate that the signal is not used.

ENTER HDPX BIT: DEF=XX -
Enter the CRU bit value, in the range from 1 to >FF, for the half duplex enable bit in the port CRU control space. Enter 0 to indicate that half duplex is not available.

RUN INTERNAL OR EXTERNAL MODE? (0=INT, 1=EXT) DEF=X -
Select 1 if you want to use a loopback connector. Select 0 if you want to use the IC internal loopback mode instead of a connector. In this mode, COM90X cannot test the external driver/receiver circuits.

NOTE

If you select 0 and there are external devices connected to the port under test, you may receive misleading error messages. Therefore, when you select internal mode, disconnect any external devices (including the loopback connector).

If you specify external mode (indicating that one of the loopback conditions is present) COM90X displays the following prompt:

```
EXT LOOPBACK TYPE? ( DI=DIGITAL, AL=ANALOG, FE=FAR END )
     DEF=DI -
```

NOTE

If you select AL or FE, you should execute a digital or an internal loopback test mode first to ensure that the TMS 9902/9903 communication integrated circuitry is functioning properly.

The loopback type depends upon the test environment. Appendix B illustrates the portions of the system that are tested in each mode. The following table states the type of loopback connector required for each test mode and the additional prompts that are displayed if you select analog or far-end.

Test Mode	Loopback Connector	Modem	Comm Line
DI - Digital loopback	Yes	No	No
AL - Analog loopback	No	Yes	No
FE - Far-End loopback	No	Yes	Yes

DOES LOOPBACK PLUG LOOPBACK RI? (0=NO, 1=YES) DEF=X

If you enter DI in response to the EXT LOOPBACK TYPE? prompt, this prompt appears. It refers to the pin connections for the ring indicator (RI). In most cases, enter 0 if you are using a 990/5 computer and 1 if you are using any other type of computer. For special configurations, check the pin connection drawings in paragraph 4. If you are testing with a digital loopback environment, initialization is complete and the EXECUTE EA VERB? prompt appears next.

TI INTERNAL MODEM? (0=NO, 1=YES) DEF=X

If you enter AL in response to the EXT LOOPBACK TYPE? prompt, this prompt appears. If you enter 0, indicating that the device is not a TI modem, the following prompt is displayed:

```
MODEM AL SWITCH ON? ( 0=NO, 1=YES ) -
```

Confirm that the modem analog switch is in the ON position.

If the switch is on, type a 1 (YES). If not, turn it on, then enter a 1.

FAR END IN REMOTE LOOPBACK? (0=NO, 1=YES)
If you enter FE in response to the EXT LOOPBACK TYPE? prompt, this prompt appears. Confirm that the far-end connection is in loopback mode and enter a 1.

ENTER 9903 DATA MODE (0=ASYNC, 1=SYNC) DEF=X -
This prompt is displayed if you are testing a TMS 9903 with a modem. Select the data mode, asynchronous or synchronous, for that port.

ENTER MODEM BAUD RATE: (1) 300, (2) 1200, (3) 1800,
(4) 2400, (5) 4800, (6) 9600, DEF=X
This prompt appears if you are testing analog or far-end loopback on external modems. Enter the baud rate associated with the modem.

EXECUTE EA VERB? (0=NO, 1=YES) DEF=X
This prompt follows the initialization prompts. If you want to execute the entire COM90X test, respond with a 1; otherwise, enter a 0.

If you enter a 1 (YES), the port number is requested as follows:

ENTER PORT NUMBER: (1=1, 2=2, ETC., F=ALL) DEF=X -

After you enter the port number, DOCS executes all COM90X tests that can be run in the test environment and mode that you selected.

If the EA verb executes without errors, you can assume that the communications ports that were tested are operating correctly, and you do not need to perform further testing. However, if any error messages are displayed, rerun the test or tests that indicate errors, using the appropriate testing verbs to determine the cause.

NOTE

When any verb displays the instruction "INSTALL LOOPBACK CONNECTOR AT PORT X -", install the connector and then press RETURN.

When the test sequence is complete, DOCS displays the VERB? prompt. You can enter any other DOCS or COM90X test verb.

2.2 TEST VERBS

Whenever DOCS displays the VERB? prompt, you can enter any DOCS or COM90X test verb described in the following paragraphs. To display the VERB? prompt, press the @, CMD, HELP, or ESC key, depending upon your terminal.

Most COM90X test verbs fall into two categories: test execution verbs and utility verbs. Test execution verbs execute one or more of the COM90X tests.

Test Execution Verb	Function
EA	Execute all tests one time
ET	Execute an individual test one time
LA	Loop on all tests
LT	Loop on an individual test

Utility verbs help you isolate errors that are detected during the execution of test parts:

Utility Verb	Function
DP	Display port status
PE	Print errors
PV	Print verb descriptions
RP	Reset port
TD	Test data access arrangement

Additionally, use the IT (Initialize Test) and IP (Initialize Port) verbs to reinitialize the COM90X parameters. The test execution verbs are discussed in paragraphs 2.2.1 through 2.2.4, utility verbs in paragraphs 2.2.5 to 2.2.9, IT verb in paragraph 2.2.10, and IP verb in paragraph 2.2.11.

If you are running COM90X in automatic mode, the diagnostic verifies that the port number(s) you designate in response to verb prompts are valid for the environment you selected during initialization. If a port number is not valid, COM90X issues a warning message and displays the prompt again.

If you selected manual mode, you can only designate ports that you specified in response to the ENTER PORT NUMBER initialization prompt. If you now want to test additional ports, you must reinitialize.

When test execution time is lengthy, COM90X displays a blip character ">" at the terminal intermittently to indicate that the test is still in progress.

2.2.1 Execute All Tests One Time (EA) Verb

The EA verb executes the total series of tests required to fully test a given environment one time. It runs Tests 1, 2, and 3 for a TMS 9902 and Tests 1, 2, and 4 for a TMS 9903. If the test sequence is being performed in a multiport environment, a prompt reminds you to connect the loopback connector to the necessary ports when required.

The prompts for the EA verb appear as follows:

EXECUTE ALL TESTS:

ENTER PORT NUMBER: (1=1, 2=2, ETC, F=ALL) DEF=F

Specify F if you want to test all ports during the execution of COM90X. Otherwise, enter the number of the port you wish to test.

INSTALL THE LOOPBACK CONNECTOR AT PORT X

If you indicated during initialization that not all ports had loopback plugs installed, the verb displays this message for each port (X) missing a loopback connector. Install the connector and then press RETURN.

2.2.2 Execute Individual Test (ET) Verb

The ET verb executes any one of Tests 1 through 4, one time. If the test is being run in digital loopback (DI) mode, a prompt reminds you to connect the loopback connector.

The ET verb displays the following prompts:

EXECUTE SINGLE TEST: ENTER TEST NUMBER: DEF=X

Enter the number for the test you want to execute.

ENTER PORT NUMBER: (1=1, 2=2, ETC, F=ALL) DEF=F

Specify F if you want to test all ports during the execution of COM90X. Otherwise, enter the number of the port you wish to test.

INSTALL THE LOOPBACK CONNECTOR AT PORT X

This message appears when you are required to install the loopback connector. The X represents the number of the port you are testing. Install the connector, then press RETURN.

NOTE

Test 1 does not require the use of a loopback plug. Therfore, if you are executing Test 1, the INSTALL THE LOOPBACK CONNECTOR AT PORT X prompt does not appear.

2.2.3 Loop On All Tests Continuously (LA) Verb

The LA verb causes Tests 1, 2, and 3 (for the 9902) or Tests 1, 2, and 4 (for the 9903) to execute continuously until you press the @, CMD, HELP, or ESC key. You must install a loopback connector on each port that you designate.

The LA verb displays the following prompt:

LOOP ALL TESTS:

ENTER PORT NUMBER: (1=1, 2=2, ETC., F=ALL) DEF=x

Specify the individual port number or specify F to select all ports. The default value displayed depends upon previous prompt responses.

If the port you designate does not exist for the environment you specified during initialization, the verb issues a warning message and displays the prompt again.

If you are running COM90X in manual mode and you attempt to designate a port that you did not specify during initialization, the verb aborts. In this case, DOCS then displays the VERB? prompt.

2.2.4 Loop On a Test Continuously (LT) Verb

The LT verb causes the selected test to execute continuously until you press the @, CMD, HELP, or ESC key, depending upon your terminal. If a loopback connector is required, it reminds you to connect it at the beginning of the test.

The LT verb displays the following prompts:

LOOP SINGLE TEST: ENTER TEST NUMBER: DEF=X

Enter the number of the test you want to execute.

ENTER PORT NUMBER: (1=1, 2=2, ETC, F=ALL) DEF=F

Specify F if you want to test all ports during the execution of COM90X. Otherwise, enter the number of the port you are using.

INSTALL THE LOOPBACK CONNECTOR AT PORT X

This message appears when you are required to install the loopback connector. The X represents the number of the port you are testing. Install the connector, then press RETURN.

2.2.5 Print Errors (PE) Verb

The PE verb displays the current error and loop counts. The verb's message is also displayed automatically following execution of each test verb and following a pass through a loop.

The PE verb displays the following message:

```
*** STATUS ERRORS=XXXX.   TEST ERRORS=XXXX ***
     TOTAL ERRORS=XXXX.   LOOPS=XXXX.
```

This message gives you the number of status errors, test errors, and total errors generated by the test, and the number of times the test looped.

2.2.6 Print Verbs (PV) Verb

The PV verb causes COM90X to list the test verbs.

2.2.7 Display Port Status (DP) Verb

The DP verb reads the modem status of a port. The verb displays the following prompt:

```
DISPLAY PORT STATUS
ENTER PORT NUMBER: (1=1, 2=2, ETC, F=ALL) DEF=X  CRU ADDR = XXXX
     Enter the number of the port you are using.
     F is not a valid response in this case.
```

After you select a port, the verb displays the the modem interface signals available (an X indicates that the signal is active) in the following format:

```
LOWER 990X=LLLL. UPPER 990X=UUUU. PORT STATUS=PPPP.
  RTS   CTS   DSR   DCD   SDCD  RING
```

where:

RTS = Request to send
CTS = Clear to send
DSR = Data set ready
DCD = Data carrier detect
SDCD = Secondary data carrier detect
RING = Ring

The verb first displays the status of the lower 16 bits, those at the CRU address. They are followed by the status of the upper 16 bits, those at the CRU address plus 16. The port status is that of the port control CRU address plus 32 bits.

2.2.8 Reset Port (RP) Verb

The RP verb causes a reset of the communications port. The RP verb displays the following prompt:

```
ENTER PORT NUMBER:  ( 1=1, 2=2, ETC, F=ALL ) DEF=X
```

Enter the number of the port you are using. F is not a valid response in this case.

The verb then displays the CRU address of the reset port as follows:

```
RESET PORT:  CRU ADDR=XXXX
```

2.2.9 Test DAA (TD) Verb

The TD verb tests a data access arrangement (DAA). The verb displays the following prompt:

```
TEST DAA
ENTER PORT NUMBER: ( 1=1, 2=2, ETC, F=ALL ) DEF=X
```

Enter the number of the port you are using. F is not a valid response in this case.

Next, call the station number of the DAA from a nearby telephone. The test monitors the incoming RING signal for a condition indicating that an incoming call has been detected. During this monitoring period, the following message is output every ten seconds to notify you that the test is active:

```
..WAITING FOR RING SIGNAL FROM MODEM..
```

When the RING signal is received, the test sets the Data Terminal Ready (DTR) modem lead, causing an answer-back tone to be transmitted on the communications line. Then the following message is output:

```
RING RECEIVED!  DTR NOW SET.  BEGIN 10 SEC WAIT FOR DSR.
```

If the modem DSR signal is set within ten seconds, the message TEST COMPLETE is output and the test ends. If the DSR signal is not detected within ten seconds, the following message is output:

```
*** TIMEOUT ERROR!  DSR NOT SET.
```

You can execute the TD verb only on ports that have nonzero RING and DTR bit offsets (indicating that the signals are present on the interface). If you attempt to execute the verb for an illegal environment, one of the following messages is displayed, followed by the VERB? prompt:

```
*** DTR  BIT OFFSET = 0! *** TEST ABORTED!!
*** RING BIT OFFSET = 0! *** TEST ABORTED!!
```

2.2.10 Initialize Test (IT) Verb

After COM90X is loaded, DOCS executes the IT verb automatically to begin initialization. You may execute the IT verb afterwards to reinitialize the original parameters.

2.2.11 Initialize Port (IP) Verb

Use this verb to display or change the parameters of any of the eight ports. The verb displays the following prompt:

ENTER PORT NUMBER: (1=1, 2=2 ETC, F=ALL) DEF=X

Enter the number of the port that you are using. F is not a valid response in this case.

The IP verb uses the same prompts as the manual mode initialization routine. See paragraph 2.1.2 if you need help answering the prompts.

2.3 TEST DESCRIPTIONS

The COM90X test consists of the following tests, which are described in subsequent paragraphs:

Test	Title
1	Timer/interrupt test
2	Data set interface test
3	TMS 9902 communications test
4	TMS 9903 communications test

2.3.1 Test 1 -- Timer/Interrupt Test

Test 1 checks the common internal functions of the TMS 9902 and 9903 that require no external devices or connections, including:

* Basic 990X functioning and proper CRU response (including proper channel separation on CI-402)
* Operation of the 990X interrupt level
* Operation of the interrupt enable and disable functions
* Operation of the interval timer, including:
  - Timer countdown and ability to reset
  - Timer interrupt generation and ability to reset
  - Timer error overrun and ability to reset
  - Timer accuracy in generating consistent intervals
  - Timer accuracy relative to the line frequency (within a range of positive to negative six percent)
  - Timer ranges
* 990X internal test mode

No loopback connector is required to run Test 1.

2.3.2 Test 2 -- Data Set Interface Test

Test 2 verifies that the interface circuitry of the TMS 990X to the external connector is working properly by testing the following functions:

* RTS to CTS and DCD loopback
* Transmit data output to receive data input loopback
* Data set status change interrupt generation
* Half duplex operation is checked when supported by environment
* DTR to DSR loopback
* SRTS to SDCD loopback (or DTR to SDCD)
* Analog loopback to RING loopback (or DTR to RING)
* Off-board communications enable (if available) For a complete test, you must install a loopback connector on the input/output connector of the port being tested. If the selected environment does not have the signal available, the applicable signal test is skipped. In manual mode, the signal test also is skipped if you selected a bit offset of 0 for a signal. (Read paragraph 4.2.)

Other variations of the signals tested depend upon the environment selected. For example, the 990/10A connects DSR or DCD to DSR, depending on a board jumper connection. COM90X automatically adjusts for this condition.

2.3.3 Test 3 -- TMS 9902 Communications Test

Test 3 verifies the basic performance of the TMS 9902 and its associated circuitry by testing the following functions:

* Status signal lines
* Character lengths (5, 6, 7, and 8 bits per character)
* Rate register accuracy and operation
* Transmission rates from 200 to 19,200K bytes, depending on test environment
* Odd, even, or no transmit parity generation for all character patterns
* Data transmission and reception

2.3.4 Test 4 -- TMS 9903 Communications Test

Test 4 verifies the correct operation of the TMS 9903. It also checks the interface of the TMS 9903 to the data set and other support circuitry. The specific functions tested include the following (tested only if they are present in the test environment):

* RTS, CTS, DCD, and analog loopback mode of a TI internal modem
* Character length operation (5, 6, 7, 8, and 9 bits per character) (Mode 0)
* Odd and even transmit parity generation
* Odd and even receive parity reception and error detection
* Asynchronous data transmission (Mode 6)
* Bisynchronous data transmission (Mode 3)
* Bit-oriented data transmission -- SDLC mode (Mode 1)
* CRC generation and detection
* Transmission rate of the baud-rate clock generator relative to the line frequency (only run with digital loopback option). Test 4 may require that you install a loopback connector on the port input/output connector. However, if you are using an external modem, the test runs automatically.

3.1 ERROR MESSAGES

When an error occurs during the execution of COM90X, an error message is output to the error message terminal (provided that you selected the print error option during DOCS initialization). All error messages are output on a new line and are preceded by three asterisks (***). If the system you are testing has a programmer front panel, the corresponding error number is also displayed on the panel lights.

Generally, an error message is output no more than six times when a repetitive test section fails. After this limit is reached, error message output aborts. For example, if up to six errors occur during execution of the 256-character asynchronous data test, the remainder of the test error output is skipped since enough errors have been presented to clearly indicate an error condition. However, the number of errors is continuously incremented to give an accurate error count.

There are two types of error messages: the first type indicates status signal errors and the second type indicates specific failure conditions. The following paragraphs describe these types in detail.

3.1.1 Type 1 Error Messages

Type 1 error messages state that a specific status signal was either missing or was detected when it was not expected. When these errors repeat on an individual port, a malfunctioning data set circuit usually is indicated. When many errors occur, not isolated to one port, an inoperative TMS 990X circuit may be the problem. If there are failures for the signals associated with the data set, it is likely that an EIA driver or receiver between the TMS 990X integrated circuit and the EIA connector has failed.

An example of a type 1 error message is as follows:

```
*** RBRL MISSING OFFSET=NNNN. CRU=NNNN
```

Type 1 error messages contain the following information:

* Name of the tested signal (for example, RBRL)
* Whether an expected signal was not detected (MISSING) or an unexpected signal was detected (UNWANTED)
* Memory location of the tested signal relative to the beginning of the test (OFFSET=NNNN)
* CRU address of the port being tested (CRU=NNNN)

Notice that type 1 errors can originate from anywhere in the test. The only distinction in the error message is the offset number or the specific test header that precedes the error message.

Table 1 lists each tested signal and its function, along with the error number that is output if that signal fails.

Table 1 Type 1 Error Messages

Error Number	Signal Name and Function	
1	RCVERR	- Summary receive error
2	RPER	- Receive parity error
3	ROVER	- Receive overrun
4	RFER	- Receive framing error
5	RFBD	- Receive full bit detect
6	RSBD	- Receive start bit detect
7	RIN	- Receive data input
8	RBINT	- Receive buffer loaded interrupt
9	XBINT	- Transmit buffer loaded interrupt
A	TIMINT	- Timer expired interrupt
B	DSCINT	- Data set signal change interrupt
C	RBRL	- Receive buffer loaded
D	XBRE	- Transmit buffer emptied
E	XSRE	- Transmit shift register emptied
F	TIMERR	- Interval timer error
10	TIMELP	- Interval timer expired
11	RTS	- Request to send (data set signal)
12	DSR	- Data set ready (data set signal)
13	CTS	- Clear to send (data set signal)
14	DSCH	- Data set status change

Table 1 Type 1 Error Messages (Continued)

Error Number	Signal Name and Function
15	FLAG - Any control flag set
16	INT - Summary interrupt
17	DCD - Data carrier detect (data set signal)
18	RING - Ring indicator (data set signal)
19	SDCD - Secondary data carrier detect (data set signal)
1A	DTR - Data terminal ready (data set signal)
1B	ANLB - Analog loopback (data set signal)
1C	SRTS - Secondary request to send (data set signal)
1D	TMS9902 - Presence bit
1E	4MHZCLOCK - Presence bit
1F	HDPLX - Half duplex enable

3.1.2 Type 2 Error Messages

Type 2 error messages are output when specific failure situations occur. The following table describes these messages:

Error Number	Error Message and Description
20	*** CPU DID NOT RECEIVE 990X GENERATED INTERRUPT! COM90X detected (via the CRU status) that the 990X generated an interrupt but the computer did not process it. The computer did not trap through the interrupt vectors. Run the applicable CPU diagnostic test to verify that the interrupt circuits function. Also, check any interrupt jumper options to verify that the 990X interrupt is connected to the CPU. Note that you can bypass the interrupt test, if necessary, using an initialization option. If the CPU test passes, check the CPU interrupt logic or jumpers.
21	*** UNEXPECTED INTERRUPT RECEIVED! The interrupt level assigned to the port under test received an unexpected interrupt. The port should not generate an interrupt. If it receives an interrupt on a level other than the test level, DOCS detects this condition and displays an applicable warning message.

Error Number	Error Message and Description
22	*** INTERVAL TIMER ERROR, TIMER REG=ZZ. The TMS 990X interval timer did not generate a consistent interval period for 50 consecutive tests. The ZZ represents the value of the timer register that failed.
23	*** TIMER ERROR REL TO LINE FREQ. CLOCK = FAST (SLOW) The interval timer accuracy relative to the line frequency is not within a six percent tolerance. This message is also output when the timer is operating properly but the line frequency is in error.
24	*** BAUD RATE ERROR! ZZZ BAUD RATE IS FAST (SLOW) The internal baud rate clock generator relative to the 50 or 60 Hz line frequency is not within a six percent tolerance. This message is also output when the internal clock is accurate but the line frequency is in error.
25	*** TIMER ERROR (TEST MODE TEST) The 990X interval timer did not go 32 times faster in the test mode.
26	*** COB NOT DETECTED!! The communications option board (COB) present bit was not detected when expected.

Error Number	Error Message and Description

27 *** COB 9902 BIT NOT SET!

The 9902 present bit for the communications option board was not detected when expected. To correct the problem, perform the following steps:

* Check that you inserted the correct COB and that you installed the board properly.
* Check that you selected the proper environment during initialization.
* Check that the interconnection cables between boards are fitted properly.
* Check for CRU failure.

28 *** COB 9902 BIT NOT RESET!

The 9902 present bit for the communications option board was detected when not expected. To correct the problem, perform the following steps:

* Check that you inserted the correct COB and that you installed the board properly.
* Check that you selected the proper environment during initialization.
* Check that the interconnection cables between boards are fitted properly.
* Check for CRU failure.

29 *** CHAR LENGTH ERROR! XMIT=XX, RECV=YY.

The TMS 990X is not transmitting or receiving characters of the proper length. The XX represents the character transmitted and YY represents the character received.

Error Number	Error Message and Description
2A	*** RATE ERROR! RATE REG=XXXX. The TMS 9902 internal clock rate generator relative to the 50 or 60 Hz line frequency is not within the six percent tolerance. This error message also is generated when the internal clock rate generator is accurate but there is a line frequency error exceeding the six percent tolerance. The XXXX represents the rate register value.
2B	*** EVEN PARITY ERROR! XMIT CHAR=XX. The TMS 990X is not generating the proper even parity on transmission. The XX refers to the transmitted character with the wrong parity.
2C	*** ODD PARITY ERROR! XMIT CHAR=XX. The TMS 9902 did not generate the proper odd parity on transmission. The XX refers to the transmitted character with the wrong parity.
2D	*** DATA ERROR! XMIT=XX, RECV=YY. The received data did not agree with the transmitted data. The XX represents the data transmitted and YY represents the data received.
2E	*** STATUS ERROR! A receive status error was detected (parity, overrun, or framing).
2F	*** RECEIVE TIME OUT ERROR! No synchronous characters were received. This is normally due to an open connection in the external loopback or data set signal path. It may also indicate missing external synchronizing clocks.

Error Number	Error Message and Description
31	*** CRC COMPARE ERROR BY CHIP RCRC GEN! The TMS 9903 Receive CRC generator did not generate the correct cyclic redundancy check character.
32	*** CRC COMPARE ERROR BY CHIP XCRC GEN! The TMS 9903 Transmit CRC generator did not generate the correct cyclic redundancy check character.
33	*** CRC COMPARE ERROR IN RECV DATA! The received CRC character did not equal the transmitted cyclic redundancy check character. The TMS 9903 is designed to transmit and receive SDLC frames in internal or external loopback mode.
34	*** NO 9903 INSTALLED! The TMS 9903 status is equivalent to an empty socket.
35	*** CHANNEL ADDRESS ERROR, CHANNEL X ACCESSED BY WRITE TO CHANNEL Y. Channel X expected to read X but received Y. If Y=0 or >F, then the channel failed to read any character.

3.2 ERROR ANALYSIS

Since the primary devices under test are the TMS 9902 and TMS 9903 multifunction integrated circuits, it is common for a circuit to either pass the test with no errors or fail most of the tests. Therefore, if the test logs only a few errors, the loopback circuitry (as well as the test port circuits) may be faulty.

Other possible error causes are as follows:

* The external loopback connection is missing. If you are running in external mode, the test will generate a lengthy error listing because of the missing connector.

* A data set driver or receiver is faulty (that is, the problem is not with the 99OX but with the interface circuits). The test will generate intermittent data errors only in external mode.

* The loop-back function is faulty. If the same signal is missing repeatedly, move the loop-back function to another port. If the same error occurs at the new port, you can attribute it to the loopback function.

* The data set interface circuitry is faulty. If an error occurs repeatedly for a specific signal, it is likely that the data set interface circuitry is faulty, rather than the TMS 99OX integrated circuit.

* The line frequency is outside the normal value. Tests that use the CPU line frequency as the master timing source may indicate errors if the tested unit is operating properly but the time frequency is outside the test tolerance limits. Verify the line frequency accuracy if erratic timing test errors occur.

* The 99OX chip or its associated circuitry is probably faulty if errors occur intermittantly.

4.1 SUPPLEMENTAL INFORMATION

The paragraphs in this section contain the following:

* Tables of the environmental parameters for each equipment configuration
* Information about the communications port connectors
* Information about the channel loopback connector

4.2 ENVIRONMENTAL PARAMETERS LIST

The following tables list the specific parameters used when testing for the 990/5, 990/10A, S200/S300/S300A COB, and CI-402 environments.

Table 2 Parameters for 990/5 and 990/10A Environments

Parameter	990/5 CPU P1	990/5 CPU P2	990/5 CPU P3	990/10A CPU
Port Number	1	2	3	1
Comm IC Type	9902	9902	9903	9902
Chip CRU Address	1700	1740	1780	1700
Port CRU Address	1780	1780	1780	1700
9901 CRU Address	NA	NA	NA	NA
Interrupt Level	8	E	6	8#1
Interrupt Enable Bit	24	25	26	26
External Communications Enable Bit	27	27	27	27
External Clock Generator	No	No	Yes	No
Prog DTR Bit	Fixed	Fixed	20	20
Prog Analog Loopback	0	0	21	21
Half Duplex Enable	0	0	0	0
Program Secondary RTS Bit	0	0	22	0
Modem DCD signal	0	0	20	#2
Modem RING signal	0	0	21	21
Modem Secondary DCD signal	0	0	22	No
Connector Type	DB25	DB25	DB25	FCC
Clock Frequency	4.0	4.0	4.0	2.5
Line Frequency	Both	Both	Both	Both

Notes:

1. NA means not applicable.

2. All table entries are in hexadecimal except those entries for Comm IC Type, Connector Type, and Clock Frequency.

3. Chip CRU address is the CRU base address of the test communications chip.

4. Port CRU address refers to the added circuitry that controls port operations other than those the chip provides (for example, interrupt enable, external communications enable, or DTR).

5. For the 990/10A, DCD can replace DSR via a jumper connection. Thus, in loopback mode, DTR -> DSR or RTS -> DSR.

Table 3 Parameters for S200/300/300A COB Environment

Parameter	2-Channel P1	2-Channel P2	4-Channel P3	4-Channel P4	4-Channel P5	4-Channel P6
Port Number	1	2	3	4	5	6
Comm IC Type	9903	9902	9902	9902	9902	9902
Chip CRU Address	0B00	0B80	0400	0480	0500	0580
Port CRU Address	0B00	0B80	0400	0480	0500	0580
9901 CRU Address	1F80	1F80	NA	NA	NA	NA
Interrupt Level	5/3	6/4	B/6	B/7	B/A	B/C
Interrupt Enable Bit	26	26	26	26	26	26
External Communications Enable Bit	27	27	27	27	27	27
External Clock Generator	Yes	No	No	No	No	No
Prog DTR Bit	20	20	20	20	20	20
Prog Analog Loopback	0	0	0	0	0	0
Half Duplex Enable	0	0	25	25	25	25
Prog Secondary RTS Bit	22	22	0	0	0	0
Modem DCD Signal	20	20	20	20	20	20
Modem RING Signal	21	21	21	21	21	21
Modem Secondary DCD Signal	22	22	22	22	22	22
Connector Type	DB25	DB25	DB25	DB25	DB25	DB25
Clock Frequency	See CPU		See CPU		See CPU	
Line Frequency	None	None	None	None	None	None

Notes:

1. NA means not applicable.

2. All table entries are in hexadecimal except those entries for Comm IC Type, Connector Type, and Clock Frequency.

3. Chip CRU address is the CRU base address of the test communications chip.

4. Port CRU address refers to the added circuitry that controls port operations other than those the chip provides (for example, interrupt enable, external communications enable, or DTR).

5. When reading the interrupt level entries for the S200, S300, and S300A COB, the first number is for the S200 and the second is for the S300/300A.

6. For the CI-421 and CI-422, the loopback plug uses DTR to DRIVE RING.

Table 4 Parameters for CI-402 Environment

Parameter	P1	P2
Port Number	1	2
Comm IC Type	9902	9902
Chip CRU Address	0800	0880
Port CRU Address	0800	0880
9901 CRU Address	NA	NA
Interrupt Level	See CPU	See CPU
Interrupt Enable Bit	26	26
External Communications Enable Bit	27	27
External Clock Generator	No	No
Prog DTR Bit	20	20
Prog Analog Loopback	21	21
Half Duplex Enable	25	25
Prog Secondary RTS Bit	22	22
Modem DCD Signal	20	20
Modem RING Signal	21	21
Modem Secondary DCD Signal	22	22
Connector Type	FCC	FCC
Clock Frequency	4.0	4.0
Line Frequency	Both	Both

Notes:

1. NA means not applicable.

2. All table entries are in hexadecimal except those entries for Comm IC Type, Connector Type, and Clock Frequency.

3. Chip CRU address is the CRU base address of the test communications chip.

4. Port CRU address refers to the added circuitry that controls port operations other than those the chip provides (for example, interrupt enable, external communications enable, or DTR).

5. CI-402 can be set for CRU address in the range of >0800 through >1B00, and uses the interrupt assigned to the P1 side of the chassis in which it resides.

4.3 COMMUNICATIONS PORT CONNECTIONS

Table 5 gives the pin connections for the 990/5 and 990/10A environments involved. A number instead of a Y or dash indicates that the signal is present on a pin number different from the standard RS-232 definition. The 990/10A entries are the pin numbers for the 18-pin EMI connector.

Table 5 Pin Connections for 990/5 and 990/10A Environments

DB25 Pin	Signal Name	990/5 P1	990/5 P2	990/5 P3	990/10A
1	PROTECT GND	-	-	-	-
2	XMIT DATA	Y	Y	Y	1
3	RECV DATA	Y	Y	Y	2
4	REQ TO SEND	Y	Y	Y	3
5	CLR TO SEND	Y	Y	Y	4
6	DATA SET RDY	Y	Y	Y	5#2
7	SIGNAL GND	Y	Y	Y	16
8	DATA CAR DET	-	-	Y	6
9	POS TEST V	-	-	-	-
10	NEG TEST V	-	-	-	-
11	SEC RTS	-	-	Y	-
12	SEC DCD	-	-	Y	-
13	ANALOG LUPBK	-	-	Y	15
14	SEC XDATA	-	-	-	-
15	XMT CLOCK	-	-	Y	-
16	SEC RDATA	-	-	-	-
17	RCV CLOCK	-	-	Y	-
18		-	-	-	-
19	SEC RTS	-	-	Y	-
20	DATA TER RDY	Y#1	Y#1	Y	12
21	SIG QUAL DET	-	-	-	-
22	RING	-	-	Y	13
23	DATA RATE SL	-	-	-	-
24	EXT XCLOCK	-	-	Y	-
25	BUSY	-	-	-	-

Notes:

1. The 990/5 P1 and P2 DTR signals are nonprogrammable (derived from +12V).

2. The DSR signal to the 990/10A TMS 9902 is jumper selectable to be either DSR or DCD modem signals.

Table 6 gives the pin connections for the S200/S300/S300A environment involved. A number instead of a Y or dash indicates that the signal is present on a pin number different from the standard RS-232 definition.

Table 6 Pin Connections for S200/S300/S300A Environment

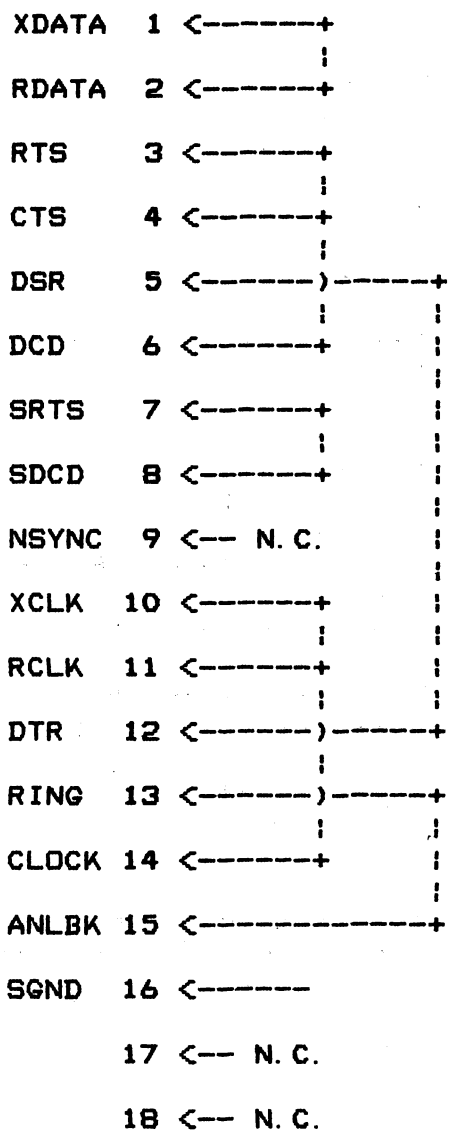
DB25 Pin	Signal Name	S200/S300 P1	P2	P3	P4	P5	P6
1	PROTECT GND	Y	Y	Y	Y	Y	Y
2	XMIT DATA	Y	Y	Y	Y	Y	Y
3	RECV DATA	Y	Y	Y	Y	Y	Y
4	REQ TO SEND	Y	Y	Y	Y	Y	Y
5	CLR TO SEND	Y	Y	Y	Y	Y	Y
6	DATA SET RDY	Y	Y	Y	Y	Y	Y
7	SIGNAL GND	Y	Y	Y	Y	Y	Y
8	DATA CAR DET	Y	Y	Y	Y	Y	Y
9	POS TEST V	-	-	-	-	-	-
10	NEG TEST V	-	-	-	-	-	-
11	SEC RTS	Y	Y	-	-	-	-
12	SEC DCD	Y	Y	Y	Y	Y	Y
13	ANALOG LUPBK	-	-	-	-	-	-
14	SEC XDATA	-	-	-	-	-	-
15	XMT CLOCK	Y	Y	Y	Y	Y	Y
16	SEC RDATA	-	-	-	-	-	-
17	RCV CLOCK	Y	Y	Y	Y	Y	Y
18		-	-	-	-	-	-
19	SEC RTS	-	-	-	-	-	-
20	DATA TER RDY	Y	Y	Y	Y	Y	Y
21	SIG QUAL DET	-	-	-	-	-	-
22	RING	Y	Y	Y	Y	Y	Y
23	DATA RATE SL	-	-	-	-	-	-
24	EXT XCLOCK	Y	Y	Y	Y	Y	Y
25	BUSY	-	-	-	-	-	-

Note:

On Business System computers, ports 1 and 2 correspond to 940 ports 1 and 3. Ports 3 through 6 are taken off a pigtail cable assembly that plugs into the 4-channel interface board.

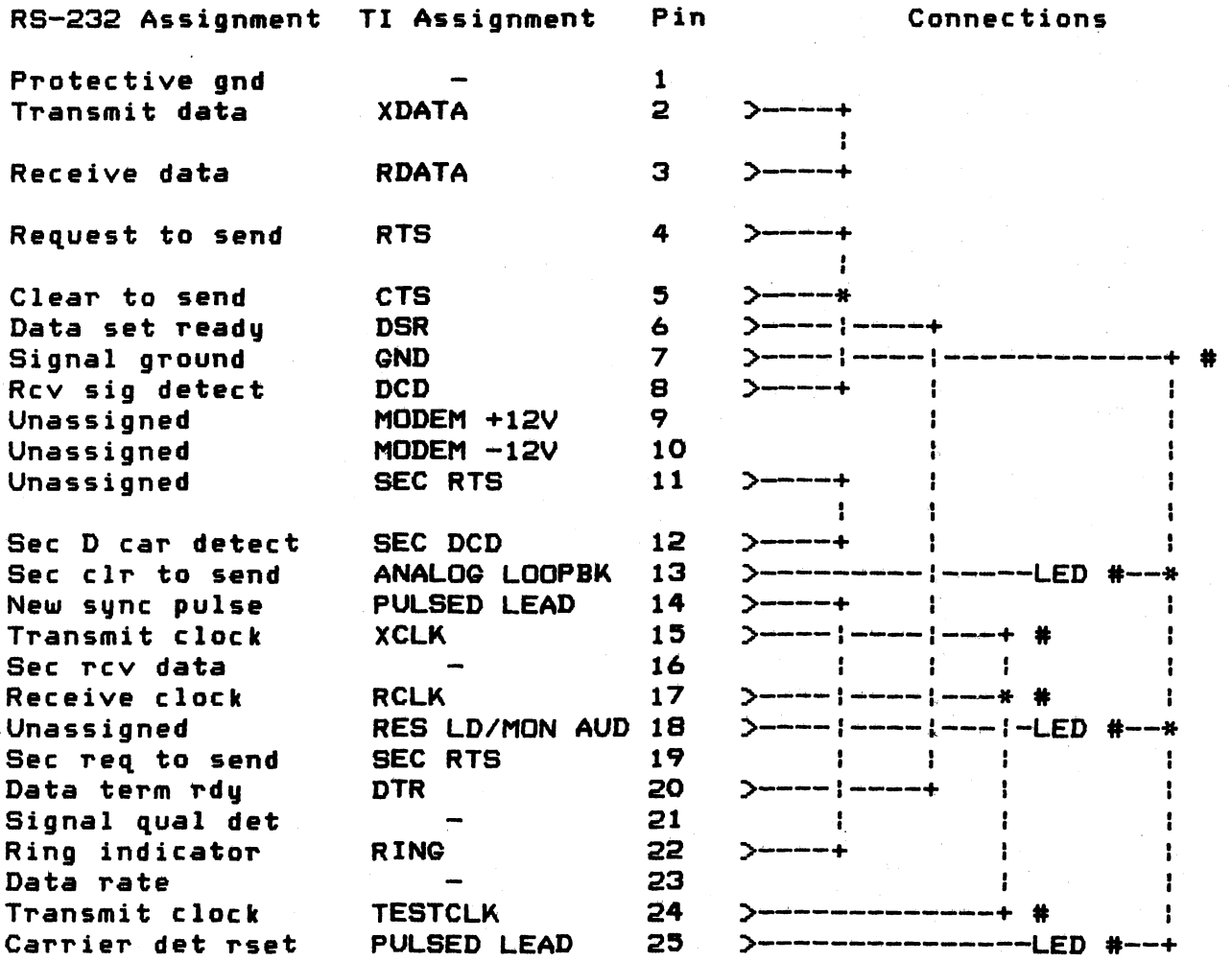
4.4 EIGHTEEN-PIN CHANNEL LOOPBACK CONNECTOR

The following diagram shows the loopback connector (part number 2303065-0001) that the 18-pin female FCC-EMI communications interface uses:



4.5 TWENTY-FIVE-PIN LOOPBACK CONNECTOR

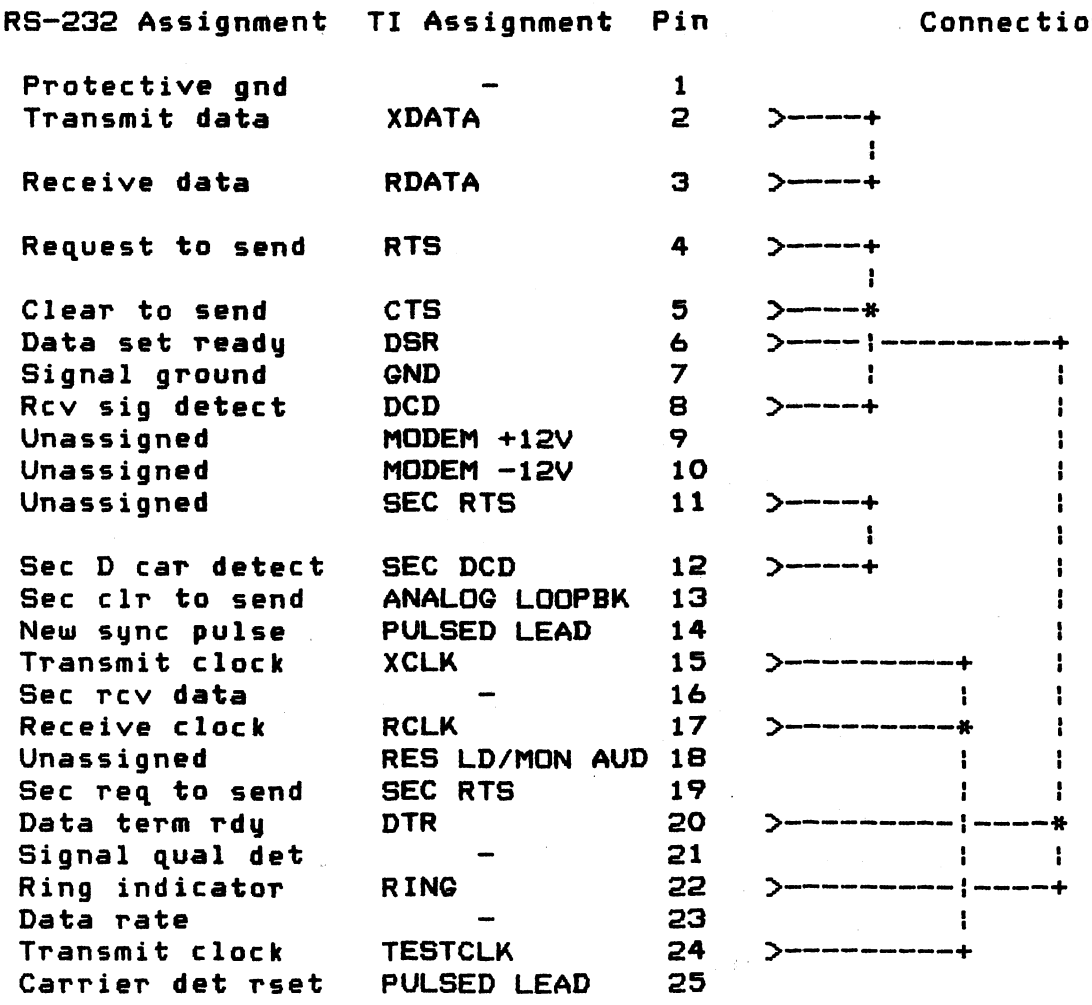
The following diagram shows the loopback connector (part number 948550-0001) that the 25-pin female RS-232C communications interface uses.



* Indicates a connection.
\# Indicates revision *C only.

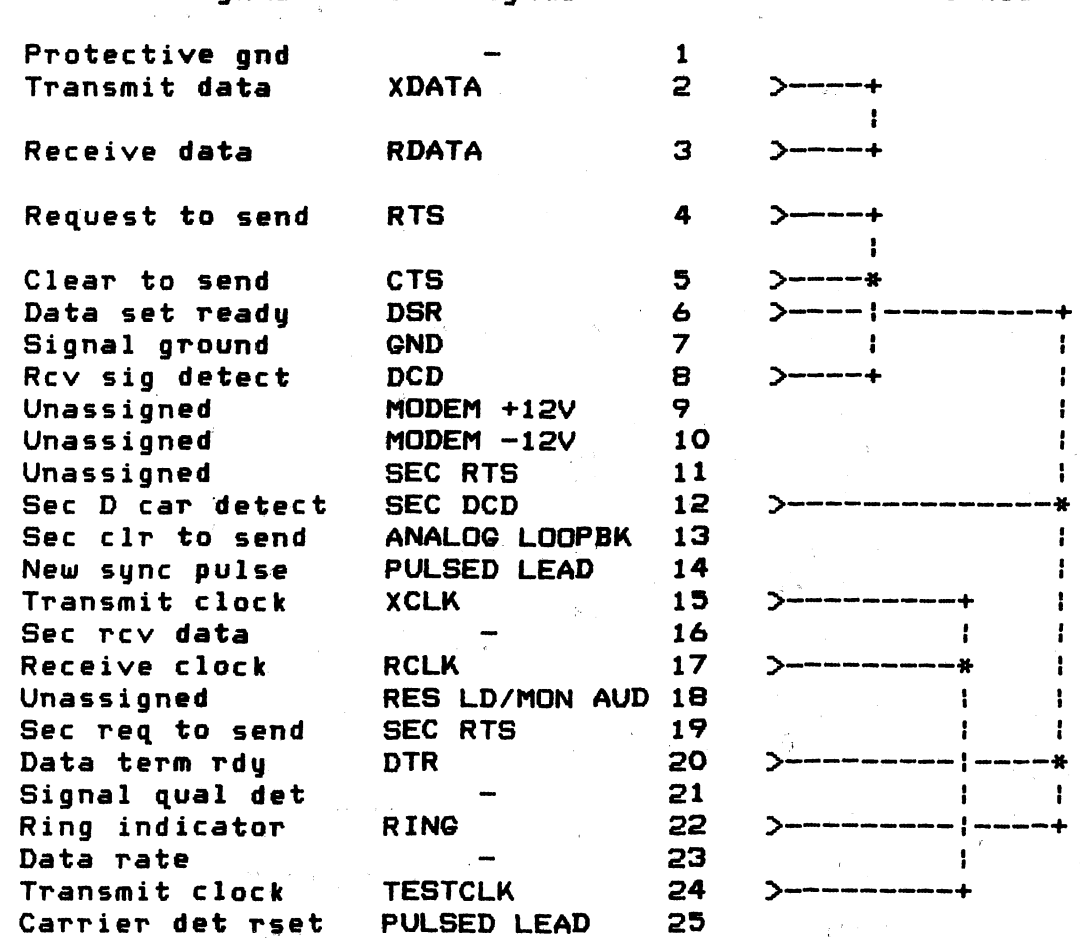
4.6 TWENTY-FIVE-PIN LOOPBACK CONNECTOR FOR THE TWO-CHANNEL COB

The following diagram shows the loopback connector (part number 2230510-0001) utilized with the 25-pin female RS-232C communications interface for the 2-channel communications option board.



4.7 TWENTY-FIVE-PIN LOOPBACK CONNECTOR FOR THE FOUR-CHANNEL COB

The following diagram shows the loopback connector (part number 2532884-0001) utilized with the 25-pin female RS-232C communications interface for the 4-channel communications option board.



CRCOMM

COMMUNICATIONS INTERFACE MODULE TEST

COMMUNICATIONS INTERFACE MODULE TEST (CRCOMM)

CRCOMM

Communications Interface Module Test

1.1 INTRODUCTION

The Communications Interface Module Test (CRCOMM) verifies the correct operation of the communications interface module (CIM) and diagnoses fault conditions detected on the CIM.

1.2 TEST REQUIREMENTS

The following equipment is required to operate the CRCOMM test:

* A Model 990 Computer with a minimum of 24K bytes of memory
* A communications interface module (part number 946105) with either the standard interface or the 2741 interface
* A loopback test connector (part number 948550-0001) or modem. (Both of these devices are optional; however, you must use one of them in order to execute the entire test.)
* An interactive terminal
* A device to load the test program

1.3 TEST CHARACTERISTICS

The CRCOMM test has certain characteristics that you should know before operating the test:

* CRCOMM operates under the control of DOCS. Information about DOCS operation can be found in Volume 1 of this handbook.
* CRCOMM runs in either internal or one of three external test modes. The test is in an external mode when either a loopback connector or a modem is installed and runs in

internal mode when neither of these devices is present. Certain tests are not executable in internal mode.

* CRCOMM consists of 22 tests and is structured so that you can run either the complete set of tests or any separate test. These tests are as follows:

Test	Title
1	Internal RSVOUT, MODE Test
2	Internal SRTS, SDCD, and NSF Test
3	Internal Timer Test
4	Internal ID Switch Test
5	Internal Interrupt Test
6	Internal Word 2 and 3 Pattern Test
7	Internal Word 2 and 3 Checkerboard Test
8	Internal NEW SYNC, RING Test
9	External NEW SYNC/RING, and Light Blink Test
A	External DTR, DSR, and NSF Test
B	External RTS, CTS, and DCD Test
C	External SRTS and SDCD Test
D	Internal WRQ Test
E	Internal HDX RRQ Mask Test
F	Internal Break, Parity, and Framing Error Test
10	Internal Baud Rate Test
11	Internal SYNC OVERRUN Test
12	Internal SYNC UNDERRUN and DLE/SYNC Fill Test
13	Internal Synchronous Data Test
14	External Asynchronous Data Test
15	External Synchronous Data Test
16	Internal Synchronous Strip Test

* CRCOMM uses a number of test verbs, or commands, to execute various tests and functions. Some of these verbs execute individual tests one time or continuously. Others have utility functions that help isolate hardware faults in tests that have detected errors. The CRCOMM test verbs are as follows:

Verb	Function
IT	Initialize test
EA	Execute all tests one time
ET	Execute an individual test one time
LT	Loop continuously on an individual test
LA	Loop continuously on all tests
DL	Data loopback
DS	Display the CIM status
ML	Monitor line
PE	Print error count
RM	Read modem interface
RS	Reset CIM

Verb	Function
RT	Remote test
SP	Select pattern (used by test 6)
TD	Test DAA
TM	Transmit message

2.1 TEST EXECUTION

The CRCOMM module must be loaded and initialized by DOCS before execution can begin.

NOTE

In order to run CRCOMM with the latest version of the loopback connector, the jumper near location U51 must connect E0 and E2. Before the CIM assembly is returned to normal service with an external modem, the jumper must connect E1 and E2. The jumper is only changed for new loopback connector tests.

2.2 LOADING

The loading procedure is explained in Section 3 of Volume 1.

2.3 INITIALIZATION

When DOCS loads the test module, it outputs the name and version of the test:

CRCOMM - COMM INTERFACE MODULE DIAGNOSTIC VERSION=XX : MM/YY

Then DOCS executes the initialize test (IT) verb by asking you the following questions. If the default value shown with each question is correct, press the RETURN key. If not, enter the correct value.

ENTER CRU BASE ADDRESS: DEF=0040 -

The CRU base address is the identification number of the chassis slot where the communications interface module is installed.

ENTER INTERRUPT LEVEL: DEF=4 -

Enter any value between 3 and >F for the interrupt level. This is determined by the back panel wiring.

```
ENTER ID SWITCH VALUE: DEF=00 -
```

Enter any value between 00 and >7F for the ID switch value.

```
ENTER COMPUTER LINE FREQ: (0=50, 1=60) DEF=1 -
```

Indicate the line frequency of the computer by either pressing RETURN or entering a 0.

```
INTERNAL OR EXTERNAL TEST: (0=INT, 1=EXT) DEF=1 -
```

Select the internal test mode (0) if no loopback connector or modem is installed. If you are using one of these devices, enter a 1. DOCS then outputs the following question:

```
EXT LOOPBACK TYPE? (DI=DIGITAL, AL=ANALOG, FE=FAR END)
DEF = DI -
```

The loopback type or mode that you select depends upon the system configuration or the part of the system that you want to test. Refer to the following table to determine the appropriate loopback mode and to Appendix B for an illustration of the portions of the system that are tested in each mode.

Test Mode	Loopback Connector	Modem	Comm Line
DI - Digital Loopback	Yes	No	No
AL - Analog Loopback	No	Yes(TI)	No
FE - Far End Loopback	No	Yes	Yes

If you determine that the loopback type is digital (DI), DOCS responds with the following question:

```
DOES LOOPBACK CONNECTOR HAVE LITES, IE REV C OR HIGHER?
(0=NO, 1=YES) DEF=1 -
```

Press RETURN if the loopback connector has lights; otherwise enter a 0.

If you indicate that the loopback type is analog (AL), DOCS asks the following question:

```
TI INTERNAL MODEM? (0=NO, 1=YES) DEF=0 -
```

If you enter a 0, indicating that no TI modem is present, DOCS outputs a reminder that the modem should be in the test loopback condition:

```
MODEM AL SWITCH ON? (0=NO, 1=YES) -
```

You must answer this question with a 1.

If you indicate that the loopback type is far end (FE), DOCS reminds you that the far end must be in loopback mode:

```
FAR END IN REMOTE LOOPBACK? (0=NO, 1=YES) -
```

You must answer this question with a 1.

DOCS asks the following questions if either internal or any of the external modes are selected:

```
ASYNCHRONOUS OR SYNCHRONOUS MODE? (0=ASYNC, 1=SYNC)
DEF=1 -

ENTER SYNC CHAR IN HEX: (DEF=16) -
```

The final initialization question reminds you that the clock jumper must be changed to provide the external clock:

```
DOES CLOCK JUMPER CONNECT E0 &E2 (0=NO, 1=YES) DEF=0 -
```

When you have answered the initialization questions, DOCS asks if you want to execute the entire CRCOMM test:

```
EXECUTE EA VERB? (DEF=1) -
```

If you press RETURN, all parts of CRCOMM that may be run in the test mode that you have selected are executed one time. If the EA verb executes without errors, you may assume that the CIM is operating correctly and that no further testing is necessary. Should errors occur, run the test or tests indicating errors and use any of the appropriate utility verbs to determine their cause. The following messages are output when the EA verb executes the entire CRCOMM test without errors:

```
.START TEST 01: INT RSVOUT, MODE TEST COMPLETED.
.START TEST 02: INT SRTS, SDCD, NSF, INTSUM TEST COMPLETED.
.START TEST 03: INT TIMER TEST COMPLETED.
```

```
.START TEST 04:  INT ID SWITCH TEST COMPLETED.
.START TEST 05:  INT INTERRUPT TEST COMPLETED.
.START TEST 06:  INT WORD 2 & 3 PATTERN TEST COMPLETED.
.START TEST 07:  INT WORD 2 & 3 CHECKERBOARD TEST COMPLETED.
.START TEST 08:  INT NEW SYNC, RING TEST COMPLETED.
.START TEST 09:  EXT NEW SYNC, RING, LITE BLINK TEST COMPLETED.
.START TEST 0A:  EXT DTR, DSR, NSF TEST COMPLETED.
.START TEST 0B:  EXT RTS, CTS, DCD TEST COMPLETED.
.START TEST 0C:  EXT SRTS, SDCD TEST COMPLETED.
.START TEST 0D:  INT WRQ TEST COMPLETED
.START TEST 0E:  EXT HDX RRQ MASK TEST COMPLETED.
.START TEST 0F:  EXT BREAK, PARITY & FRAMING ERROR TEST COMPLETED
.START TEST 10:  INT BAUD RATE TEST COMPLETED.
.START TEST 11:  INT SYNC OVERRUN TEST COMPLETED.
.START TEST 12:  INT SYNC UNDERRUN & DLE/SYNC FILL TEST COMPLETED
.START TEST 13:  INT SYNC DATA TEST COMPLETED.
.START TEST 14:  EXT ASYNC DATA TEST COMPLETED.
.START TEST 15:  EXT SYNC DATA TEST COMPLETED.
.START TEST 16:  INT SYNC STRIP TEST COMPLETED.
ALL EA TEST COMPLETED.  ERRORS = 0000.
```

If you respond with a 0 (no) to the question EXECUTE EA VERB?, DOCS outputs the following question:

```
VERB? -
```

You may then execute any DOCS or CRCOMM test verb. If you later want to alter any of the initialization parameters, reexecute the IT verb.

2.4 TEST VERBS

When DOCS outputs the question VERB?, you may enter any of the CRCOMM test verbs, which are discussed in the following paragraphs. To receive the question VERB?, press the @, CMD, HELP, or ESC key.

2.4.1 ET Verb

The ET verb executes an individual test one time. When you enter this verb, the test outputs the following information. You must indicate which test you want to run:

```
TEST NUMBER? -

START TEST NN:

TEST COMPLETE (or) TEST SKIPPED
```

The message TEST SKIPPED is output if the test environment does not permit execution of the chosen test. If you enter an invalid number, the following message is output:

*** TEST NOT AVAILABLE ***

2.4.2 LT Verb

The LT verb causes the specified test to execute continuously, or loop. When you enter this verb, the test outputs the following information. You must indicate which test you want to run.

TEST NUMBER? -

START TEST NN:

TEST COMPLETE (or) TEST SKIPPED

The LT verb output the message TEST SKIPPED if the test you choose cannot be executed in the test environment. It outputs the following message if you enter an invalid number:

*** TEST NOT AVAILABLE ***

The test continues to loop until you press the @, CMD, HELP, or ESC key. The loop count, or number of times the test has executed, is output to both the interactive terminal and the computer front panel. The fault light illuminates if any errors occur.

2.4.3 LA Verb

The LA verb causes the continuous execution of the entire CRCOMM test. (Some tests may be omitted, depending on the test environment.) The loop and error counts are continuously displayed on the computer front panel and are output to the interactive terminal at the end of each execution of the verb. To halt execution of the LA verb, press the @, CMD, HELP, or ESC key.

2.4.4 DL Verb

The DL verb performs a data loopback test on the CIM. (The CIM is initialized to operate in a seven-bit-data-plus-odd-parity format.) The verb sends a preamble of synchronizing characters followed by the continuous transmission and reception of a single character that you specify. When you execute the DL verb, the following instructions are output:

```
ENTER TRANSMIT DATA IN HEX: -
```

Enter the hexadecimal code character of an ASCII character from 00 through >7F (for example, 0 for 30 and A for 41). Refer to Appendix A for a table cross-referencing the ASCII characters with their corresponding hexadecimal code numbers. When you have entered the hexadecimal code character, the DL verb outputs the following message:

```
** DATA LOOPBACK ACTIVE
```

The verb transmits a preamble of eight synchronizing characters and then continuously transmits the character that you entered. The CIM is monitored to verify that the same character is being received. The character is displayed in the two left-hand sets of lights on the computer front panel, while the number of characters transmitted is displayed in the two right-hand sets of lights. If a data error occurs, the fault light on the front panel illuminates and the verb outputs the following message, with XX representing the erroneous character that was received:

```
*** DATA TRANSFER ERROR! XX
```

2.4.5 DS Verb

The DS verb outputs the status of the CIM in the following format:

```
CIM STATUS: IW0 = AAAA. IW1 = BBBB. IW2 = CC. IW3 = DD.
```

AAAA, BBBB, CC, and DD are the status words as read from the CIM. Consult the Communications Systems Installation and Operation Manual for the computer input bit assignments.

2.4.6 ML Verb

The ML verb monitors the receive line for 20-character header and trailer data patterns that you define. All data received between these headers is displayed. When you execute this verb, it outputs the following question:

```
USE LAST INPUTS? (0 = NO, 1 = YES)
```

If the test has been run before, you can use the same set of header and trailer data entered during the previous execution by answering this question with a 1. If the test is being run for

the first time, the header and trailer data patterns must be created, and you should answer this question with a 0. The verb then outputs the following instructions:

```
ENTER UP TO 20 SETS OF 2 DIGIT HEX NUMBERS (00-7F).
THESE REPRESENT THE ASCII CHARACTERS. (EX: 34 = "4", 41
= "A", ETC.). END THE INPUT BY ENTERING HEX FF.
```

Enter the header data in ten groups of four characters each, for example:

```
ENTER HEADER:

-1122   -3344   -5566     etc.
```

The header entry is terminated when you have entered 40 characters (representing 20 ASCII characters) or when you enter the hexadecimal number FF. This data is echoed back to you so that you can verify the input, for example:

```
** ACCEPTED = 11+22+33+44+55+66+   etc.
```

The + sign following each header pair signifies that the pair is part of the header text.

Then you are instructed to define the trailer data in the same manner. For example:

```
ENTER TRAILER:

    -1234   -5678   -007F   etc.
```

The data is echoed back to you in the same way as the header data, except that a - sign follows each trailer pair to signify that the data is part of the trailer text:

```
ACCEPTED = 12-34-56-78-00-7F-   etc.

** ENABLED.
```

The ENABLED message indicates that the monitor line function is active and that the search of the receive data stream is in progress. The following is an example of a typical message display:

```
** ENABLED.

40+40+48 49 20 54 48 45 52 45 21 41-41-
```

2.4.7 PE Verb

The PE verb outputs the current error count in the following format:

```
ERRORS = XXXX
```

2.4.8 RS Verb

The RS verb causes the CIM to reset.

2.4.9 RM Verb

The RM verb reads the status of the CIM and displays the status of the modem interface signals available in the following message (the Xs indicate that the signal is true):

RTS	CTS	DSR	DCD	SDCD	DTR	RING
	X			X		

2.4.10 RT Verb

The RT verb places the local interface in remote test mode. This means that signals coming into the CIM from a remote location are echoed back to that location. (Refer to the Communications Interface Module Operation and Maintenance Manual for a description of the signals involved.) When the remote test function has been activated, the verb outputs the following information:

```
** ENABLED
```

2.4.11 SP Verb

The SP verb allows you to select the pattern used by test 6. The messages output by this verb are as follows:

```
SELECT TEST 6 PATTERN:

PAT1 = 00  -

PAT2 = FF  -
```

You may change the patterns by entering new values. If you want to accept the displayed defaults, press the RETURN key.

2.4.12 TD Verb

The TD verb monitors the incoming RING signal for a set condition, indicating that an incoming call has been detected. During this monitoring period, a message is output every 10 seconds to notify you that the test is active:

```
..TEST DAA

..WAITING FOR RING SIGNAL FROM MODEM..
```

When the RING signal has been received, the DTR modem lead is then set, causing an answer-back tone to be transmitted on the communications line. When this occurs, the following message is output:

```
** RING RECEIVED!  DTR NOW SET.

BEGIN 10 SEC WAIT FOR DSR
```

If the modem DSR signal goes active within 10 seconds, the message TEST COMPLETED is output and execution of the verb ends. If DSR is not detected within 10 seconds, the following message is output:

```
*** TIMEOUT ERROR! DSR NOT SET.
```

2.4.13 TM Verb

The TM verb continuously transmits a 20-ASCII-character data pattern that you specify. (This message is transmitted in seven-bit-plus-odd-parity format.) When you execute this verb, it outputs the following instruction:

```
..TRANSMIT MESSAGE :

USE LAST INPUTS? (0 = NO, 1 = YES)
```

If the test has been run before, you can use the same data pattern entered during the previous execution by answering this question with a 1. If the test is being run for the first time, the data

pattern must be created, and you should answer this question with a 0. The verb then outputs the following instructions:

```
ENTER UP TO 20 SETS OF 2 DIGIT HEX NUMBERS (00-7F).
THESE REPRESENT THE ASCII CHARACTERS. (EX: 34 = "4", 41
= "A", ETC.). END THE INPUT BY ENTERING HEX FF.
```

Enter the data, using the table in paragraph 2.4.5 to determine the correct hexadecimal code characters. End the input by entering the characters FF. The TM verb then echoes the pattern back to you so that you can verify the input. Then the test pauses and outputs the following message:

```
START TRANSMIT MESSAGE? (0=N, 1=Y) -
```

You may then either terminate the test (0) or start the continuous tranmission of the data pattern (1).

2.5 TEST DESCRIPTIONS

The CRCOMM test consists of 22 tests, which are listed in the following table along with the four test modes. A Y in a test mode column indicates that the test is executed in that mode; an N indicates that the test is skipped. (Refer to paragraph 2.3 for a guide to selecting the test mode.)

Test	Title	Internal Mode	External Modes DI	AL	FE
1	Internal RSVOUT, MODE Test	Y	Y	Y	Y
2	Internal SRTS, SDCD, and NSF Test	Y	Y	Y	Y
3	Internal Timer Test	Y	Y	Y	Y
4	Internal ID Switch Test	Y	Y	Y	Y
5	Internal Interrupt Test	Y	Y	Y	Y
6	Internal Word 2 and 3 Pattern Test	Y	Y	Y	Y
7	Internal Word 2 and 3 Checkerboard Test	Y	Y	Y	Y
8	Internal NEW SYNC, RING Test	Y	Y	Y	Y
9	External NEW SYNC/RING and Light Blink Test	N	Y	N	N
A	External DTR, DSR, and NSF Test	Y	Y	N	N
B	External RTS, CTS, and DCD Test	Y	Y	N	N
C	External SRTS and SDCD Test	Y	Y	N	N
D	Internal WRQ Test	Y	Y	Y	Y
E	Internal HDX RRQ Mask Test	N	Y	N	N
F	Internal Break, Parity, and Framing Error Test	Y	Y	N	N
10	Internal Baud Rate Test	Y	Y	Y	Y
11	Internal SYNC OVERRUN Test	Y	Y	Y	Y

Test	Title	Internal Mode	External Modes DI	AL	FE
12	Internal SYNC UNDERRUN and DLE SYNC/Fill Test	Y	Y	Y	Y
13	Internal Synchronous Data Test	Y	Y	Y	Y
14	External Asynchronous Data Test	Y	Y	Y	Y
15	External Synchronous Data Test	Y	Y	Y	Y
16	Internal Synchronous Strip Test	Y	Y	Y	Y

NOTE

Some tests are performed several times, but if a test fails, any remaining loops are bypassed and the next test is executed. This eliminates multiple output of the same error message.

2.5.1 Test 1 -- Internal RSVOUT, MODE Test

Test 1 toggles RES MODEM LD OUT (output word 4, bit 3) and SYNC MODE (output word 3, bit 5) and tests the corresponding input bits for agreement.

2.5.2 Test 2 -- Internal SRTS, SDCD, and NSF Test

Test 2 sets DTR and then toggles SRTS to determine if SDCD toggles in agreement. Then it verifies that NSF (new status flag) and INTSUM set and clear properly.

2.5.3 Test 3 -- Internal Timer Test

Test 3 verifies that the 250-millisecond timer (TIMEXP) sets and clears properly and that the timing is within a plus-or-minus 15 percent tolerance. It also checks INTSUM for proper setting and clearing.

2.5.4 Test 4 -- Internal ID Switch Test

Test 4 reads the ID switches on the CIM. If the ID switches are set to a value that is different from the values entered during test initialization, the test outputs an error message indicating the ID switch value that it reads.

2.5.5 Test 5 -- Internal Interrupt Test

Test 5 verifies that the interrupt logic interrupts the CPU only when it is enabled.

2.5.6 Test 6 -- Internal Word 2 and 3 Pattern Test

Test 6 writes a pattern of zeros (pattern 1) to OUTPUT WORDS 2 and 3, strobing each to the ASTRO. It reads the ASTRO registers to verify correct operation. The test then writes a pattern of >FF (pattern 2) and repeats the process. You may change the patterns by executing the select pattern (SP) verb.

2.5.7 Test 7 -- Internal Word 2 and 3 Checkerboard Test

Test 7 writes a walking 1 pattern to OUTPUT WORDS 2 and 3, strobing each to the ASTRO. The ASTRO registers are then read back through the interface to verify correct operation. Then the test writes a walking 0 pattern and repeats until a 1 and a 0 have been moved through all eight bit positions.

2.5.8 Test 8 -- Internal NEW SYNC and RING Test

Test 8 verifies the correct operation of the one-to-two-millisecond pulsed modem lead, used as CARRIER DETECT RESET on an asynchronous modem and NEW SYNC on a synchronous modem. The PULSED MODEM LD (output word 4, bit 4) bit is toggled repeatedly to verify that the output timing and the setting of the RING input are correct.

2.5.9 Test 9 -- External NEW SYNC/RING and Light Blink Test

Test 9 checks the CDR/NEW SYNC EIA driver and the RING EIA receiver. The PULSED MODEM LD is toggled and RING is checked for agreement. Since this test requires a loopback connector, it is executed only when the connector is present. If the loopback connector has LED indicators, the test verifies that the EIA output drivers and LEDs function by blinking the three red and three green LEDs three times, and then blinking each pair once. If test 8 passes and test 9 fails, the EIA driver or the receiver circuits associated with these signals are probably failing.

2.5.10 Test A -- Internal/External DTR, DSR, and NSF Test

Test A toggles DTR and checks the toggling of DSR. It also verifies that DSR setting causes NSF to set, when NSF is enabled. This test is not executed when a modem is present.

2.5.11 Test B -- External RTS, CTS, and DCD Test

Test B toggles RTS and checks the toggling of CTS and DCD. It also verifies that the setting of DCD causes NSF to set when NSF is enabled. This test is not executed when a modem is present.

2.5.12 Test C -- External SRTS and SDCD Test

Test C toggles SRTS and checks the toggling of SDCD. It also verifies that changes in SDCD cause NSF to set, when NSF is enabled. This test is not executed when a modem is present.

2.5.13 Test D -- Internal WRQ Test

Test D sets up the conditions that cause WRQ to be set and then verifies that WRQ is set when it is enabled and reset when it is disabled. It also verifies that INTSUM is set when WRQ equals 1.

2.5.14 Test E - Internal HDX RRQ Mask Test

Test E enables the HALF-DUPLEX bit, which masks the receive data to a space, and verifies that no RRQ interrupts are generated.

2.5.15 Test F -- Internal Break, Parity, and Framing Error Test

Test F forces a line-break condition (the transmitted data equals a constant space) and verifies the proper operation of the BREAK bit. Since the breaking condition also forces a parity error and framing error, these bits (PE and FE) and RCVERRSUM are also checked.

2.5.16 Test 10 -- Internal Baud Rate Test

Test 10 verifies that the baud rate generator circuits are within a three percent tolerance, using the real time clock as the reference timing element. The test first determines that the 9600 baud rate is within the three percent tolerance. Then it verifies that the 4800, 2400, 1200, 880, 600, and 200 baud rates are within a six percent tolerance. If the 9600 rate fails and the other rates pass, the internal oscillator is off frequency, but the divider circuits are functioning.

Test 10 also transfers data in asynchronous mode to verify data transfer capability.

2.5.17 Test 11 -- Internal SYNC OVERRUN Test

Test 11 sets up a data transfer with RRQ disabled, thus forcing an OVERRUN condition. It verifies that the OVERRUN and RCVERRSUM bits are set. It then enables RRQ and verifies that RRQ goes from 0 to 1. The test also receives the character transmitted and verifies that the transfer was made correctly.

2.5.18 Test 12 - Internal SYNC UNDERRUN and DLE/SYNC Fill Test

Test 12 writes the SYNC and DLE registers of the ASTRO and then uses the transparent idle fill feature to transmit a DLE/SYNC sequence. This constitutes a transmitter UNDERRUN condition; therefore, the setting of the UNDERRUN bit is tested. Then the receiver is enabled and the proper transmission and reception of the DLE/SYNC sequence is verified.

2.5.19 Test 13 -- Internal Synchronous Data Test

Test 13 performs a series of 200-byte data transfers in self-test, synchronous mode to verify the data transfer capability of the CIM. The data pattern used is a repeating >AA55AA55, etc. The transfer is performed four times and must be executed without errors all times in order to pass.

2.5.20 Test 14 -- External Asynchronous Data Test

Test 14 is the primary modem test for asynchronous modems. It performs four 200-byte data transfers in asynchronous mode at a different baud rate from test 12. The data pattern used is an incrementing data pattern. The baud rate is 1200 baud for all eight-bit combinations. Other test parameters are essentially the same as in test 12.

2.5.21 Test 15 -- External Synchronous Data Test

Test 15 is the primary modem test for synchronous modems. It performs 10 200-byte data transfers in synchronous mode. Five test data patterns are used including incrementing data and alternating ones and zeros. The character length used is eight bits per character with no parity. The baud rate is 9600 bps with the test connector or at the modem rate. Other test parameters are essentially the same as in test 13, except that all 10 of the data transfers must be successfully completed.

NOTE

Tests 13 and 15 use a clock-recovery method for synchronizing the data (unless a synchronous modem or the loopback connector with lights is present). Thus, although the data format is synchronous, the clocking scheme can be essentially asynchronous.

2.5.22 Test 16 -- Internal Synchronous Strip Test

Test 16 performs a series of 200-byte data transfers in self-test, synchronous mode to verify the data transfer capability of the CIM. The transfer is performed four times without resetting the module to verify that the module strips have synchronized characters between blocks.

3.1 ERROR MESSAGES

When the CRCOMM test detects a fault condition, it outputs a self-explanatory error message and an error message number. Messages are constructed in a modular fashion, that is, a given error message number may appear with two or more conditions. (For example, RSVOUT NOT SET and RSVOUT NOT RESET have the same error number.) The modular message strings are as follows:

NOT SET

NOT RESET

SHORT

TOO LONG

SET WHEN NOT EXPECTED

All messages that relate to a status error condition are preceded by the following message:

*** STATUS ERROR!

The CRCOMM error messages are listed in the following table.

Error Number	Error Message
1	RSVOUT
2	MODE
3	SDCD
4	NSF
5	INTR SUM
6	TIMEXP
7	TIMER
8	BY TIMEXP
9	*** ERROR! ID SWITCH READS = XX; EXPECTED = YY.
A	UNEXPECTED INTERRUPT AT LEVEL X.
B	UNEXPECTED INTERRUPT FROM CIM.
C	CIM DOES NOT INTERRUPT CPU.
D	WROTE READ XOR OW2 = XXXX. XXXX. ZZZZ. OW3 = XXXX. XXXX. ZZZZ.
E	RING
F	PULSED MODEM TIMING (NEW SYNC)
10	RWBUSY
11	DSR
12	CTS
13	DCD
14	WRQ
15	RRQ
16	OVERRUN

Error Number	Error Message
17	FRAMING ERROR
18	PARITY ERROR
19	*** DATA TRANSFER ERROR! XMIT = XX RECV = YY. BYTE COUNT = B
1A	RRQ GENERATED WHEN HALF DUPLEX SELECTED.
1B	RCVERR
1C	*** TIME OUT ERROR!
1D	*** STATUS ERROR!
1E	*** RATE ERROR! XXXX BAUD RATE TOO HIGH/LOW.

3.2 ERROR MESSAGE ANALYSIS

The following list outlines probable causes of various error indications.

* If errors are detected when the CRCOMM test is executed with a loopback connector present, it is likely that the CIM is faulty.

* If the test is executed in internal mode and there are errors, it is possible that the basic CRU circuitry of the CPU or chassis is malfunctioning.

* If the CIM functions in internal mode but generates errors when a loopback connector is present, it is likely that the EIA driver/receiver has an error.

* If the test executes properly with a loopback connector but not with an external modem, it is likely that the modem cable or the modem itself is at fault.

* If there are intermittent data errors when using a modem, these errors are attributable to the modem.

* When the message ***STATUS ERROR! RWBUSY NOT RESET appears repeatedly, this indicates that the program is unable to attain basic communication with the CIM and that the initialization parameters may have an error. The message *** TIME OUT ERROR! is symptomatic of the same condition.

* If tests 3, 9, or 10 fail, it is possible that the CPU line frequency is outside a tolerance of plus or minus 1 Hz.

ENETST

ETHERNET(tm) INTERFACE BOARD DIAGNOSTIC
EI990, EI300 BOARDS

ETHERNET(tm) INTERFACE BOARD DIAGNOSTIC (ENETST)

ENETST

ETHERNET(tm) INTERFACE BOARD (EI990,/300) DIAGNOSTIC TEST

1.1 INTRODUCTION

ENETST, the Ethernet Interface Board Diagnostic Test, assures full performance of the EI990 and EI300 interface boards (part numbers 2239135-0001 and 2239155-0001, respectively).

ENETST is loaded and controlled by DOCS. You can execute ENETST with no external equipment connected, but the self-tests and Part 60 (the 60 series tests) will fail without a loopback connector.

1.2 TEST REQUIREMENTS

The following equipment is required to operate ENETST:

* A 990 computer with CPU of mapped 990/10, 990/10A, 990/12, S300, or S300A with a minimum of 64K bytes of memory (where K equals 1024)
* An Interface to an Ethernet local area network (LAN) (EI990/300)
* An interactive terminal
* A loading device

One of the following is necessary to run all tests in loopback mode:

* For the EI990: A loopback connector (part number 2303065-0001). The local line /X.21 end of the loopback connector fits into the 18-pin connector on the EI990 controller.

Ethernet is a trademark of Xerox Corporation.

* For the EI300: (1) A loopback connector (part number 2239709-0001). The connector fits into the 15-pin connector J4 on the external 1-to-4 cable adapter. (2) An external 1-to-4 cable adapter (part number 2239163-0001). The assembly mates with the 40-pin connector at the back of the EI300 board.

Both parts are necessary to perform the ENETST on the EI300.

All of the following are necessary to run all tests in network mode:

* A viable network of at least one additional operating system that will function as an echo server.

* An interface-to-transceiver cable, 10 meters (32.8 feet): for the EI990, part number 2239129-0001, 0002, or 0003; for the EI300, part number 2239133-0001 or 0002

* A 3Com 3C100 Ethernet Transceiver, properly terminated into the network.

For more specific details refer to the EI990 Ethernet Local Area Network (LAN) Controller Installation and Operation manual, part number 2234392-9701.

NOTE

The Ethernet Transceiver, (3-COMM, 3C100), properly terminated if disconnected from the network, can be used to run the ENETST in Loopback Mode.

1.3 TEST CHARACTERISTICS

ENETST operates under the control of DOCS. Refer to Volume 1 of the Unit Diagnostics Handbook for information about DOCS operation.

ENETST consists of 17 tests, all run from the EA, LA, ET, or LT verbs.

Test	Title
11	TPCS MS & STF Bits Test
12	TPCS Interface Test
13	TPCS Data Lines Test
21	Verify Primitive Commands Test
22	Verify Data Link Commands Test
31	Self-Test Test
41	Unmapped Address Test
42	Mapped Memory Test
51	Short Transmit Test
52	Medium Transmit Test
53	Long Transmit Test
54	Complex Transmit Test
61	Short Transmit/Receive Test
62	Medium Transmit/Receive Test
63	Long Transmit/Receive Test
64	Complex Transmit/Receive Test
65	Max Packet Transmit/Receive Test

In addition to the verbs supplied by DOCS, ENETST uses the following test execution verbs:

Test Execution Verb	Function
EA	Execute all tests
ET	Execute an individual test one time
LA	Loop on all tests
LT	Loop on an individual test

Utility verbs help you isolate errors that are detected during test execution:

Utility Verb	Function
DS	Display status
FE	Find echo servers
IT	Initialize test
PE	Display error count
PT	Print tests
PV	Print verbs
RS	Reset controller
SC	Display status counters
SL	Oscilloscope timing loop
TH	Display test history

Other verbs utilized in the execution of ENETST are:

Verb	Function
BC	Build command lists
LO	Loop on command lists
ST	Run self-tests
ES	Echo serve mode
CD	Collision detect
ID	Display station identification
TD	Time domain
MN	Monitor mode

You can also use the Initialize Test (IT) verb to reinitialize the ENETST initialization parameters.

You should execute all the tests in the ENETST diagnostic to verify that the hardware is functioning properly.

For information on the data structures used by the Ethernet controller System Communication Area (SCA), Transmit Data Block (TDB), Transmit Data Descriptor (TDD), Receive Control Block (RCB), and Receive Data Descriptor (RDD), consult the EI300/EI990 Ethernet Interface Programming and ROM Code Listing.

2.1 TEST INITIALIZATION

ENETST must be loaded and initialized by DOCS before you can begin testing. Volume 1 of the Unit Diagnostics Handbook explains the loading procedure. When DOCS has loaded the ENETST module, the name and version of the test appears:

```
ENETST - ETHERNET INTERFACE CONTROLLER DIAGNOSTIC.

VERSION  XX  JJJ/YY

ENETST TESTS EI990 AND EI300 BOARDS.
```

where:

XX indicates the revision letter.

JJJ is the Julian date.

YY is the year.

Then DOCS executes the IT verb with the following prompts:

```
ENTER EI990 TILINE BASE ADDRESS:  DEF = F8E0 -
     Enter the TILINE(tm) Peripheral Control Space (TPCS) address.
```

TILINE is a trademark of Texas Instruments Incorporated.

ENTER EI990 INTERRUPT LEVEL: DEF = F -
Enter the CPU interrupt level of the EI990/300 board.

ENTER ENVIRONMENT TYPE: [0=WITH LOOP-BACK, 1=ON NETWORK] -
DEF = 1
If the test is being conducted with a loopback connector, enter 0. If the test is being conducted on a system that is part of a network, enter 1. (ENETST will also run in loop-back mode if you are on a network.)

DO YOU WANT TO RUN THE TEST WITH INTERRUPTS? [0=NO, 1=YES] DEF=1
Normal operation is with interrupts.

ENTER COMPUTER LINE FREQ: [0=50, 1=60] DEF = 1 -
This prompt is not asked on an S300/S300A.

If 1 was entered for ENVIRONMENT TYPE (on a network), the following displays:

THE TEST WILL USE THE FIRST ECHO SERVER FOUND IF NOT SPECIFIED. -

DO YOU WANT TO SPECIFY AN ECHO SERVER? [0=NO, 1=YES] DEF = 0 -
If you have indicated that you wish to specify an echo server, then the following is asked:

YOU MUST ENTER 12 ID DIGITS + 4 CHECKSUM DIGITS. -

TEST WILL CORRECT CKSUM AND ASK AGAIN IF ID & CHECKSUM

DON'T MATCH.

ENTER MOST SIGNIFICANT DIGITS FIRST.

DEF ID = XX-XX-XX-XX-XX-XX*XX-XX -
A total of 16 digits must be entered in order for the ID digits to be justified correctly. Press RETURN to accept the default.

You must enter 12 ID digits. If you do not know the checksum, enter any four numbers and the test will calculate the checksum for you and return it as a default.

2.2 VERB DESCRIPTIONS

ENETST uses many verbs common to other diagnostic tests. Often, however, these verbs take on special characteristics for their use in ENETST execution. These verbs assist you in diagnosing controller faults by correct analysis of test data.

2.2.1 Test Execution Verbs

The following ENETST-driver verbs are used to execute one or more test sequences, and/or to cause continuous looping on one or more of these sequences. These verbs are common to most diagnostics; since they govern the execution of the test itself, they change little in definition from one diagnostic test to the next.

NOTE

Batch streams can be utilized to expand or automate execution of various test sequences not provided by the test execution verbs.

2.2.1.1 Execute All Tests (EA) Verb. The EA verb causes all the tests in the diagnostic to execute a single time.

2.2.1.2 Execute Individual Test (ET) Verb. The ET verb causes one test in the diagnostic to execute a single time. This routine branches to the routine associated with the reply number entered in response to the TEST # __ prompt.

2.2.1.3 Loop On All Tests (LA) Verb. The LA verb causes all tests to execute in sequence. The number of times all tests in the diagnostic will loop is controlled by your reply to the following prompt:

ENTER NUMBER OF LOOPS; DEF = >XXXX -

If you enter 0 for the number of loops, then LA loops until ATOUT (CMD OUT, ESC OUT). Otherwise, LA loops until the number of test repetitions equals the number entered in response to the prompt.

2.2.1.4 Loop On Individual Test (LT) Verb. The LT verb causes a single specific test in the diagnostic to loop. If you enter 0 for the number of loops, then LT loops until ATOUT (CMD OUT, ESC OUT). Otherwise, LT loops until the number of test repetitions equals the number entered in response to the same prompt as seen in the case of the LA verb.

2.2.2 Utility Verbs
Utility verbs provide DOCS service functions that are required by the diagnostic. For the purpose of ENETST, the following verbs are classed as utility verbs.

2.2.2.1 Display Status (DS) Verb. The DS verb performs the following functions:

* Reads TPCS words 0-3 (controller slave words) and displays as hex values the labels for individual words and fields

* Reads the System Communication Area (SCA) and displays its contents (if the SCA address is in the lower 64K of TILINE memory)

* Displays the current SCA address

2.2.2.2 Find Echo Servers (FE) Verb. The FE verb prints a list of echo server stations that have responded to a broadcast for echo servers. The responding LAN boards can be EI990, EI300, or TI Professional Computer type LAN boards. The verb lists up to 16 echo servers. It times out if 16 have not responded within 4 seconds. The FE verb then prompts you for a number (0-F) to use as the echo server, with the number 0 as the default.

2.2.2.3 Initialize Test (IT) Verb. The IT verb is always the first verb to execute after the initial loading of a diagnostic. (See paragraph 2.1.) The IT verb inputs all pertinent parameters concerning the testing environment being used. It can also be used to change parameters during testing.

2.2.2.4 Display Error Count (PE) Verb. The PE verb displays diagnostic error counts on the interactive device.

2.2.2.5 Print Tests (PT) Verb. The PT verb outputs the ENETST test numbers to the DOCS I/O device along with a short description of each test.

2.2.2.6 Print Verbs (PV) Verb. The PV verb ouputs the ENETST verb list to the DOCS I/O device along with a short description of each.

2.2.2.7 Reset Controller (RS) Verb. The RS verb issues a software reset or master reset to the EI990/300 board only.

2.2.2.8 Display Status Counters (SC) Verb. The SC verb reads and displays the EI990/300 status counters. The status counters are read using a Read Status Counters command.

The format displayed by this verb is similar to the format encountered in the use of the DOCS Dump Memory (.DM) verb. For a description of the .DM verb and the subsequent memory dump,

consult Unit Diagnostics Volume I, General Diagnostics Information.

Just as the .DM verb causes a memory dump, the SC verb causes a dump of status counters. Definitions of each word in the dump are shown in the following table.

Offset (Bytes)	Word Length (Bits)	Number of Words	Contents
>0000	32	1	Number of received frames
>0004	32	2	Number of received bytes
>000C	32	24	Received frame size
>006C	16	1	Number of frames with CRC errors
>006E	16	1	Number of frames with alignment errors
>0070	16	1	No receive buffer error count
>0072	16	1	Receiver overrun error count
>0074	32	1	Number of frames transmitted
>0078	32	2	Number of bytes transmitted
>0080	32	24	Transmitted frame size count
>00E0	32	1	Number of frames too small for Ethernet
>00E4	32	1	Number of frames too large for Ethernet
>00E8	32	1	Heartbeat count
>00EC	32	1	No carrier sensed during transmit
>00F0	32	1	Loss of clear to send
>00F4	32	1	Transmit underrun
>00F8	32	1	Transmit deferred to traffic
>00FC	32	1	Number of frames with no collisions
>0100	32	1	Number of frames with 1 collision
>0104	32	1	Number of frames with 2 collisions
>0108	32	1	Number of frames with 3 collisions
>010C	32	1	Number of frames with 4 collisions
>0110	32	1	Number of frames with 5 collisions
>0114	32	1	Number of frames with 6 collisions
>0118	32	1	Number of frames with 7 collisions
>011C	32	1	Number of frames with 8 collisions
>0120	32	1	Number of frames with 9 collisions
>0124	32	1	Number of frames with 10 collisions
>0128	32	1	Number of frames with 11 collisions
>012C	32	1	Number of frames with 12 collisions
>0130	32	1	Number of frames with 13 collisions
>0134	32	1	Number of frames with 14 collisions
>0138	32	1	Number of frames with 15 collisions
>013C	32	1	Number of frames with maximum collisions
>0140	8	8	Current Ethernet address plus checksum
>0148	8	8	Ethernet address in ROM plus checksum
>0150	32	1	Select header fields list pointer
>0154	32	1	Multicast filter list pointer
>0158	32	1	82586 configuration data pointer
>015C	8	20	Revision data (text)

2.2.2.9 Oscilloscope Timing Loop (SL) Verb. The SL verb requests that you specify read or write mode. It then reads or writes to a memory address that you specify. The SL verb suppresses TILINE time-outs, memory errors, or all interrupts, if requested.

If asked to suppress all interrupts, the SL verb will loop up to >FFFF (64K) times as specified by the operator and then checks to see if it has been interrupted by an @ or CMD on the interactive device. If you entered 0 in response to the NUMBER OF LOOPS? prompt, the SL verb loops until halted from the front panel.

2.2.2.10 Display Test History (TH) Verb. The TH verb summarizes the results of the last test you executed. The TH verb shows the status of each command run by the controller during the test's execution, providing a trace of the test's commands and the status associated with those commands. It cannot show the results of previous tests because of memory limitations.

2.2.3 Miscellaneous Verbs

The following additional verbs are utilized by ENETST. These are special purpose verbs required for the testing and manufacture of the EI300/EI990 controllers.

2.2.3.1 Build Command Lists (BC) Verb. The BS verb, by accepting your input, allows you to build a command structure or unique EI300/990 command sequence. You are only required to input the variable data bytes of the EI300/990 command. The Build Command will format all required control characters. The BC verb then appends this command to a specified list of commands, clearing the last word in each list.

The BC verb can be used to perform EI300/990 firmware verification. Or, when used in conjunction with DOCS batch command streams, it can provide new test capabilities to the test designer. Consult the EI300/EI990 Ethernet Interface Programming and ROM Code Listing for command input formats.

2.2.3.2 Loop On Multiple Commands (LO) Verb. The LO verb allows you to issue any command sequence that has been built in a list by the BC verb. The LO verb issues commands in this specific list, or on all lists, or in a given memory location, for the number of loops specified.

You can direct the LO verb to loop on one or all of the valid lists. If you specify 0 in response to the prompt, the controller executes the loop until interrupted by an entry of @ on the interactive device. LO outputs a bad status error if bad status is returned from the driver.

The LO verb can be used to perform EI300/990 firmware verification, or, when used in conjunction with DOCS batch command streams, can provide new test capabilities to the test designer.

2.2.3.3 Run Self-Tests (ST) Verb. The ST verb issues the command for a specified self-test (or all of them) for a specified number of loops. If you specify 0 in response to the NUMBER OF LOOPS? prompt, the controller executes the loop until interrupted by an entry of @ on the interactive device. For more information on self-tests, see paragraph 3.4.

2.2.3.4 Echo Serve Mode (ES) Verb. The ES verb places the station in echo-server mode, which causes the station to listen to the Ethernet and echo all packets that are detected back out onto the network.

This verb can provide the Echo-Off-Server Test with an echo server. The atout function is used to exit this verb, after which the controller should be reset with the RS verb to return to a known state.

2.2.3.5 Collision Detect (CD) Verb. The CD verb asks you to cause collisions to occur by some external means, such as opening (unterminating) the network cable and then pressing the RETURN key. The verb then verifies that the controller recognizes the collision signal sent by the transceiver. An error is output if collisions are not detected. If the verb reports an error, it will return the TDB and frame status.

2.2.3.6 Display Station Identification (ID) Verb. The ID verb tells the controller to check and return the station ID number, which the verb then displays on the interactive device.

2.2.3.7 Time Domain (TD) Verb. Thg TD verb performs a TDR (Time Domain Reflectometry maintenance test) on the serial link and returns a value (time), which can be converted into a distance for linear analysis of the link (cable).

After the controller receives a TDR command, it performs a Time Domain Reflectometer Test by transmitting a jam pattern and monitoring Carrier Sense and Collision Detect signals. When a jam is transmitted, an internal 12-bit counter starts counting.

There are four possible test results:

4XXX The Carrier Sense signal does not go active before the counter expires. For a Transceiver that should return Carrier Sense during transmission, this means that there is a problem on the cable between the 82586 and the Transceiver. For a Transceiver that should not return Carrier Sense during transmission, this is normal.

1XXX The Carrier Sense signal goes active and then inactive before the counter expires. For a Transceiver that should return Carrier Sense during transmission, this means that there is a short on the link.

2XXX The Collision Detect signal goes active before the counter expires. This means that the link is not properly terminated (and open).

8XXX The Carrier Sense signal goes active but does not go inactive and Collision Detect does not go active before the counter expires. This is the normal case and indicates that there is no problem on the link.

The distance to the cable failure can be calculated as follows:

Distance = TIME * Vs / 2 * Fs

where: xxxxx

TIME = XXX (Indicated in the previous test results)

Vs is the wave propagation speed on the link (M/s)
(NOM = 2.4 * 10 X E08)

Fs is the serial clock frequency (Hz)
(NOM = 10 X E07)

Accuracy is plus/minus Vs / 2 * Fs

Upon completion, the Transmit-Byte-Machine passes the RESULT word to the CPU.

2.2.3.8 Monitor Mode (MN) Verb. The MN verb places the station into monitor mode, which causes it to monitor the Ethernet and display the source, destination, length, and status of packets the station detects on the network.

2.3 TEST DESCRIPTIONS

ENETST consists of 17 tests which, in addition to interpreting the self-test results, verify the controller's ability to communicate on the network.

ENETST is not a network diagnostic in that it does not analyze faults on the network, but merely isolates faults to the Field Replaceable Part (FRP) or to the network.

2.3.1 Parts

The tests which together comprise the ENETST diagnostic are normally run singly to simplify the process of debugging. However, they can be run in specific grouping through the use of parts. You can answer the TEST? prompt with the number of a given part just as though the part were itself a test. The function of the part is to then call and run certain tests in a given order as shown in the following table.

Part Number	Tests Called	
10	11	TPCS MS & STF Bits Test
	12	TPCS Interface Test
	13	TPCS Data Lines Test
20	21	Verify Primitive Commands Test
	22	Verify Data Link Commands Test
30	31	Run Each Self-Test
40	41	Unmapped Address Test
	42	Mapped Address Test
50	51	Short Transmit Test
	52	Medium Transmit Test
	53	Long Transmit Test
	54	Complex Transmit Test
60	61	Short Transmit/Receive Test
	62	Medium Transmit/Receive Test
	63	Long Transmit/Receive Test
	64	Complex Transmit/Receive Test
	65	Max Packet Transmit/Receive Test

Tests 11, 12, and 13 verify that the TILINE address is valid and that the controller is present at the specified address by issuing a master reset and checking the results. These tests verify that the IP, PA, SWR, MR, and STF bits function correctly. The rest of the TPCS bits are checked by the Self-Test, test 31.

2.3.2 Test 11 -- TPCS MS and STF Bits Test

Format: Test 11 runs from the EA, LA, ET, and LT verbs.

Test 11 tests the function and set/reset ability of TPCS words 0 and 1, and bits MR and STF. All other TPCS bits are checked in test 11, test 12, or self-tests 7 and 8.

2.3.3 Test 12 -- TPCS Interface Test

Format: Test 12 runs from the EA, LA, ET, and LT verbs.

Test 12 tests the function and set/reset ability of TPCS words 0 and 1, bits IP, PA, and SWR. All other TPCS bits are checked in self-tests 7 and 8 (which test 12 also calls), or tests 11 and 13.

2.3.4 Test 13 -- TPCS Data Lines Test

Format: Test 13 runs from the EA, LA, ET, and LT verbs.

Test 13 writes data patterns to TPCS word 2. These patterns check for stuck-at-0s or stuck-at-1s faults.

2.3.5 Test 21 -- Verify Primitive Commands Test

Format: Test 21 runs from the EA, LA, ET, and LT verbs.

Test 21 executes a list of all the primitive commands and verifies that each has performed its defined function and/or executed without status errors. Run the TH verb if listed error/status messages are desired for each command.

2.3.6 Test 22 -- Verify Data Link Commands Test

Format: Test 22 runs from the EA, LA, ET, and LT verbs.

Test 22 executes a list of some primitive and most of the data link commands (those that should run in data link mode) and verifies correct completion. This ensures that the EI990 will function in both the primitive and data link modes. All data link commands (with the exception of Transmit and Receive commands) are tested in this test. These commands are tested in the Echo-Off-Server Tests (60 test series).

2.3.7 Test 31 -- Self-Test Test

Format: Test 31 runs from the EA, LA, ET, and LT verbs.

Test 31 will execute all the Self-Test commands and verify correct completion on the interactive device.

NOTE

The self-tests are caused to run automatically by power-up, or the use of the Master Reset, or the running of test 11. Test 31 is of primary benefit because the results of this intentional running of each self-test is that the status of each individual test may then be viewed by using the TH verb, which is not the case when the self-tests are caused to run automatically.

2.3.8 Test 41 -- Unmapped Memory Addressing Test

Format: Test 41 runs from the EA, LA, ET, and LT verbs.

Test 41 tests the controller's ability to address unused TILINE memory from the end of the diagnostic to >F800. The test first initializes all the memory from the end of the diagnostic to >F800, then moves the data to a buffer in the diagnostic (>C00 bytes at a time), verifying the data with each block moved.

2.3.9 Test 42 -- Mapped Memory Addressing Test
Format: Test 42 runs from the EA, LA, ET, and LT verbs.

Test 42 reads memory from >01XXXX to >1FXXXX, (with XXXX = to a table of: >0000, >5554, >AAAA, >CCCC, >F0F0, >FF00, >FFFE) to check the controller's ability to address mapped memory. The test compares the data read from the tests LDS instruction with the data returned from the RW command from the controller.

If a memory error occurs, test 42 checks to make sure the EI990/300 returns a memory error status. Then the test initializes the current test memory address with the Most Significant Byte of this address set equal to the Most Significant Byte of the Most Significant Word (MSB = MSB of the MSW) and the Least Significant Byte set equal to the Least Significant Byte of the Least Significant Word (LSB = LSB of the LSW). For example, at address 1F5554, the data would be 1F54.

The test then reads memory from the same address again. If a memory error still occurs, test 42 outputs an error and increments to the next address.

If a TILINE time-out occurs, test 42 checks for a time-out in the returned status. Test 42 issues an RW command with a byte address to test the Invalid Address Detected status.

Test 42 reads >FBFE to generate a TILINE time-out. If the controller completes all the reads with good status and the compares are OK, the test completes successfully. Otherwise, an error is issued.

For all reads that generate an error, test 42 compares the address sent with the address latched in EI990/300 memory. When an error occurs, the test outputs an error and continues. If you want to use the TH verb after an error, Pause On Errors should be set before running the test.

NOTE

The following tests, tests 51 through 54 and 61 through 64, are arranged in the order of increasing complexity to make debugging tasks more practical. Therefore, if a controller passes test 54, it need not be probed with tests 51, 52, or 53. The same principle is true of the 61 through 64 test series. Test 65, however, should not be skipped since it tests the ability to transmit and receive a maximum length frame (packet).

2.3.10 Test 51 -- Short Transmit Test
The tests in the 50 series (51 through 54), verify the controller's ability to transmit packets of data onto the Ethernet.

Format: Test 51 runs from the EA, LA, ET, and LT verbs.

Test 51 tests the controller's ability to transmit one frame (packet of data) consisting of one Transmit Data Descriptor (TDD).

2.3.11 Test 52 -- Medium Transmit Test
Format: Test 52 runs from the EA, LA, ET, and LT verbs.

Test 52 tests the controller's ability to transmit one frame (packet of data) consisting of two TDDs.

2.3.12 Test 53 -- Long Transmit Test
Format: Test 53 runs from the EA, LA, ET, and LT verbs.

Test 53 tests the controller's ability to transmit one frame (packet of data) consisting of three TDDs.

2.3.13 Test 54 -- Complex Transmit Test
Format: Test 54 runs from the EA, LA, ET, and LT verbs.

Test 54 tests the controller's ability to transmit six frames (packets of data) consisting of one, two, and three TDDs.

2.3.14 Test 61 -- Short Transmit/Receive Test
Format: Test 61 runs from the EA, LA, ET, and LT verbs.

Each of the tests in the 61 through 65 (60 series) tests the controller's ability to find an echo server by broadcasting an echo request and addressing the rest of its packet(s) to the first station that responds. Optionally, each test addresses its packets to the station specified in the corresponding IT verb prompt. These tests send echo-request packets of variable length and data patterns. Upon receiving them back, the test verifies them. On completion, the tests notify the operator what station was used as an echo server.

If a transmitted packet is lost, an error is reported and the TH verb status reports a lost packet for that particular transmit command. Normal Ethernet operation is on a Best Try basis. It does not guarantee the packet will be delivered. What this means in relation to the diagnostic is that some packets might be lost through no fault of the EI990/EI300 controller or the diagnostic.

If ENETST is operating under one or more of the following conditions or configurations, an occasional lost packet (as reported in the TH verb) may not necessarily indicate a board hardware problem:

* Using a TI Professional Computer (or non-TI LAN) as an echo server

* Having two or more stations executing part 60 (60 series tests) to the same echo server, especially if using the firmware echo server (self-test number 82)

* Running ENETST on a busy network where other stations are sending and receiving packets

A packet should never be lost while testing in loopback mode. Also, the ES verb can handle without error at least two stations looping on test 64, and will probably handle up to five stations without dropping any packets if there is no other traffic on the network.

NOTE

The first time one of the 60 series tests executes, and the test is finding an echo server, only the first packet echoed from another station will be accepted. All others will be called unexpected and rejected. Since the board loops all broadcast packets, ENETST will reject its own station looped packet also.

Test 61 tests the controller's ability to transmit and receive one normal-size frame (packet of data), consisting of one Transmit Data Descriptor (TDD).

2.3.15 Test 62 -- Medium Transmit/Receive Test
Format: Test 62 runs from the EA, LA, ET, and LT verbs.

Test 62 tests the controller's ability to transmit and receive one normal-size frame (packet of data), consisting of two TDDs.

2.3.16 Test 63 -- Long Transmit/Receive Test
Format: Test 63 runs from the EA, LA, ET, and LT verbs.

Test 63 tests the controller's ability to transmit and receive one normal-size frame (packet), consisting of three TDDs.

2.3.17 Test 64 -- Complex Transmit/Receive Test
Format: Test 64 runs from the EA, LA, ET, and LT verbs.

Test 64 tests the controller's ability to transmit and receive six normal-size frames (packets), consisting of one, two and three TDDs.

2.3.18 Test 65 -- Maximum Packet Transmit/Receive Test
Format: Test 65 runs from the EA, LA, ET, and LT verbs.

Test 65 tests the controller's ability to transmit and receive the maximum-size frame (packet), which is one 1514-byte packet consisting of one TDD.

3.1 ERROR MESSAGES

ENETST issues error messages whenever it detects error conditions. All error messages are routed to the DOCS error message device. These messages are listed in the following table along with their corresponding error numbers (in hexadecimal).

Error Number	Error Message
>03	TILINE TIMEOUT READING TPCS ADDRESS = XXXX
>04	TPCS W2 SHOULD = >4549 ("EI") OR LSW OF SCA; XXXX WAS ACTUAL VALUE
>E	TPCS W3 SHOULD = >4F4B ("OK") OR MSW OF SCA; XXXX WAS ACTUAL VALUE
>E	TPCS = >XXXX MAY NOT BE A EI990, OR SELF-TEST ERROR OCCURRED, OR OLD 'SCA'SELF TEST SHOULD RUN OK BEFORE RUNNING TESTS
>05	TILINE TIMEOUT OCCURRED - WP = XXXX - PC = XXXX - ST = XXXX
>08	*** TEST NOT INITIALIZED - EXECUTE ITVERB ***
>0A	MEMORY ERROR OCCURRED ON A READ FROM ADDRESS XXXX
>0B	BAD STATUS WAS RETURNED AFTER ISSUING TEST(S) IN LIST X'
>0F	IP BIT DID NOT SET
>1C	* UNABLE TO CLR INTERRUPT AT P2-66 WITH TPCS; GENERATED I/O RESET *

Error Number	Error Message
>11	*** UNABLE TO CLR INTERRUPT WITH I/O RESET CPU IS @ IDLE, @ OUT TO PROCEED***
>12	*** UNEXPECTED INTERRUPT AT LEVEL X OCCURRED; EI990 BOARD?
>13	*** ERROR COUNT = >XXXX
>14	EXPECTED TPCS WORD 0 =>0800, ACTUAL =>XXXX AFTER SOFTWARE RESET
>16	MR BIT DID NOT SET
>17	MR BIT NOT CLR IN 1 SEC
>18	EXPECTED TPCS WORD 0 =>0800, ACTUAL =>XXXX AFTER MASTER RESET
>19	TEST (OR VERB) XX FAILED USE "TH" (TEST HISTORY VERB) TO VIEW STATUS ERROR OCCURRED ON EI990 AT TPCS=>XXXX ** IF TEST IS USING AN ECHO SERVER, THIS ERROR MAY INDICATE NORMAL ETHERNET OPERATION AND NOT A CONTROLLER ERROR. SEE DIAGNOSTIC MANUAL FOR MORE INFORMATION. '
>1A	NO COLLISIONS DETECTED IN TRANSMIT
>1B	STF BIT NOT SET IN 1 SEC
>1C	TDB CONTROL & STATUS WORD =>XXXX TDB FRAME STATUS WORD =>XXXX
>1E	JUMP TO SUBROUTINE COMMAND FAILED
>1F	FATAL ERROR OCCURRED REMAINING COMMANDS WILL BE ABORTED.
>20	SWR BIT DID NOT SET

Error Number	Error Message
>22	One of the following messages will be output in the prompt below: - (Message Here . . .) - READ ADDRESS >XXXXXXXX - EXPECTED DATA = >XXXX; DATA RETURNED = >XXXX - NO TILINE TIMEOUT, BUT SET AT EI990 - NO MEMORY ERROR, BUT SET AT EI990 - NORMAL READ, BUT STATUS HAD ERRORS AT EI990 - NO INVALID ADDRESS, BUT SET AT EI990 - TILINE TIMEOUT, BUT NOT SET AT EI990 - MEMORY ERROR OCCURRED, BUT NOT SET AT EI990 - INVALID ADDRESS PASSED, BUT NOT SET AT EI990 - DATA PASSED DID NOT = DATA READ AT EI990 - ADDRESS READ IS IN LAN BD. MEMORY
>23	PASSED ADDRESS >XXXXXXXX TO EI990 ''RW'' COMMAND' EI990 READ ADDRESS = >XXXXXXXX
>50	COMMAND CONTROLLER NOT IDLE AFTER 2 SECS.
>51	SELF-TEST FAILURE
>52	NO SELF TEST FAILURE, BUT NO EI-OK

Error Number	Error Message
>53	COMMAND TIMED OUT
>55	PRIMITIVE ATTENTION SET UNEXPECTEDLY
>56	NO AFB WHEN IPB WAS SET
>57	A COMPLETE TDB WAS EXPECTED BUT NOT FOUND
>58	NO LGA SET AFTER WAITING 8.33 MSECS
>59	EI990 TIMER EXPIRED UNEXPECTEDLY
>60	NO AFA SET WHEN IPA WAS SET
>61	A HOST-OWNED RCB WAS EXPECTED BUT NOT FOUND
>63	TCB INITIATING TDB IS NOT ON RECEIVED QUEUE
>64	UNMAPPED MEMORY ADDRESSING TEST FAILED.
>66	TRANSMIT TEST FAILED.
>67	SHORT PACKET VERIFICATION TEST FAILED.
>68	LONG PACKET VERIFICATION TEST FAILED.
>69	ECHO SERVER TERMINATED ON FATAL ERROR. USE DS VERB TO VIEW STATUS.
>70	COULD NOT FIND AN ECHO SERVER
>71	MONITOR VERB TERMINATED ON FATAL ERROR. USE DS VERB TO VIEW STATUS.

3.2 DATA LINK COMMANDS AND ERROR CODES

The following table assists you in the enterpretation of data output by the Test History (TH) verb. If you wish to use the Build Command (BC) verb to create a unique test, consult the EI300/EI990 Ethernet Interface Programming and ROM Code Listing for further information on the scope and function of data link commands.

Opcode	Command	Error Code	Error Description
>01	Read word	--	--
>02	Write word	--	--
>03	Move block	--	--
>07	Read EI Ethernet address	--	--
>08	Set Ethernet address	>81	Transmitter or receiver active
		>82	Error reported by 82586
>09	Configure 82586	>83	Transmitter or receiver active
		>84	Error reported by 82586
>0A	Select frame header fields	>85	Receiver active
		>86	Select count greater than 20
		>87	Select offsets not in ascending order
>0B	Set multicast address filter	>88	Transmitter or receiver active
		>89	Count greater than 20 addresses
		>8A	Error reported by 82586
>0C	Read status counters	>8B	Select count greater than available status
>0D	Enable receiver	--	--
>0E	Disable receiver	--	--
>0F	Start transmitter	>8C	Transmitter is active
		>8D	Null TDB list pointer
>10	Halt transmitter	--	--
>11	Enable timer	--	--
>12	Return to primitive	--	--

3.3 PRIMITIVE COMMANDS AND ERROR CODES

The following table assists you in the enterpretation of data output by the Test History (TH) verb. If you wish to use the Build Command (BC) verb to create a unique test, consult the EI300/EI990 Ethernet Interface Programming and ROM Code Listing for further information on the scope and function of primitive commands.

Opcode	Command
>01	Read word
>02	Write word
>03	Move block
>04	Self-test
>05	Jump subroutine
>06	ROM initial program load

Error Code	Type of Error
>80	TILINE time-out
>81	TILINE memory error
>82	EI DRAM parity error
>83	Invalid address detected
>84	Address error
>85	Unsupported exception vector

Crash Code	Type of Error
>91	Transmit buffer management error; no small buffers available
>92	Transmit buffer management error; no large buffers available

3.4 SELF-TESTS

Self-tests for the EI300 and the EI990 are identical. The asynchronous communication channels on the EI300 are not tested by the on-board self-test routines. However, they are checked by the S300/S300A computer power-up self-tests.

The table below lists the self-tests and the area that each self-test checks. The entries in the table that start with MF are maintenance functions that provide helpful services for diagnosing problems in the EI300 or EI990.

This table assists you in the enterpretation of data output by the Test History (TH) verb. If you wish to use the Build Command (BC) verb to create a unique test, consult the EI300/EI990 Ethernet Interface Programming and ROM Code Listing for further information on the scope and function of self-tests, and the error messages each test can return.

Test Number	Test Name	Test Description
>00	Self-test all	Performs all power-up tests
>01	EPROM checksum	Tests the firmware EPROMs
>02	RAM test #1	Tests DRAM for ability to hold data
>03	RAM test #2	Tests DRAM for addressing faults
>04	RAM test #3	Tests DRAM for pattern sensitivity
>05	PIT/interrupt-timer	Tests the parallel interface timer I/O, interrupt, and timer logic
>06	RAM test #4	Tests DRAM parity logic
>07	TILINE master W2, W3	Tests read/write of slave words 2 and 3
>08	TILINE master W0, W1	Tests read/write of slave words 0 and 1
>09	Programmer error	Tests programmer error detection logic
>0A	ID ROM checksum	Tests ID ROM data integrity
>0B	Ethernet controller (82586) self-test	Activates the Ethernet controller and checks its internal timers with an internal self-test

Test Number	Test Name	Test Description
>0C	Ethernet controller (82585) loopback	Loops back data at the Ethernet controller output; does not test the encoder/decoder
>0D	Encoder/decoder loopback and address reject (82501) test	Loops back data at the output of the encoder/decoder chip and tests the Ethernet controller's ability to reject addresses
>0E	Multicast receive (82586) test	Tests the Ethernet controller's ability to receive multicast messages
>0F	Ethernet controller CRC logic test (82586)	Tests the Ethernet controller's CRC generation and checking logic
>10	External loopback	Tests Ethernet communication offboard
MF80	82586 time domain reflectrometer test	Performs a time domain reflectrometer test on the Ethernet link
MF82	Ethernet primitive echo server	Provides an echo server for testing purposes
MF83	Ethernet primitive loop-on-transmit	Provides continuous transmission of packets
MF84	Ethernet primitive promiscuous receiver	Receives all packets and maintains information on them
MF85	82586 status dump function test	A maintenance function to dump the 82586 registers

The self-tests execute automatically when power is applied to the EI300 or EI990, or when either device is reset by the host. The self-tests can also be executed individually or all at once through the self-test ST verb, or the use of test 11 or test 31.

3.5 EI300/EI990 CONTROLLER COMMANDS

Value	Mnemonic	Description
CMD = >1	RW	Read a word through controller
CMD = >2	WW	Write a word through controller
CMD = >3	MB	Move block
CMD = >4	ST	Self-test command
CMD = >5	JS	Jump to subroutine
CMD = >6	IP	ROM initial program load
CMD = >7	RE	Read EI990 ID (address)
CMD = >8	SE	Set Ethernet address
CMD = >9	CC	Configure 82586 chip
CMD = >A	SH	Select frame header fields
CMD = >B	SM	Set multicast address filter
CMD = >C	SC	Read status counters
CMD = >D	ER	Enable receiver
CMD = >E	DR	Disable receiver
CMD = >F	SX	Start transmitter
CMD = >10	DX	Disable transmitter
CMD = >11	TM	Enable timer
CMD = >FF	BI	Buffer initialize command
CMD = >FE	BC	Buffer clear command
CMD = >FD	CB	Compare buffers command
CMD = >FC	M1	Master reset command
CMD = >FB	M2	Software reset command
CMD = >FA	CS	Check command status

3.6 TPCS INTERFACE

The host communicates with the Ethernet interface (EI) through four registers located in the host computer's peripheral control space (PCS). The PCS is an area of host memory dedicated to communicating with and controlling high-speed device controllers, such as the EI300 and the EI990. The four registers are called slave words. The slave word number (0 through 3) indicates the offset (in words) from the base address of the EI.

The host central processing unit (CPU) and the MC68000 microprocessor on the EI use the first two slave words (0 and 1) to synchronize communications between the two processors. Slave words 2 and 3 usually contain the TILINE address of data structures used to pass additional information between the two devices. In the primitive mode, the EI returns self-test status or error information to the host in slave words 2 and 3.

The following table shows the format of the slave words and defines the function of the bits in slave words 0 and 1.

Notice that the first eight bits (bits 0 through 7) in slave words 0 and 1 are identical. Bits 8 through 15 in slave words 0 and 1 are identical except that they are designated as channel A in slave word 0 and channel B in slave word 1. This feature provides two separate communication channels between the host computer and the EI. Communication channel A is via slave word 0, channel B is via slave word 1. In later discussions, channel A is referred to as the command channel and channel B is referred to as the receive channel.

In the discussion of the function of the slave word bits, to set a bit means to place the bit or function in its active or asserted state (logic 1). To clear or reset the bit means to deactivate or deassert the function (logic 0).

The host and the EI both access the slave words via the TILINE. The column labeled Read/Write in the following table indicates that the device accessing the bit via the TILINE is able to read or write the bit as indicated in the column.

WORD	BIT 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	IP	IE	IPA	IPB	PA	SWR	MR	STF	LGA	LMA	LRA	AFA	AMA	AFCA	ATA	ATRA
1	IP	IE	IPA	IPB	PA	SWR	MR	STF	LGB	LMB	LRB	AFB	AMB	AFCB	ATB	ATRB
2	msb	Most significant byte address pointer														lsb
3	msb	Least significant byte address pointer														lsb

Mnemonic	Bit Function	Read/Write	Active State
IP	Interrupt pending (any)	Read only	(1=Active)
IE	Interrupt enable (all)	Read/write	(1=Enable)
IPA	Interrupt pending A	Read only	(1=Active)
IPB	Interrupt pending B	Read only	(1=Active)
PA	Primitive attention	Read only	(1=Active)
SWR	Software reset	Read/set	(1=Active, set)
MR	Master reset	Read/set	(1=Active, set)
STF	Self-test failed/in progress	Read only	(1=Active/failed)
LGA	Lock granted A	Read only	(1=Granted)
LMA	Lock mask A	Read/write	(1=Enabled)
LRA	Lock request A	Read/write	(1=Requesting)
AFA	Attention from A	Read only	(1=Active)
AMA	Attention mask A	Read/write	(1=Enabled)
AFCA	Attention from clear A	Write (read=0)	(1=Clear AFA)
ATA	Attention to A	Read only	(1=Active)
ATRA	Attention to request A	Write (read=0)	(1=Set ATA)
LGB	Lock granted B	Read only	(1=Granted)
LMB	Lock mask B	Read/write	(1=Enabled)
LRB	Lock request B	Read/write	(1=Requesting)
AFB	Attention from B	Read only	(1=Active)
AMB	Attention mask B	Read/write	(1=Enabled)
AFCB	Attention from clear B	Write (read=0)	(1=Clear AFA)
ATB	Attention to B	Read only	(1=Active)
ATRB	Attention to request B	Write (read=0)	(1=Set ATB)

3.7 ADDITIONAL INFORMATION SOURCES

For complete descriptions and installation information on the EI300 and EI990, refer to the following manuals:

* EI300 Ethernet Interface Installation and Operation, part number 2232518-9701
* EI990 Ethernet Interface Installation and Operation, part number 2234392-9701
* EI990 Specification, part number 2239139-9701
* EI300/EI990 Interface Programming and ROM Code Listing, part number 2234394-9701

EXTACU

EXTERNAL AUTOCALL UNIT INTERFACE TEST

EXTERNAL AUTOCALL UNIT INTERFACE TEST (EXTACU)

EXTACU

External Autocall Unit Interface Test

1.1 INTRODUCTION

EXTACU, the External Autocall Unit Interface Test, performs fault isolation testing on the external autocall unit interface (EACUIF) module. It also verifies the correct operation of the autocall unit with the EACUIF.

1.2 TEST REQUIREMENTS

The following equipment is required to operate EXTACU:

* A Model 990 Computer with a minimum of 16K bytes of memory
* An EXTACU kit (part number 2263907-0001)
* A loopback connector (part number 2263478-0001)
* An interactive terminal
* A loading device

1.3 TEST CHARACTERISTICS

EXTACU operates under the control of DOCS. Refer to Volume 1 of the Unit Diagnostics Handbook for information about DOCS operation.

EXTACU consists of six parts:

Part	Title
1	CRU bit test
2	State sequencer test
3	PND, DSS, and ACR interrupt test
4	Internal clock test
5	EIA drivers and PWI interrupt test
DN	Dial number test

In addition to the verbs supplied by DOCS, EXTACU uses the following test execution verbs:

Test Execution Verb	Function
EA	Execute all parts
E1-E5	Execute parts 1 through 5 individually one time
LA	Loop continuously on all parts
L1-L5	Loop continuously on parts 1 through 5 individually
DN	Execute part DN
PE	Print error count

You can also use the Initialize Test (IT) verb to reinitialize the EXTACU initialization parameters.

2.1 TEST INITIALIZATION

EXTACU must be loaded and initialized by DOCS before you can begin testing. Volume 1 of the Unit Diagnostics Handbook explains the loading procedure. When DOCS has loaded the EXTACU module, the name and version of the test appears:

EXTACU-EXTERNAL AUTOCALL UNIT INTERFACE TEST VERSION # MM/YY XX

where:

MM is the month.

YY is the year.

XX is the revision letter.

Then DOCS executes the IT verb with the following prompts:

ENTER THE EXTACU CRU BASE ADDRESS D = 0080 -
Enter the EXTACU CRU base address. The default is 0080.

ENTER THE EXTACU INTERRUPT LEVEL D = 0C -
Enter the EXTACU interrupt level. The default is 0C.

ARE INTERRUPTS AVAILABLE? D = 1 -
If the interrupts are available, enter 1 (yes). Otherwise, enter 0 (no).

After you respond to the initialization prompts, DOCS displays the following prompt:

EXECUTE EA VERB? (DEF=1) -

If you accept the default (yes), parts 1 through 5 execute.

NOTE

If you enter 1 in response to the EXECUTE EA VERB? prompt, be sure that the loopback test connector is not installed while parts 1 through 4 execute. The loopback test connector must only be installed during execution of part 5.

If you enter 0 (no) in response to the EXECUTE EA VERB? prompt, the following prompt is displayed:

```
VERB? -
```

You can then execute any part of EXTACU by entering the appropriate test verb.

If errors occur during a test, you should reexecute the test. Use the appropriate verb to determine the cause of the errors. The following messages appear when EXTACU executes without errors:

```
PART 1 START
PART 1 DONE

PART 2 START
PART 2 DONE

PART 3 START
PART 3 DONE

PART 4 START
PART 4 DONE

PART 5 START
PART 5 DONE
```

2.2 TEST VERBS

EXTACU contains the following test verbs:

Test Execution Verb	Function
EA	Execute all parts
E1-E5	Execute parts 1 through 5 individually one time
LA	Loop continuously on all parts
L1-L5	Loop continuously on parts 1 through 5 individually
DN	Execute part DN
PE	Print error count

You can also use the IT verb to reinitialize the EXTACU initialization parameters. The following paragraphs discuss the test verbs.

2.2.1 Execute All Parts (EA) Verb

The EA verb executes parts 1 through 5 consecutively one time.

2.2.2 Execute Parts 1 Through 5 Individually One Time (E1-E5) Verbs

The E1 through E5 verbs execute parts 1 through 5 individually. The selected test is executed one time. Disconnect the EACUIF from the autocall unit before executing any of these verbs.

2.2.3 Loop Continuously on All Parts (LA) Verb

The LA verb causes continuous execution of parts 1 through 4 consecutively. Part 5 is not included in the LA verb execution because it requires the installation of a loopback connector. Parts 1 through 4 cannot execute with this connector installed.

The LA verb displays the loop count after each execution of the four parts is completed. To halt execution of this verb, press the @ key. Disconnect the EACUIF from the autocall unit before executing the LA verb.

2.2.4 Loop Continuously on Parts 1 Through 5 Individually (L1-L5) Verbs

The L1 through L5 verbs cause parts 1 through 5 to execute individually and continuously until you press the @ key. The loop count is displayed after the completion of each loop. Disconnect the EACUIF from the autocall unit before executing any of these verbs.

2.2.5 Execute Part DN (DN) Verb

The DN verb executes part DN of the EXTACU test, which dials a phone number using the EACUIF board and the autocall unit. Refer to the DN test description for instructions on executing part DN.

2.2.6 Print Error Count (PE) Verb

The PE verb prints the current error count and can be used to determine the number of errors that occurred during execution of the last verb. The output from the PE verb is as follows:

```
ERROR COUNT = XXXX
```

where:

XXXX represents the number of errors.

2.3 TEST DESCRIPTIONS

EXTACU consists of six parts:

Part	Title
1	CRU bit test
2	State sequencer test
3	PND, DSS, and ACR interrupt test
4	Internal clock test
5	EIA drivers and PWI interrupt test
DN	Dial number test

The following paragraphs describe each test.

2.3.1 Part 1 -- CRU Bit Test

Part 1 verifies the latch and reset capabilities of CRU output bits 1, 2, 3, 4, 5, 8, 9, A, and D and CRU input bits 1, 2, 3, 6, 7, and E.

2.3.2 Part 2 -- State Sequencer Test

Part 2 tests the state sequencer circuitry by performing the following functions:

1. Takes over control of the internal clock
2. Places the unit in test mode
3. Steps through the sequences
4. Checks for the proper outputs at each step

2.3.3 Part 3 -- PND, DSS, and ACR Interrupt Test

Part 3 is executed if you indicated during test initialization that interrupts are available. It performs the following functions:

1. Checks for the proper occurrence of the present next digit (PND), data set status (DSS), and abandon call and retry (ACR) interrupts.
2. Ensures that these interrupts do not occur unless the proper enabling signals are present.
3. Verifies that each interrupt can be reset by the appropriate signals.

2.3.4 Part 4 -- Internal Clock Test

Part 4 exercises the state sequencer using the internal clock of the EACUIF board.

2.3.5 Part 5 -- EIA Drivers and PWI Interrupt Test

Part 5 tests the EACUIF line drivers and receivers. It also checks the power indication (PWI) interrupt provided that you indicated during test initialization that interrupts are available. When you execute part 5, the test asks if a loopback connector, which is required to execute the test, is installed:

```
IS LOOPBACK CONNECTOR INSTALLED (DEF = 0)?
```

You must respond to this prompt by entering 1 (yes).

2.3.6 Part DN - Dial Number Test

Part DN exercises the EACUIF with the autocall unit by dialing a telephone number that you enter. You can specify a local or long-distance telephone number. The EACUIF must be connected to the autocall unit. When you execute part DN, the following instructions are displayed:

```
PART DN START

ENTER THE NUMBER YOU WISH TO DIAL.  YOU ARE RESTRICTED
TO 22 (BASE 10) CHARACTERS.  THE FOLLOWING ARE THE ONLY
          VALID ONES:

THE DIGITS 0 - 9
D (WAITS FOR SECOND DIAL TONE)
C (DOES NOT WAIT FOR COMPUTER TO ANSWER)
- (A DASH HAS NO AFFECT)
X NUMBER TERMINATOR MUST BE LAST CHARACTER
BEFORE CARRIAGE RETURN.
```

A maximum of 22 characters can be entered. The last character entered must be X. For example, a local telephone number would be entered as follows:

```
555-6278X
```

Part DN is a functional test only. It provides no fault isolation information, however, it does indicate whether the unit as a whole is operational.

3.1 ERROR MESSAGES

The following errors can occur during execution of EXTACU. The messages are self-explanatory and indicate the type of error and the circuitry that is probably at fault. A corresponding error number is also displayed on the computer front panel. The first digit indicates in which part the error occurred. For example, error 14 occurs during execution of part 1.

Error Number	Error Message
11	1-1 FAILED TO GENERATE A CLEAR WHEN COMPCLR WAS SET HIGH. CHECK THE CLEAR (COMPCLR) CKTRY. EXPECTED CRU = 0000 RECEIVED CRU = XXXX
12	1-2 FAILED TO GENERATE A CLOCK PULSE WHEN COMPCLK SET HIGH. CHECK THE EXTERNAL CLOCK (COMPCLK) CKTRY. EXPECTED CRU = 1000 RECEIVED CRU = XXXX
13	1-3 CLOCK FAILED TO RESET WHEN COMPCLK WAS CLEARED. CHECK THE EXTERNAL CLOCK (COMPCLK) CKTRY. EXPECTED CRU = 0000 RECEIVED CRU = XXXX
14	1-4 FAILED TO GO INTO THE TEST MODE WHEN THE TEST BIT WAS SET. CHECK THE TEST (TEST) CKTRY. EXPECTED CRU = 4000 RECEIVED CRU = XXXX
15	1-5 SYSTEM STAYED IN THE TEST MODE WHEN THE TEST BIT WAS RESET. CHECK THE TEST (TEST) CKTRY. EXPECTED CRU = 0000 RECEIVED CRU = XXXX
16	1-6 FAILED TO GENERATE DIGIT PRESENT (INPUT BIT 6) WHEN DPR BIT WAS SET. CHECK THE DIGIT PRESENT (DPR) CKTRY. EXPECTED CRU = 0040 RECEIVED CRU = XXXX

Error Number	Error Message
17	1-7 FAILED TO CLEAR DIGIT PRESENT (INPUT BIT 6) WHEN DPR BIT WAS RESET. CHECK THE DIGIT PRESENT (DPR) CKTRY. EXPECTED CRU = 0000 RECEIVED CRU = XXXX
18	1-8 FAILED TO GENERATE CALL REQUEST (INPUT BIT 7) WHEN CRQ BIT SET. CHECK THE CALL REQUEST (CRQ) CKTRY. EXPECTED CRU = 0080 RECEIVED CRU = XXXX
19	1-9 FAILED TO CLEAR CALL REQUEST (INPUT BIT 7) WHEN CRQ BIT RESET. CHECK THE CALL REQUEST (CRQ) CKTRY. EXPECTED CRU = 0000 RECEIVED CRU = XXXX
1A	1-A FAILED TO SET CRU INPUT BIT X (IN THE TEST MODE) WHEN OUTPUT BIT X WAS SET. CHECK THE TEST CKTRY AND APPROPRIATE SIGNALS: ANB2 (BIT 1), ANB4 (BIT 2), ANB8 (BIT 3) EXPECTED CRU = XXXX RECEIVED CRU = XXXX
1B	1-B FAILED TO RESET CRU INPUT BIT X (IN THE TEST MODE) WHEN OUTPUT BIT X RESET. CHECK THE TEST CKTRY AND APPROPRIATE SIGNALS: ANB2 (BIT 1), ANB4 (BIT 2), ANB8 (BIT 3) EXPECTED CRU = XXXX RECEIVED CRU = XXXX
1C	1-C FAILURE IN CRU COMMUNICATIONS. CHECK CRU CKTRY. EXPECTED CRU = XXXX RECEIVED CRU = XXXX
21	2-1 COUNTER ENABLE WAS NOT SET AT THE PROPER TIME. FAILURE IN THE COUNTER ENABLE (CCTEN) CKTRY. SEQUENCE COUNTER IS IN STATE X EXPT STATE IS X.
22	2-2 COUNTER ENABLE WAS SET AT THE WRONG TIME. FAILURE IN THE COUNTER ENABLE (CCTEN) CKTRY. SEQUENCE COUNTER IS IN STATE X EXPT STATE IS X.

Error Number	Error Message
23	2-3 STATE SEQUENCER FAILED TO STEP TO EXPT COUNT. CHECK COUNTER FOR PROPER OPERATION. SEQUENCE COUNTER IS AT STATE X EXPT STATE IS X.
24	2-4 PNDSTAT WAS NOT SET AT THE PROPER TIME. CHECK THE PNDSTAT CKTRY. SEQUENCE COUNTER IS IN STATE X EXPT STATE IS X.
25	2-5 PNDSTAT WAS SET AT WRONG TIME. CHECK THE PNDSTAT CKTRY. SEQUENCE COUNTER IS AT STATE X EXPT STATE IS X.
26	2-6 FAILED TO RESET DIGIT PRESENT AT STATE 6 OF THE STATE SEQUENCER. CHECK DIGIT (DPR & BDPR) CKTRY.
31	3-1 FAILED TO RECEIVE PND INT. WHEN EXPECTED. CHECK PND INTERRUPT CKTRY.
32	3-2 FAILED TO RESET PND INT WITH SIGNAL X SIGNALS: 0 = DPR SET 1 = PNDINT RESET 2 = I/O RESET GENERATED 3 = COMPCLR SET 4 = CALL REQUEST LOW 5 = INT ON/OFF OFF
33	3-3 FAILED TO RECEIVE A DSS INT WHEN EXPECTED. CHECK DSS INTERRUPT CKTRY.
34	3-4 FAILED TO RECEIVE AN DSS INT WHEN EXPECTED. CHECK ACR INTERRUPT CKTRY.
35	3-5 FAILED TO RESET DSS INT WITH SIGNAL X. SIGNALS: 0 = DPR SET 1 = PNDINT RESET 2 = I/O RESET GENERATED 3 = COMPCLR SET 4 = CALL REQUEST LOW 5 = INT ON/OFF OFF

Error Number	Error Message
36	3-6 FAILED TO RESET ACR INT WITH SIGNAL X. SIGNALS: 0 = DPR SET 1 = PNDINT RESET 2 = I/O RESET GENERATED 3 = COMPCLR SET 4 = CALL REQUEST LOW 5 = INT ON/OFF OFF
37	3-7 GENERATED A PND INT. WITH PND INT ENABLE LOW.
41	4-1 SEQUENCER FAILED TO COUNT ON INTERNAL CLOCK. CHECK THE EXTACU INTERNAL CLOCK CKTRY (CLOCKA).
51	5-1 FAILED LOOPBACK ON SIGNAL NBX. FAILURE IN LINE DRIVER/RECEIVER CKTRY.
52	5-2 FAILED TO LOOPBACK ON SIGNAL DPR. FAILURE IN LINE DRIVER/RECEIVER CKTRY.
53	5-3 FAILED TO LOOPBACK ON SIGNAL CRQ FAILURE IN LINE DRIVER/RECEIVER CKTRY.
54	5-4 FAILED TO RECEIVE A PWI INTERRUPT WHEN EXPECTED. CHECK PWI INTERRUPT CKTRY.
55	5-5 FAILED TO RESET PWI INT WITH SIGNAL X SIGNALS: 0 = DPR SET 1 = PNDINT RESET 2 = I/O RESET GENERATED 3 = COMPCLR SET 4 = CALL REQUEST LOW 5 = INT ON/OFF OFF
56	5-6 GENERATED A PWI INT WITH SIGNAL PWI INT DISABLE SET. CHECK THE PWI INT CKTRY.

FC3TST

FOUR-CHANNEL COMMUNICATIONS CONTROLLER TEST

FOUR-CHANNEL COMMUNICATIONS CONTROLLER TEST (FC3TST)

FC3TST

Four-Channel Communications Controller Test

1.1 INTRODUCTION

FC3TST, the Four-Channel Communications Controller Test, verifies the correct operation of the Four-Channel Communications Controller (FCCC) by utilizing the FCCC on-board self-test and communications software. The test isolates any hardware faults to the field-replaceable integrated circuit or section of logic causing errors. It also provides software tools to assist in the installation and verification of Texas Instruments-supplied modems and data access arrangements (DAAs).

FC3TST is a series of numbered tests, with each test using the logic tested by its predecessors so that as little untested hardware as possible is used in each test. When the tests are executed in consecutive order, the FCCC hardware is tested working from the systems TILINE interface to and including the communications channels (0 through 3) EIA interfaces. Additional tests exercise each communication channel at its maximum data transfer rate.

1.2 TEST REQUIREMENTS

The following equipment is required to operate the FC3TST test:

* A Model 990 Computer with a minimum of 64K bytes of memory
* A Four-Channel Communications Controller (part number 2263882)
* An interactive terminal
* A device to load the test module

The following equipment is optional:

* A loopback connector (part number 948550-0001 *C)
* A test cable (part number 2265161 **)
* A TI internal modem

1.3 TEST CHARACTERISTICS

The FC3TST test has certain characteristics that you should know before operating the test:

* FC3TST operates under the control of DOCS. Information about DOCS operation can be found in Volume 1 of this handbook.
* A variety of external equipment may be connected to each channel of the FCCC to increase testing capability, including:
  - A loopback connector
  - A channel-to-channel cable
  - An asynchronous modem
  - A synchronous modem

  A channel may also be tested with no external equipment. Certain tests are not executable in certain equipment configurations. Those tests that cannot be performed are skipped, with a message so indicating.
* FC3TST consists of 22 tests and is structured so that you can run either the complete set of tests or any separate test. These tests are as follows:

Test	Title
1	Self-Test
2	Self-Test
3	Slave Words Test
4	TILINE Master Test
5	TILINE Data Test
6	TILINE Address Test
7	Internal Synchronous Test
8	Internal Asynchronous Test
9	Internal BOP Test
A	Internal BOP NRZI Test
B	Modem Control Test

Test	Title
C	EIA Data Synchronous Test
D	EIA Data Asynchronous Test
E	EIA Data BOP Test
F	EIA Data BOP NRZI Test
10	Local Line Test
11	Max Rate 0 Test
12	Max Rate 1 Test
13	Max Rate 2 Test
14	Max Rate 3 Test
15	FDX EIA Test
16	HDX Local Line Test

* FC3TST uses a number of test verbs, or commands, to execute various parts and functions of the test. These verbs are as follows:

Verb	Function
IT	Initialize test
EA	Execute all tests one time
ET	Execute an individual test one time
LT	Loop continuously on an individual test
LA	Loop continuously on all tests
DS	Display status
PE	Display error count
TD	Test DAA
RC	Read FCCC channel interface status
WC	Write FCCC channel interface
RD	FCCC ROM release data
ID	Read FCCC ID switches
TH	Test history
MX	Monitor connector exercise
PV	Print verbs

2.1 TEST EXECUTION

The FC3TST module must be loaded and initialized by DOCS before execution can begin.

2.2 LOADING

The loading procedure is explained in Section 3 of Volume 1.

2.3 INITIALIZATION

When DOCS loads the test module, it outputs the name and version of the test:

```
FC3TST
FOUR CHANNEL COMMUNICATIONS CONTROLLER DIAGNOSTIC
VERSION = **  MM/YY
```

Then DOCS executes the initialize test (IT) verb by asking you the following questions. If the default value shown with each question is correct, press the RETURN key. If not, enter the correct value. The value that you enter becomes the default for the next execution of the test.

```
ENTER FCCC TILINE ADDRESS: (DEF = XXXX)

ENTER FCCC INTERRUPT LEVEL: ( DEF = X)

CHANNEL TEST CONFIGURATION, CHANNEL 0
  0=NO CONNECTOR(IN), 1=LOOPBACK CONNECTOR(DI),
  2=CHAN TO CHAN CABLE(DI), 3=SYNC MDM(AL), 4=ASYNC MDM(AL)
(DEF = X)
```

IN represents internal loopback mode, DI represents digital loopback mode, and AL represents analog loopback mode. Refer to Appendix B for an illustration of the portions of the system that are tested in each test mode.

```
CHANNEL TEST CONFIGURATION CHANNEL 1
(DEF = X)
CHANNEL TEST CONFIGURATION CHANNEL 2
(DEF = X)
CHANNEL TEST CONFIGURATION CHANNEL 3
(DEF = X)

DO YOU WANT TO RUN THE TEST WITH INTERRUPTS? (DEF = X)

ENTER COMPUTER LINE FREQ: ( 0=50, 1=60 DEF = X)
```

When you have answered the initialization questions, DOCS asks if you want to execute the entire FC3TST test:

```
EXECUTE EA VERB? (DEF = 1)
```

If you enter a 1 (yes), all parts of FC3TST that may be run in the test mode that you have selected are executed If any error messages are output, it is recommended that you run the test or tests that indicate errors and use any of the appropriate verbs to

determine their cause.

The following is an example of the messages output when the EA verb executes without errors:

```
TEST 01 SELFTEST STARTED BY TILINE I/O RESET
TEST 01 COMPLETE
TEST 02 SELFTEST STARTED BY WRITE TO SLAVE WORD ZERO
TEST 02 COMPLETE
TEST 03 FCCC TILINE SLAVE WORD DATA TEST
TEST 03 COMPLETE
TEST 04 LOW LEVEL TILINE MASTER TEST
TEST 04 COMPLETE
TEST 05 TILINE MASTER DATA TRANSFER TEST
TEST 05 COMPLETE
TEST 06 TILINE MASTER ADDRESSING TEST
TEST 06 COMPLETE
TEST 07 9903 INTERNAL LOOPBACK SYNC MODE
TESTING  0  1  2  3
TEST 07 COMPLETE
TEST 08 9903 INTERNAL LOOPBACK ASYNC MODE
TESTING  0  1  2  3
TEST 08 COMPLETE
TEST 09 9903 INTERNAL LOOPBACK BOP MODE
TESTING  0  1  2  3
TEST 09 COMPLETE
TEST 0A 9903 INTERNAL LOOPBACK BOP NRZI MODE
TESTING  0  1  2  3
TEST 0A COMPLETE
TEST 0B EIA MODEM CONTROL
TESTING  0  1  2  3
TEST 0B COMPLETE
TEST 0C CHANNEL DATA TEST SYNC MODE
TESTING  0  1  2  3
TEST 0C COMPLETE
TEST 0D CHANNEL DATA TEST ASYNC MODE
TESTING  0  1  2  3
TEST 0D COMPLETE
TEST 0E CHANNEL DATA TEST BOP MODE
TESTING  0  1  2  3
TEST 0E COMPLETE
TEST 0F CHANNEL DATA TEST BOP NRZI MODE
TESTING  0  1  2  3
TEST 0F COMPLETE
TEST 11 CHANNEL 0 MAX RAT BOP
TEST 11 COMPLETE
TEST 12 CHANNEL 1 MAX RATE BOP
TEST 12 COMPLETE
TEST 13 CHANNEL 2 MAX RATE BOP
TEST 13 COMPLETE
TEST 14 CHANNEL 3 MAX RATE BOP
TEST 14 COMPLETE
TEST 15 CHANNEL TO CHANNEL EIA FDX BOP
```

```
TEST 15 COMPLETE
TEST 16 CHANNEL TO CHANNEL LOCAL LINE HDX BOP NRZT
TEST 16 COMPLETE
```

If you respond with a 0 (no) to the question EXECUTE EA VERB?, DOCS outputs the following question:

```
VERB? -
```

You may then execute any DOCS or FC3TST test verb. If you later want to alter any of the initialization parameters, reexecute the IT verb.

2.4 TEST VERBS

Whenever DOCS outputs the question VERB?, you may enter IT, EA, or any of the FC3TST test verbs, which are discussed in the following paragraphs. To receive the question VERB?, press the @, CMD, HELP, or ESC key.

NOTE

When a verb or test is aborted abnormally, such as when you are using the @ key, FC3TST outputs the message TEST ABORTED. At this time, the state of the FCCC is unknown and no further tests may be run without properly restarting the controller. To restart, run tests 2, 3, 4, and 5 consecutively.

2.4.1 ET Verb

The ET verb executes an individual test that you select one time. When you enter this verb, the test asks you to enter the number of the test to be performed:

```
TEST #
```

2.4.2 LT Verb

The LT verb causes an individual test that you select to be executed continuously. When you enter the verb, it outputs the message TEST #, indicating that you should enter the number of the test you want to run. The loop count, or number of times the test

has executed, and the number of errors detected is output to the computer front panel lights as the LT verb executes. To halt execution, press the @, CMD, HELP, or ESC key.

2.4.3 LA Verb

The LA verb causes the continuous execution of the entire FC3TST test. (Some tests may be omitted, depending on the test environment.) The loop count is continuously displayed on the front panel and the loop and error counts are output to the interactive terminal after each execution of the entire FC3TST test. To halt execution of the LA verb, press the @, CMD, HELP, or ESC key.

2.4.4 DS Verb

The DS verb outputs the status of the FCCC. The following example illustrates the output from this verb, with AAAA, BBBB, CCCC, and DDDD representing the status words read from the FCCC TILINE slave words. (Consult the FCCC Installation and Operation Manual for definitions of the bits.)

```
FCCC STATUS:
ROSW0  ROSW1  ROSW2  ROSW3
AAAA   BBBB   CCCC   DDDD
```

2.4.5 PE Verb

The PE verb outputs the current error count in the following format:

```
ERRORS = XXXX.
```

2.4.6 TD Verb

The TD verb monitors the modem signal RING indicator for an incoming call. When you execute this verb, the test instructs you to select a channel:

```
ENTER CHANNEL NUMBER TO ANSWER ( DEF =X)
```

A message is output every 10 seconds to notify you that the signal is being monitored:

```
..WAITING FOR RING SIGNAL FROM MODEM..
```

When the RING signal is received, DTR is set on the selected FCCC channel and the following message is output:

```
* * RING RECEIVED!  DTR NOW SET.

BEGIN 10 SEC WAIT FOR DSR.
```

The presence of DTR causes the modem DAA pair to answer the incoming call, transmit the answer-back tone (approximately 2.5 seconds), and set DSR. If DSR is received from the modem within 10 seconds, the following message is output and the verb completes execution:

```
DTR RESET TO DISCONNECT LINE
```

If DSR is not detected, the following message is output:

```
*** TIMEOUT ERROR! DSR NOT SET.
```

2.4.7 RC Verb

The RC verb reads the status of the channel that you select when you respond to the following message:

```
READ CHANNEL INTERFACE
CHANNEL ID (0 TO 3) -
```

It then displays the status of the available modem interface signals in the following message (an X indicates that the signal is true):

DCD	SDCD	RING	LLEN	CTS	DSR
	X			X	

The RC verb should be run only after tests 2, 3, 4, and 5 have been executed consecutively.

2.4.8 WC Verb

The WC verb enables you to modify all control bits associated with an FCCC communications channel. The verb should be run only after tests 2, 3, 4, and 5 have been executed consecutively. When you execute this verb, the following parameters must be established:

```
CHANNEL NUMBER (0 TO 3) X -
```

```
BIT RATE SELECT (0 TO F) X -

TRANSMIT CLOCK SELECT X -

RECEIVE CLOCK SELECT X -

AUDIO MONITOR (PIN 18) X -

NEW SYNC (PIN 14) X -

DATA TERMINAL READY (PIN 20) X -

SECONDARY REQUEST TO SEND (PIN 11 & 19) X -

ANALOG LOOPBACK (PIN 13) X -

ANALOG LOOPBACK (PIN 25) X -

SELECT FULL DUPLEX X -

SELECT LOCAL LINE (DXS) X -

REQUEST TO SEND (PIN 4) X -

**** MONITOR CONNECTOR P7 ****

TRANSMIT ACTIVE X -

RECEIVER SYNC DETECT X -

RECEIVER ERROR X -

HOST ERROR X -
```

The WC verb uses this data to construct a command that it issues to the FCCC to write the selected channel interface.

2.4.9 RD Verb

The RD verb displays the release date stored in the FCCC ROM. This verb should be run only after tests 2, 3, 4, and 5 have been executed consecutively. In the following format for this verb, YY represents the year and JJJ the Julian date for the ROM:

```
READ FCCC ROM RELEASE DATE

ROM DATE = YY.JJJ
```

2.4.10 ID Verb

The ID verb displays the FCCC ID switches in the following format:

```
READ FCCC ID SWITCHES:

ID = XX.
```

The ID verb should be run only after tests 2, 3, 4, and 5 have been executed consecutively.

2.4.11 TH Verb

The TH verb allows you to review all commands that have been processed during testing at the completion of any numbered test. The verb records the commands and the status returned by the FCCC for each commmand. This information is helpful in troubleshooting the FCCC firmware and in determining the cause of errors.

When you execute the TH verb, the test asks if the test history should be printed. If you selected the print option during DOCS initialization and the error message terminal is a printer, the complete history of the last test performed is printed. If you have not selected the print option, each test command block (TCB) is displayed on the interactive terminal. Press RETURN to scroll to the next TCB.

There are several classes of TCBs; each is displayed in an appropriate format. All TCBs have four words of overhead that are displayed at the beginning of each TCB format. The command code of the TCB is expanded on the next line of the display. The test driver control commands are displayed in the following format:

```
TCB ADDRESS = qqqq     TCB LINK WORDS = rrrr  ssss

TCB COMMAND = tttt     TCB STATUS = uuuu

(The TCB command code is expanded on this line.)
```

Commands that initialize or compare test data buffers display part of the buffer in addition to other information associated with the command.

The FCCC has two command formats: commands with buffers (long commands) and those without buffers (short commands). There are two forms of short commands. The first is a normal short command in which the returned status conforms to a standard by which all FCCC slave words are returned unchanged. Slave word 0 is an exception: this word has a status bit indicating proper completion of the command. FCCC short commands are displayed in

the following format:

```
TIME OUT = xxxx   REMAINING TIME = yyyy

FCCC COMMAND        W0     W1     W2     W3

COMMAND ISSUED      aaaa   aaaa   aaaa   aaaa

STATUS RETURNED     bbbb   bbbb   bbbb   bbbb
```

The second FCCC short command format is used for commands where the status returned is expected to be special data. This information accompanies the information displayed in the preceding format and appears as follows:

```
STATUS MASK         cccc   cccc   cccc   cccc

STATUS EXPECTED     dddd   dddd   dddd   dddd
```

The FCCC long commands that have an associated buffer use the same display format as the short command in addition to the following information:

```
BUFFER HEADER

ISSUED              eeee   eeee   eeee   eeee

RETURNED            ffff   ffff   ffff   ffff
```

The field TCB address qqqq is the address of the TCB in memory. The fields rrrr and ssss are pointers to other TCBs used in the test. Field rrrr is a pointer to the next TCB; field ssss points to the previous TCB. TCB status field uuuu is 0 if no error was reported by the TCB. When TCB is nonzero, an error is associated with the TCB. Each TCB that contains a command for the FCCC has a time-out xxxx, which is copied and decremented each clock tick (8.33 ms for a 60 Hz line frequency and 10.0 ms for 50 Hz). When the command is complete, the decremented copy is displayed as time remaining. All other TCB bit definitions are contained in the FCCC Installation and Operation Manual.

If the TCB status field is nonzero during execution of the TH verb, the following message is output:

```
* * * * * *  ERROR IN THIS TCB * * * * * *
```

The message is accompanied by the status returned and status expected from the bits that were tested, and the FCCC command that was issued.

2.4.12 MX Verb

The MX verb uses the special test interface board (STIB) of the Technical Evaluation System (TES) to test the outputs of the FCCC monitor connector (P7). If the test detects an error, the following message is output:

MONITOR CONNECTOR OUTPUT ERROR

NOTE

The MX verb can be used only when the FCCC under test is installed in a TES or FVS test system.

2.4.13 PV Verb

The PV verb outputs a list of the FC3TST test verbs.

2.5 TEST DESCRIPTIONS

The FC3TST consists of 22 tests, which are listed in the following table along with the configuration necessary to execute each test.

Tests that exercise a communications channel execute only if the channel is properly configured (with loopback connectors in place, etc.). When multiple channels are configured alike they are tested concurrently. If no channel is in the required configuration, the test is skipped.

The entire FC3TST test executes in less than one minute. Execution times for individual tests vary, depending on the equipment configuration.

Test	Title	TMS 9903	Loop Back	Sync Modem	Async Modem	Chan Cable
1	Self-Test	X	X	X	X	X
2	Self-Test	X	X	X	X	X
3	Slave Words Test	X	X	X	X	X
4	TILINE Master Test	X	X	X	X	X
5	TILINE Data Test	X	X	X	X	X
6	TILINE Address Test	X	X	X	X	X
7	Internal Sync. Test	REQ	X	X	X	X
8	Internal Async. Test	REQ	X	X	X	X
9	Internal BOP	REQ	X	X	X	X
A	Internal BOP NRZI	REQ	X	X	X	X

Test	Title	TMS 9903	Loop Back	Sync Modem	Async Modem	Chan Cable
B	Modem Control Test	REQ	REQ	SKP	SKP	SKP
C	EIA Data Sync. Test	REQ	OPT	OPT	SKP	SKP
D	EIA Data Async. Test	REQ	OPT	SKP	OPT	SKP
E	EIA Data BOP Test	REQ	OPT	OPT	SKP	SKP
F	EIA Data BOP NRZI	REQ	OPT	SKP	OPT	SKP
10	Local Line Test	REQ	REQ	SKP	SKP	SKP
11	Max Rate 0 Test	REQ	REQ	SKP	SKP	SKP
12	Max Rate 1 Test	REQ	REQ	SKP	SKP	SKP
13	Max Rate 2 Test	REQ	REQ	SKP	SKP	SKP
14	Max Rate 3 Test	REQ	REQ	SKP	SKP	SKP
15	FDX EIA Test	REQ	SKP	SKP	SKP	REQ
16	HDX Local Line Test	REQ	SKP	SKP	SKP	REQ

REQ -- Required for test SKP -- Test is skipped
X -- No effect on test OPT -- Option (one is required)

2.5.1 Test 1 -- Self-Test Started by TILINE I/O Reset

Test 1 monitors the operation of the FCCC self-test that is initiated by a TILINE I/O reset. When errors are reported by the firmware, test 1 outputs an error message along with a list of possible causes. The following logic blocks or field replaceable components are tested during the execution of test 1:

1. FCCC slave address logic
2. TMS 9900 microprocessor
3. TMS 2532 EPROMS (four) or TMS 4732 mask ROMS (four)
4. TMS 4116 dynamic RAMs (17)
5. TMS 9901 programmable systems interface
6. TMS 9903 synchronous communications controllers (four)

2.5.2 Test 2 -- Self-Test Started by Write to Slave Word Zero

Test 2 monitors the FCCC self-test that is initiated by a write to slave word zero. The primary purpose of this test is to verify the operation of the initiate-master-reset logic. Test 2 begins the FCCC self-test by setting the initiate-master-reset bit (ROSW 0, bit 1). After the self-test has started, test 2 repeats test 1. The primary targets of test 2 are as follows:

1. Slave word addressing logic
2. Slave word write logic
3. All logic and components checked during test 1

2.5.3 Test 3 -- FCCC TILINE Slave Word Data Test

Test 3 verifies the capability of the FCCC to transfer data to and from the FCCC TILINE slave words. Test patterns are written to slave words 1 and 2 and an illegal command is written to slave word 3. The FCCC firmware echos these three words with illegal command status in TILINE slave word zero. This data is read from the slave words and verified. The following blocks of logic are tested by test 3:

1. TILINE data logic
2. TILINE slave word addressing logic

2.5.4 Test 4 -- Low-Level TILINE Master Test

Test 4 is a short test of the ability of the FCCC to read and write to TILINE memory. Each FCCC master channel first transfers four words of data (>AAAA, >5555, >FFFF, >0000) to TILINE memory. The data is then read and compared by the FCCC firmware. Test 4 verifies the operation of the following:

1. TILINE master logic
2. TILINE data logic
3. TILINE addressing logic

2.5.5 Test 5 -- TILINE Master Data Transfer Test

Test 5 writes 256 bytes of data to the FCCC dynamic RAM using the download procedure. The data is transferred back to the host and

compared to the original buffer for any errors that may have occurred. Test 5 checks the following:

1. TILINE master data paths
2. Least significant bits of TILINE address
3. FCCC dynamic RAM

2.5.6 Test 6 -- TILINE Master Addressing Test

Test 6 verifies the integrity of every 8K-byte block in memory past the end of the FC3TST test. For each block of memory, it attempts an 8K-byte data transfer using the FCCC TILINE master controller. If the CPU has determined that an eight-byte block of memory is present, status of the controller is checked and the 8K bytes of transferred data is compared. If the CPU finds that no 8K-byte block of memory is present, the returned status is checked for a TILINE time-out. Test 6 verifies the correct operation of the following:

1. TILINE addressing logic
2. TILINE data logic

2.5.7 Test 7 -- 9903 Internal Loopback Synchronous Mode Test

Test 7 places the TMS9903s on all four channels in internal loopback mode unless they failed the self-test earlier. In this test, synchronous data is transmitted through the TMS9903s on all four channels in loopback mode. The targets of test 7 are as follows:

1. The TMS9903 synchronous communications controllers for channels 0 through 3
2. All FCCC logic

2.5.8 Test 8 -- 9903 Internal Loopback Asynchronous Mode Test

Test 8 is identical to test 7, except that asynchronous data is transmitted.

2.5.9 Test 9 -- 9903 Internal Loopback BOP Mode Test

Test 9 is identical to test 7 except that BOP data is transmitted.

2.5.10 Test A -- 9903 Internal Loopback BOP NRZI Mode Test

Test A is identical to test 7 except BOP NRZI data is transmitted.

2.5.11 Test B -- EIA Modem Control Signal Test

Test B verifies the proper operation of the EIA modem controls. A loopback connector must be installed on the communications interface connector (P3 through P6) for the channels to be tested. This test sets a particular modem control lead, checks the looped back signal to verify that it is on, and checks all other modem leads to ensure that they are not affected. There are three EIA outputs that are not looped back. The loopback connector has a pair of LEDs (one green and one red) for each of these signals. At the beginning of test B all green LEDs are on. To test these signals, you must observe the following:

1. All red LEDs are ON.
2. Only the red LED marked AL on the test connector is ON.
3. Only the red LED marked AM on the test connector is ON.
4. Only the red LED marked CD on the test connector is ON.
5. All green LEDs are ON.

NOTE

The EIA clocks and data signals are not checked in this test but are checked in test C.

The primary targets of test B are as follows:

1. The EIA drivers and receivers
2. The CRU decode logic

2.5.12 Test C -- EIA Channel Data Path Synchronous Mode Test

Using an external modem (in analog loopback mode) or a loopback connector, test C transfers a 256-byte block of data full-duplex on all selected channels simultaneously. If the channel is connected to a modem, the bit rate is set by that modem. Those channels using loopback connectors select a 4800-bps internal bit rate clock. At the completion of the data transfer, the receiving buffers are compared to the transmit buffers. Test C verifies the operation of the following:

1. TMS 9903 data input and output
2. TMS 9903 data clocks and control input/output
3. EIA drivers and receivers for the modem clocks and transmit and receive data

NOTE

The EIA transmit clock receiver is tested only when a synchronous modem or modem eliminator is used.

2.5.13 Test D -- EIA Channel Data Path Asynchronous Mode Test

Test D transfers and compares data using an asynchronous data format. In an asynchronous mode, all data timing is generated by the baud rate generators of the FCCC. The test checks the two baud rate generators by comparing the time required to transfer 256 bytes of data to an upper and lower limit. If the transfer time is out of limits, the test outputs an error message.

2.5.14 Test E -- EIA Channel Data Path BOP Mode Test

Test E is identical to test C except that BOP data is transmitted.

2.5.15 Test F -- EIA Channel Data Path BOP NRZI Mode Test

Test F is identical to test C except that BOP NRZI data is transmitted.

2.5.16 Test 10 -- Local Line Data Path Test

Test 10 checks the operation of all four local line channels at 4800 bps. It forces the full-duplex mode so that transmitted data can be received. The targets of test 10 are as follows:

1. Local line data paths
2. Local line power supplies

2.5.17 Test 11 -- Maximum EIA Data Rate Transfer Test, Channel 0

Test 11 verifies the correct operation of the EIA data paths and modem clocks. It begins by transferring data through the loop-back connector at 19.2K bits per second full duplex. After four 256 byte blocks of data are transferred, the received data is compared to the data transmitted. Data is transmitted in a BOP mode.

2.5.18 Test 12 -- Maximum EIA Data Rate Transfer Test, Channel 1

Test 12 is identical to test 11 except that channel 1 is used for the data transfer.

2.5.19 Test 13 -- Maximum EIA Data Rate Transfer Test, Channel 2

Test 13 is identical to test 11 except that channel 2 is used for the data transfer.

2.5.20 Test 14 -- Maximum EIA Data Rate Transfer Test, Channel 3

Test 14 is identical to test 11, except that channel 3 is used for the data transfer.

2.5.21 Test 15 -- Data Transfer Channel-to-Channel FDX BOP Test

Test 15 checks the EIA/local line select and data path logic and the bit rate generator rate between channels. It requires the installation of a channel-to-channel cable (part number 2265161-0001) between the channel pairs to be tested. Data is transferred using the EIA interface signals full-duplex at 4800 bps.

2.5.22 Test 16 -- Channel-to-Channel Local Line HDX BOP NRZI Test

Test 16 tests the local line drivers and receivers and the local line logic. It requires the installation of a channel-to-channel cable between the channel pairs to be tested. The cable may only

be used between channels 0 and 2 and channels 1 and 3. Data is transferred half-duplex at 9.6K bits per second using the local line interface signals.

3.1 ERROR MESSAGES

When FC3TST detects an error condition, it outputs a self-explanatory error message. These messages are listed in the following table along with their corresponding error numbers.

Error Number	Error Message
1	A TILINE TIMEOUT OCCURRED WHEN READING THE FCCC SLAVE WORDS PROBABLE CAUSES ARE: FCCC TILINE ADDRESS SWITCHES ARE SET INCORRECTLY FCCC IS NOT INSTALLED. FAILURE OF 74LS359 AT "JJ15". FCCC TILINE SLAVE CONTROL LOGIC FAILURE. FCCC TILINE BUS ARBITRATION LOGIC.
2	FCCC SELF-TEST WAS NOT PROPERLY STARTED BY TILINE I/O RESET SLAVE WORD ZERO SHOULD = >47XX SLAVE WORD ZERO = >XXXX PROBABLE CAUSES ARE: 1) TILINE I/O RESET "TLIORES" FAILED TO START SELF-TEST 2) FCCC TILINE SLAVE WORD ZERO DATA FAILURE. 3) FCCC TILINE SLAVE CONTROL LOGIC.
3	FCCC ILLEGAL LEVEL X INTERRUPT. PROBABLE CAUSES ARE: 1) FAILING TMS9901. 2) FAILING TMS9900. 3) FAILING FCCC ROM OR RAM.
4	FCCC SELF-TEST TIMEOUT. PROBABLE CAUSES ARE: 1) FAILURE OF 74LS359 CLOCK GENERATOR "JJ15". 2) FAILURE TMS9900 "LL11". 3) FAILURE OF FCCC ROM.
6	FCCC SELF-TEST REPORT UNDEFINED STATUS. PROBABLE CAUSES ARE: 1) FAILURE OF FCCC SLAVE WORD DATA LOGIC. 2) FAILURE OF FCCC ROM.

Error Number	Error Message
	3) FAILURE OF TMS9901 AT "J4". 4) FAILURE OF TMS9900 AT "LL11".
9	FCCC ENCOUNTERED AN ILLEGAL XOP. PROBABLE CAUSES ARE: 1) ROM OR RAM ERROR AFTER SELF-TEST. 2) FAILING TMS9900.
A	FCCC TMS9900 FAILED SELF-TEST. PROBABLE CAUSES ARE: 1) FAILING TMS9900. 2) ROM OR RAM ERROR.
B	FCCC FAILED ROM CRC. PROBABLE CAUSES ARE: 1) TMS2532 AT LOCATION XXX. 2) ROM OR RAM ERROR.
C	FCCC FAILED RAM TEST. PROBABLE CAUSES ARE: 1) TMS4116 AT LOCATION XXXX. 2) LOGIC FAILURE ON THE TMS9900 DATA BUS.
D	FCCC TMS9901 CLOCK TEST FAILURE. PROBABLE CAUSES ARE: 1) TMS9901 A LOCATION "J4". 2) FAILURE OF FCCC CRU LOGIC.
E	SELF-TEST DETECTED A TMS9903(S) FAILURE. PROBABLE CAUSES ARE: 1) CHANNEL X TMS9903 AT LOCATION "XXXX". 2) FCCC CRU DECODE LOGIC.
F	FCCC FAILED RAM ADDRESSING TEST. PROBABLE CAUSES ARE: 1) TMS4116 AT LOCATION XXXX.

Error Number	Error Message
10	FCCC SELF-TEST ERROR. MEM PARITY ERROR NOT SET BY RESET. PROBABLE CAUSES ARE: 1) FAILURE PARITY ERROR FLIP-FLOP. 2) FAILURE OF FCCC RESET LOGIC. 3) FAILURE OF TMS9901 AT "J4".
11	FCCC SELF-TEST ERROR A FORCED MEM PARITY ERROR DID NOT INTERRUPT PROBABLE CAUSES ARE: 1) FAILURE OF TMS9901 AT "J4" 2) FAILURE OF TMS9900 AT "LL11"
12	FCCC SELF-TEST ERROR CAN NOT CLEAR MEMORY PARITY ERROR PROBABLE CAUSES ARE: 1) FAILURE OF THE PARITY ERROR FLIP-FLOP 2) FAILURE OF FCCC CRU DECODE LOGIC 3) FAILURE OF TMS9901 AT "J4"
13	FCCC SELF-TEST ERROR TILINE TIMEOUT ERROR NOT SET BY RESET PROBABLE CAUSES ARE: 1) FAILURE OF TILINE TIMEOUT ERROR FLIP-FLOP 2) FAILURE OF FCCC RESET LOGIC 3) FAILURE OF TMS9901 AT "J4"
14	FCCC SELF-TEST ERROR CAN NOT CLEAR TILINE TIMEOUT ERROR PROBABLE CAUSES ARE: 1) FAILURE OF TILINE TIMEOUT ERROR FLIP-FLOP 2) FAILURE OF FCCC CRU DECODE LOGIC 3) FAILURE OF TMS9901 AT LOC "J4"
15	RAM REFRESH ERROR PROBABLE CAUSES ARE: 1) FAILURE OF THE SN72555 AT LOC "K21" 2) FAILURE OF OTHER RAM REFESH LOGIC

Error Number	Error Message
16	**** ERROR IN TILINE SLAVE WORD DATA TEST **** PROBABLE CAUSES ARE: 1) TILINE BUS DATA LOGIC 2) TILINE BUS CONTROL LOGIC 3) TILINE CONTROL RAM FAILURE
17	**** ERROR LOW LEVEL TILINE MASTER TEST **** PROBABLE CAUSES ARE: 1) FCCC''S TILINE MASTER CONTROLLER 2) TILINE BUS ADDRESS LOGIC 3) TILINE BUS CONTROL LOGIC
18	**** ERROR TILINE MASTER DATA TRANSFER TEST **** PROBABLE CAUSES ARE: 1) TILINE CONTROLLER COUNTER LOGIC 2) TILINE BUS MASTER DATA LOGIC 3) TILINE BUS CONTROL LOGIC
19	**** ERROR TILINE MASTER ADDRESSING TEST **** PROBABLE CAUSES ARE: 1) TILINE ADDRESS COUNTER MSB'S 2) TILINE ADDRESS DRIVERS
20	**** ERROR 9903 INTERNAL LOOPBACK SYNC MODE **** PROBABLE CAUSES ARE: 1) TMS9903 FOR THE FAILING CHANNEL 2) SPEED PROBLEM WITH THE CRU LOGIC
21	**** ERROR 9903 INTERNAL LOOPBACK ASYNC MODE **** PROBABLE CAUSES ARE: 1) TMS9903 FOR THE FAILING CHANNEL 2) SPEED PROBLEM WITH THE CRU LOGIC
22	**** ERROR 9903 INTERNAL LOOPBACK BOP MODE **** PROBABLE CAUSES ARE: 1) TMS9903 FOR THE FAILING CHANNEL 2) SPEED PROBLEM WITH THE CRU LOGIC
23	**** ERROR 9903 INTERNAL LOOPBACK BOP NRZI MODE **** PROBABLE CAUSES ARE: 1) TMS9903 FOR THE FAILING CHANNEL 2) SPEED PROBLEM WITH THE CRU LOGIC

Error Number	Error Message
24	**** ERROR EIA MODEM CONTROL **** PROBABLE CAUSES ARE: 1) LOOPBACK CONNECTOR IS NOT INSTALLED 2) FAILURE OF AN EIA DRIVER OR RECEIVER 3) THE FAILING CHANNELS TMS9903 4) FAILURE OF THE TTL MODEM CONTROL LOGIC
25	**** ERROR CHANNEL DATA TEST SYNC MODE **** PROBABLE CAUSES ARE: 1) FAILURE OF A BIT RATE GENERATOR 2) OTHER CHANNEL DATA CLOCK LOGIC 3) THE FAILING CHANNELS TMS9903
26	**** ERROR CHANNEL DATA TEST ASYNC MODE **** PROBABLE CAUSES ARE: 1) BIT RATE GENERATOR AT 32X CLOCK 2) THE FAILING CHANNELS TMS9903
27	BIT RATE ERROR ON CHANNEL XX UPPER TIME LIMIT = XXXX LOWER TIME LIMIT = XXXX TEST TIME = XXXX PROBABLE CAUSES ARE: 1) THE BIT RATE GENERATOR CRYSTAL 2) THE BIT RATE GENERATOR 3) POWER LINE FREQ NOT WITHIN 1% TOLERANCE
28	**** ERROR CHANNEL DATA TEST BOP MODE **** PROBABLE CAUSES ARE: 1) THE TMS9903 ON THE FAILING CHANNEL
29	**** ERROR CHANNEL DATA TEST BOP NRZI MODE **** PROBABLE CAUSES ARE: 1) THE TMS9903 ON THE FAILING CHANNEL
30	**** ERROR LOCAL LINE DATA BOP NRZI MODE **** PROBABLE CAUSES ARE: 1) LOCAL LINE DRIVES OR RECEIVERS 2) CHANNEL 0 ISOLATED POWER SUPPLIES 3) CHANNEL TTL DATA SELECT LOGIC

Error Number	Error Message
31	**** ERROR CHANNEL 0 MAX TRANSFER RATE BOP **** PROBABLE CAUSES ARE: 1) FAILURE OF THE TMS9903 AT LOC "UU28" 2) FAILURE OF THE BIT RATE GENERATOR 3) SLOW EIA DRIVERS AND RECEIVERS OR TTL LOGIC
32	**** ERROR CHANNEL 1 MAX TRANSFER RATE BOP **** PROBABLE CAUSES ARE: 1) FAILURE OF THE TMS9903 AT LOC "TT22" 2) FAILURE OF THE BIT RATE GENERATOR 3) SLOW EIA DRIVERS AND RECEIVERS OR TTL LOGIC
33	**** ERROR CHANNEL 2 MAX TRANSFER RATE BOP **** PROBABLE CAUSES ARE: 1) FAILURE OF THE TMS9903 AT LOC "UU14" 2) FAILURE OF THE BIT RATE GENERATOR 3) SLOW EIA DRIVERS AND RECEIVERS OR TTL LOGIC
34	**** ERROR CHANNEL 3 MAX TRANSFER RATE BOP **** PROBABLE CAUSES ARE: 1) FAILURE OF THE TMS9903 AT LOC "UU4" 2) FAILURE OF THE BIT RATE GENERATOR 3) SLOW EIA DRIVERS AND RECEIVERS OR TTL LOGIC
35	**** ERROR CHANNEL TO CHANNEL EIA FDX BOP **** PROBABLE CAUSES ARE: 1) CHANNEL TO CHANNEL CABLE IS NOT INSTALLED 2) FAILURE OF LOCAL LINE ENABLE LOGIC 3) THE TWO BIT RATE GENERATORS ARE NOT RUNNING AT THE SAME SPEED
36	**** ERROR CHANNEL TO CHANNEL LOCAL LINE HDX BOP NRZI PROBABLE CAUSES ARE: 1) FAILURE OF A LOCAL LINE DRIVER TO TURN OFF 2) FAILURE OF THE HALF-DUPLEX CONTROL LOGIC

The following messages are output with specific error messages from the preceding list:

**ERROR DETECTED ON FCCC CHANNEL 0

**ERROR DETECTED ON FCCC CHANNEL 1

**ERROR DETECTED ON FCCC CHANNEL 2

**ERROR DETECTED ON FCCC CHANNEL 3

LLMTST

LOCAL LINE MODULE TEST

LOCAL LINE MODULE TEST (LLMTST)

LLMTST

Local Line Module Test

1.1 INTRODUCTION

LLMTST, the Local Line Module Test, verifies the ability of the local line module (LLM) to communicate with the host computer and another LLM.

1.2 TEST REQUIREMENTS

The LLMTST test may be executed with either one or two LLMs:

1. Using one LLM (the module under test), the test may be run up to the line driver/line receiver stages without a second LLM module.

2. Using two LLMs, the line driver/line receiver stages of the test may be executed. The second LLM must be fault-free.

The following equipment is required to operate the LLMTST test using one module:

* A Model 990 Computer with a minimum of 24K bytes of memory

* The LLM under test (part number 2267730-0001)

* An LLM download cable kit (part number 2270026-0001)

* A half-slot extender board (part number 226851-0001)

* An interactive terminal

* A device to load the test module

The following additional hardware is required to run the test using two LLMs:

* A functional (no faults) LLM
* An LLM-to-LLM test cable (part number 2267805-0001)
* A half-slot extender board

1.3 TEST CHARACTERISTICS

The LLMTST has certain characteristics that you should know before executing the test:

* LLMTST operates under the control of DDCS. Information about DDCS operation can be found in Volume 1 of this handbook.
* LLMTST consists of eight tests and is structured so that you can run either the complete set of tests or any separate test. These tests are as follows:

Test	Title
1	Echo Test
2	Switch Address Test
3	Self-Test
4	Receive Test
5	Transmit/Receive Test
6	Download Test
7	Interrupt Test
8	Deadman Timer Test

* LLMTST uses a number of test verbs, or commands, that execute various functions of the test. Several of these verbs execute parts of the test once or continuously. Others have utility functions that isolate hardware faults that have been identified during execution of test parts. The LLMTST test verbs are as follows:

Verb	Function
IT	Initialize test
EA	Execute all tests one time
E1-E8	Execute tests 1-8, respectively, one time
L1-L8	Loop continuously on tests 1-8, respectively
LA	Loop continuously on all tests
TX	Transmit data
TS	Transmit data using TX parameters
DB	Display TX and RX buffers and byte counts
RF	Read faulty data
ED	Echo data
RS	Reset LLM

Verb	Function
LP	Loop control
DS	Display status
PE	Print error count

2.1 TEST EXECUTION

The LLMTST module must be loaded and initialized by DOCS before execution can begin.

2.2 LOADING

The loading procedure is explained in Section 3 of Volume 1.

2.3 INITIALIZATION

When DOCS loads the test module, it outputs the name and version of the test:

LLMTEST LOCAL LINE MODULE DIAGNOSTIC VERSION # = MM/YY XX

Then DOCS executes the initialize test (IT) verb by asking you the following questions. If the default value is correct, press the RETURN key. If not, enter the correct value. You may later change the initialization parameters by reentering the IT verb.

ENTER THE CRU BASE ADDRESS OF THE LLM UNDER TEST. DEF=00A0-

ENTER THE INTERRUPT LEVEL OF THE LLM UNDER TEST. DEF=000F-

ENTER LLM1 SWITCH ADDRESS. DEF=0000-

IS LLM2 PRESENT AND CONNECTED TO LLM1 (0=NO 1=YES) DEF=0000

LLM1 is always the module under test. If you answer the last question with a 1 (yes), DOCS issues the following instructions:

ENTER THE CRU BASE ADDRESS OF THE LINE TEST LLM. DEF=0120-

When you have answered all the initialization questions, DOCS asks if you want to run the EA verb, which executes all parts of the LLMTST test one time:

EXECUTE EA VERB? (DEF=1) -

If press RETURN, LLMTST executes one time. If the test executes without errors, you may assume that the LLM under test is

operating properly and that no further testing is necessary. However, if any error messages are output, it is recommended that you run the test or tests that indicate errors and use any of the appropriate utility verbs to determine their cause. The following messages are output when the EA verb executes without errors:

```
EXECUTING PART 1. ECHO TEST
PART 1 COMPLETE.
EXECUTING PART 2. SWITCH ADDRESS TEST.
PART 2 COMPLETE.
EXECUTING PART 3. SELF-TEST
PART 3 COMPLETE.
EXECUTING PART 4. RECEIVE TEST
 1 BROADCAST ADDRESS TEST.
 2 SWITCH ADDRESS TEST.
 3 WRONG ADDRESS TEST.
PART 4 COMPLETE.
EXECUTING PART 5. TRANSMIT RECEIVE TEST.
PART 5 COMPLETE.
EXECUTING PART 6. DOWNLOAD TEST.
PART 6 COMPLETE.
EXECUTING PART 7. INTERRUPT TEST.
PART 7 COMPLETE.
EXECUTING PART 8 DEADMAN TIMER TEST.
PART 8 COMPLETE.
```

If you answer no (O) to the question EXECUTE EA VERB?, DOCS outputs the question VERB? and you may then execute any DOCS or LLMTST test verb.

2.4 TEST VERBS

Whenever DOCS outputs the question VERB?, you may enter the IT, EA, or any of the LLMTST test verbs discussed in the following paragraphs. To receive the question VERB?, press the @, CMD, HELP, or ESC key.

NOTE

The following verbs require that two LLMs be installed: TX, TS, E5, and L5. All other verbs can execute with only one LLM.

2.4.1 E1 Through E8 Verbs

The E1 through E8 verbs perform one execution of tests 1 through 8, respectively.

2.4.2 L1 Through L8 Verbs

The L1 through L8 verbs cause tests 1 through 8, respectively, to execute continuously, or loop, until you press the @ key.

2.4.3 LA Verb

The LA verb causes the continuous execution of tests 1 through 8 in consecutive order. To halt execution, press the @, CMD, HELP, or ESC key.

2.4.4 TX Verb

The TX verb allows you to transmit data from one LLM to another. When you execute this verb, it asks which LLM is to be the transmitter; the other module becomes the receiver. The TX verb then asks if the receive data should be compared to the transmit data. If you indicate yes, the compare is made and any differences are displayed. If you indicate no, no compare is made, nor does the the verb verify that data is received by the receive LLM.

The TX verb then asks for the number of bytes to be transmitted. The transmit data buffer cannot contain more than 32 bytes of data, so if the byte count you specify is greater than the number of bytes in the transmit data buffer, the buffer data is repeated as often as nescessary to transmit the proper number of bytes. If the byte count is smaller than the buffer size, only the specified number of bytes are transmitted. The byte count must always be greater than 1.

Finally, the verb asks whether user or default data is to be transmitted. The default data is a 32-byte data block. If you specify user data, the verb asks you to enter the data. When this is done, the data is transmitted from the selected transmit LLM to the receive LLM and compared if you chose to have the comparison made.

2.4.5 TS Verb

The TS verb executes the TX verb using the options selected during the last execution of the TX verb.

2.4.6 DB Verb

The DB verb displays the transmit and receive data buffers and byte counts from the last transmit-receive cycle. When you execute this verb, it outputs the following information:

```
****** TRANSMIT BYTE COUNT OXXXX
TRANSMIT BUFFER DATA
BYTE   0  1  2  3 . . . F
0000
DISPLAY RECEIVE BUFFER? (1 = YES, 0 = NO)
```

If you answer the preceding question with a 1 (yes), the DB verb outputs the following information:

```
**** RECEIVE BYTE COUNT OXXXX
RECEIVE BUFFER DATA
BYTE  0  1  2  3 . . . F
0000
VERB?
```

2.4.7 RF Verb

The RF verb allows you to read faulty data, that is, data that an LLM received but did not pass to the computer because of a problem such as a CRC error. This verb displays the entire contents of the data buffer of the receive LLM.

2.4.8 ED Verb

The ED verb puts the LLM under test into echo mode and asks you to enter data to echo:

```
ENTER ECHO DATA.  DEFAULT = AXXXX
```

The verb then transmits the data that you enter to the LLM and checks the echoed data. Continual execution of this verb is useful for checking the CRU data interface.

2.4.9 RS Verb

The RS verb resets one of the LLMs and then toggles the CRU reset bit and checks the interface to verify that the reset has been performed. When you execute the RS verb, it asks which LLM to reset:

```
ENTER NUMBER OF LLM TO RESET. LLM1 =1  LLM2 =2
DEFAULT = 1XXXX
```

2.4.10 LP Verb

The LP verb allows looping on separate tests of the execute verbs (E1 through E8). The LP verb asks if you want to loop on a test, and which test should be executed. If you indicate that you do not want looping, the tests do not loop. For example, if you enter the number 4, the execute verb that has a test 4 executes tests 1, 2, and 3 and then loops on test 4. The messages that accompany each execute verb are numbered so you can easily determine which test to loop on. To prevent looping, reexecute the LP verb and respond with a 0 to the question:

```
LOOP ON VERBS? (0=NO, VALUE=LOOP ON THAT PART OF VERB)
DEFAULT = 0XXXX
```

All other verbs loop if any nonzero value was entered during the last execution of the LP verb.

2.4.11 DS Verb

The DS verb displays the CRU interface of both LLMs. The following is an example of output from this verb:

```
DATA  EOB WRQ RRQ MSK INT  ADR
AA     0   0   0   0   1   04    LLM1
F0     0   0   0   0   1   17    LLM2


EOB - end-of-block (CRU bit 9)
WRQ - write request (CRU bit 11)
RRQ - read request (CRU bit 12)
MSK - interrupt mask (CRU bit 14)
ADR - LLM switch address (read through
      the CRU data line, CRU bits 0-7)
```

The data word is CRU bits 0 through 7. The data is the last data sent from the LLM to the host.

2.4.12 PE Verb

The PE verb outputs the accumulated error total of all errors that have occured since the execution of the last execute or loop verb. The number of loops is also output.

2.5 TEST DESCRIPTIONS

The LLMTST test consists of the following eight tests, which are discussed in the following paragraphs.

Test	Title
1	Echo Test
2	Switch Address Test
3	Self-Test
4	Receive Test
5	Transmit/Receive Test
6	Download Test
7	Interrupt Test
8	Deadman Timer Test

2.5.1 Test 1 -- Echo Test

Test 1 checks the basic host computer-to-LLM CRU interface. The computer sends all 256 possible data patterns to the LLM, which then echos each pattern back to the host for verification. The data is passed back and forth using a handshaking method of data exchange.

If the data pattern received from the LLM does not compare to what was sent, the following error message is output:

```
ERROR #1
ECHO COMPARE ERROR.  EXPECTED = XX    ACTUAL = XX
```

The bit in error may be determined by comparing the expected and the received data. If the handshaking process on the LLM is not working properly, one of the following error messages may also be output:

```
ERROR #5
RRQ FAILED TO SET AFTER DAV WAS RESET

ERROR #6
RRQ FAILED TO RESET AFTER DAV WAS SET
```

2.5.2 Test 2 -- Switch Address Test

Test 2 checks the address switches of the LLM. The test reads these switches to determine if they are set to the address you entered during test initialization. A description of address switch setting may be found in the LLM Specifications.

If the switch address that the test reads does not compare to the address entered during initialization, an error message is output.

2.5.3 Test 3 -- Self-Test

Test 3 causes the LLM under test to execute an EPROM resident self-test, which consists of four parts:

1. The EPROM self-test first does a checksum on itself. If the checksum does not agree with the expected value, an error message is output.

2. The self-test then checks the LLM RAM memory address lines.

3. Then the self-test performs a data pattern test on the RAM. If a problem is found in the RAM test, an error message is output indicating which RAM chip is faulty.

   The standard LLM has only two RAM chips, but sockets are provided for two additional chips. The self-test determines how many RAM chips are available before the test begins.

4. The fourth part of the self-test causes the TMS9903 to loop back internally and then transmits and receives four bytes of data through the TMS9903. If this part of the test fails, an error message is output.

2.5.4 Test 4 -- Receive Test

Test 4 checks the receive functions of the LLM. This test is executed with the TMS9903 in internal loopback mode. The LLM under test is the transmitting as well as the receiving LLM. Test 4 consists of three parts:

1. The first part transmits a message and checks for errors using the broadcast address.

2. The second part sends a message using the address you entered during test initialization.

3. The third part sends a message using an address other than the broadcast address or the address entered during test initialization. This message should be rejected by the LLM. The test verifies that the message is rejected and outputs an error message if it is not.

2.5.5 Test 5 -- Transmit/Receive Test

Test 5 checks the LLM line driver/line receiver stages. A second LLM that is fault-free is required for this test. The test sends a message from the LLM under test to the second LLM to verify the line driver operation. The test also sends a message from the second LLM to the LLM under test to verify the line receiver operation.

2.5.6 Test 6 -- Download Test

Test 6 checks the download features of the LLM. This test is executed with the TMS9903 in internal loopback mode, and consists of two parts:

1. In the first part, the LLM sends a download command to itself, using the address that you entered during test initialization. The LLM should then send itself a response consisting of the module address and a data byte of >73.

2. In the second part, the LLM sends a download command to itself using the broadcast address. No response is expected.

With the download cables connected, execution of test 6 forces the computer into the load routine before the test has completed.

2.5.7 Test 7 -- Interrupt Test

Test 7 checks the LLM interrupt by unmasking the interrupt and sending a message with the TMS9903 on the LLM in internal loop-back mode. The LLM should receive the message sent and interrupt the computer. If no interrupt occurs, an error message is output.

2.5.8 Test 8 -- Deadman Timer Test

Test 8 checks the deadman timer by beginning a data transfer to the LLM and then terminating communication with the LLM for approximately 30 seconds. The LLM should time out the data transfer in about 20 seconds and then enter a state in which it no longer responds to the computer until the computer resets the LLM.

At the end of 30 seconds, test 8 attempts to continue the data transfer that it started and verifies that the LLM does not respond. If the LLM responds, the test indicates that the deadman timer is not working properly.

3.1 ERROR MESSAGES

When the LLMTST test detects a fault condition, it outputs an error message and corresponding error number. These messages are explained in the following table.

Error Number	Error Message
1	ECHO COMPARE ERROR. EXPECTED =XX ACTUAL =XX
	This message is output during execution of the verbs E1 and ED. It indicates a problem in the interface between the computer and the LLM. The data presented to the computer is not the same data sent to the LLM. Check devices U5, U11, U3, U4, U2, U8, U26, and U17 to ensure that the data is reaching the TMS9980A and U14. Check U14 for proper operation, and check U10, U19, U26, U30, U23, U4, and U13 to ensure that the TMS9980A is presenting the same data to the computer.
2	UNEXPECTED LLM1 INTERRUPT
	This message indicates that the LLM under test produced an interrupt that should have been masked off. Check U9, pin 11 to determine if INTMASK is set to 0. If it is, check U13 for proper operation.
3	(reserved for expansion)
4	SELFTEST FAILED TO COMPLETE. REASON UNKNOWN.
	This message is output during execution of the E3 verb. It indicates that the self-test took too long to complete. The part in execution when the test timed out is unknown. Check devices U14, U39, U28, U36, and U37. Also verify that device U34 is providing a clock input to device U39 through devices U40 and U42.

Error Number	Error Message

5 RRQ FAILED TO SET AFTER DAV WAS RESET.

This message occurs during the execution of the verbs E1, E3, E4, E5, E6, E7, E8, RF, TX, and TS. It indicates a handshaking problem with the LLM. RRQ is not being set by the LLM as expected. Check devices U4, U9, U16, U19, U14, U17, U24, U6, and U13.

6 RRQ FAILED TO RESET AFTER DAV WAS SET.

This message occurs during execution of the verbs E1, E3, E4, E5, E6, E7, E8, RF, TX, and TS. It indicates a handshaking problem with the LLM. RRQ is not being reset by the LLM as expected. Check devices U4, U9, U19, U14, U17, U24, U6, and U13.

7 SELFTEST REPORTED AN ILLEGAL ERROR CODE.

This message is output during execution of the E3 verb. It indicates that the self-test has resulted in an error code that is not used. Check devices U14, U39, U28, U36, and U37. The interface between the TMS9980A and the computer may also have resulted in the illegal error code.

8 EOB FAILED TO RESET AFTER CRU RESET BIT WAS TOGGLED.

This message indicates that setting the CRU reset bit does not result in the EOB bit being reset. Check devices U4, U9, U10, U15, and U22 to ensure that the reset interrupt reaches the TMS 9980A. Check U14 for proper operation and check U10, U19, and U17 to ensure that the TMS 9980A clears the EOB bit in response to this interrupt. Also check U24, U6, and U13 to ensure that this information is reaching the computer.

Error Number	Error Message

9 WRQ FAILED TO RESET AFTER CRU RESET BIT WAS TOGGLED.

This message indicates that setting the CRU reset bit does not result in the WRQ bit being reset. Check devices U4, U9, U10, U15, and U22 to ensure that the reset interrupt reaches the TMS9980A. Check U14 for proper operation and check U10, U19, and U17 to ensure that the TMS9980A clears the EOB bit in response to this interrupt. Also check U24, U6, and U13 to ensure that this information is reaching the computer.

10 RRQ FAILED TO RESET AFTER CRU RESET BIT WAS TOGGLED.

This error indicates that setting the CRU reset bit does not result in the RRQ bit being reset. Check devices U4, U9, U10, U15, and U22 to ensure that the reset interrupt reaches the TMS9980A. Check U14 for proper operation and check U10, U19, and U17 to ensure that the TMS9980A clears the EOB bit in response to this interrupt. Also check U24, U6, and U13 to ensure that this information is reaching the computer.

11 RECEIVER OVERRUN OCCURRED.

This message is output during execution of the verbs E4, E5, E6, E7, TX, and TS. It indicates that a new character was received before the previous character was removed from the receive buffer, resulting in a lost character. Check devices U14 and U39.

12 CRC ERROR ON RECEIVED DATA.

This message is output during execution of the verbs E4, E5, E6, E7, TX, and TS. It indicates that a CRC error was detected during data reception. If it occurs during the execution of verbs E4, E6, or E7, check devices U14 and U39. If it occurs during the execution of verb E5, devices U40, U45, U46, and AT2 should also be checked.

Error Number	Error Message
13	LLM REPORTED A RECEIVE TIMEOUT ERROR. This message is output during execution of the verbs E4, E5, E6, E7, TX, and TS. It indicates that the LLM timed out while receiving data from the communications line. If it occurs during the execution of verbs E4, E6, or E7, check devices U14 and U39. If it occurs during the execution of verb E5, devices U40, U45, U46, and AT2 should also be checked.
14	LLM TIMED OUT WHILE TRANSMITTING. This message is output during execution of the verbs E4, E5, E6, E7, TX, and TS. It indicates that the LLM timed out while transmitting data on the communications line. Check devices U14 and U39. Also verify that device U34 is providing a clock input to device U39 through devices U40 and U42.
15	(reserved for expansion)
16	(reserved for expansion)
17	RECEIVE DATA BUFFER OVERFLOWED. This message is output during execution of the verbs E4, E5, E6, E7, TX, and TS. It indicates that the LLM received more data than may be stored in the buffer space provided on the LLM. Check devices U14, U28, U36, U37, and U39.
18	LLM RECEIVED AN ABORT. This message is output during execution of the verbs E4, E5, E6, E7, TX, and TS. It indicates that the LLM detected an abort character in the receive data string. If it occurs during the execution of verbs E4, E6, or E7, check devices U14 and U39. If it occurs during the execution of verb E5, devices U40, U45, U46, and AT2 should also be checked.

Error Number	Error Message
19	TRANSMIT DATA BUFFER OVERFLOWED. This message is output during execution of the verbs E4, E5, E6 E7, TX, and TS. It indicates that more data was passed from the computer to the LLM than may be stored in the LLM buffer space. Check devices U14, U28, U36, and U37. If this message occurs during execution of the TX and TS verbs, it could indicate that the number of bytes entered in response to the TX questions is more than the number of bytes available in the transmitting LLM buffer space.
20	SELFTEST REPORTED A ROM CHECKSUM ERROR. This message is output during execution of the E3 verb. It indicates that the EPROM test has resulted in an error. Check devices U14, U19, U12, U25, and U28.
21	RAM # 1 FAILED SELFTEST. This message is output during execution of the E3 verb. It indicates that RAM chip U36 has failed. Check devices U36, U14, U19, U12, and U25.
22	RAM # 2 FAILED SELFTEST. This message is output during execution of the E3 verb. It indicates that RAM chip U37 has failed. Check devices U37, U14, U19, U12, and U25.
23	RAM # 3 FAILED SELFTEST. This message is output during execution of the E3 verb. It indicates that RAM chip U35 has failed. Check devices U35, U14, U19, U12, and U25.
24	RAM # 4 FAILED SELFTEST. This message is output during execution of the E3 verb. It indicates that RAM chip U38 has failed. Check devices U38, U14, U19, U12, and U25.

Error Number	Error Message
25	A RECEIVE FRAME ERROR HAS BEEN DETECTED. This message is output during execution of the E3 verb. It indicates that one or more bits have been lost or gained during the self-test loopback, resulting in a partial character as the final character. Check devices U14 and U39.
26	SELFTEST LOOPBACK DATA ERROR DETECTED. This message is output during execution of the E3 verb. It indicates that the internal loopback test using the TMS9903 has resulted in a data error. Check devices U14 and U39.
27	SELFTEST CRC ERROR DETECTED. This message is output during execution of the E3 verb. It indicates that the internal loopback test using the TMS9903 has resulted in a CRC error. Check devices U14 and U39.
28	(reserved for expansion)
29	(reserved for expansion)
30	INTERRUPT MASK FAILED TO RESET AFTER CRU RESET BIT WAS TOGGLED This message indicates that setting the CRU reset bit does not result in the interrupt mask being reset as expected. Check devices U4, U9, U10, U15, and U22 to ensure that the reset interrupt reaches the TMS9980A. Check U14 for proper operation and check U10, U19, and U17 to ensure that the TMS9980A clears the EOB bit in response to this interrupt. Also check U24, U6, and U13 to ensure that this information is reaching the computer.

Error Number	Error Message
31	WRQ FAILED TO SET AFTER DAV WAS SET.

This message is output during execution of the verbs E4, E5, E6, E7, TX, TS, and RF. It indicates a hand-shaking problem with the LLM. WRQ is not being set by the LLM as expected. Check devices U4, U9, U16, U19, U10, U15, U22, U18, U14, U17, U6, U24, and U13.

32 WRQ FAILED TO RESET AFTER DAV WAS RESET.

This message is output during execution of the verbs E4, E5, E6, E7, TX, TS, and RF. It indicates a hand-shaking problem with the LLM. WRQ is not being reset by the LLM as expected. Check devices U4, U9, U16, U19, U10, U15, U22, U18, U14, U17, U6, U24, and U13.

33 HOST RECEIVE BUFFER OVERFLOWED.

This message is output during execution of the verbs E4, E5, E6, E7, TX, and TS. It indicates that the receive buffer set aside in the test has overflowed.

34 TIMED OUT WAITING FOR RECEIVE DATA.

This message is output during execution of the verbs E4, E5, E6, E7, TX, and TS. It indicates that the test timed out while waiting for receive data. If it occurs during execution of the verbs E4, E6, or E7, check devices U14 and U39. If it occurs during execution of the E5 verb, devices U40, U45, U46, and AT2 should also be checked.

35 THE LLM RETURNED AN ILLEGAL ERROR CODE.

This message indicates that the LLM presented an invalid error code to the computer. Check devices U14, U28, and the devices in the computer interface.

Error Number	Error Message
36	TRANSMIT AND RECEIVE BYTE COUNT ARE NOT EQUAL. TRANSMIT BYTE COUNT =XXXX RECEIVE BYTE COUNT =XXXX This message is output during execution of the verbs E4, E5, E6, E7, TX, and TS. It indicates that the receiving LLM has just transferred to the computer a data block whose byte count does not agree with the byte count of the data block transferred to the transmitting LLM. Since the LLM did not detect an error, the data block size was changed in the transfer to the transmitting computer or in the transfer from the receiving LLM to the computer. Check devices U14, U28, U36, and U37.
37	RECEIVE DATA ERROR. EXPECTED=XX ACTUAL=XX BYTE#=XXXX. This message is output during execution of the verbs E4, E5, E6, E7, TX, and TS. It indicates that the data transferred to the transmitting LLM does not agree with the data transferred from the receiving LLM to the computer. Since the receiving LLM did not detect a CRC error, the data was probably garbled in the transfer from the computer to the LLM or the transfer from one LLM to the other LLM. Check devices U3, U4, U8, U2, U17, U26, U19, U14, U30, U10, U23, and U13.
38	LLM1 SWITCH ADDRESS INCORRECT. EXPECTED= XX ACTUAL = XX This message is output during execution of the E2 verb. The switch address is expected to be set to the address entered during test initialization for the E2 verb. Verify that the address entered during initialization agrees with the address set up on the address switches on the module. If it does, check devices S1, U7, U6, and U13.

Error Number	Error Message

39 ADDRESS DECODE FAILED. LLM1 ATTEMPTED TO PASS DATA WHICH WAS NOT ADDRESSED TO LLM1.

This message is output during execution of the verbs E4 and E6. Under the E4 verb, it indicates that the LLM is accepting data that has an address other than its address or the broadcast address when address decode is selected. Ensure that switch S2-4 is set up for address decoding. If it is, check devices U16, U19, U14, and S2-4.

Under the E6 verb, the message indicates that the LLM has sent a response to a download command that contained the broadcast address.

40 LLM1 FAILED TO INTERRUPT THE HOST.

This message is output during execution of the E7 verb. It indicates that the LLM under test did not interrupt the computer as expected when data was transmitted to it. Check devices U4, U9, U13, U14, U17, U19, and U20.

41 LLM1 DEADMAN TIMER FAILED

This message is output during execution of the E8 verb. It indicates that the LLM under test did not time out the data transfer from the computer to the LLM as expected. Check devices U14, U19, U17, U20, U21, and U18.

MUXTST

CI403 AND CI404 ASYNCHRONOUS COMMUNICATIONS INTERFACE TEST

CI403 AND CI404 ASYNCHRONOUS COMMUNICATIONS INTERFACE TEST (MUXTST)

MUXTST

CI403 and CI404 Asynchronous Communications Interface Test

1.1 INTRODUCTION

MUXTST, the CI403 and CI404 Asynchronous Communications Interface test, assures full performance of the CI403 and CI404 communications interfaces hardware (part numbers 2230350-0001 and 2230360-0001, respectively).

MUXTST is loaded and controlled by DOCS. By specifying the channel test configuration, you exercise indirect control over the tests to be performed. You can execute MUXTST with no external equipment connected, or you can attach a loopback connector or an asynchronous modem. MUXTST skips tests that cannot be performed and displays a message to indicate the unexecuted tests.

1.2 TEST REQUIREMENTS

The following equipment is required to operate MUXTST:

* A Model 990 Computer with TILINE (TILINE is a trademark of Texas Instruments) and a minimum of 64K bytes of memory (where K equals 1,024)
* A CI403 or CI404 communications controller
* An interactive terminal
* A loading device

The following equipment is optional:

* A loopback connector (part number 2265197-0001). The EIA side of the loopback connector fits into the 18-pin connectors on the CI403 controller.
* A loopback assembly (part number 2265197-0001). The assembly mates with the 25-pin connector on cables with the following part numbers: 2303070, 2303071, and 2303077.

* An external asynchronous modem.

* A fiber optic loopback connector (part number 2233202-0001).

1.3 TEST CHARACTERISTICS

MUXTST operates under the control of DOCS. Refer to Volume 1 of the Unit Diagnostics Handbook for information about DOCS operation.

MUXTST consists of 13 tests:

Test	Title
1	Self-test started by TILINE I/O reset
2	Self-test started by write to slave word zero
3	MUX timer function test
4	UART interface data path test
5	Internal loopback data transfer test
6	Transmit FIFO control test
7	Channel baud rate test (max test time 90 sec)
8	RS-232-C interface test
9	Half-duplex EIA data test
A	Data loopback 5 bit char
B	Data loopback 6 bit char
C	Data loopback 7 bit char
D	Data loopback 8 bit char

In addition to the verbs supplied by DOCS, MUXTST uses the following test execution verbs:

Test Execution Verb	Function
EA	Execute all tests
ET	Execute an individual test one time
LA	Loop on all tests
LT	Loop on an individual test

Utility verbs help you isolate errors that are detected during test execution:

Utility Verb	Function
DS	Display status
PE	Display error count
PV	Print verbs
RM	Read/modify channel interface bits
TH	Display test history

You can also use the Initialize Test (IT) verb to reinitialize the MUXTST initialization parameters.

You should execute all the tests in the MUXTST diagnostic to verify that the hardware is functioning properly. If a failure occurs, only use the first error message to isolate the cause of failure.

When executing MUXTST with an external loopback, assume that the failure was caused by equipment farthest away from the central processing unit (CPU). For example, if you run test >A with an asynchronous modem attached (the modem is in analog loopback) and the test fails, assume the modem is bad rather than the controller.

After making your assumption, select a channel test configuration that uses all the hardware except that of the isolated equipment. If the test that previously failed runs without errors from that configuration, then the malfunction lies in the isolated equipment. Using the previous example, you should test all the hardware except the modem. When selecting test initialization parameters, set the channel test configuration to select for the EIA loopback connector. If test >A completes without errors, you have isolated the problem to the modem.

2.1 TEST INITIALIZATION

MUXTST must be loaded and initialized by DOCS before you can begin testing. Volume 1 of the Unit Diagostics Handbook explains the loading procedure. When DOCS has loaded the MUXTST module, the name and version of the test appears:

```
MUXTST
CI403 & CI404 COMMUNICATIONS INTERFACE DIAGNOSTIC
VERSION  XX  JJJ/YY
```

where:

XX indicates the revision letter.

JJJ is the Julian date.

YY is the year.

Then DOCS executes the IT verb with the following prompts:

ENTER MUX TILINE BASE ADDRESS: (DEF = XXXX) -
Enter the hexadecimal address of the communications controller.

ENTER MUX INTERRUPT LEVEL: (DEF = X) -
Enter the interrupt level of the communications controller.

ENTER MUX BOARD TYPE: (0=CI403, 1=CI404) (DEF = X) -
If you are testing a CI403 communications controller, enter 0. If you are testing a CI404 communications controller, enter 1.

```
CHANNEL TEST CONFIGURATION
0 = DO NOT TEST CHANNEL
1 = UART INTERNAL LOOPBACK
2 = FIBER OPTIC MODEM INTERNAL LOOPBACK
3 = FIBER OPTIC PWB EDGE LOOPBACK P/N 2233202-0001
4 = EIA RS-232C PWB EDGE LOOPBACK P/N 2303065-0001 OR
    CABLE P/N 2303070-0001 WITH CABLE END LOOPBACK P/N 2265197-0001
5 = EIA RS-232C CABLE P/N 2303077-0001 WITH
    CABLE END LOOPBACK P/N 2265197-0001
6 = EIA RS-232C CABLE P/N 2303077-0001 WITH
    EXTENSION CABLE P/N 2303071-000X AND
    CABLE END LOOPBACK P/N 2265197-0001
7 = EXTERNAL MODEM IN LOOPBACK CONNECTED WITH CABLE P/N 2303070-0001
CHANNEL 0 TEST CONFIGURATION ( DEF = X ) -
CHANNEL 1 TEST CONFIGURATION ( DEF = X ) -
CHANNEL 2 TEST CONFIGURATION ( DEF = X ) -
CHANNEL 3 TEST CONFIGURATION ( DEF = X ) -
```

For each prompt, enter the number that corresponds to the configuration that you are testing. For example, if your configuration has a UART internal loopback on channel 0, enter 1 in response to the CHANNEL 0 TEST CONFIGURATION prompt.

If you enter 7 in response to the prompts, the following additional prompt appears:

```
SELECT EXTERNAL ASYNCHRONOUS MODEM BAUD RATE 0 = 300BPS, 1 = 1200BPS, 2 = 2400BPS (DEF = X)
```

If the modem baud rate is 300 bits per second (BPS), enter 0. If the rate is 1200 or 2400 BPS, enter 1 or 2, respectively.

```
DO YOU WANT TO RUN THE TEST WITH INTERRUPTS? ( DEF = X ) -
```

If you want to execute the test with interrupts, enter 1 (yes). Otherwise, enter 0.

```
ENTER COMPUTER LINE FREQ: (0=50, 1=60, DEF = X) -
```

Select the line frequency used by the CPU. Enter 0 for 50 Hz, or 1 for 60 Hz.

After you respond to the initialization prompts, DOCS displays the following prompt:

```
EXECUTE EA VERB? (DEF=1) -
```

If you accept the default (yes), tests >1 through >D execute in the test mode that you selected during initialization. If you enter 0 (no), the following prompt is displayed:

```
VERB? -
```

You can then execute any part of MUXTST by entering the appropriate test verb.

If errors occur during a test, you should reexecute the test. Use the appropriate verb to determine the cause of the errors. The following messages appear when MUXTST executes without errors:

```
TEST 01 SELF TEST STARTED BY TILINE I/O RESET
TEST 01 COMPLETE

TEST 02 SELF TEST STARTED BY WRITE TO SLAVE WORD ZERO
TEST 02 COMPLETE

TEST 03 MUX TIMER FUNCTION TEST
TEST 03 COMPLETE

TEST 04 UART INTERFACE DATA PATH TEST
TESTING 0 1 2 3
TEST 04 COMPLETE

TEST 05 INTERNAL LOOPBACK DATA TRANSFER TEST
TESTING 0 1 2 3
TEST 05 COMPLETE

TEST 06 TRANSMIT FIFO CONTROL TEST
TESTING 0 1 2 3
TEST 06 COMPLETE

TEST 07 CHANNEL BAUD RATE TEST MAX TIME 90 SEC
TESTING 0 1 2 3
TEST 07 COMPLETE

TEST 08 RS-232C INTERFACE TEST
TESTING 0 1 2 3
TEST 08 COMPLETE

TEST 09 HALF DUPLEX EIA DATA TEST
TESTING 0 1 2 3
TEST 09 COMPLETE

TEST 0A DATA LOOPBACK 5 BIT
TESTING 0 1 2 3
TEST 0A COMPLETE

TEST 0B DATA LOOPBACK 6 BIT
TESTING 0 1 2 3
TEST 0B COMPLETE

TEST 0C DATA LOOPBACK 7 BIT
TESTING 0 1 2 3
TEST 0C COMPLETE
```

```
TEST OD DATA LOOPBACK 8 BIT
TESTING 0 1 2 3
TEST OD COMPLETE
```

2.2 TEST VERBS

MUXTST contains the following test execution verbs:

Test Execution Verb	Function
EA	Execute all tests
ET	Execute an individual test one time
LA	Loop on all tests
LT	Loop on an individual test

Utility verbs help you isolate errors that are detected during test execution:

Utility Verb	Function
DS	Display status
PE	Display error count
PV	Print verbs
RM	Read/modify channel interface bits
TH	Display test history

You can also use the IT verb to reinitialize the MUXTST initialization parameters. The following paragraphs discuss the verbs.

2.2.1 Execute All Tests (EA) Verb

The EA verb executes all the tests consecutively. MUXTST may skip some tests, depending on the test configuration selected.

2.2.2 Execute an Individual Test One Time (ET) Verb

The ET verb executes an individual test one time. Enter the hexadecimal number of the the test that you want to execute.

2.2.3 Loop on All Tests (LA) Verb

The LA verb causes continuous looping of the EA test sequence. The loop count displayed equals the number of times the EA sequence has executed. The error count also appears. To terminate looping, press the @, CMD, or HELP key.

2.2.4 Loop on an Individual Test (LT) Verb

The LT verb allows continuous looping of an individual test. The loop count is displayed continuously on the front panel. To terminate looping, press the @, CMD, or HELP key. If any errors occur during a test, the error count appears on the interactive terminal.

2.2.5 Display Status (DS) Verb

The DS verb displays the status of the CI403 or CI404 board in the form of TILINE slave words 0 through 3. An example of the status table is as follows:

```
INTERFACE STATUS:
  SW0     SW1     SW2     SW3
 4004    7380    0324    8024


MUX STATUS HISTORY (NEWEST STATUS FIRST)

1B00    1A00    1900    1800    1B00    1A00    1900    1800
1B00    1A00    1900    1800    1B00    1A00    1900    1800
1B00    1A00    1900    1800    1B00    1A00    1900    1800
1B00    1A00    1900    1800    1B00    1A00    1900
 CLEAR MUX STATUS HISTORY (DEF=0) -
```

The status word is read from the MUX TILINE interface. Enter 1 (yes) in response to the CLEAR MUX STATUS HISTORY if you want the status history cleared. Otherwise, enter 0.

Consult the installation and operation manual for the type of communications controller you are using for the definition of these TILINE slave word bits.

2.2.6 Display Error Count (PE) Verb

The PE verb displays the current error count in hexadecimal at the I/O device in the following format:

```
MUXTST ERRORS = XXXX
 ZERO ERROR COUNT (DEF=1) -
```

If there are no errors, enter 1 (yes) in response to the ZERO ERROR COUNT prompt. Otherwise, enter 0.

2.2.7 Print Verbs (PV) Verb

The PV verb prints the descriptions for each of the MUXTST verbs as follows:

```
     MUXTST VERBS
IT - INITIALIZE TEST
ET - EXECUTE TEST
LT - LOOP TEST
EA - EXECUTE ALL TESTS
LA - LOOP ALL TESTS
DS - DISPLAY STATUS
PE - DISPLAY ERROR COUNT
RM - READ & MOD CHANNEL INTERFACE STATUS
TH - TEST HISTORY
```

2.2.8 Read/Modify Channel Interface Bits (RM) Verb

The RM verb reads the channel status and displays the status of the modem interface signals for the CI403 or CI404 board. (The RM verb has little use in the CI404 environment although it can be used.) The RM verb format is as follows:

```
READ/MODIFY CHANNEL INTERFACE BITS

WHICH CHANNEL? DEF=0 -
     Enter the number of the channel that you want to read/modify.
```

The following is an example of the table that is displayed. A 1 under the signal name indicates a true state, and a blank indicates a false state.

DTR	DSR	RTS	CTS	SRTS	DCD	RI	AL
1		1	1				1

Data terminal ready (DTR), request to send (RTS), secondary request to send (SRTS), and analog loopback (AL) are output signals. Data set ready (DSR), clear to send (CTS), data carrier detect (DCD), and ring (RI) are input signals. The following prompts appear after the table and allow you to change the state of the output signals. Using the previous table as an example, the current states of the output signals follow the prompts:

```
DTR  = 1 -
RTS  = 1 - 0
SRTS = 0 -
AL   = 1 -
```

To change the state of the output signal, enter 1 for a true state or 0 for a false state. In this example, the RTS output signal is changed to a false state. The table is displayed again showing the changes that you made.

DTR	DSR	RTS	CTS	SRTS	DCD	RI	AL
1							1

NOTE

You must use @ out or CMD key to exit the RM verb.

2.2.9 Display Test History (TH) Verb

The TH verb is used for software maintenance purposes. It allows you to review all the commands processed during testing when the test series completes. The first prompt asks if you want to print the test history. If you select the print option and the error message device is a printer, the complete history of the last test executed prints. If you do not select the print option, the interactive device displays each test command block (TCB). You can then press the RETURN key to display the next TCB. If you do not want to view the complete test history, press the CMD key to exit the TH verb early.

2.3 TEST DESCRIPTIONS

MUXTST consists of 13 tests:

Test	Title
1	Self-test started by TILINE I/O reset
2	Self-test started by write to slave word 0
3	MUX timer function test
4	UART interface data path test
5	Internal loopback data transfer test
6	Transmit FIFO control test
7	Channel baud rate test
8	RS-232-C interface test
9	Half-duplex EIA data test
A	Data loopback 5 bit
B	Data loopback 6 bit
C	Data loopback 7 bit
D	Data loopback 8 bit

Tests 1 through 7 test the system, and the CI403 and CI404 boards internally. (Tests 1 through 3 always execute. Tests 4 through 7 do not execute on channels that are initialized with test configuration zero.) Tests 8 and 9 operate only on the CI403, and verify the EIA interface functions correctly. Tests A through D verify that the UART data transfer using external loopback operates properly. (Execution time for tests A through D depend on whether you select modems.)

Each test uses the logic tested by previous tests so that it uses a minimum of untested hardware. When tests are executed in ascending order, MUXTST begins testing hardware at the TILINE interface and progresses until it reaches the communication channel interface. Those tests which target the communication channel execute only if you have selected the proper initialization parameters. The channel configuration that you specify during initialization determines whether tests A through D execute. Refer to Table 1 for test configurations. MUXTST checks one piece of hardware at a time in incremental steps, from the processor to the channel interface.

Table 1 lists the tests by number and the configuration necessary to execute them.

Table 1 MUXTST Test Configurations

Test Number	UART	Loopback (Board) 2303065	Loopback (Cable) 2303070	Loopback (Cable) 2303077 2303071	Analog Loopback (Modem) Async	Fiber Optic Loopback 2266202
1	x	x	x	x	x	x
2	x	x	x	x	x	x
3	x	x	x	x	x	x
4	Req	x	x	x	x	x
5	Req	x	x	x	x	x
6	Req	x	x	x	x	x
7	Req	x	x	x	x	x
8	Req	Req	Opt	Opt	Skipped	Skipped
9	Req	Req	Opt	Opt	Skipped	Skipped
A	Req	Opt	Opt	Opt	Opt	Opt
B	Req	Opt	Opt	Opt	Opt	Opt
C	Req	Opt	Opt	Opt	Opt	Opt
D	Req	Opt	Opt	Opt	Opt	Opt

Notes:

UART is an abbreviation for Universal Asynchronous Receiver/Transmitter.

An x means that the test executes with or without the specified hardware item.

Req means that the specified hardware is required for the test to execute.

Opt means that the specified hardware is optional.

Skipped means that the test is not executed.

2.3.1 Test 1 -- Self-Test Started by TILINE I/O Reset
Test 1 verifies that a board is present, and then monitors the operation of the CI403 and CI404 self-test that is initiated by an I/O reset. An I/O reset is performed and the board identification number is verified against the number in slave word 0.

2.3.2 Test 2 -- Self-Test Started by Write to Slave Word 0
Test 2 monitors the operation of the CI403 self-test that is initiated by the CPU. The test verifies that a board is present and that the board identification number is verified against the number in slave word 0.

2.3.3 Test 3 -- MUX Timer Function Test
Test 3 monitors the 250MS onboard clock for four cycles by checking it against the AC line frequency to the system. If the clock does not meet specifications, an error message is displayed.

2.3.4 Test 4 -- UART Interface Data Path Test
Test 4 checks the 990 system data path through the UART's internal data register. It writes data internally to the four UARTs onboard and verifies that the resulting data is correct.

2.3.5 Test 5 -- Internal Loopback Data Transfer Test
Test 5 transfers 16 bytes to the UARTs in an internal loopback mode and verifies that the data was transferred.

2.3.6 Test 6 -- Transmit FIFO Control Test
Test 6 checks the first-in, first-out (FIFO) control circuitry is functioning correctly by transferring data and monitoring the results.

2.3.7 Test 7 -- Channel Baud Rate Test
Test 7 transfers one second's worth of data in an internal loopback mode at each of the baud rates used by the CI403 or CI404 board. This test executes in approximately 90 seconds.

2.3.8 Test 8 -- RS-232-C Interface Test
Test 8 executes on the CI403 board only. You must install an external loopback plug to execute this test. Test 8 exercises RS-232-C control signals to an external loopback and monitors their return. This test is skipped if you specified fiber optic testing during MUXTST initialization.

2.3.9 Test 9 -- Half Duplex EIA Data Test
Test 9 executes on the CI403 board only. It transfers one byte of data through the EIA drive receivers in the full-duplex mode, and then one byte is transferred in the half-duplex mode. Then the EIA interface is checked for proper half-duplex operation. You must install an external loopback connector to execute this test.

2.3.10 Test A -- Data Loopback 5 Bit Test

Test A executes in modem configuration. You must install an external loopback connector to execute this test. Test A transfers and receives 5-bit groups of data through an external loopback at 19.2K baud for the CI403 board and 38.4K baud for the CI404 board. The data received is compared to the data that was transmitted to check for errors.

2.3.11 Test B -- Data Loopback 6 Bit Test

Test B executes in modem configuration. You must install an external loopback connector to execute this test. Test B transfers and receives 6-bit groups of data through an external loopback at 19.2K baud for the CI403 board and 38.4K baud for the CI404 board. The data received is compared to the data that was transmitted to check for errors.

2.3.12 Test C -- Data Loopback 7 Bit Test

Test C executes in modem configuration. You must install an external loopback connector to execute this test. Test C transfers and receives 7-bit groups of data through an external loopback at 19.2K baud for the CI403 board and 38.4K baud for the CI404 board. The data received is compared to the data that was transmitted to check for errors.

2.3.13 Test D -- Data Loopback 8 Bit Test

Test D executes in modem configuration. You must install an external loopback connector to execute this test. Test D transfers and receives 8-bit groups of data through an external loopback at 19.2K baud for the CI403 board and 38.4K baud for the CI404 board. The data received is compared to the data that was transmitted to check for errors.

3.1 MESSAGES

MUXTST issues two types of messages: informative and error messages. The following paragraphs discuss each type.

3.1.1 Informative Messages

Informative messages indicate the start and completion of tests, providing you with a brief test description. As each test begins, MUXTST issues a message in the following format:

```
TEST XX (.....test description.....)
```

When a test begins executing, it checks for a required channel configuration. If the channel is not in the required configuration, MUXTST skips the test and issues the following message:

```
**** S K I P P E D ****
```

When the test completes, the following message is displayed:

```
TEST XX COMPLETE
```

Tests 4 through D contain the following additional message in this format:

```
TESTING 0 1 2 3
```

This message indicates the channel test configuration that you specified during initialization. For example, if did not want to test channels 0 and 2, the preceding message would be as follows:

```
TESTING 1 3
```

3.1.2 Error Messages

When errors occur in a test, an error message is displayed. These messages help you to locate a fault in the unit under test. MUXTST provides the following error messages:

Error Number	Error Message
>0001	**** ERROR MUX TILINE TIME OUT **** PROBABLE CAUSES ARE: 1) MUX IS NOT INSTALLED 2) MUX IS NOT AT THE TILINE BASE SPECIFIED 3) MUX TILINE INTERFACE LOGIC
>0002	**** MUX SELF-TEST WAS NOT PROPERLY STARTED BY TILINE I/O RESET **** PROBABLE CAUSES ARE: 1) MUX MASTER RESET LOGIC 2) CLOCK GENERATOR LOGIC 3) 'TLIORES' NOT REACHING THE MUX
>0003	**** MUX SELF-TEST WAS NOT PROPERLY STARTED BY SLAVE WORD WRITE **** PROBABLE CAUSES ARE: 1) MUX TILNE WRITE INTERFACE LOGIC (SW0) 2) MUX MASTER RESET LOGIC
>0004	**** TIME OUT MUX SELF-TEST **** PROBABLE CAUSES ARE: 1) MUX TILINE INTERFACE LOGIC READ (SW0) 2) MUX INTERNAL LOGIC
>0005	**** MUX FAILED CHANNEL ERROR REPORTED **** PROBABLE CAUSES ARE: 1) MUX INTERNAL LOGIC 2) ACE (UART) ON FAILING CHANNEL
>0006	**** MUX TIMEOUT ERROR READ ACE REG 7 **** PROBABLE CAUSES ARE: 1) MUX TILINE INTERFACE LOGIC (SW1) 2) MUX INTERNAL LOGIC
>0007	**** MUX TYPE ID ERROR HARDWARE IS NOT CI403 **** PROBABLE CAUSES ARE: 1) WRONG TYPE SELECTED IN "IT" VERB 2) ERROR WHEN READING ID FROM SLAVE WORD 0

Error Number	Error Message
>0008	**** MUX TYPE ID ERROR HARDWARE IS NOT CI404 ****
	PROBABLE CAUSES ARE:
	1) WRONG TYPE SELECTED IN "IT" VERB
	2) ERROR WHEN READING ID FROM SLAVE WORD 0
>0009	**** MUX FAILED SELFTEST WITH UNDEFINED ERROR CODE ****
>000A	**** ERROR IN MUX TIMER FUNCTION TEST ****
	PROBABLE CAUSES ARE:
	1) MUX TIMER GENERATION LOGIC
	2) SYSTEM POWER LINE FREQUENCY ERROR
>000B	**** ERROR IN MUX ACE (UART) DATA PATH TEST ****
	PROBABLE CAUSES ARE:
	1) MUX TILINE INTERFACE LOGIC (SW1)
	2) MUX INTERNAL LOGIC OR ACE (UART)
>000C	**** ERROR INTERNAL DATA LOOPBACK TEST ****
	PROBABLE CAUSES ARE:
	1) MUX TILINE INTERFACE LOGIC TRANSMIT AND RECEIVE FIFO LOGIC (SW2 & SW3)
	2) MUX INTERNAL LOGIC OR ACE (UART)
	3) INTERRUPT NOT WIRED IN SYSTEM
>000D	**** ERROR TRANSMIT FIFO CONTROL TEST ****
	PROBABLE CAUSES ARE:
	1) MUX INTERNAL LOGIC
	2) MUX TILINE INTERFACE LOGIC (SW1)
>000E	**** ERROR IN CHANNEL BAUD RATE TEST ****
	PROBABLE CAUSES ARE:
	1) MUX CLOCK LOGIC OR ACE (UART)
	2) SYSTEM POWER LINE FREQUENCY ERROR
>000F	**** ERROR RS-232C INTERFACE TEST ****
	PROBABLE CAUSES ARE:
	1) LOOPBACK SELECTED DOES NOT MATCH HARDWARE
	2) LOOPBACK CONNECTOR IS NOT INSTALLED
	3) EIA DRIVER OR RECEIVER OR UART
	4) CABLE IN LOOPBACK IS BROKEN

	USE THE "IT" VERB TO SELECT A LOOPBACK POINT NEARER THE CARD EDGE TO ISOLATE THE FAILURE

Error Number	Error Message
>0010	**** ERROR HALF-DUPLEX EIA DATA TEST **** PROBABLE CAUSES ARE: 1) LOOPBACK CONNECTOR IS NOT INSTALLED 2) EIA DRIVER, RECEIVER, UART HALF-DUPLEX LOGIC 3) CABLE IN LOOPBACK IS BROKEN --- USE THE "IT" VERB TO SELECT A LOOPBACK POINT NEARER THE CARD EDGE TO ISOLATE THE FAILURE ---
>0011	**** ERROR IN DATA LOOPBACK TEST **** PROBABLE CAUSES ARE: 1) DATA LOOPBACK IS NOT INSTALLED 2) BROKEN CABLE IN LOOPBACK DATA PATH 3) BROKEN MODEM IN LOOPBACK DATA PATH 4) MUX DATA PATH LOGIC --- USE THE "IT" VERB TO SELECT A LOOPBACK POINT NEARER THE CARD EDGE TO ISOLATE THE FAILURE ---

Appendix A

Cross-Reference of ASCII Characters with Hexadecimal Codes

ASCII Character	Hex Code	ASCII Character	Hex Code
NUL	00	0	30
SOH	01	1	31
STX	02	2	32
ETX	03	3	33
EOT	04	4	34
ENQ	05	5	35
ACK	06	6	36
BEL	07	7	37
BS	08	8	38
HT	09	9	39
LF	0A	A	41
VT	0B	B	42
FF	0C	C	43
CR	0D	D	44
SO	0E	E	45
S1	0F	F	46
DLE	10	G	47
DC1	11	H	48
DC2	12	I	49
DC3	13	J	4A
DC4	14	K	4B
NAK	15	L	4C
SYN	16	M	4D
ETB	17	N	4E
CAN	18	O	4F
EM	19	P	50
SUB	1A	Q	51
ESC	1B	R	52
FS	1C	S	53
GS	1D	T	54
RS	1E	U	55
US	1F	V	56
SPACE	20	W	57
!	21	X	58
.	2E	Y	59
/	2F	Z	5A
?	3F	DEL	7F

Appendix B

Loopback Modes

B.1 INTRODUCTION

The communications diagnostic tests can take various paths through the communications system under test. The path selected depends on the loopback mode that you choose during test initialization. This appendix explains which system components are tested in each mode and the prerequisites to the use of each mode.

The communications tests run in either internal (IN) mode or one of three external modes:

* Digital loopback (DI) mode
* Analog loopback (AL) mode
* Far-end loopback (FE) mode

When a loopback connector, modem, or transmission medium is installed, the test may be placed in an external mode; the test must be run in internal mode when none of these devices is present. Most tests require you to use the loopback connector that has LEDs (part number 948550-0001, revision *C or later). The LEDs on the connector indicate the condition of bit signals that are not looped back. The LED connector also loops back an internal test clock to the transmit and receive receivers. It allows full external loopback testing in synchronous mode. Figure B-1 illustrates the signals that are looped back and the pin assignments in the loopback connector.

It is recommended that you run the test first in internal mode and then progress through digital, analog, and then far-end mode if the system configuration permits and you have the necessary test equipment. Table B-1 lists the parts of the system that are tested in each test mode. Figure B-2 illustrates the testing path each mode takes.

The system under test may be entirely local or it may be a local system connected by transmission media to a remote CPU and communications interface in a different area. The transmission medium may be a telephone line to another city or a twisted cable to the next room.

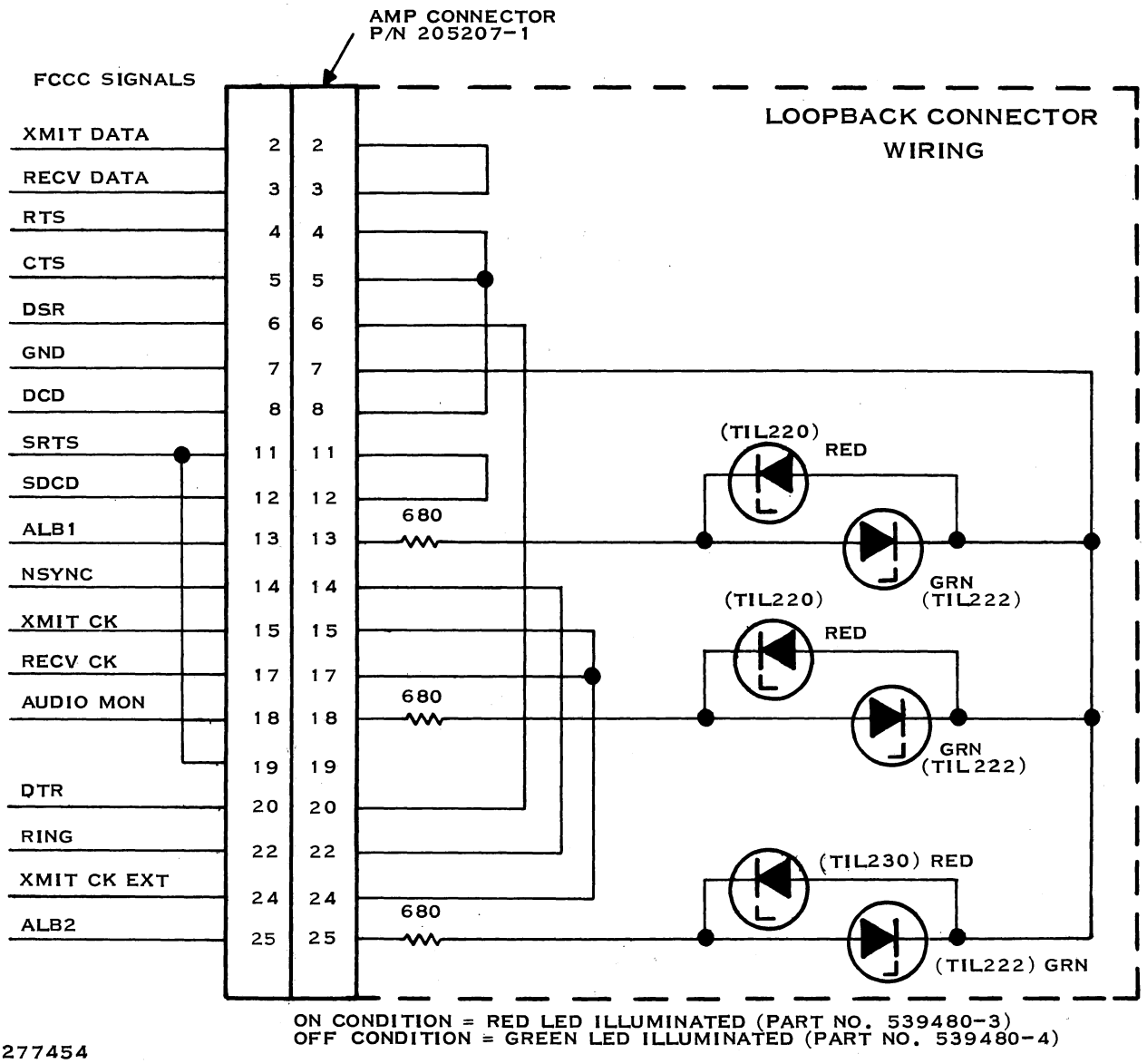


Figure B-1. Loopback Connector Wiring

Table B-1. System Components Tested in Test Modes

	Component Tested				
Test Mode	Local Inter-Face	Local Modem Cable	Local Modem	Trans-Mission Medium	Remote Modem
Internal	yes	no	no	no	no
External:					
Digital	yes	yes*	no	no	no
Analog	yes	yes	most	no	no
Far-End:					
A-local line loopback	yes	yes	yes	no	no
B-remote line loopback	yes	yes	yes	yes	no
C-remote modem analog loop-back switch	yes	yes	yes	yes	partial
D-remote CIM with RT verb	yes	yes	yes	yes	yes

Note:

If the loopback connector is used on the modem end of the cable

B.1.1 Internal Loopback Mode

Internal mode loops back digital signals on the local communications interface, testing most of the on-board circuitry. No additional hardware or special test equipment is required. This mode can be used when you want to eliminate the CPU and communications interface as the source of errors found when a test is executed under another test mode.

B.1.2 Digital Loopback Mode (External)

Digital mode tests the local communications interface and, optionally, the interface-to-modem cable. Install a loopback

connector at the modem end of the cable to test both the cable and the interface or at the interface connector to test only the interface.

B.1.3 Analog Loopback Mode (External)

Analog mode loops back signals at the output of the local modem and tests the communications interface circuitry, the interface-to-modem cable, and most of the local modem. The transmission medium and any hardware beyond the local modem are not tested in this mode.

Analog mode can be used only with TI modems or with vendor modems that have a manual analog loopback switch. Vendor modems do not normally respond to the analog loopback signal.

B.1.4 Far-End Mode (External)

Far-end mode tests the local modem and the components beyond this device. This mode is used when the modems on both ends of the system are capable of full-duplex operation and a four-wire line is used between them. In this case, the far-end modem can be placed in digital loopback mode to allow signals to be transmitted to the far-end modem and looped back to the local system. This provides a quick check of the local system, the transmission medium, and the far-end modem.

A few modems (such as the Bell 212A) are capable of full-duplex operation on two-wire systems, including the switched telephone network. If this type modem is used at both the local and remote sites in a system, digital loopback of the far-end modem is possible on a two-wire system.

Far-end loopback mode has a loopback path at the remote modem where the analog signals transmitted to the remote modem are converted to digital signals, looped back, converted back to analog, and then transmitted back to the local system.

There are four loopback points available when using far-end mode. The points that can be used depend on how the system is configured. These points are discussed in the following paragraphs.

B.1.4.1 Point A -- Local Line Loopback. When you make a loopback connection at this point, signals are looped back at the local modem and that unit is included in the testing. (See item A in Figure B-2.)

B.1.4.2 Point B -- Remote Line Loopback. When you make a loopback connection at this point, the test transmits signals through the transmission medium up to but not including the remote modem and then loops these signals back. (See item B in Figure B-2.)

B.1.4.3 Point C -- Remote Modem Analog Loopback Switch. A loopback connection at this point loops back signals at the remote modem. (See item C in Figure B-2.)

B.1.4.4 Point D -- CIM with RT Verb. A loopback connection can be made at this point when testing a four-wire, full-duplex system that uses TI internal modems and the CIM module as the remote communications interface. The signals are looped back at the far-end CIM. You must enter the CRCOMM test verb RT on the remote system when using this loopback point or set switch 8 on the CIM to Remote Test (ON). (See item D in Figure B-2.)

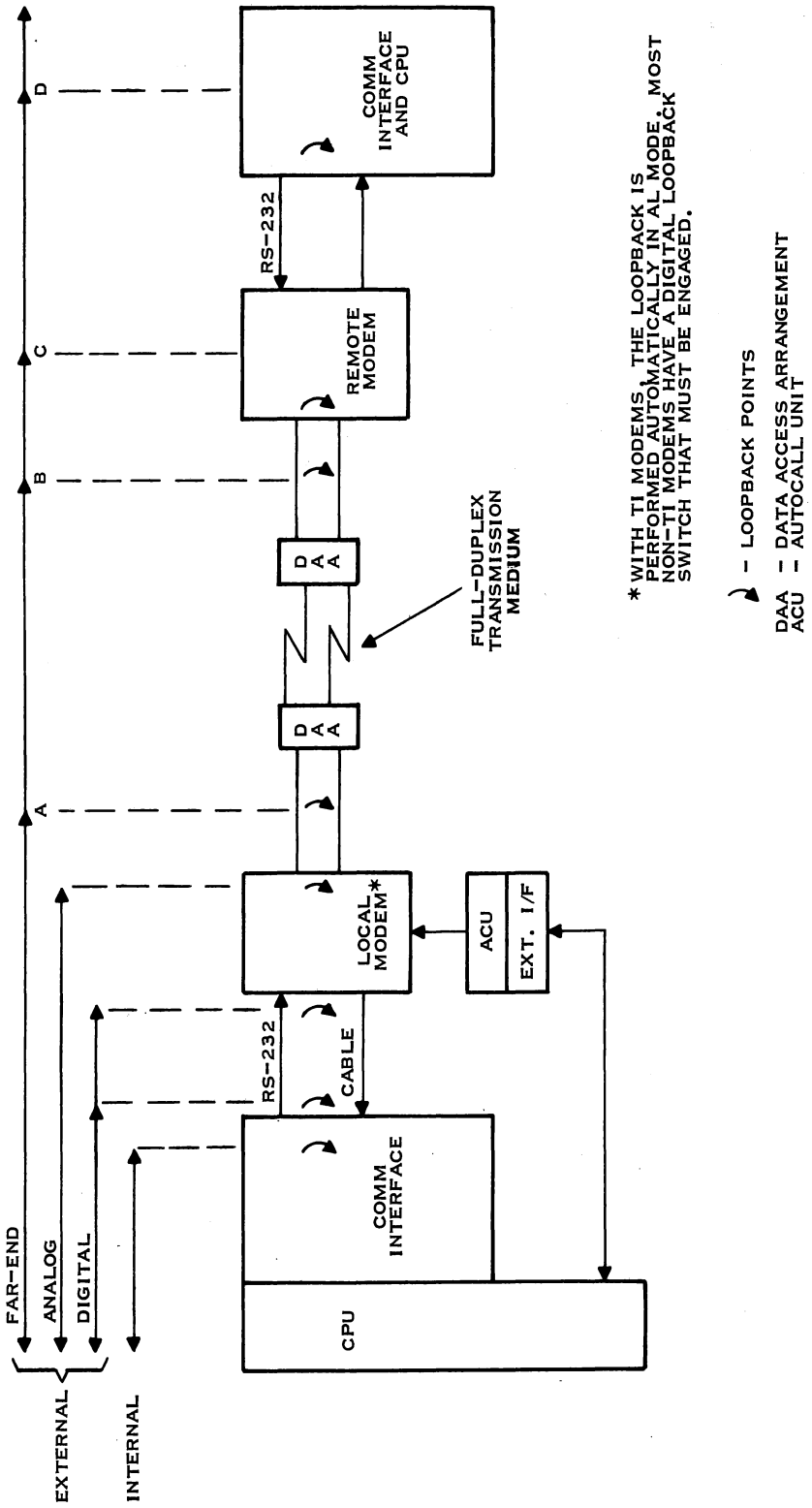


Figure B-2. Communications Systems Test Paths

CUT ALONG LINE

USER'S RESPONSE SHEET

Manual Title: Unit Diagnostics Handbook, Volume 6, Diagnostics for 990 Communications Interfaces (945400-9706)

Manual Date: April 1985 **Date of This Letter:** _____

User's Name: _____ **Telephone:** _____

Company: _____ **Office/Department:** _____

Street Address: _____

City/State/Zip Code: _____

Please list any discrepancy found in this manual by page, paragraph, figure, or table number in the following space. If there are any other suggestions that you wish to make, feel free to include them. Thank you.

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