SPERRY UNIVAC®

PRIORITY INTERRUPT MODULE OPERATION AND SERVICE MANUAL

UP-8630

98 A 9902 428

FEBRUARY 1978

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Printed in U.S.A.

CHANGE RECORD

Page Number	Issue Date	Change Description
Various	2/78	Deleted all references to Varian.

Change Procedure:

When changes occur to this manual, updated pages are issued to replace the obsolete pages. On each updated page, a vertical line is drawn in the margin to flag each change and a letter is added to the page number. When the manual is revised and completely reprinted, the vertical line and page-number letter are removed.

LIST OF EFFECTIVE PAGES

Page Number	Change in Effect
All	Complete revision

96A0731-000B

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SECTION 1
GENERAL DESCRIPTION

The Priority Interrupt Module is an I/O option available with 70 series and 620 computer systems. This manual is divided into six sections:

- Features and specifications
- Installation and interconnection
- Operation
- Theory of Operation
- Maintenance
- Mnemonics list

Documents such as logic diagrams, schematics, and parts lists are supplied in a system documentation package. This package is assembled when the equipment is shipped, and reflects the configuration of a specific system.

The following list contains the part numbers of other manuals pertinent to the V70 series computers (the x at the end of each document number is the revision number and can be any digit 0 through 9):

V70 Series Architecture Reference Manual	98A 9906 00X
V70 Series Processor Manual	98A 9906 02X
V70 Series Option Board	98A 9906 05X
V77-600 Computer System Description	98A 9906 40X
V77-400 Computer System Description	98A 9906 41X
V77-200 Computer System Description	98A 9906 42X
V77-400 Processor Operation and Service Manual	98A 9906 43X
V77-200 Processor Manual	98A 9906 50X
V77-800 Processor Manual	98A 9906 61X

The priority interrupt module (PIM) provides for the orderly servicing of peripheral-initiated interrupts of a program in progress. It does so by:

a. Establishing up to eight levels of interrupt priority for selected peripheral controllers.

b. Storing interrupt requests originated by associated peripheral controllers and placing the requests on the I/O bus in the order of the established priority.

In effect, the PIM organizes a "priority-within-a-priority" system. Peripheral controllers that cannot normally initiate an interrupt because of their inability to generate memory addresses can do so when connected to the PIM. PIM-controlled priority assignments are prewired at the factory to user specifications.

Table 1-1 lists the PIM specifications.

Table 1-1. PIM Specifications

Parameter	Description
Organization	Contains line synchronization, and mask registers; an interrupt address generator; priority and control logic; and line drivers and receivers
Control Capability	Establishes and implements eight levels of interrupt priority (user-assigned) for system peripheral controllers.
I/O Capability	Five external control and three transfer instructions
Standard Device Address	040 through 043
Interrupt Addresses	First PIM: 0100 through 0117 Second and succeeding PIMs: 0120 through 0177

Table 1-1 PIM Specifications (continued)

System Priority Assignment	Determined by location in the system priority chain (user-selected)
Logic levels (internal)	High = +2.4 to +5.0V dc Low = 0 to +0.4V dc
Logic levels (I/O bus)	High = +2.8 to +3.6V dc Low = 0 to +0.5V dc
Size	Contained on one 7-3/4-by-12-inch (19.7 x 30.3 cm) printed-circuit board.
Power	5V dc at 0.45A
Operating Environment	0 to 50 degrees C, 0 to 90 percent relative humidity without condensation.

SECTION 2
INSTALLATION

2.1 INSPECTION

The PIM has been packed and inspected to ensure its arrival in good working order. To prevent damage, take care during unpacking and handling. Check the shipping list to ensure that all equipment has been received. Immediately after unpacking, inspect the equipment for shipping damage. If damage exists:

a. Notify the transportation company.

b. Notify Sperry Univac.

c. Save all packing material.

2.2 PHYSICAL DESCRIPTION

The PIM circuits are contained on a single printed-circuit (PC) board (p/n 44P0683). As illustrated in figure 2-1, the board contains three connectors P1, J1, and J2. Connectors J1 and J2 each contain eight interrupt lines (IL00- through IL07-) that can be connected to selected peripheral controllers. Connector P1 also contains the same eight interrupt lines as well as all I/O bus control signals for the PIM.

2.3 PIM INTERRUPT LINES

The PIM has eight interrupt lines that enable up to eight peripheral controllers to be connected in the desired order of priority. The interrupt lines are designated IL00- through IL07-, where IL00- has the highest priority and IL07- the lowest. For controllers that are installed in the same chassis as the PIM, the interrupt lines are connected at the computer backplane connector that mates with P1 of the PIM board. For controllers in a different chassis, the interrupt lines are contained in either an I/O expansion cable that connects to P1 of the PIM (via computer backplane) or in an interrupt cable that connects to J1 or J2 of the PIM. Pin assignments for the interrupt lines are listed in table 2-1.

Table 2-1. Pin Assignments for Interrupt Lines

Interrupt Lines	P1	J1	J2	Interrupt Lines	P1	J1	J2
IL00-	108	3	3	IL04-	102	11	11
IL01-	114	13	13	IL05-	88	5	5
IL02-	104	9	9	IL06-	112	1	1
IL03-	110	15	15	IL07-	86	7	7

2.4 DEVICE ADDRESS ASSIGNMENT

The device address for each PIM is implemented with jumper wires installed on the computer backplane connector that mates with P1 of the PIM board (figure 2-2). Device addresses 040 through 043 are reserved for PIM. Normally 040 is assigned to the first PIM, 041 to the second, 042 to the third, and 043 to the fourth. Address 044 affects all PIMs simultaneously and is used to enable or disable all PIMs.

2.5 INTERCONNECTION

In the V70 series systems, the PIM is installed in a designated slot of an I/O chassis. Refer to the appropriate system reference manual for further installation information.

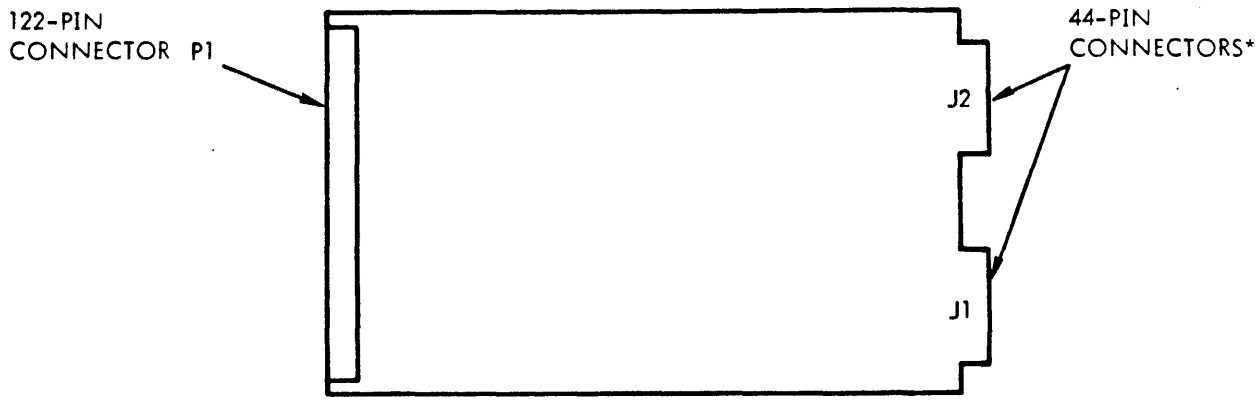

Figure 2-1. PIM Board (Component Side)

The PIM can be installed in designated slots of the mainframe and expansion chassis for 620/L systems. Further installation information for these computer systems, can be found in the 620/L Maintenance Manual (document number 98 A 9905 15x).

The PIM can be installed in the 77-400/200 mainframe or expansion chassis "S" slot connector plane. Further information for these computer systems can be found in the 77-400 and 77-200 System Reference Manuals and in the 77-400/200 Configuration Guide.

The pin assignments for the connectors on the PIM board are provided in logic diagram 91D0016.

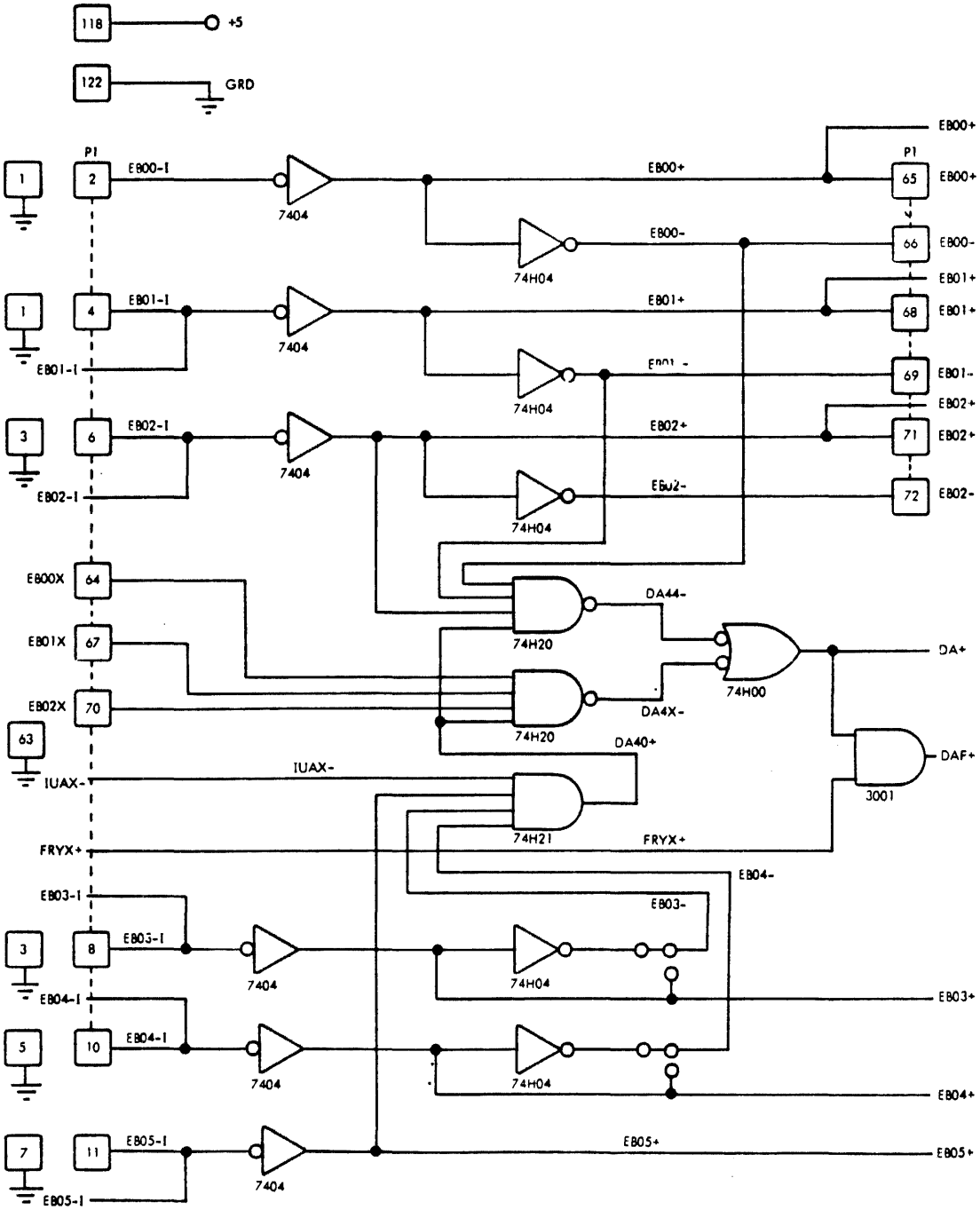

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Figure 2-2. Device Address Connections

SECTION 3
OPERATION

The PIM has no operating controls or indicators. It operates under program control.

3.1 I/O INSTRUCTIONS

The PIM responds to the five external control and three data transfer instructions listed in table 3-1.

loops. Two NOP instructions are required after an external control (EXC) instruction.

For computer systems containing the memory protection (MP) option in addition to the PIM, the MP is disabled everytime an interrupt is serviced. Therefore at the end of the PIM service program, the MP must be enabled again.

Table 3-1. I/O Instructions

Mnemonic	Program Code	Functional Description
External Control		
EXC 014*	10014*	Clear interrupt registers.
EXC 024	10024	Enable PIM.
EXC 0244	100244	Enable all PIMs in system.
EXC 034	10034	Clear interrupt registers and enable PIM.
EXC 044	10044	Disable PIM.
EXC 0444	100444	Disable all PIMs in system.
EXC 054	10054	Clear interrupt registers and disable PIM.
Data Transfer		
OME 04	10304	Transfer contents of memory to mask register.
OAR 04	10314	Transfer contents of A register to mask register.
OBR 04	10324	Transfer contents of B register to mask register.

*** represents the last octal digit of the device address.**

3.2 PROGRAMMING CONSIDERATIONS

When preparing a PIM program, clear the interrupt registers to establish initial conditions. To mask peripheral controllers, write a mask word in the program. The eight least significant bits of the mask word correspond to the eight priority interrupt lines. Setting bit 0 inhibits the highest priority line, setting bit 1 inhibits the second-highest priority line, etc. The mask register must be loaded by the program after any power-up sequence, including the power-up cycle of the power failure/restart (PF/R) feature. System reset does not clear the PIM mask register.

When program loops contain only uninterruptable instructions, interrupts cannot occur. Thus, when recognition of an interrupt is imperative (such as with the PF/R), at least one no-operation (NOP) instruction must be added to such

3.3 UNINTERRUPTABLE INSTRUCTIONS AND CONDITIONS

An interrupt can be detected only during the last cycle of an instruction execution. In V70 systems using the memory protection feature, interrupts can be detected immediately following all instructions except:

a. Halt (HLT) instructions

b. Any external control (EXC) I/O instruction

c. Any execution instruction. If the condition is met, interrupts are inhibited between executions of an execution instruction and the instruction at the execution address. If the condition is not met,

interrupts are inhibited between executions of an execution instruction and the instruction following in sequence.

d. Any instruction executed in the step mode.

In 70 series systems without the memory protection feature, detection of an interrupt is inhibited during the following types of instructions:

a. Halt (HLT) instructions

b. All shift instructions

c. All I/O instructions

d. All double-word instructions

e. All multiplication or division instructions

f. Any instruction executed in the step mode

In all 620/L systems, detection of an interrupt is inhibited during the following types of instructions and conditions:

a. Halt (HLT) instructions

b. All jump, jump and mark, or execution instructions when the jump condition is met. (When the jump condition is not met these instructions are interruptable).

c. All I/O instructions

d. All shift or rotation instructions

e. All multiplication or division instructions

f. During the processor cycle immediately following an external control (EXC) I/O instruction.

g. During the processor cycle immediately following a shift, rotation, multiplication, or division instruction during which a trap occurred (DMA operation).

h. During the first instruction executed after entering run mode if that instruction is a single-word instruction.

i. During a manual step operation

j. During a halt condition

Refer to the 77-400 and 77-200 processor manuals for the uninterruptable instructions and conditions for those computer systems.

3.4 PROGRAM EXAMPLE

Table 3-2 shows a typical program using the PIM. In this program, 256 descending binary frames are transferred to the high-speed paper tape punch. Memory locations 01000 to 01023 are used in the program as are computer mnemonic codes with corresponding machine language codes.

Table 3-2. Program Example

Machine Code		Source Code			
Location	**Instruction**	**Label**	**Mnemonic**	**Operand**	**Description**
001000		STRT	.ORG	.01000	
001000	011011		.LDA	.MASK	FETCH INTERRUPT MASK
001001	103140		.OAR	.040	AND STORE IN REGISTER
001002	006010		.LDAI	.0377	INITIALIZE OUTPUT DATA
001003	000377				
001004	103137		.OAR	.037	PRIME INTERRUPT MODULE
001005	100240		.EXC	.0240	ENABLE PIM
001006	005000		.NOP	.	
001007	001000		.JMP	.-1	DELAY FOR INTERRUPTS
001010	001006				
001011	000376	MASK	.DATA	.0376	
		INTERRUPT	PROCESSING	SUBR	
001012	000000	INTR	.ENTR	.	
001013	005311		.DAR	.	DECR OUTPUT DATA
001014	103137		.OAR	.037	OUTPUT DATA TO PUNCH
001015	100240		.EXC	.0240	RE-ENABLE PIM
001016	001010		.JAZ	.+4	
001017	001022				
001020	001000		.JMP*	.INTR	EXIT
001021	101012				
001022	100440		.EXC	.0440	CLEAR PIM
001023	000000		.HLT	.	END OF PROGRAM
		INTERRUPT	ADDRESS		
000100			.ORG	.0100	
000100	002000		.JMPM	.INTR	
000101	001012				
	000000		.END	.	

SECTION 4
THEORY OF OPERATION

4.1 GENERAL

Communication between the PIM and the processor is similar to that of any peripheral controller except that the PIM can request a program interrupt. When the computer acknowledges the interrupt, the PIM specifies the memory location of the instruction to be executed.

The PIM scans the interrupt lines with every cycle of the interrupt clock (IUCX-I). If signals are detected on more than one line, the highest-priority signal is acknowledged. The remaining interrupt requests are stored in the PIM interrupt-line register until acknowledged. The PIM has an eight-bit mask register that selectively inhibits interrupt requests from the interrupt-line register. When a given flip-flop of the mask register is set, corresponding interrupt requests from the interrupt-line register are inhibited. When the mask register flip-flop is reset, the interrupt request is not inhibited. The mask register is unaffected by system reset and must be loaded under program control using data-transfer instructions.

Acknowledgment of an interrupt by the processor causes execution of the instruction located at the memory address specified by the PIM. Any instruction can be executed except an I/O type. An interrupt is thus serviced in one instruction period.

4.2 FUNCTIONAL DESCRIPTION

The following subsections describe the five functional circuits of the PIM (figure 4-1). Refer to the timing waveforms of figure 4-2 and the PIM logic diagram.

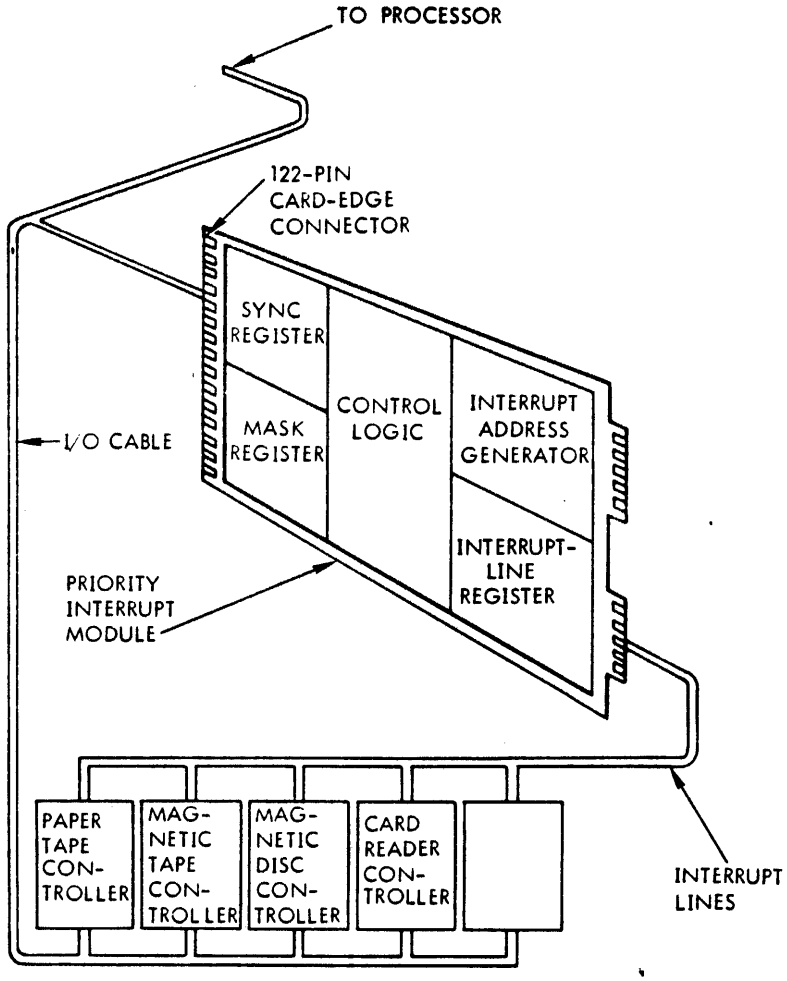

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Figure 4-1. PIM Functional Block Diagram

4.2.1 Control Logic

The control logic circuit directs and sequences the response of the PIM to external control, data transfer, and interrupt operations. When a computer program interrupt is requested, the processor requests the PIM to place the interrupt address on the I/O bus. If the PIM has system priority, the address line drivers are enabled. The PIM interrupt-request signal will remain active until all interrupts stored (but not inhibited) by the PIM have been acknowledged, or until PIM priority is lost.

The control logic circuit consists of flip-flops PRME, DTOX, IURM and associated gates. During the execution of an output data transfer command, signals FRYX and DA set DTOX. DTOX + high and DRYX + generate SMR1- low, which transfers the mask word from the I/O bus to the mask register. At the end of the transfer, DRYX + resets flip-flop DTOX. DA, in conjunction with FRYX +, indicates that the central processor is communicating with the PIM.

External control commands for the PIM are indicated by EXCX + low. EB06 +, EB07 +, and EB08 + are combined with EXCX + to actuate the five external control commands.

Flip-flop PRME provides master enable/disable for the entire PIM. When PRME is reset, computer program interrupts cannot be requested by the PIM; however, the PIM continues to receive and store interrupts from external devices. When PRME + is high, flip-flop IURM is set by INR1 + high, one IUCX-I clock period after an interrupt is clocked into the sync register. IURM + and PRME + high plus PRMX-I low generate IURX-I low, requesting an interrupt.

When a computer program interrupt is requested by the PIM, the processor responds with signal IUAX-I low. This signal requests that PIM place the interrupt instruction address on the I/O bus.

If the PIM has system priority, the address line drivers are enabled as long as IUAX-I is low. When IUAX-I goes low, IUCX-I is held low. Interrupt conditions are therefore held static during the time that IUAX-I is low. Flip-flop IURM is cleared when all interrupts received by the PIM have been acknowledged by the central processor.

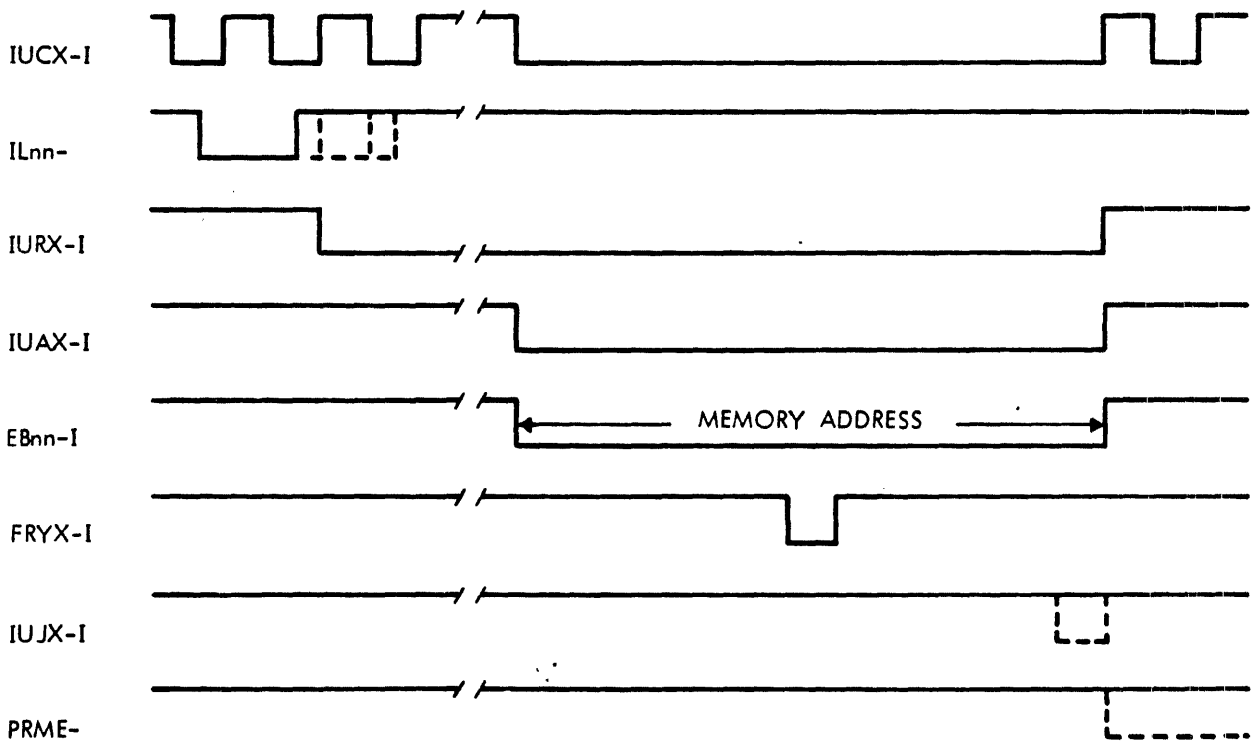

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Figure 4-2. Timing for Reception and Servicing of a Single Interrupt

4.2.2 Interrupt Address Generator

The interrupt address generator consists of coding logic that generates the binary number of the interrupt line requesting the interrupt. A pair of memory locations is reserved for each interrupt line. The interrupt addresses are normally in memory locations 0100 through 0117. However, the 16 interrupt addresses can be placed anywhere within the first 128 memory locations except 040 through 047, and may be placed at other addresses by special request.

The interrupt address generator consists of three gates that use line priority signals to generate signals A0XX+, A1XX+, and A2XX+. These signals consititute three bits of the address code for the interrupt line to be serviced. They are placed on the I/O bus by IAEX+ low. The least-significant bit of the address code is always low, resulting in an even address. This bit is supplied by the processor when the second word of a double-word interrupt instruction is accessed.

Signal IAEX+ low is generated by signals PRMX-I and IUAX-I low and FF set signal PRME+ and IURM+ high. These four signals indicate, respectively, that: the PIM has priority; the PIM interrupt has been acknowledged; the PIM is activated; and interrupt awaits on one of the interrupt lines.

4.2.3 Interrupt-Line Register

The interrupt-line register consists of eight flip-flops that asynchronously accept interrupt inputs. An interrupt is stored in the register until the interrupt is serviced or until the entire register is cleared by command.

The interrupt-line register consists of flip-flops LR00 through LR07. An interrupt is generated when an interrupt line signal, ILnn−, goes low. IL00− through IL07− are each connected to the clock input of an interrupt-line register flip-flop. ILnn− may remain low for any period of time greater than 0.2 microseconds; a constant low does not produce repetitive interrupts. If the interrupt is serviced, the flip-flop is reset by IUCP+ and a line priority signal, LPnn+. Although IUCP+ is sent to all register flip-flops, only the flip-flop that was serviced is reset.

4.2.4 Sync Register and Line Priority

The sync register consists of eight flip-flops. At each interrupt clock period, the outputs of the interrupt-line register are clocked into the sync register. The sync register, therefore, samples the status of the eight interrupt lines synchronously with the computer interrupt clock. The sync register outputs activate the priority logic used to generate the interrupt address.

If two or more interrupts occur simultaneously, the line with the highest priority is given precedence and all other lines are temporarily inhibited. An interrupt line can request a computer program interrupt only if the line has not been inhibited and a higher-priority line is not active.

The sync register consists of flip-flops IR00 through IR07. IUC1− clocks the contents of the interrupt-line register into the sync register. The outputs of the sync register are fed into a network of gates that determine the priority of each interrupt line signal. The line priority circuit generates signal INR1+, which enables the generation of signal IURX−I. In addition, LP00+ through LP07+ determine the interrupt address and the interrupt-line register flip-flop to be reset after servicing its interrupt. IL00− has the highest priority, and signal IL07− has the lowest.

4.2.5 Mask Register

The mask register inhibits interrupt requests from selected interrupt lines to be disarmed while other lines are permitted to cause a program interrupt. The eight flip-flops of the mask register inhibit corresponding interrupt requests from the interrupt-line register. The mask register must be loaded under program control to establish which interrupts are to be inhibits.
EB00+ through EB07+ are loaded into the mask register when a particular interrupt is to be masked (inhibited). SMR1+ clocks this mask word into the register. The register outputs are fed into the line priority circuit. If one or more interrupts are inhibited by the mask register, the highest-priority unmasked interrupt is serviced.

SECTION 5
MAINTENANCE

Maintenance personnel should be familiar with the contents of this manual before attempting PIM troubleshooting. The MAINTAIN III test program system (Test Programs Manual, 98 A 9952 07x) contains a PIM test program used to test various phases of PIM operation. Further diagnosis can then be made by referring to this manual.

5.1 TEST EQUIPMENT

The following test equipment and tools are recommeded for maintenance:

a. Oscilloscope, Tektronix type 547 with dual-trace plug-in unit, or equivalent.

b. Multimeter, Triplett type 630 or equivalent.

c. Soldering iron, 39-watt pencil type.

5.2 CIRCUIT-BOARD REPAIR

If it has been determined that circuit-board repair is required, it is recommended that the Sperry Univac customer service department be contacted so that a new circuit board can be installed in the user's system and the faulty one returned to the factory for repairs. However, if the user decides to perform his own repairs, caution should be used so that the circuit board is not permanently damaged. Approved repair procedures should be followed such as the ones described in document IPC-R-700A prepared by the Institute of Printed Circuits.

SECTION 6
MNEMONICS

Mnemonics	Description
AnXX	Address code of device with priority interrupt.
CACR	Clear ac register. Generates signal CILR on receipt of signal EXCX.
CILR	Clear line register. Clears the line and sync registers.
DA	Decoded device address.
DRYX	Data ready pulse that resets flip-flop DTOX; enables signal SMR1.
DTOX	Data transfer out flip-flop. Stores the occurrence of an output command from the processor.
EBnn-I	Address or function code bit from I/O bus.
EXCX	Enables initialization of PIM upon external control command.
FRYX	Function ready pulse that sets flip-flop DTOX.
IAEX	Interrupt address enable. Gates address of interrupt line onto I/O bus.
ILnn	Interrupt line from peripheral controller.
INRn	Interrupt request. Indicates a request from one or more interrupt lines.
IRnn	Sync register outputs. Stores the status of the line register in synchronism with the interrupt clock signal.
IUAX	Interrupt acknowledgment. Enables servicing of PIM interrupts.
IUCP	Interrupt completion resets line register flip-flop after interrupt is serviced.
IUCX	Interrupt clock. Provides timing for servicing of PIM interrupt request.
IUCI	Interrupt clock inverted. Clocks contents of line register into sync register.
IUDX	Interrupt detection. Sets flip-flop IURM.
IUJX	Interrupt jump. Inhibits the PIM after a jump and mark command.
IURM	Interrupt request memory flip-flop. Stores a request for an interrupt from an interrupt line.
IURX-I	Interrupt request. Sent to the processor to request signal IUAX-I.
KPRME	K-input to PRME
LPii	Line priority signals. Indicates the eight PIM priorities.
LRnn	Line register flip-flop outputs. Stores request for an interrupt from a device connected to an interrupt line.
PRME	PIM enabling flip-flop. Stores the activation of the PIM.
PRMX	Priority input. Gives priority to PIM.
PRNX	Priority output. Passes priority to next in line after interrupts are serviced.
SMR1	Clocks mask word into mask register.
SYRT	System reset. Clears flip-flops DTOX and PRME and generates signal CILR when control-panel reset switch is pressed.

S.O.454618 Rev.00
Maintenance Documentation Set
F-3024-01
Priority Interrupt Module

F3024-01

010094-001	Priority Interrupt Module
66P0192	Priority Interrupt Module
66D0192	Priority Interrupt Module
66A0194	Logic Diagram
9809902-428	Manual-Priority Interrupt Module

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PARTS LIST

MFG. CODE	ISSUE DATE	CONTROL	CA	TYPE	COMM. CODE	ST.	DOC NO	SHEET	PL REV.
J W	02/07/80	W77		M		A	PL W 0100094	1	D

TITLE: PRIORITY INTERRUPT OPTION, EXPANSION

CL	U/M	AC	DOC SIZE	RANGE	THRU	ISSUE	PIC. REV
A	EA	9	A				D

FIND NO.	QUANTITY REQUIRED	U/M	SIZE	PART OR IDENT NO. DOCUMENT NO.	DASH	NOMENCLATURE OR DESCRIPTION	SP	CHG
Z04				W-87464	-02	PL REV D, PIC REV D, RANGE 00 - 03 EIR RELEASED 02/07/80		
Z03				W-87474	-22	PL REV C, PIC REV B, RANGE 00 - 03 EIR RELEASED 10/15/79		
**********						********** COMMON DATA **********		
S01		X		SW01163	-00	PART IDENTIFICATION PART IDENTIFICATION	A	
S02		X		SW00114	-00	TEST SPECIFICATION PRIORITY INTERRUPT MODULE	A	
S03		X		SW00191	-00	DESIGN SPECIFICATION PRIORITY INTERRUPT MODULE	A	
**********						620 I EXPANSION * VARIABLE DATA - 00**********		
2	1	FA		6600198	-00	PC ASSEMBLY-PIM. (4400683-000)	A	*
5	1	FA	W	5300019	-00	CABLE ASSY -PRIORITY INTERRUPT INTERNAL	A	
6	1	FA	W	5300020	-00	CABLE - PRIORITY INTERRUPT, EXTERNAL	A	
A	18	FA	W	5800002	-00	CONTACT #22-26 AWG, .036-.103 INS DIA	A	
11	4	FA	W	2104402	-61	SCREW, TRUSS HEAD 4-40 REPLACED BY 2100062	A	
12	4	FA	W	2204400	-01	WASHER-FLAT, NO. 4 .250 OD,.125 ID,.028 THK	A	
13	4	FA	W	2204401	-02	WASHER, LOCK, INT TOOTH	A	
14	4	FA	W	2304400	-01	NUT, HEXAGON, LARGE PATTERN #4-40	A	
**********				F3024-01		********** VARIABLE DATA - 01**********		
2	1	FA		6600198	-00	PC ASSEMBLY-PIM (4400683-000)	A	*
**********						********** VARIABLE DATA - 02**********		
3	1	FA	W	4400022	-00	PC ASSEMBLY PRIORITY INTERRUPT DM124	A	
5	1	FA	W	5300019	-00	CABLE ASSY -PRIORITY INTERRUPT INTERNAL	A	
7	1	FA	W	5300060	-00	CABLE ASSY -PRIORITY INTERRUPT EXTERNAL	A	
A	36	FA	W	5800002	-00	CONTACT #22-26 AWG, .036-.103 INS DIA	A	
11	8	FA	W	2104402	-61	SCREW, TRUSS HEAD 4-40 REPLACED BY 2100062	A	
12	8	FA	W	2204400	-01	WASHER-FLAT, NO. 4 .250 OD,.125 ID,.028 THK	A	
13	8	FA	W	2204401	-02	WASHER, LOCK, INT TOOTH	A	
14	8	FA	W	2304400	-01	NUT, HEXAGON, LARGE PATTERN #4-40	A	

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PARTS LIST

MFG. CODE	ISSUE DATE	CONTROL	CA	TYPE	COMM. CODE	ST	DOC NO	SHEET	REV
J W	02/07/80	W777		M		A	PL W 0100094	2	D

TITLE: PRIORITY INTERRUPT OPTION, EXPANSION

CL	U/M	AC	DOC SIZE	RANGE	THRU	ISSUE	PIC REV
A	EA	9	A				D

FIND NO.	QUANTITY REQUIRED	U/M	SIZE	PART OR IDENT NO. DOCUMENT NO.	DASH	NOMENCLATURE OR DESCRIPTION	SP	CHG
23	1	FA		W 0100019	-00	CONN ASSY, PLUG - 26 CONTACT	1 MALE & 1 FEMALE JACKSCREWS	A
24	26	FA		W 5800004	-02	PIN - CONNECTOR	20 AWG WIRE SIZE MAX	A
**********							VARIABLE DATA - 03**********	
3	1	FA		W 4400022	-00	PC ASSEMBLY	PRIORITY INTERRUPT DM124	A
5	1	FA		W 5300019	-00	CABLE ASSY -PRIORITY INTERRUPT	INTERNAL	A
11	4	FA		W 2104402	-61	SCREW, TRUSS HEAD 4-40	REPLACED BY 2100062	A
12	4	FA		W 2204400	-01	WASHER-FLAT, NO. 4	.250 OD,.125 ID,.028 THK	A
13	4	FA		W 2204401	-02	WASHER, LOCK, INT TOOTH		A
14	4	FA		W 2304400	-01	NUT, HEXAGON, LARGE PATTERN	#4-40	A
23	1	FA		W 0100019	-00	CONN ASSY, PLUG - 26 CONTACT	1 MALE & 1 FEMALE JACKSCREWS	A
24	26	FA		W 5800004	-02	PIN - CONNECTOR	20 AWG WIRE SIZE MAX	A

DWG NO. W0100094

REVISIONS					
REV	EIR	CHG CODE	DESCRIPTIONS	DR	APPD
B	W87474 -22		RELEASE TO API	PB	12-5-79
D	W87464 -02		REVISED PEREIR, UPDATED FORMAT, DOC. NO. WAS 01A0094.		

PART NO. W0100094-00 THRU -03

~~IDENT NO.~~

FOR MATL REQUIREMENTS SEE PL
PL REV LETTER CONTROLS DOCUMENT.

NEXT ASSEMBLY	MODEL NO.	SPERRY UNIVAC

DR	MUMEMTHALER	3/21/68
CHK	JB	3/25/68
DSGN	JB	3/25/68
ENGR	D. MARTIN	4/2/68
APPD	D. MARTIN	4/2/68
APPD	R. PEPPER	4/2/68

CODE IDENT NO. 21101

TITLE

PRIORITY INTERRUPT OPTION
620 I EXPANSION

SIZE	DWG NO.	REV
A	W0100094	D

SHEET 1 OF 9

NOTES:

1 This drawing provides the Priority Interrupt Option for the 6201 Expansion Unit. The assemblies mount in either the central processor (W0100001) or the expansion chassis (W0100074) or both

2. Parts List, W0100094

3 Install parts per W0100074 (Also see sheets 3, 4, 5. & 6 of this drawing).

4 For wiring information see sheet 7.

5 Unterminated wires of cables are trimmed to length at installation and terminal (W5800002-00) are attached.

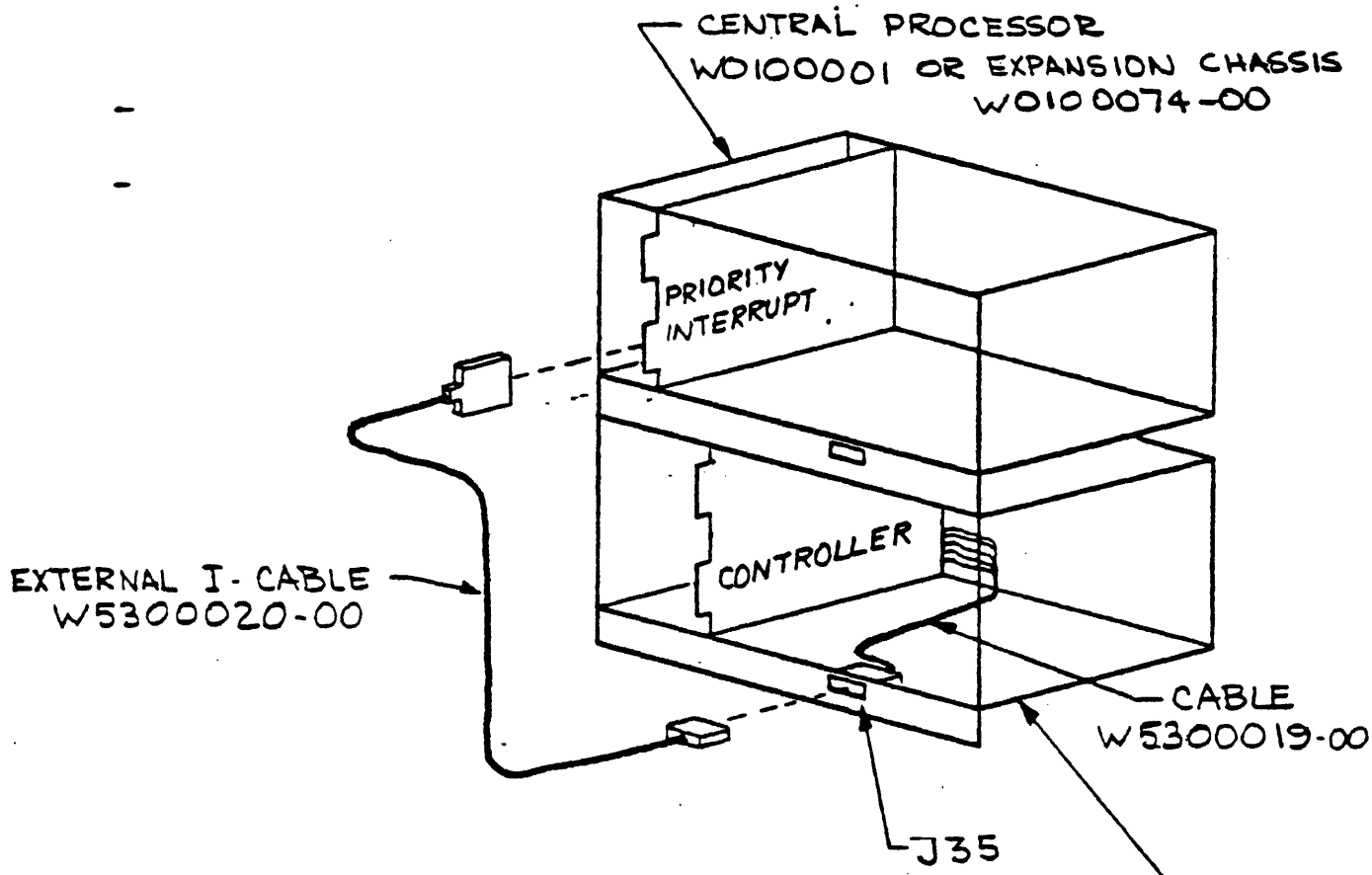
6 If the Priority Interrupt Option is to be shipped for customer installation, package it in a suitable container and identify the container with the following information:

Part No W0100094 - (Applicable Dash No and Rev Ltr)

7 Wiring changes per W9500003 CHG AB must be incorporated to enable this option to function

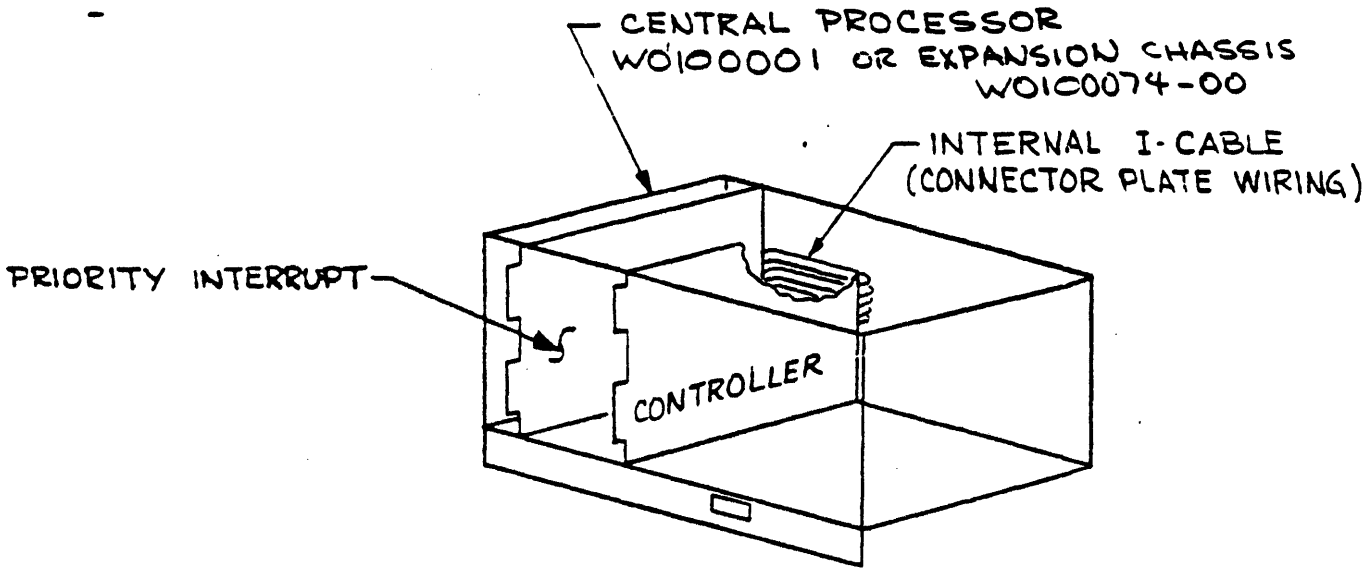
8 Test per W9800114

9 Design Spec W9800191



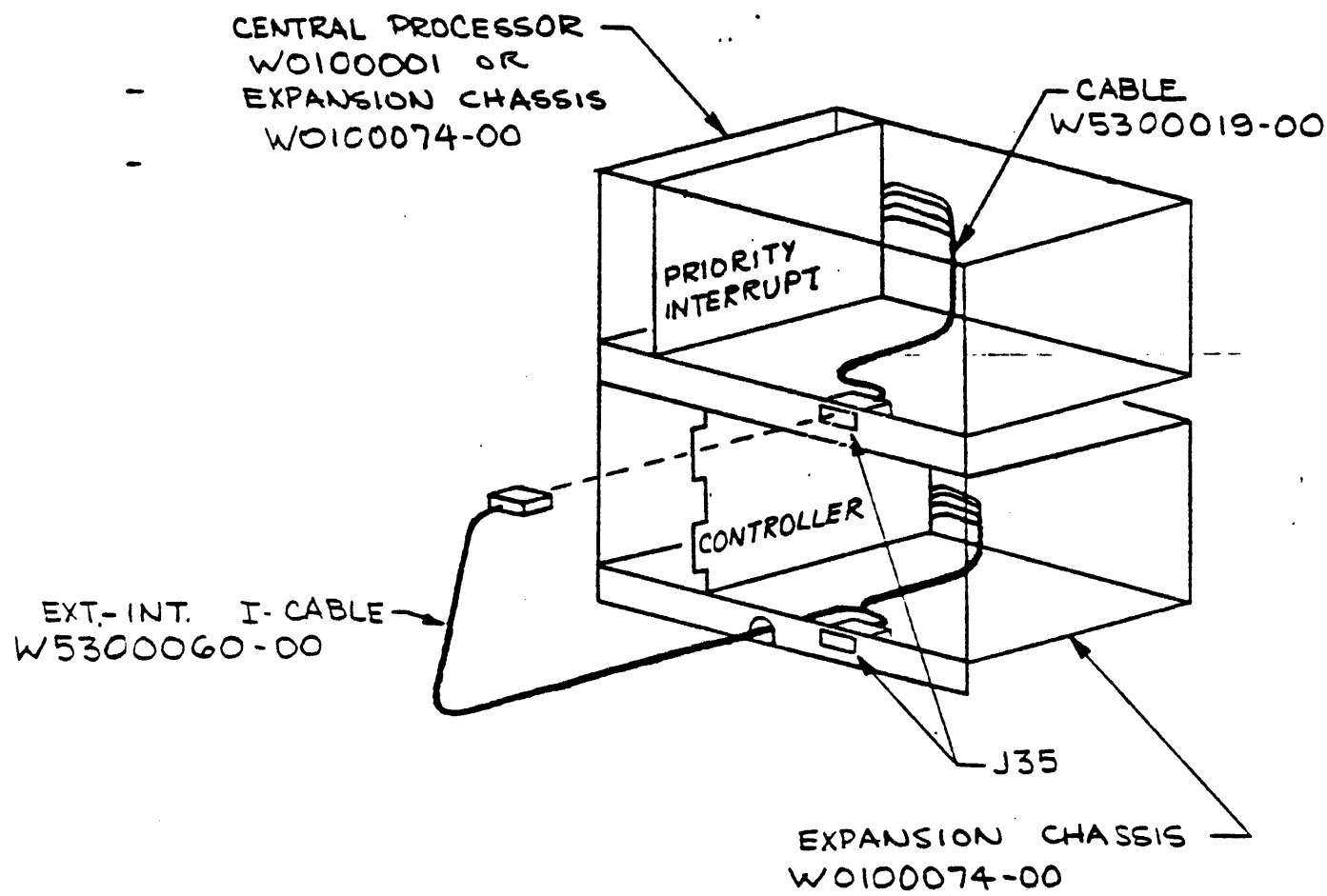
-00

	CODE IDENT NO.	SIZE		REV
	21101	A	W0100094	D
	SCALE NONE			SHEET 3 OF 9



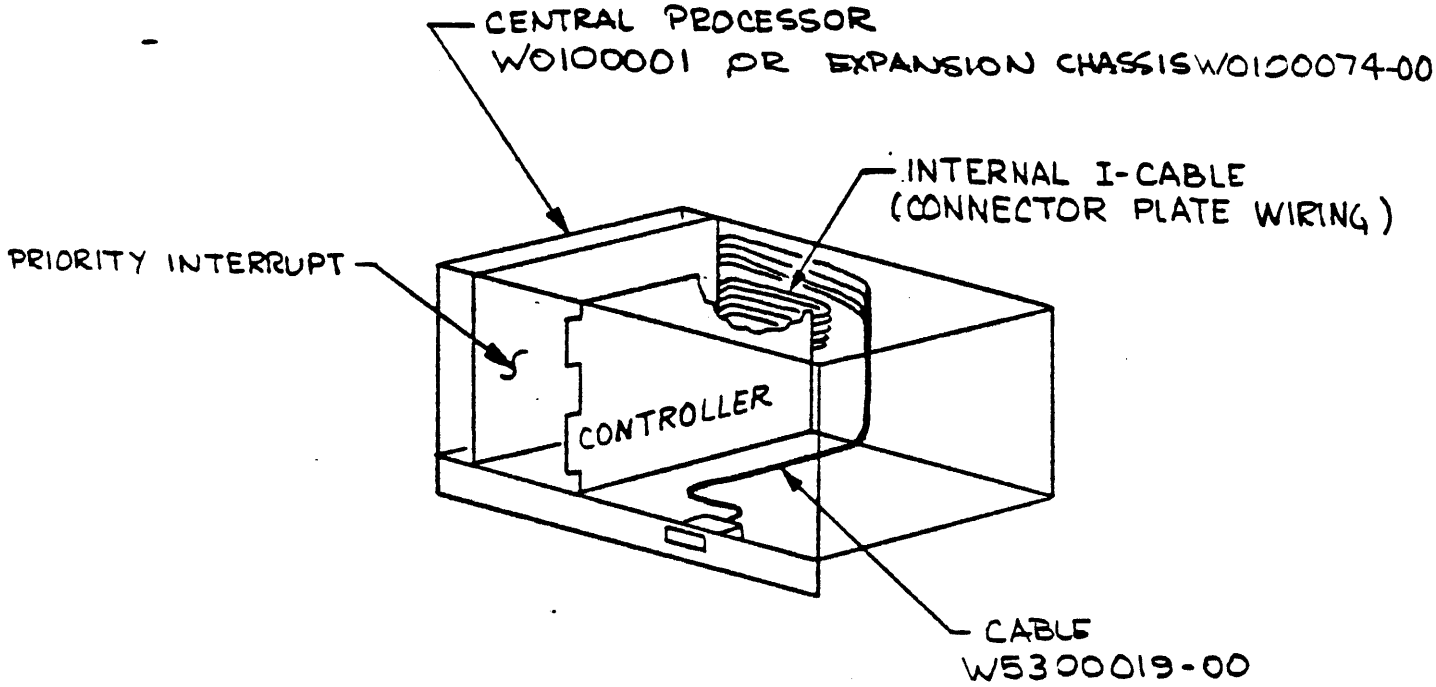
-01

CODE IDENT NO. 21101	SIZE A	W0100094	REV D
SCALE NONE			SHEET 4 OF 9



-02

	CODE IDENT NO.	SIZE		REV
	21101	A	W0100094	D
	SCALE NONE			SHEET 5 OF 9



-03

	CODE IDENT NO.	SIZE		REV
	21101	A	W0100094	D
	SCALE NONE			SHEET 6 OF 9

THE FOLLOWING FUNCTIONS WILL APPEAR AT THE CONNECTORS AS SHOWN:

FUNCTION	CARD EDGE CONNECTOR	26 PIN CONNECTOR
IL00-	3	A
R	4	B
IL01-	13	C
R	14	D
IL02-	9	E
R	10	F
IL03-	15	H
R	16	J
IL04-	11	K
R	12	L
IL05-	5	M
R	6	N
IL06-	1	P
R	2	R
IL07-	7	S
R	8	T
SPARE	17	U
SPARE	18	V

DEVICE ADDRESS TABLE
FOR THE NEW PIM (6600102)

TO SELECT DEVICE ADDRESS	LOCATION CD1		
	S3	S2	S1
40	A	A	A
41	A	A	B
42	A	B	A
43	A	B	B

NOTES:

1. MAKE NO CONNECTION TO PIN 63 FOR DEVICE ADDRESSING.
2. TO INSTALL A NEW PIM W4400683 OR 6600192 IN PLACE OF AN OLD STYLE PIM (W4400172), REMOVE ENTIRE WIRE WRAP STRING (IF ANY) BETWEEN PIN 63 AND ANY OF THE FOLLOWING PINS: 66, 69 AND 72.

DEVICE ADDRESS WIRING TABLE FOR PIM(W4400172) (SHOWN FOR REFERENCE)

TO SELECT DEVICE ADDRESS	ADD W/W JUMPER FROM P1			
	PIN 64 TO PIN	PIN 67 TO PIN	PIN 70 TO PIN	PIN 63 TO PIN'S
40	66	69	72	—
41	65	69	72	66
42	66	68	72	69
43	65	68	72	66, 69
44	66	69	71	72
45	65	69	71	66, 72
46	66	68	71	69, 72
47	65	68	71	66, 69, 72

DEVICE ADDRESS WIRING TABLE FOR PIM(W4400683) SHOWN FOR REFERENCE

TO SELECT DEVICE ADDRESS	ADD W/W JUMPER FROM P1		
	PIN 64 TO PIN	PIN 67 TO PIN	PIN 70 TO PIN
40	66	69	72
41	65	69	72
42	66	68	72
43	65	68	72
44	66	69	71
45	65	69	71
46	66	68	71
47	65	68	71

SPERRY UNIVAC — SPERRY UNIVAC IS A DIVISION OF SPERRY RAND CORP

PARTS LIST

MFG CODE	ISSUE DATE	CONTROL	CA	TYPE	COMM CODE	ST		DOC NO	SHEET	PL REV
W	09/27/79	W777		AP		A	PL	6600192	1	-

TITLE	CL	U/M		AC	DOC SIZE	RANGE THRU	ISSUE	PIC REV
PC ASSEMBLY-PIM (4400683-000)	A	EA		1	D			-

FIND NO	QUANTITY REQUIRED	U/M	SIZE	PART OR IDENT NO DOCUMENT NO	DASH	NOMENCLATURE OR DESCRIPTION	SP	CHG
200				W-87436	-03	PL REV -, PIC REV -, RANGE 00 - 00 EIR RELEASED 09/27/79		
**********	**********	**	**	**********	**********	********** VARIABLE DATA - 00**********	**	**
1	1	EA		6600193	-00	PC BOARD-PIM	A	*
2	4	EA		W 4900002	-00	INTEGRATED CIRCUIT 14 DIL - PLASTIC	A	*
4	4	EA		W 4900012	-00	INTEGRATED CIRCUIT PLASTIC OR CERAMIC	A	*
6	1	EA		W 4900022	-00	INTEGRATED CIRCUIT 14 DIL - PLASTIC	A	*
8	2	EA		W 4900023	-00	INTEGRATED CIRCUIT 14 DIL - PLASTIC OR CERAMIC	A	*
10	1	EA		W 4900036	-00	INTEGRATED CIRCUIT 14 DIL - PLASTIC	A	*
12	4	EA		W 4900039	-00	INTEGRATED CIRCUIT 14 DIL - PLASTIC	A	*
14	4	EA		W 4900040	-00	INTEGRATED CIRCUIT 14 DIL - PLASTIC	A	*
16	6	EA		W 4900056	-00	INTEGRATED CIRCUIT 14 DIL - PLASTIC	A	*
18	5	EA		W 4900082	-01	INTEGRATED CIRCUIT 14 DIL - PLASTIC OR CERAMIC	A	*
20	1	EA		W 4900093	-01	INTEGRATED CIRCUIT 14 DIL - PLASTIC	A	*
22	1	EA		W 4900094	-01	INTEGRATED CIRCUIT 14 DIL - PLASTIC OR CERAMIC	A	*
24	3	EA		W 4900104	-00	INTEGRATED CIRCUIT 14 DIL - PLASTIC OR CERAMIC	A	*
26	2	EA		W 4900128	-01	INTEGRATED CIRCUIT 14 DIL PLASTIC OR CERAMIC SEL	A	*
28	1	EA		W 4900138	-00	INTEGRATED CIRCUIT 14 DIL - PLASTIC OR CERAMIC	A	*
30	1	EA		W 4900554	-01	INTEGRATED CIRCUIT 14 DIL - PLASTIC OR CERAMIC	A	*
32	6	EA		W 6502500	102	RESISTOR, FIXED COMP, 1/4W, 5%1000 OHMS	A	*
				REF DES	1	R1 R10 THRU R14		*
33	8	EA		W 6502500	151	RESISTOR, FIXED COMP, 1/4W, 5%150 OHMS	A	*
				REF DES	1	R2 THRU R9		*
34	1	EA		W 6505000	151	RESISTOR, FIXED, CARBON .5W 5% 150 OHMS	A	*
				REF DES	1	R15		*
35	15	EA		6630012	-11	CAPACITOR, FIXED, CERAMIC .100 MF,50VDC,+80%,-20%	A	*
				REF DES	1	C2 THRU C9 C17 THRU C23		*

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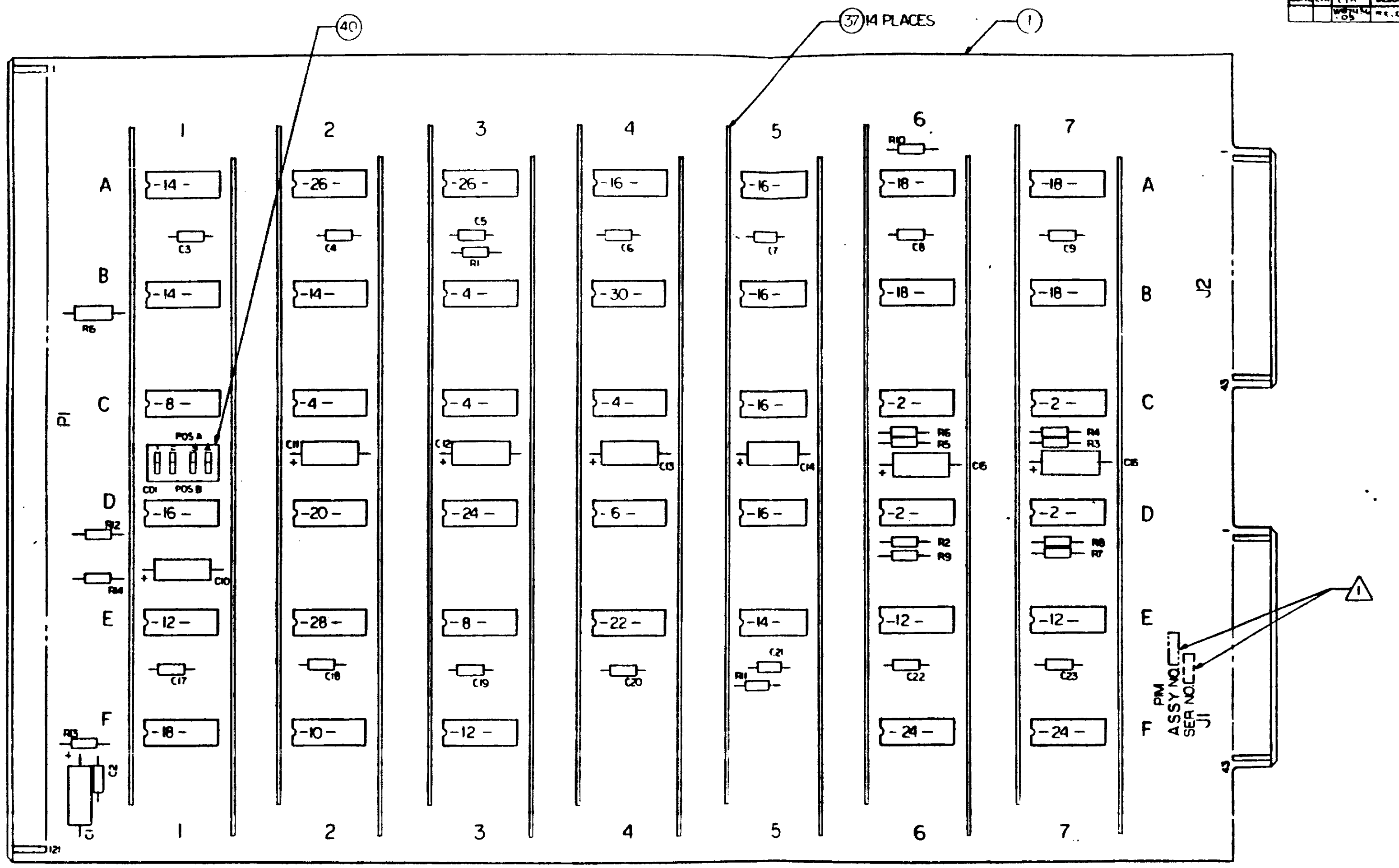
PARTS LIST

MFG CODE	ISSUE DATE	CONTROL	CA	TYPE	COMM CODE	ST		DOC NO	SHEET	PL REV
W	09/27/79	W777		AP		A	PL	6600192	2	-

TITLE	CL	U/M		AC	DOC SIZE	RANGE THRU	ISSUE	PIC REV
PC ASSEMBLY-PIM (4400683-000)	A	EA		1	D			-

FIND NO	QUANTITY REQUIRED	U/M	SIZE	PART OR IDENT NO DOCUMENT NO	DASH	NOMENCLATURE OR DESCRIPTION	SP	CHG
36	8	EA		W 7100200	475	CAPACITOR, TANTALUM 20V 10% 4.7 MF	A	*
				REF DES	1	C1 C10 THRU C16		*
37	14	EA		W 5300194	-00	BUS, POWER DISTRIBUTION 8 SPACE	A	*
40	1	EA		W 7800114	-00	SWITCH,DIP AND SWITCH COVER SWITCH,DIP FOR ROCKER	A	*
F01		X		6600194	-00	LOGIC DIAGRAM-PIM	A	*
S01		X		SW01163	-00	MARKING SPEC PART IDENTIFICATION	A	*



3. "FIND" NUMBERS FOR PARTS IDENTIFIED BY REFERENCE DESIGNATIONS APPEAR IN PARTS LIST.

2. NUMBERS BETWEEN DASHES ARE FIND NUMBERS

1 (in triangle) IDENTIFY PER SPECIFICATION (801)

NOTE: UNLESS OTHERWISE SPECIFIED

REVISIONS						
ZONE	LTR	ETR	DESCRIPTION — FOR DETAILS SEE ETR	CHK	DATE	APPROVED
			RELEASE PART -00			

PART NO. 6600192 - 00

FOR MATL REQUIREMENTS SEE PL. PL REV LETTER CONTROLS DOCUMENT.

UNLESS OTHERWISE SPECIFIED
DIMENSIONS IN INCHES TOL ON
2 PLACE DECIMALS ± .03 | 3 PLACE DECIMALS ± .010 | ANGLES ± 0.5°
HOLE DIA TOL
THREADS EXT CL 2A, INT CL 2B
COMMODITY CODE

LAYOUT	DATE
DRAFTSMAN BERGQUIST	
CHECKER M.C. PHILLIPS	
ENGINEER	
APPROVAL	

CLASS A

SPERRY UNIVAC

TITLE: PC ASSEMBLY - PIM

SIZE D | CODE IDENT NO. 21101 | DWG NO. 6600192

SCALE 2/1 | WEIGHT | SHEET 1 OF 1

DO NOT SCALE THIS PRINT

DWG NO 6600192

REVISIONS						
ZONE	LTR	E.I.R.	DESCRIPTION — FOR DETAILS SEE E.I.R.	CHK	DATE	APPROVED
	-	W87496 1.00	RELEASE PALT-00		6-11-79	

NOTES: (UNLESS OTHERWISE SPECIFIED)

1. ALL RESISTORS ARE 1/4 W, 5%

TABLE OF CONTENTS

C24	
R15	
P1	
J2	
HIGHEST	NOT USED

REFERENCE DESIGNATIONS

ASSEMBLY NO. 6600192-00 IDENT NO. 6600194-00

SHEET / REV	1.0	2.0	3.0	4.0	5.0	6.0	7.0	8.0	9.0	10.0
SHEET										
REV	-	-	-	-	-	-	-	-	-	-

SHEET INDEX

LAYOUT		DATE
DRAFTSMAN E. DYNES ROMERO		5/24/
CHECKER M.C. PHILLIPS		6/11/79
ENGINEER J. BUNNELL		9-7-79
APPROVAL		

CLASS A

SPERRY UNIVAC

TITLE: LOGIC DIAGRAM - PIM

SIZE	CODE IDENT NO.	DWG NO.	REV
C	21101	6600194	-

SHEET 1.0 OF 10.0

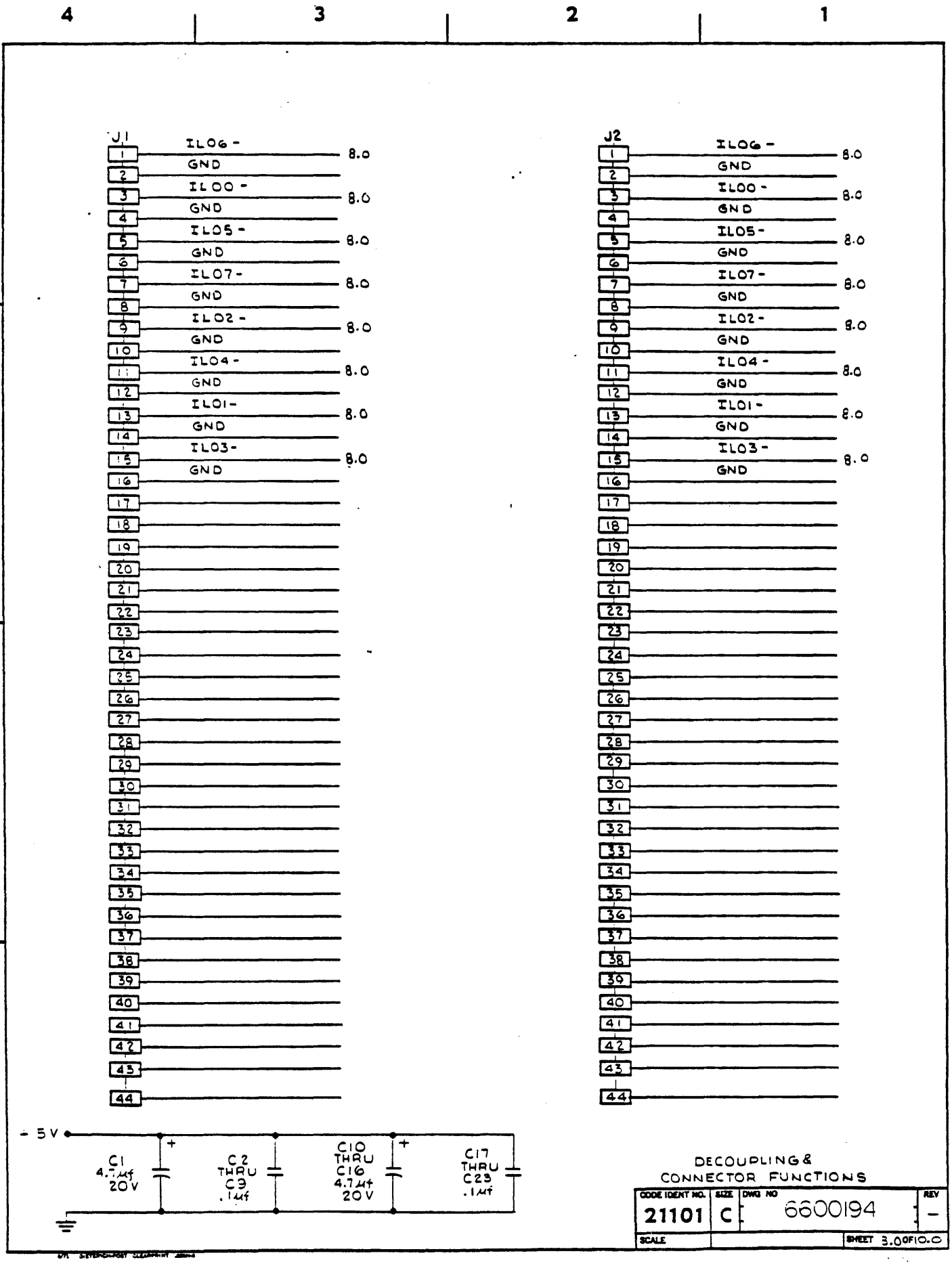
DWG NO. 6600194

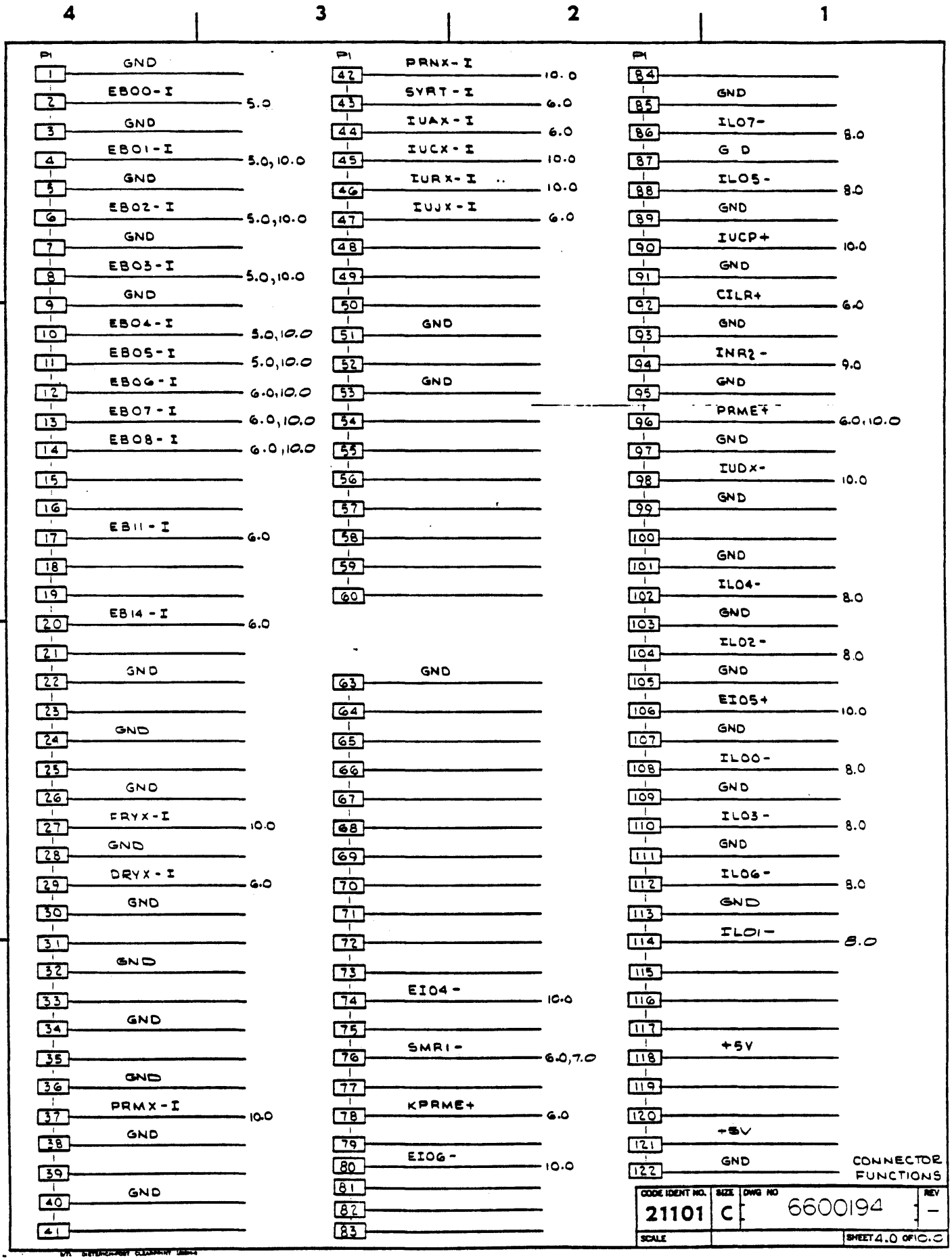
LOC	CHIP TYPE	WHERE USED					
A1	7404	5.0	5.0	5.0	5.0	5.0	5.0
A2	7438 SEL	10.0	10.0	10.0	10.0		
A3	7438 SEL	10.0	10.0	10.0	10.0		
A4	74H20	10.0	10.0				
A5	74H20	8.0	10.0				
A6	74H74	8.0	8.0				
A7	74H74	8.0	8.0				
B1	7404	6.0	6.0	6.0	6.0	6.0	10.0
B2	7404	6.0	6.0	6.0	9.0	10.0	10.0
B3	7474	7.0	7.0				
B4	74H10	9.0	9.0	9.0			
B5	74H20	9.0	9.0				
B6	74H74	8.0	8.0				
B7	74H74	8.0	8.0				
C1	74H04	5.0	5.0	5.0	5.0	5.0	6.0
C2	7474	7.0	7.0				
C3	7474	7.0	7.0				
C4	7474	7.0	7.0				
C5	74H20	9.0	9.0				
C6	7473	8.0	8.0				
C7	7473	8.0	8.0				
D1	74H20	5.0	5.0				
D2	74H50	6.0	6.0				
D3	3001	5.0	6.0	5.0	10.0		
D4	74H11	9.0	9.0	10.0			
D5	74H20	6.0	9.0				
D6	7473	8.0	8.0				
D7	7473	8.0	8.0				
E1	74H00	5.0	6.0	6.0	10.0		
E2	7437	6.0	7.0	10.0	10.0		
E3	74H04	6.0	6.0	9.0	10.0	10.0	10.0
E4	74H21	5.0	9.0				
E5	7404	9.0	9.0	9.0	9.0	9.0	9.0
E6	74H00	8.0	8.0	8.0	8.0		
E7	74H00	8.0	8.0	8.0	8.0		
F1	74H74	6.0	10.0				
F2	74H73	6.0					
F3	74H00	6.0	10.0	10.0	10.0		
F4							
F5							
F6	3001	8.0	8.0	8.0	8.0		
F7	3001	8.0	8.0	8.0	8.0		

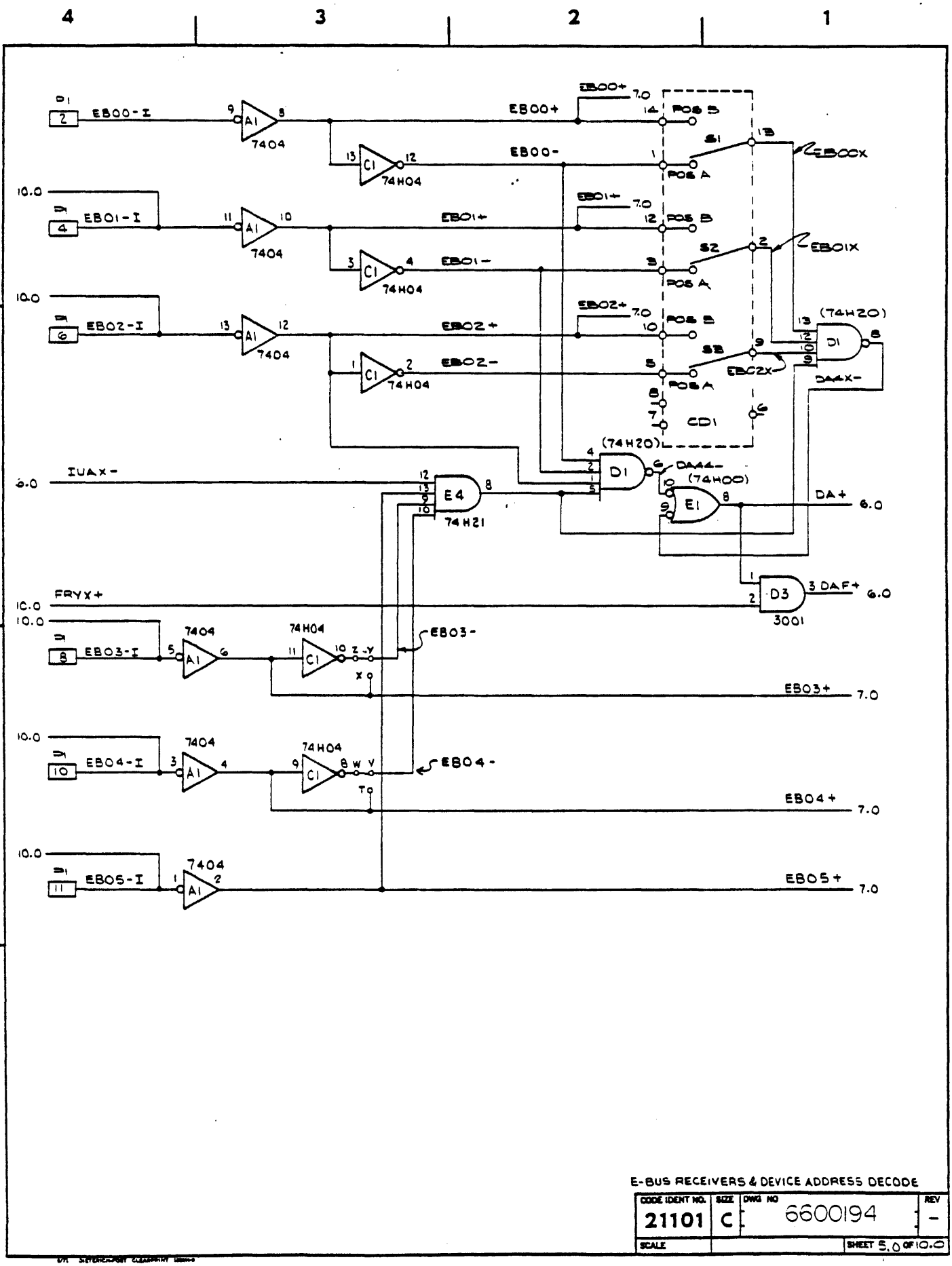
LOC	CHIP TYPE	WHERE USED

LOC	CHIP TYPE	WHERE USED

CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	6600194	-
SCALE		SHEET 2.0 OF 10.0	

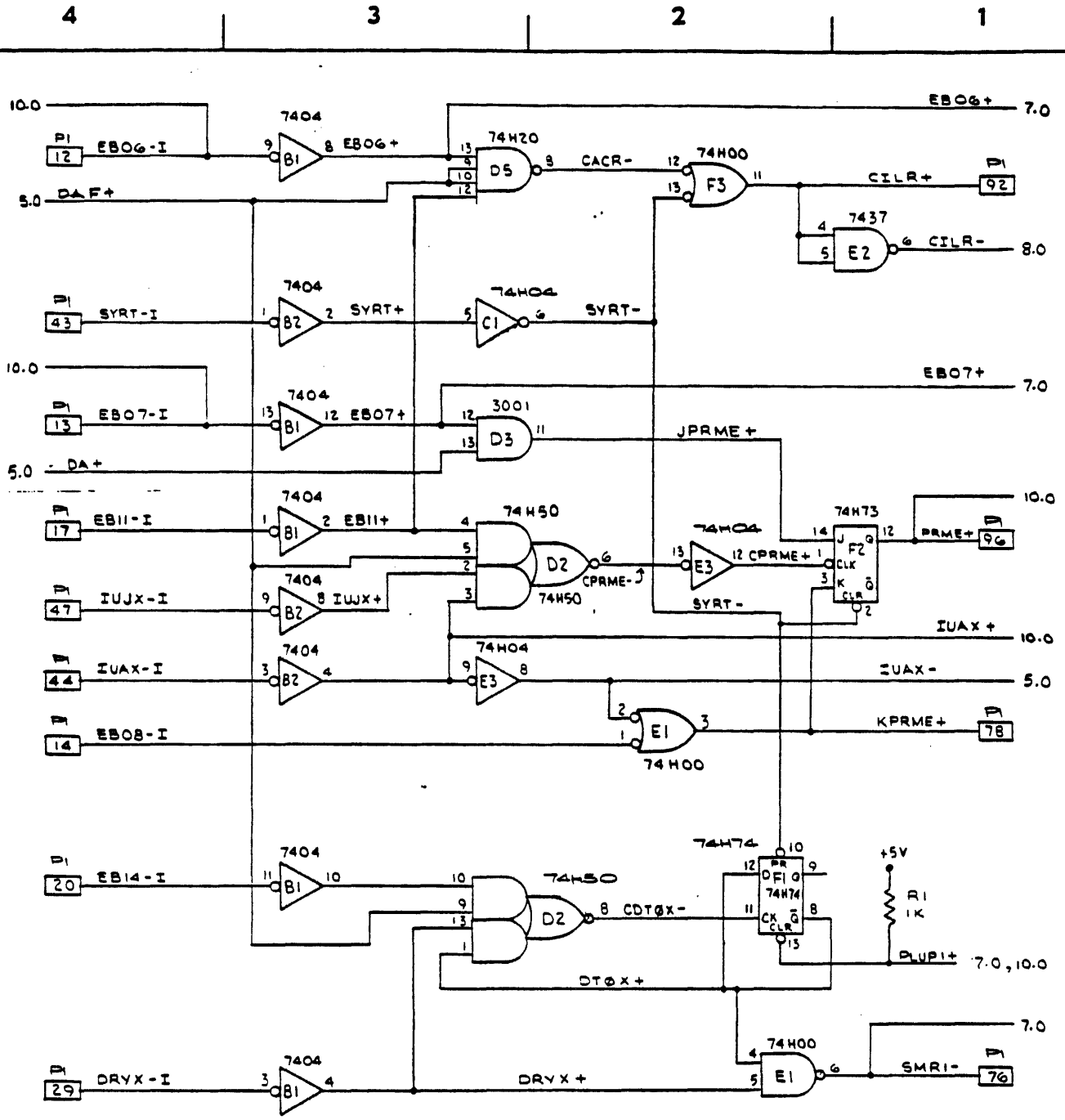

4
3
2
1
D
C
B
A
J1
1 ILO6 - 8.0
2 GND
3 ILO0 - 8.0
4 GND
5 ILO5 - 8.0
6 GND
7 ILO7 - 8.0
8 GND
9 ILO2 - 8.0
10 GND
11 ILO4 - 8.0
12 GND
13 ILO1 - 8.0
14 GND
15 ILO3 - 8.0
16 GND
17
18
19
20
21
22
23
24
25
26
27
28
29
30
31
32
33
34
35
36
37
38
39
40
41
42
43
44
J2
1 ILO6 - 8.0
2 GND
3 ILO0 - 8.0
4 GND
5 ILO5 - 8.0
6 GND
7 ILO7 - 8.0
8 GND
9 ILO2 - 8.0
10 GND
11 ILO4 - 8.0
12 GND
13 ILO1 - 8.0
14 GND
15 ILO3 - 8.0
16 GND
17
18
19
20
21
22
23
24
25
26
27
28
29
30
31
32
33
34
35
36
37
38
39
40
41
42
43
44
- 5V
C1 4.7µf 20V
C2 THRU C9 .1µf
C10 THRU C16 4.7µf 20V
C17 THRU C23 .1µf
DECOUPLING & CONNECTOR FUNCTIONS
CODE IDENT NO. 21101
SIZE C
DWG NO 6600194
REV -
SCALE
SHEET 3.00F10.0


4
3
2
1
D
C
B
A
P1
1 GND
2 EB00-I 5.0
3 GND
4 EB01-I 5.0,10.0
5 GND
6 EB02-I 5.0,10.0
7 GND
8 EB03-I 5.0,10.0
9 GND
10 EB04-I 5.0,10.0
11 EB05-I 5.0,10.0
12 EB06-I 6.0,10.0
13 EB07-I 6.0,10.0
14 EB08-I 6.0,10.0
15
16
17 EB11-I 6.0
18
19
20 EB14-I 6.0
21
22 GND
23
24 GND
25
26 GND
27 FRYX-I 10.0
28 GND
29 DRYX-I 6.0
30 GND
31
32 GND
33
34 GND
35
36 GND
37 PRMX-I 10.0
38 GND
39
40 GND
41
P1
42 PRNX-I 10.0
43 SYRT-I 6.0
44 IUAX-I 6.0
45 IUCX-I 10.0
46 IURX-I 10.0
47 IUJX-I 6.0
48
49
50
51 GND
52
53 GND
54
55
56
57
58
59
60
63 GND
64
65
66
67
68
69
70
71
72
73
74 EI04- 10.0
75
76 SMR1- 6.0,7.0
77
78 KPRME+ 6.0
79
80 EI06- 10.0
81
82
83
P1
84
85 GND
86 IL07- 8.0
87 G D
88 IL05- 8.0
89 GND
90 IUCP+ 10.0
91 GND
92 CILR+ 6.0
93 GND
94 INR2- 9.0
95 GND
96 PRME+ 6.0,10.0
97 GND
98 IUDX- 10.0
99 GND
100
101 GND
102 IL04- 8.0
103 GND
104 IL02- 8.0
105 GND
106 EI05+ 10.0
107 GND
108 IL00- 8.0
109 GND
110 IL03- 8.0
111 GND
112 IL06- 8.0
113 GND
114 IL01- 8.0
115
116
117
118 +5V
119
120
121 +5V
122 GND
CONNECTOR FUNCTIONS
CODE IDENT NO. 21101
SIZE C
DWG NO 6600194
REV -
SCALE
SHEET 4.0 OF 10.0



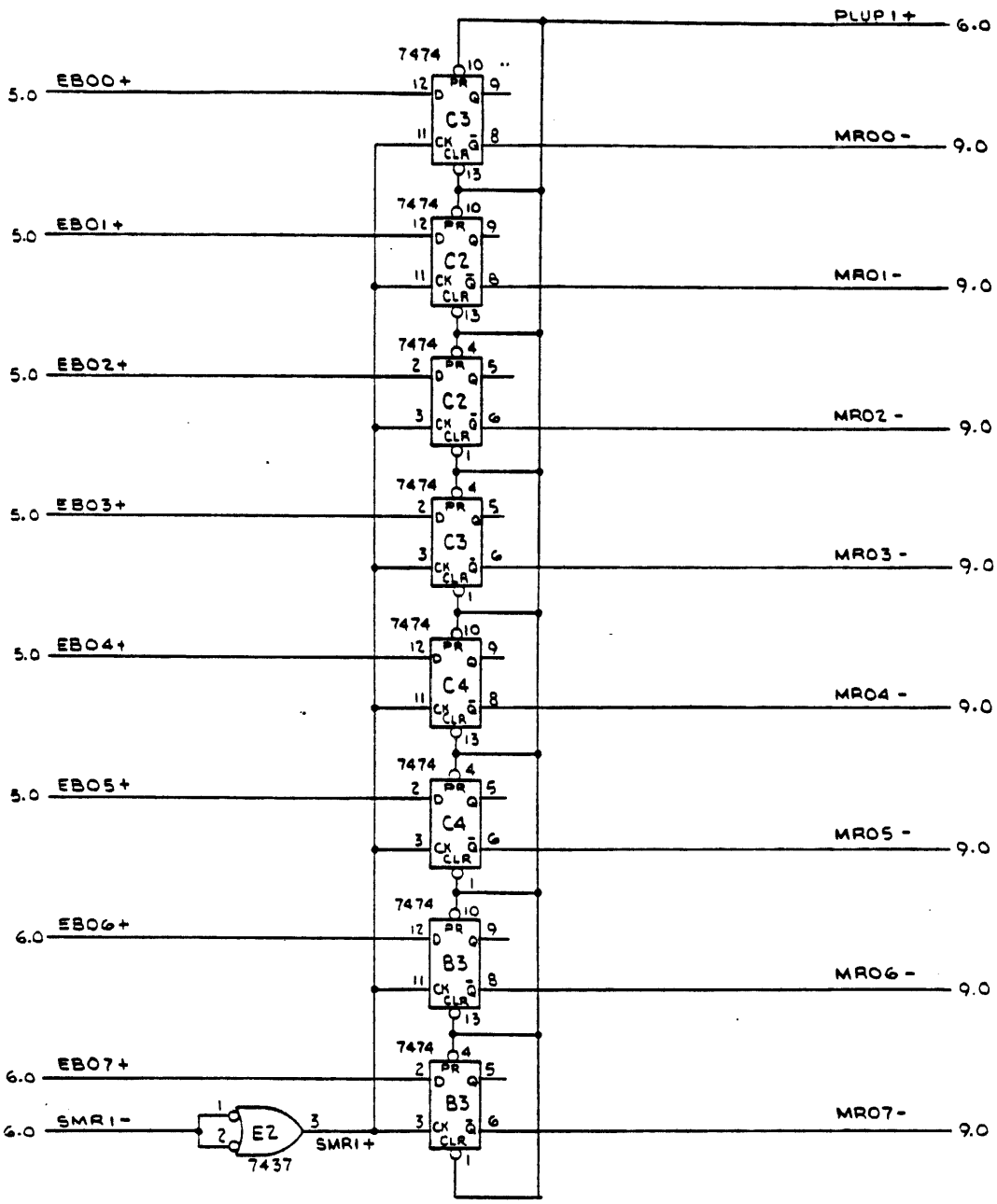
E-BUS RECEIVERS & DEVICE ADDRESS DECODE

CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	6600194	-
SCALE		SHEET 5.0 OF 10.0	



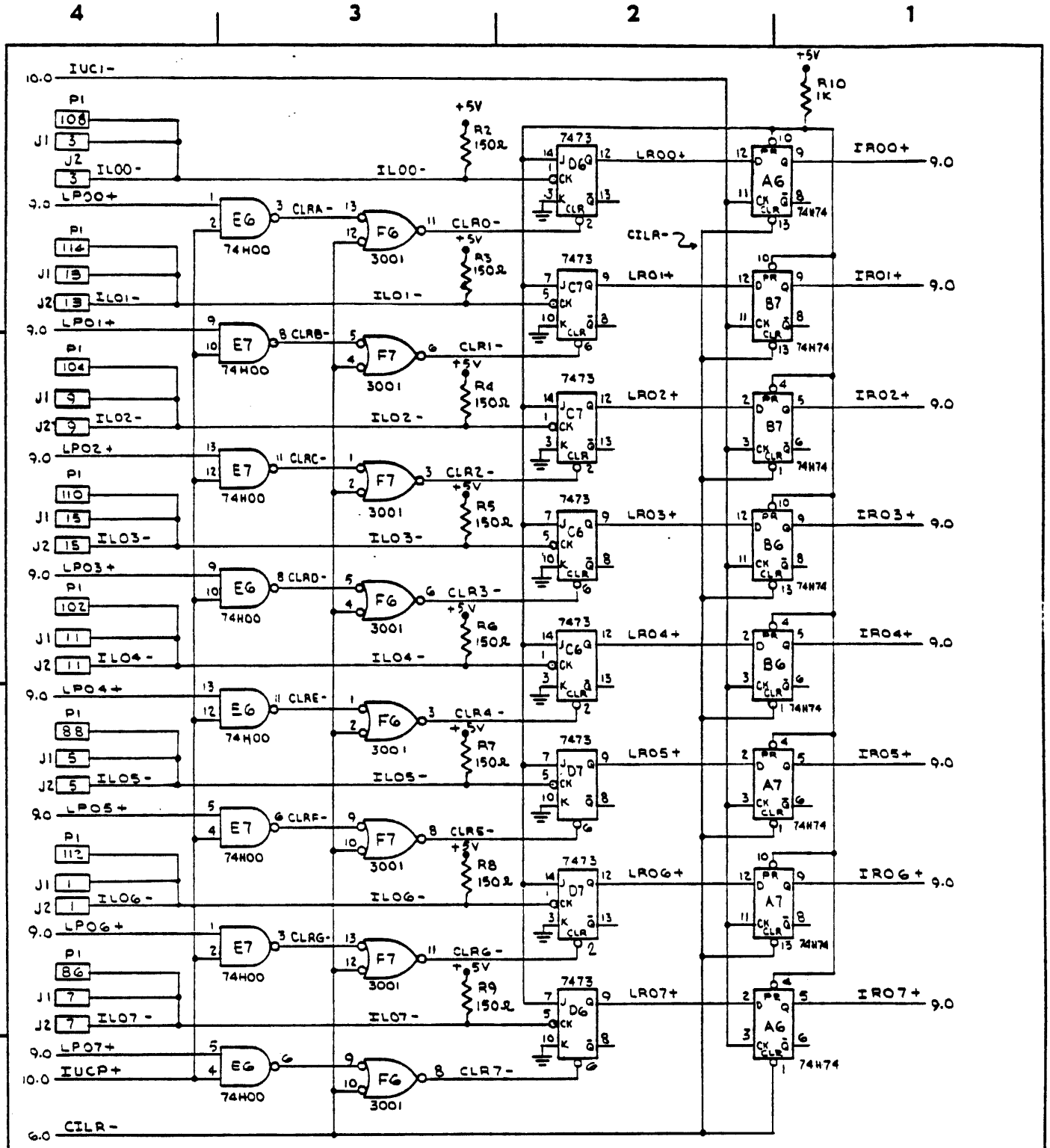
E-BUS RECEIVERS & CONTROL LOGIC

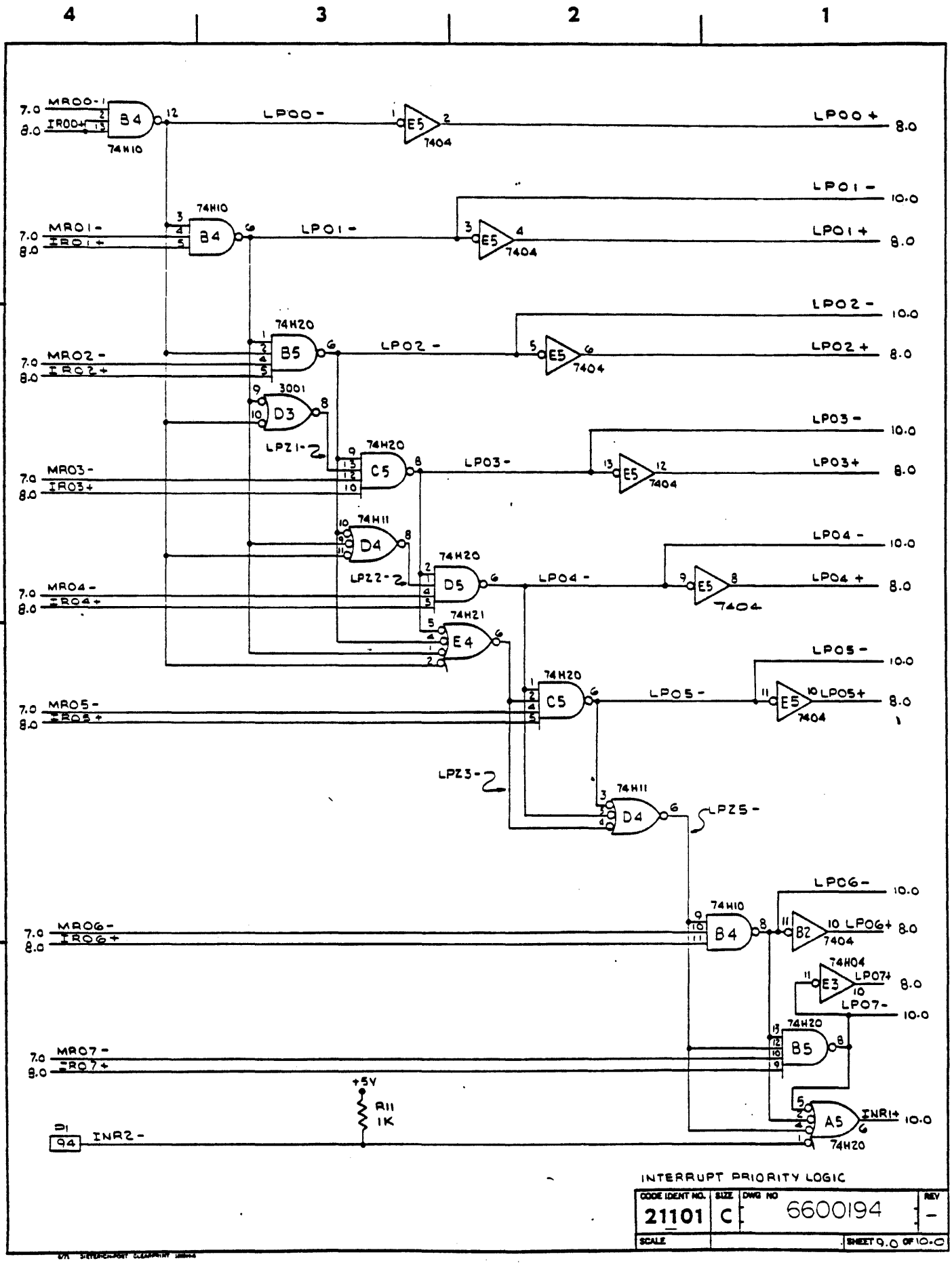
CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	6600194	—
SCALE		SHEET 6.0 OF 10.0	

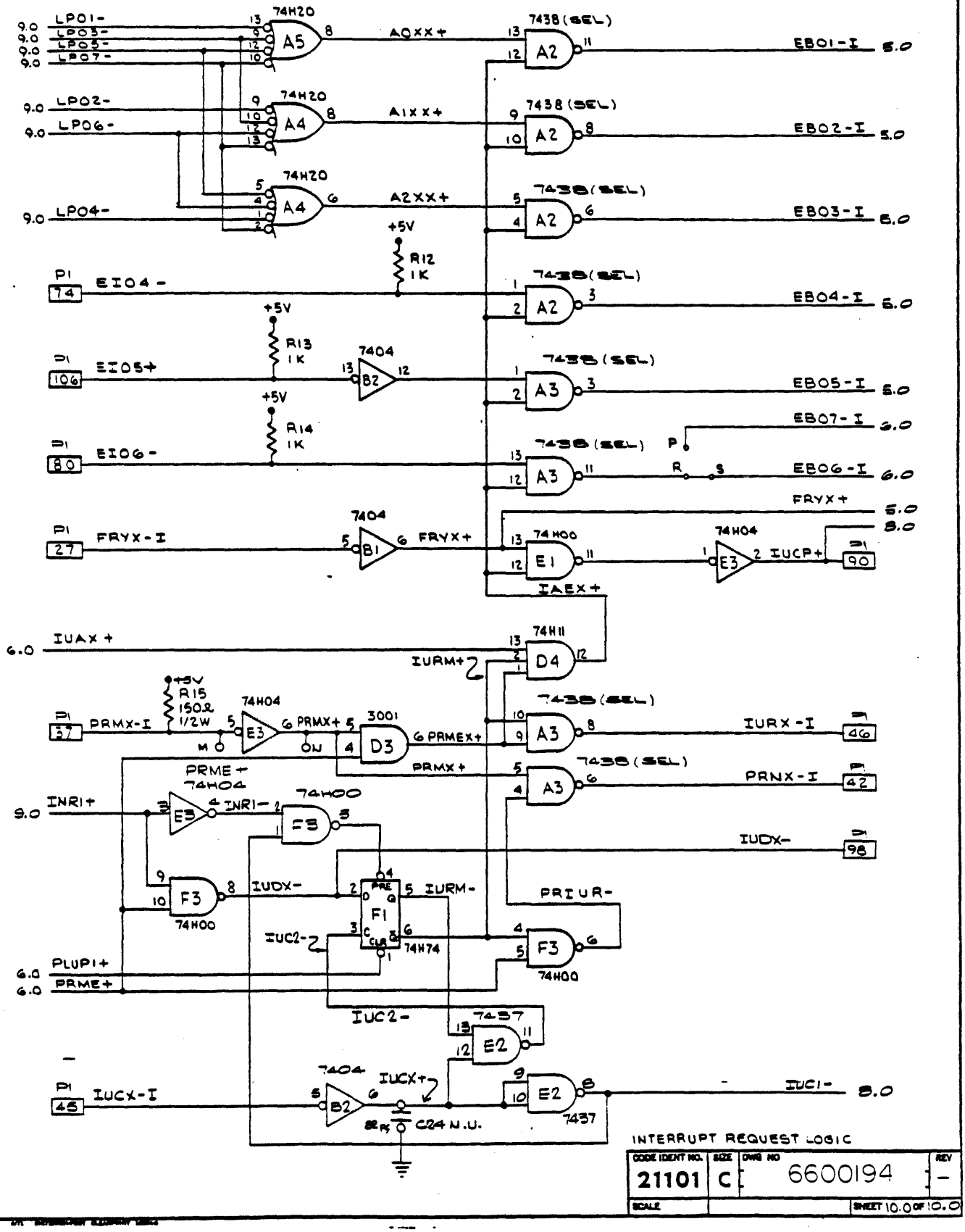


INTERRUPT MASK REGISTER

CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	6600194	—
SCALE		SHEET 7.0 OF 10.0	


4
3
2
1
D
C
B
A
IUC1-
10.0
+5V
R10
1K
P1
108
J1
3
J2
3
IL00-
LP00+
9.0
E6
74H00
CLRA-
F6
3001
CLR0-
R2
150Ω
7473
LR00+
A6
74H74
IR00+
9.0
P1
114
J1
13
J2
13
IL01-
LP01+
E7
CLRB-
F7
CLR1-
R3
150Ω
LR01+
B7
IR01+
P1
104
J1
9
J2
9
IL02-
LP02+
CLRC-
CLR2-
R4
150Ω
LR02+
IR02+
P1
110
J1
15
J2
15
IL03-
LP03+
CLRD-
CLR3-
R5
150Ω
LR03+
B6
IR03+
P1
102
J1
11
J2
11
IL04-
LP04+
CLRE-
CLR4-
R6
150Ω
LR04+
IR04+
P1
88
J1
5
J2
5
IL05-
LP05+
CLRF-
CLR5-
R7
150Ω
LR05+
A7
IR05+
P1
112
J1
1
J2
1
IL06-
LP06+
CLRG-
CLR6-
R8
150Ω
LR06+
IR06+
P1
86
J1
7
J2
7
IL07-
LP07+
IUCP+
CLR7-
R9
150Ω
LR07+
IR07+
CILR-
6.0
INTERRUPT LINE REGISTER &
INTERRUPT REGISTER
CODE IDENT NO. 21101
SIZE C
DWG NO 6600194
REV -
SCALE
SHEET 8.0 OF 10.0


4
3
2
1
D
C
B
A
MR00-1
IR00+
B4
74H10
LP00-
E5
7404
LP00+
8.0
LP01-
10.0
MR01-
IR01+
LP01+
MR02-
IR02+
LP02-
LP02+
3001
D3
LPZ1-2
MR03-
IR03+
LP03-
LP03+
74H11
D4
LPZ2-2
MR04-
IR04+
LP04-
LP04+
74H21
E4
MR05-
IR05+
LP05-
LP05+
LPZ3-2
LPZ5-
MR06-
IR06+
LP06-
LP06+
74H04
E3
LP07+
LP07-
MR07-
IR07+
+5V
R11
1K
P1
94
INR2-
INR1+
A5
INTERRUPT PRIORITY LOGIC
CODE IDENT NO.
21101
SIZE
C
DWG NO
6600194
REV
SCALE
SHEET 9.0 OF 10.0


4
3
2
1
D
C
B
A
LP01-
LP03-
LP05-
LP07-
LP02-
LP06-
LP04-
74H20
A5
A4
A4
AOXX+
A1XX+
A2XX+
7438(SEL)
A2
A2
A2
A2
EB01-I
EB02-I
EB03-I
EB04-I
+5V
R12
1K
R13
1K
R14
1K
P1
74
EI04-
106
EI05+
80
EI06-
7404
B2
A3
A3
EB05-I
EB07-I
EB06-I
FRYX+
P1
27
FRYX-I
B1
74H00
E1
74H04
E3
IUCP+
90
IAEX+
IUAX+
6.0
74H11
D4
IURM+2
R15
150Ω
1/2W
P1
57
PRMX-I
E3
PRMX+
3001
D3
PRMEX+
IURX-I
46
PRME+
74H04
PRMX+
PRNX-I
42
INRI+
9.0
E3
INRI-
74H00
F3
IUDX-
98
F3
IUDX-
F1
74H74
IURM-
PRIUR-
IUC2-2
F3
74H00
PLUP1+
6.0
PRME+
6.0
IUC2-
7457
E2
7404
B2
IUCX-I
45
IUCX+
82pf
C24 N.U.
E2
7437
IUC1-
8.0
INTERRUPT REQUEST LOGIC
CODE IDENT NO.
21101
SIZE
C
DWG NO
6600194
REV
-
SCALE
SHEET 10.0 OF 10.0