

More comments from Jens, owner of a sheet-fed A3-size scanner as of March 2nd, 2022.

Following FozzTexx's thoughts on Twitter, I have scanned these Tabloid-sized pages with 300DPI and chose a lossless format: The scanner software spits out PNG either in colour, or 8-bit grey scale. I have only done a palette reduction to 16 colours and 4 bit depth using Imagemagick, resulting in about 80% data reduction. Rest assured that no information was lost, as the original prints are purely black&white. Some parts are unreadable, but they are also unreadable in the original.

Like I wrote a few times on Twitter, I find it interesting that there are a few hand-written notes in these schematics. I still could not find out who's hand writing it is - if you happen to know a German technician who has worked for the „GEI“ near Aachen, Germany in the 1980s, let me know.

Contact me:

eMail: jens@icomp.de
twitter: @schoenfeld_jens

Please upload this file to other freely accessible archives.

As promised, here's some translation help for the comments:

Power supply page 1/1:

„Primärspule“ means „primary winding“
„Rückkopplungsspule“ means „feedback winding“

Disk drive schematic

page 2/9:

„Brücke für single/double-sided“ means „bridge for...“

page 5/9:

location D8 „Schreiben“ means „write“, „löschen“ means „erase“
location B3 „geändert auf“ means „changed to 750 Ohms“
location A3 „Schreibstrom“ means „write current“
location A7 „Löschstrom“ means „erase current“
location A6 „Stromrichtung beim Schreiben“ means „current direction when writing“

page 7/9: Self-explanatory

page 9/9: „Darlington-Ersatz“ means „Darlington-replacement“

(next page..)

Audio interface 14/14:

„Spannungs-Stabilisator“ means „voltage stabilizer“

128k memory schematic, page 3/4:

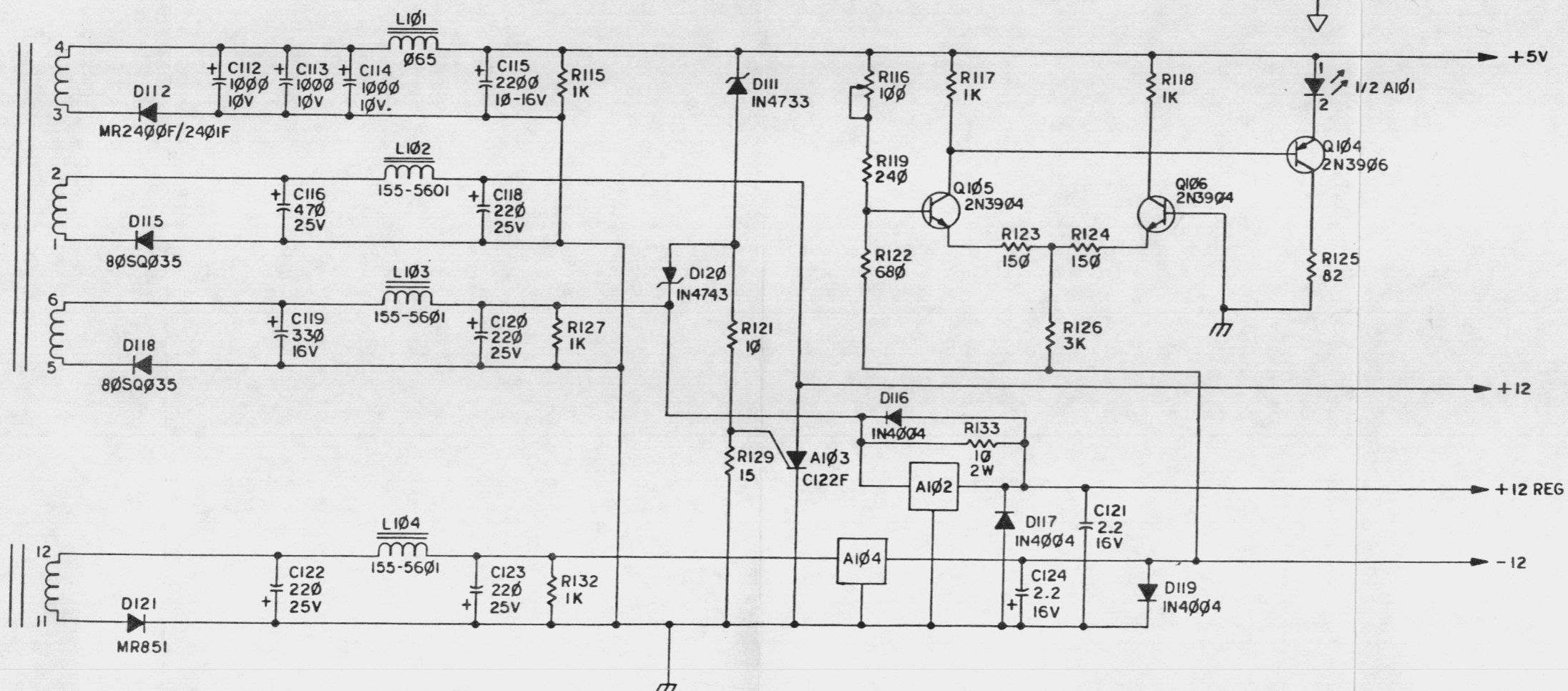
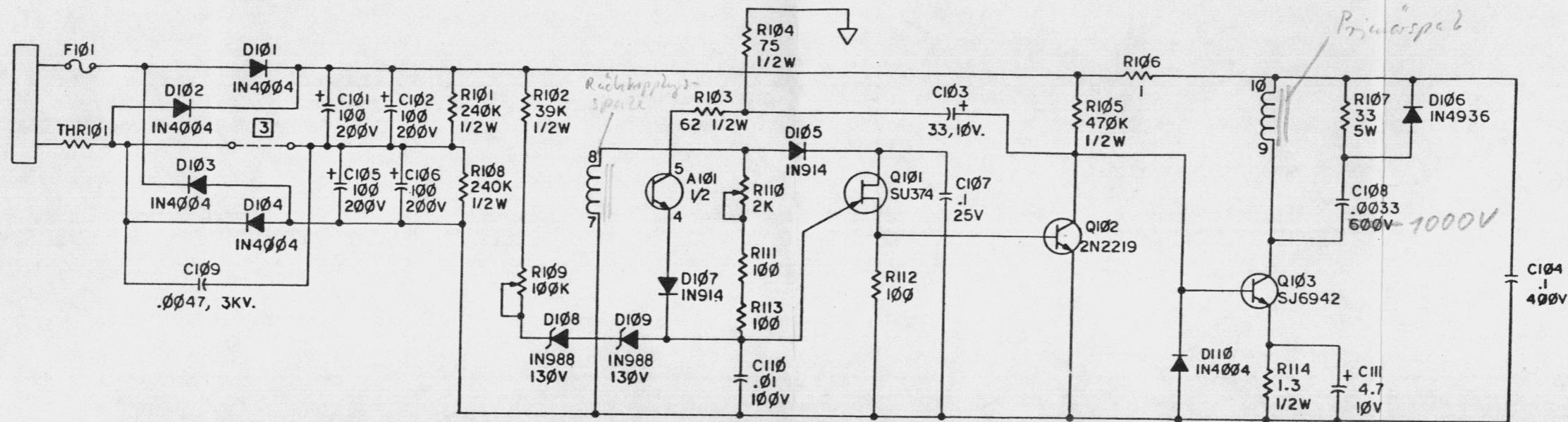
location C4: „Verändern“ means „change“ [refresh timing]

location C3: „Timing-anpassung bei Verwendung anderer RAMs“ means „timing adjustment if other RAMs are used“. Yep - scary RC combo for Mux timing...

Note that this „timing option“ is not there on the 384k expansion schematic. They probably found out that „fully sync“ is the way to go. The only way. Also, the 384k expansion schematic shows that it's not prepared for 256k machines, as mapping to start address \$4.0000 is not possible for this version (only \$2.0000 and \$8.0000). This indicates that this schematic is quite early.

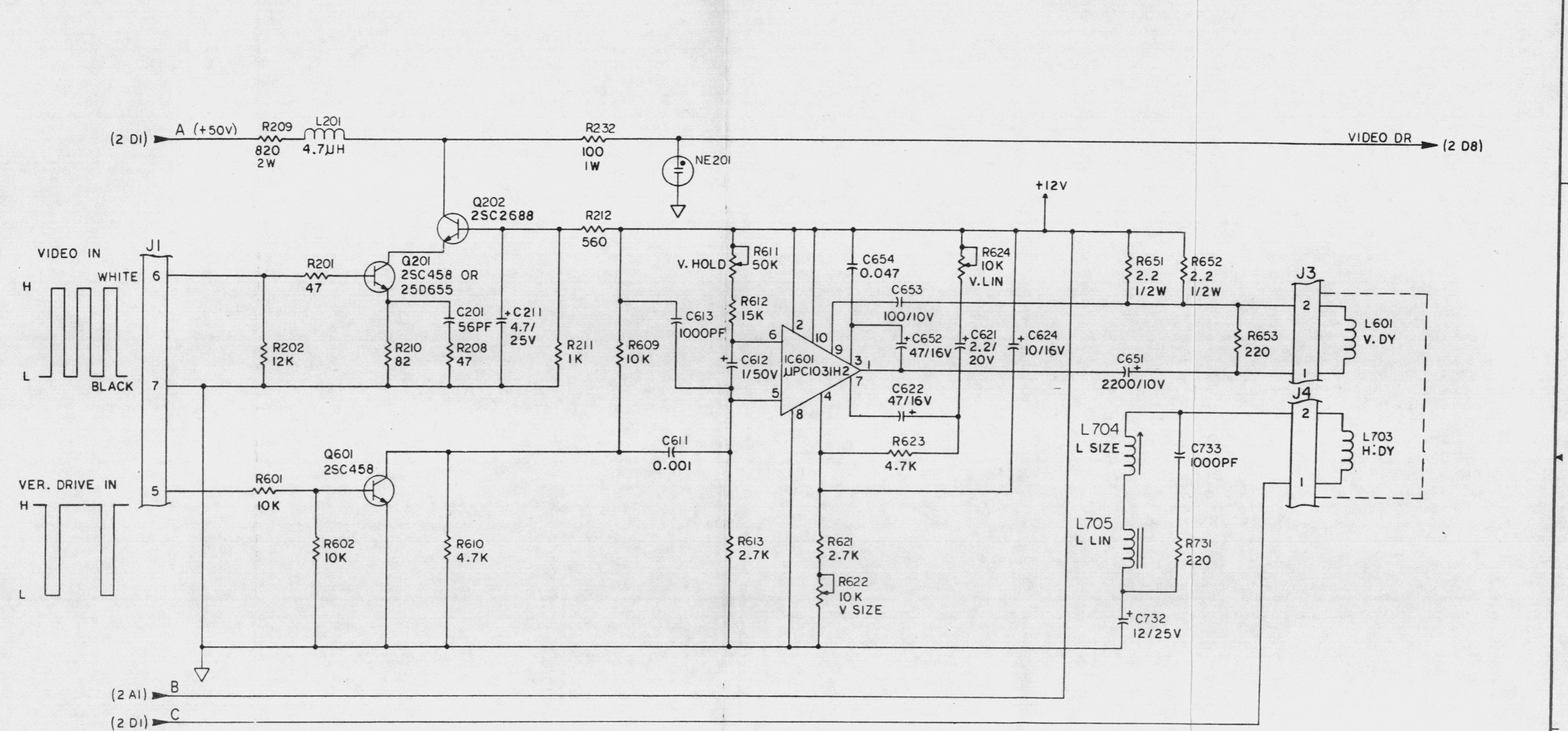
The CPU schematic shows that the RS232 drivers are properly connected to 12V/-12V, so the bulletin that Paul Devine has scanned (thanks for that!) is either a mishap upon transferring schematics to board design, or it refers to an even earlier design revision.

Now I have this itch to take up that work that the guys from French „jurassic computer club“ have started: Reverse-engineering that DMA-SASI-card for a harddisk. If I only had more time...



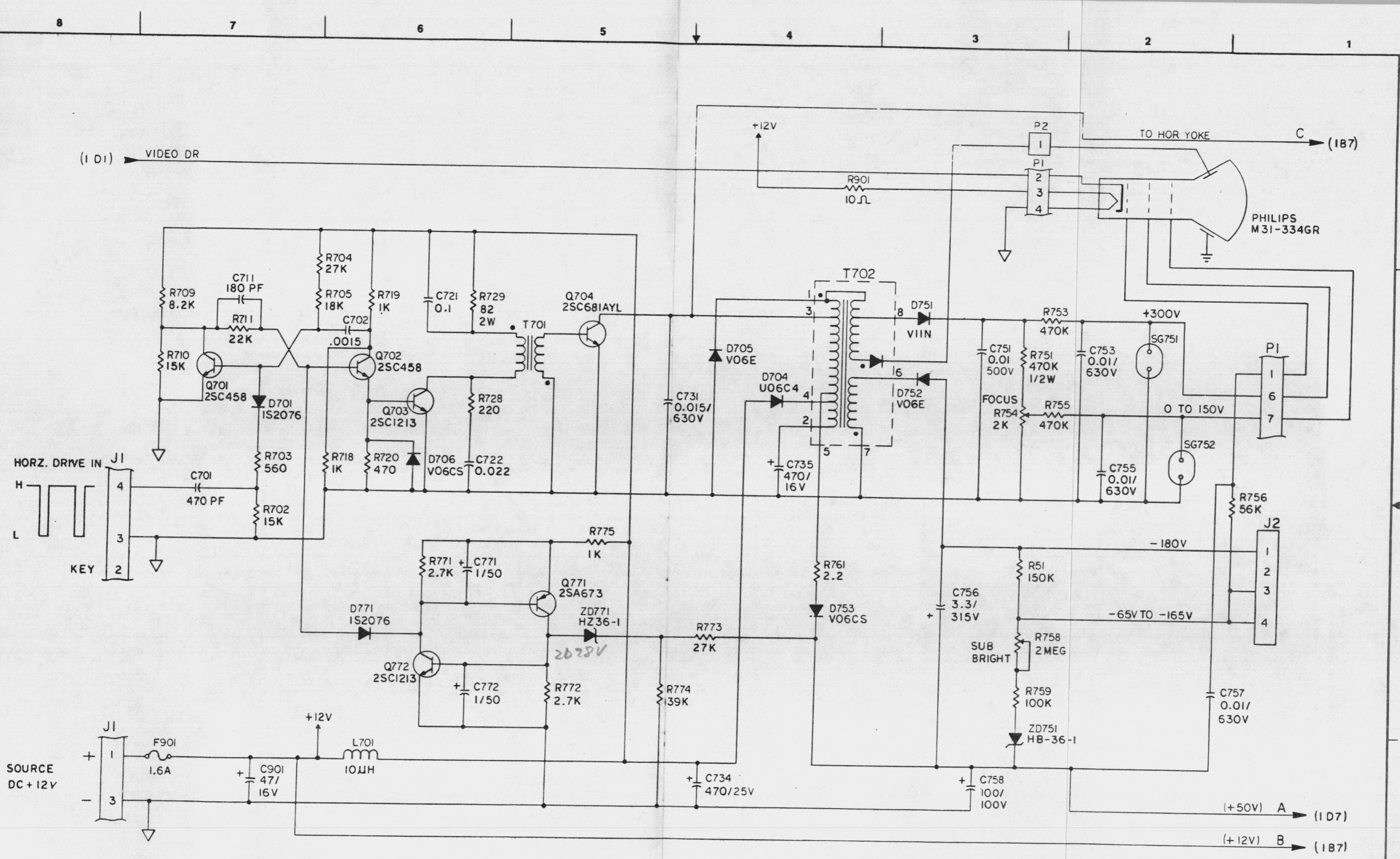
- 4 REF COMPOWER CORP., CP-5102 SCHEMATIC, DWG NO 90017.
- 3 CUT FOR 220V OPERATION
- 2. ALL RESISTORS ARE $\pm 5\%$, 1/4W.
- 1. ELECTRICAL VALUES ARE IN OHMS, MICROFARADS AND MICROHENRIES.

8 7 6 5 4 3 2 1

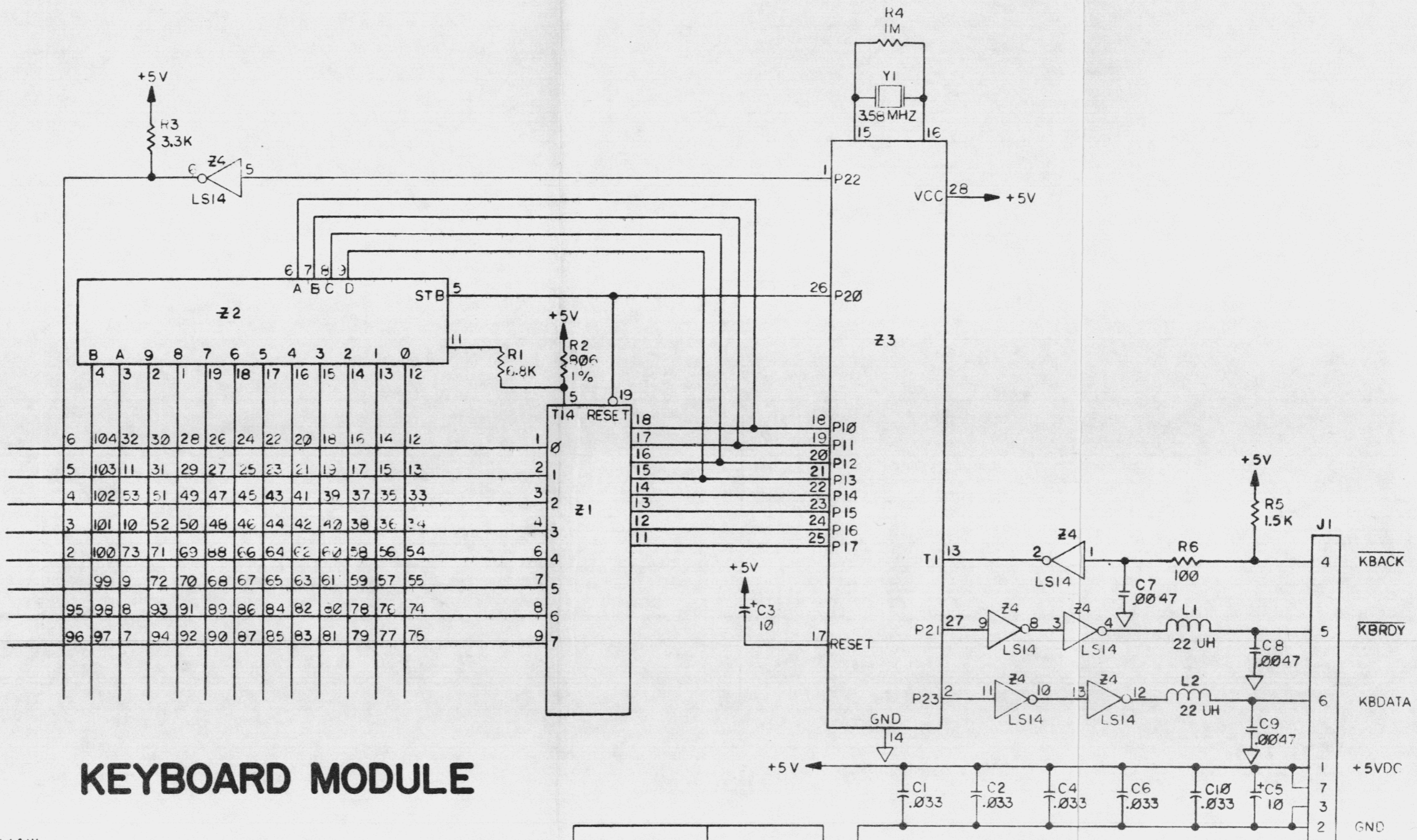


SHT. 1 OF 2 REV. DWG. NO. 100691 VICTOR VID. C'NTR'L BD. SCHEMATIC

8 7 6 5 4 3 2 1



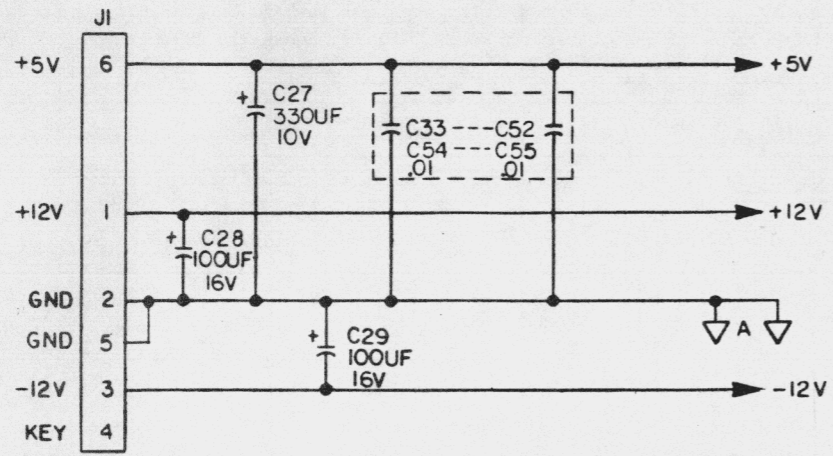
SHT. 2 OF 2 REV. VICTOR
 DWG. NO. 100691 VID. C'NTR'L BD. SCHEMATIC



KEYBOARD MODULE

- 3. ALL RESISTORS ARE $\pm 5\%$, 1/4 W
 - 2. ELECTRICAL VALES ARE IN OHMS, MICROFARADS & MICROHENRIES
 - 1. MADE SCHEMATIC FROM KEY TRONIC CORPORATION, SPOKANE, WASH. PART NUMBER 35-02307-XXX
- NOTE: UNLESS OTHERWISE SPECIFIED

Z4 - Y1 - J1	
R6 - C10 - L2	
LAST USED	NOT USED
REF. DES.	



NOTES: UNLESS OTHERWISE SPECIFIED.

1. ELECTRICAL VALUES ARE IN OHMS, MICROFARADS AND MICROHENRIES.

2. ALL RESISTERS ARE $\pm 5\%$, 1/4 W.

3. F.S. IS FACTORY SELECT COMPONENTS.

4. Q1, Q2 ARE MOUNTED ON HEATSINK.

5. ALL INTEGRATED CIRCUITS ARE SN74 SERIES.

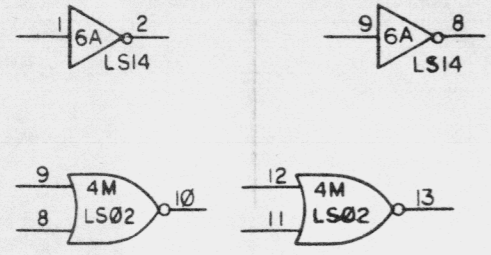
6. I.C. PINS ARE GND=7, +5V=14 EXCEPT FOR:

TYPE	GND	+5V
74LS123	8	16
74LS133	8	16
74LS139	8	16
74LS157	8	16
74LS165	8	16
74LS190	8	16
74LS191	8	16
74LS373	10	20
2316	12	24
75462	4	8

7. ALL DIODE ARE 1N4148.

8. SEE TABULATION TABLE THIS PAGE.

POWER & SPARES

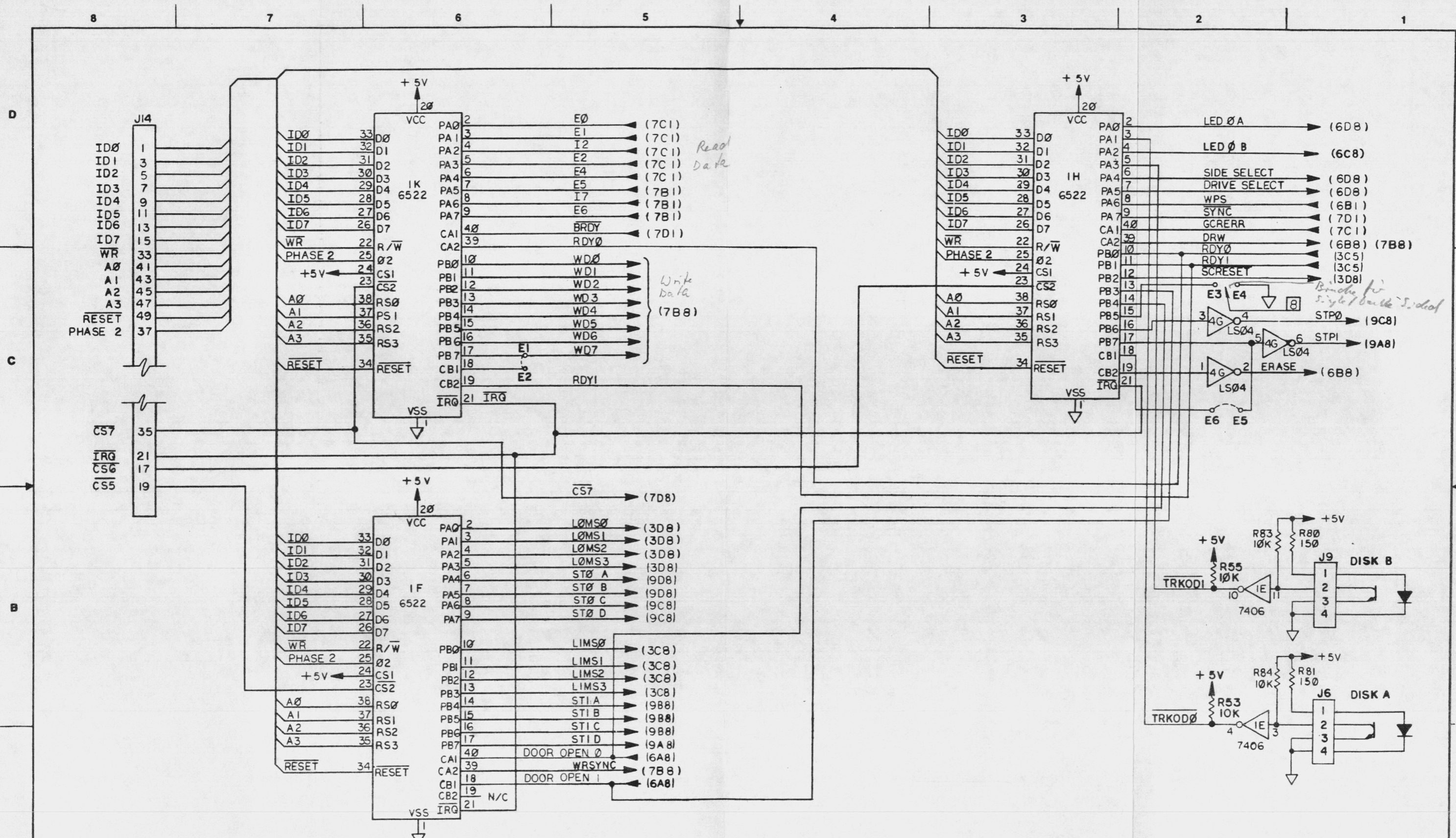


SPARE GATES

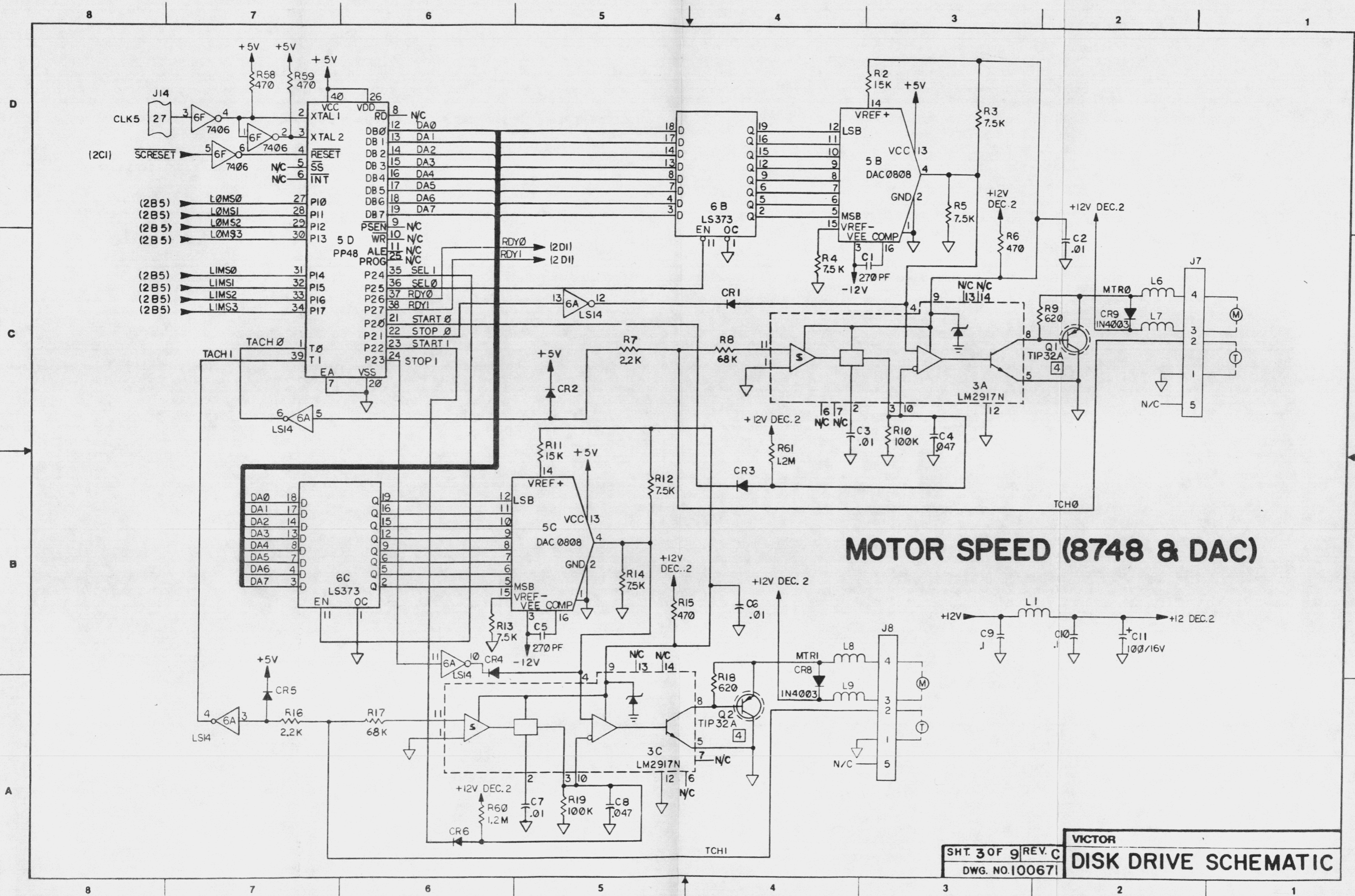
SHEET	DESCRIPTION
1	POWER & SPARES
2	CPU INTERFACE (6522)
3	MOTOR SPEED (8748 & DAC)
4	PLL
5	RD/WR HEAD INTERFACE
6	DRIVE SELECT, LED, DECODE
7	GCR EN/DE-CODER
8	DISK CONNECTORS (REF)
9	STEPPER CONTROL

SHT. 1 OF 9 REV. C
DWG. NO. 100671

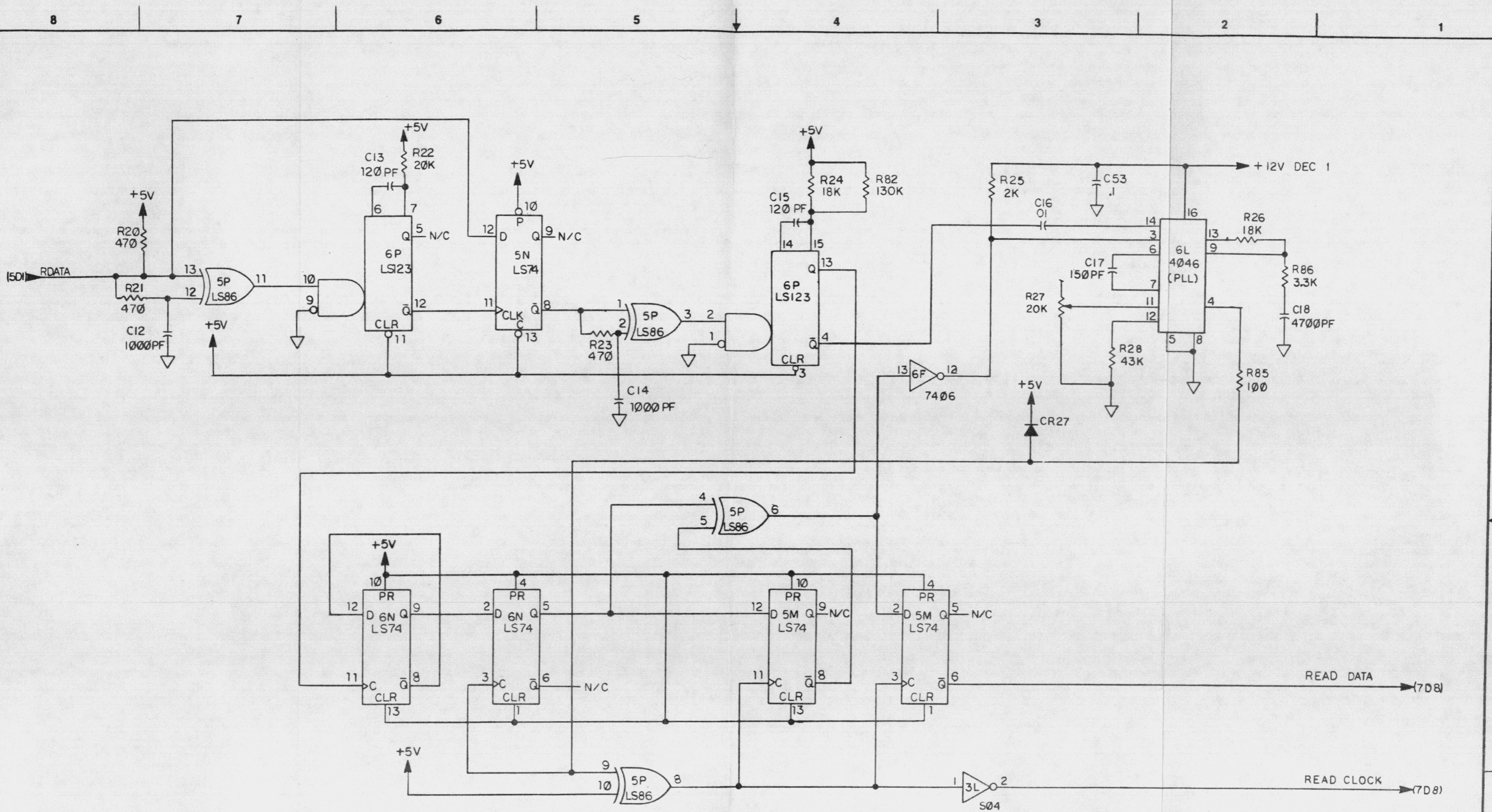
VICTOR
DISK DRIVE SCHEMATIC



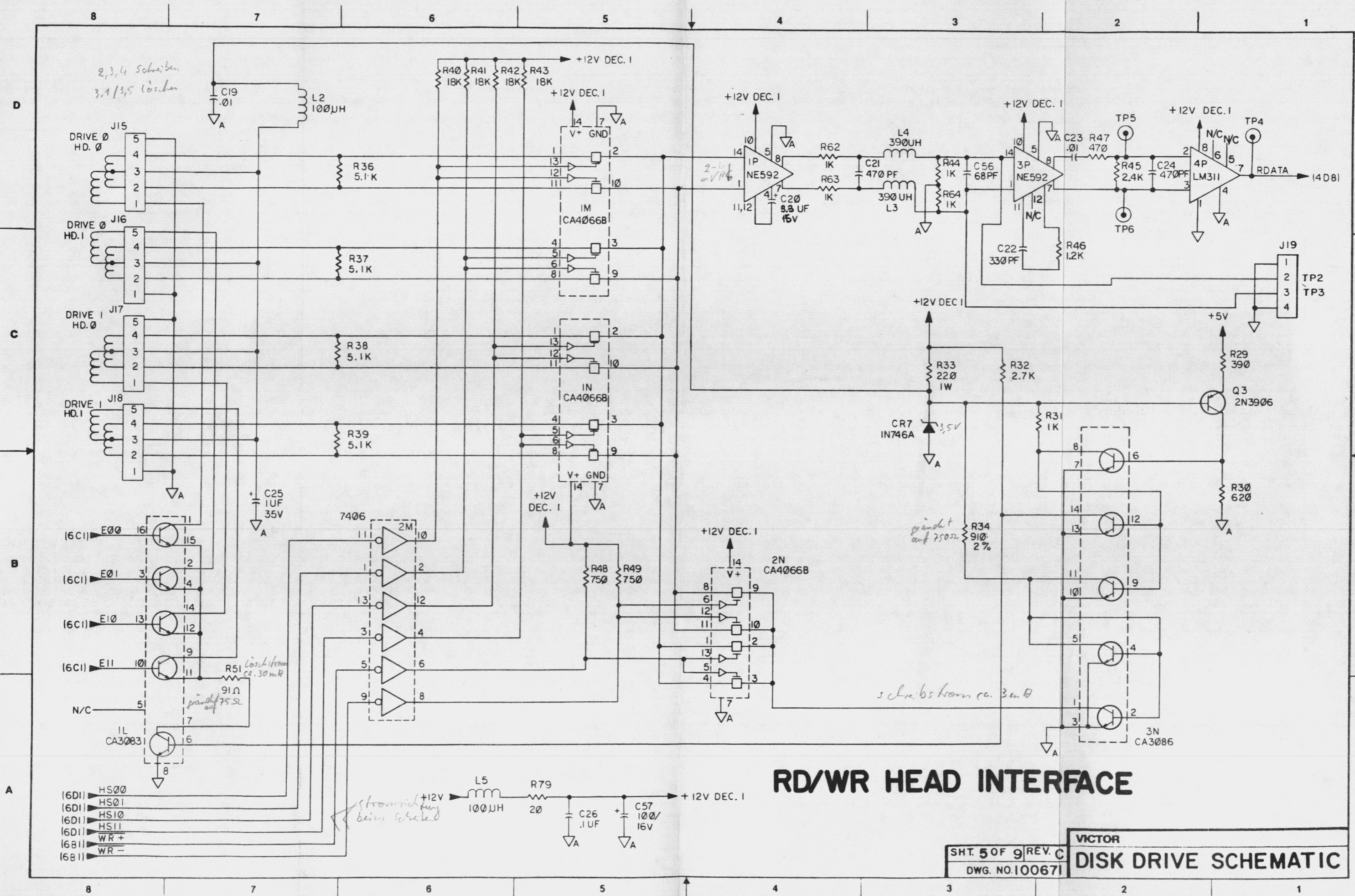
CPU INTERFACE (6522)



MOTOR SPEED (8748 & DAC)



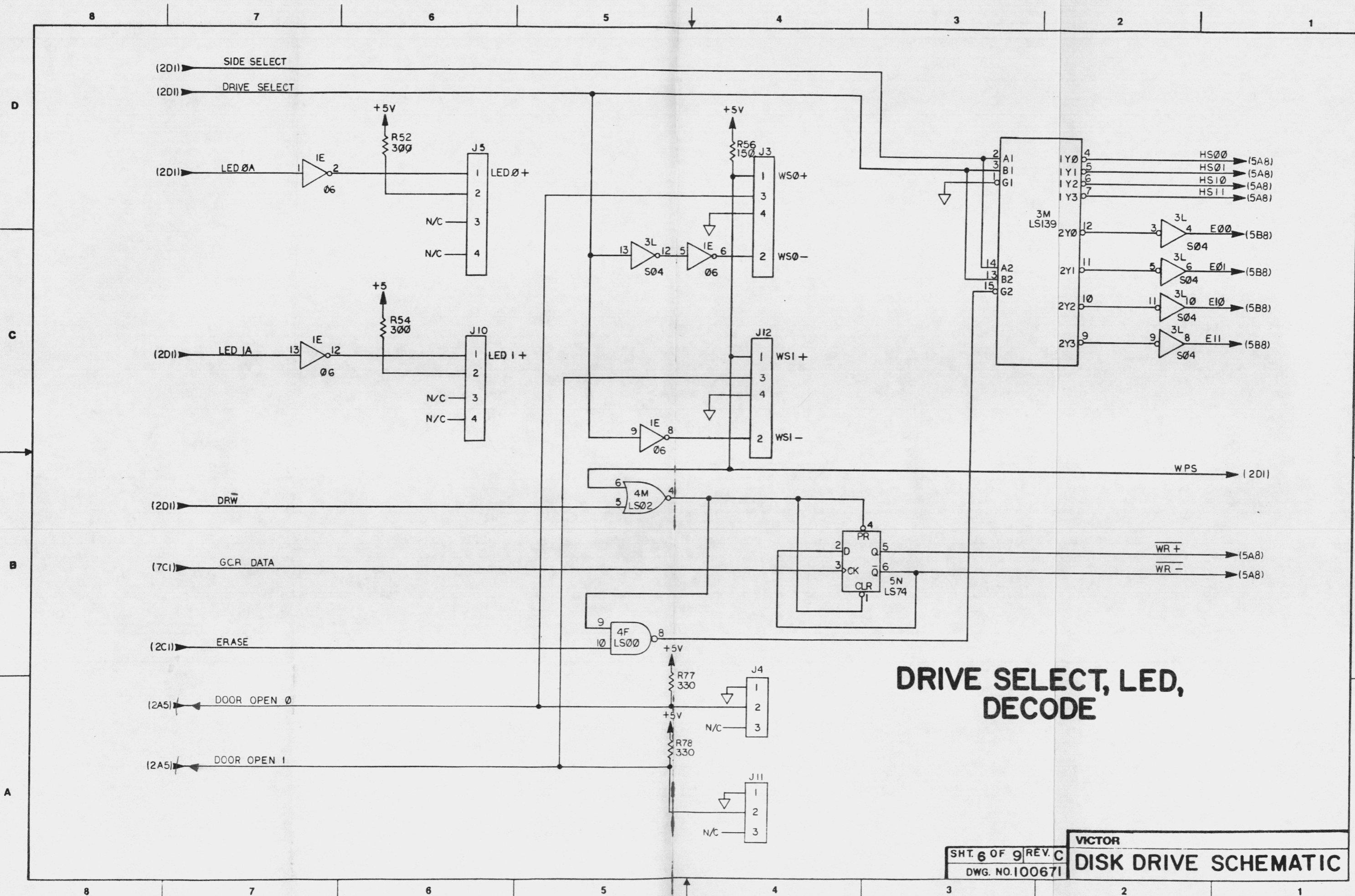
PHASE LOCKED LOOP



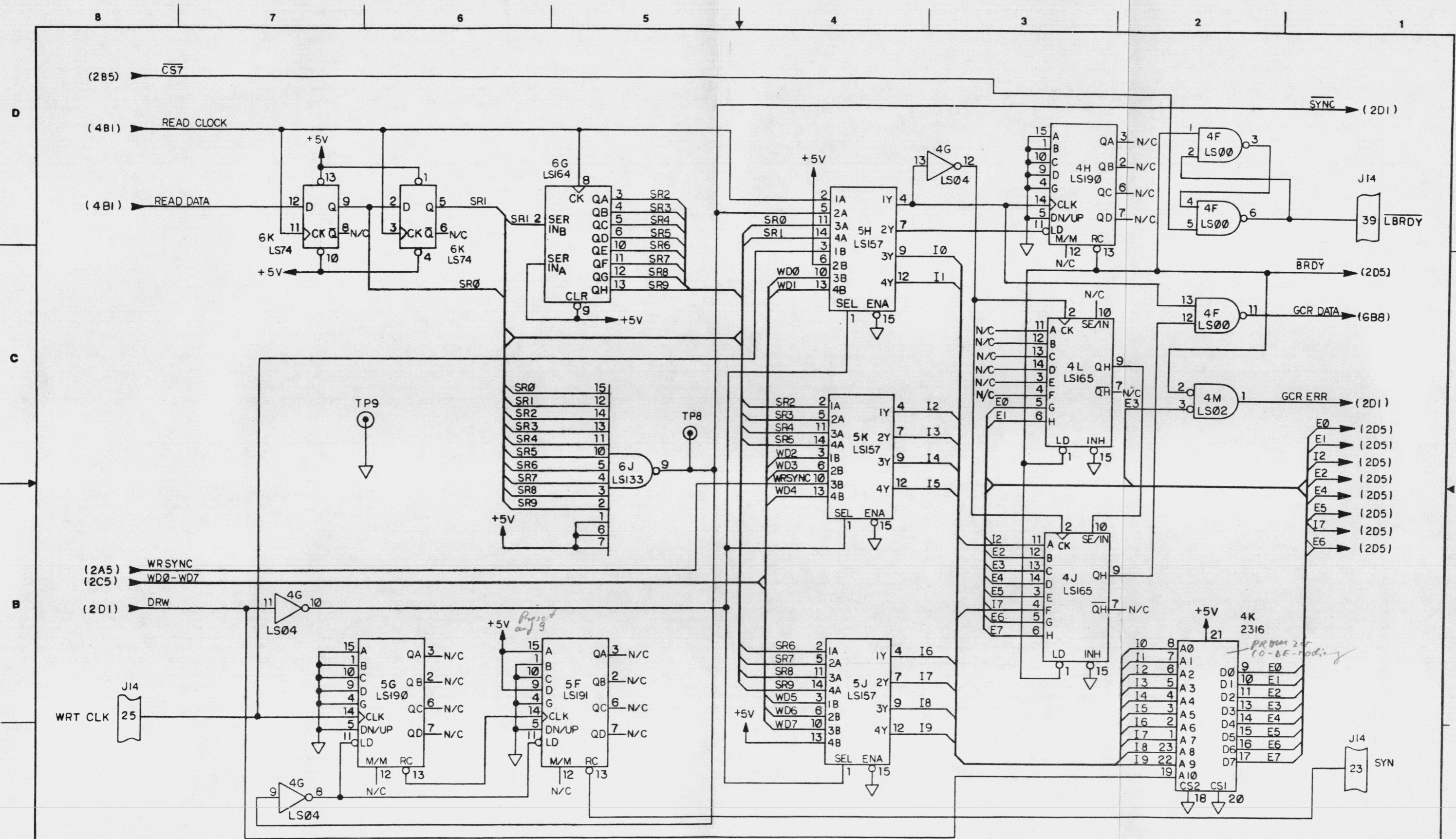
RD/WR HEAD INTERFACE

SHT. 5 OF 9 REV. C
DWG. NO. 100671

VICTOR
DISK DRIVE SCHEMATIC

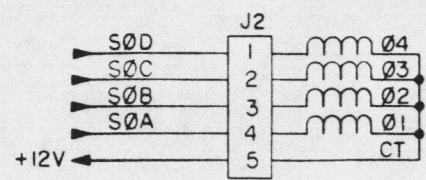


DRIVE SELECT, LED, DECODE

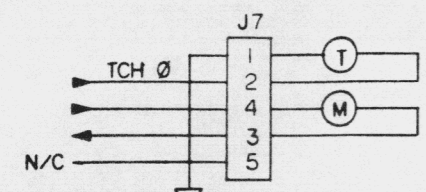


GCR EN/DE-CODER

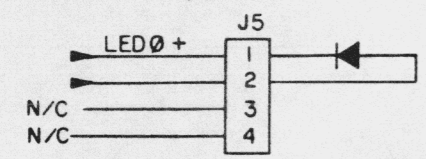
8 7 6 5 4 3 2 1



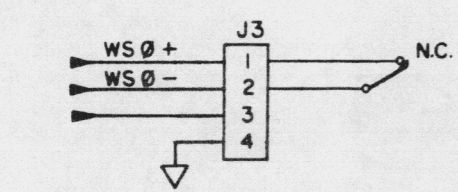
STEPPER A
(SHT 9)



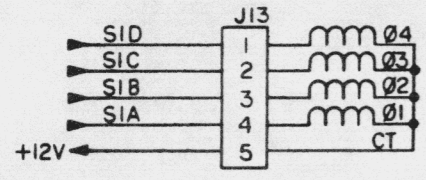
MOTOR A (8748, DAC, DISCRETE)
(SHT 3)



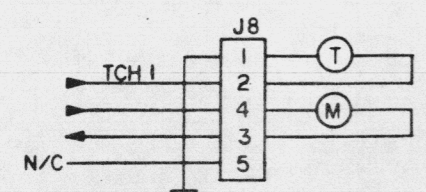
ACTIVITY LED A
(SHT 6)



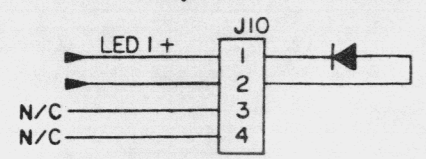
WRITE PROTECT A
(SHT 6)



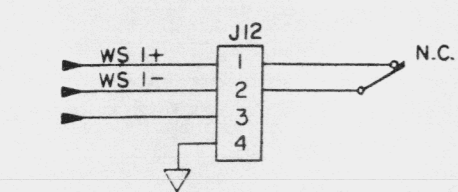
STEPPER B
(SHT 9)



MOTOR B
(SHT 3)

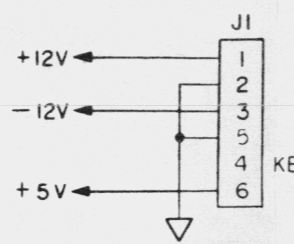
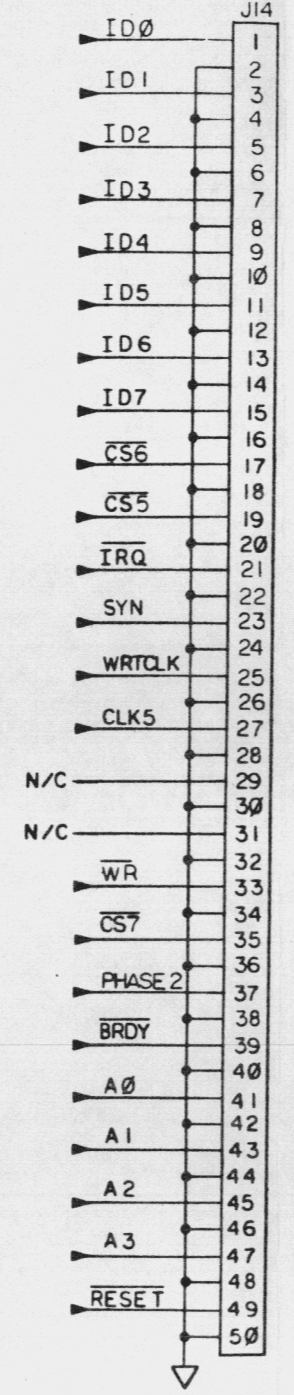


ACTIVITY LED B
(SHT 6)



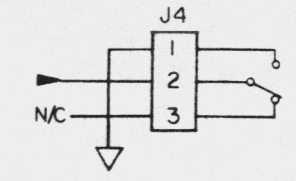
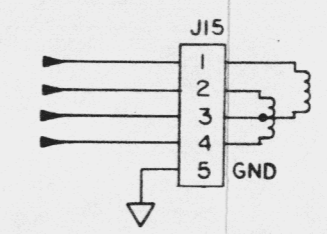
WRITE PROTECT B
(SHT 6)

CPU INTERFACE (6522)
(SHT 2)



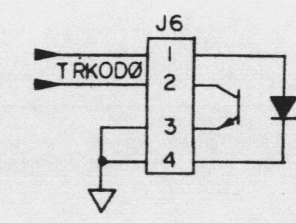
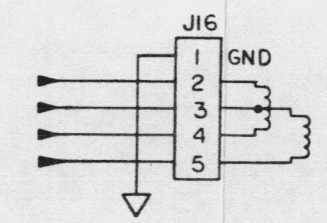
POWER CONNECTOR
(SHT 1)

DRIVE A HEAD 0
(SHT 5)



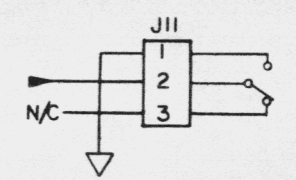
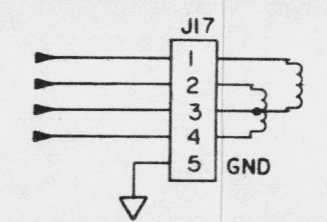
MOTOR START SWITCH A
(SHT 6)

DRIVE A HEAD 1
(SHT 5)



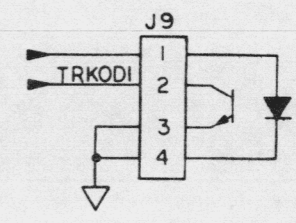
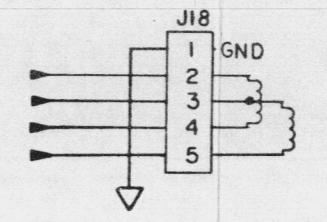
DISK A
(SHT 2)

DRIVE B HEAD 0
(SHT 5)



MOTOR START SWITCH B
(SHT 6)

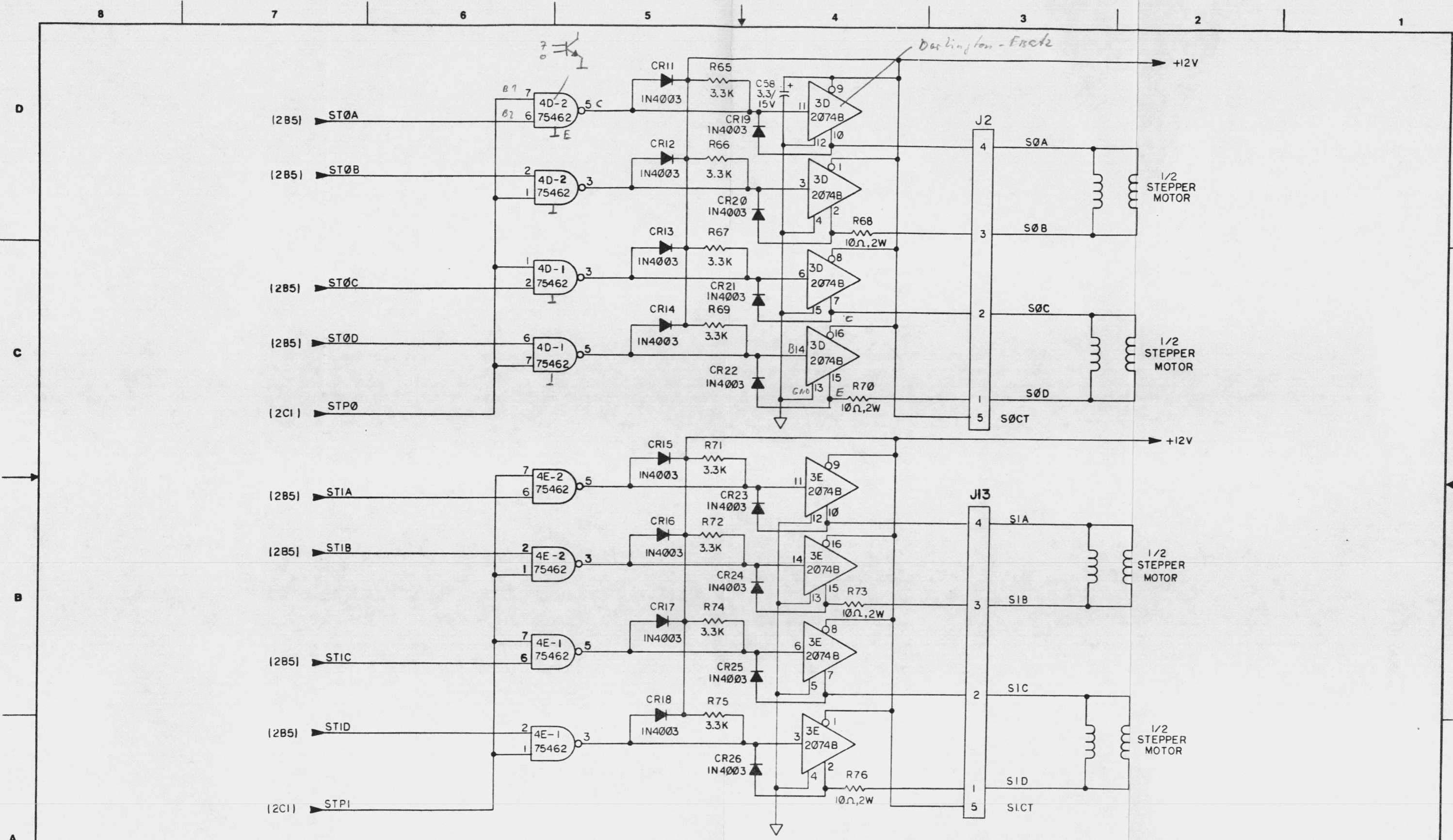
DRIVE B HEAD 1
(SHT 5)



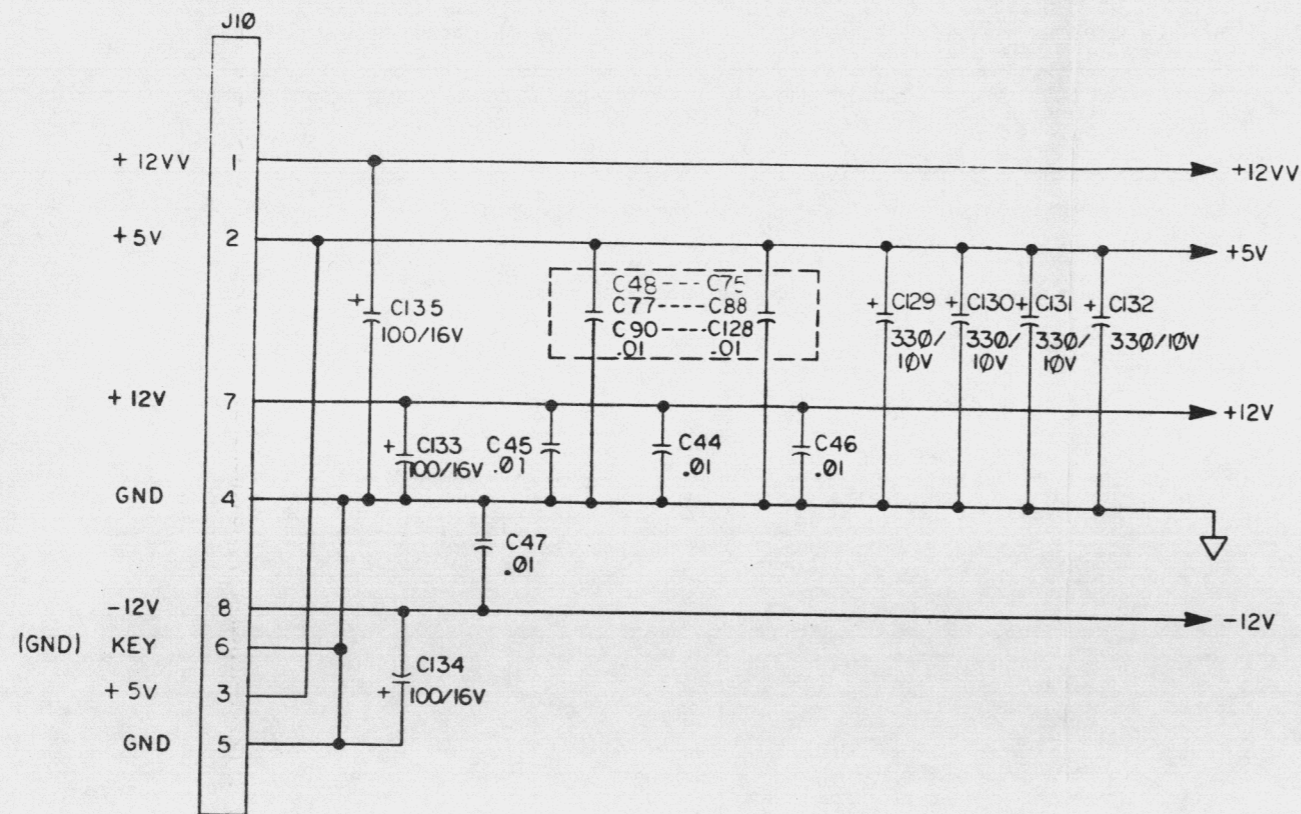
DISK B
(SHT 2)

DISK CONNECTORS (REF)

8 7 6 5 4 3 2 1



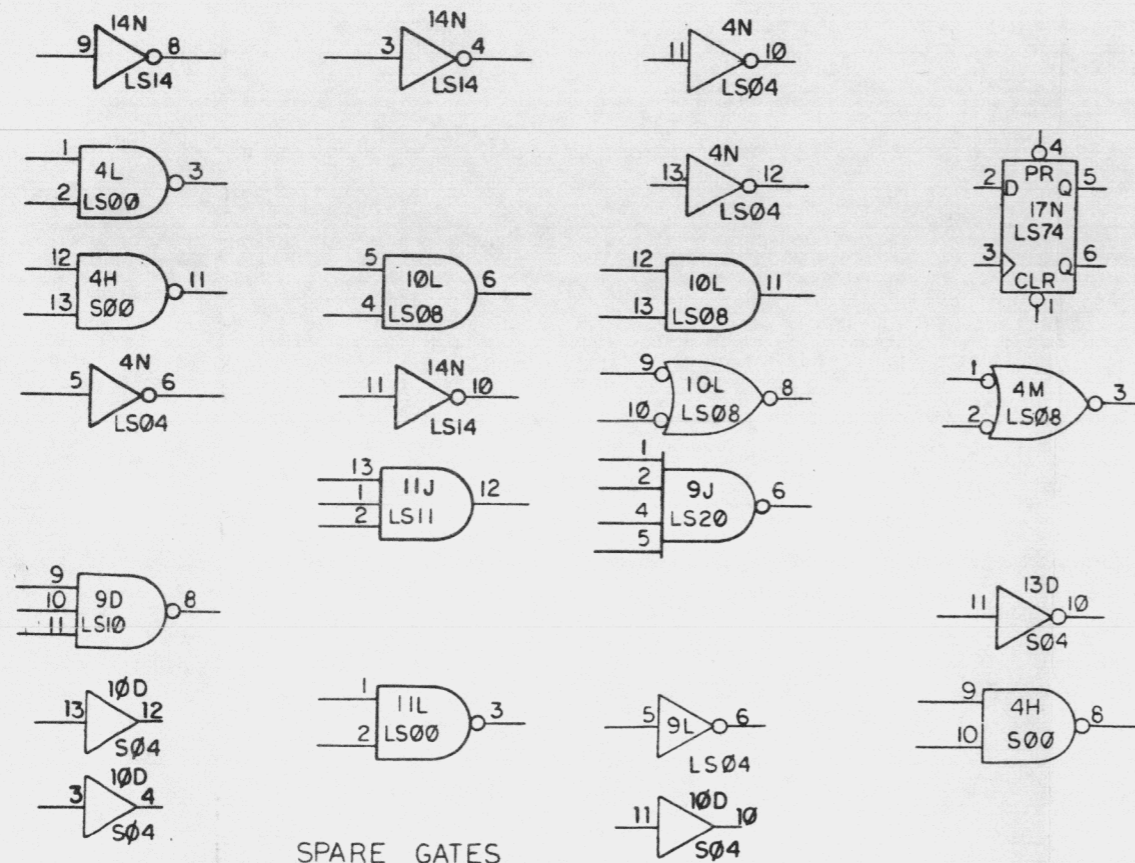
STEPPER CONTROL



NOTES: UNLESS OTHERWISE SPECIFIED:

1. ELECTRICAL VALUES ARE IN OHMS, MICROFARADS AND MICROHENRIES
2. ALL RESISTORS ARE $\pm 5\%$, 1/4 W
3. ALL INTEGRATED CIRCUITS ARE SN74 SERIES.
4. I.C. PINS ARE GND=7, +5V=14 EXCEPT FOR:

TYPE	GND	+5V	+12V
74LS112	8	16	—
74LS138	8	16	—
74LS139	8	16	—
74LS151	8	16	—
74LS153	8	16	—
74LS157	8	16	—
74LS163	8	16	—
74LS166	8	16	—
74LS257	8	16	—
74LS244	10	20	—
74LS245	10	20	—
74LS374	10	20	—
74LS373	10	20	—
74LS374	10	20	—
LM324	11	—	4
4066	7	—	14
2732	12	24	—
75160	10	20	—
75161	10	20	—
6116	12	24	—
4164	8	16	—
8259A	14	28	—
74LS90	10	5	—



5. NOT USED: J15, RESISTORS: R18,30, 31, 39,40,41,42, 44, 45,46, 47,48,49,50, 63,68 69,43,66,67. CAPS: 1,13, 19,20,21,22,23,24, 27,136 28,76,39, E19,20,21,22,13,14,15,16,17,18

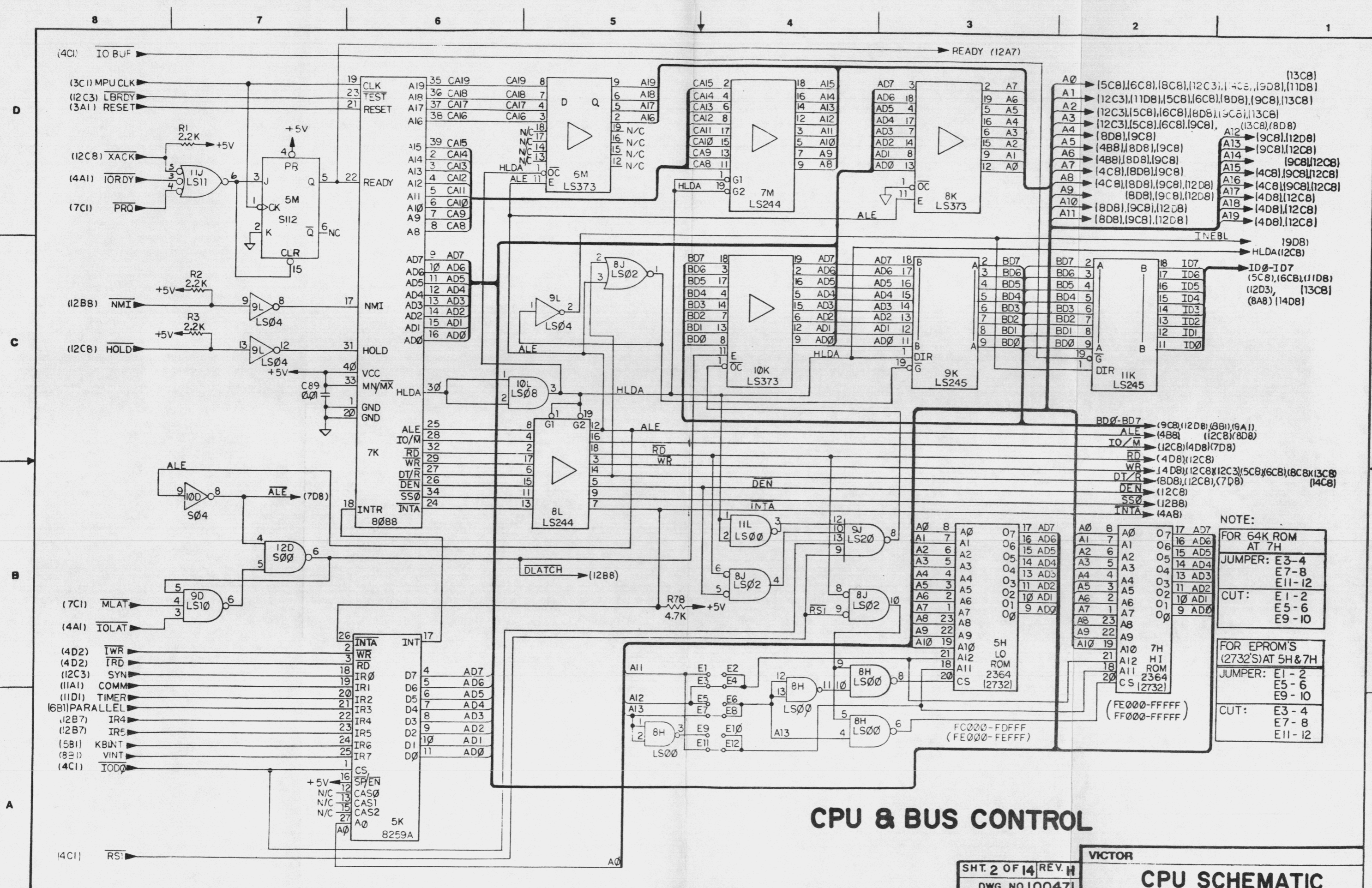
6. FOR JUMPER CONFIGURATION FOR USE WITH EITHER PROMS IN LOCATIONS 5H & 7H OR 64K ROM IN LOCATION 7H SEE NOTE IN AREA B1 ON SHEET 2.

POWER & SPARES

SHT. 1 OF 14 REV. H
DWG. NO. 100471

VICTOR

CPU SCHEMATIC



CPU & BUS CONTROL

NOTE:

FOR 64K ROM AT 7H
 JUMPER: E3-4
 E7-8
 E11-12
 CUT: E1-2
 E5-6
 E9-10

FOR EPROM'S (2732'S) AT 5H & 7H
 JUMPER: E1-2
 E5-6
 E9-10
 CUT: E3-4
 E7-8
 E11-12

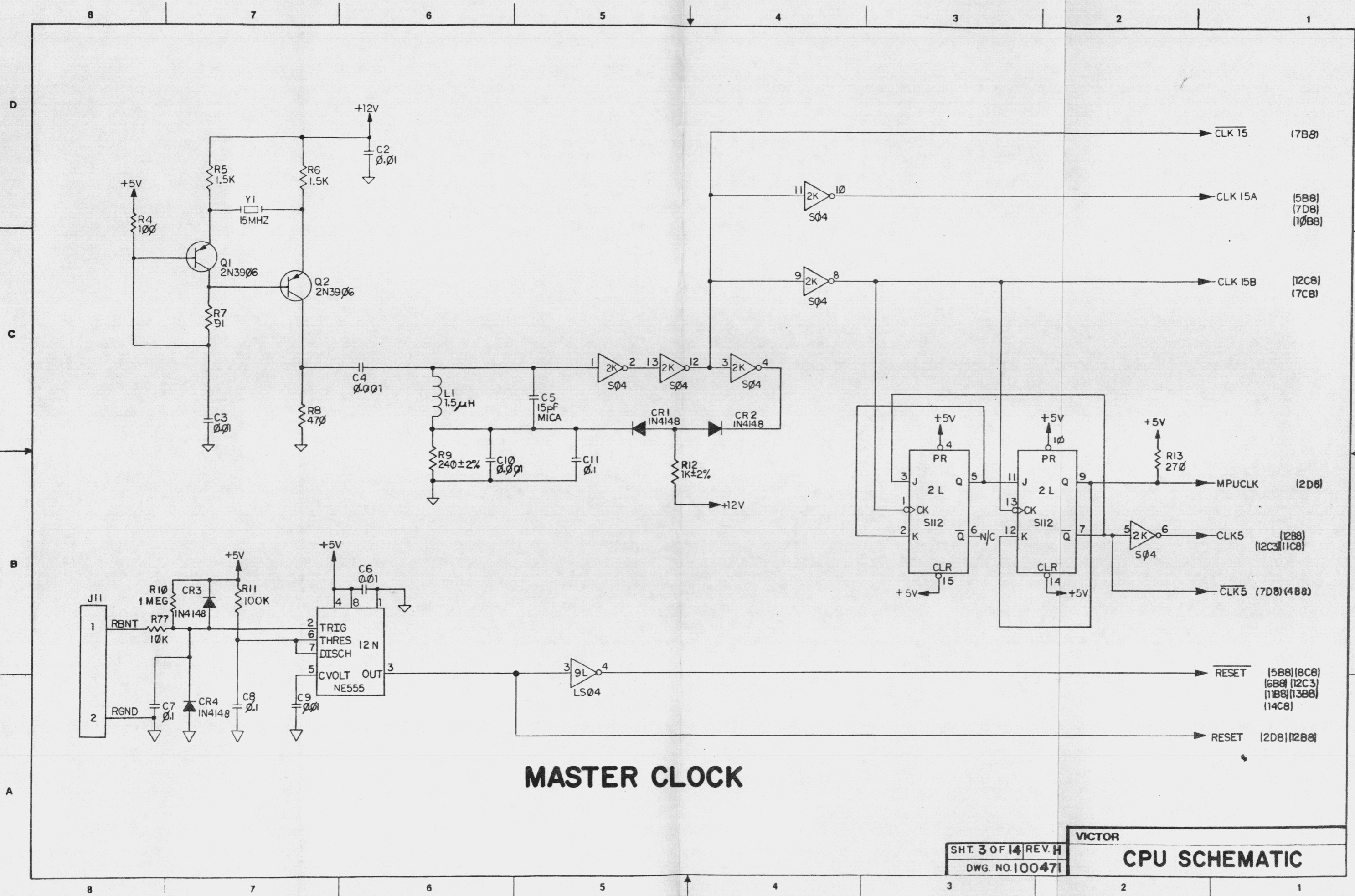
A0	8	A0	07	17	AD7
A1	7	A1	06	16	AD6
A2	6	A2	05	15	AD5
A3	5	A3	04	14	AD4
A4	4	A4	03	13	AD3
A5	3	A5	02	11	AD2
A6	2	A6	01	10	AD1
A7	1	A7	00	9	AD0
A8	23	A8			
A9	22	A9			
A10	19	A10	5H	LO	ROM
A11	18	A11	2364		
A12	20	A12	2364		
A13	19	A13	CS		
A14	18	A14			
A15	17	A15			
A16	16	A16			
A17	15	A17			
A18	14	A18			
A19	13	A19			

BD0-BD7 → (9C8),(12D8),(8B1),(9A1), (4B8) (12C8),(8D8)
 ALE → (12C8),(4D8),(7D8)
 IO/M → (4D8),(12C8)
 RD → (4D8),(12C8)
 WR → (4D8),(12C8),(12C3),(5C8),(6C8),(8C8),(13C8) (14C8)
 DT/R → (8D8),(12C8),(7D8)
 DEN → (12C8)
 SS0 → (12B8)
 INTA → (4A8)

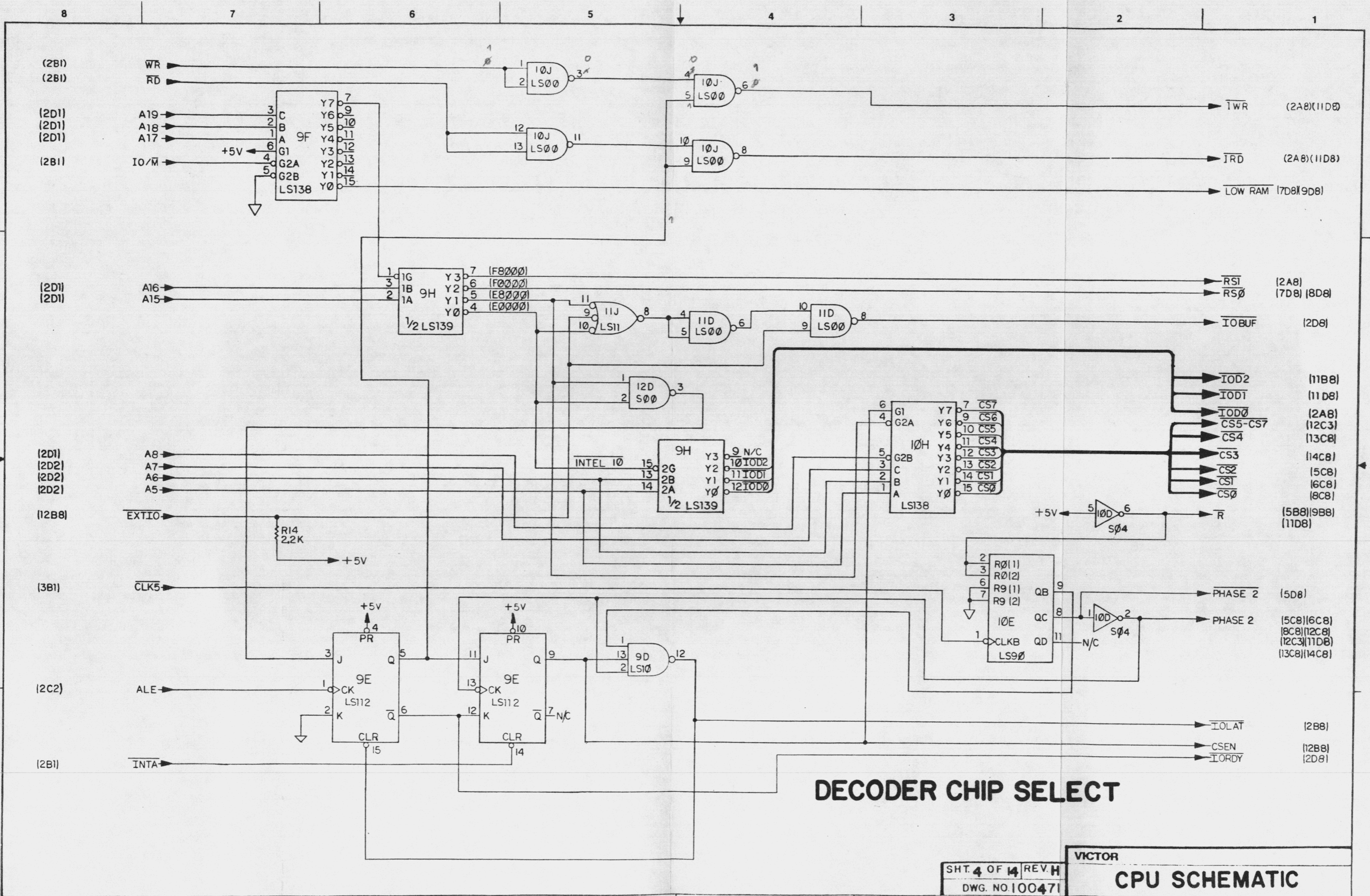
19D8) HLDA (12C8)
 ID0-ID7 → (5C8),(6C8),(11D8) (12D3), (13C8) (8A8) (14D8)

A0 → (13C8) (15C8),(6C8),(8C8),(12C3),(14C8),(9D8),(11D8)
 A1 → (12C3),(11D8),(15C8),(6C8),(8D8),(9C8),(13C8)
 A2 → (12C3),(15C8),(6C8),(8D8),(9C8),(13C8)
 A3 → (12C3),(15C8),(6C8),(8D8),(9C8),(13C8)
 A4 → (12C3),(15C8),(6C8),(8D8),(9C8),(13C8)
 A5 → (8D8),(9C8)
 A6 → (4B8),(8D8),(9C8)
 A7 → (4C8),(8D8),(9C8)
 A8 → (4C8),(8D8),(9C8)
 A9 → (4C8),(8D8),(9C8),(12D8)
 A10 → (8D8),(9C8),(12D8)
 A11 → (8D8),(9C8),(12D8)

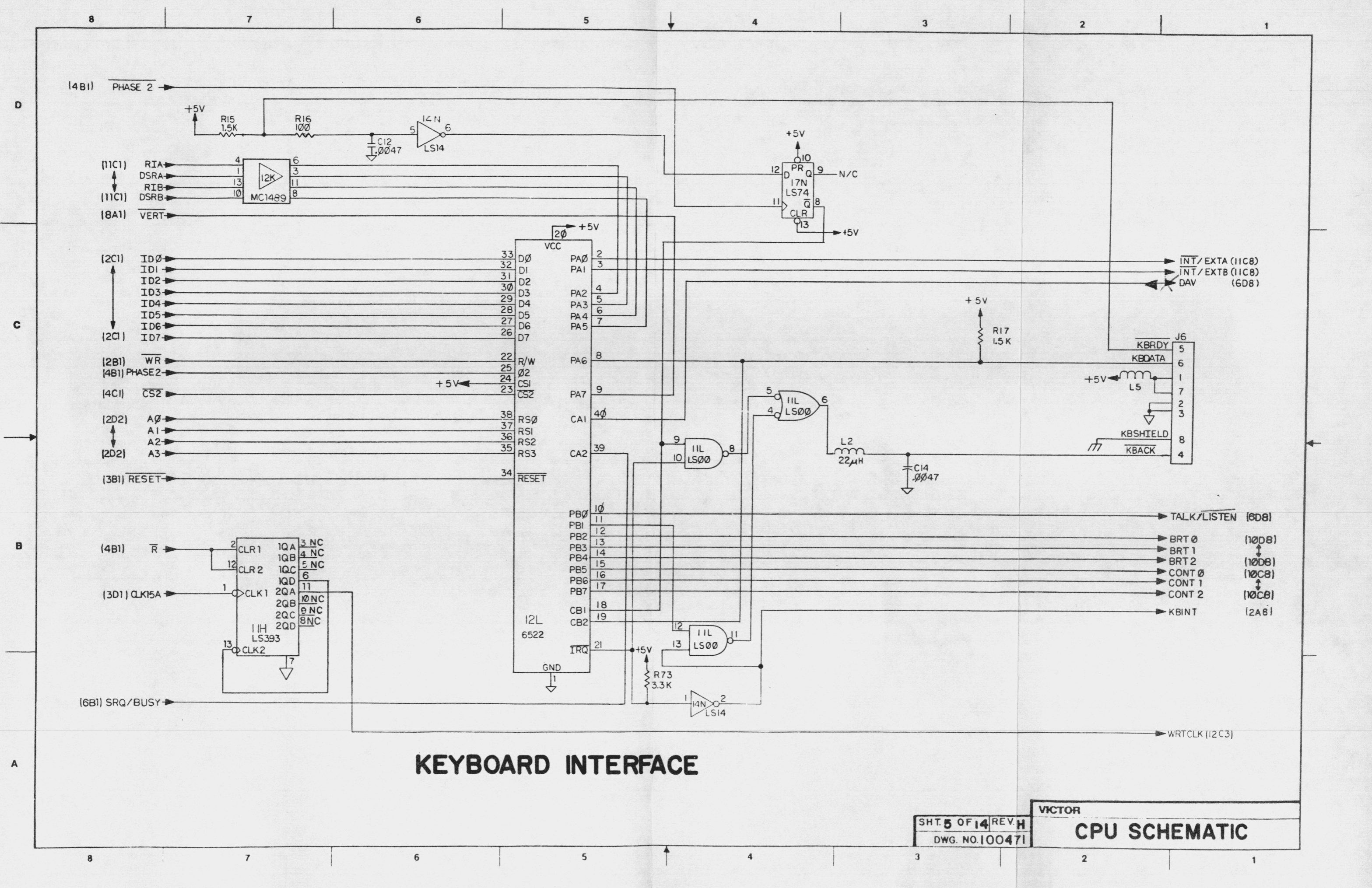
A12 → (13C8),(8D8)
 A13 → (9C8),(12D8)
 A14 → (9C8),(12C8)
 A15 → (9C8),(12C8)
 A16 → (4C8),(9C8),(12C8)
 A17 → (4C8),(9C8),(12C8)
 A18 → (4D8),(12C8)
 A19 → (4D8),(12C8)



MASTER CLOCK



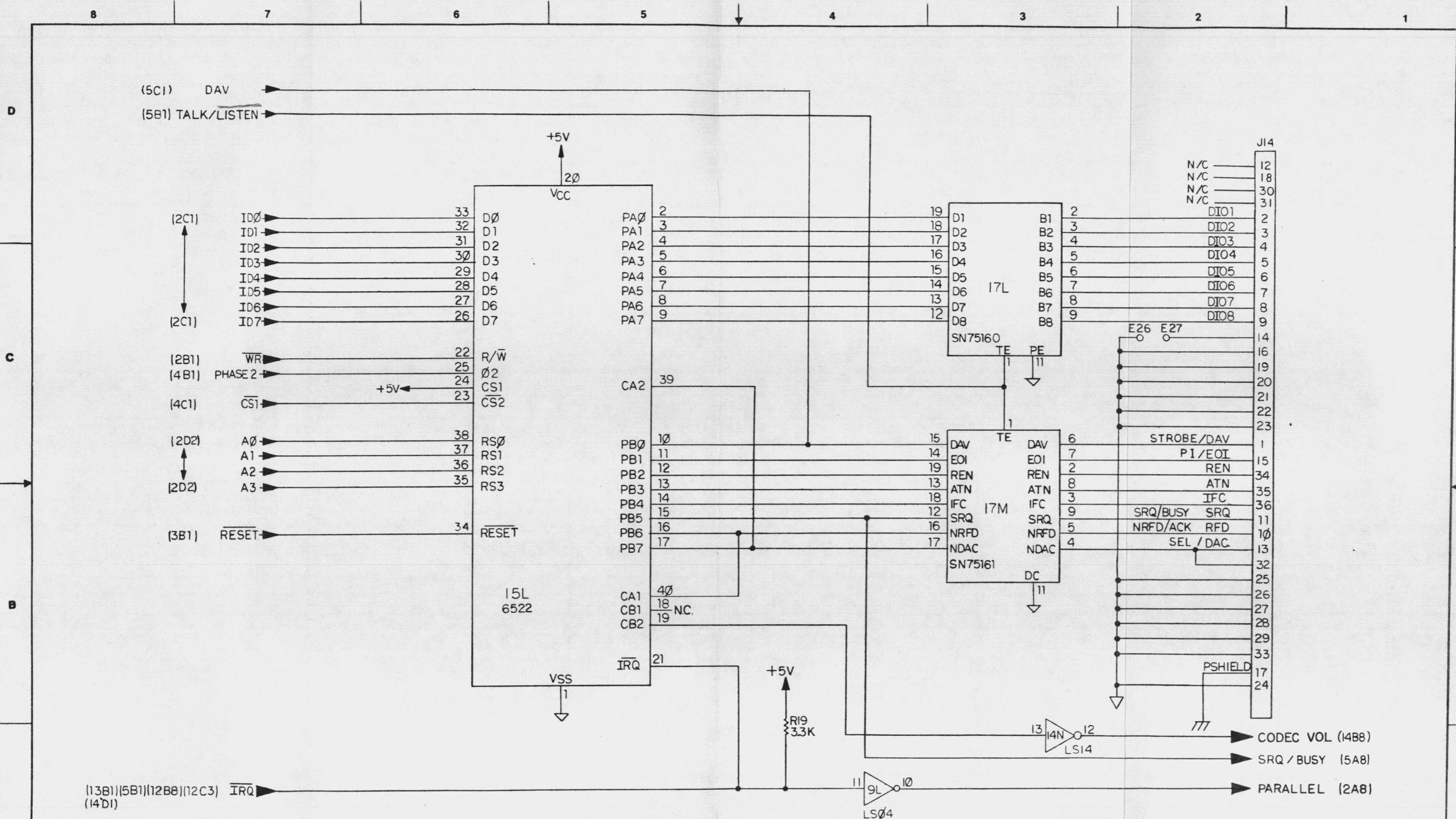
DECODER CHIP SELECT



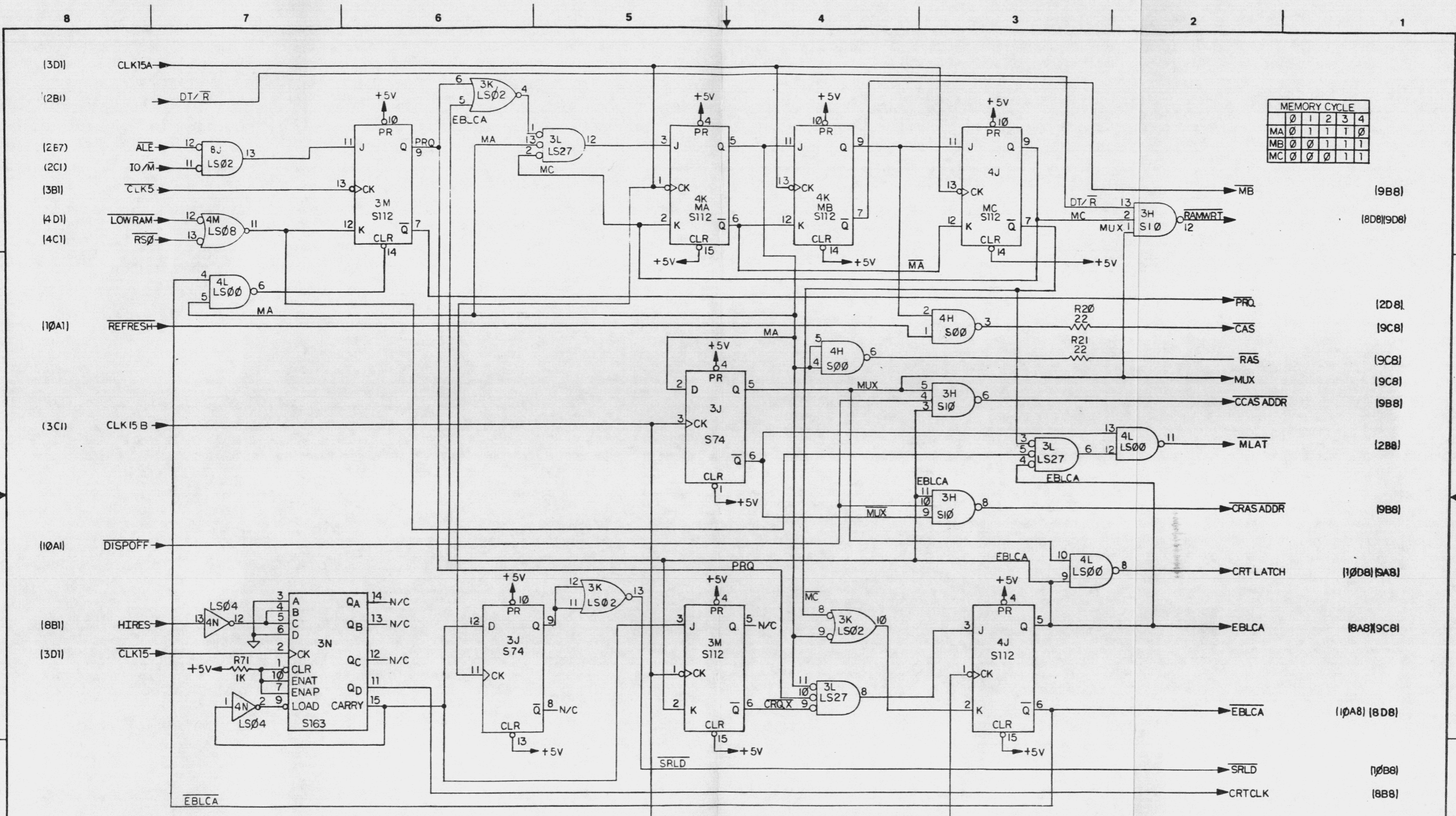
KEYBOARD INTERFACE

SHT. 5 OF 14 REV. H
 DWG. NO. 100471

VICTOR
CPU SCHEMATIC



IEEE CENTRONICS INTERFACE

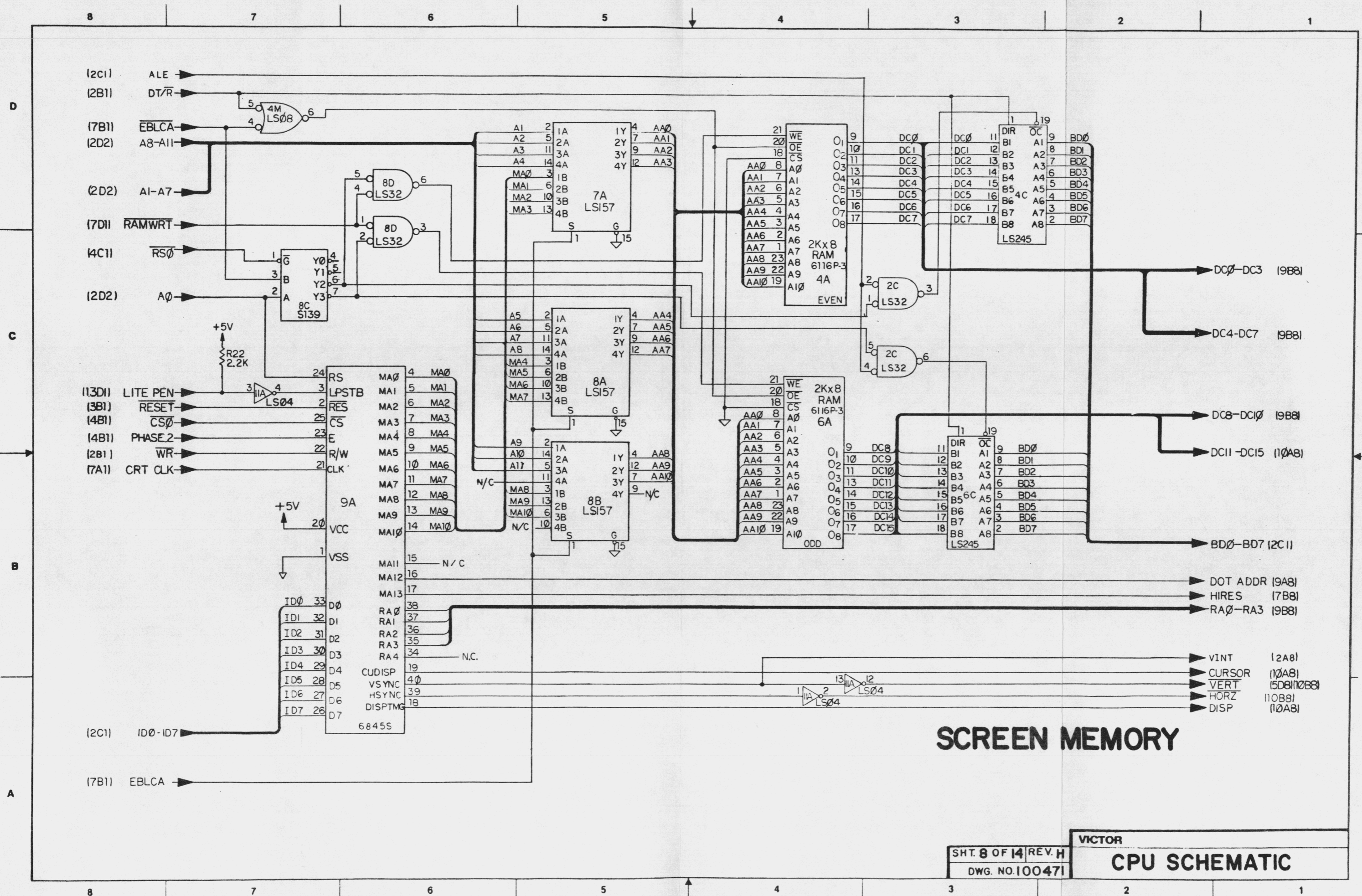


MEMORY CYCLE					
	0	1	2	3	4
MA	0	1	1	1	0
MB	0	0	1	1	1
MC	0	0	0	1	1

CRT CYCLE HIRES										
	3	4	5	6	7	8	9	0	1	2
CA	0	1	0	1	0	1	0	1	0	1
CB	0	0	1	1	0	0	1	1	1	1
CC	0	0	0	0	1	1	1	1	1	1
CD	1	1	1	1	1	1	1	1	0	0

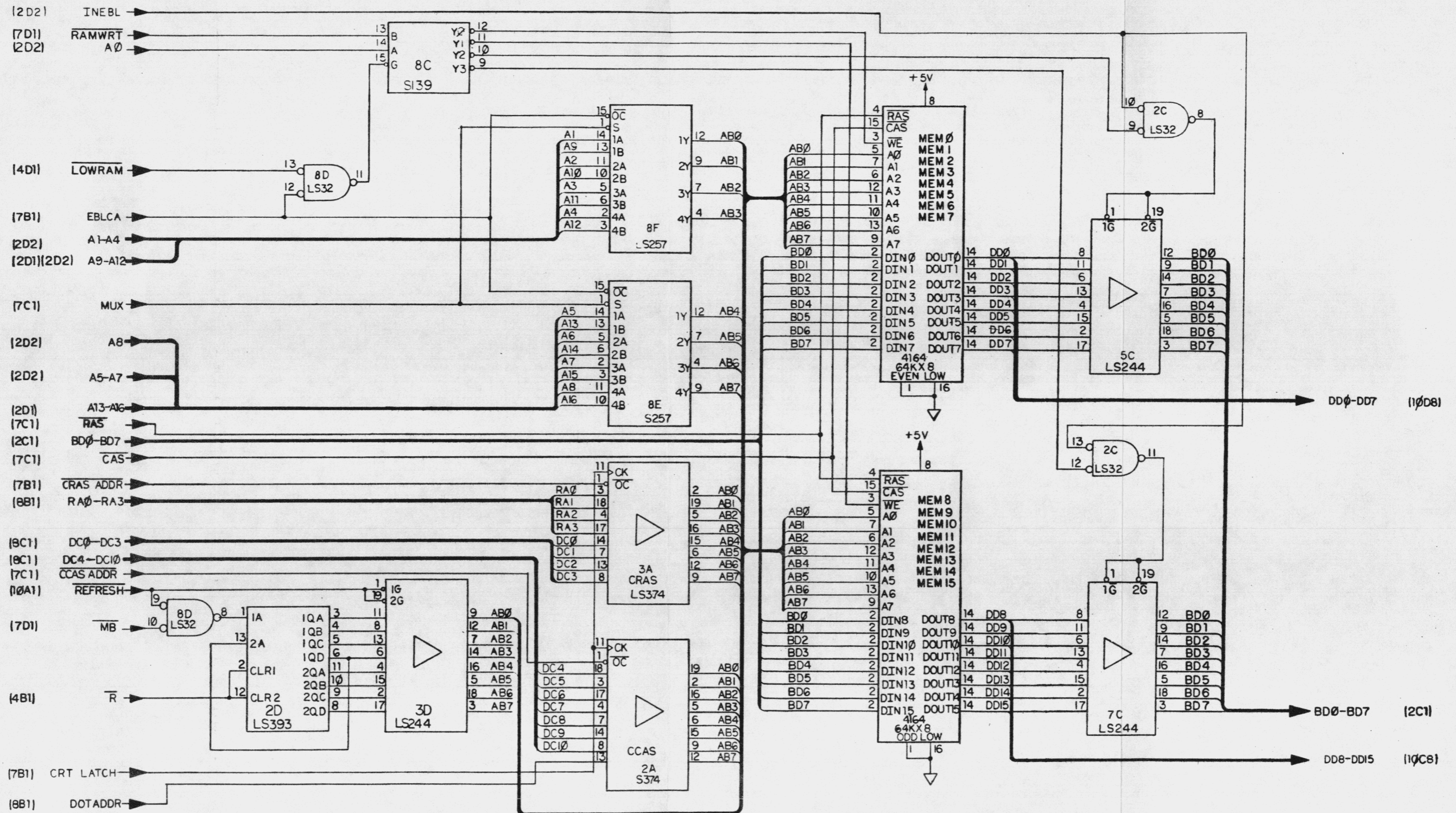
CRT CYCLE HIRES																
	9	10	11	12	13	14	15	0	1	2	3	4	5	6	7	8
CA	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
CB	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
CC	0	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1
CD	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0

CONTROL SIGNALS



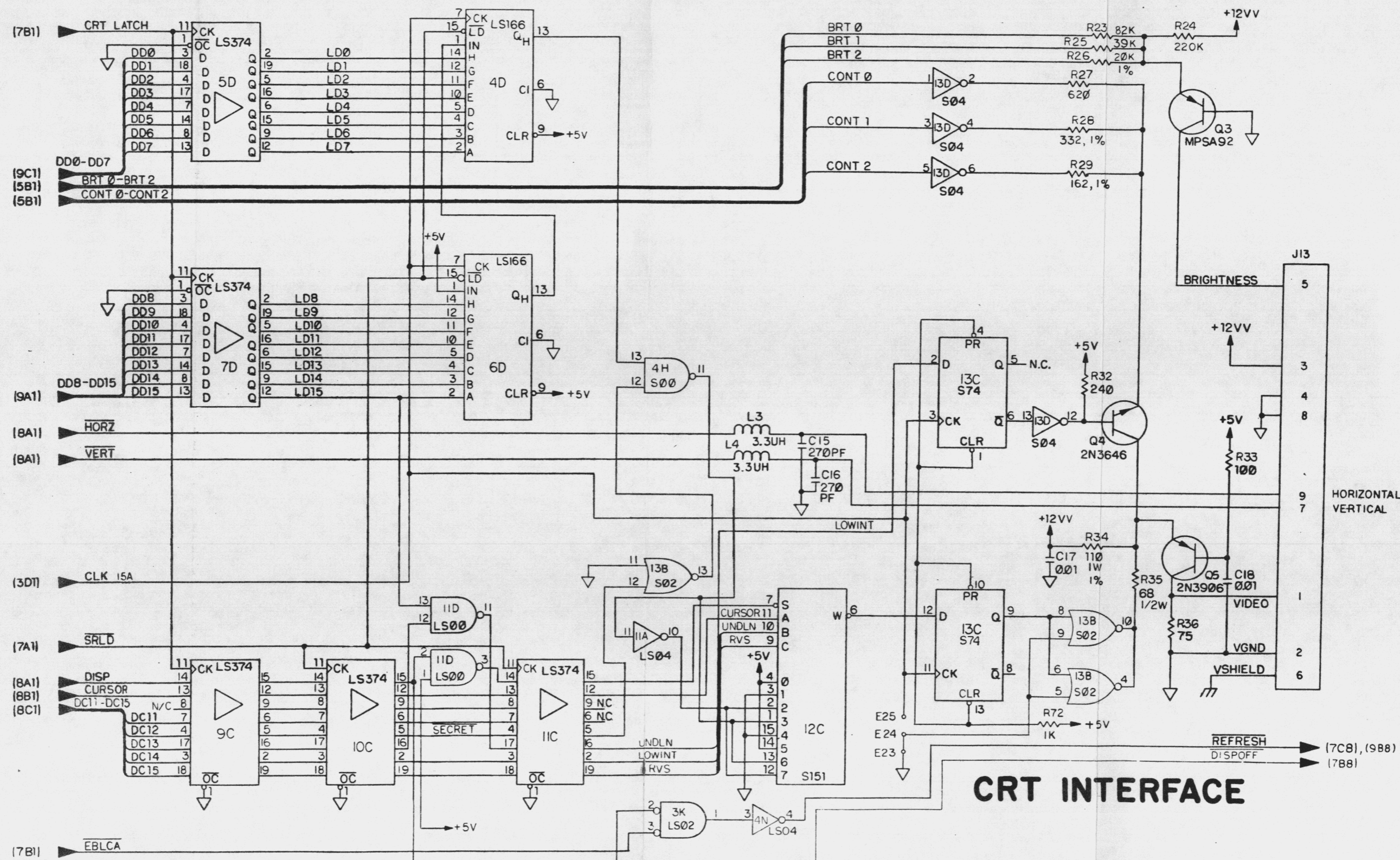
SCREEN MEMORY

SYSTEM MEMORY

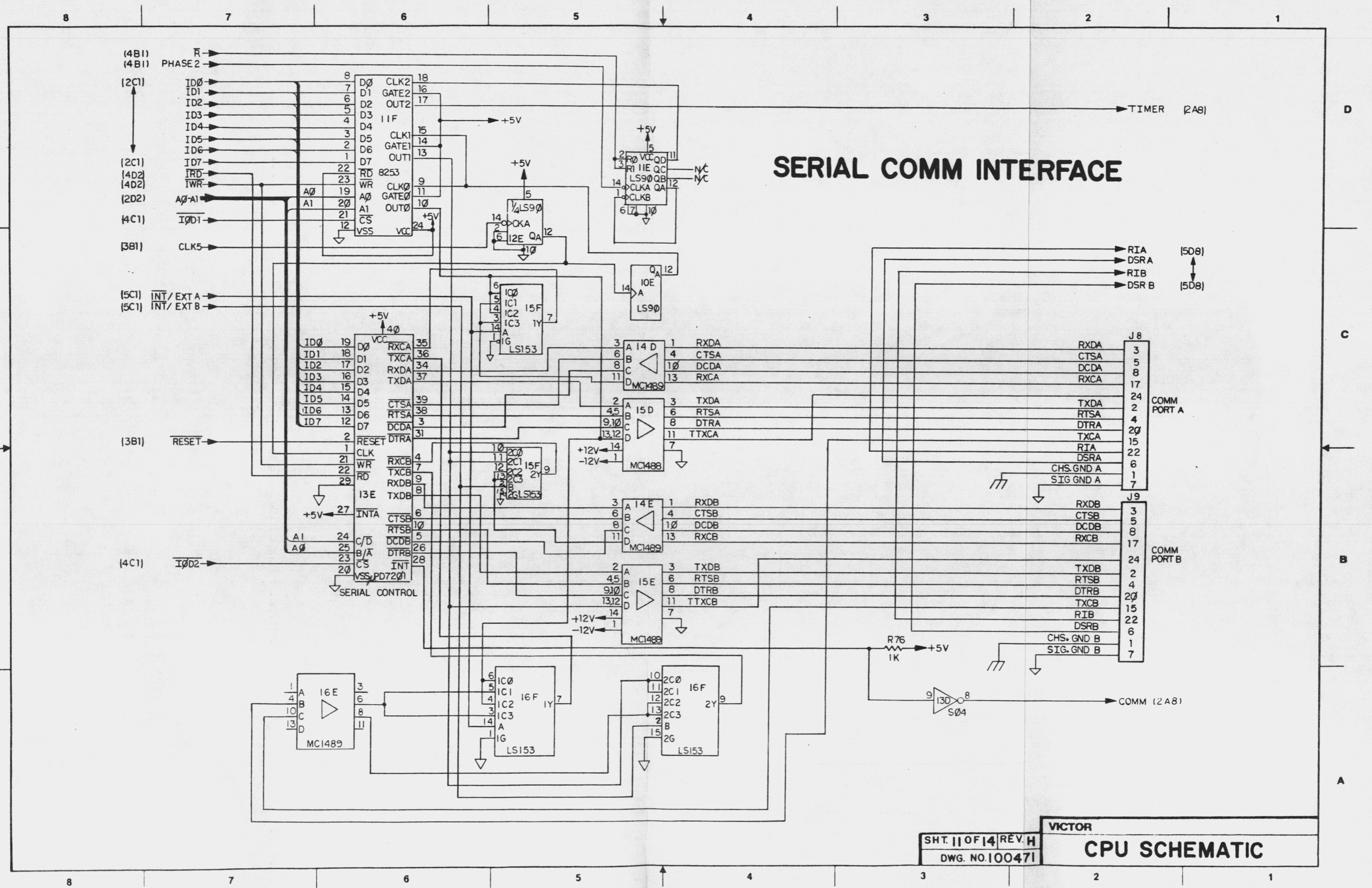


SHT. 9 OF 14 REV. H
DWG. NO. 100471

VICTOR
CPU SCHEMATIC



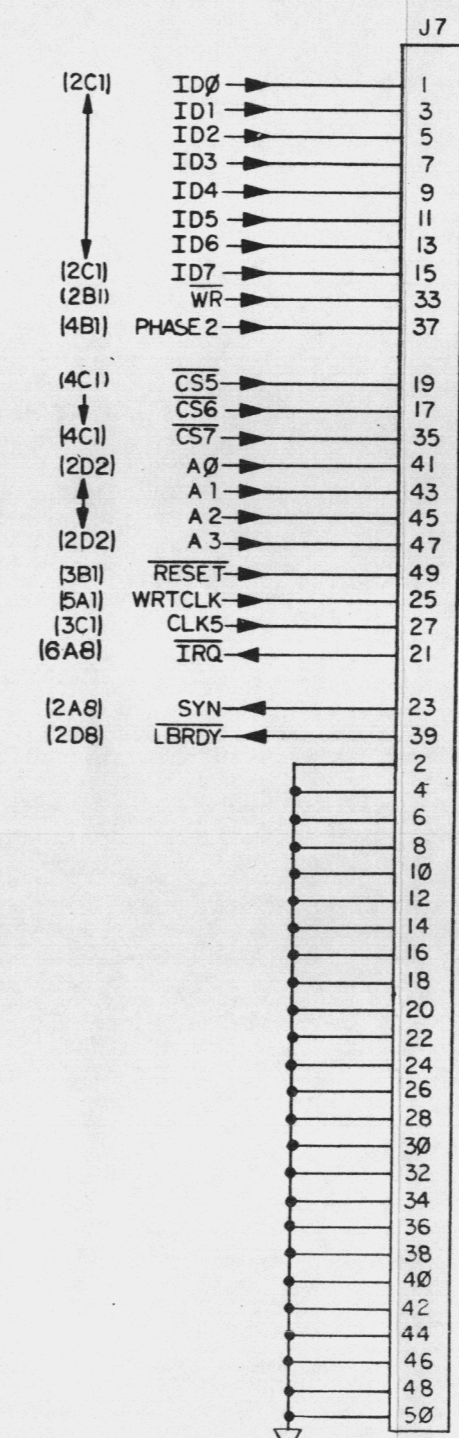
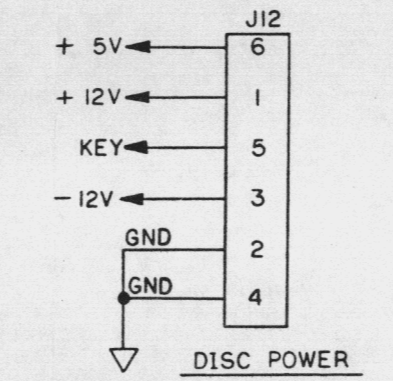
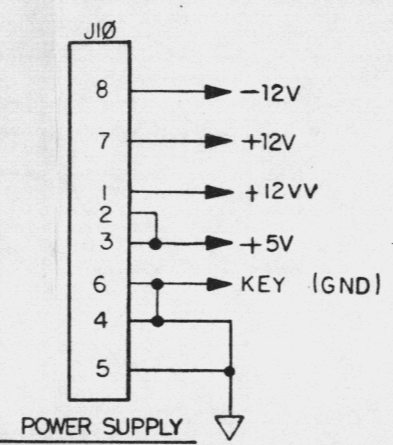
CRT INTERFACE



SERIAL COMM INTERFACE

SHT. 11 OF 14 REV. H
 DWG. NO. 100471

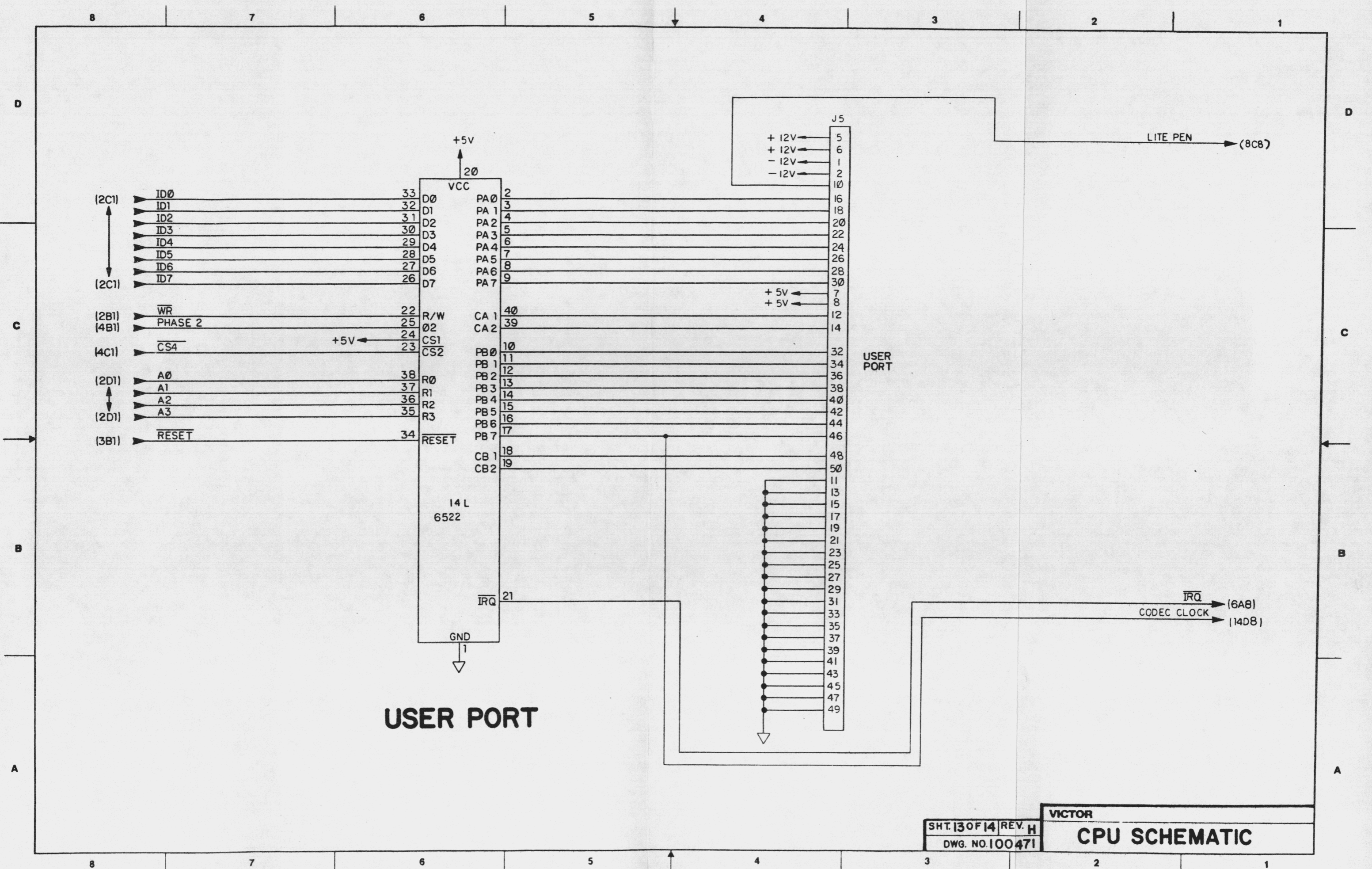
VICTOR
CPU SCHEMATIC



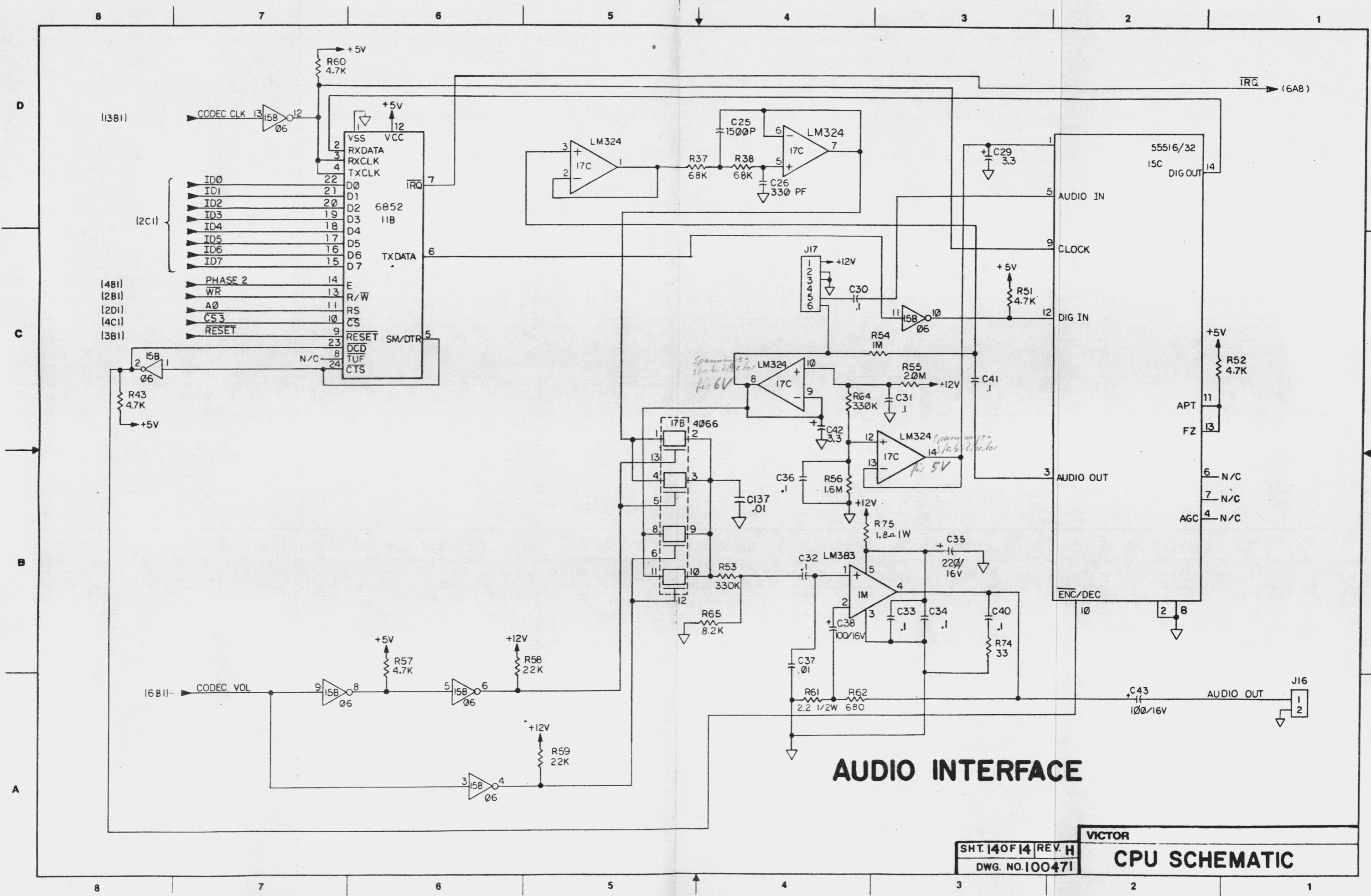
EXPANSION BUS

DISK DRIVE

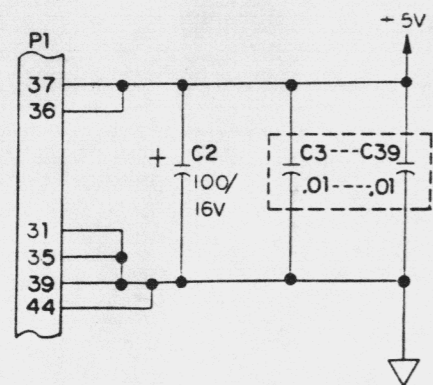
CPU CONNECTORS (REF)



USER PORT



AUDIO INTERFACE

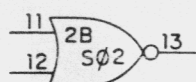


POWER & SPARES

NOTES: UNLESS OTHERWISE SPECIFIED

1. ELECTRICAL VALUES ARE IN OHMS, MICROFARADS, AND MICROHENRIES.
2. ALL RESISTORS ARE $\pm 5\%$, 1/4W
3. ALL INTEGRATED CIRCUITS ARE SN74 SERIES.
4. IC PINS ARE ,GND=7, +5V=14

IC TYPE	GND	+5V
74LS138	8	16
74LS139	8	16
74LS153	8	16
74LS157	8	16
74LS174	8	16
74LS175	8	16
74LS245	10	20
74LS373	10	20
4164	16	8

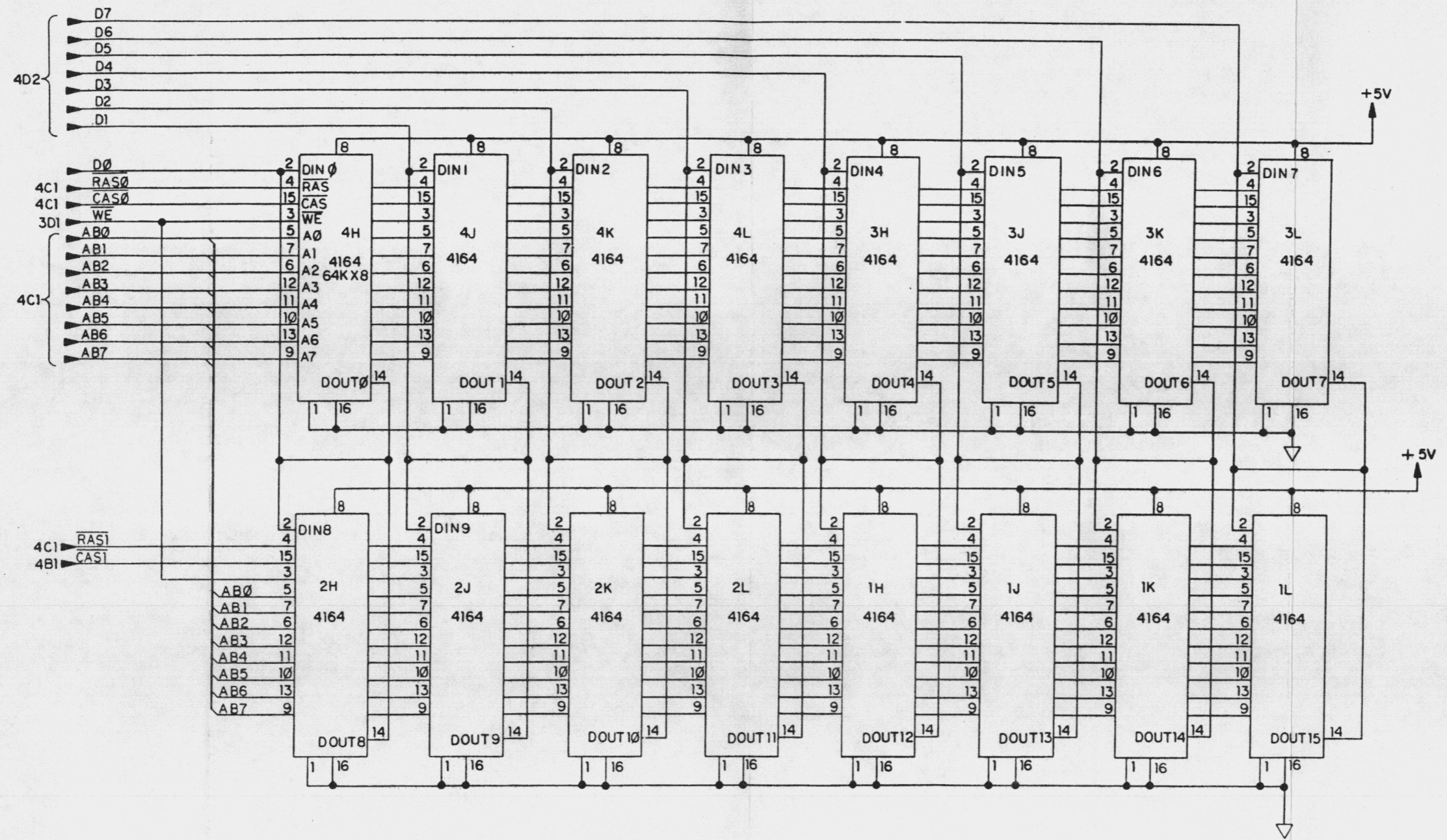


SPARE GATES

SHT. 1 OF 4 REV. P1
DWG. NO. 100901

VICTOR

128 K MEMORY SCHEMATIC

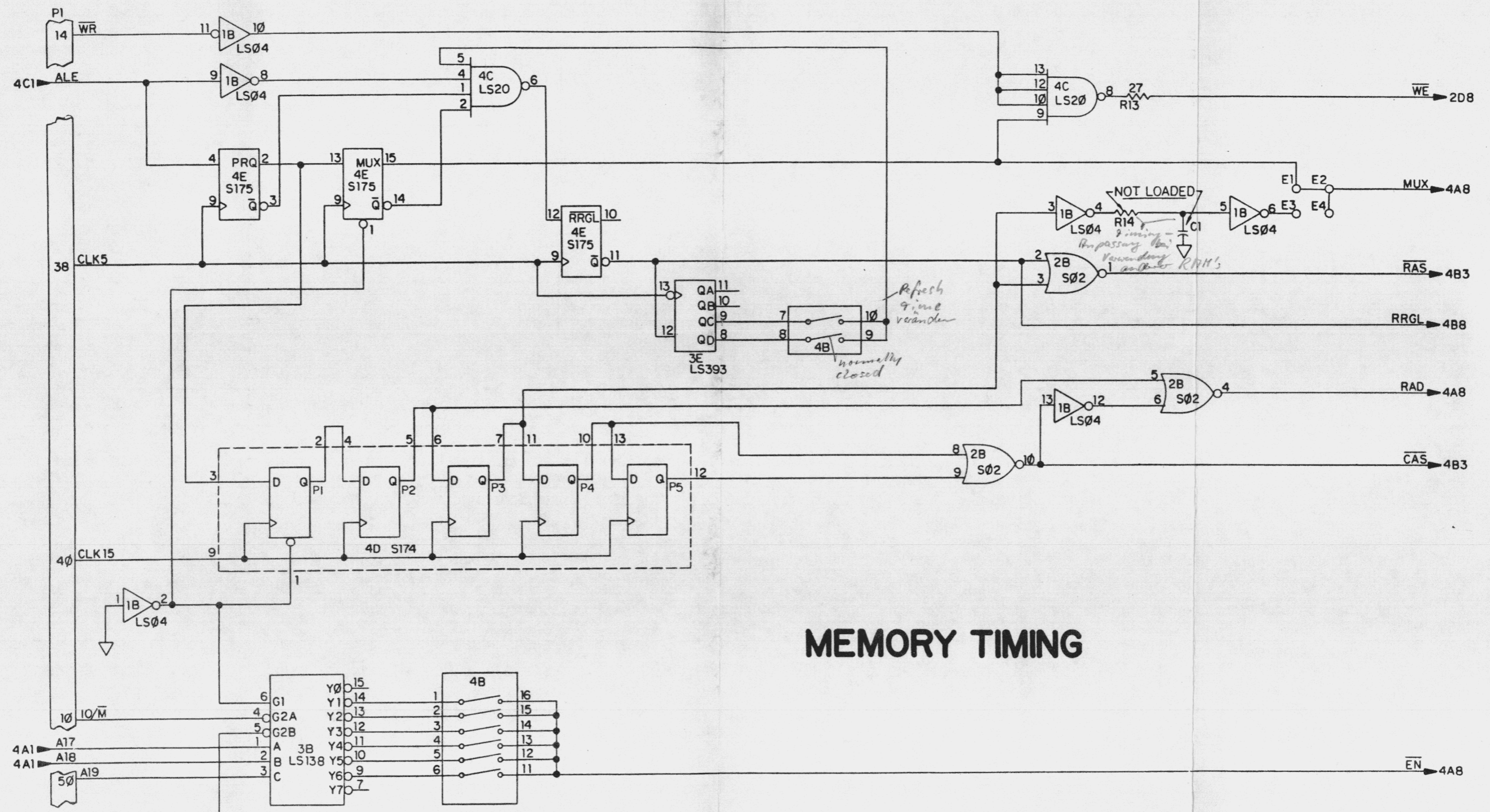


DYNAMIC RAMS

8 7 6 5 4 3 2 1

D

D



MEMORY TIMING

C

C

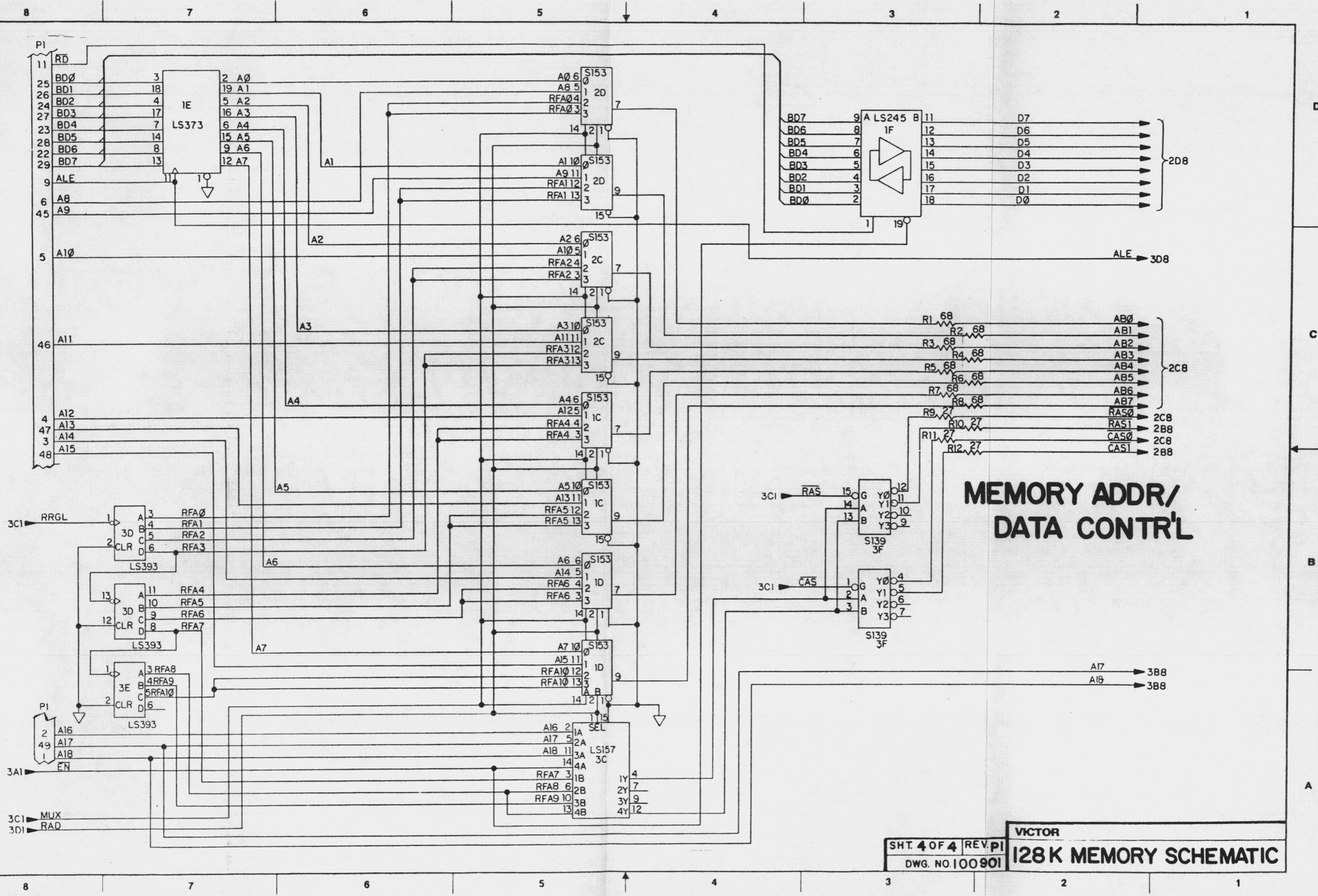
B

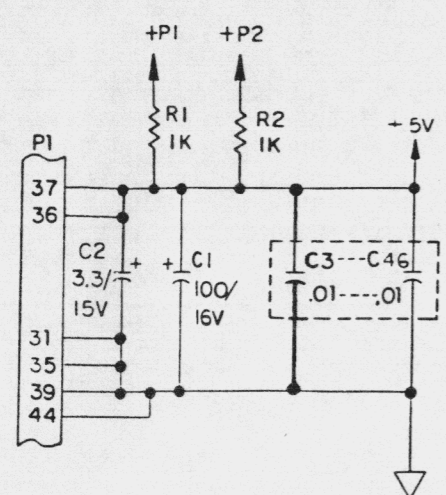
B

A

A

8 7 6 5 4 3 2 1

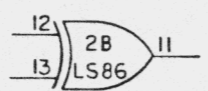
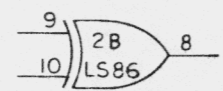
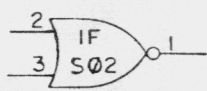
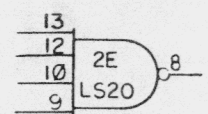
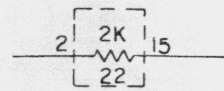




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74 S153	8	16
74LS157	8	16
74 S174	8	16
74 S175	8	16
74LS245	10	20
74LS373	10	20
4164	16	8 (REF)

POWER & SPARES

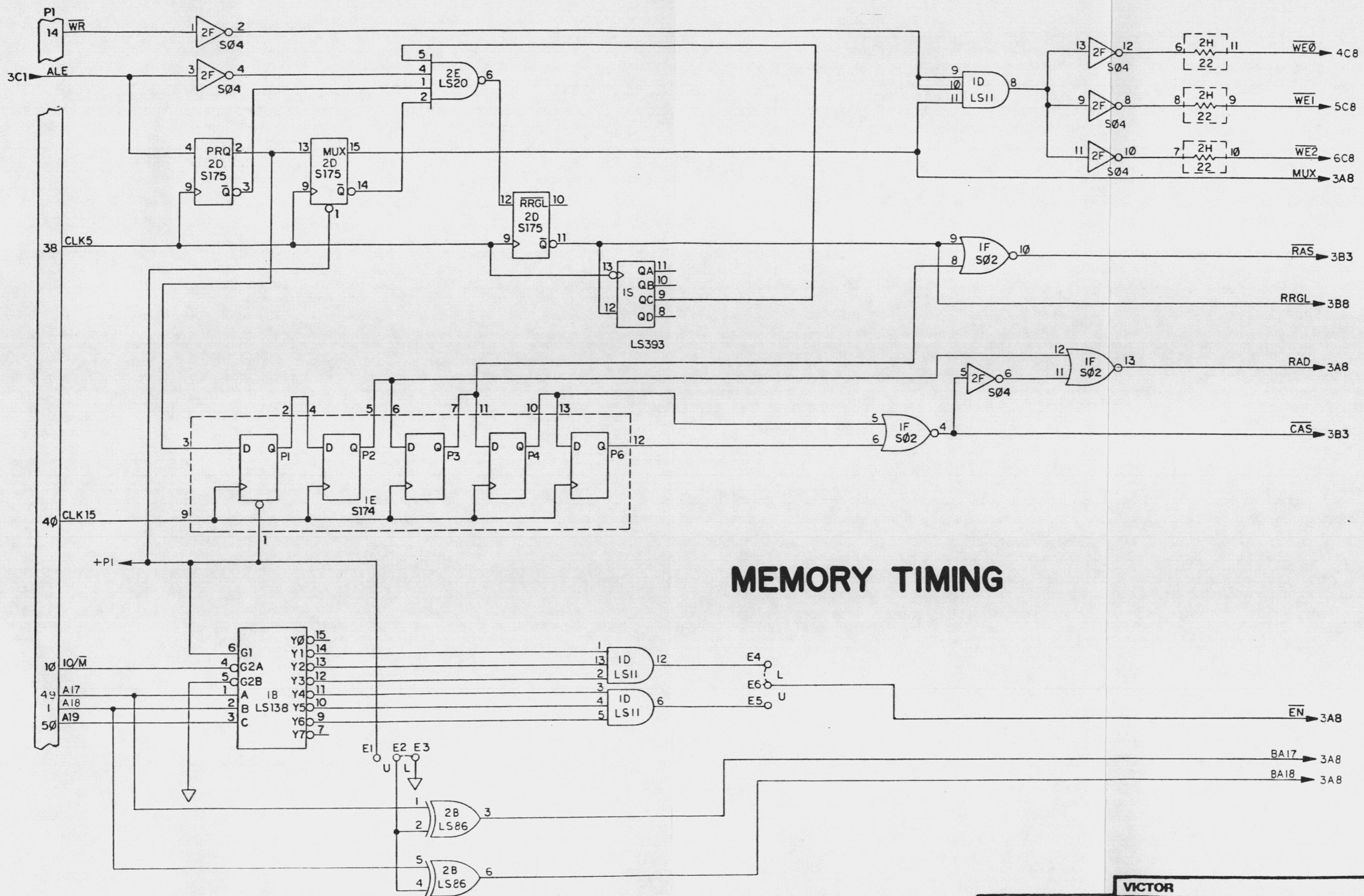


SPARE GATES

SHT. 1 OF 6 REV. A
DWG. NO. 10 10 71

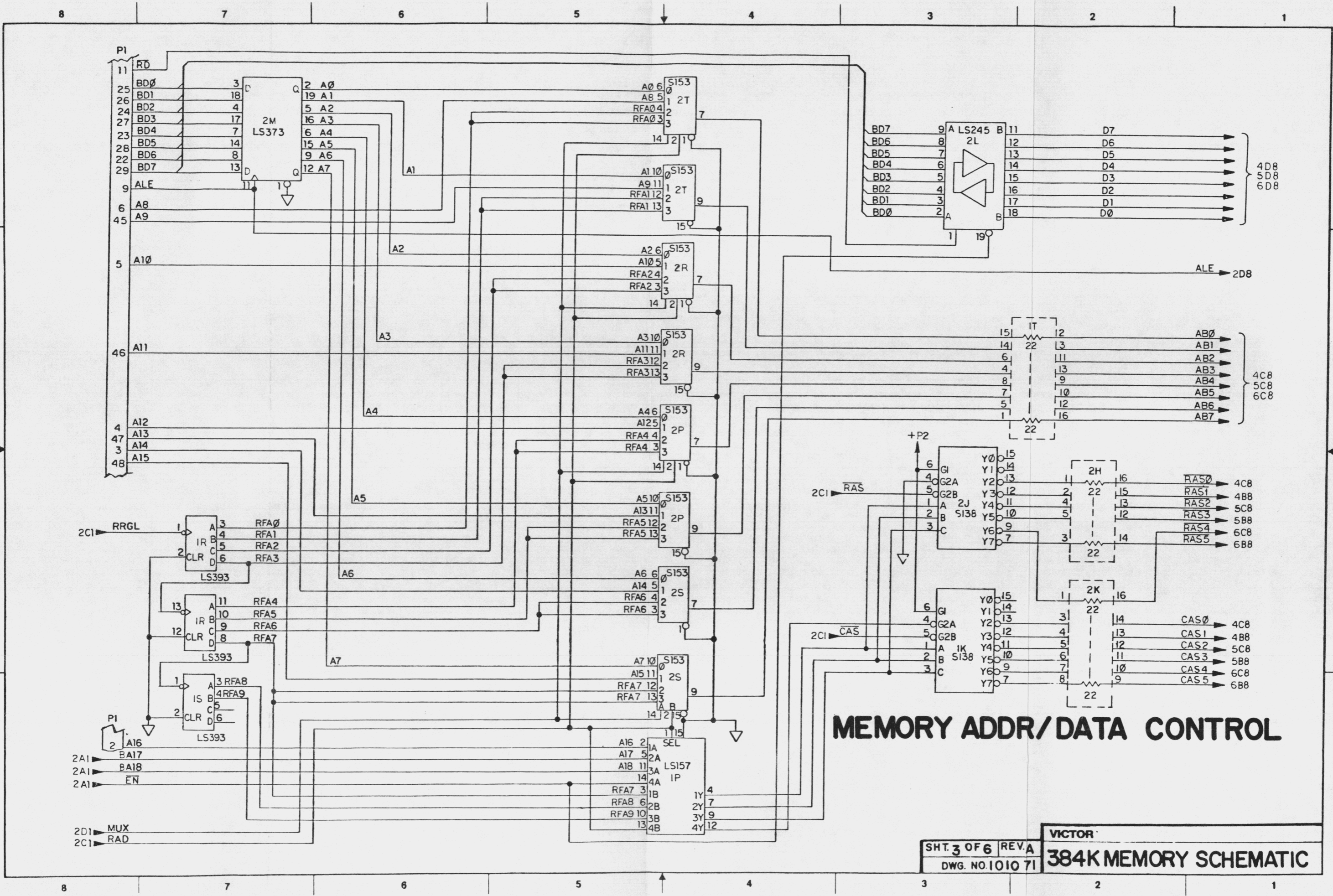
VICTOR
384K MEMORY SCHEMATIC

MEMORY TIMING

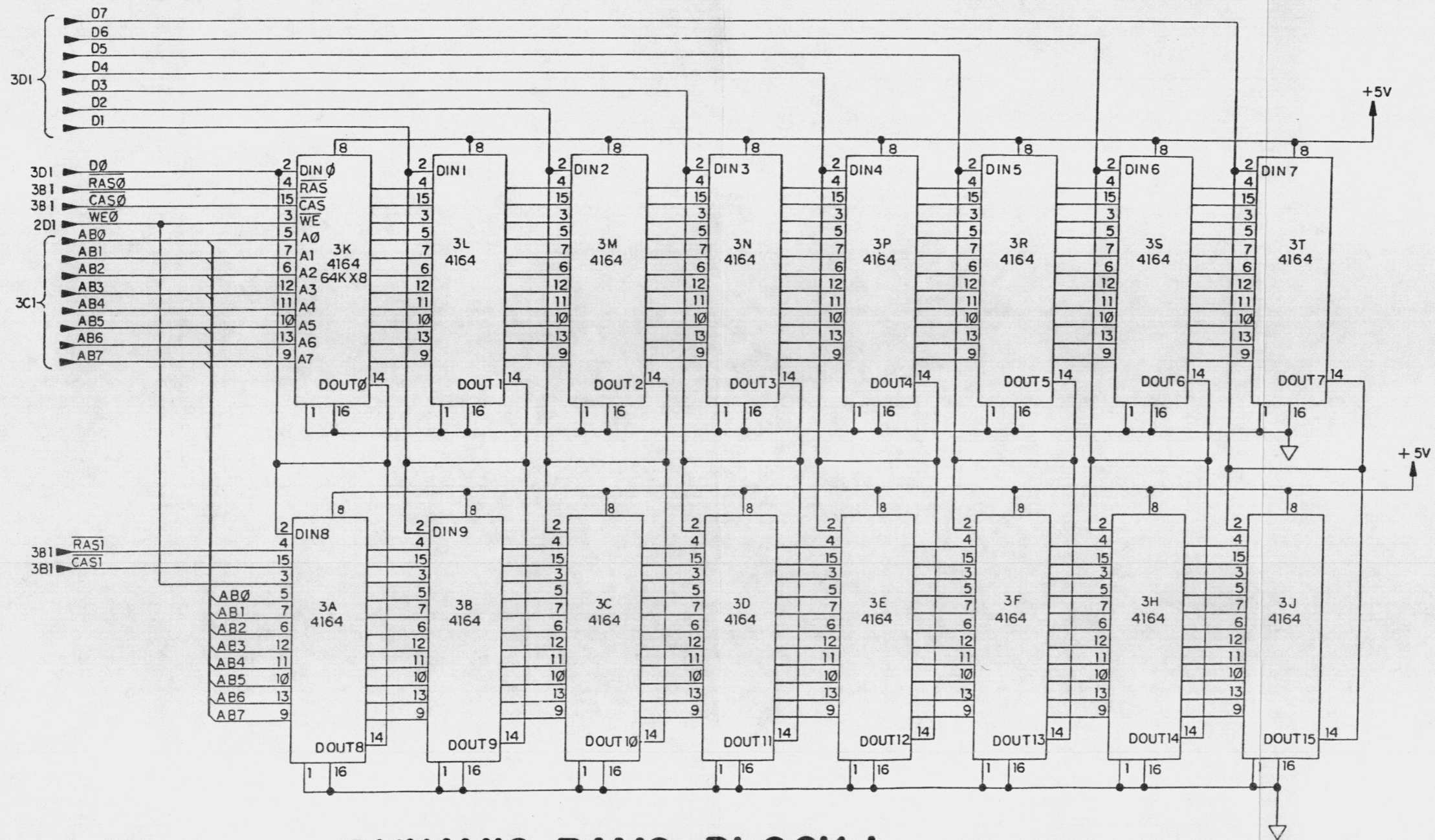


SHT. 2 OF 6 REV. A
DWG. NO. 10 10 71

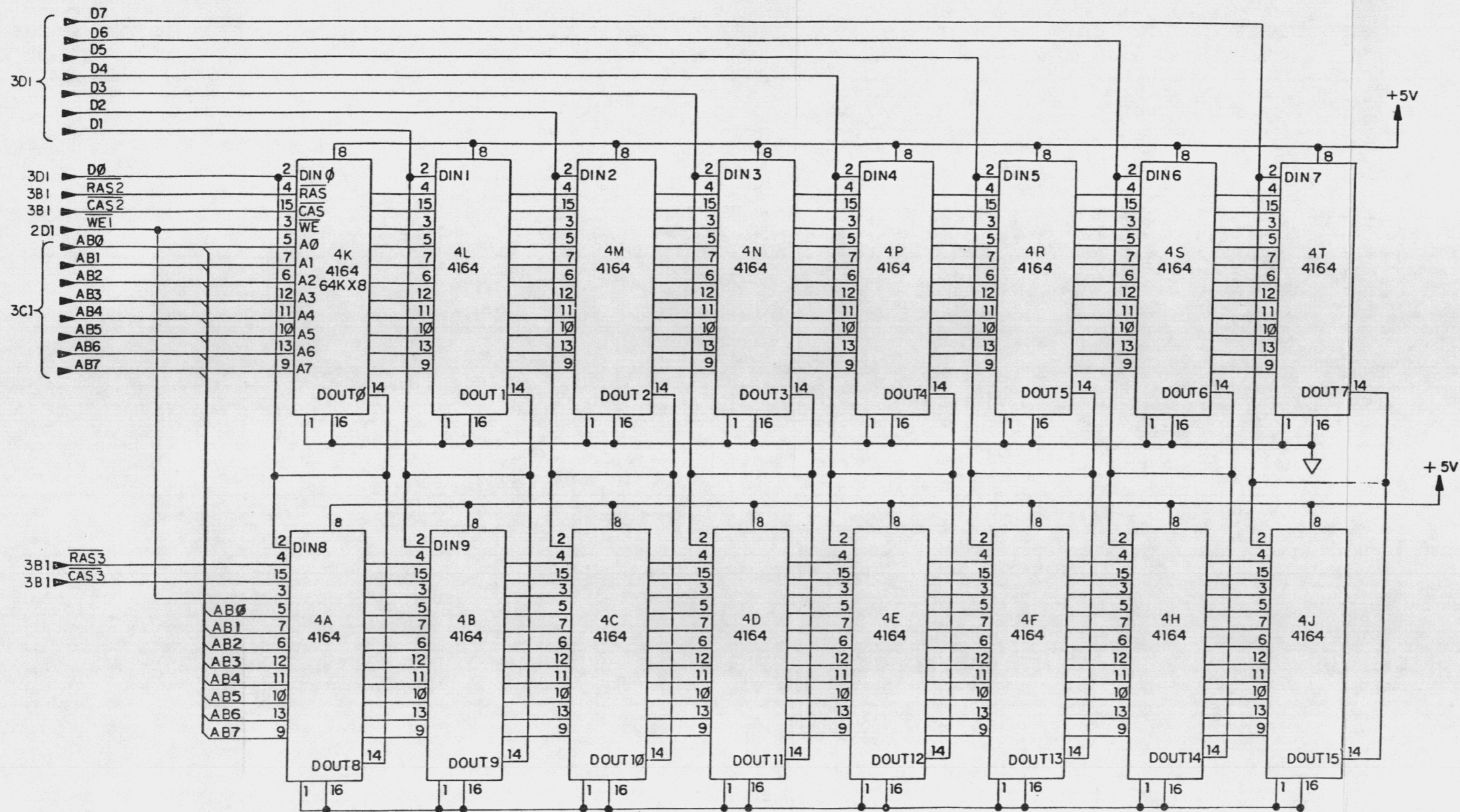
VICTOR
384K MEMORY SCHEMATIC



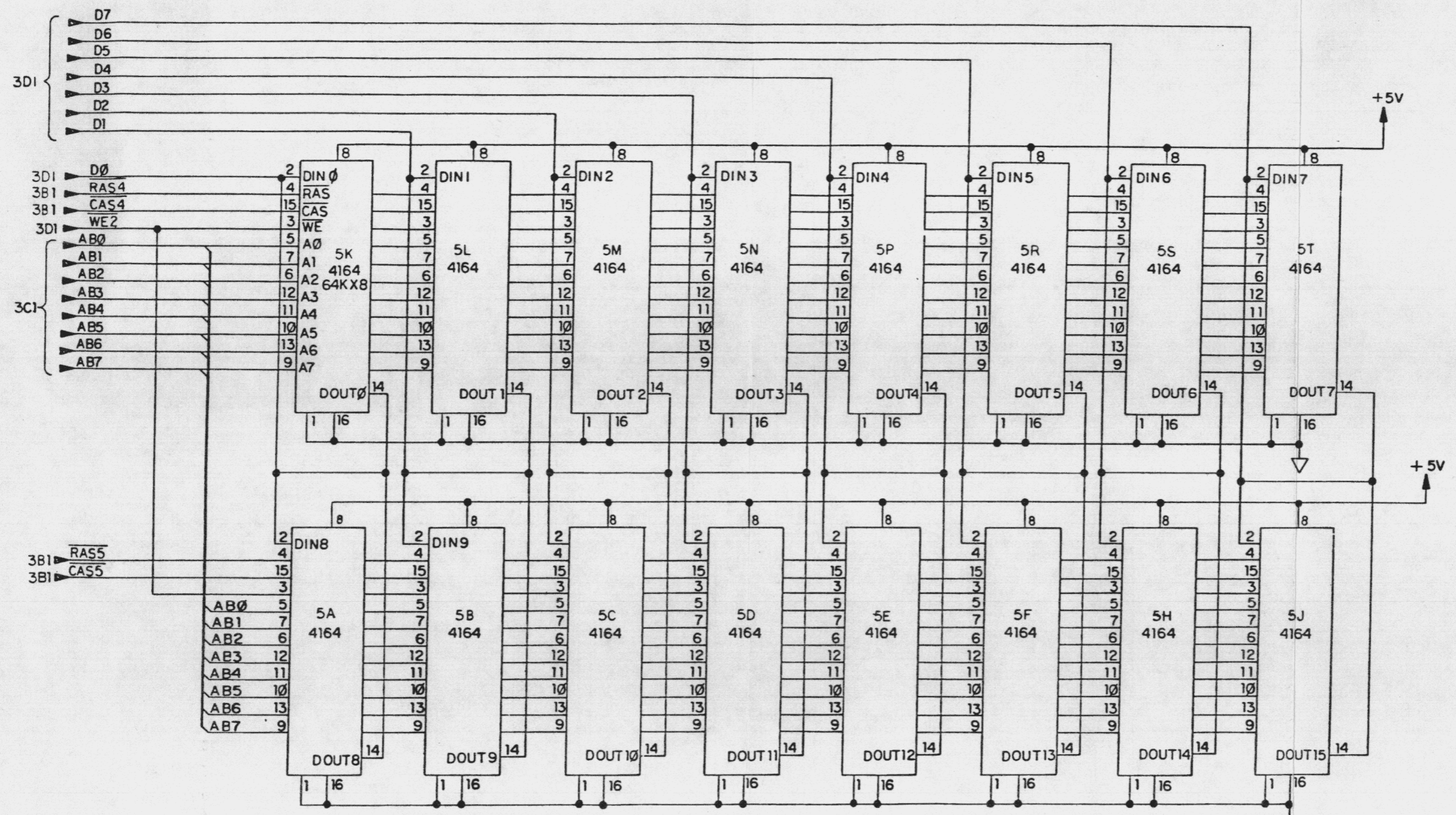
MEMORY ADDR/DATA CONTROL



DYNAMIC RAMS, BLOCK I



DYNAMIC RAMS, BLOCK 2



DYNAMIC RAMS, BLOCK 3