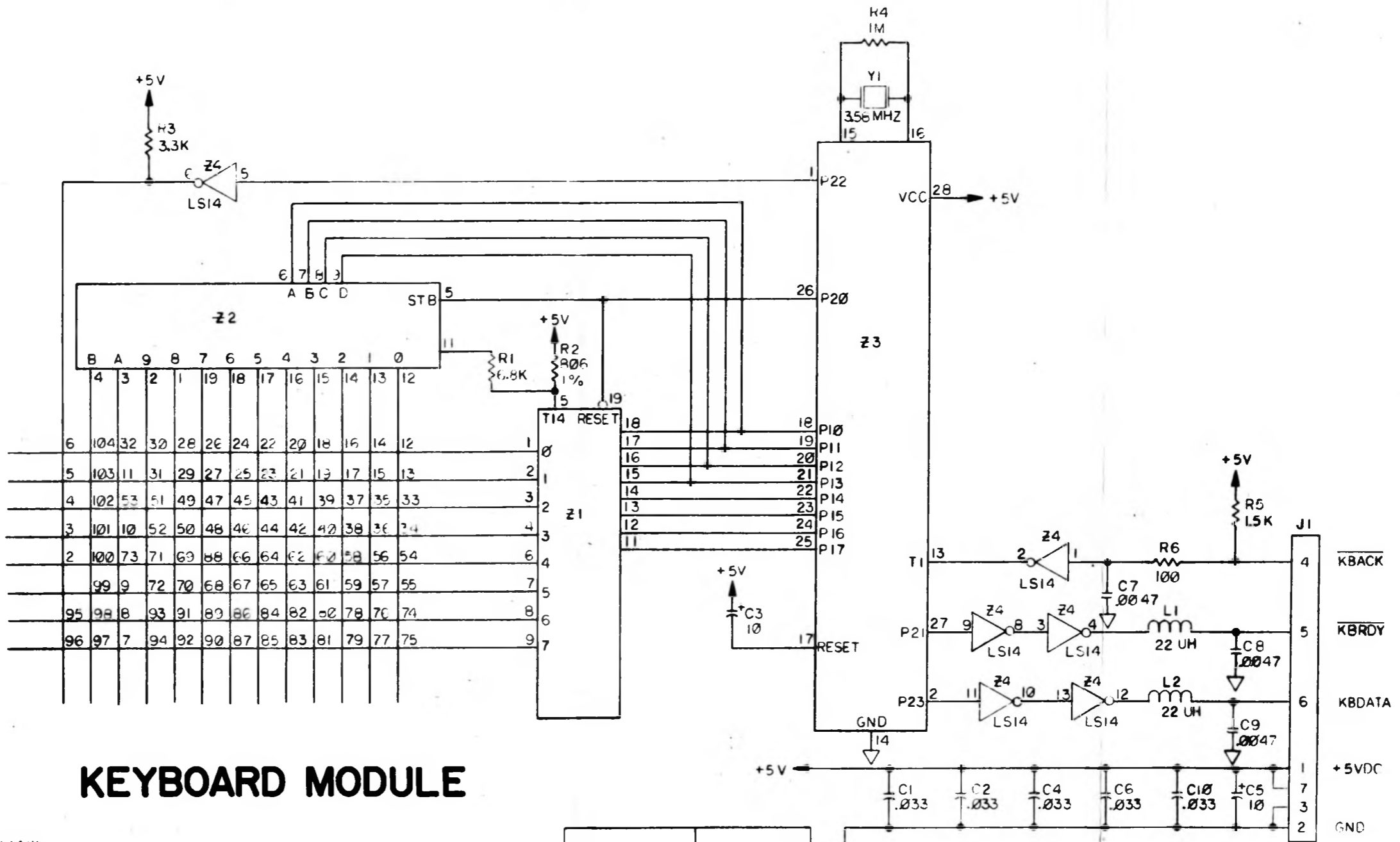


- 4 REF COMPOWER CORP., CP-5102 SCHEMATIC, DWG NO 90017.
- [3] CUT FOR 220V OPERATION
- 2. ALL RESISTORS ARE $\pm 5\%$, 1/4W.
- 1. ELECTRICAL VALUES ARE IN OHMS, MICROFARADS AND MICROHENRIES.

SHT. | OF | REV. P1
 DWG. NO. 100701

VICTOR BUSINESS PRODUCTS
 PWR. SUPPLY SCHEMATIC

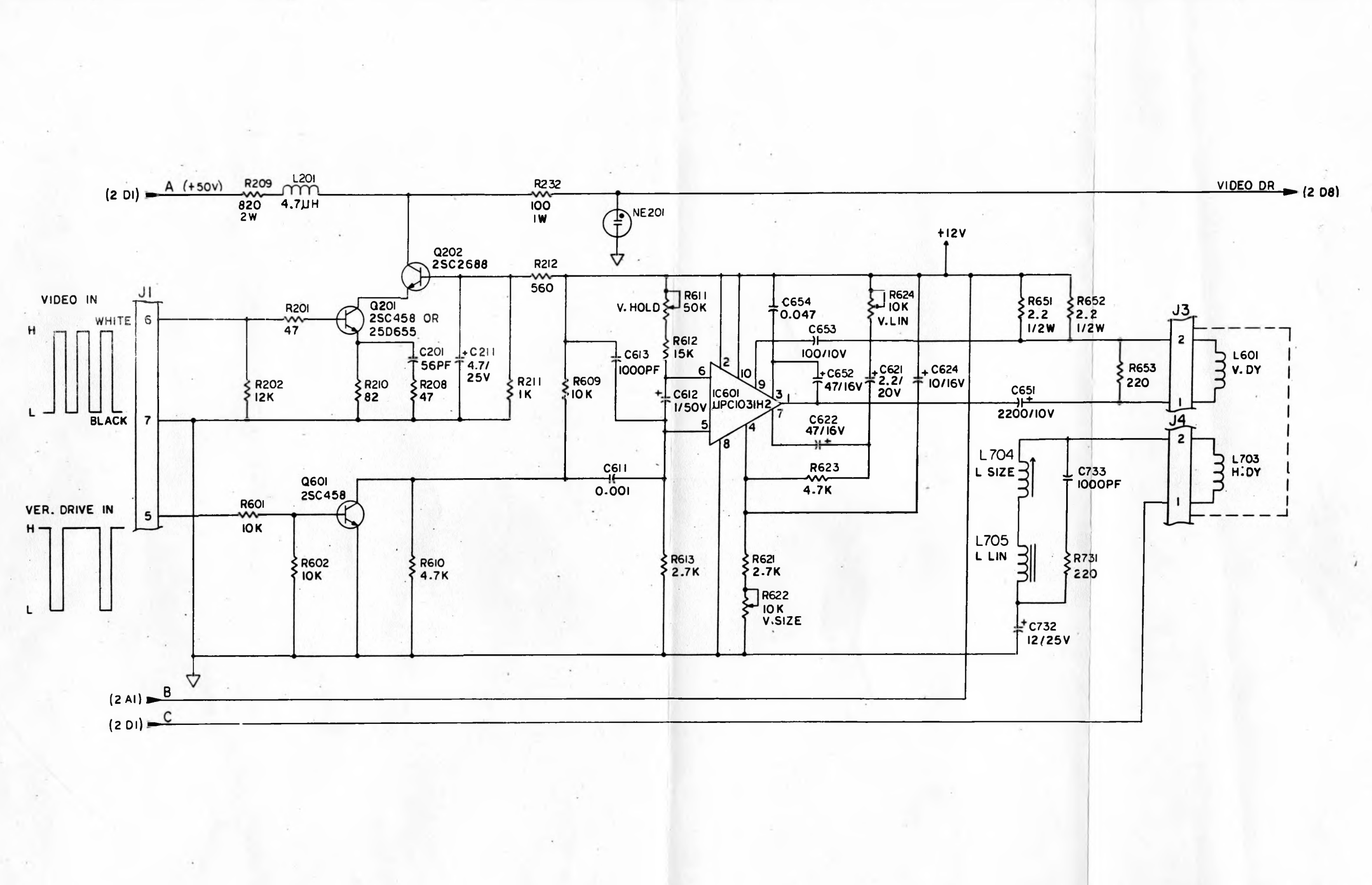


KEYBOARD MODULE

- 3. ALL RESISTORS ARE $\pm 5\%$, 1/4W
 - 2. ELECTRICAL VALES ARE IN OHMS, MICROFARADS & MICRCHENRIES
 - 1. MADE SCHEMATIC FROM KEY TRONIC CORPORATION, SP. KANE, WASH. PART NUMBER 35-02307-XXX.
- NOTE: UNLESS OTHERWISE SPECIFIED

Z4 - Y1 - J1	
R6 - C10 - L2	
LAST USED	NOT USED
REF. DES.	

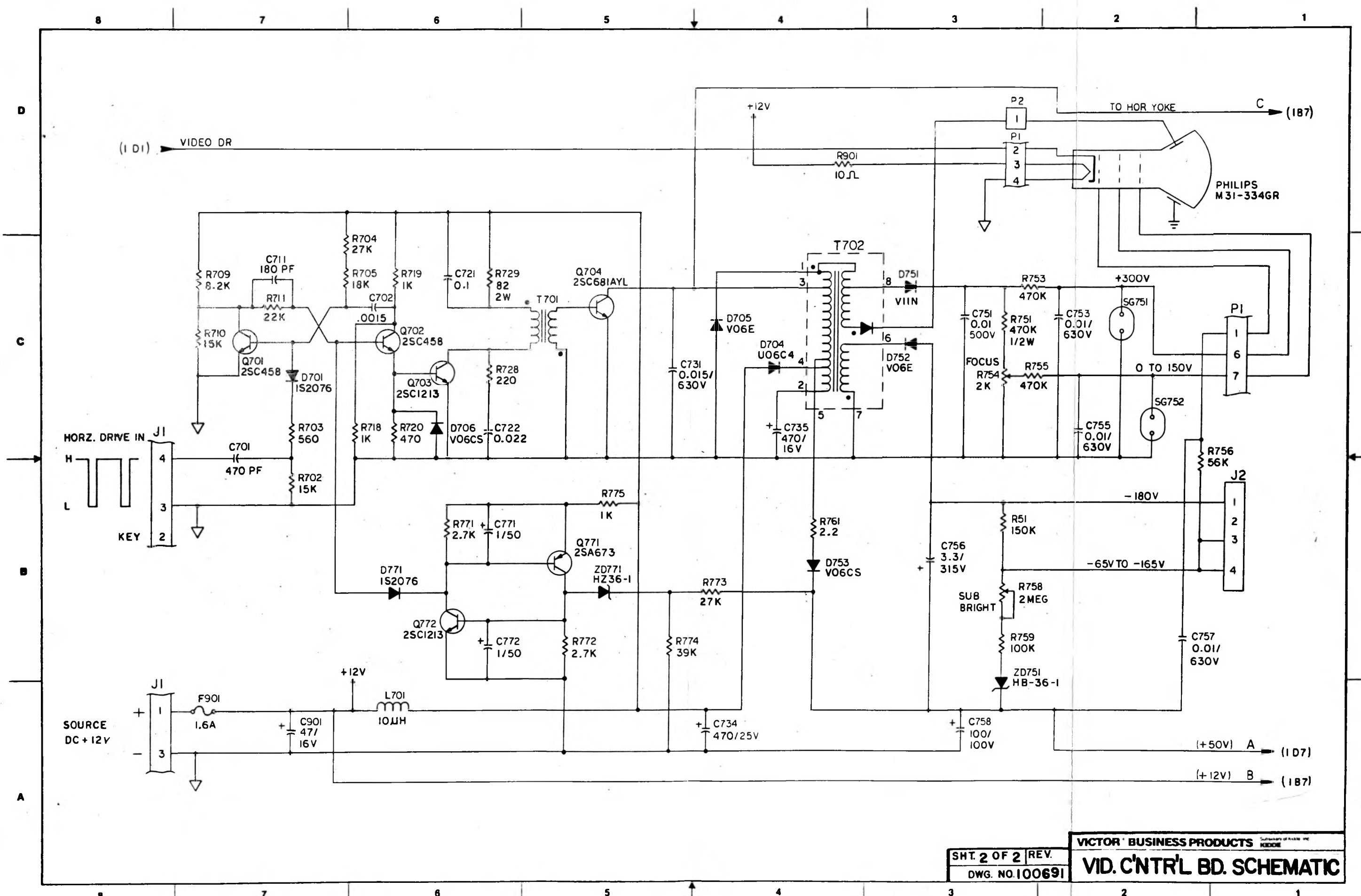
8 7 6 5 4 3 2 1

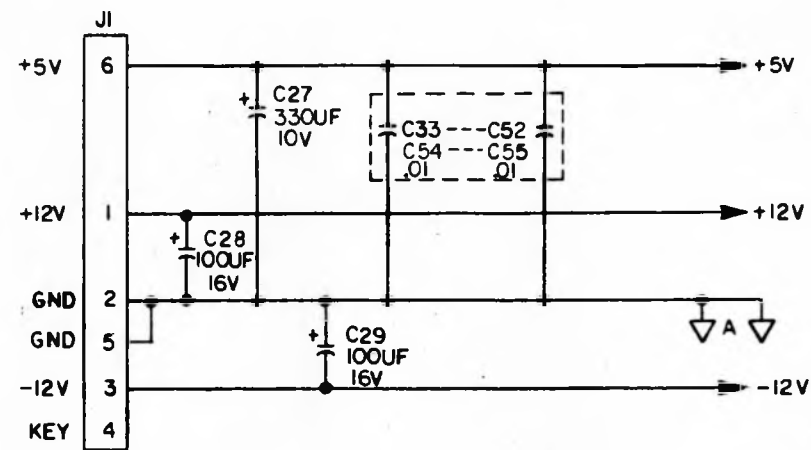


8 7 6 5 4 3 2 1

SHT. 1 OF 2 | REV
DWG. NO. 100691

VICTOR BUSINESS PRODUCTS
VID. C'NTR'L BD. SCHEMATIC





NOTES: UNLESS OTHERWISE SPECIFIED.

1. ELECTRICAL VALUES ARE IN OHMS, MICROFARADS AND MICROHENRIES.

2. ALL RESISTORS ARE $\pm 5\%$, 1/4 W.

3. F.S. IS FACTORY SELECT COMPONENTS.

4. Q1, Q2 ARE MOUNTED ON HEATSINK.

5. ALL INTEGRATED CIRCUITS ARE SN74 SERIES.

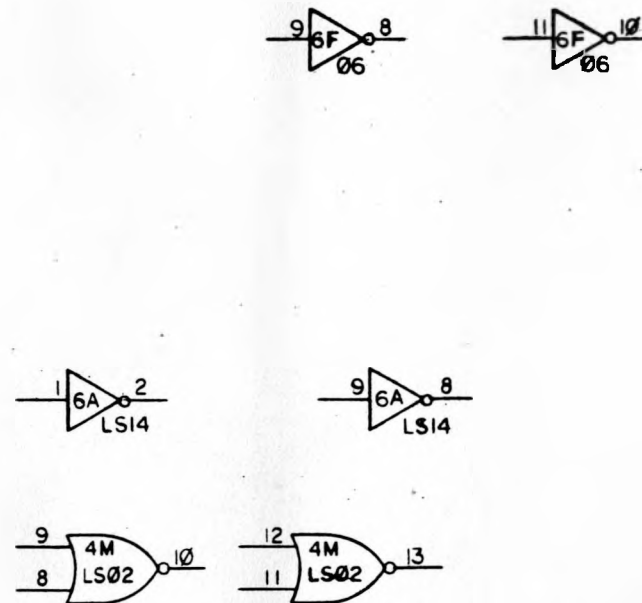
6. I.C. PINS ARE GND=7, +5V=14 EXCEPT FOR:

TYPE	GND	+5V
74LS123	8	16
74LS133	8	16
74LS139	8	16
74LS157	8	16
74LS165	8	16
74LS190	8	16
74LS191	8	16
74LS373	10	20
2316	12	24
75462	4	8

7. ALL DIODE ARE 1N4148.

8. SEE TABULATION TABLE THIS PAGE.

POWER & SPARES

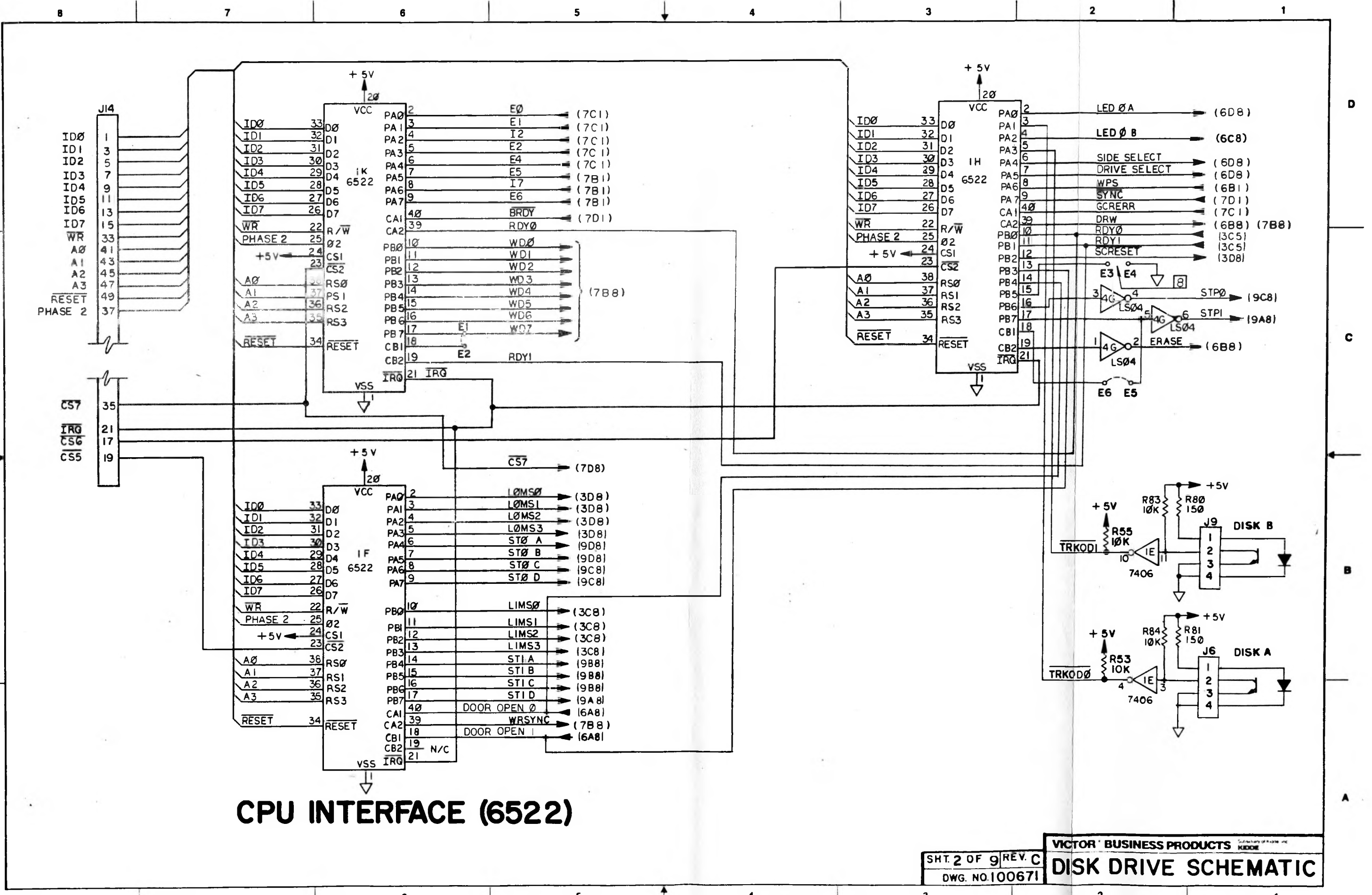


SPARE GATES

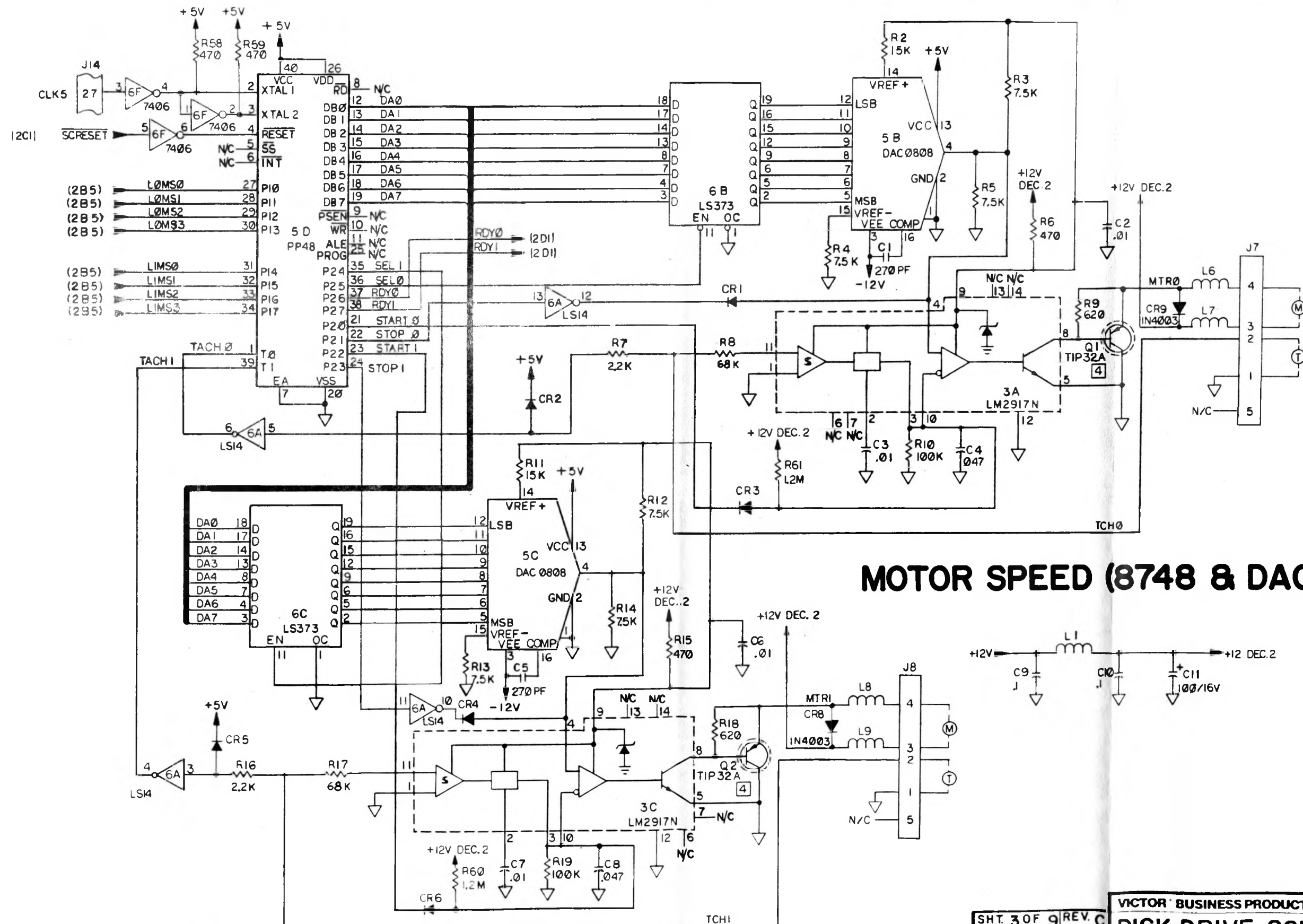
SHEET	DESCRIPTION
1	POWER & SPARES
2	CPU INTERFACE (6522)
3	MOTOR SPEED (8748 & DAC)
4	PLL
5	RD/WR HEAD INTERFACE
6	DRIVE SELECT, LED, DECODE
7	GCR EN/DE-CODER
8	DISK CONNECTORS (REF)
9	STEPPER CONTROL

SHT. 1 OF 9 REV. C
DWG. NO. 100671

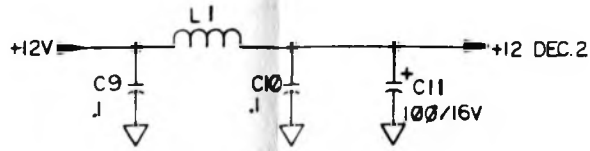
VICTOR BUSINESS PRODUCTS
DISK DRIVE SCHEMATIC

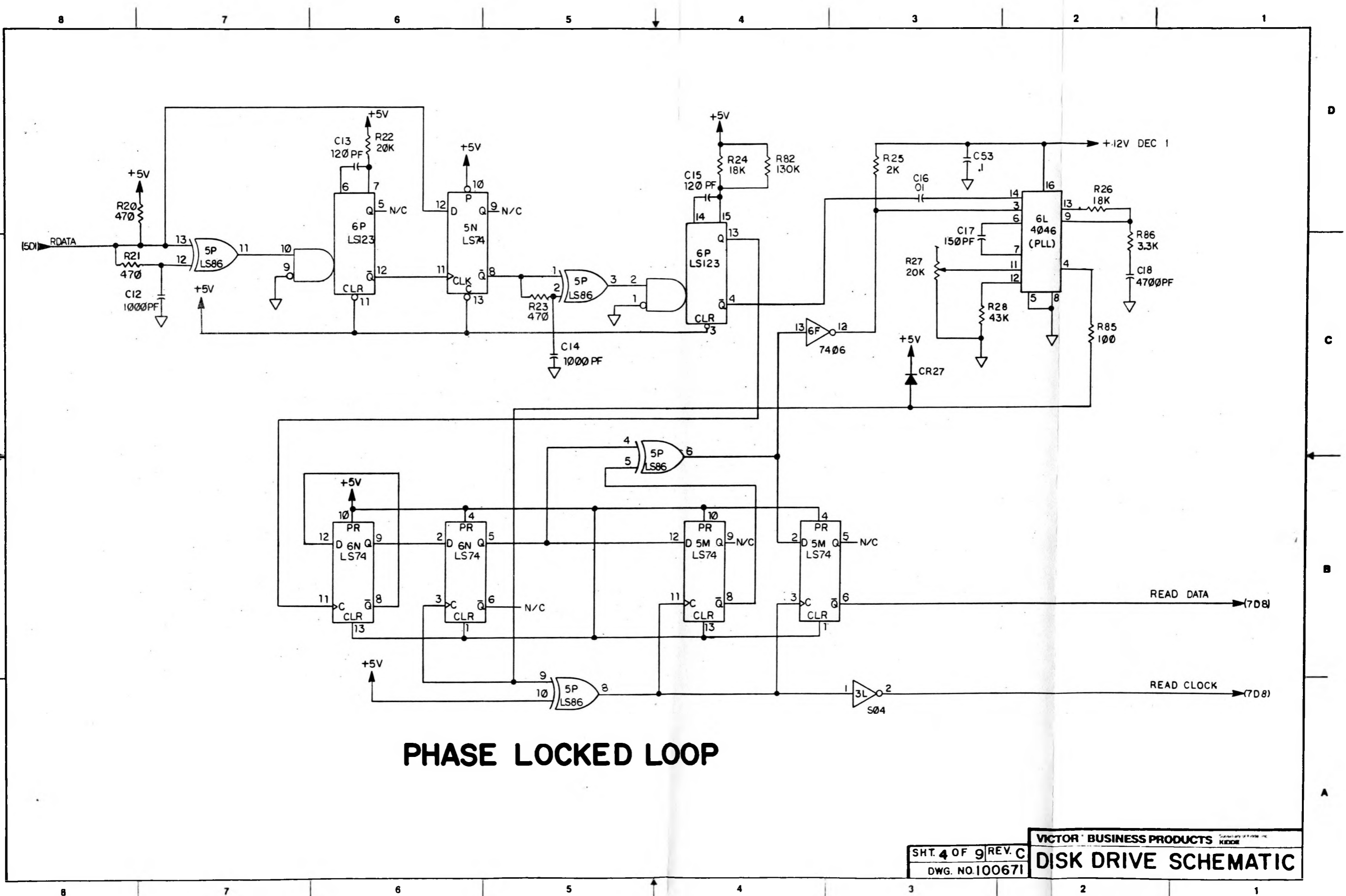


CPU INTERFACE (6522)



MOTOR SPEED (8748 & DAC)

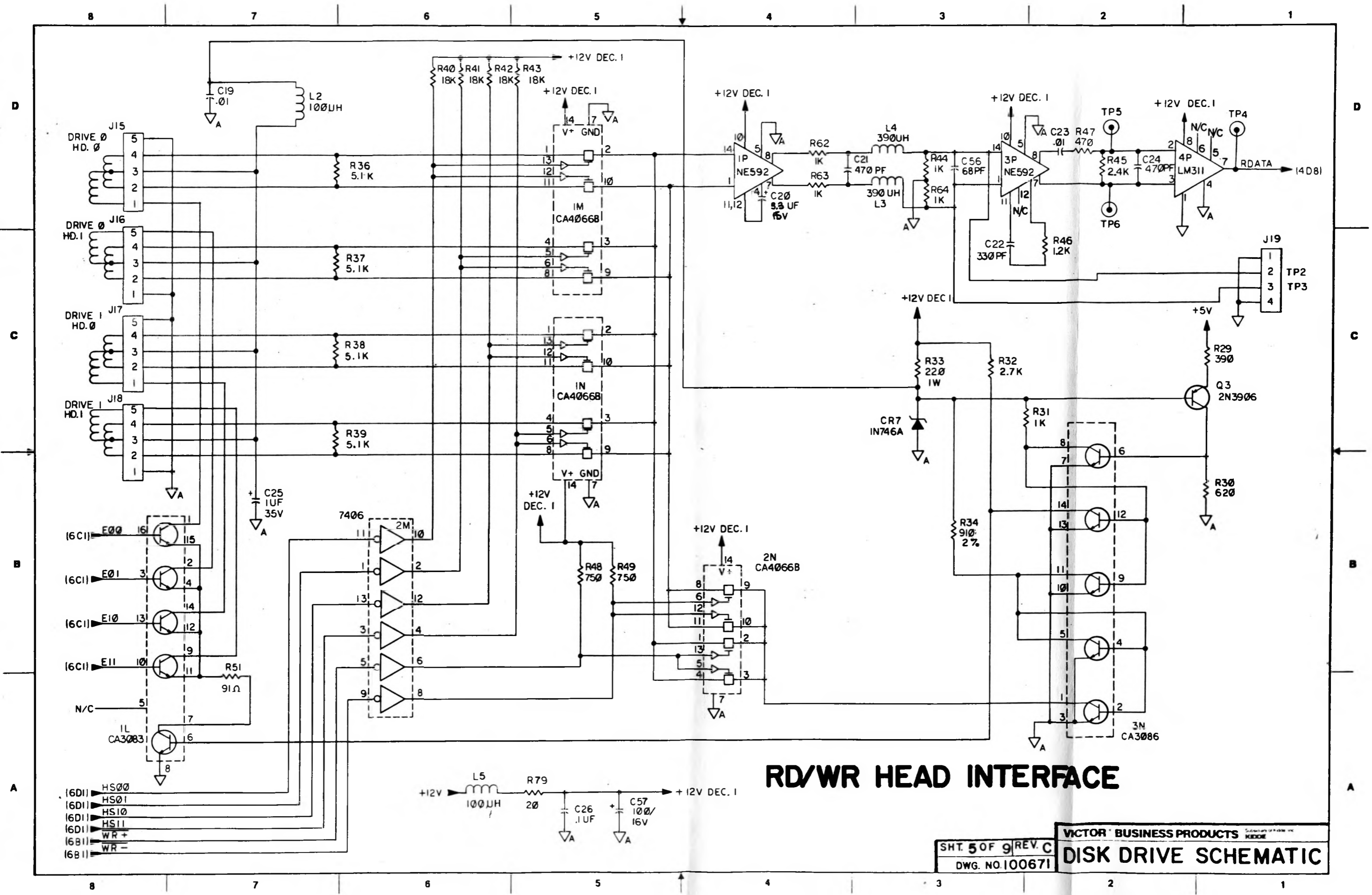




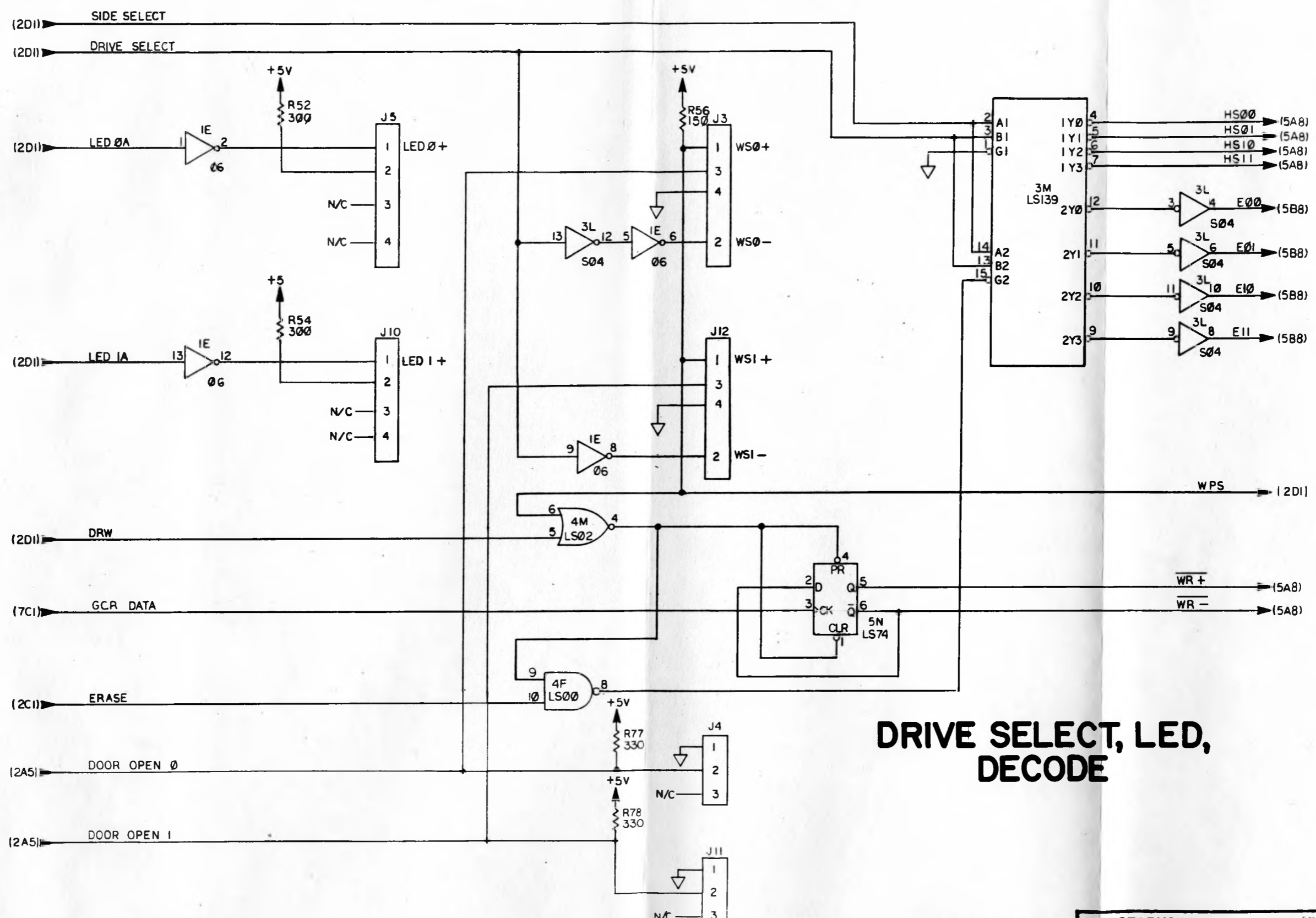
PHASE LOCKED LOOP

SHT. 4 OF 9 REV. C
DWG. NO. 100671

VICTOR BUSINESS PRODUCTS
DISK DRIVE SCHEMATIC



RD/WR HEAD INTERFACE



DRIVE SELECT, LED, DECODE

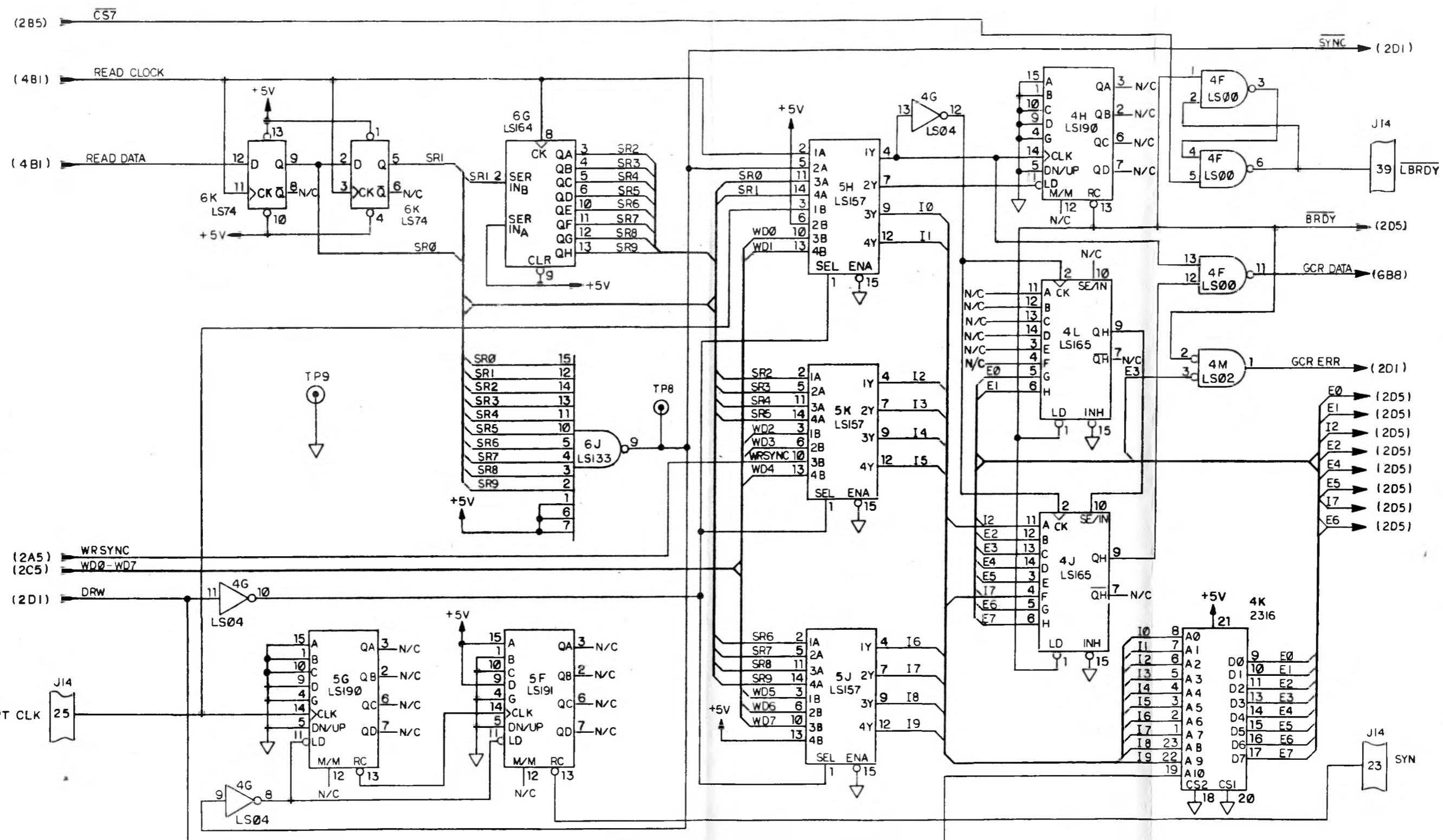
B 7 6 5 4 3 2 1

D

C

B

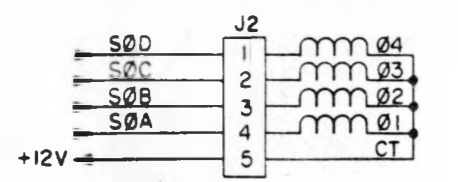
A



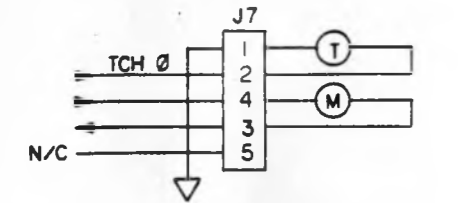
GCR EN/DE-CODER

8 7 6 5 4 3 2 1

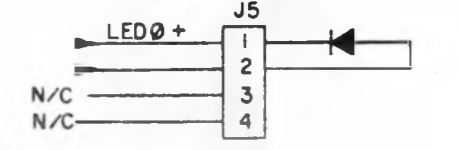
8 7 6 5 4 3 2 1



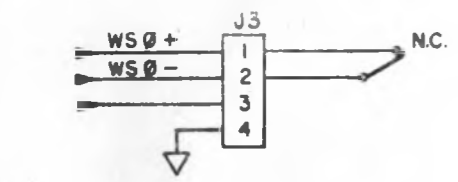
STEPPER A
(SHT 9)



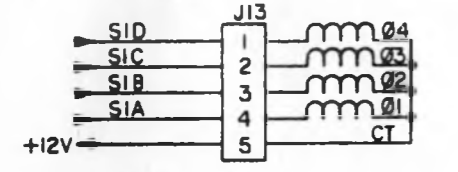
MOTOR A (8748, DAC, DISCRETE)
(SHT 3)



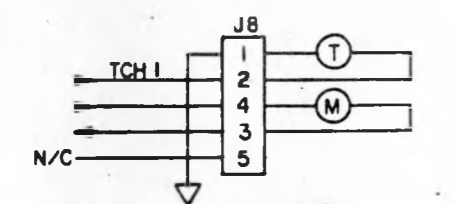
ACTIVITY LED A
(SHT 6)



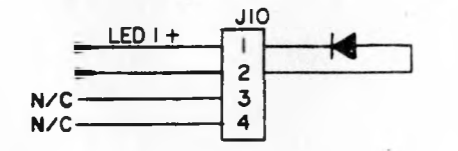
WRITE PROTECT A
(SHT 6)



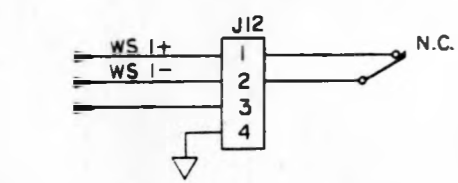
STEPPER B
(SHT 9)



MOTOR B
(SHT 3)

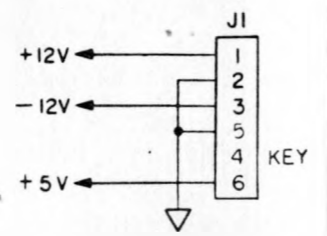
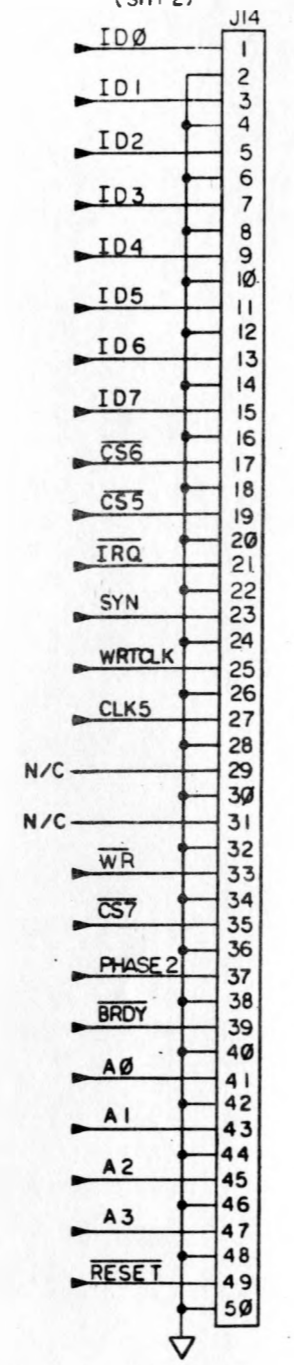


ACTIVITY LED B
(SHT 6)



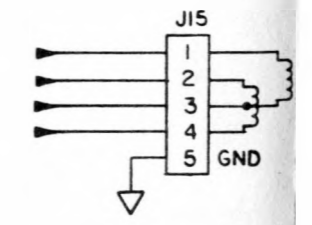
WRITE PROTECT B
(SHT 6)

CPU INTERFACE (6522)
(SHT 2)

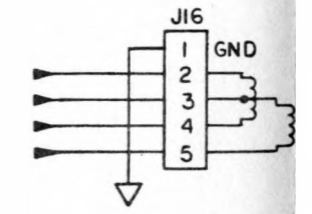


POWER CONNECTOR
(SHT 1)

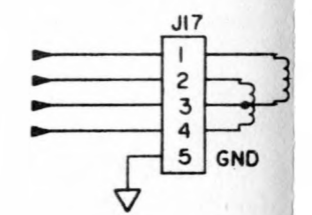
DRIVE A HEAD 0
(SHT 5)



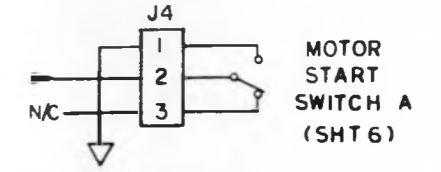
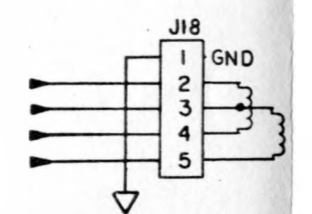
DRIVE A HEAD 1
(SHT 5)



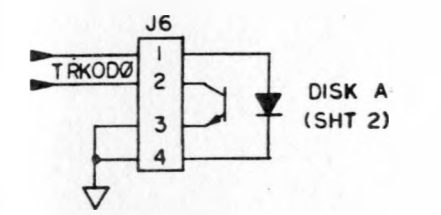
DRIVE B HEAD 0
(SHT 5)



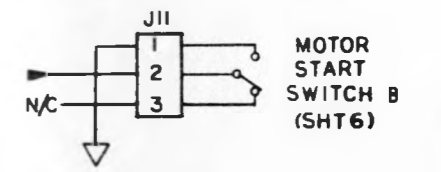
DRIVE B HEAD 1
(SHT 5)



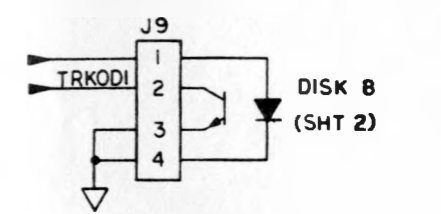
MOTOR START SWITCH A
(SHT 6)



DISK A
(SHT 2)



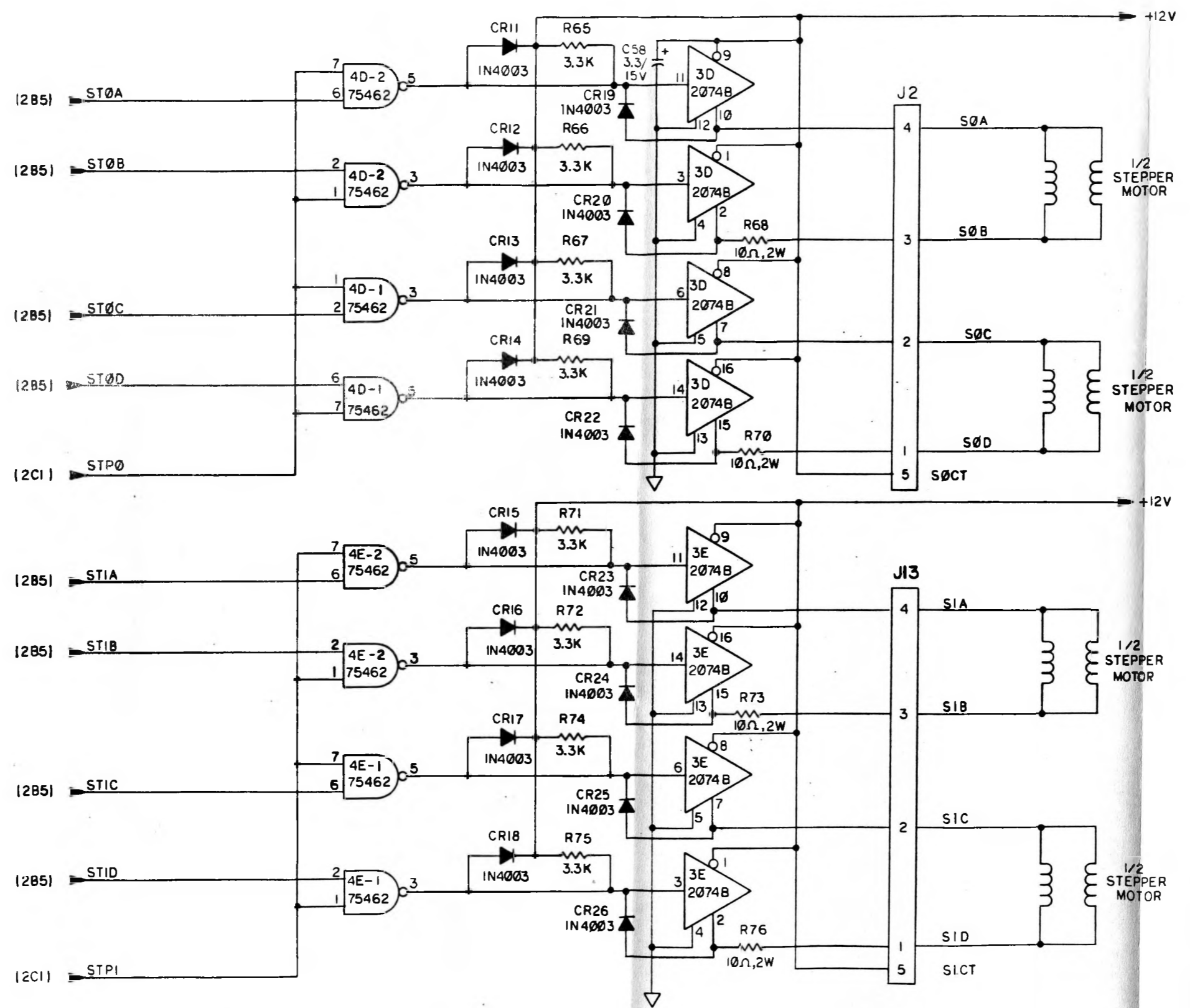
MOTOR START SWITCH B
(SHT 6)



DISK B
(SHT 2)

DISK CONNECTORS (REF)

8 7 6 5 4 3 2 1

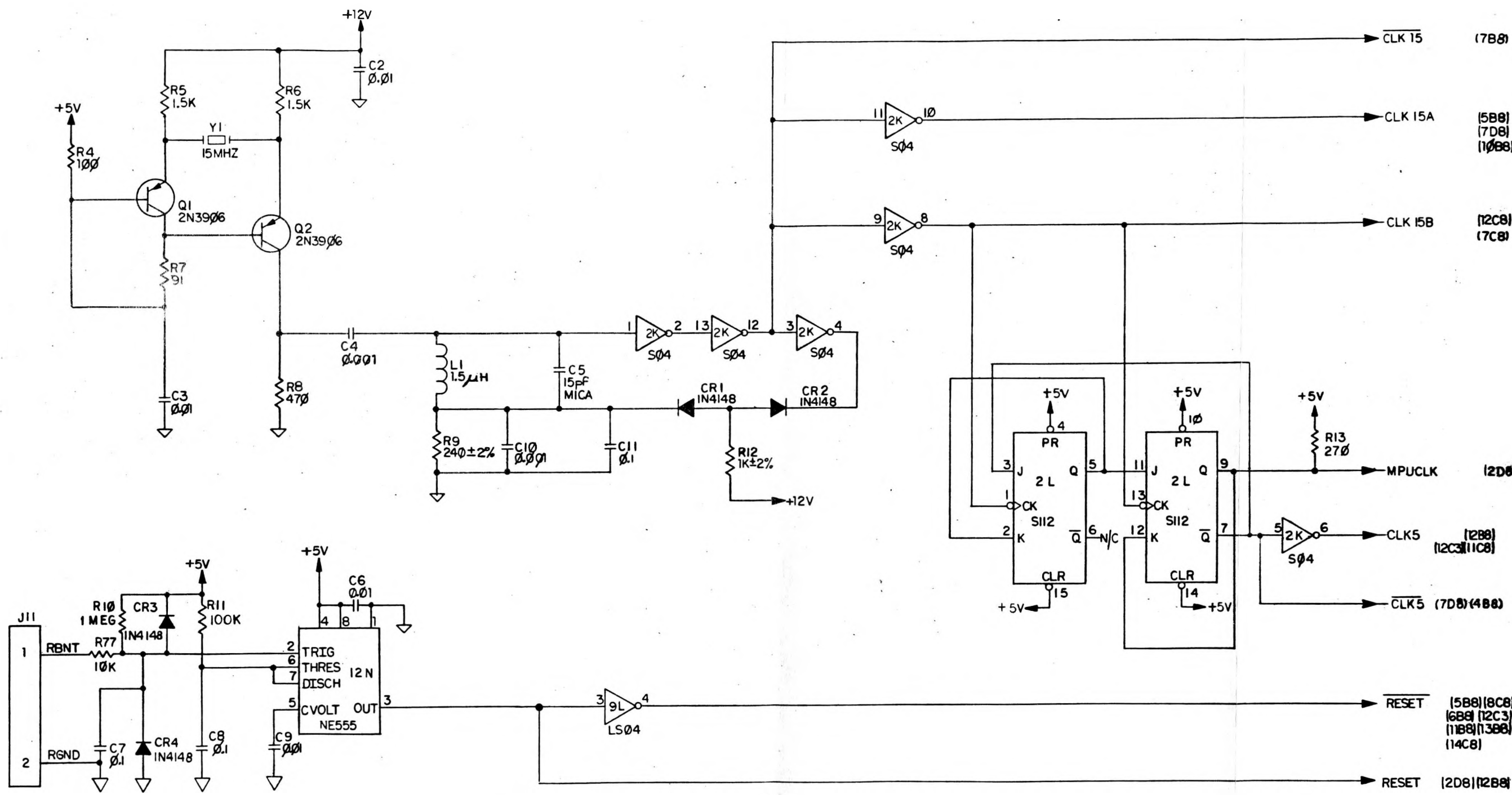


STEPPER CONTROL

SHT. 9 OF 9 REV C
DWG. NO. 100671

VICTOR BUSINESS PRODUCTS
DISK DRIVE SCHEMATIC

8 7 6 5 4 3 2 1



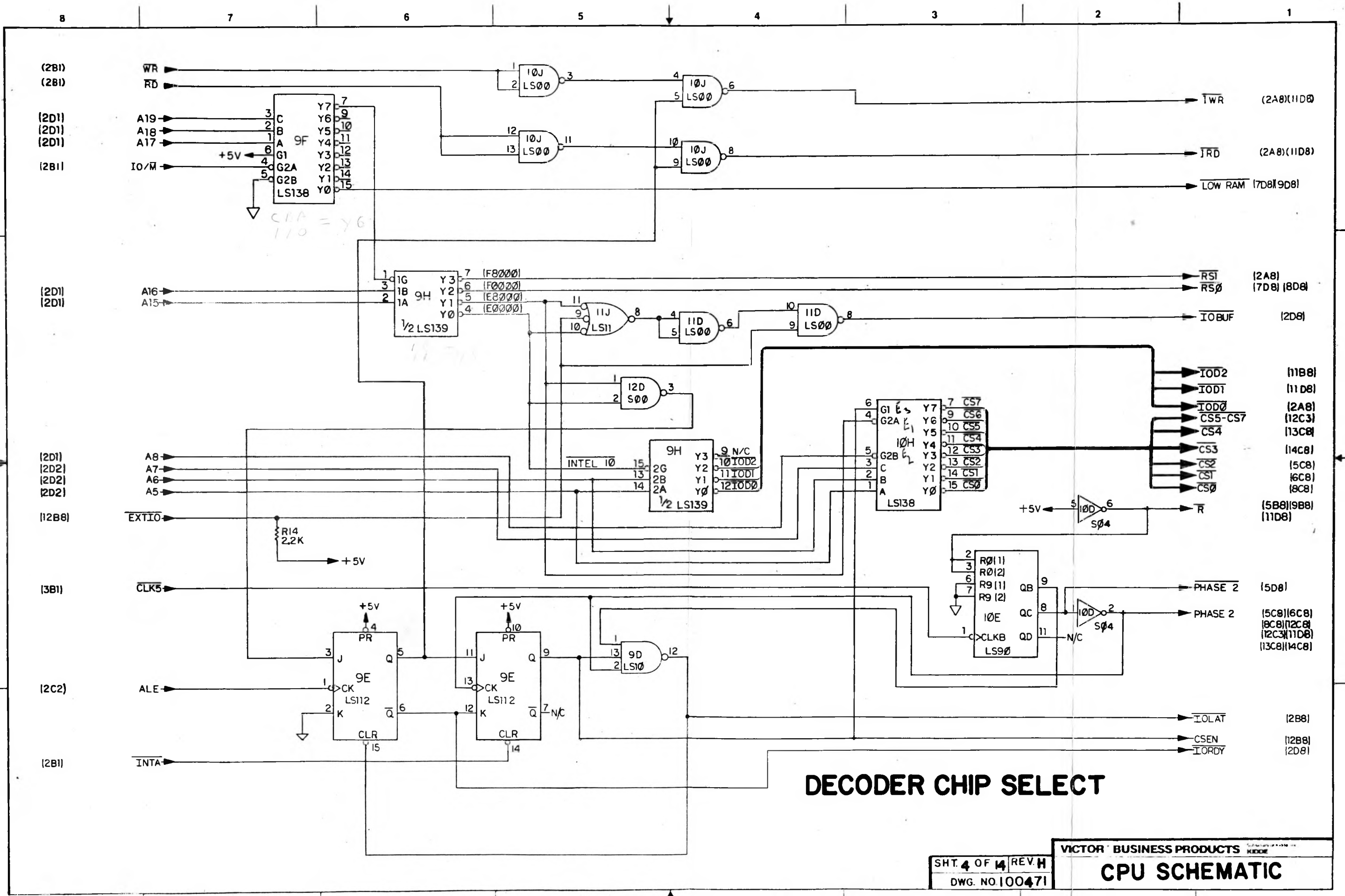
MASTER CLOCK

SHT. 3 OF 14 REV H
DWG. NO. 100471

VICTOR BUSINESS PRODUCTS
CPU SCHEMATIC

8 7 6 5 4 3 2 1

4

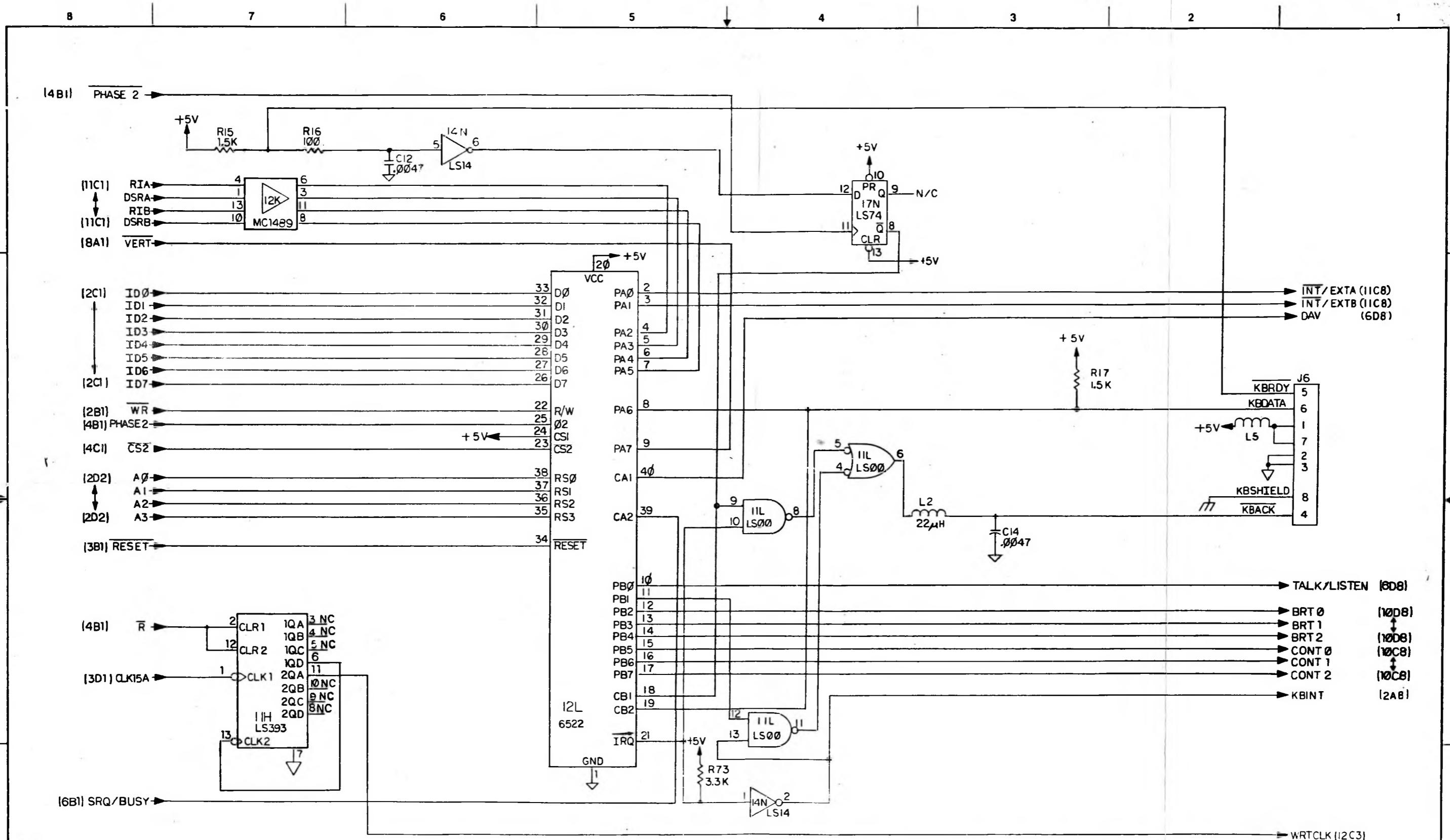


DECODER CHIP SELECT

SHT. 4 OF 14 REV. H
 DWG. NO. 100471

VICTOR BUSINESS PRODUCTS
 CPU SCHEMATIC

5

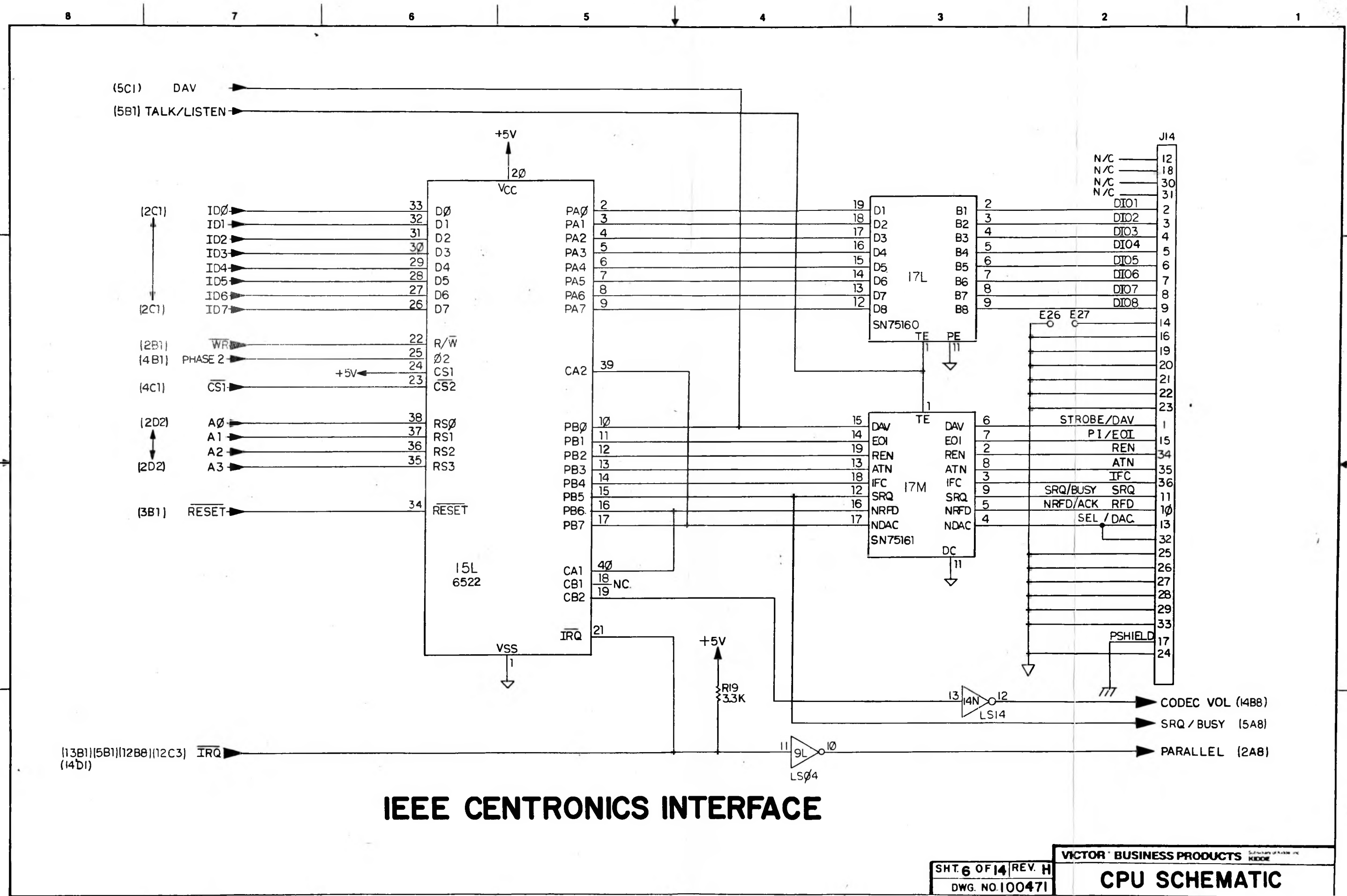


KEYBOARD INTERFACE

SHT. 5 OF 14 REV. H
DWG. NO. 100471

VICTOR BUSINESS PRODUCTS
CPU SCHEMATIC

6

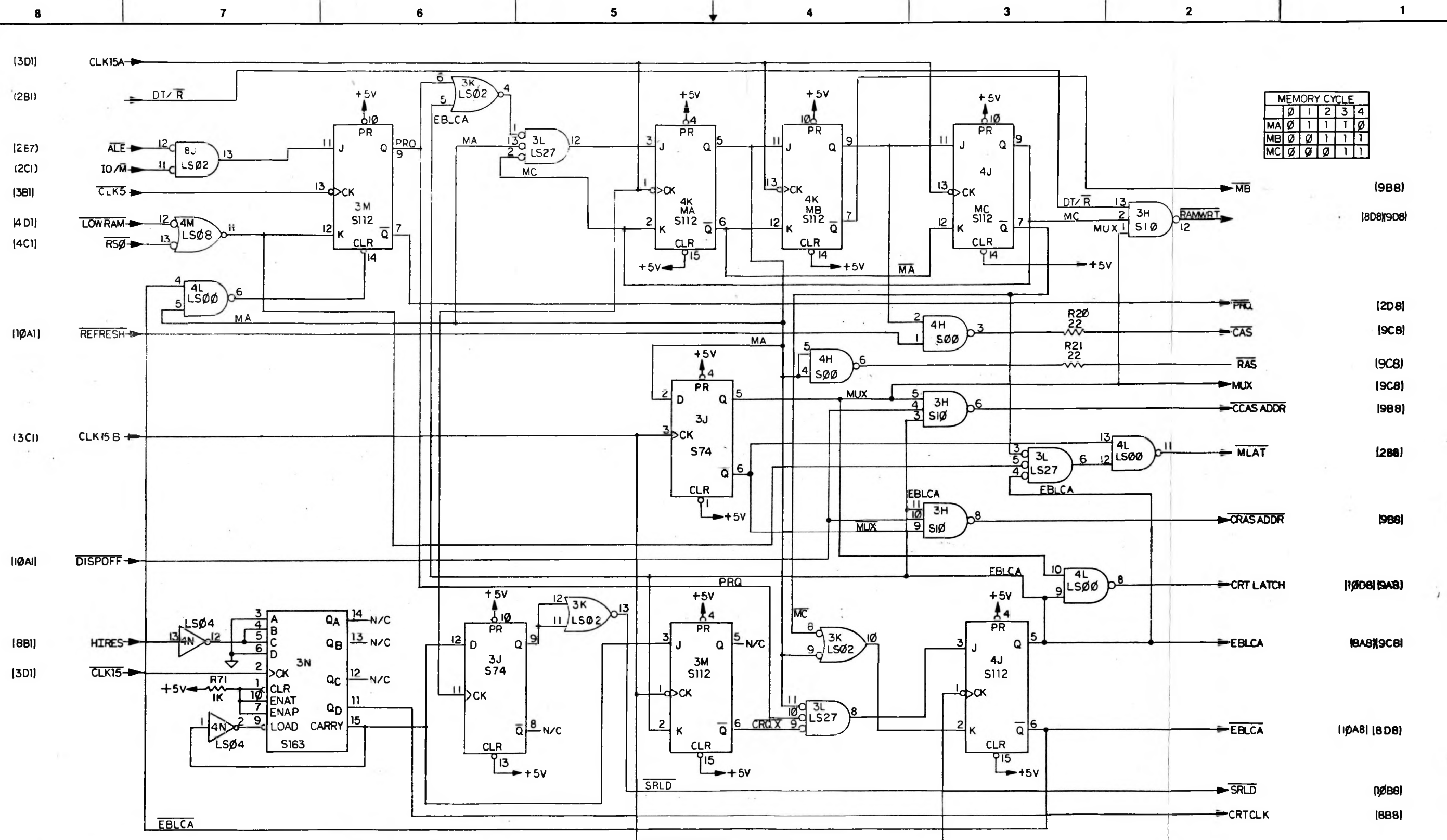


IEEE CENTRONICS INTERFACE

SHT. 6 OF 14 REV. H
 DWG. NO. 100471

VICTOR BUSINESS PRODUCTS
 CPU SCHEMATIC

7



MEMORY CYCLE					
	0	1	2	3	4
MA	0	1	1	1	0
MB	0	0	1	1	1
MC	0	0	0	1	1

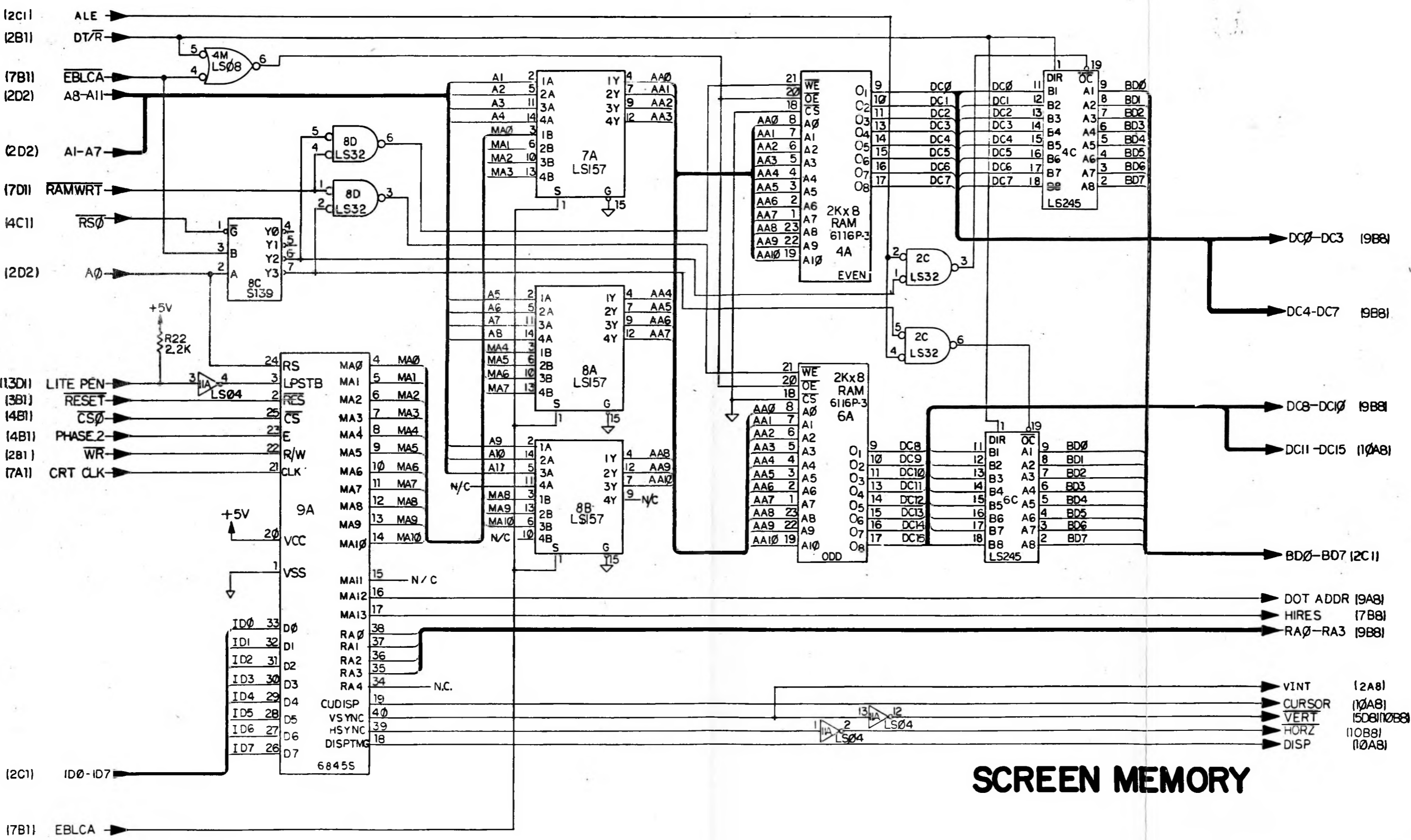
CRT CYCLE HIRES										
	3	4	5	6	7	8	9	0	1	2
CA	0	1	0	1	0	1	0	1	0	1
CB	0	0	1	1	0	0	1	1	1	1
CC	0	0	0	0	1	1	1	1	1	1
CD	1	1	1	1	1	1	1	1	1	0

CRT CYCLE HIRES																
	9	10	11	12	13	14	15	0	1	2	3	4	5	6	7	8
CA	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
CB	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
CC	0	0	0	0	1	1	1	1	0	0	0	0	0	1	1	1
CD	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0

CONTROL SIGNALS

SHT. 7 OF 14 REV. H
DWG. NO. 100471

VICTOR BUSINESS PRODUCTS
CPU SCHEMATIC



SCREEN MEMORY

SHT. 8 OF 14 REV. H
 DWG. NO. 100471

VICTOR BUSINESS PRODUCTS
 CPU SCHEMATIC

(7B1) EBLCA

(2C1) ID0-ID7

(7A1) CRT CLK

(2B1) WR

(4B1) PHASE 2

(4B1) CS

(3B1) RESET

(13D1) LITE PEN

(2D2) A0

(17D1) RAMWRT

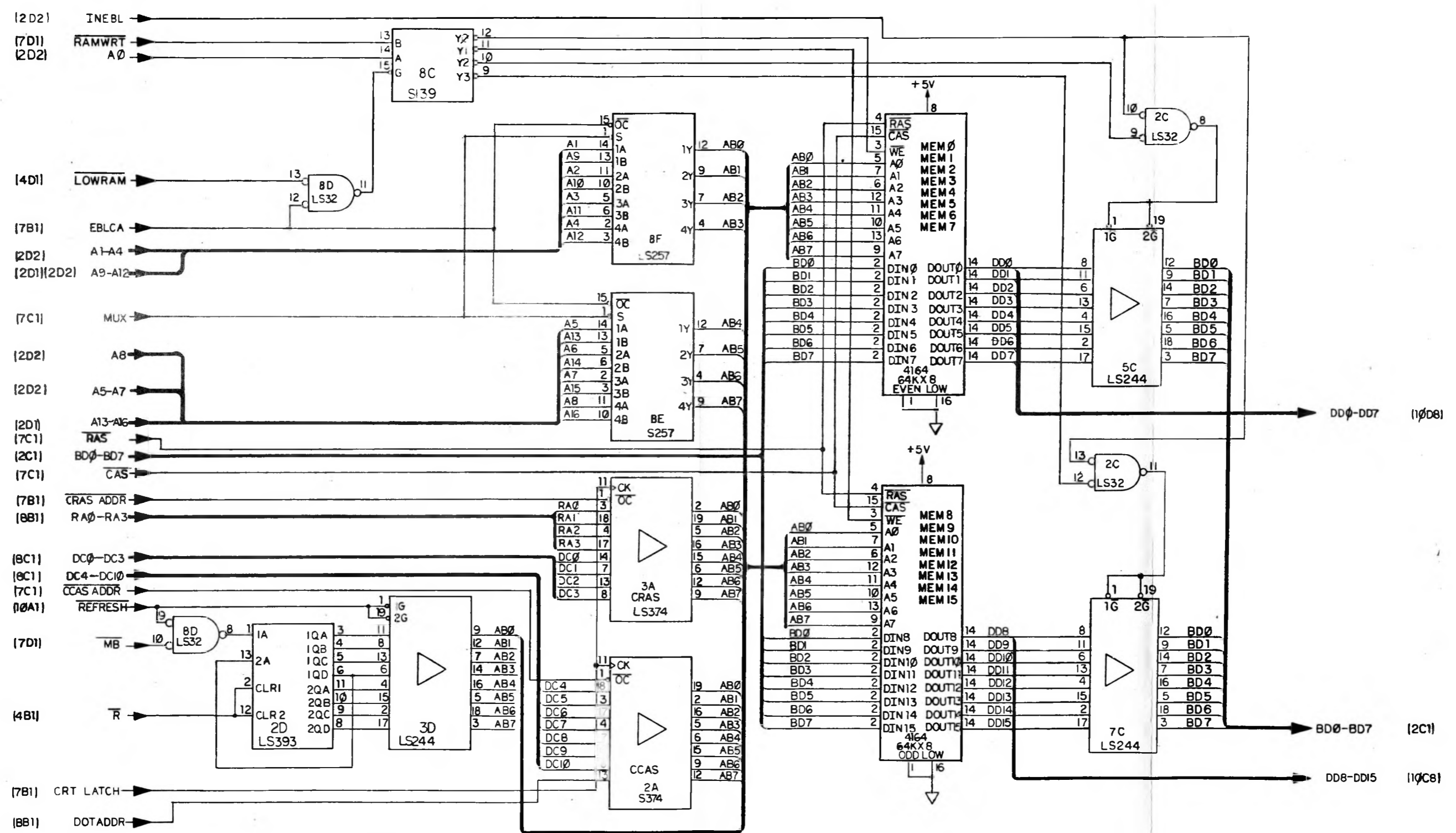
(2D2) AI-A7

(17B1) EBLCA

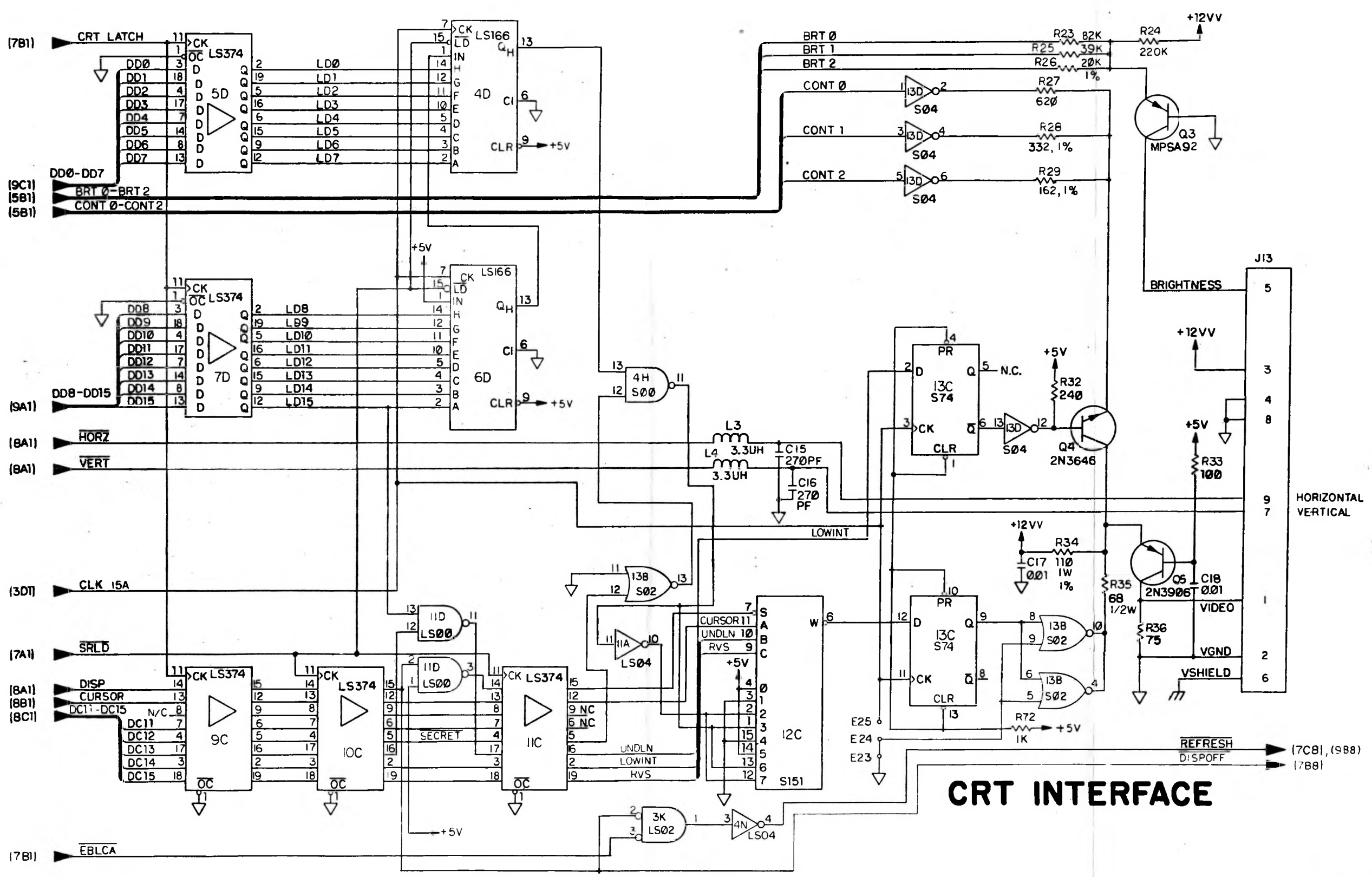
(2B1) DT/R

(2C1) ALE

9



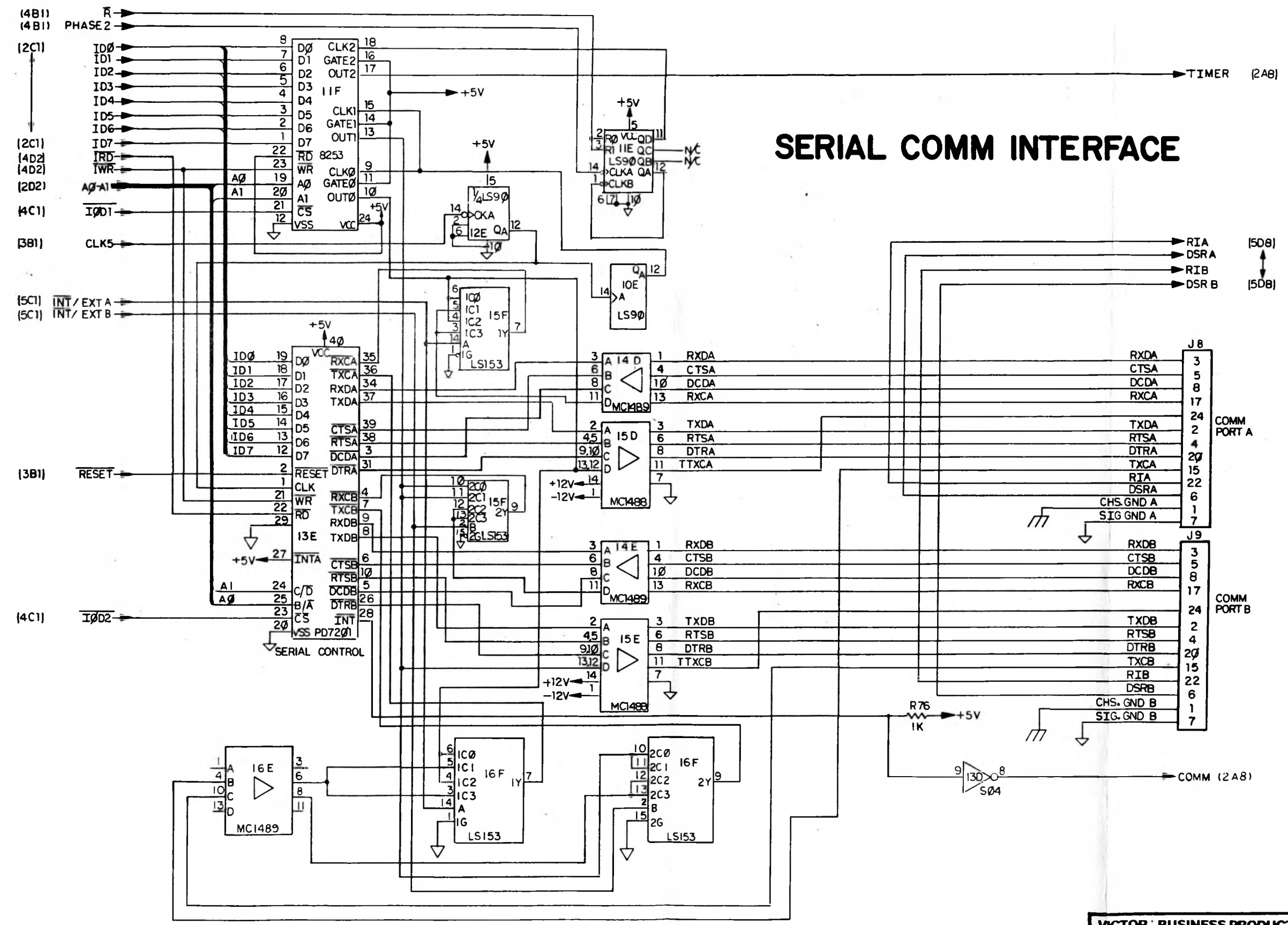
SYSTEM MEMORY



CRT INTERFACE

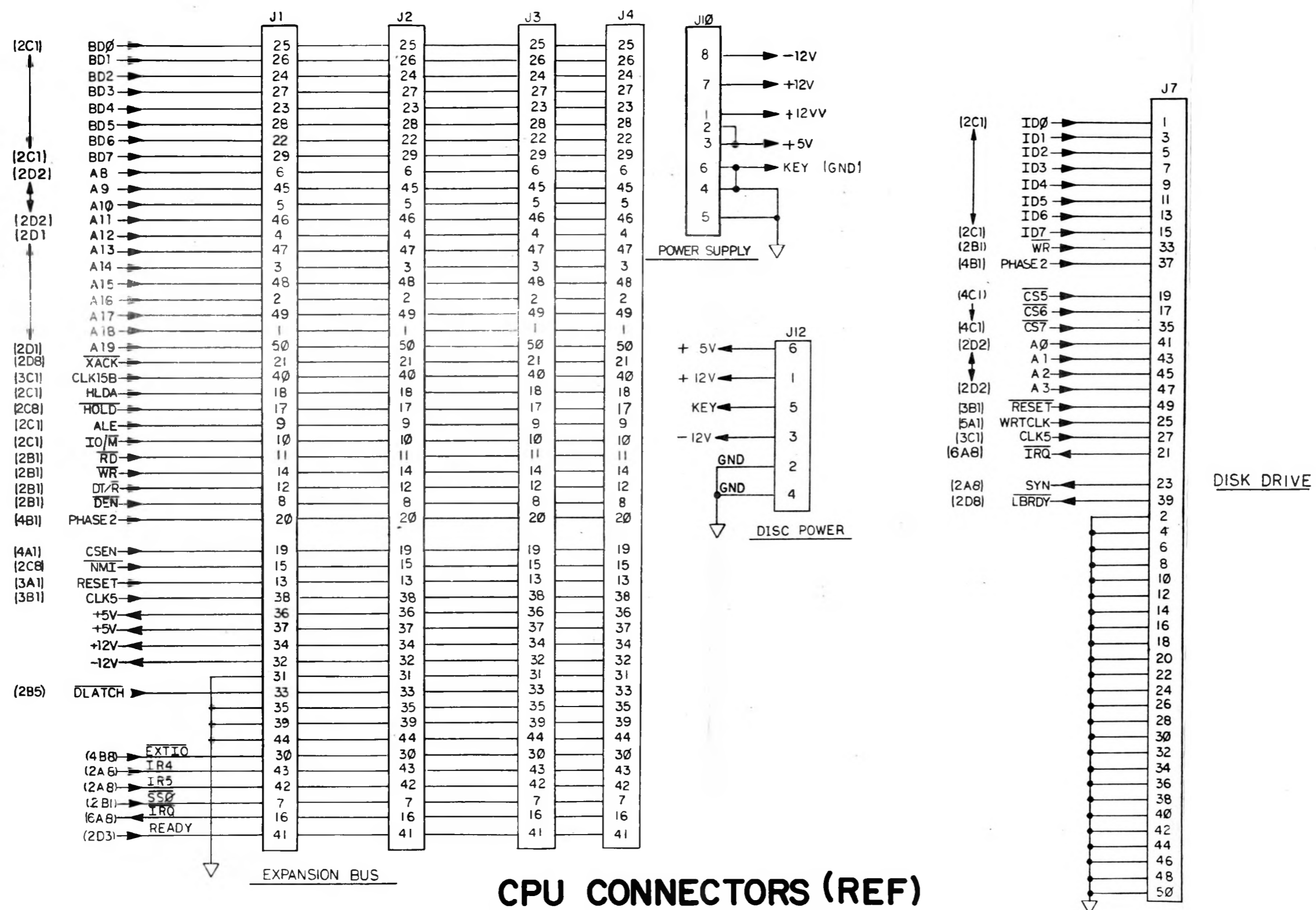
11

SERIAL COMM INTERFACE



SHT. 11 OF 14 REV. H
 DWG. NO. 100471

VICTOR BUSINESS PRODUCTS
CPU SCHEMATIC



CPU CONNECTORS (REF)

DISK DRIVE

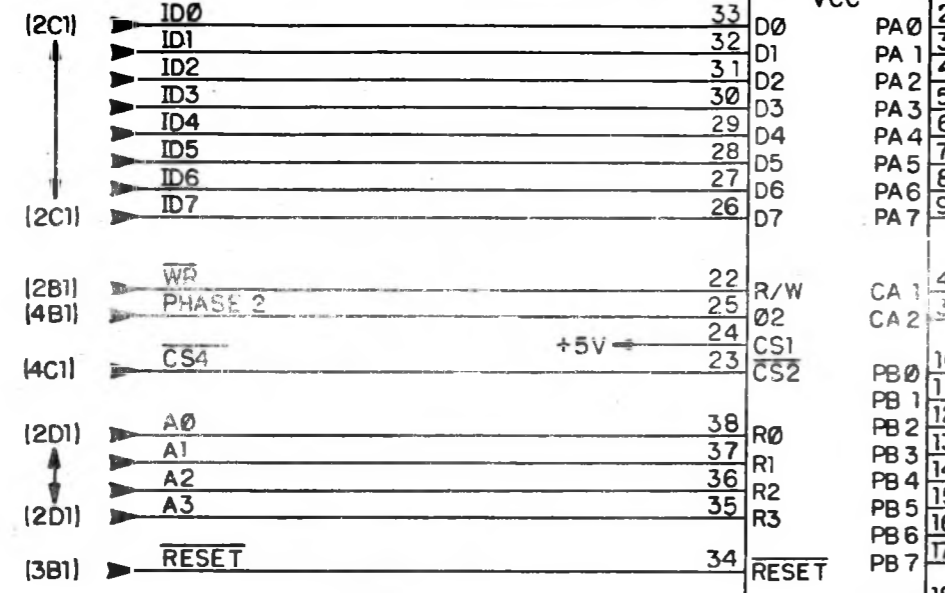
8 7 6 5 4 3 2 1

D

C

B

A



+5V

20

VCC

1

GND

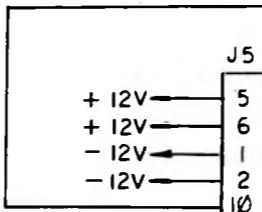
14 L

6522

IRQ

21

USER PORT



USER PORT

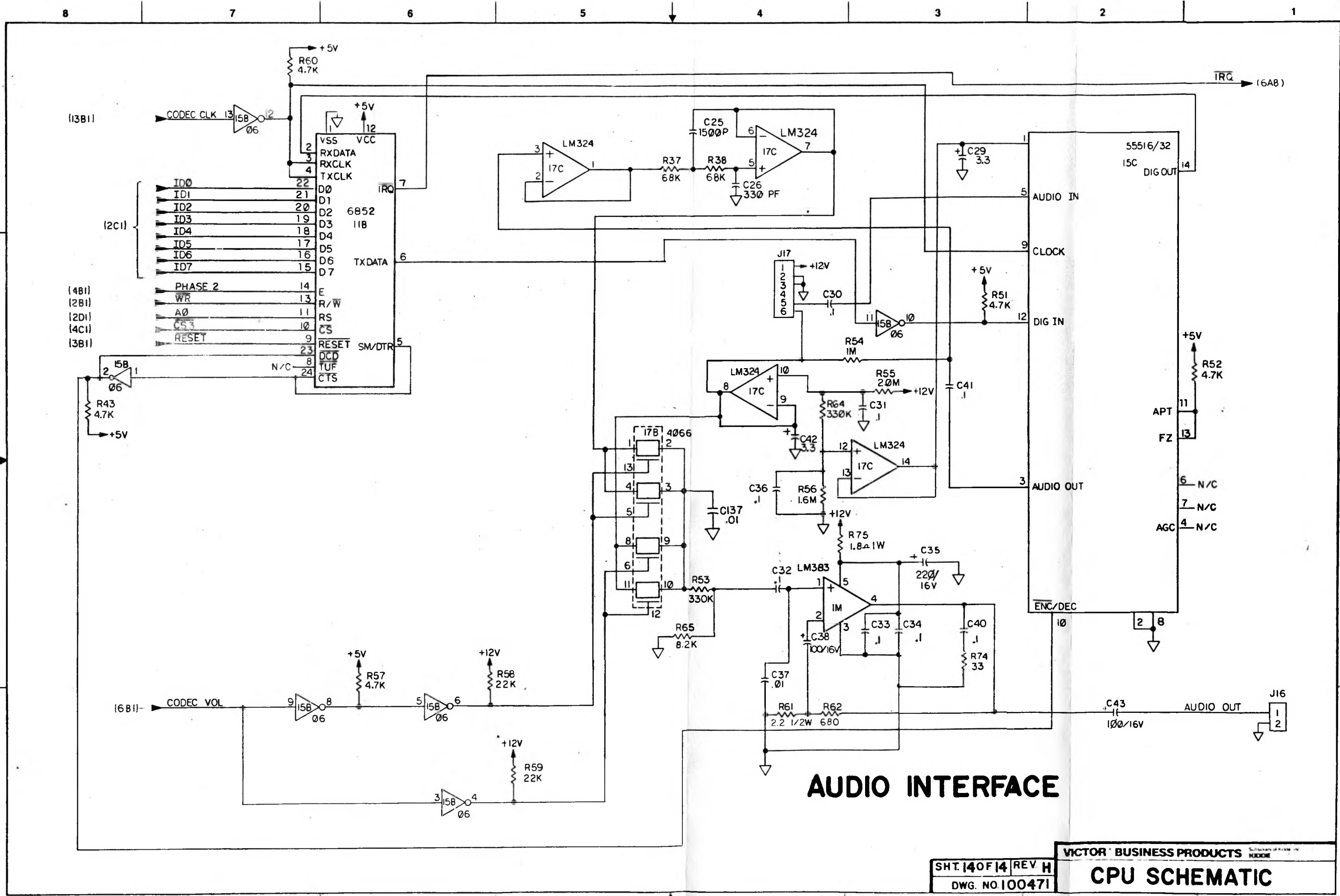
LITE PEN (8C8)

IRQ (6A8)
CODEC CLOCK (14D8)

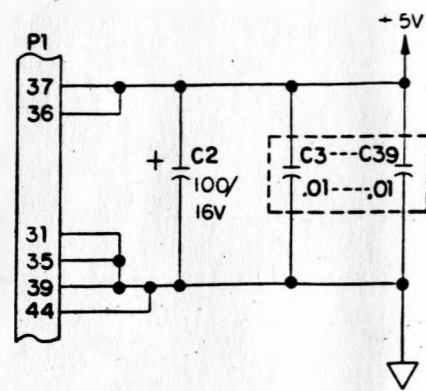
SHT. 13 OF 14 REV. H
DWG. NO. 100471

VICTOR BUSINESS PRODUCTS
CPU SCHEMATIC

8 7 6 5 4 3 2 1



AUDIO INTERFACE

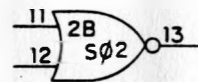


POWER & SPARES

NOTES: UNLESS OTHERWISE SPECIFIED

1. ELECTRICAL VALUES ARE IN OHMS, MICROFARADS, AND MICROHENRIES.
2. ALL RESISTORS ARE $\pm 5\%$, 1/4W
3. ALL INTEGRATED CIRCUITS ARE SN74 SERIES.
4. IC PINS ARE , GND=7, +5V=14

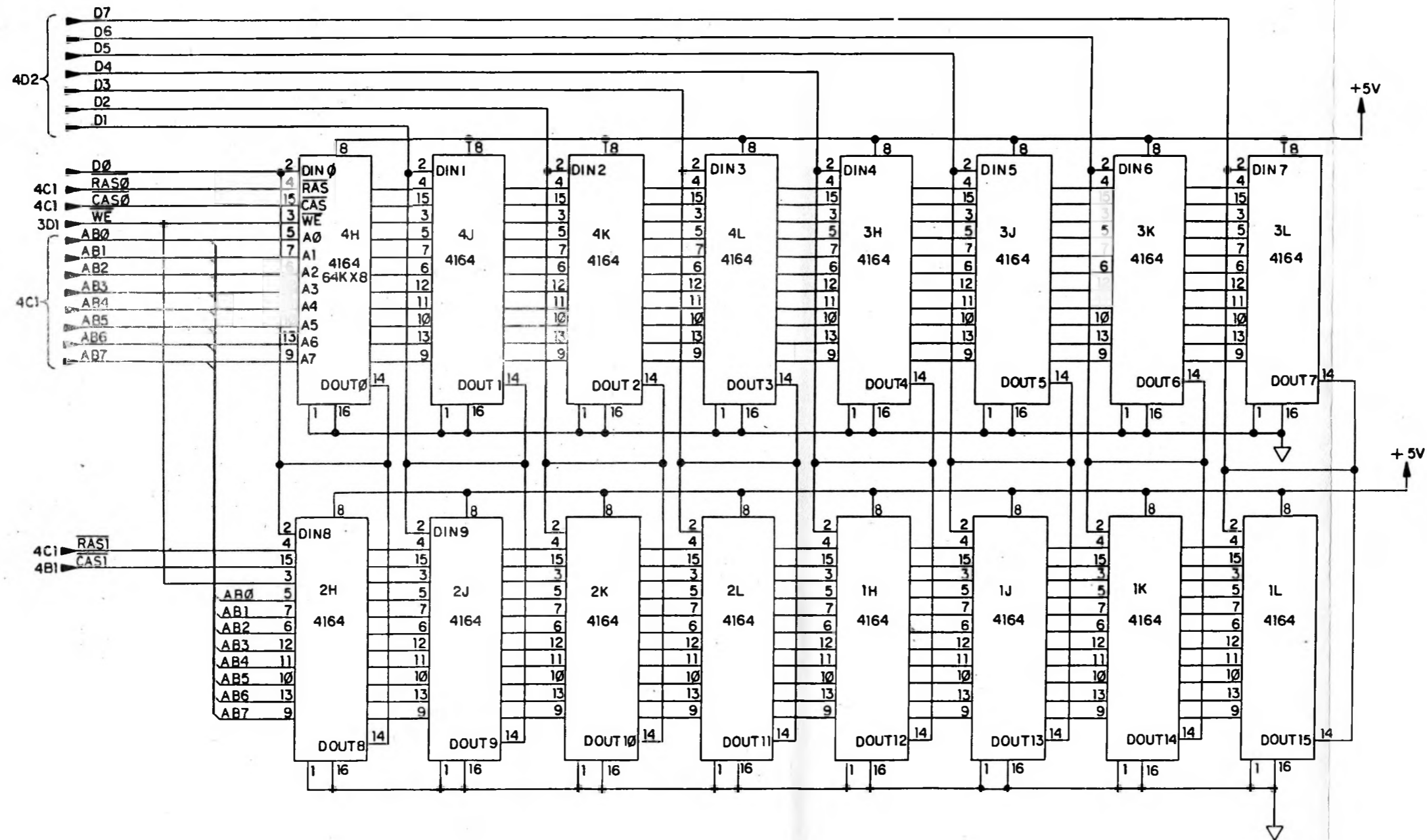
IC TYPE	GND	+ 5V
74LS138	8	16
74LS139	8	16
74LS153	8	16
74LS157	8	16
74LS174	8	16
74LS175	8	16
74LS245	10	20
74LS373	10	20
4164	16	8



SPARE GATES

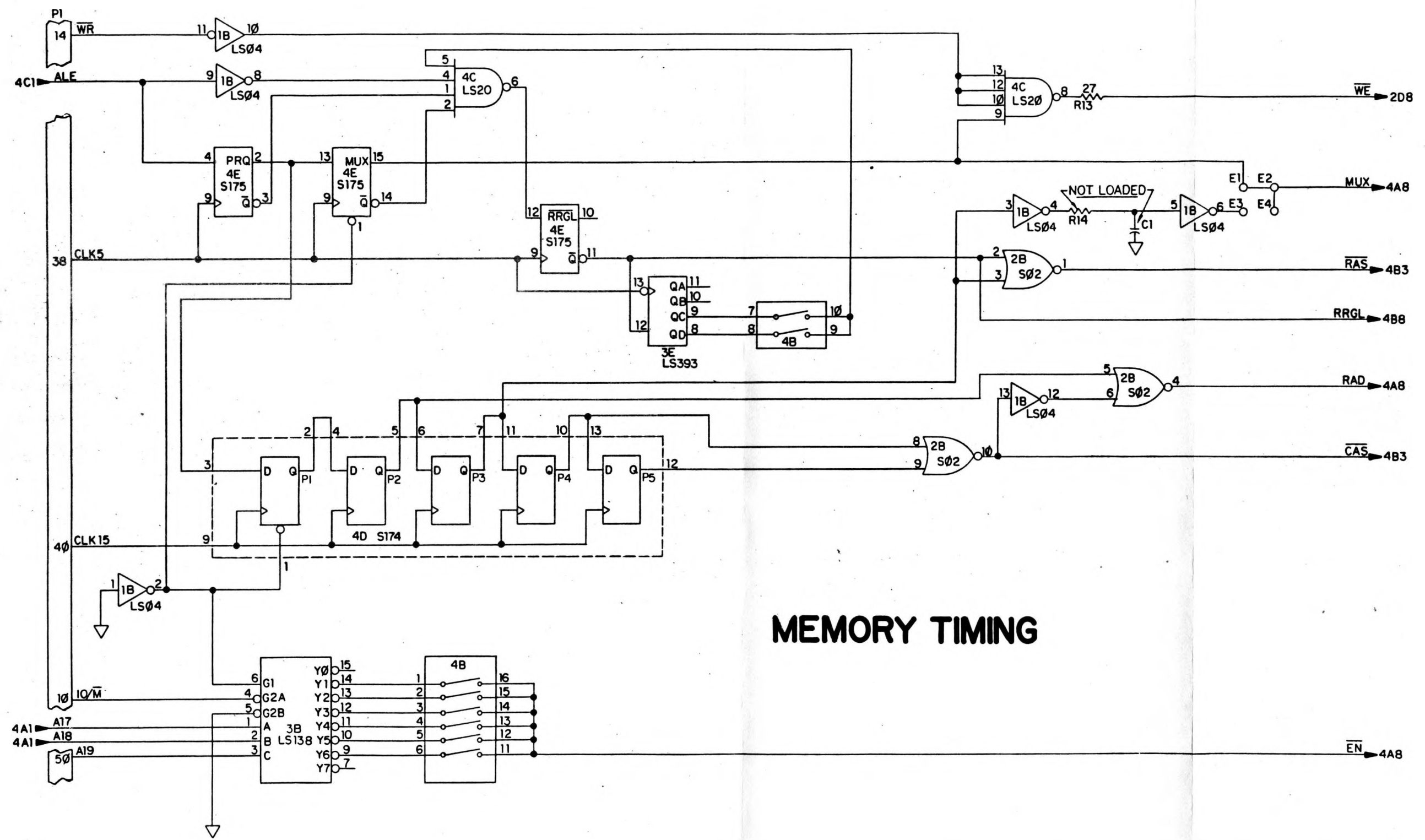
SHT. 1 OF 4 REV. P1
DWG. NO. 100901

VICTOR BUSINESS PRODUCTS SUBSIDIARY OF AMER. MIC. KODAK
128K MEMORY SCHEMATIC



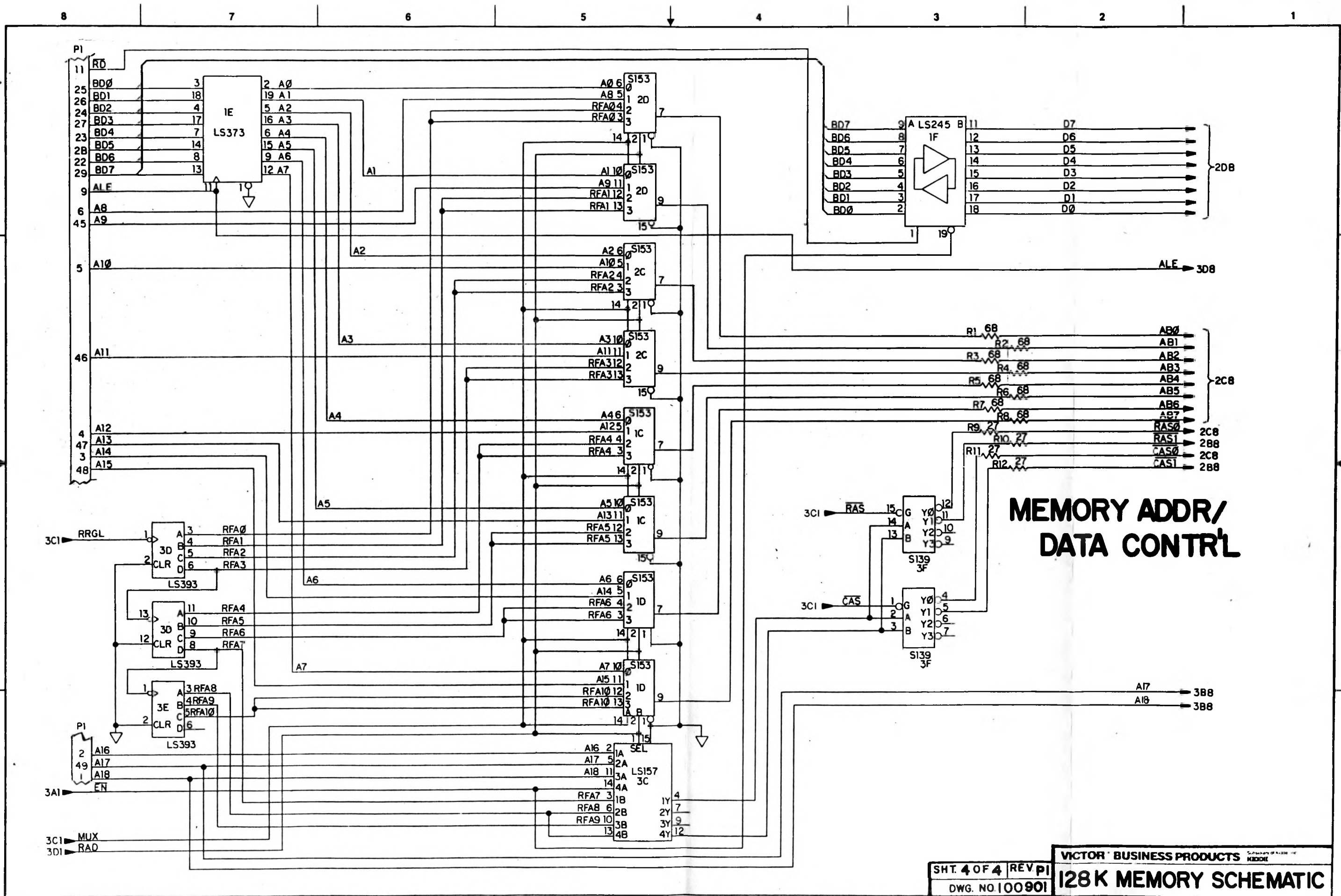
DYNAMIC RAMS

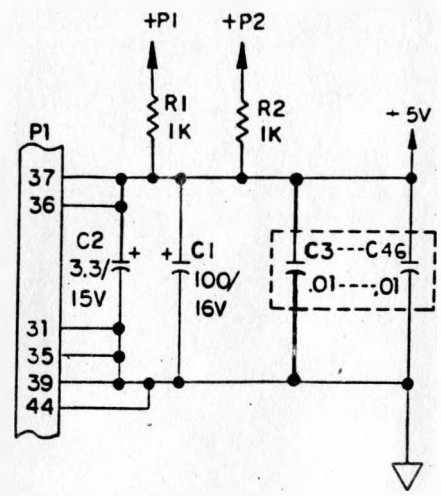
8 7 6 5 4 3 2 1



MEMORY TIMING

8 7 6 5 4 3 2 1



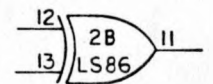
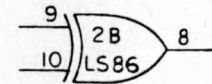
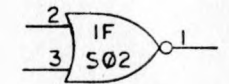
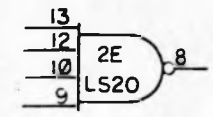
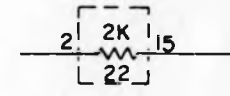


NOTES: UNLESS OTHERWISE SPECIFIED

1. ELECTRICAL VALUES ARE IN OHMS, MICROFARADS, AND MICROHENRIES.
2. ALL RESISTORS ARE $\pm 5\%$, 1/4W
3. ALL INTEGRATED CIRCUITS ARE SN74 SERIES.
4. IC PINS ARE , GND=7, +5V=14

IC TYPE	GND	+ 5V
74LS138	8	16
74 S153	8	16
74LS157	8	16
74 S174	8	16
74 S175	8	16
74LS245	10	20
74LS373	10	20
4164	16	8 (REF)

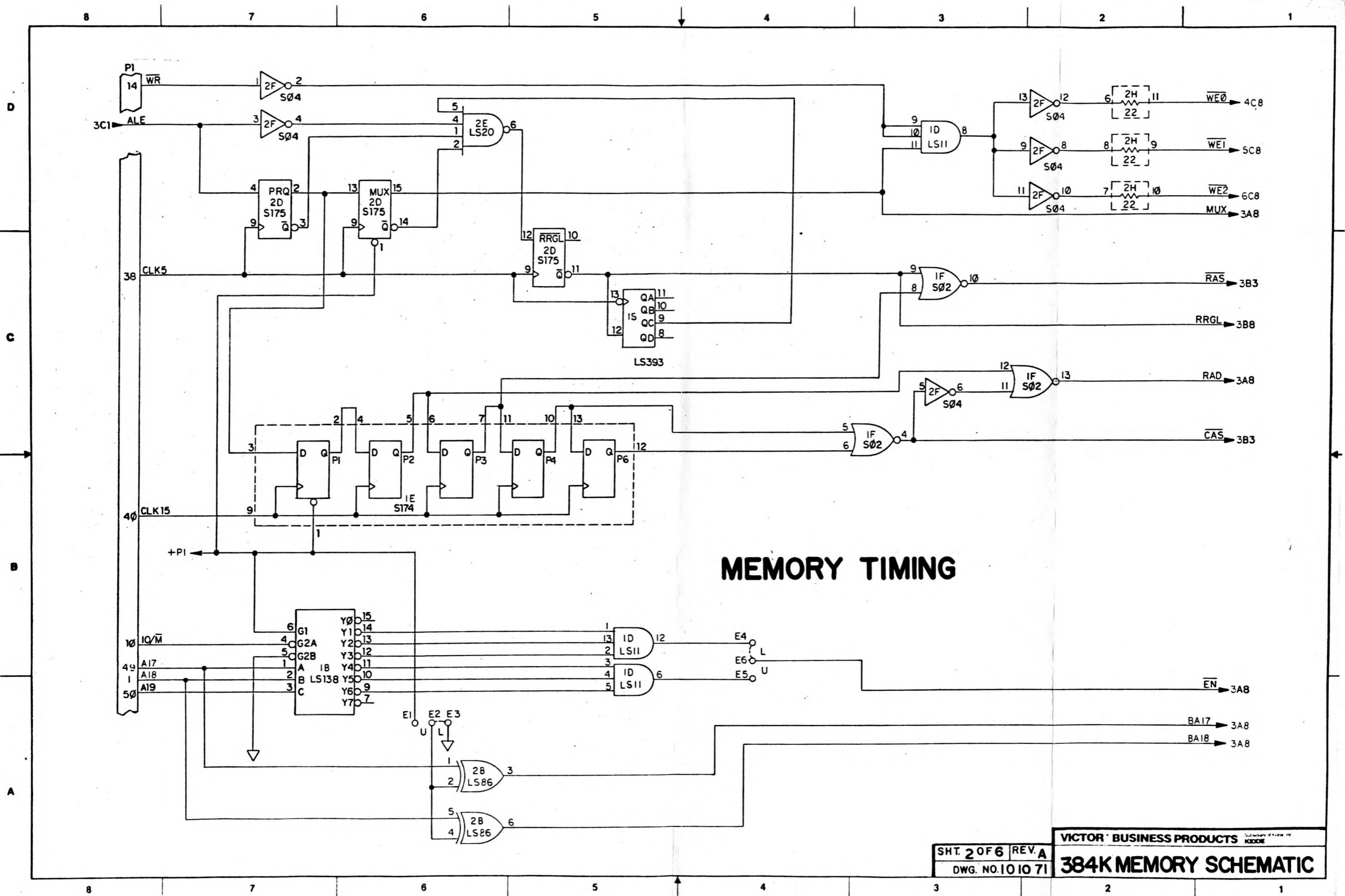
POWER & SPARES



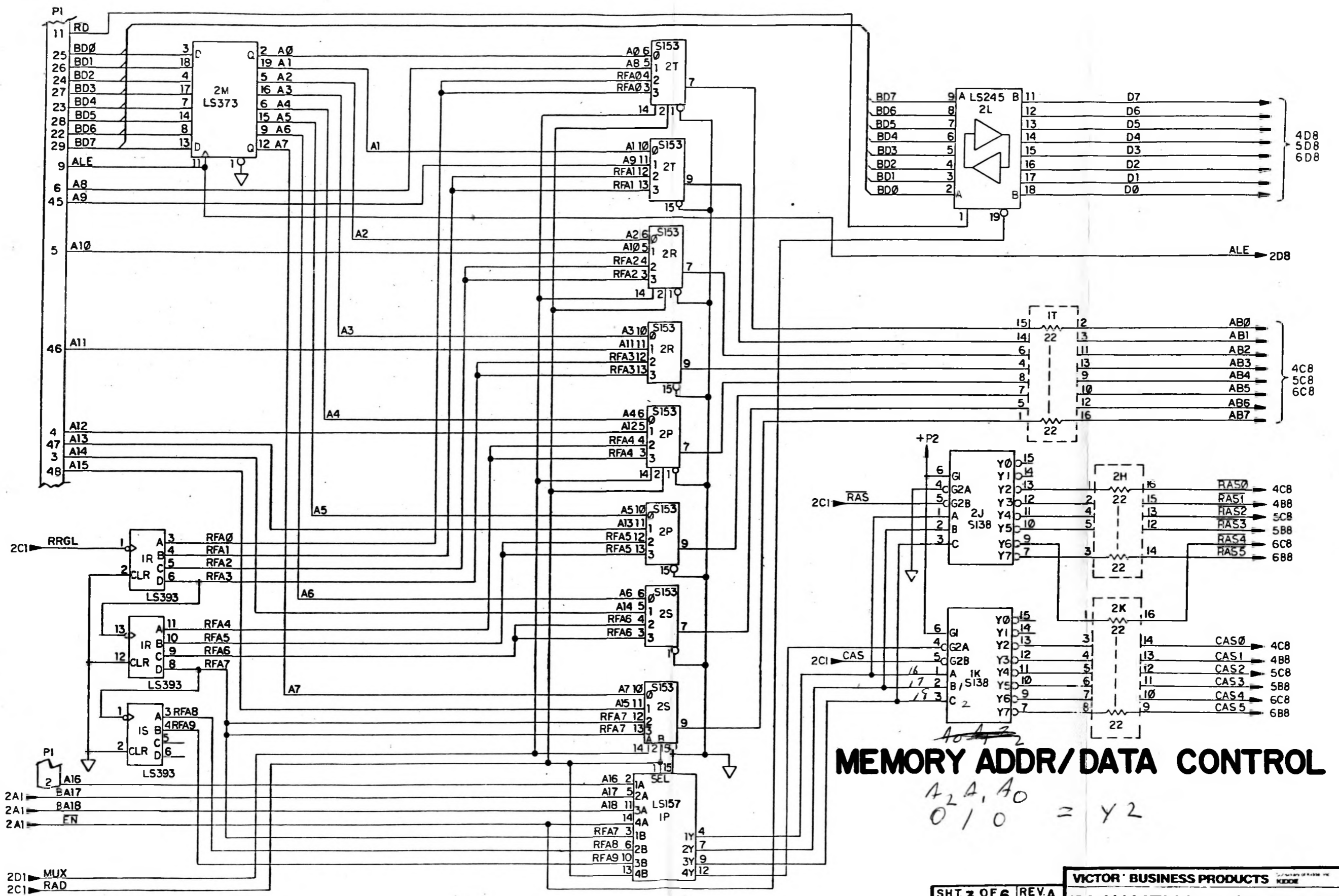
SPARE GATES

SHT. 1 OF 6 REVA
DWG. NO 10 10 71

VICTOR BUSINESS PRODUCTS
384K MEMORY SCHEMATIC

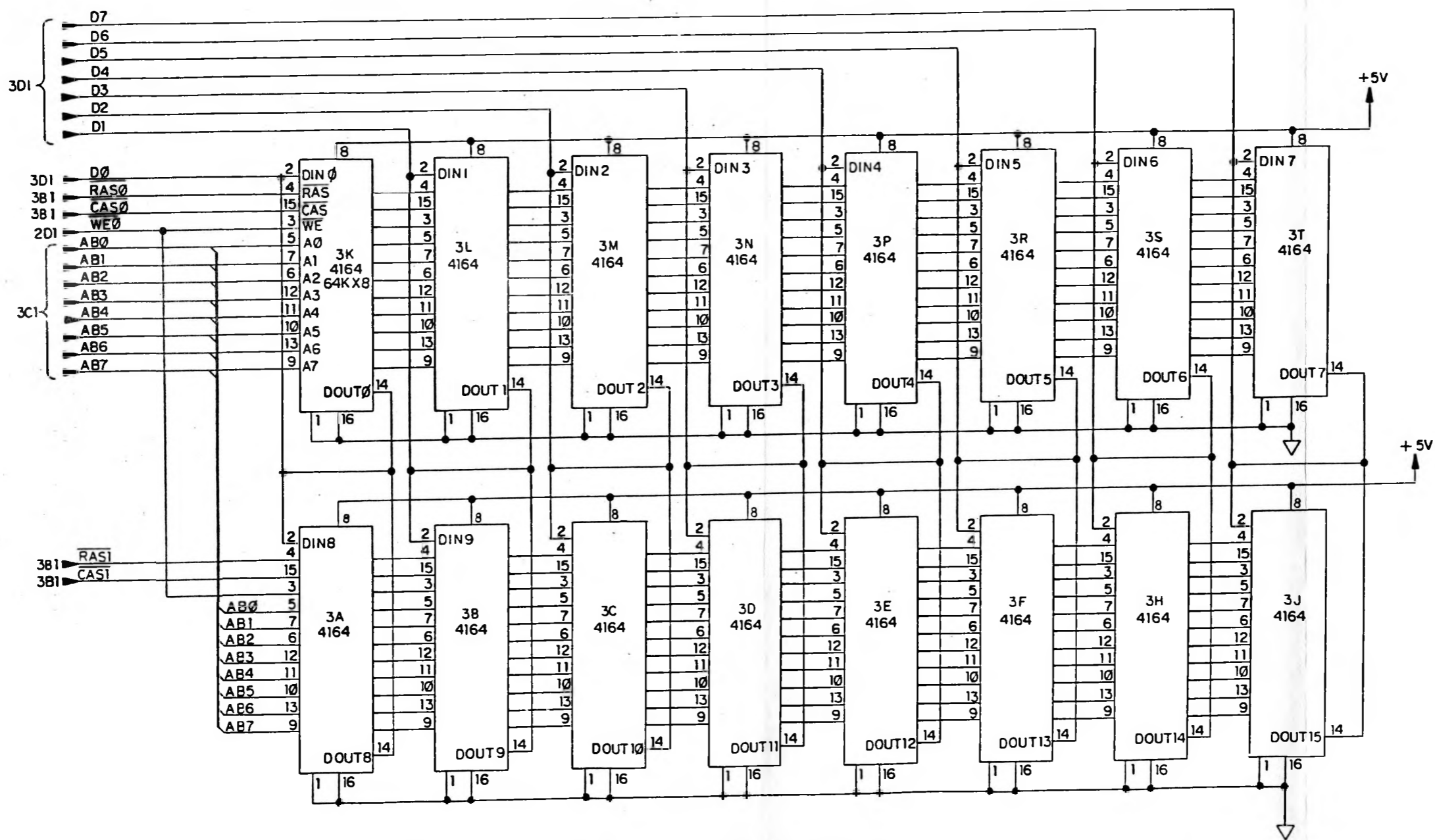


MEMORY TIMING

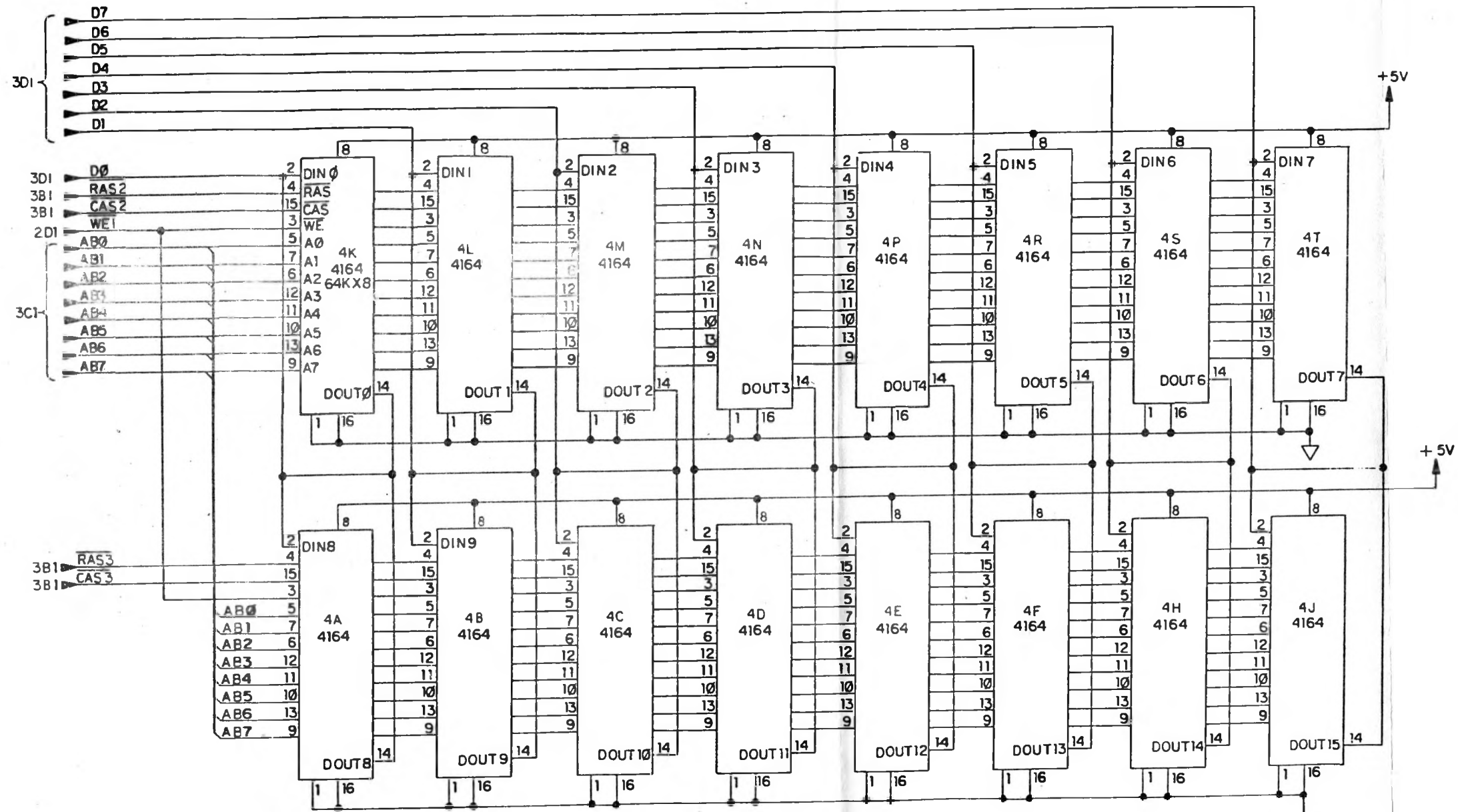


MEMORY ADDR/DATA CONTROL

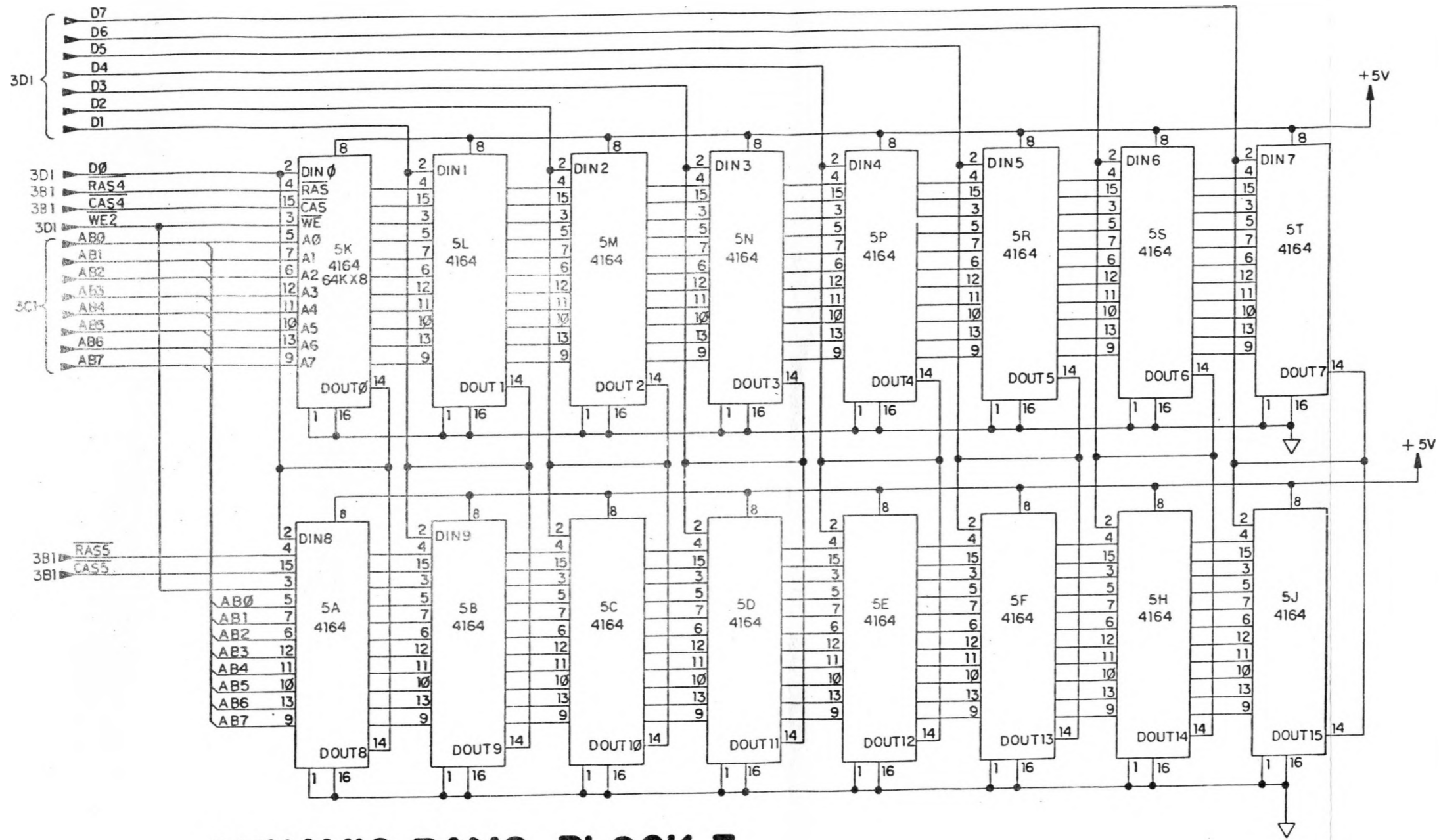
A₂A₁A₀ = Y₂
010 = Y₂



DYNAMIC RAMS, BLOCK I



DYNAMIC RAMS, BLOCK 2



DYNAMIC RAMS, BLOCK 3