

WANG

3404

**4200 - Series
VS/OIS Workstation**

Models:

4230

4205

PREFACE

This microfiche document is the Standard Maintenance (STD) Manual for the Wang 4230 and 4205 Workstations. It is organized in accordance with the approved STD outline established at the Field/Home Office Publications meetings conducted on September 14th and 15th, 1982. The scope of this manual reflects the type of maintenance philosophy selected for this product (swap unit, printed circuit assembly, chip level or any combination thereof).

The purpose of this manual is to provide the Wang-trained Customer Engineer (CE) with instructions to operate, troubleshoot and repair the Wang 4230 and 4205 Workstations. It will be updated on a regular schedule.

Third Edition (August 1984)

This edition of the 4230/4205 Workstation STD manual obsoletes document number 729-1339-A. The material in this document may only be used for the purpose stated in the Preface. Updates and/or changes to this document will be published as Product Update Bulletins (PUBs) or subsequent editions.

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WARNING

Do not open the switching Power Supply under any circumstance. Extremely dangerous voltage and current levels (in excess of 300 volts and unlimited current) are present within the Power Supply. Do not attempt to repair the switching Power Supply; it is field replaceable only. After powering the unit down and disconnecting the ac power plug from the wall outlet, allow one minute before removing the Power Supply to provide adequate time for any residual voltage to drain through the bleeder resistors.

CHAPTER

1

**INTRO-
DUCTION**

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CHAPTER 1

INTRODUCTION

1.1 SCOPE AND PURPOSE OF MANUAL

This manual contains installation, operation and maintenance information for the 4230 VS/OIS Workstation and the 4205 VS Workstation. (Refer to Figure 1-1.) These workstations are supported in the field on a board/unit-swap basis. Maintenance tasks, functional theory and parts replacement in this manual are detailed to that same level. Collectively, these workstations are referred to as the 4230/05 Workstations throughout this manual.

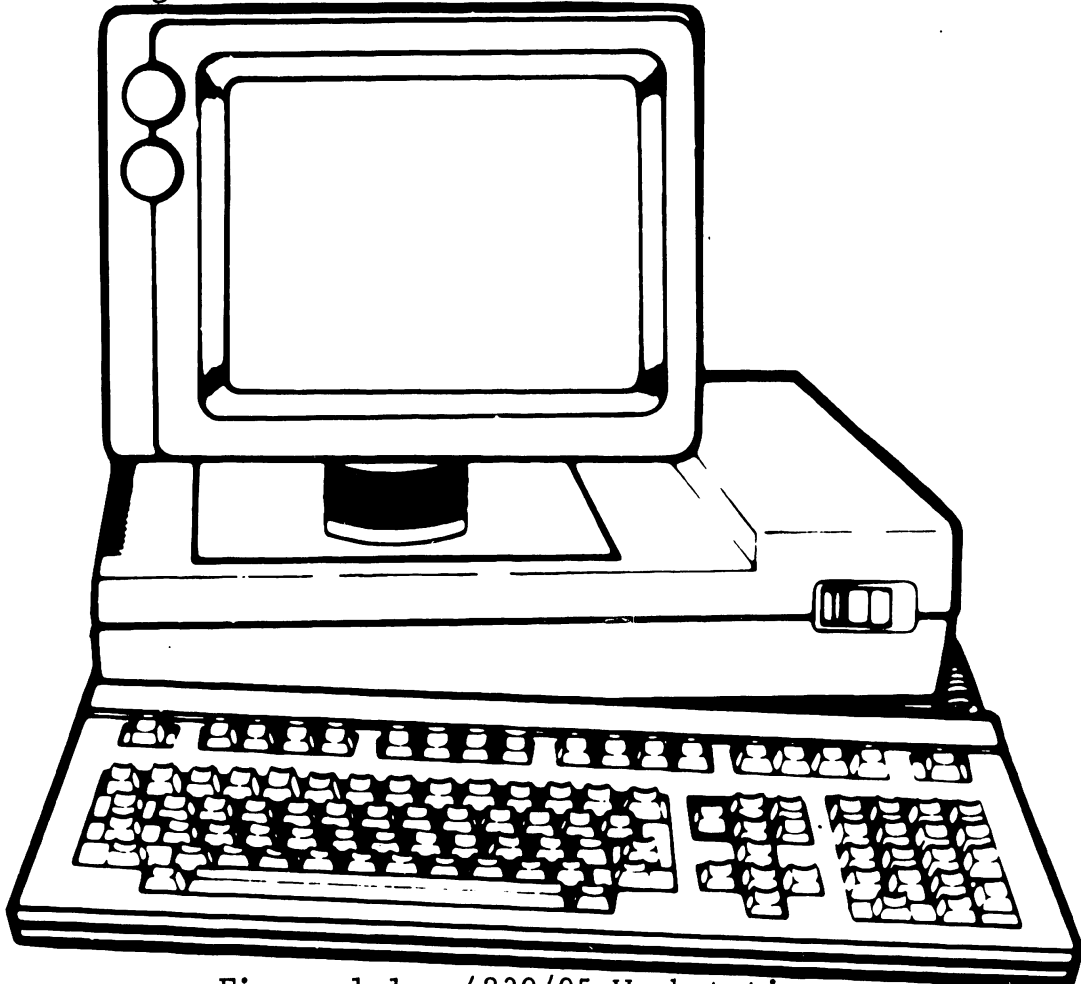


Figure 1-1. 4230/05 Workstation

1.2 APPLICABLE DOCUMENTATION

1.2.1 PUBLICATIONS

Publications relating to the 4230/05 Workstations and their installation, operation and use on VS/OIS systems are listed in Table 1-1. Ordering addresses for publications appear below.

Address For Wang User Manuals
(Prefix 700-, 800-):

WANG LABORATORIES, Inc.
Information Resources (M/S 5511)
c/o Order Entry Dept.
51 Middlesex Street
No. Chelmsford, MA 01863

Address For Wang CE Manuals
(Prefix 729-, 741-, 742-):

WANG LABORATORIES, INC.
Order Entry Dept.
c/o (Your Area Representative)
437 So. Union Street
Lawrence, MA 01843

Table 1-1. Related Publications

PUBLICATION	ORDER NUMBER
VS-100 Maintenance Manual	729-0871-A
VS 95 Maintenance Manual	729-1224
VS 25/45 Maintenance Manual	729-1032-A
VS Input/Output Processor Manual	729-0824
22V17 WS/Printer/AWS I/O Processor PSN	729-0932
Site Planning Guide	700-5978
VS System Administrative Reference (O/S Release 6.X)	800-1144-01
VS Operating System Release 6.X Software Bulletin	800-3111
OIS Operator's Guide	700-5739A
OIS Operator's Reference Guide	700-5740B
CE Documentation Control & Processing Catalog/Index	729-0000-B
Corporate Literature Catalog	700-7647

1.2 APPLICABLE DOCUMENTATION (continued)1.2.2 DIAGNOSTICS

The 4230/05 Workstations contain Built-In Test (BIT) diagnostic PROMs for use in isolating malfunctions to the defective assembly or board. In addition, on-line diagnostics are also available in the VS and OIS diagnostic test operating systems (DTOS). Table 1-2 lists the part numbers and current revisions of the BIT PROMs along with the documentation part numbers for those packages.

Table 1-2. Diagnostics

4230 BIT PROM Diagnostics					
PKG. P/N	DOC. P/N	DOC. REV.	S/W P/N	S/W REV	PROM P/N
195-2697-3	760-1192	9370	702-0270	5370	378-8046
4205 BIT PROM Diagnostics					
PKG. P/N	DOC. P/N	DOC. REV.	S/W P/N	S/W REV	PROM P/N
195-2838-3	760-1219	93B0	702-0279	53B0	378-8051

Abbreviations used in above table:

Pkg. P/N = package part number

Doc. P/N = documentation part number

Doc. Rev. = documentation revision

S/W P/N = software part number

S/W Rev = software revision

PROM P/N = PROM part number.

1.3 DESCRIPTION

The 4230/05 Workstations are modular, easy to service workstations offered by Wang for VS and OIS customers. The 4230 is a multi-system unit capable of operation on either VS or OIS systems, while the 4205 is offered for use on VS systems only. Specific applications of these workstations are discussed in section 1.4.

The workstations are Z-80 based and modular in design, comprising three basic components which operate together to provide the workstation functions. The modular approach allows greatly simplified methods of service to be employed in the field, as well as supporting the ergonomic design principles typical of Wang equipment.

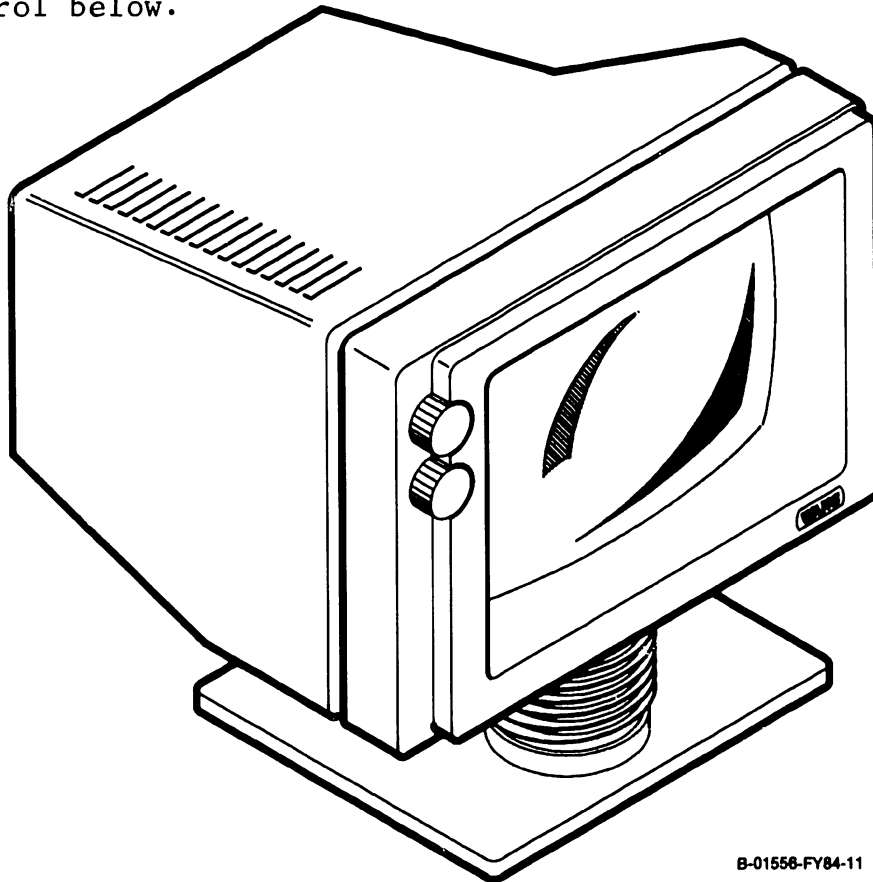
Note that this is the same Monitor currently used with the Wang Professional Computer.

1.3 DESCRIPTION (continued)

1.3.1 VIDEO MONITOR

Figure 1-2 shows the Monitor used with the 4230/05 Workstations. The unit provides an 80 column by 25 row, 12-inch diagonal green-on-black viewing screen, with the cathode-ray tube (CRT) and associated electronics housed in a two-piece enclosure. Altogether, the self-contained Monitor sits atop a pedestal attached by means of a ball-joint fitting. This allows the Monitor, and hence the viewing screen, to be tilted to suit the operator. The pedestal fits into a depression in the cover of the Electronics Base.

Brightness and contrast controls are placed in the upper left corner of the unit, with the brightness control on top and the contrast control below.



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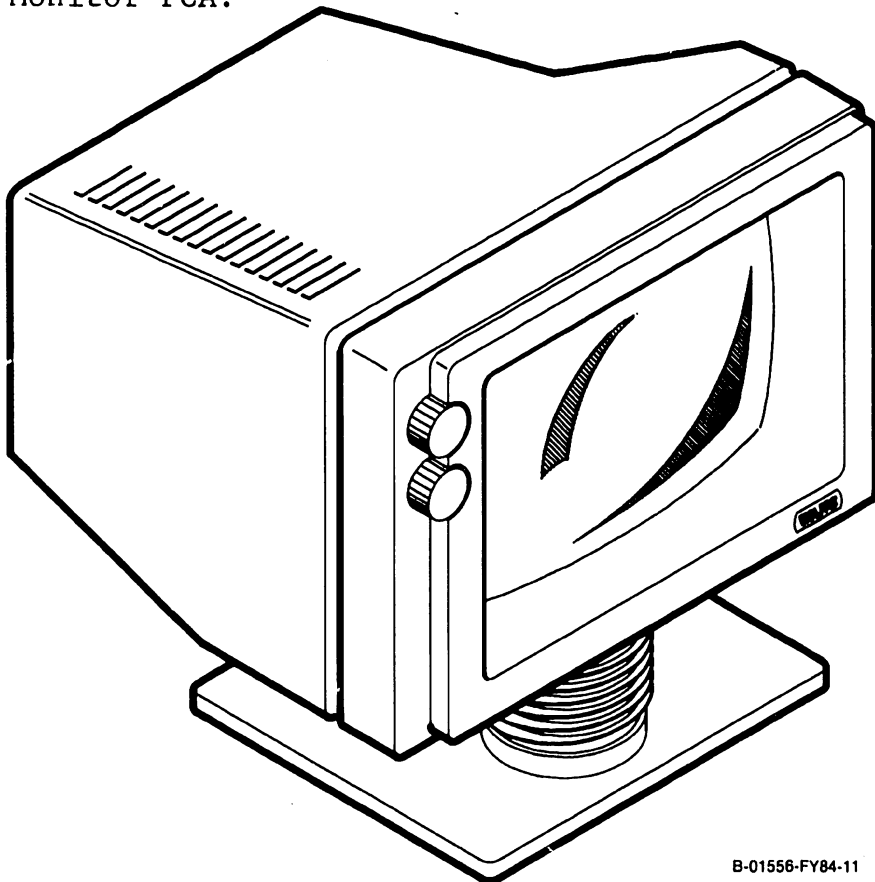
Figure 1-2. Monitor

1.3 DESCRIPTION (continued)

1.3.1 VIDEO MONITOR (continued)

Internally, the Monitor uses one of two printed circuit assemblies (PCAs) to process and display incoming video and synchronization signals. The Monitor has no internal power supply of its own, but relies on a +12 Vdc input from the Electronics Base.

A dual cable connects the Monitor to the Electronics Base, with one of the cables connecting power between the units and the other carrying the video and synchronization signals. The dual cable is terminated on both ends with a molded 3-pin DIN connector for the power cable and a molded 8-pin DIN connector for the video cable. The cables connect to the Monitor on its underside, through two access holes in the cover. The DIN sockets are mounted directly to the internal Monitor PCA.

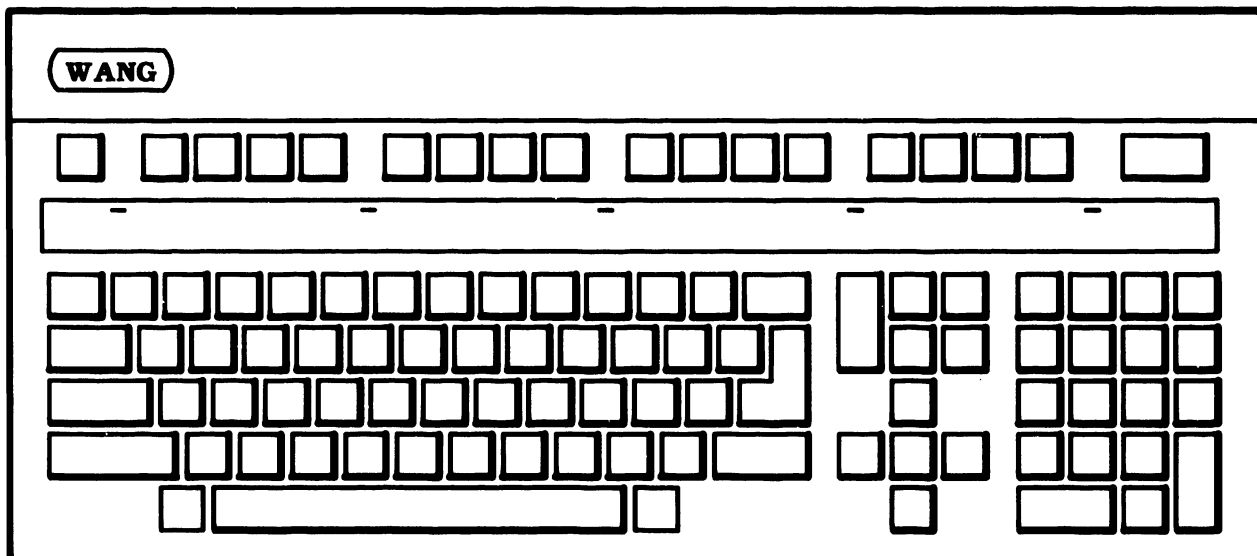


1.3 DESCRIPTION (continued)

1.3.2 KEYBOARD

The 4230/05 Workstations use the low-profile, universal serial Keyboard in use in other current Wang products, including the Wang Professional Computer. Refer to Figure 1-3. An Arabic version of the universal serial Keyboard is used with the 4230/05 Arabic Workstations. It is identical to the the keyboard shown in figure 1-3; the only difference being Arabic keycaps instead of Qwerty: US Standard.

The low-profile serial Keyboard is a separate, detachable unit containing 101 keys and a programmable speaker.



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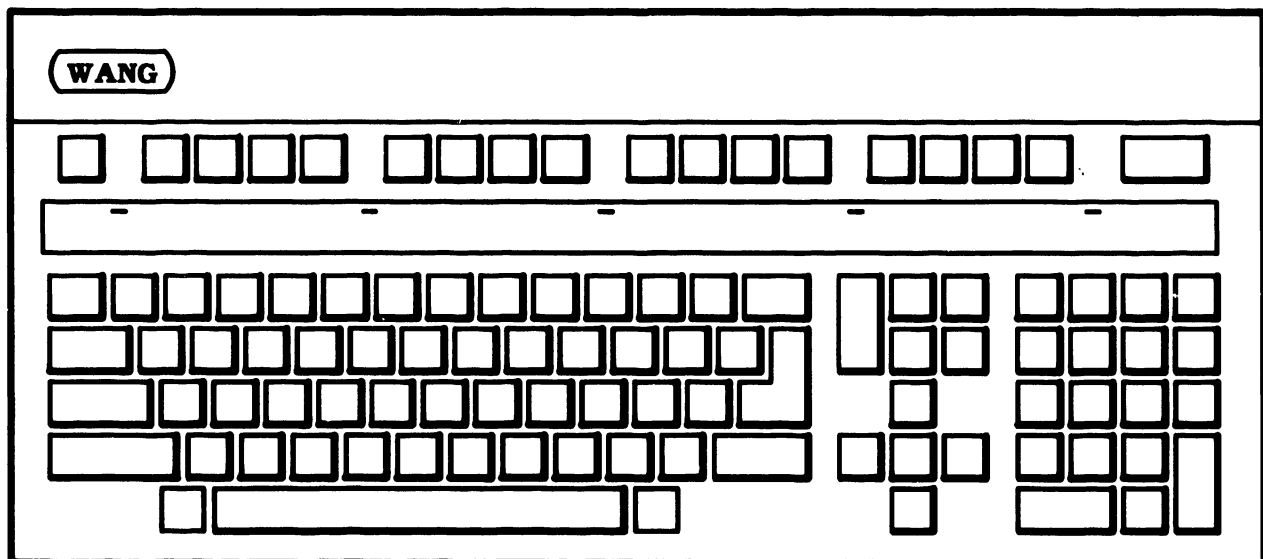
Figure 1-3. Low-Profile Serial Keyboard

1.3 DESCRIPTION (continued)1.3.2 KEYBOARD (continued)

The Keyboard offers 16 program function keys, a HELP key, four cursor control keys (north arrow, south arrow, east arrow, and west arrow), as well as a calculator-style key pad. Standard word processing edit keys are also supported (e.g., INSERT, DELETE, MOVE, COPY).

The Keyboard attaches to the Electronics Base through a coil-cord emanating from the right rear corner of the Keyboard, and terminated in a 4-pin DIN connector. The Keyboard is thus free to be moved according to the operator's preference.

An additional feature of this Keyboard is a series of six light-emitting diode (LED) indicators. Five of these are placed above the section of typewriter keys, and one is built into the LOCK key.

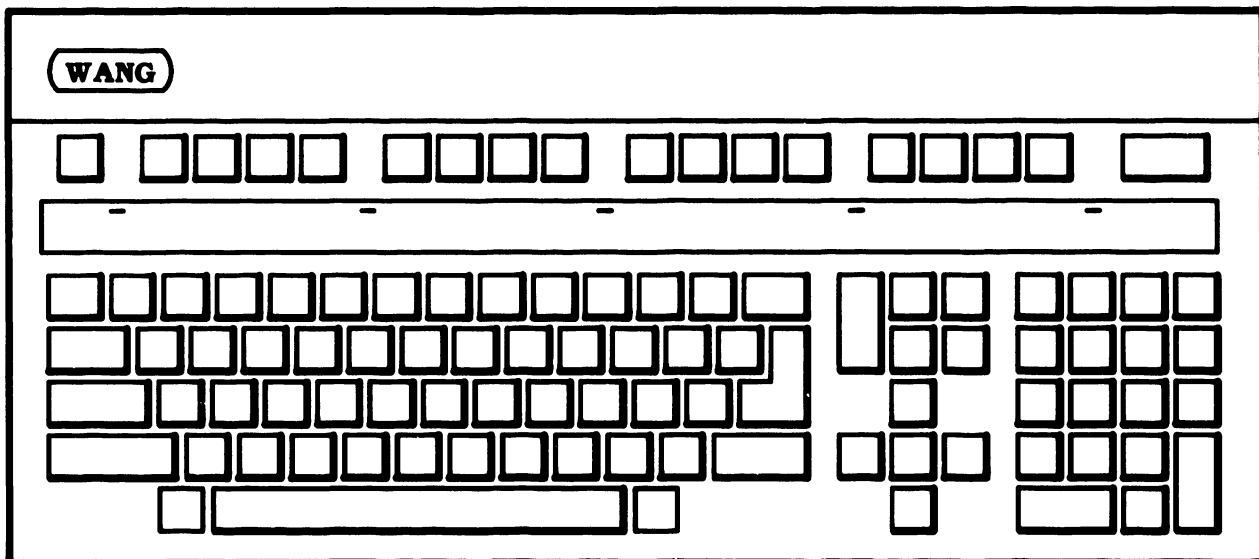


1.3 DESCRIPTION (continued)

1.3.2 KEYBOARD (continued)

These LEDs are used to display information relative to the Built-In Test (BIT) diagnostics. (Refer to Chapter 4 of this manual for details.) The LED in the LOCK key is also used to indicate, during normal operation, that either the the caps-lock or shiftlock feature is active. Caps-lock, normally used in a DP environment, and shift-lock, normally found in an office automation environment, is selected by workstation microcode.

Communication between the Keyboard and the Electronics Base is in serial format at 62.5k baud. The Keyboard itself is microprocessor based, using an 8031 CPU with PROM-based microcode.

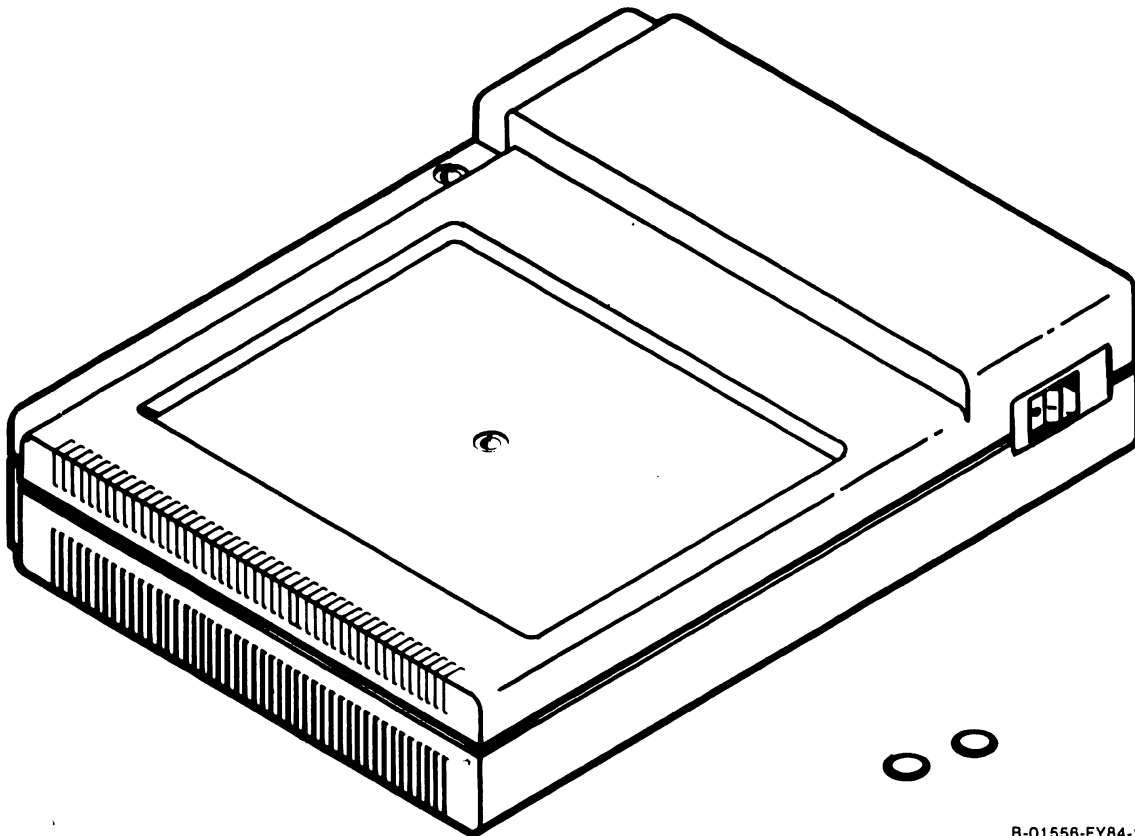


1.3 DESCRIPTION (continued)

1.3.3 ELECTRONICS BASE

The Electronics Base houses the main logic PCAs associated with the 4230/05 Workstations, along with an 80-Watt Harris switching Power Supply. Refer to Figure 1-4.

The Power Supply is field replaceable only, and is not intended to be serviced in the field. The unit supplies +5 Vdc and +12 Vdc potentials to the operating circuitry of the workstation, and incorporates a built-in ventilating fan, ac line fuse, ac power cord connector, 115V/230V switch and ac power on/off (1/0) switch in one easy-to-replace package.



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Figure 1-4. Electronics Base

1.3 DESCRIPTION (continued)

1.3.3 ELECTRONICS BASE (continued)

The unit is mechanically fastened to the base with only two screws. The base itself and the enclosed Power Supply are identical in both models of the workstation. The PCA loading of the base differentiates one model from the other.

1.3.3.1 4230 Electronics Base

The standard 4230 Electronics Base with no options houses one CPU PCA, 210-8287, which carries out all logic functions of the workstation. An optional Telecommunications PCA, 210-8298, is also available for the 4230 Workstation. Applications details of the 4230 Workstation are given in section 1.4.

The front edge of the PCAs are secured in capture slots in the front of the base, and the connector headers at the rear of the PCAs interlock with each other and the edge of the base bottom and cover. The PCAs are spaced in the center by a support/spacer rod which fits between the PCAs, seated against the upper and lower parts of the base. The rod also provides support for the physical weight of the Monitor which is placed atop the Electronics Base.

1.3.3 ELECTRONICS BASE (continued)

1.3.3.1 4230 Electronics Base (continued)

The 8287 CPU PCA contains three LSI (large scale integration) devices and their support logic, thus providing all logic required for workstation operation on a single board. The LSI devices are a Z-80 CPU, an 8031 microprocessor for the serial keyboard interface and a WL-2001 device which provides all the functions of a standard Wang 928 data link in a single LSI device.

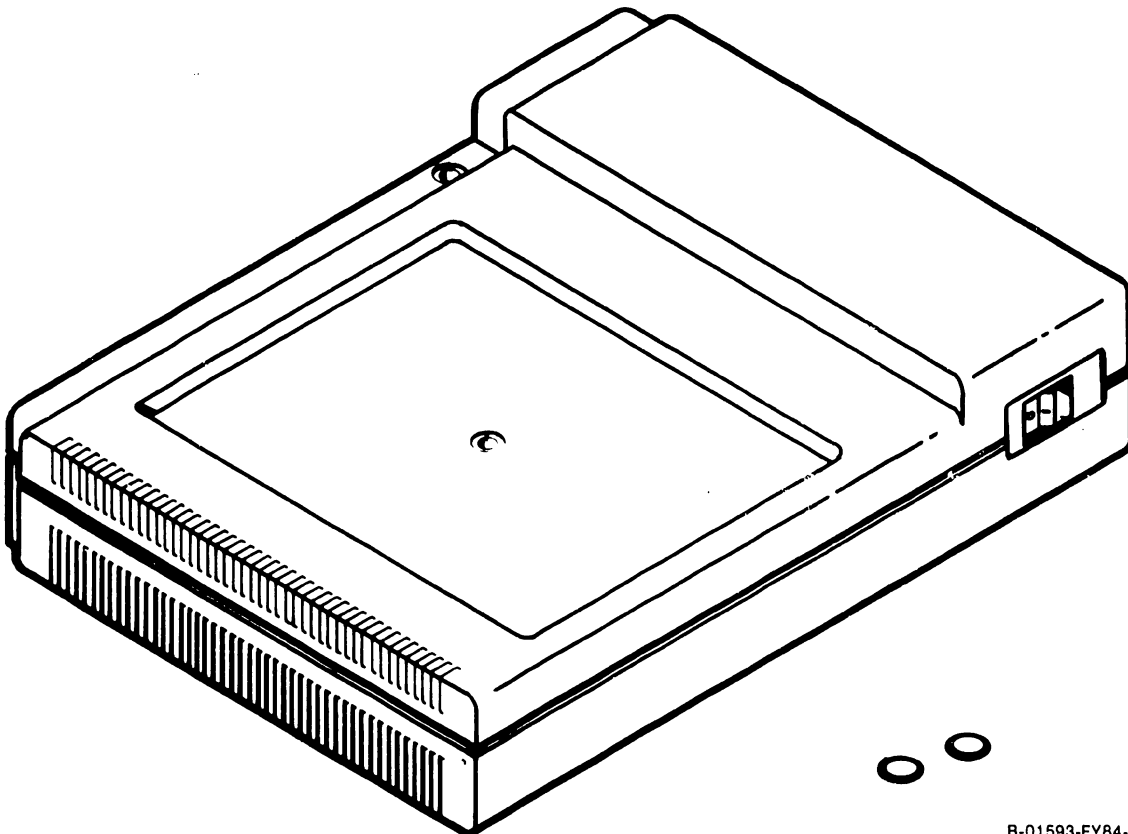
Support logic for these main LSI devices includes 64k bytes of main memory with parity, a 4k PROM containing the Built-In Test (BIT) power-up diagnostic, and CRT RAM including 4k of character RAM, 4k of attribute RAM and 8k of font RAM. Another 4k PROM stores the operating program for the 8031 microprocessor.

Workstation operating software (microcode) is downline loaded from the system host CPU and stored in main memory. The unit features softwareloadable fonts which are also downline loaded from the system host. The connector header mounted on the rear of the CPU PCA contains the DATA LINK BNC/TNC connectors for cable connection to the host.

1.3.3 ELECTRONICS BASE (continued)

1.3.3.2 4205 Electronics Base

The 4205 Workstation Electronics Base is essentially the same as the 4230, with minor changes to the CPU PCA. The 4205 uses a 210-8287-1 CPU PCA which provides only 32k of main memory and 4k of font memory. As a result of the reduced main and font memory, the 4205 Workstation supports fewer functions than the full-feature 4230 unit. Applications details are in section 1.4.



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1.4 SYSTEM APPLICATIONS (Continued)

1.4.1 4230 WORKSTATION APPLICATIONS (Continued)

The 4230 operates as a full-functioning 64k workstation when connected to OIS and Alliance systems. All advanced word processing and most optional software packages can be used with the 4230 including: WP Plus, BASIC, spelling verifier, CP/M^R and Microsoft's Multiplan. On the VS, the 4230 can be used for data processing applications, VS/IIS word processing and VS/ Alliance. In addition, the 4230 can operate as the system console workstation (workstation zero) on all VS systems. The 4230 does not support scientific typing, archiving, proportional spacing, CHARTER graphics or audio.

In the VS 50/60/80, 4230 Workstations communicate with the host CPU via a 22V17 extended serial IOP designed for use with serial devices such as workstations and printers. In the VS 90/100, the appropriate serial IOP is the 22V27. In OIS systems, the 4230 connects directly to the host CPU.

^RCP/M is a registered trademark of Digital Research, Inc.

1.4 SYSTEM APPLICATIONS (Continued)

1.4.2 4205 WORKSTATION SYSTEM APPLICATIONS

The 4205 has limited main memory (32k) and font memory (4k) and thus supports data processing functions on VS systems only. In the VS 50/60/80, 4205 Workstations communicate with the host CPU via a 22V17 extended serial IOP designed for use with serial devices such as workstations and printers. In the VS 90/100, the appropriate serial IOP is the 22V27.

1.5 SPECIFICATIONS

Specifications for the 4230/05 Workstations are given in Table 1-3.

Table 1-3. Specifications

PARAMETER	DESCRIPTION																
CRT: 80 column by 25 row (24 rows supported by software)	12-inch diagonal, green on black,																
Data Link:	4.275 Mbps, serial asynchronous																
Keyboard Interface:	62.5k baud, asynchronous																
CPU:	Z-80																
Line Tolerance:	<table> <thead> <tr> <th></th> <th>Volts</th> <th></th> <th>Hertz</th> </tr> <tr> <th>Min.</th> <th>Nominal</th> <th>Max.</th> <th>Frequency</th> </tr> </thead> <tbody> <tr> <td>90</td> <td>115</td> <td>132</td> <td>47 - 63</td> </tr> <tr> <td>180</td> <td>230</td> <td>264</td> <td>47 - 63</td> </tr> </tbody> </table>		Volts		Hertz	Min.	Nominal	Max.	Frequency	90	115	132	47 - 63	180	230	264	47 - 63
	Volts		Hertz														
Min.	Nominal	Max.	Frequency														
90	115	132	47 - 63														
180	230	264	47 - 63														
Power Requirements:	100 Watts maximum, 80 Watts typical																
Ambient Operating Temperature:	60°F to 90°F (16°C to 32°C)																
Relative Humidity:	20% to 80% (non-condensing)																
Monitor Dimensions & Weight:	<table> <thead> <tr> <th>Height</th> <th>Width</th> <th>Depth</th> <th>Weight</th> </tr> <tr> <th>in./ (cm)</th> <th>in./ (cm)</th> <th>in./ (cm)</th> <th>lb./ (kg)</th> </tr> </thead> <tbody> <tr> <td>11.5</td> <td>13.0</td> <td>10.8</td> <td>15.0</td> </tr> <tr> <td>29.2</td> <td>33.0</td> <td>27.0</td> <td>6.8</td> </tr> </tbody> </table>	Height	Width	Depth	Weight	in./ (cm)	in./ (cm)	in./ (cm)	lb./ (kg)	11.5	13.0	10.8	15.0	29.2	33.0	27.0	6.8
Height	Width	Depth	Weight														
in./ (cm)	in./ (cm)	in./ (cm)	lb./ (kg)														
11.5	13.0	10.8	15.0														
29.2	33.0	27.0	6.8														
Keyboard Dimensions & Weight:	<table> <thead> <tr> <th>Height</th> <th>Width</th> <th>Depth</th> <th>Weight</th> </tr> <tr> <th>in./ (cm)</th> <th>in./ (cm)</th> <th>in./ (cm)</th> <th>lb./ (kg)</th> </tr> </thead> <tbody> <tr> <td>1.7</td> <td>18.3</td> <td>7.8</td> <td>4.5</td> </tr> <tr> <td>(4.3)</td> <td>(46.5)</td> <td>(19.8)</td> <td>(2.0)</td> </tr> </tbody> </table>	Height	Width	Depth	Weight	in./ (cm)	in./ (cm)	in./ (cm)	lb./ (kg)	1.7	18.3	7.8	4.5	(4.3)	(46.5)	(19.8)	(2.0)
Height	Width	Depth	Weight														
in./ (cm)	in./ (cm)	in./ (cm)	lb./ (kg)														
1.7	18.3	7.8	4.5														
(4.3)	(46.5)	(19.8)	(2.0)														
Electronics Base Dimensions & Weight:	<table> <thead> <tr> <th>Height</th> <th>Width</th> <th>Depth</th> <th>Weight</th> </tr> <tr> <th>in./ (cm)</th> <th>in./ (cm)</th> <th>in./ (cm)</th> <th>lb./ (kg)</th> </tr> </thead> <tbody> <tr> <td>4.1</td> <td>19.0</td> <td>14.1</td> <td>6.5</td> </tr> <tr> <td>(10.5)</td> <td>(48.8)</td> <td>(35.3)</td> <td>(2.9)</td> </tr> </tbody> </table>	Height	Width	Depth	Weight	in./ (cm)	in./ (cm)	in./ (cm)	lb./ (kg)	4.1	19.0	14.1	6.5	(10.5)	(48.8)	(35.3)	(2.9)
Height	Width	Depth	Weight														
in./ (cm)	in./ (cm)	in./ (cm)	lb./ (kg)														
4.1	19.0	14.1	6.5														
(10.5)	(48.8)	(35.3)	(2.9)														

1.6 OPERATING SYSTEM SUPPORT

Operating system support for the 4230/05 Workstations is listed below.

4230/42054230 ONLY

VS 5.01.73

OIS 8.3

VS 5.03.90

ALLIANCE 4.J

VS 6.11.02

VS ALLIANCE 1.0

VS 6.20.00

1.7 OPTIONS

1.7.1 4230 TELECOMMUNICATIONS

The TC PCA 210-8298 provides an RS-232C interface for connection to a modem, thus allowing the 4230 to be used for Telecommunications. Emulations supported with the 4230 TC Workstation are TTY/2741, 2780, 3780 and WPS. Telecommunication with VS systems is not supported by the 4230 TC Workstation. UJ Kit #UJ-1282, P/N 206-1282 allows the 4230 to be upgraded with TC.

1.7.2 MONITOR ARM

A Monitor arm option, similar to the one used with the Wang Professional Computer, is available for the 4230/05 Workstations. The arm allows more efficient use of work space by enabling the user to swing and tilt the Monitor over and away from the work area. An eight-foot Monitor to Electronics Base cable, included with this option, allows the Electronics Base to be placed conveniently away from the desk surface. Order number for the Monitor arm option is 4200AC-001. The Monitor arm option is customer-installable and an installation guide, document part number 700-8695, is packed with the unit.

1.7 OPTIONS (Cont'd)

1.7.3 4230/05 ARABIC

The Arabic (Middle Eastern) Workstations (Models 4230-OA-ME/4205-VS-ME) are 4230/4205 Workstations capable of supporting all existing features and options with modifications to enable easy implementation of middle eastern languages. These languages require right-to-left orientation (as opposed to English left-to-right), which would mean a substantial software effort, without hardware assist.

The hardware has been modified to allow software to treat the document as left-to-right (English), but the display will be in the correct right-to-left (Middle Eastern) orientation. The scan is software selectable to either left-to-right or right-to-left orientation but not both. Although improved software is planned, this hardware change is necessary to provide a workstation compatible with and as a replacement for the 2246S-ME.

The PCA complement consists of a 210-8287-3 PCA with Reverse Scan and a 210-8244 Monitor PCA.

CHAPTER

2

THEORY

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This chapter contains block level theory of operation discussions for the subassemblies of the 4230/05 Workstations. The equipment is covered in the subsections of this chapter as listed below.

Section 2.1 Monitor
Section 2.2 Keyboard
Section 2.3 Electronics Base
Section 2.4 4230 TC Option
Section 2.5 4230/05 Arabic WS

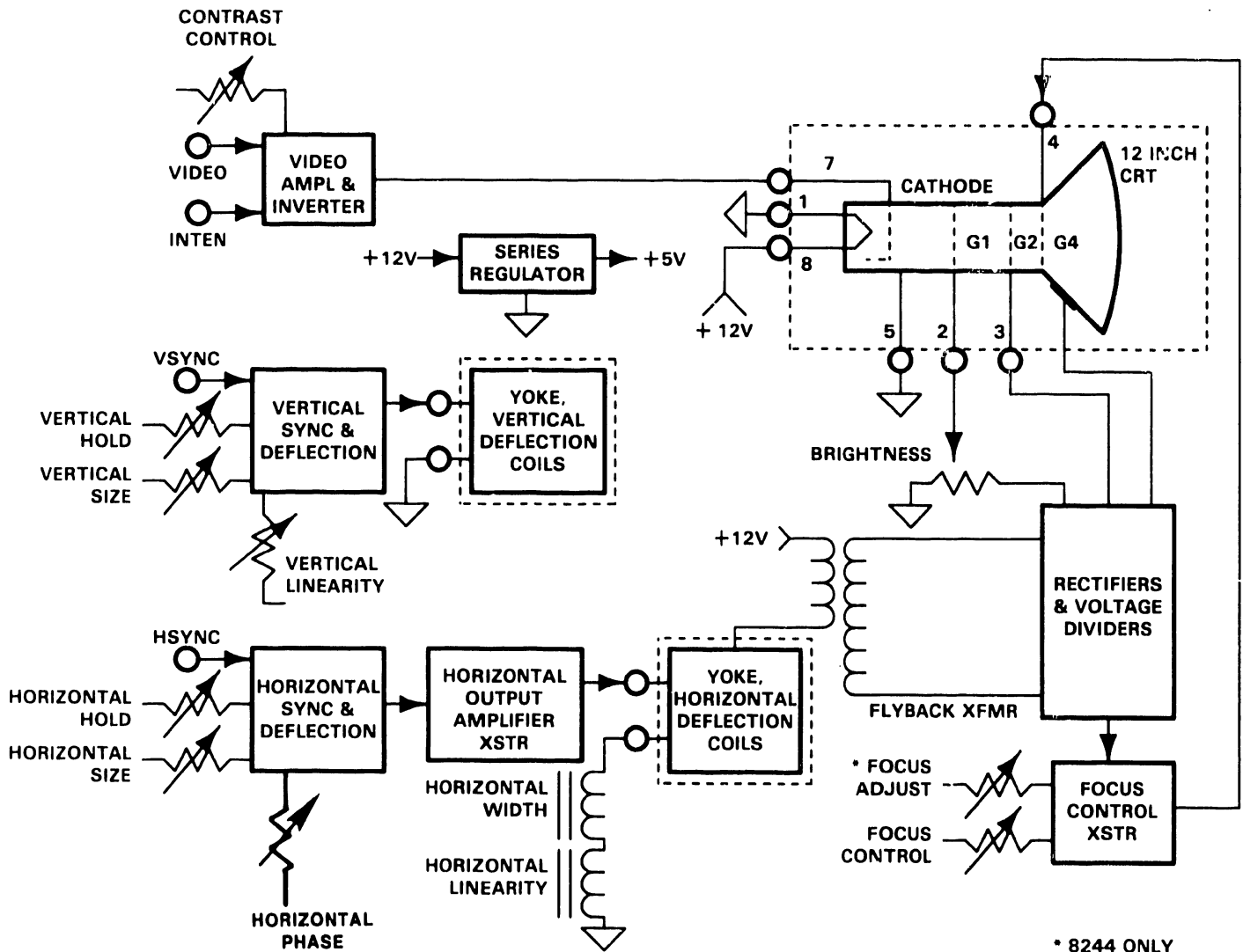
2.1 MONITOR

The Monitor unit (figure 2-1) contains a 12-inch green-on-black CRT with a Monitor PCA to process video and synchronization signals. The CRT screen has a capacity of 25 lines with 80 characters per line for a total of 2000 characters displayed.

The Monitor PCA receives +12 Vdc from the switching power supply in the Electronics Base via one lead of the Monitor power cable assembly. The +12 Vdc directly supplies the higher current horizontal deflection circuitry and the CRT filament. A series regulator is used to derive a +5 Vdc supply from the +12 Vdc input for the logic devices on the Monitor PCA.

Input signals to the Monitor PCA include VIDEO, HSYNC, VSYNC and INTEN which are generated in the Electronics Base of the particular model Workstation. These signals are applied to the Monitor PCA via the eight-pin monitor video cable, buffered and then presented to the appropriate circuits on the PCA.

2.1 MONITOR (Continued)



* 8244 ONLY

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Figure 2-1. Monitor PCA Block Diagram

2.1 MONITOR (Continued)

The VIDEO input is applied to a common-emitter stage in the video amplifier and inverter which provides amplification and inversion of the incoming video signal. The amplified and inverted video drives the cathode of the 12-inch (diagonal) CRT. A special portion of the video amplifier and inverter receives the INTEN signal, which is used to intensify or highlight selected characters on the CRT screen. The INTEN signal causes the CRT cathode voltage to decrease, causing an increase in intensity for the instant that the INTEN signal is present. The front-panel contrast control adjusts the extent to which the circuit reacts to the INTEN signal.

The horizontal sync (HSYNC) input is applied to the horizontal sync and deflection circuitry, comprising a horizontal processor device followed by a driver and, finally, the horizontal output amplifier. The horizontal phase and horizontal hold adjustments are inputs to the horizontal sync and deflection device and provide for a phase and frequency-stable horizontal deflection ramp to be fed to the output stage.

The horizontal output transistor feeds the horizontal deflection coils of the yoke with a saw-tooth-type deflection waveform. The current in the yoke windings develops an electro-magnetic field for deflecting the CRT electron beam in the horizontal direction. Adjustments for horizontal width and horizontal linearity form part of the total horizontal deflection coil load.

2.1 MONITOR (Continued)

At horizontal retrace (flyback), the current field in the horizontal deflection coils of the yoke collapses and the resultant energy is stepped up by the flyback transformer. On the secondary side of the flyback transformer are separate windings which feed diode rectifiers and associated voltage divider circuits. Anode operating potential, focus (G4), G1 and G2 voltages are all derived from these rectifier and voltage divider circuits.

The vertical sync (VSYNC) input is applied to the vertical sync and deflection circuitry. Vertical processing is performed wholly by a vertical processor device which develops the final vertical sawtooth waveform that drives the vertical deflection coils of the yoke. Vertical hold, vertical size and vertical linearity adjustments are all inputs to the vertical sync and deflection device.

2.2 KEYBOARD

This section provides an overview of Keyboard operations as well as a functional block diagram level of theory discussion.

2.2.1 KEYBOARD OVERVIEW

The detached Keyboard contains a dedicated 8031 microprocessor that accepts commands from the Z-80 in the Electronics Base while sending both Keyboard status data and keystroke data back to the Z-80. This communication occurs between the serial I/O port of the 8031 in the Keyboard and another 8031 located in the Electronics Base. The Keyboard communicates in a full-duplex mode.

Pressing a key causes the Keyboard to send a 7-bit keystroke code to the Z-80 in the Electronics Base. Every key has its own unique keystroke code, which is arbitrary and bears no relationship to any of the various character codes. In addition to the keystroke codes produced when they are pressed, the left and right SHIFT keys also generate different codes, called release codes, when they are released.

The release code for any key is identical to its keystroke code, but with high-order bit 7 set (i.e., keystroke code plus '80'). Special Keyboard commands establish release codes for up to five other designated keys or, alternately, for all of the keys on the Keyboard.

2.2 KEYBOARD (Continued)

2.2.1 KEYBOARD OVERVIEW (Continued)

The LOCK and SHIFT keys have transmittable codes that allow maximum flexibility at the host system. The LOCK key has an LED (bit 0) for a visual indication that the key is engaged. The host system decodes the LOCK key transmittal code and returns a code back to the Keyboard through the 8031 to light the LOCK LED.

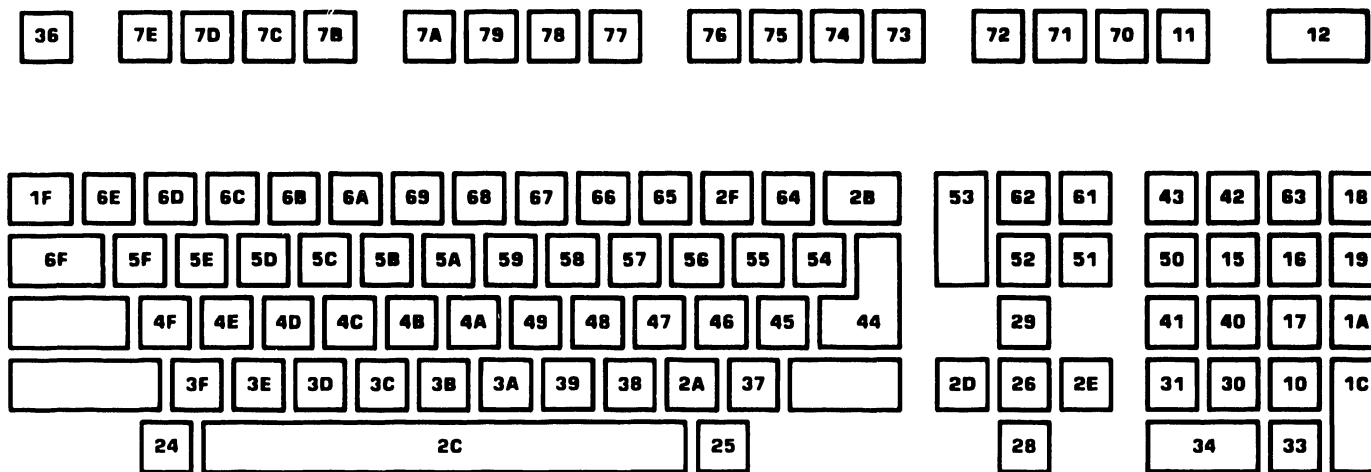
The left and right SHIFT keys have make and break codes in the Keyboard default scheme. When either SHIFT key is depressed, it will transmit its own X/Y code (make code). When the SHIFT key is released, a break code will be transmitted. When a shift condition is sensed, the host system will append an '80' bit to all keys until it sees the break code for the shift key.

Any key on the Keyboard is a potential repeat key. If the Keyboard is programmed to generate a release code for a particular key, the Z-80 in the Electronics Base can assume that the key remains down (or pressed) between the time it receives the keystroke code and the time it receives the corresponding release code. Therefore, when a program that is monitoring the Keyboard recognizes a pressed key in this way, it can decide whether the key will repeat, and at what rate.

2.2 KEYBOARD (Continued)

2.2.1 KEYBOARD OVERVIEW (Continued)

Figure 2-2 shows keystroke code assignments for the standard Keyboard. There are some possible keystroke codes and their corresponding release codes that are not produced by any key.



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Figure 2-2. Keycode Assignments

2.2 KEYBOARD (Continued)

2.2.1 KEYBOARD OVERVIEW (Continued)

One of these, code '01', is used as a query response byte, which is always followed by one or more status bytes. When the Z-80 makes an inquiry by sending one of the query control byte sequences, it continues accepting Keyboard input until it receives the '01' query response byte and then accepts the appropriate number of status bytes before resuming normal Keyboard input.

A 4-conductor cable fitted with a 4-pin DIN connector carries power and interface signals between the Keyboard interface and the detached Keyboard. The Keyboard connector and 4-pin DIN connector signals are shown below.

<u>CONNECTOR</u> <u>PIN NO.</u>	<u>DIN PLUG</u> <u>PIN NO.</u>	<u>SIGNAL</u>
1	N/C	Negative lead to speaker
2		Positive lead to speaker
3	1	Ground
4	2	Data output to Keyboard
5	4	5 Vdc power
6	3	Data input from Keyboard

LED control commands are used to turn on individual LEDs as well as turn on and turn off all LEDs. The Keyboard LEDs are used to indicate diagnostic errors. The LED status command allows the host system to read the LED status at any time. The Keyboard is initialized with all LEDs off.

2.2 KEYBOARD (Continued)

2.2.1 KEYBOARD OVERVIEW (Continued)

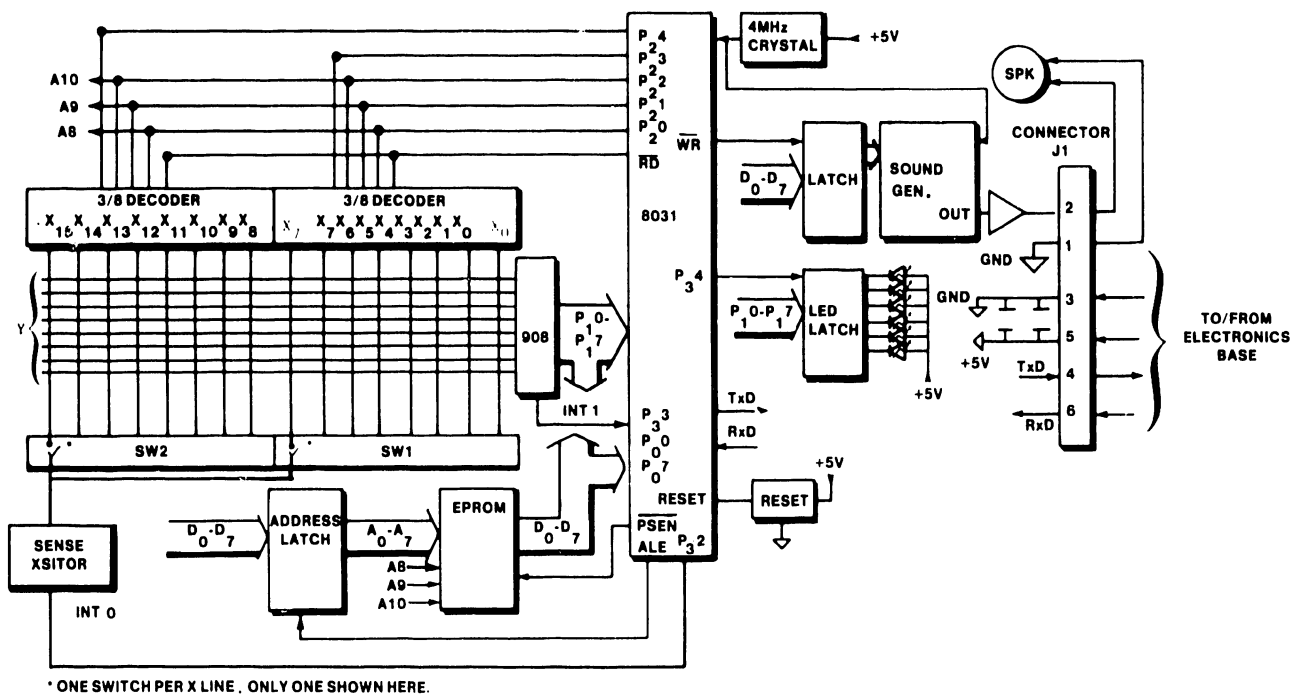
N-key rollover exists between all encoded keys on the Keyboard. Therefore, when a key is depressed while other keys are held down, the Keyboard will be able to output the latest keycode. Two 8-bit switchbanks on the Keyboard identify the particular Keyboard configuration.

The Keyboard interface in the Electronics Base is designed around an 8031 microprocessor with a full duplex serial port UART operating at 62.5k baud. On power-up or system reset, hardware initializes the 8031 to transmit and receive serial protocol that consists of one start bit (cleared to zero), an 8-bit data word (least significant bit first), and two stop bits (set to one), without parity.

2.2 KEYBOARD (Continued)

2.2.2 KEYBOARD THEORY OF OPERATION

Refer to Figure 2-3 for the following discussion.



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Figure 2-3. Low-Profile Serial Keyboard Block Diagram

2.2 KEYBOARD (Continued)

2.2.2 KEYBOARD THEORY OF OPERATION (Continued)

The 8031 device is a single-component 8-bit microprocessor that contains 128 x 8-bit internal RAM memory, an internal oscillator and timing circuit for data synchronization, and a full duplex serial port UART. The 8031 device requires one supply voltage (+5 volts) for operation. Keyboard data is either sent or received across the full-duplex Keyboard interface.

A 4 MHz crystal-generated clock is used for the synchronization of the 8031 to the various other components located on the board. This clock is necessary since only power and data are transmitted from the Electronics Base.

The 8031 uses its port zero lines as both the data and the address bus in a multiplexed bus scheme. Lines D0 - D7 identify the shared bus. Signal ALE (address latch enable) enables the address latch when the bus is in the address mode, thus storing an address in the latch. The address latch addresses the EPROM while signal PSEN (program store enable) enables the EPROM to read the instruction at that address onto the bus, which is now in the data mode. The EPROM stores the operational routines for the 8031.

2.2 KEYBOARD (Continued)

2.2.2 KEYBOARD THEORY OF OPERATION (Continued)

At power-up, the reset circuit sets the 8031 program counter to zero and the 8031 starts executing its initialization code from the EPROM. The initialization routine performs the following tasks:

1. Configure internal UART to 62.5k baud
2. Configure line protocol (1 start bit, 8 data bits, 2 stop bits)
3. Load zeros to sound generator
4. Clear LEDs
5. Set up two internal timers

After initialization, the 8031 starts its X axis scan routine, continuously polling port 1 for an input from the X/Y matrix. The Keyboard keys are laid out in a 16 x 8 X/Y matrix for a total of 128 possible configurations. Not all possible configurations are used. The 8031 supplies three scan lines (A8, A9, A10) to the two 3-to-8 decoders. The three scan lines count in binary from zero to 7 for each of the two decoders, thus causing a strobe to occur sequentially from X_0 to X_{15} .

The Y lines in the matrix are the return lines to the 908 device. When a key is pressed, the capacitive reactance is sensed by the 908 device and the device translates the sense to a TTL level for the 8031. Upon receipt of the input from the 908, the 8031 reads the 908 input again to confirm the original read.

2.2 KEYBOARD (Continued)

2.2.2 KEYBOARD THEORY OF OPERATION (Continued)

The 8031 now looks in an internal table for the keycode that matches the Y location from the 908 device and the X location from the 3-to-8 decoders.

The keycode is then sent to the 8031's internal UART where it is serialized. A start bit and two stop bits are added and the serial stream is transmitted to the Electronics Base. After transmission of the last bit in the stream, the 8031 UART generates an internal interrupt which causes the 8031 to resume its X axis scanning routine.

The X portion of the X/Y matrix also serves to read the settings of the two on-board switch-banks. One side of each switch is connected to one of the X lines. Each X line is normally pulled up to 5V. The other side of each switch is connected to one common transistor. When an X line is strobed (brought low) and its switch is closed, the strobe is coupled through the switch to the transistor and the transistor changes state.

This pulse is applied to the 8031 as an interrupt at P3.2, and the 8031 registers the switch closure in an internal register dedicated to holding the switch settings. When an X line is strobed (brought low) and its switch is open, the transistor is unaffected and no interrupt occurs.

2.2 KEYBOARD (Continued)

2.2.2 KEYBOARD THEORY OF OPERATION (Continued)

The switch setting scan routine occurs after each X/Y matrix read routine. The switch settings can be read from the 8031's internal register anytime the Z-80 in the Electronics Base issues a query command.

Communication from the Z-80 in the Electronics Base to the 8031 in the Keyboard occurs as follows. The command to the Keyboard is received by the 8031's internal UART, the start and stop bits are stripped and the command is looked up in a table in the 8031. The starting address of the routine associated with that command is put on the address bus, and the 8031 executes code from the EPROM to satisfy the particular routine.

The six LEDs located on the Keyboard PCB are under the control of the Z-80 CPU in the Electronics Base. The Z-80 CPU sends LED data serially to the 8031 in the Keyboard. The 8031 strips the start and stop bits and converts the serial data to parallel data. The LED data is then placed on port zero lines P0.0 - P0.7 and latched in the tri-state LED latch. The 8031 enables the LED latch, thus driving the LEDs with the data from the Z-80 in the Electronics Base. Any low output from the LED latch will illuminate the associated LED.

A programmable sound generator device provides the Keyboard with its beep and click sounds.

2.2 KEYBOARD (Continued)

2.2.2 KEYBOARD THEORY OF OPERATION (Continued)

Upon receipt of a beep or click command from the Z-80 in the Electronics Base, the associated routine is called from the EPROM.

The 8031 receives the appropriate data for the sound generator from the EPROM. This includes the data required to load the sound generator's attenuation and frequency registers to produce the desired sound. The data is latched from the data bus and then applied to the sound generator. A common operational amplifier is used to drive the speaker.

2.3 4230/4205 ELECTRONICS BASE

The standard 4230/4205 Electronics Base with no options houses one PCA which carries out all logic functions of the workstation. This PCA is referred to as the 4230 Workstation Electronics PCA, part number 210-8287, or the 4205 Workstation Electronics PCA, part number 210-8287-1. These PCAs are referred to in this section simply as the 8287 PCA. The information contained in this section is applicable to both the 4230 and the 4205 Workstation Electronics PCA except where specifically noted.

Figure 2-4 is a functional representation of the single PCA workstation.

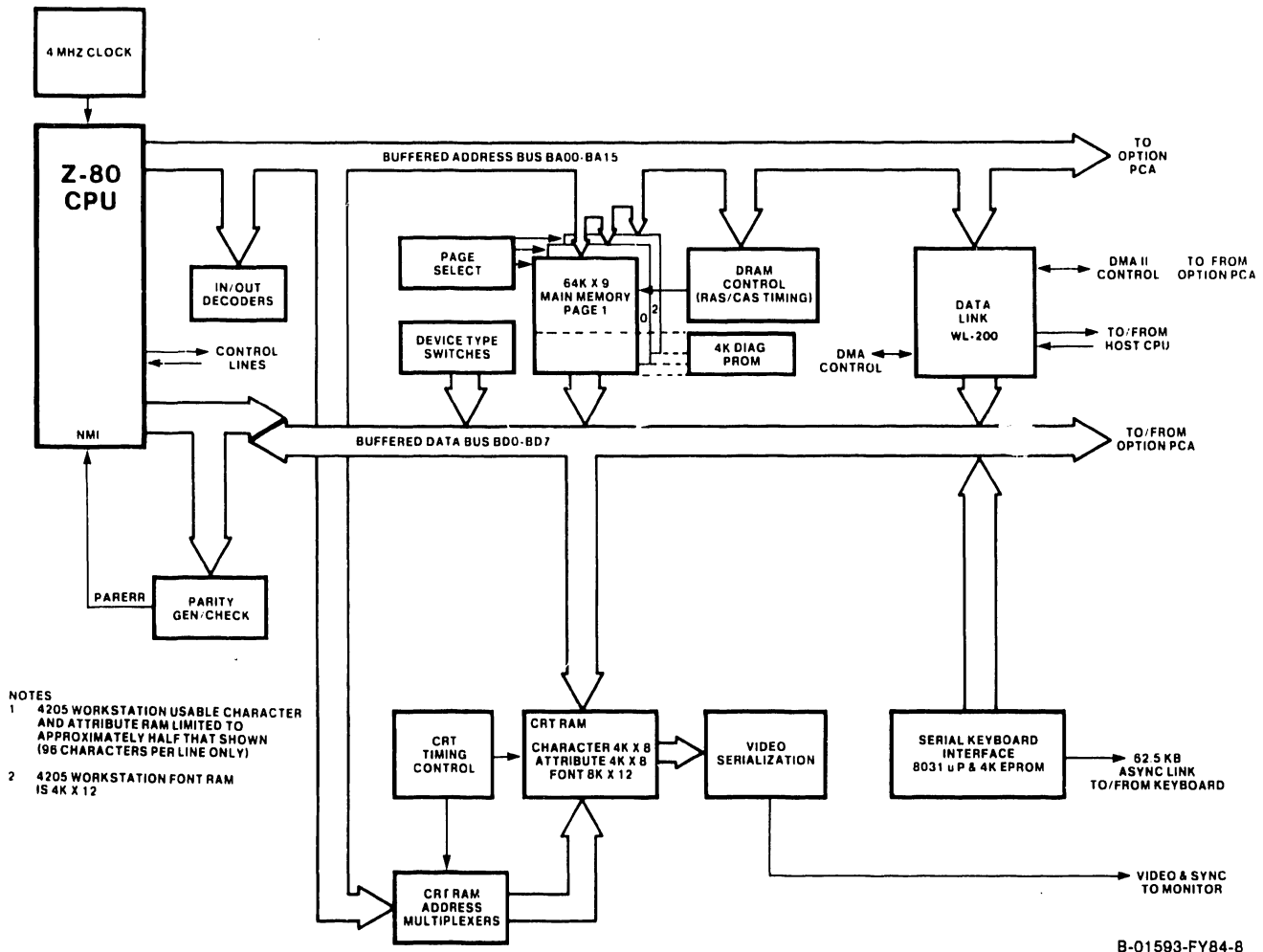


Figure 2-4. 4230/4205 Workstation
Functional Block Diagram

2.3 4230/4205 ELECTRONICS BASE (Continued)

2.3.1 210-8287 CPU PCA

The 8287 CPU PCA contains three LSI (large scale integration) devices and their support logic, thus providing all logic required for workstation operation on a single board. The LSI devices are a Z-80 CPU, an 8031 microprocessor for the serial keyboard interface and a WL-2001 device which provides all the functions of a standard Wang 928 data link in a single LSI device.

Support logic for these main LSI devices includes 64k bytes of main memory with parity, a 4k PROM containing the Built-In Test (BIT) power-up diagnostic, and CRT RAM including 4k of character RAM, 4k of attribute RAM and 8k of font RAM. (The 4205 has only 4K of font RAM.) Another 4k PROM stores the operating program for the 8031 microprocessor.

The connector header mounted on the rear of the PCA contains the DATA LINK BNC/TNC connectors for cable connection to the host CPU as well as the connectors for the Monitor and Keyboard.

2.3.1.1 Z-80 Central Processor Unit (CPU)

Bus operations are controlled by the Z-80A CPU. The CPU receives sequential instructions from main memory over the data bus. It assigns device access and tasks based on these instructions and communicates with workstation logic through the data, address, and control buses.

2.3.1 210-8287 CPU PCA (Continued)

2.3.1.1 Z-80 Central Processor Unit (CPU)
(Continued)

CPU signals are sequenced according to both its internal instruction set and instructions received from main memory over the data bus. The CPU requires a single, +5 Vdc supply and employs a 4 MHz clock as its time base.

Bidirectional data flow is accomplished by an 8-bit, tri-state data bus. The CPU transmits address information over a 16-bit, tri-state address bus. A reset line initializes the CPU and the six control-output lines. The six control-output lines are:

M1, CPU Fetch Cycle: This line is active during the first cycle (fetch cycle) of each instruction-request cycle, and during the special interrupt cycles.

MREQ, Memory Request: Active when the address bus holds a valid address for a memory read or write operation.

IORQ, Input/Output Request: Active when the lower half of the address bus holds a valid I/O address for an I/O read or write operation. Also becomes active for the interrupt acknowledge cycle.

RD, Read: When active, indicates that the CPU will input data while performing a memory-access or I/O instruction.

2.3.1 210-8287 CPU PCA (Continued)

2.3.1.1 Z-80 Central Processor Unit (CPU)
(Continued)

WR, Write: When active, indicates that the CPU will output data while performing a memory-access or I/O instruction.

RFSH, Refresh: During an M1 (memory period 1) cycle, the CPU outputs an address for memory refresh. RFSH confirms the active presence of that address.

In addition to the control-output lines, there are three CPU input control lines. These lines are:

BUSRQ, Bus Request: An outside device can request bus access by asserting this signal. BUSRQ input causes the CPU to switch its address, data, and status lines into a high-impedance state to accommodate the outside device.

BUSAK, Bus Acknowledge: Becomes active to indicate that the CPU has complied with a BUSRQ.

WAIT: An outside device can request the CPU to extend the current memory access or I/O cycle by asserting this signal. The CPU waits as long as the signal remains asserted.

2.3.1.2 CPU Interrupts

The workstation employs Z-80 interrupt mode 0. In this mode, the CPU receives its next instruction from the interrupting device.

2.3.1 210-8287 CPU PCA (Continued)

2.3.1.2 CPU Interrupts (Continued)

The workstation employs Z-80 interrupt mode 0. In this mode, the CPU receives its next instruction from the interrupting device. In the 4230/4205 Workstation, interrupts are received from the 8031 processor used for the Keyboard interface. The interrupt notifies the CPU that a keystroke has been received and is ready for processing.

Two interrupt inputs to the CPU are provided, maskable (INT) and nonmaskable (NMI). Keystroke interrupts are of the maskable type, while a non-maskable interrupt (unconditional entrance to the program) occurs only for a detected memory parity error.

2.3.1.3 Main Memory

Main memory consists of 64k bytes of dynamic RAM with one bit of parity for each byte of memory. Physically, memory is implemented with nine 64k x 1-bit devices. Main RAM can be accessed by both the CPU and the data link. (The data link is a DMA path.) The DRAM controller is responsible for generating row address strobe (RAS) and column address strobe (CAS) logic to address main memory. RAS and CAS lines enable 16-bit addresses to be processed in 8-bit, half-address form, permitting 16-bit main memory addresses to dynamic RAM devices with only eight address input pins.

2.3.1 210-8287 CPU PCA (Continued)

2.3.1.3 Main Memory (Continued)

RAS/CAS logic transfers high and low-order address bits through the same device pins at different times.

RAS/CAS cycles are required any time main memory is addressed. Main memory is addressed during these operations: CPU instruction fetch/refresh cycle, CPU data read, CPU data write and DMA transfer

2.3.1.4 Main Memory Parity Checking

Memory parity logic is one of two parity generation/detection circuits. The other circuit is part of the Data Link. Memory parity logic generates and then tests for even parity on all data transfers leaving or entering the CPU through the data bus. During a CPU write, each parity bit is calculated and stored in main memory.

The parity line is checked on each CPU read. If a memory parity error is detected, the diagnostic PROM is enabled and the CPU receives a non-maskable interrupt which causes it to jump to location '0066'. At that location in PROM is the main memory parity error routine which causes the contents of the CRT screen to be underlined, thus informing the operator of the error.

2.3.1 210-8287 CPU PCA (Continued)

2.3.1.4 Main Memory Parity Checking (Continued)

The underlining condition can be cleared only through a Z-80 RESET. In the 4230/4205, a RESET can be accomplished by cycling ac power to the workstation or, in some cases, by the host CPU.

Following workstation reset (restart), the diagnostic built-in test (BIT) runs and the usual power-up checks ensue. If the memory parity error was a soft error, the workstation will pass the BIT and be ready for operation again. During diagnostics, the parity detection circuitry itself is tested by forcing bad parity to be written and then reading back the same data location.

2.3.1.5 Address Assignments and Page Select Logic

The Z-80 CPU, with its 16 address lines, is capable of addressing up to 65,536 (64k) different memory locations. Many of the programs available on a host VS/OIS CPU require the full 64k of main memory within the 4230 workstation in order to run. Nevertheless, character, attribute and font memories comprise another large segment of memory that must be addressed as directed by CRT controlling routines within the workstation.

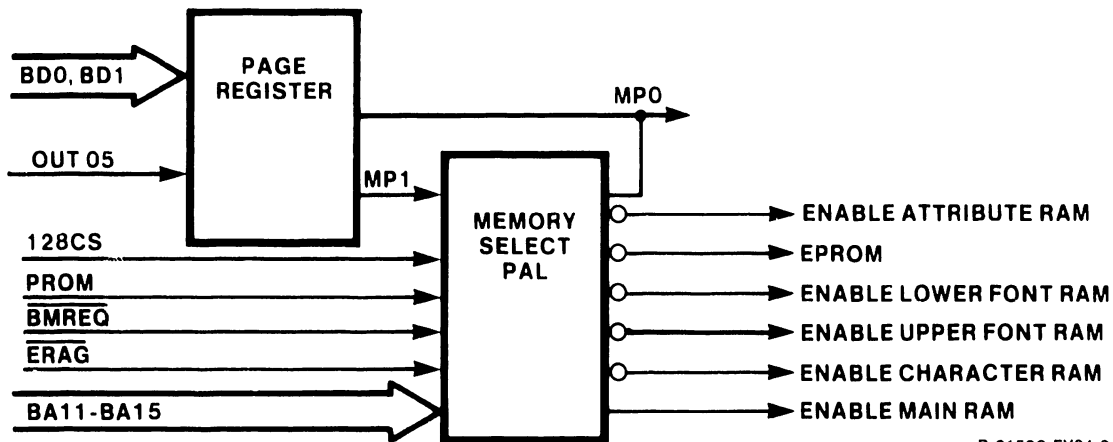
To overcome the limit placed upon the number of available addresses by the 16-bit address bus, a method of memory address assignments called page selection is used in the 4230/4205 Workstation.

2.3.1 210-8287 CPU PCA (Continued)

2.3.1.5 Address Assignments and Page Select Logic (Continued)

Page selection allows the same addresses to be assigned to more than one physical memory device. Thus, while both the main and CRT memories see the address lines from the CPU, only the memory that is enabled at the time responds to the current address on the bus.

Figure 2-5 is a simplified representation of the hardware used to implement the page select scheme. The central element in the page select hardware is the block memory decode PAL (programmable array of logic). The PAL is programmed to output the appropriate memory enables for the combination of inputs it receives. In the 4205, this PAL is programmed to inhibit main RAM addresses above 32k.



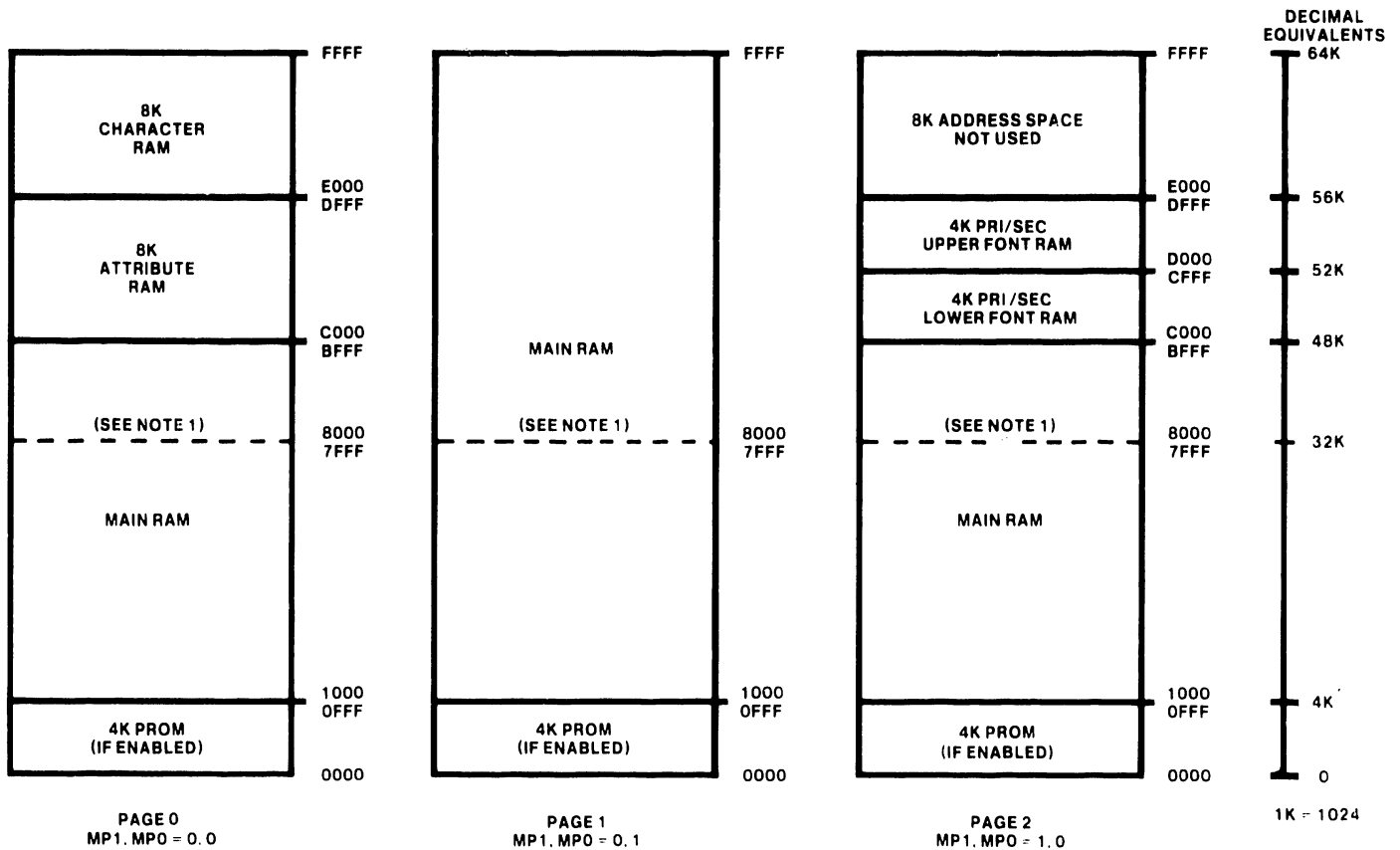
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Figure 2-5. 4230/4205 Workstation Memory Page Select Logic

2.3.1 210-8287 CPU PCA (Continued)

2.3.1.5 Address Assignments and Page Select Logic (Continued)

The available addresses are assigned differently for each of three pages available to the CPU for selection. The three pages and their address assignments are shown in Figure 2-6.



NOTES:
1. 4205 WORKSTATION MAIN MEMORY ADDRESSES ARE LIMITED TO 32K.

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Figure 2-6. 4230/4205 Workstation Memory Addressing Assignments

2.3.1 210-8287 CPU PCA (Continued)

2.3.1.5 Address Assignments and Page Select
Logic (Continued)

The inputs to the PAL are listed below with a description of their function in the page selection scheme. Table 2-1 shows how the different inputs combine to decode blocks of memory addresses.

Table 2-1 Block Memory Decoding

CONDITIONS REQUIRED											
MEM. ADDRESSED	EPR0M	MP1	MPO	128CS	ADDRESS	A15	A14	A13	A12	A11	A10-A0
EPR0M	1	x	x	x	0K4K	0	0	0	0	x	x
CHARACTER RAM	x	0	0	x	56K-64K	1	1	1	x	x	x
ATTRIBUTE RAM	x	0	0	x	48K-56K	1	1	0	x	x	x
LOWER FONT RAM	x	1	0	0	48K-52K	1	1	0	0	x	x
LOWER FONT RAM	x	1	0	1	48K-50K	1	1	0	0	0	x
UPPER FONT RAM	x	1	0	0	52K-56K	1	1	0	1	x	x
UPPER FONT RAM	x	1	0	1	52K-54K	1	1	0	1	0	x
MAIN RAM	0	x	x	x	0K4K	0	0	0	0	x	x
MAIN RAM	x	x	x	x	4K8K	0	0	0	1	x	x
MAIN RAM	x	x	x	x	8K-16K	0	0	1	x	x	x
MAIN RAM	x	x	x	x	16K-32K	0	1	x	x	x	x
MAIN RAM	x	x	x	x	32K-48K	1	0	x	x	x	x
MAIN RAM	x	x	1	x	48K-64K	1	1	x	x	x	x

Notes:

1. x = don't care
2. Main RAM addresses above 32k are inhibited in the 4205 Workstation.
3. The 4205 has only 4k of font memory versus 8k in the 4230.

2.3.1 210-8287 CPU PCA (Continued)

2.3.1.5 Address Assignments and Page Select
Logic (Continued)

MP0, MP1: The Z-80 CPU selects the appropriate page configuration (page 0, 1, 2) required for any operation by writing to the page register. Command OUT '05' clocks page select data off the data bus (BD0, BD1) and into the page register. The resultant lines MP0 and MP1 (MP = memory page) are used as inputs to the memory select PAL.

PROM: An active PROM bit disables the lower 4k of workstation main memory and enables the 4k diagnostic PROM. All write cycles to the lower 4k of memory addresses are inhibited. All read cycles are called from the PROM regardless of what page is indicated by the page register.

128CS: An active 128 character set bit inhibits all memory cycles to the upper 2k of the lower and the upper font memory. The font memory can contain two 256 character sets, requiring the total 4k lower font memory and 4k upper font memory. If a 128 character set is selected, however, this bit is used to prevent memory accesses outside of the selected character set.

BA11 - BA15: Address bits BA11 - BA15 determine which 4k block within the current page is to be accessed.

The memory request signal (BMREQ) and the eight-bit refresh generator signal (ERAG) from the Z-80 are also applied to the PAL for synchronizing its memory enable outputs.

2.3.1 210-8287 CPU PCA (Continued)

2.3.1.6 Programmable Read-Only Memory (PROM)

At power-up, the CPU executes code from the diagnostic PROM which is selected by the block memory decode logic. Sequential testing of different groups of logic is performed to verify the integrity of the workstation. During this phase, the data link is disabled. Upon successful completion of the tests, PROM is deselected and the data link is enabled. At this point, conventional data link downloading commences as though the workstation had just been powered-up.

2.3.1.7 I/O Decoders

The Z-80 uses IN and OUT instructions to transfer data to and from input/output devices. The Z-80 design allows for 256 discrete I/O ports to be assigned using the eight least significant bits of the address bus (A0 - A7). An active IORQ from the CPU indicates that a valid I/O address is present on the lower half of the address bus. The I/O decoders decode these address lines to provide single chip enable lines for each I/O address.

2.3.1 210-8287 CPU PCA (Continued)

2.3.1.7 I/O Decoders (Continued)

The I/O port assignments for the 4230/4205 workstation are shown in Table 2-2.

Table 2-2 4230/4205 Workstation Input/Output Commands

COMMAND	DESCRIPTION
OUT00	Sounds Keyboard Clicker
OUT01	Sounds Keyboard Speaker
OUT02	Loads data into start column register
OUT05	Loads data into page register
OUT06	Selects primary character set
OUT07	Selects secondary character set
OUT09	Selects normal or reverse video
OUT0E	Diagnostic use
OUT10	TC Loopback Enable/Disable (4230 TC only)
OUT11	Sets TC baud rate (4230 TC only)
OUT12	Clears key pending interrupt (4230 TC only)
OUT13	Clears 10 msec interrupt (4230 TC only)
OUT14	Selects TC clock mode and sets/clears secondary RTS (4230 TC only)
OUT15	Writes data to USART (4230 TC only)
OUT16	Disables TC interrupts (4230 TC only)
OUT17	Enables TC interrupts (4230 TC only)
OUT20	Selects 256 or 128 character set
OUT21	Selects/deselects Arabic mode
OUT25	Writes commands to Keyboard
OUT35	Writes command or control information to USART (4230 TC only)
IN00	Reads serial Keyboard keystroke data
IN02	Reads TC status register (4230 TC only)
IN03	Reads interrupt status register (4230 TC only)
IN04	Reads installation status switches (4230 TC only)
IN07	Reads device type switch
IN08	Reads device type switch
IN15	Reads data from USART (4230 TC only)
IN35	Reads status from USART (4230 TC only)

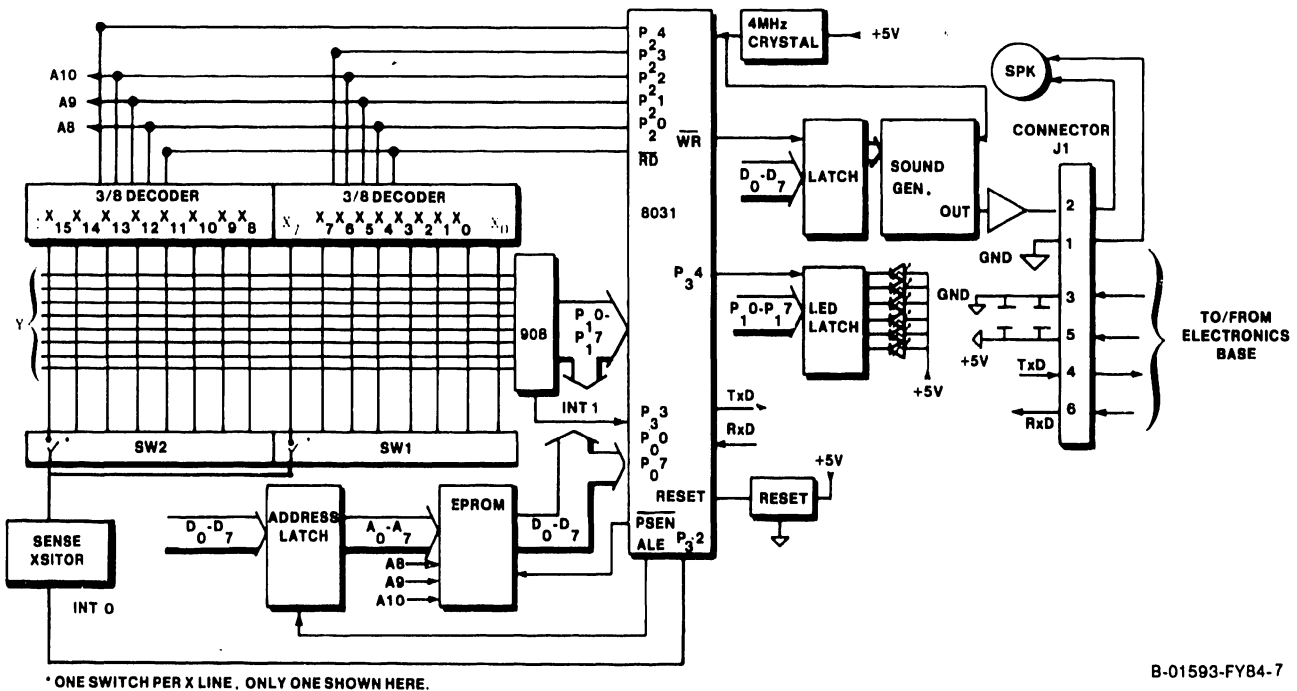
2.3.1 210-8287 CPU PCA (Continued)

2.3.1.8 Data Link

The 4230/4205 Workstation employs a recently introduced LSI device, the WL-2001, to carry out the standard Wang 928 data link functions.

The data link permits workstation memory to be loaded or read by the host CPU. The host CPU can write new memory instructions into workstation memory; it can also record (archive) information entered by the workstation onto a common disk. The workstation CPU is disabled when the host CPU uses the Data Link. During this time, the data link device provides bus synchronization and timing for direct memory access (DMA) read/write operations into and out of workstation main memory. DMA logic does not support CRT memory transfers.

The data link (Figure 2-7) permits the host CPU to transfer data at high speed between its main memory (or disk) and main memory in its peripheral subsystems.



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Figure 2-7. Data Link Device and Support Logic

2.3.1.8 Data Link (Continued)

In particular, the host CPU uses this link to load programs into workstations, store documents produced at workstations, and to feed high-speed printers. Each workstation is connected to the host CPU separately, through a radial bus structure. All transmissions are controlled by the host CPU.

Data is transferred directly between memories using a DMA path through the data link. Data transfer is carried out in a serial, asynchronous, byte-oriented format using a half-duplex line. The transmission line itself is a balanced pair of coaxial cables operating at 4M baud. The actual data transfer rate is approximately 260k bytes per second.

2.3.1.8.1 Data Link Commands

Data link commands are received over the serial data link and processed by the WL-2001 device, thus carrying out the functions commanded by the host CPU. Six Data Link commands permit the host CPU to:

- Check Slave STATUS and ID
- Initiate Slave Operation (RESTART)
- Load Slave Memory (WRITE - 2 commands)
- Store Slave Data (READ - 2 commands)

2.3.1.8.1 Data Link Commands (Continued)

STATUS and ID Commands

STATUS and ID commands send Slave status and ID to the host CPU on command. The STATUS read is the method a host CPU uses to interrogate a slave. Upon receipt of this command, the WL-2001 reads the external status register to obtain this information. Eight bits of information are transmitted from the slave as shown and described below:

	MSB	LSB
	7 6 5 4 3 2 1 0	
Device Type	_____	
Memory PE	_____	
Receive Error	_____	
Not Ready	_____	

Not Ready: A high level indicates to the host CPU that the slave is not running.

Receive Error: A high level indicates to the host CPU that the slave has detected either a line parity error or line framing error (non-contiguous bytes in a message stream) during a transmission from the host CPU to the slave.

2.3.1.8.1 Data Link Commands (Continued)

Main Parity Error: A high level indicates the slave has detected a parity error in its own memory. In on-line applications, this bit would not be seen because the data link would be disabled, an NMI would occur and the CPU would read its memory parity routine from the diagnostic PROM.

Device Type: defines the type of slave on the data link.

RESTART Command

The RESTART command causes the WL-2001 to activate a signal (DLCL, data link clear) which can be used to reset the slave CPU. While this signal is not used in the 4230/4205 Workstation, the RESTART command is used to generate a data link restart command via the data link function lines. These lines, in turn, are decoded and a RESTART signal is applied to the power-up reset logic, thus causing a power-up reset of the workstation.

WRITE and READ Commands

WRITE and READ commands may each transfer either 1 byte or 256 bytes. A one-byte command transfers a single DMA cycle. A 256-byte command transfers a single page of data (1 page = 256 bytes).

2.3.1.8.1 Data Link Commands (Continued)

In response to any of the following commands, the WL-2001 device gains control of the Z-80 data, address and control lines via built-in DMA controls (see section 2.3.1.8.5).

1-Byte Read: This instruction is followed by two bytes indicating the address to be read from the slave's main memory. Address information is transferred to the slave (workstation) in half-address form, in order to accommodate 16-bit addresses on the 8-bit data link data bus. The WL-2001, upon latching the address, requests control of the Z-80 bus and then reads the appropriate memory location. This data is transmitted to the host CPU along the serial data link.

1-Byte Write: This instruction is similar to the 1-byte read (above), but the address is followed by a single byte of data. The data is stored in a WL-2001 internal register until memory access has been granted. The byte of data is then written into workstation main memory and the data link device returns to its receive state.

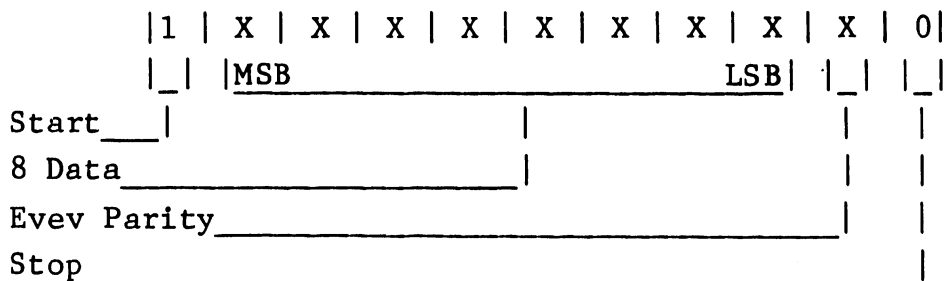
256-Byte Write: This instruction is followed by a starting address and then 256 bytes of data to be written sequentially into workstation main memory.

256-Byte Read: This instruction is followed by a starting address for a sequential memory transfer of 256 bytes of data from workstation main memory to the host CPU.

2.3.1.8.2 Data Link Receive Functions

The WL-2001 device receives commands and data via the balanced serial data link line from the host CPU. Data is first applied to a line receiver and then sent to the WL-2001 on the data link receive (DLR) line.

After power-up of the 4230/4205 Workstation, the WL-2001 idles in its receive mode, monitoring the data link receive input of the device. This means it is waiting for a command from the host CPU, which is indicated by the start bit of the 11-bit line protocol used in the data link. In total, the 11-bit stream looks as shown below.



The WL-2001 internal clock rate allows four clock cycles for each bit time. When it senses an active line (high) for two consecutive samples, a start bit is assumed to have been received and the device synchronizes itself internally so that the following data bits are sampled near their center. After the appropriate number of clock cycles have occurred for the 11-bit stream, the internal start bit detector is reset, thus allowing for variations in the transmission data rate on a byte-by-byte basis.

2.3.1.8.2 Data Link Receive Functions (Continued)

The sampled data bits are serially loaded into an 8-bit shift register inside the WL-2001. Together, the internal start bit detector and shift register function as an asynchronous receiver/transmitter to convert serial data to parallel data for use by the WL-2001 device. The received byte of data is either transferred to the internal instruction decoder or to an external register such as the low or high byte address register, or the data bus transceiver.

Internally, the WL-2001 checks received data for line parity and for framing errors. Parity is checked by calculating the parity bit for the data byte as it was received and comparing it to the parity bit sent with the data byte. If the two parity bits are not the same, the receive error (RE) line is activated.

Framing errors are gaps in the data stream. After a valid multiple byte instruction is received and the WL-2001 is expecting additional data bytes from the host CPU, a framing error will be indicated by the start bit detector being active for more than six clock samples, or 1.5 bit times. The receive error (RE) line is activated to indicate framing errors.

2.3.1.8.3 Data Link Transmit Functions

Data transmission from the WL-2001 to the host CPU is controlled by two lines, data link transmit enable (DLXEN) and data link transmit (DLT). When a transmission from the slave (workstation) to the host CPU is required, DLXEN is asserted while DLT is deactivated for a minimum of one byte time. During this one byte time, the appropriate external register is accessed (either status or data) and the data to be transmitted is loaded into the WL-2001.

The DLT line is then forced active for one bit time, thus forming the start bit of the line protocol for the host CPU. The WL-2001 internal shift register is loaded with the data to be transmitted and it is shifted serially to the DLT line, MSB first. After the 8-bit stream is shifted out, parity is appended and then a stop bit is sent. The parity bit sent to the host CPU is the main memory parity bit stored with that particular byte of data in the case of workstation main memory reads. Parity for all other data bytes is calculated within the WL-2001 and appended as the data is shifted out onto the line. If subsequent bytes of data are to be transmitted to the host CPU, they are loaded into the WL-2001 while the previous byte is being shifted out.

2.3.1.8.4 Line Turn-Around

Line turn-around control is also provided by the WL-2001 device, with two internal registers provided to set line turn-around delays. Line turn-around control ensures that the WL-2001 is ready to receive commands from the host CPU and also introduces a preset delay between transmit and receive operations on the half-duplex line. The delay allows the line to quiet between transmit and receive operations.

The interval from the reception of the last instruction or address byte from the host CPU to the beginning of a transmission to the host CPU is referred to as turn-around-time 1. Conversely, after the last byte has been transmitted to the host CPU, the interval until the start bit detector is reenabled is called turn-around-time 2. In the 4230/4205 Workstation, these turn-around times are preset to 8 and 7 microseconds respectively.

2.3.1.8.5 Direct Memory Access (DMA) and Z-80 Bus Arbitration

The WL-2001 provides a complete complement of control signals for direct memory accesses. All host CPU accesses to workstation main memory are DMA paths through the WL-2001 device. In addition, the device uses another set of control lines to allow any other devices to directly access workstation main memory. This additional DMA provision is referred to as a DMA2 operation.

2.3.1.8.5 Direct Memory Access (DMA) and Z-80 Bus Arbitration

In the 4230 Workstation, DMA2 accesses are used to support data transfers to and from the option PCA.

When either the host CPU or a DMA2 device requests a main memory access, the WL-2001 device generates a bus request signal which is forwarded to the Z-80 (slave) CPU. This signals the slave CPU that a DMA request is pending, and that it should give up control of its buses within 3.5 microseconds. The timing constraint ensures that the data and address buses will be free as soon as the incoming data byte arrives, since the WL-2001 provides no data buffering.

When the Z-80 CPU has placed its buses in the high impedance state, the WL-2001 is signaled with a bus acknowledge signal. When the WL-2001 senses bus acknowledge, and at the end of each DMA cycle, the device arbitrates between all bus requests to determine which request will be granted. The following priorities are observed:

1. Any memory operation in progress
2. Data link (host CPU) requests
3. DMA2 requests
4. Slave CPU operations

The WL-2001 provides the required memory interface signals during DMA operations including memory request and memory write (an inactive memory write indicates a read operation).

2.3.1.8.5 Direct Memory Access (DMA) and Z-80 Bus Arbitration

An additional signal, data valid, is used to signal the WL-2001 that valid data exists on the data bus or that write data has been latched. The data valid signal is generated in the DRAM control logic and applied to the WL-2001. Timing is such that, when the data valid line is active, the memory refresh function can be carried out (RAS-only memory cycle). Thus, in-between direct memory accesses, the DRAM is refreshed.

The DMA2 controls provide a means for devices other than the host or slave CPU to access workstation main memory. These controls are used in the 4230 Workstation to support data transfers to and from the option PCA. DMA2 accesses are single byte reads or writes only. The device requesting the DMA2 must provide a valid address (and data, in the case of a memory write) on the Z-80 (slave) data bus. DMA2 requests are granted only if no host CPU DMA requests are pending.

2.3.1.8.6 Data Link Functions and Function Decoding

A multiplexing scheme is used to transfer data in and out of the WL-2001 device. Data transfers occur over the 8-bit bidirectional data link data bus, DLDO - DLD7. A ninth line is used to transfer the main memory parity bit when reading from workstation main memory.

2.3.1.8 Data Link (Continued)2.3.1.8.6 Data Link Functions and Function
Decoding (Continued)

The data link data bus is connected to four registers, each serving to latch data from or drive data onto the bus. These registers are the status register, the data bus bidirectional transceiver, the high-byte address register and the low-byte address register.

The function and direction of the data on the data link data bus is under control of the data link function decode lines, DLFA - DLFD, providing up to 16 possible decoded commands. In the 4230/4205, three of these lines are decoded to provide six different commands used to control the four registers connected to the data link data bus. These commands are shown below.

<u>DLFD</u>	<u>DLFC</u>	<u>DLFB</u>	<u>DLFA</u>	<u>FUNCTION</u>
0	0	1	0	Latch Address High
0	0	1	1	Latch Address Low
0	0	0	1	Enable Write
0	1	0	1	Enable Read
0	1	0	0	Status Read
0	1	1	1	Data Link Restart

The first five of these lines are represented on the diagram in Figure 2-7 as control lines, acting as enables for the associated registers. The data bus transceiver requires both an enable and a direction control line. The sixth command is data link restart which is sent to the power-up reset logic.

2.3.1.8 Data Link (Continued)

2.3.1.8.6 Data Link Functions and Function
Decoding (Continued)

Upon decoding a data link restart, the 4230/4205 Workstation is forced into a power-up restart cycle, as if the unit had just been turned on.

2.3.1 210-8287 CPU PCA (Continued)

2.3.1.9 Serial Keyboard Interface

The serial keyboard interface to the Z-80 CPU uses an 8031 microprocessor, the same microprocessor used in the Keyboard itself. The 8031 device is a single-component, 8-bit microprocessor that contains 128 x 8-bit internal RAM, an internal oscillator and timing circuit for data synchronization, and a full duplex serial port UART. The 8031 device requires one supply voltage (+5 volts) for operation. A 4 MHz crystal-generated clock is used for synchronization. Keyboard data is either sent or received across the full-duplex Keyboard interface. (Refer to Figure 2-8.)

2.3.1.9.1 8031 Program Storage and Retrieval

The 8031 uses its port zero lines as both the data and the address bus in a multiplexed bus scheme. Lines P0.0 - P0.7 in Figure 2-8 identify the shared bus. Signal ALE (address latch enable) enables the address latch when the bus is in the address mode, thus storing an address in the latch.

2.3.1.9 Serial Keyboard Interface (Continued)

2.3.1.9.1 8031 Program Storage and Retrieval (Continued)

The address latch addresses the EPROM, along with additional address lines A8 - A11 from port 2 lines P2.0 - P2.3. Signal PSEN (program store enable) enables the EPROM to output the instruction at that address onto the bus, which is now in the data mode. The EPROM stores the operational routines for the 8031.

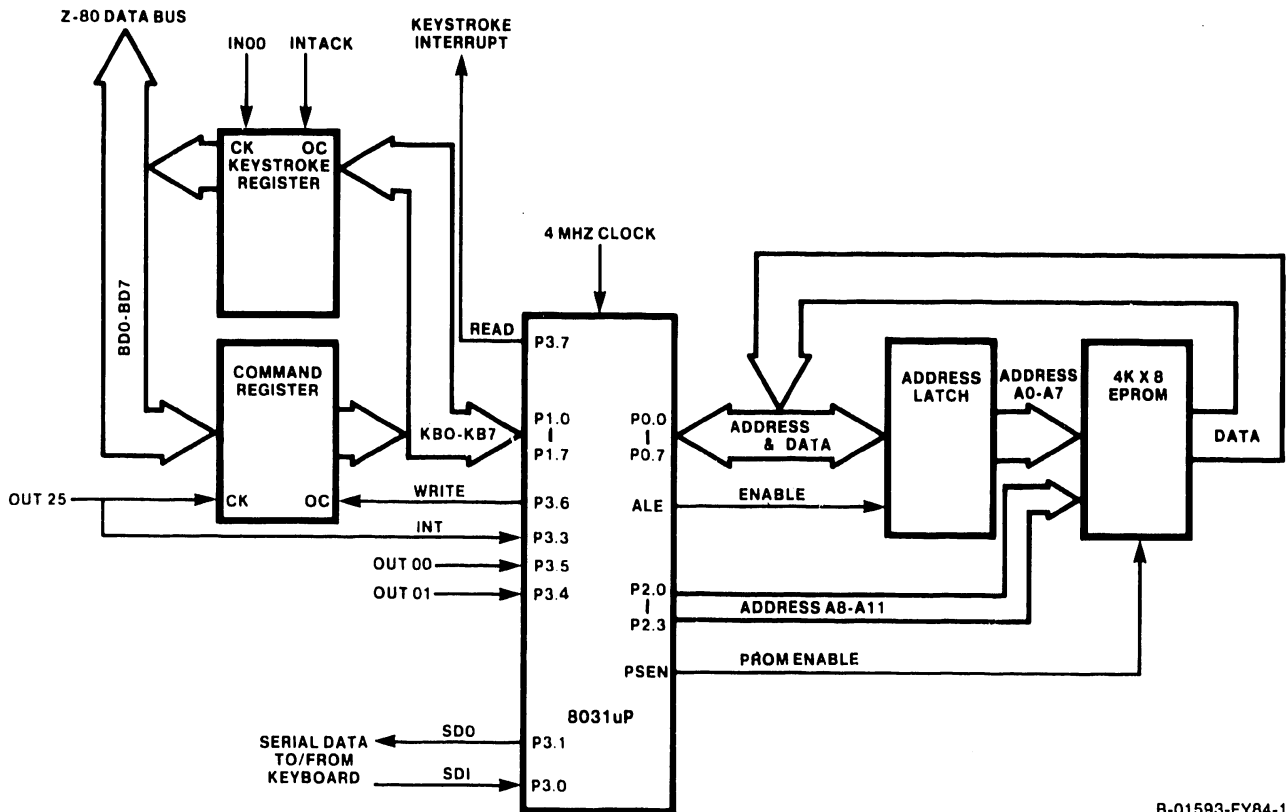


Figure 2-8. 4230/4205 WS Keyboard Interface

2.3.1.9 Serial Keyboard Interface (Continued)

2.3.1.9.2 Initialization (Continued)

At power-up, the 8031 is reset, thus setting the internal program counter to zero. The 8031 then starts executing its initialization code from the EPROM. The initialization routine configures the internal UART to 62.5k baud and sets line protocol to 1 start bit, 8 data bits and 2 stop bits. This matches the line protocol configured in the serial Keyboard.

2.3.1.9.3 Receiving Keystrokes

Upon receipt of a keystroke from the serial Keyboard (SDI, serial data in), the 8031 loads a restart instruction ('C7') into the keystroke register. Since the CPU is set for mode zero interrupts, the interrupting device must provide the CPU with the next instruction. This next instruction for the CPU is the restart instruction stored in the keystroke register.

After the restart instruction is loaded, a keystroke interrupt is issued by the 8031 to the Z-80 CPU. The CPU, in response to the keystroke interrupt, generates an interrupt acknowledge (INTACK) which reads the restart instruction from the keystroke register onto the data bus. The restart instruction loads the program counter in the CPU with the location of the keystroke servicing routine.

2.3.1.9 Serial Keyboard Interface (Continued)

2.3.1.9.3 Receiving Keystrokes (Continued)

During the time that the CPU is jumping to the keystroke routine, the 8031 loads the received keycode into the keystroke register. The CPU issues an IN '00' as part of the keystroke routine, which reads the keystroke onto the data bus for use by the CPU.

2.3.1.9.4 Transmitting Commands

The CPU can issue one-byte commands to the Keyboard via the 8031 interface, using the OUT '25' instruction. These commands are used for switching the Keyboard LEDs and a variety of other purposes detailed in the section on Keyboard theory of operation.

The one-byte command is loaded into the command register with the OUT '25' instruction. OUT '25' is also used as an interrupt for the 8031 to inform it of the pending command to be transmitted. The 8031 reads the command register onto its data bus using the write signal (P3.3), performs a parallel-to-serial conversion via its internal UART, appends the required start and stop bits and transmits the command to the Keyboard (SDO, serial data out).

2.3.1.9 Serial Keyboard Interface (Continued)

2.3.1.9.5 Beep and Click Functions

The Keyboard responds to every keystroke, legal or not in any particular software program, with either a beep or a click. Since these are high-usage, repetitive functions, the required routines to send beep and click commands to the Keyboard are stored in the 8031's EPROM. Instructions OUT '00' and OUT '01' call the click and beep routines (respectively) from the EPROM, causing the the associated keyboard commands to be transmitted to the Keyboard.

2.3.1.10 CRT RAM, Character Generation and CRT Display

A simplified representation of the CRT character generation and display circuits is shown in the block diagram of Figure 2-4 as four blocks, CRT timing control, CRT RAM address multiplexers, CRT RAM and video serialization. These blocks are expanded and shown in more detail in Figure 2-9, the CRT RAM addressing and character generation block diagram. Figure 2-9 is discussed in detail in the sections that follow.

2.3.1.10.1 Character RAM

The amount of RAM allocated for character storage is 4k bytes, or sufficient to store 25 rows of 160 characters or columns. (25 x 160 = 4000.) The CRT displays only 80 of these character columns at any time.

2.3.1.10 CRT RAM, Character Generation and CRT Display (Continued)

2.3.1.10.1 Character RAM (Continued)

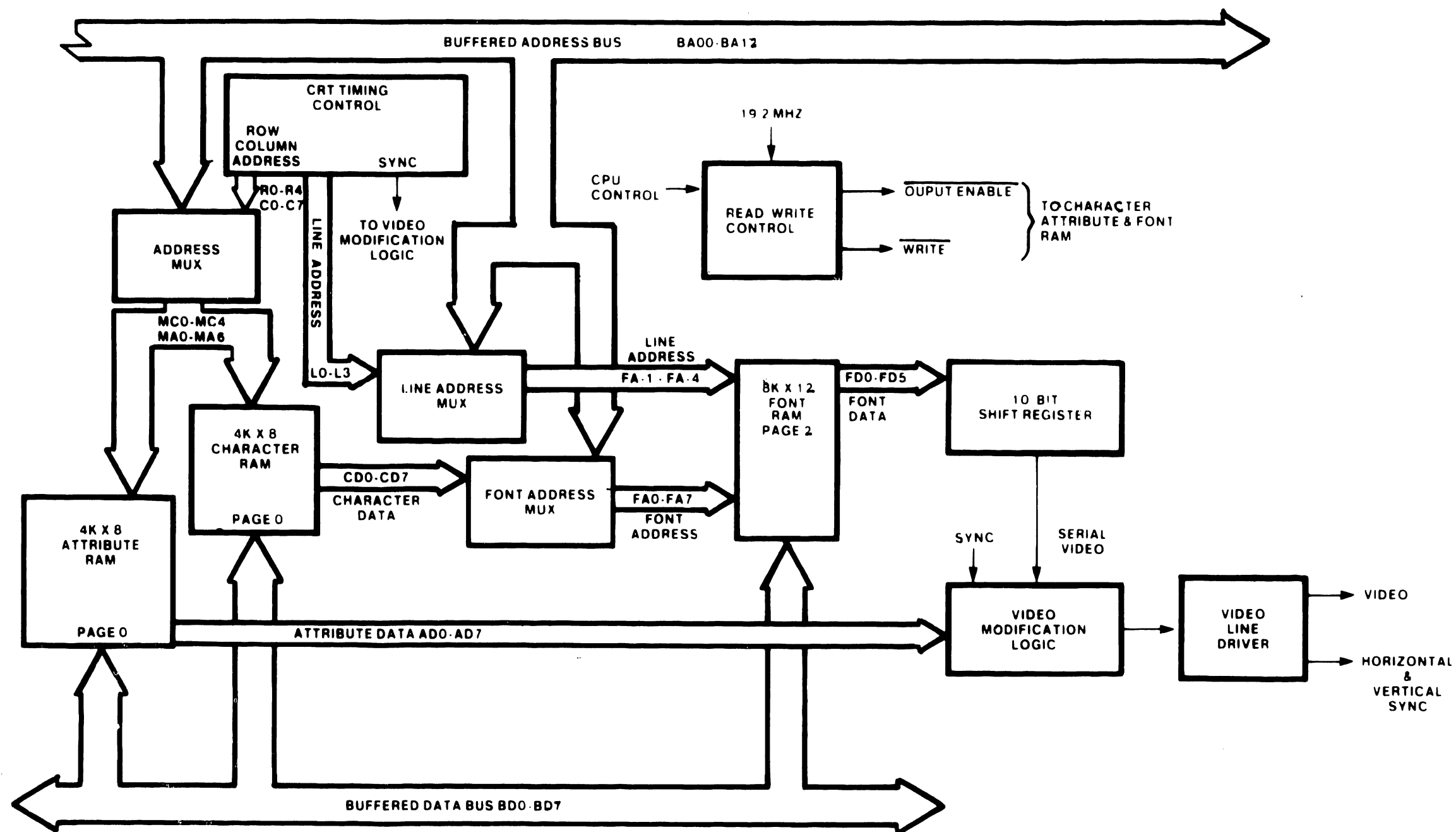
The remainder of the characters in memory can be displayed by exercising the horizontal scrolling capability of the workstation. The Z-80 CPU must enable page zero of its address assignments to access character RAM. Page zero allocates 8k of addresses for character memory, from 56 to 64k, though only 4k is used. In the 4205, character memory is limited to 96 characters per line.

The CPU addresses are multiplexed with the row and column addresses generated in the CRT timing control logic. The resulting address allows the CPU to select the three most significant bits of the address. When addressing character memory, it selects a starting address of 56k to coincide with the address assignments for character memory. The row and column addresses select which location in the next 4k of memory space will be used to store a particular character. The result of address multiplexing for the character RAM is shown below.

Z-80 Address	A15 A14 A13 A12 A11 A10 A09 A08
CRT Address	1 1 1 R04 R03 R02 R01 R00
	_____ _____
Selects 56k address range	_____ _____
Addresses rows 0 - 24	_____ _____

2.3.1.10 CRT RAM, Character Generation and CRT Display (Continued)

2.3.1.10.1 Character RAM (Continued)



NOTES

1 4205 WORKSTATION USABLE CHARACTER AND ATTRIBUTE RAM IS LIMITED TO APPROXIMATELY HALF THAT SHOWN (96 CHARACTERS PER LINE ONLY)

2 4205 WORKSTATION FONT RAM IS 4K X 12

B-01593-FY84-12

Figure 2-9. CRT RAM Addressing and Character Generation

2.3.1.10 CRT RAM, Character Generation and CRT Display (Continued)

2.3.1.10.1 Character RAM (Continued)

Z-80 Address	A07	A06	A05	A04	A03	A02	A01	A00
CRT Address	C07	C06	C05	C04	C03	C02	C01	C00
Addresses columns 0 - 159								

Character RAM is loaded by the CPU via the Z-80 bidirectional data bus, allowing the CPU to load an ASCII character code into each 8-bit location in character memory. These ASCII codes are used to generate font addresses in the font address multiplexer. The codes are transferred over lines CD0 - CD7. Read/write control for character RAM is generated in the read/write control logic.

2.3.1.10.2 Dot Matrix Display

Characters are formed on the CRT screen by a 16-line by 12-pixel matrix. ("Pixel" is short for "picture element" and is the smallest division of the CRT screen that can be displayed.)

2.3.1.10 CRT RAM, Character Generation and CRT Display (Continued)

2.3.1.10.2 Dot Matrix Display (Continued)

The CRT displays only 12 lines of 10 pixels per character as shown in Figure 2-10. Alphanumeric and special characters are created by illuminating a specific pattern of pixels within the matrix associated with each character position. A horizontal group of matrices form a character row. Twenty-five rows can be displayed on the CRT screen. Eighty character columns can be displayed in each character row.

		COLUMN 0										COLUMN 1										
		9	8	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0	PIXEL
S C A N L I N E	0																					
	1																					
	2		*							*			*		*		*					
	3			*					*			*							*			
	4				*		*					*									*	
	5					*						*										
	6				*		*					*				*		*		*		
	7		*					*				*						*		*		
	8		*						*				*		*		*					
	9																					DESCENDER
	10	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	CURSOR
	11	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	CURSOR, UNDERLINE
S C A N L I N E	0		*							*												
	1			*					*													
	2				*		*															
	3					*																
	4				*		*						*		*		*					
	5		*				*					*								*		
	6	*							*			*									*	
	7											*									*	
	8											*				*		*		*		
	9											*									*	DESCENDER
	10	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	CURSOR
	11	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	CURSOR, UNDERLINE

Figure 2-10. 4230/4205 WS Character Matrix

2.3.1.10 CRT RAM, Character Generation and CRT Display (Continued)

2.3.1.10.3 Font RAM

In order to display a character stored in character memory, a corresponding pixel pattern must be available for each character. This is the function of font memory. Within font RAM, a pixel pattern is stored for each character available in the workstation's character set.

The 4230 Workstation provides sufficient font RAM to store a 512 character set. Considering a total of 192 pixels per character ($12 \times 16 = 192$), 512 characters would require $512 \times 192 = 98,304$ memory locations to store a character set of this size. Font RAM in the 4230 Workstation is $8k \times 12$, or $8192 \times 12 = 98,304$, and thus large enough to accommodate the 512 character set. The Z-80 CPU must enable page 2 of its address assignments to access font RAM. Page 2 allocates $8k$ of addresses for font memory. (The 4205 Workstation, with its 256 character set, uses a $4k \times 12$ font memory, one half the size of the 4230.)

The four lines of pixels within font memory that are not normally displayed (lines 12 to 15) are loaded with logic 0. These four blanked lines of pixels are used for superscript or subscript characters. When a superscript character is displayed, a value of two is added to the CRT line counter value. This causes the font data for scan line 2 to be presented to the CRT circuitry when scan line 0 is normally displayed, and so on for the entire character. The result is that font data for scan lines 2 through 13 are displayed for the current character.

2.3.1.10 CRT RAM, Character Generation and CRT
Display (Continued)

2.3.1.10.3 Font RAM(Continued)

A subscript character is displayed in a similar manner. A value of fourteen is added to the CRT line counter value. This causes font data for scan lines 14, 15 and 0 through 9 to be displayed for the current character. The vertical positions for the underline and cursor are fixed.

The pixel patterns stored in font RAM are loaded via the microcode sent to the workstation at its initial program load (IPL). This approach allows fonts to be changed for different applications.

Font data for each character is received over the 8-bit Z-80 data bus which allows only eight pixels to be loaded at a time. The remaining four pixels are loaded with another byte from the Z-80. For this reason, font memory is divided into lower and upper portions. Lower font memory stores pixels 0 through 7, while upper font memory stores pixels 8 through 11. In the 4230, lower font memory occupies address space 48k to 52k while upper font memory occupies address space 52k to 56k. In the 4205, only half of these addresses are used. Use of the Z-80 data bus for loading font RAM is illustrated in the next frame.

2.3.1.10 CRT RAM, Character Generation and CRT Display (Continued)

2.3.1.10.3 Font RAM (Continued)

Z-80 Data	BD7	BD6	BD5	BD4	BD3	BD2	BD1	BD0
Pixel	7	6	5	4	3(11)	2(10)	1(9)	0(8)

Font RAM addresses are generated by multiplexing the character data from character RAM, line addresses from the line address multiplexer and CPU addresses from the Z-80 address bus. The Z-80 address controls the four most significant bits of the font address and uses these to select an address range starting at 48k or 52k for either lower or upper font RAM. Character data lines CD0 - CD7 select which pixel pattern is to read out of font RAM. Line addresses select which of the sixteen lines within the pixel pattern is to be read out of font RAM. The result of address multiplexing for font RAM is shown below. Read/write control for font RAM is generated in the read/write control logic.

Z-80 Address		A15		A14		A13		A12	
Font Address		1		1		0		0	

Selects Lower Font RAM,									
48k Address Range		_____							

2.3.1.10 CRT RAM, Character Generation and CRT Display (Continued)

2.3.1.10.3 Font RAM (Continued)

Z-80 Address		A15		A14		A13		A12	
Font Address		1		1		0		1	

Selects Upper Font RAM,									
52k Address Range_____									

Z-80 Address		A11		A10		A09		A08		A07		A06		A05		A04	
Font Address		CD7		CD6		CD5		CD4		CD3		CD2		CD1		CD0	

Selects Pixel Pattern_____																	

Z-80 Address		A03		A02		A01		A00	
Font Address		L03		L02		L01		L00	

Selects 1 of 16 lines									
in pixel pattern_____									

2.3.1.10.4 Character Serialization

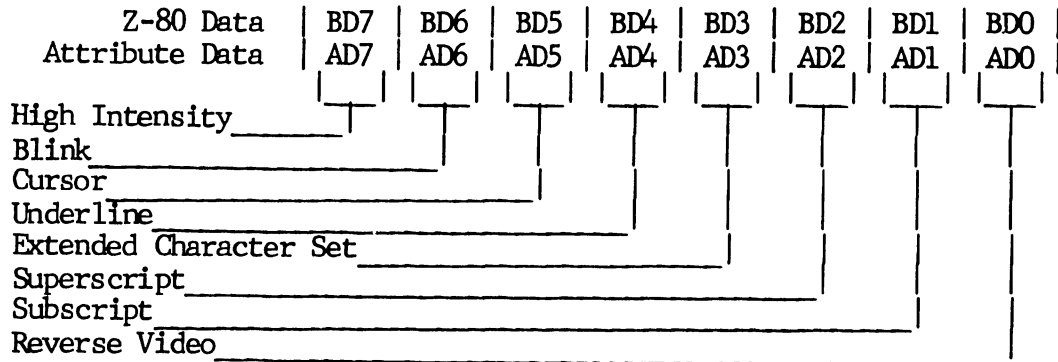
A 10-bit shift register is used to transform the parallel font data to a serial stream of data that can be used by the CRT. Font data is received from font RAM over lines FDO - FD9, serialized and then sent to the video modification logic.

2.3.1.10 CRT RAM, Character Generation and CRT Display (Continued)

2.3.1.10.5 Attribute RAM

Attribute memory stores information that controls how characters appear on the CRT, whether they are underlined, blinking, highlighted or in some other condition. Since these attributes can be different for each character, attribute RAM contains one byte of data for each byte of character RAM. The Z-80 CPU must enable page zero of its address assignments to access attribute RAM. Page zero allocates 8k of addresses for attribute memory, from 48 to 56k, though only 4k is used.

The description of character memory addressing in section 2.3.1.10.1 is the same for attribute RAM. Refer there for a complete description. Read/ write control for attribute RAM is generated in the read/write control logic. Data format for the attribute memory is shown below.



2.3.1.10.6 Video Modification Logic and Video Line Driver

All character-related data is finally merged in the video modification logic. This circuit receives serialized character data from the 10-bit shift register, synchronization signals from the CRT timing control logic and attribute data from attribute RAM. The incoming pixel stream is modified according to the attribute data for that character.

2.3.1.10 CRT RAM, Character Generation and CRT Display (Continued)

2.3.1.10.6 Video Modification Logic and Video Line Driver (Continued)

These three conditions are black (off), normal intensity, or high intensity. These two bit-streams are joined by the horizontal and vertical synchronization signals and all four of the signals are then driven by a differential line driver to the CRT.

2.3.1.10.7 CRT Timing Control Logic

The CRT timing control logic controls the horizontal and vertical beam position for the CRT via its synchronization signal outputs. It also generates row/column addresses for character and attribute RAM and line addresses for font RAM. These addresses are generated in synchronism with the CRT horizontal and vertical sync signals, thereby causing the line of pixels corresponding to the current CRT beam position to be driven to the Monitor.

2.3.1.10.8 Read/Write Control for Character, Attribute and Font RAM

The character, attribute, and font RAMs are shared by the CPU and the CRT timing logic. The CPU generates the image in memory and the CRT timing logic displays the image on the CRT.

2.3.1.10 CRT RAM, Character Generation and CRT Display (Continued)

2.3.1.10.8 Read/Write Control for Character, Attribute and Font RAM (Continued)

The read/write control timing originates from a 19.2 MHz crystal oscillator which provides the time base for the read/write logic.

The CRT logic has the highest priority when accessing character, attribute or font memory. If the CPU needs to access any of these memories, it must wait until the CRT logic operation is complete. The transfer to or from the CPU is then given 260ns to take place. A temporary storage register holds the data during a read operation since the CPU is too slow to read the memory without causing flicker in the display. This interleaving ensures that the CRT display will remain flicker-free by allowing the CRT logic to access the character, attribute, and font memories immediately when new data is required.

2.3.1.10.9 Character Set Control (4230 Only)

There are two 256 character sets which occupy the same address space (48k to 56k) in font memory. The selection of the primary or secondary character set is controlled by an OUT '06' or OUT '07' command.

2.3.1.10 CRT RAM, Character Generation and CRT Display (Continued)

2.3.1.10.9 Character Set Control (4230 Only) (Continued)

The selection of a character set can also be controlled on a character by character basis. Attribute bit three selects the extended character set when it is active. When the primary character set is selected, the secondary character set becomes the extended character set. If the secondary character set is selected, the primary character set becomes the extended character set. By utilizing attribute bit three, both the primary and secondary character sets can be used as a single 512 character set.

The software may instruct the hardware to appear as though there are two 128 character sets by executing an OUT '20' command. The hardware will inhibit all font memory accesses outside of the two 128 character sets. In this mode a maximum of 256 characters may be accessed.

2.3.1.10.10 Horizontal and Vertical Scrolling

Vertical scrolling of information on the CRT is controlled by software. The character and attribute data is read one screen location at a time and rewritten to the screen location one row above its original position. This is repeated until the entire screen has been vertically scrolled upward by one row.

2.3.1.10 CRT RAM, Character Generation and CRT
Display (Continued)

2.3.1.10.10 Horizontal and Vertical Scrolling
(Continued)

Horizontal scrolling is controlled by hardware. A start column value is loaded into a start column register by an OUT '02' command. The start column value can range from 0 to 80 (decimal) inclusive. The CRT will display the first character corresponding to the start column value on the left edge. The next 79 characters will follow from left to right. For example, if the start column value is 29, the 29th to the 108th character will be displayed on each line. Rows 0, 23 and 24 will always display characters zero to 79, that is, they cannot be horizontally scrolled. In the 4205 Workstation, a maximum of 96 characters per line can be displayed and thus horizontal scrolling will only be effective to display the remaining 16 characters not already displayed on the 80 character screen.

2.4 4230 TELECOMMUNICATIONS (Optional)

Telecommunications is supported on the 4230 64K workstation by utilizing the Z80 microprocessor and TC functions on PCA 210-8298. This optional board is loaded above the 210-8287 in the 4230 Electronics Base. The workstation can support a variety of asynchronous and synchronous communication protocols when loaded with the appropriate microcode. A typical 4230 TC local configuration is shown in Figure 2-11.

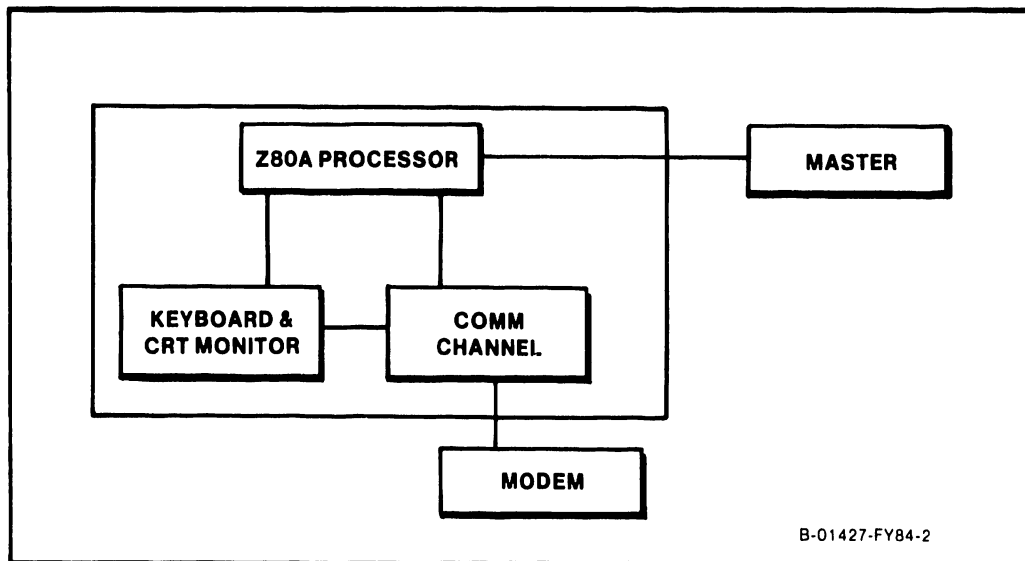
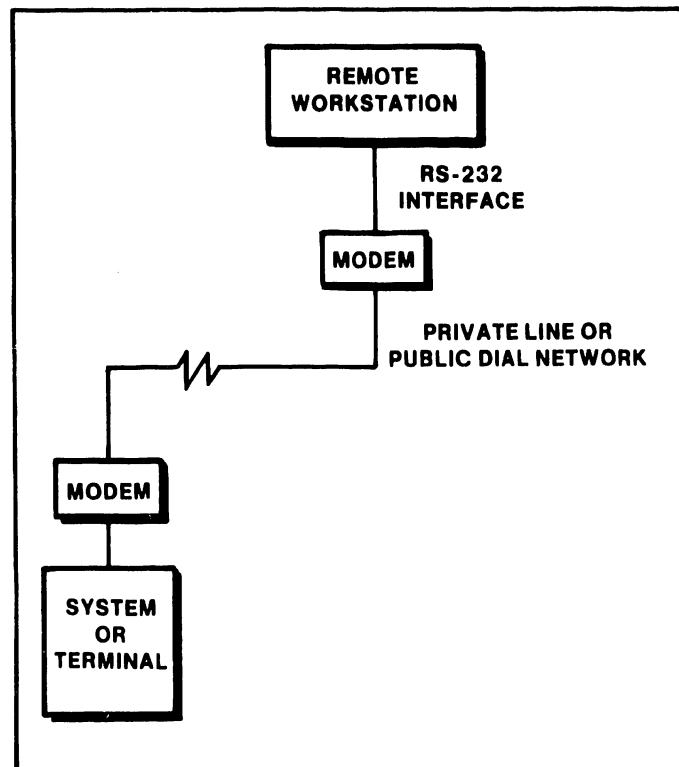
4230 Workstation

Figure 2-11. 4230 TC Local Configuration

2.4 4230 TELECOMMUNICATIONS (Optional)
(Continued)

The 64k 4230 workstation is connected to a modem by an RS-232-C cable running between the modem and the workstation modem connector. If the modem is supplied by the telephone company, they are responsible for the modem connection (figure 2-12).



B-01427-FY84-3

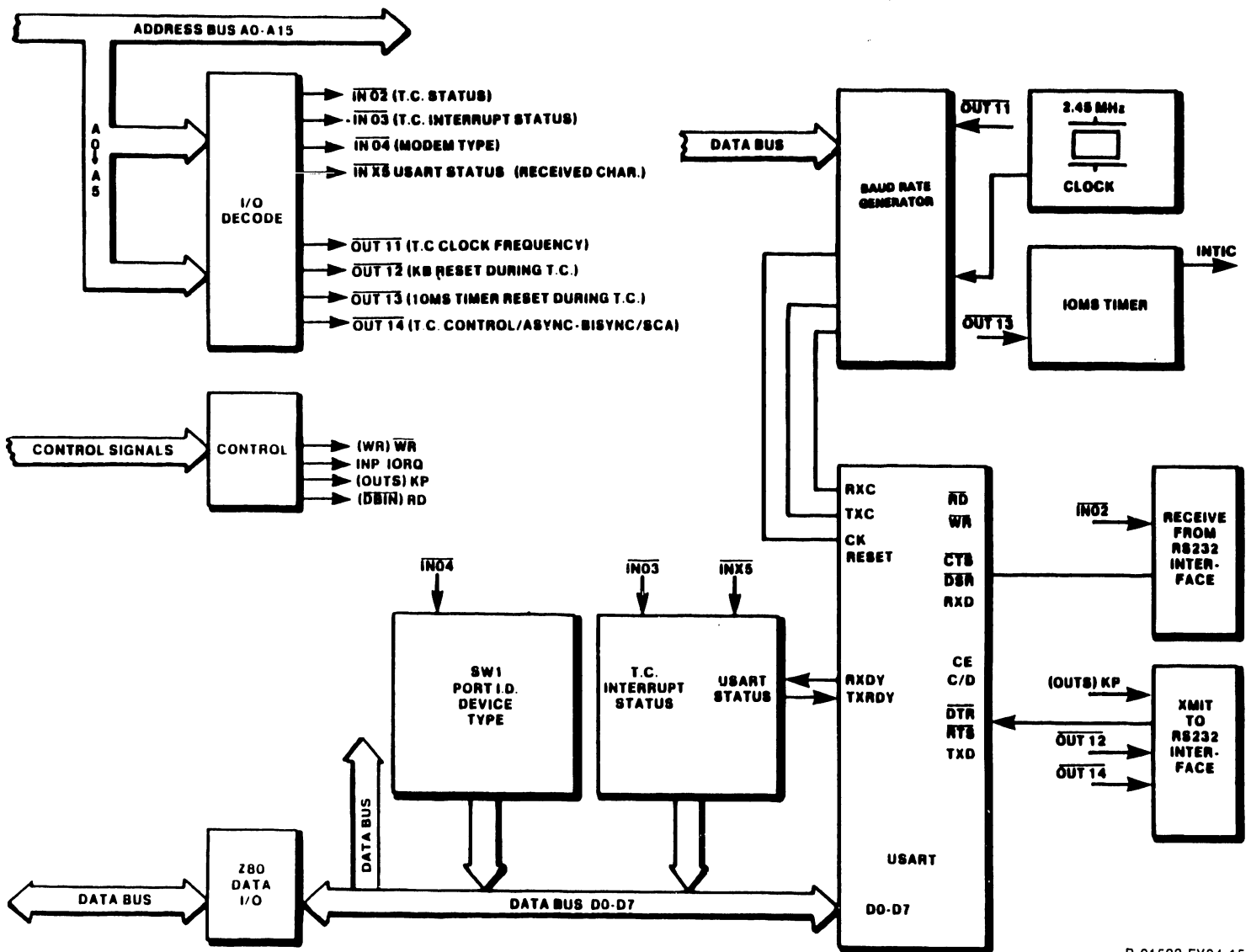
Figure 2-12. Remote TC Configuration

2.4 4230 TELECOMMUNICATIONS (Optional)
(Continued)

2.4.1 FUNCTIONAL THEORY

Telecommunications logic resides on the 210-8298 PCA. The major logic functions are:

- o USART (Conversion)
- o Data Input/Output
- o Decoders
- o Modem Interface



B-01593-FY84-15

Figure 2-13. 210-8298 Telecommunication PCA
Functional Block Diagram

2.4.1 FUNCTIONAL THEORY (Continued)

2.4.1.1 8251A USART

THE 8251A USART (Universal Synchronous/Asynchronous Receiver/Transmitter) is programmed by the CPU to operate using 2780, 3780, WPS, TTY, or 2741 protocols. When the desired protocol has been selected, the CPU sends a set of control words to the USART that program Baud Rate, Character Length, Number of Stop Bits, Synchronous or Asynchronous Operation, and Even, Odd, Off, Mark, Space, and Parity. The USART then accepts data characters from the CPU in parallel format and converts them into a continuous serial data stream for transmission. It can simultaneously receive serial data streams via the modem and converts them into parallel data characters for the CPU.

Internal device timing for the USART is provided by a 2.45 MHz clock circuit. Transmit clock and receive clock are derived from this clock circuit.

2.4.1.2 Data Input/Output

During a transmit operation, data is received from the CPU in a parallel format via a bi-directional driver. The bi-directional driver is controlled by the Z80A CPU which enables/disables the driver as well as selects the direction of the data flow. The data (D7-D0) is gated into the USART where it is converted into serial stream format, gated to the transmit driver and sent to the 25-pin RS-232-C connector interface.

2.4.1 FUNCTIONAL THEORY (Continued)

2.4.1.2 Data Input/Output (Continued)

During a receive operation, data is received by the RS-232 receive circuitry in a serial stream format and gated into the USART where it is converted into a parallel format. The data is then sent through the bi-directional driver and presented to Z80A CPU via the data bus.

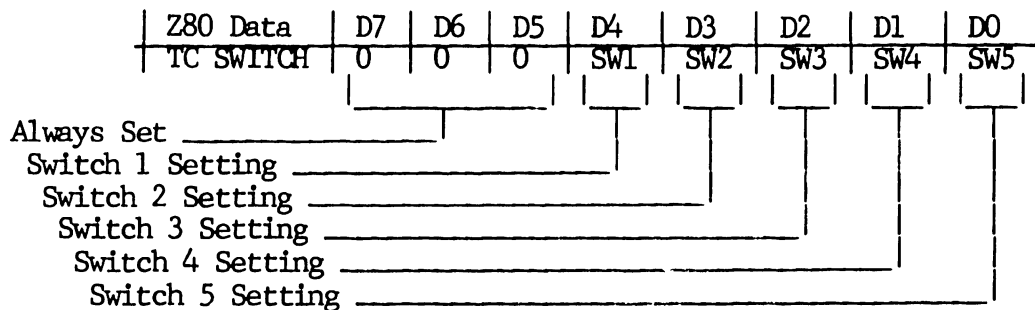
2.4.1.3 "In"/"Out" Decoding

The Z80A CPU uses "IN" and "OUT" command instructions to send or receive control or status information to and from the TC PCA. These instructions are described individually in the following sections. When setting control bits and reading status bits, a logical ON condition is represented by a "1" bit, and a logical OFF condition is represented by a "0" bit.

2.4.1 FUNCTIONAL THEORY (Continued)

2.4.1.3 "In"/"Out" Decoding (Continued)IN'04' Read Telecommunications Port ID Switch

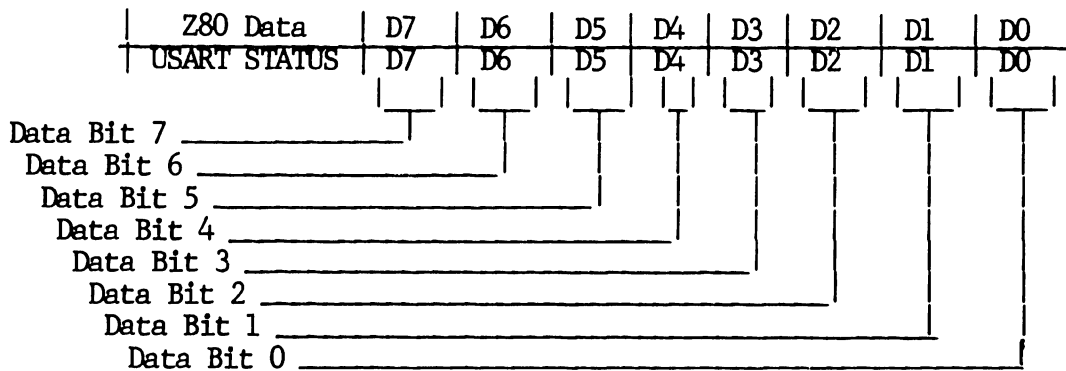
Located on the Telecommunication PCA is a 5-bank switch denoted SW1. When set, this switch indicates the Telecommunications address. The switch is read by the Master unit (via the Z80A) with an IN'04' instruction. The data pattern read is related to the switch positions of SW1. The switch positions read is in the following format:



2.4.1 FUNCTIONAL THEORY (Continued)
 2.4.1.3 "In"/"Out" Decoding (Continued)

IN'15' Input Received Character from USART

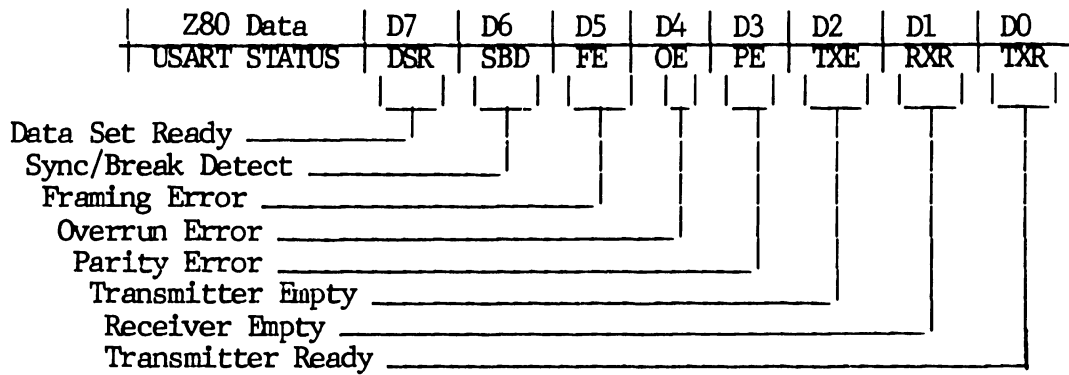
A received character is input from the USART by the Input Received Character instruction. This clears the receiver ready condition and the interrupt condition which it causes. If a transmission character of fewer than 8 bits is being used, the character to be transmitted is right adjusted in the byte input into the accumulator. This command returns the interrupt status in the following format:



2.4.1 FUNCTIONAL THEORY (Continued)

2.4.1.3 "In"/"Out" Decoding (Continued)IN'35' Read USART Status

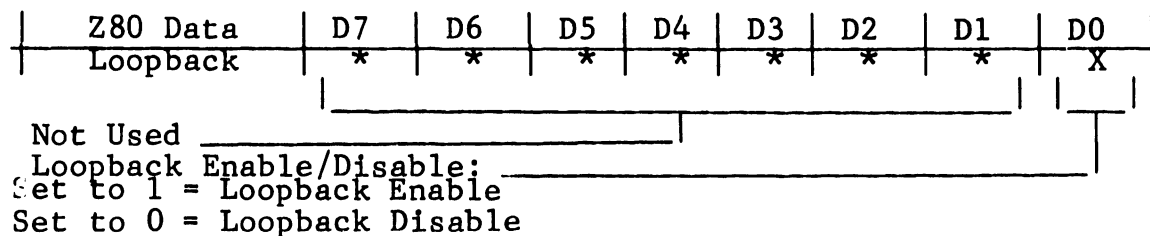
The IN'35' instruction is used to read the USART status register. This command returns the USART status in the following format:



2.4.1 FUNCTIONAL THEORY (Continued)

2.4.1.3 "In"/"Out" Decoding (Continued)OUT '10' Internal Loopback

The Internal Loopback instruction enables/disables the loopback function. This instruction is used by the Built-In-Test (B.I.T.) to verify correct operation of the TC Option board. An OUT '10' instruction with data of '01' (bit D0 set) enables the loopback test. An OUT '10' instruction with data of '00' disables loopback. This OUT instruction (when D0 is set to 1) requires a loopback connector be used on the RS-232-C Connector. Refer to paragraph 2.4.4 for loopback connector description. The command and data format is as follows:

OUT '12' Clear Keyboard Interrupt

The OUT '12' instruction clears the Key pending interrupt. The data byte supplied with the instruction is irrelevant.

2.4.1 FUNCTIONAL THEORY (Continued)

2.4.1.3 "In"/"Out" Decoding (Continued)OUT'13' Clear 10 msecond Interrupt

The OUT'13' instruction clears the 10 msecond (millisecond) interrupt. The data byte supplied with the instruction is irrelevant.

OUT'11' Set Internal Clock Rate

The OUT'11' instruction is used to set the baud rate of the USART. For asynchronous communications, the USART Baud Rate Factor must also be set by a USART mode instruction. The table below list the possible baud rates and the associated data bit pattern.

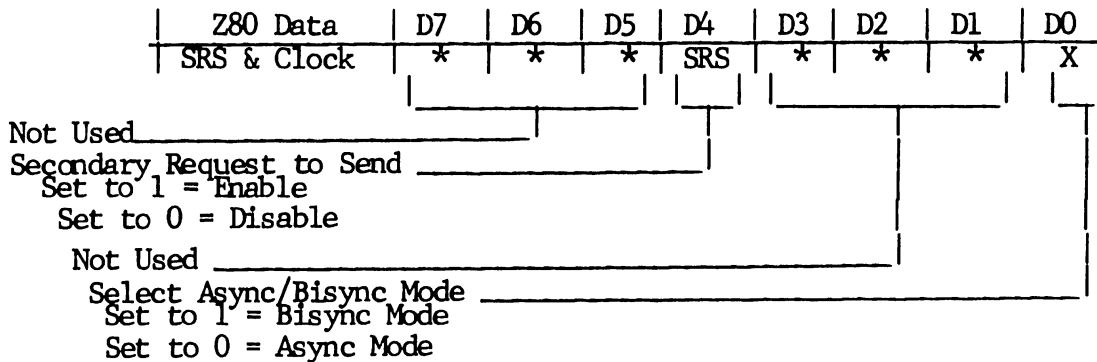
Baud Rate	OUT '11' DATA Aysnc Mode	OUT '11' DATA Sync Mode	USART Baud Rate Factor
50	'40'		1
75	'80'		1
100	'A0'		1
110	'A9'		1
134.5	'B9'		1
150	'C0'		1
200	'D0'		1
300	'E0'		1
600	'F0'		1
1200	'F8'		1
2400	'F0'	'01'	0
4800	'F8'	'80'	0
9600	'FC'	'C0'	0

Note: When the on-board clock is used to provide a synchronous clock signal, the Baud Rate Select Code is different from that used for asynchronous clock signal.

2.4.1 FUNCTIONAL THEORY (Continued)

2.4.1.3 "In"/"Out" Decoding (Continued)OUT'14' Set Secondary Request to Send and Clock Mode

The OUT'14' instruction is used to select BISYNC or ASYNC clock mode. This instruction is also used to set and clear the Secondary Request to Send signal. The modem control signal Secondary Request to Send (SRS, bit D4) and the Select Asynchronous Clock/Select Bisync Clock bit (bit D0) are set at power up. The command and data format is as follows:

OUT'16' Disable Telecommunications Interrupts

An OUT'16' instruction disables the 10 msecond, transmitter, receiver, and Key pending interrupts. All the telecommunications interrupts are disabled after power-on or a datalink restart. No data is required with this instruction.

2.4.1 FUNCTIONAL THEORY (Continued)

2.4.1.3 "In"/"Out" Decoding (Continued)OUT'17' Enable Telecommunications Interrupts

An OUT'17' enables the interrupts after the interrupts have been disabled and after an interrupt service routine has been successfully serviced. No data is required with this instruction.

OUT'15' Output Character to USART for Transmission

The OUT'15' instruction is used to write a character into the USART's transmit register. This clears the transmitter ready condition and the interrupt condition which it causes. If a transmission character of fewer than 8 bits is being used, the character to be transmitted is assumed to be right adjusted in the byte output from the accumulator.

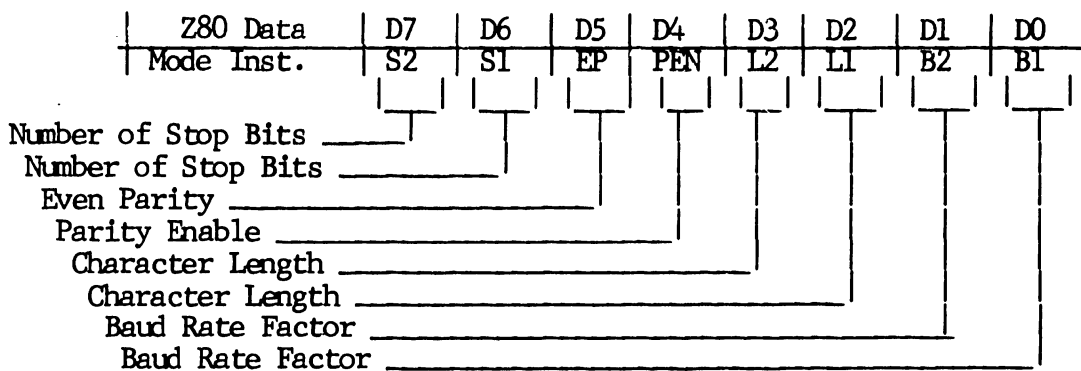
OUT'35' Set USART Mode/Command Data

The OUT'35' instruction is used to send mode, command, and sync information to the USART. The interpretation of the byte of data output by the SET USART Mode/Command instruction is determined by the state of the USART. Following a reset of the USART, which can be caused by either a power-on condition or a bit in the Command Word, the first byte output by this instruction is interpreted as a Mode instruction.

2.4.1 FUNCTIONAL THEORY (Continued)

2.4.1.3 "In"/"Out" Decoding (Continued)

If the Mode instruction selects asynchronous mode, all bytes subsequently output by the instruction (unless they specify an internal reset) are Command Words. If the Mode instruction selects synchronous mode, the next one or two bytes, as determined by the Mode instruction, output by the instruction define the synchronization pattern. All subsequently bytes output by the instruction are command words. The mode instructions for asynchronous and synchronous modes are as follows:

Asynchronous Mode

Number of Stop Bits (D7 and D6)

S2	S1	M
0	0	Invalid
0	1	1 Stop Bit
1	0	1.5 Stop Bits
1	1	2 Stop Bit

2.4.1 FUNCTIONAL THEORY (Continued)

2.4.1.3 "In"/"Out" Decoding (Continued)

Even Parity Generation/Checker (D5)

D5 = 1 denotes Even Parity, D5 = 0 denotes Odd Parity

Parity Enable (D4)

D4 = 1 denotes parity enabled, D4 = 0 denotes parity disabled

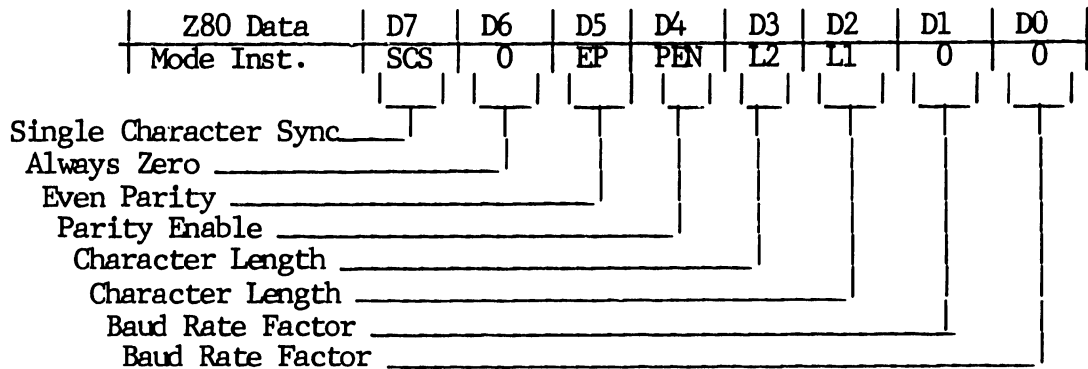
Character Length (D3 and D2)

D3	D2	Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

Baud Rate Factor (D1 and D0)

D1	D0	Factor
0	0	Sync Mode
0	1	1 Time
1	0	16 Times
1	1	64 Times

Synchronous Mode



2.4.1 FUNCTIONAL THEORY (Continued)

2.4.1.3 "In"/"Out" Decoding (Continued)

Single Character Sync (D7)

D7 = 1 denotes single sync character,

D7 = 0 denotes double sync character

Even Parity Generation/Checker (D5)

D5 = 1 denotes Even Parity, D5 = 0 denotes

Odd Parity

PEN (D4) must be set

Parity Enable (D4)

D4 = 1 denotes parity enabled, D4 = 0 denotes
parity disabled

Character Length (D3 and D2)

<u>D3</u>	<u>D2</u>	<u>Length</u>
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

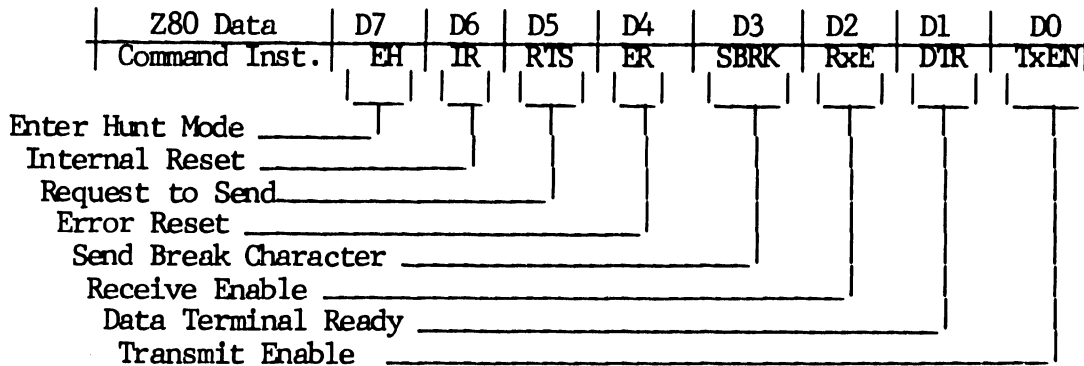
Baud Rate Factor (D1 and D2)

<u>D1</u>	<u>D0</u>	<u>Factor</u>
0	0	Sync Mode

2.4.1 FUNCTIONAL THEORY (Continued)

2.4.1.3 "In"/"Out" Decoding (Continued)

Synchronous Command



Enter Hunt Mode (D7) when set (applicable to synchronous only)

Internal Reset USART (D6) when set

Request to Send Modem Signal (D5) when set (Note: forces RST pin low)

Error Reset (D4) when set, resets Framing, Overrun, and Parity Error Status

Send Break Character (D3) when set, Break character latched until cleared

Receive Enable (D2) when set, Receive disabled when D2 = 0

Data Terminal Ready (D1) when set (Note DTR pin is forced low)

Transmit Enable (D0) when set, Transmit disabled when D0 = 0

2.4.1 FUNCTIONAL THEORY (Continued)

2.4.1.4 USART Limitations

The USART chip has several limitations which must be observed. These are:

- o The status of the USART will not be valid until 28 clock periods from an event affecting the status (11.4 microseconds).
- o The TXRDY pin will not be valid for 8 clock cycles after last transmission (3.25 microseconds).
- o The RXRDY pin will not be valid for up to 24 clocks after the last received character. (9.77 microseconds).

Note: The main USART clock is independent of the system clock and has a fixed frequency of 2.4576 MHz.

2.4 4230 TELECOMMUNICATIONS (Optional)
(Continued)

2.4.2 MODEM INTERFACE

The workstation contains a 25-pin EIA RS-232-C connector located on the rear panel of the 4230 workstation. Pin designations are shown below.

Pin	EIA	Source	Signal Description
1 *	AA	---	Protective Ground
2 *	BA	TC PCA	Transmitted Data
3 *	BB	Modem	Received Data
4 *	CA	TC PCA	Request to Send
5 *	CB	Modem	Clear to Send
6 *	CC	modem	Data Set Ready
7 *	AB	---	Signal Ground
8 *	CF	Modem	Received Line Signal Detector
9	--	---	(Reserved for Data set Testing)
10	--	---	(Reserved for Data Set Testing)
11 *	SCA	TC PCA	Secondary Request to Send
12 *	SCF	Modem	Secondary Received Line Signal Detector
13	SCB	Modem	Secondary Clear to Send
14	SBA	---	Secondary Transmitted Data
15 *	DB	Modem	Transmit Signal Element Timing
16	SBB	Modem	Secondary Received Data
17 *	DD	Modem	Receiver Signal Element Timing
18	--	---	Unassigned
19 *	SCA	TC PCA	Secondary Request to Send
20 *	CD	TC PCA	Data Terminal Ready
21	CG	Modem	Signal Quality Detector
22	CE	Modem	Ring Indicator
23	CHCI	Modem	Data Signal Rate Selector
24	DI	---	Transmit Signal Element Timing
25	--	---	Unassigned

* Denotes signals used by the TC workstation

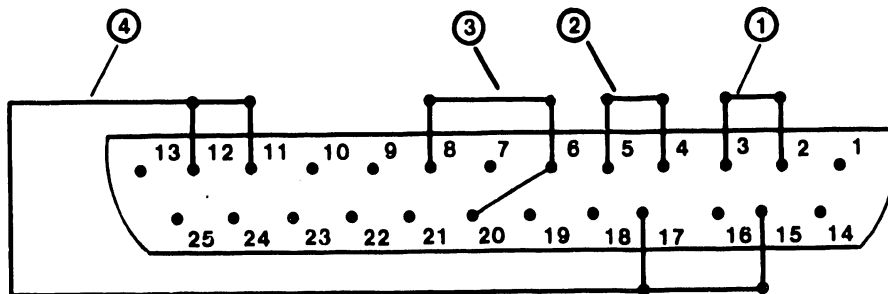
2.4 4230 TELECOMMUNICATIONS (Optional)

(Continued)

2.4.3 RS-232-C LOOPBACK CONNECTOR

An RS-232-C Loopback connector (part number 420-1040) is required for loopback testing of the 4230 TC PCA. This connector should be installed on the RS232 port prior to running the loopback diagnostics.

If the loopback connector is not available, use a RS-232 blank connector (part number 350-1030) and jumper the pins as shown in figure 2-14.



B-01427-FY84-4

(Note: loopback connector is viewed head on.)

Figure 2-14. Loopback Connector Jumper Diagram

2.5 ARABIC WORKSTATION

The theory of operation for the Arabic (Middle Eastern) Workstations is very similar to that of the 4230/4205 Workstations found in chapter 2 of this 4205/4230 Product Maintenance Manual; however, the Arabic mode will function only if a 210-8287-3 Workstation PCA has been installed in the workstation.

When software issues the proper command, circuitry on the 210-8287-3 PCA presents all characters to be displayed on the CRT in reverse order. The software instructs the workstation to go into an Arabic mode by issuing an OUT '21' command. If the command is issued with a HEX value of '01', the horizontal order of all characters on the CRT to be reversed (right-to-left). If the OUT21 command is issued with a HEX value of '00', the horizontal order of all characters on the CRT is normal (left-to-right).

The start column value functions in exactly the same way as in the non-Arabic mode. If a start column value of 29 is loaded into the start column register, the 108th to the 29th character will be displayed left to right on the CRT.

CHAPTER

3

**OPERA-
TION**

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CHAPTER 3

OPERATION

This chapter provides information pertaining to the 4230/05 Workstation operator controls and indicators, initial control settings, initial turn-on procedures, and normal and emergency shut-down procedures.

3.1 CONTROLS AND INDICATORS

The controls and indicators of the 4230/05 Workstations are shown in Figure 3-1 and discussed separately below. The Keyboard is discussed separately in section 3.3.

-1/0 (On/Off) Switch - Turns ac input power to the workstation on (1) or off (0).

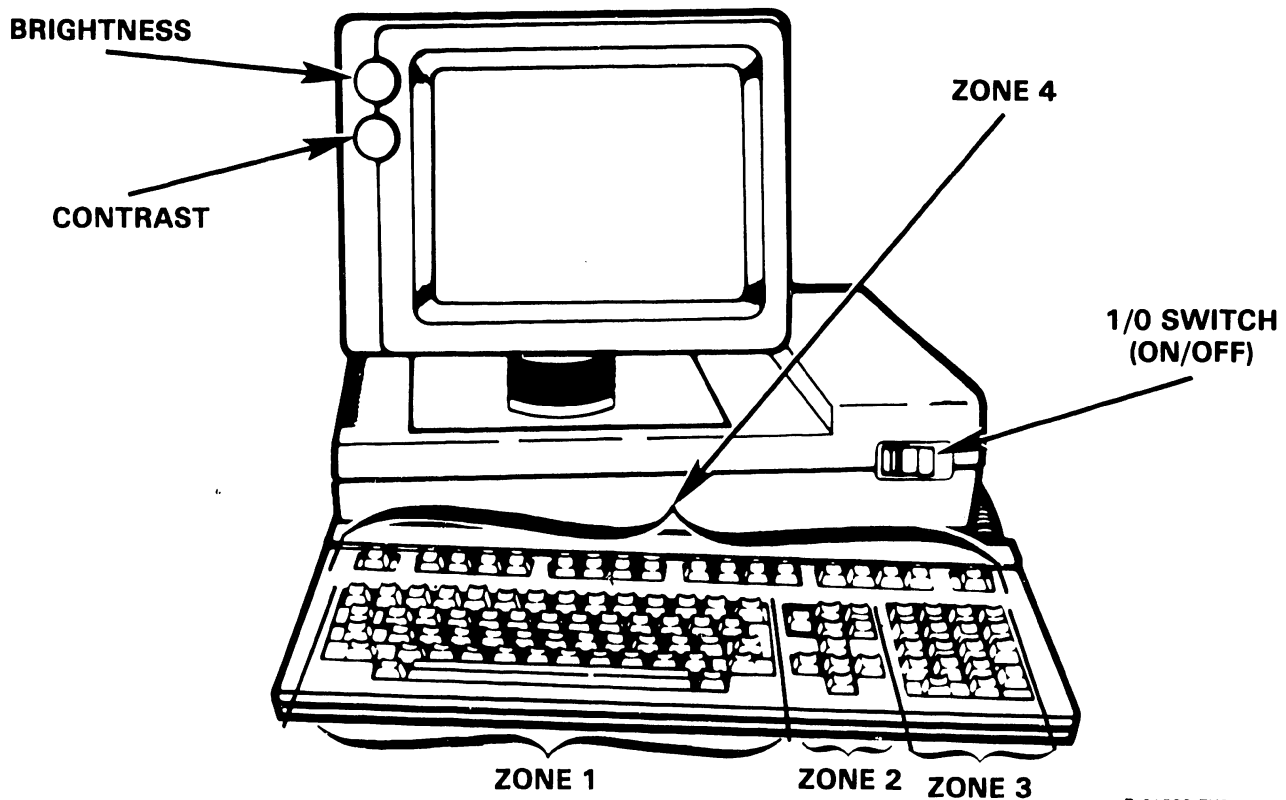
-Brightness Control - The Brightness control sets the brightness of all displayed characters, affecting normal and highlighted characters equally.

-Contrast Control - The Contrast control sets the brightness of highlighted characters only.

3.2 KEYBOARD

The workstation is equipped with the low profile, serial keyboard currently used in other Wang products (refer to Figure 3-1).

The Keyboard features the conventional typewriter format, cursor control and editing keys, and special function keys. The special function keys are those normally associated with Wang WP systems (INDENT, FORMAT, SRCH, COMMAND, etc.) and those normally associated with data processing systems (Program Function nn keys). Additionally, the Keyboard is equipped with a numeric keypad at the extreme right. An Arabic Keyboard is also available for use with the 4230/05 Arabic Workstation.



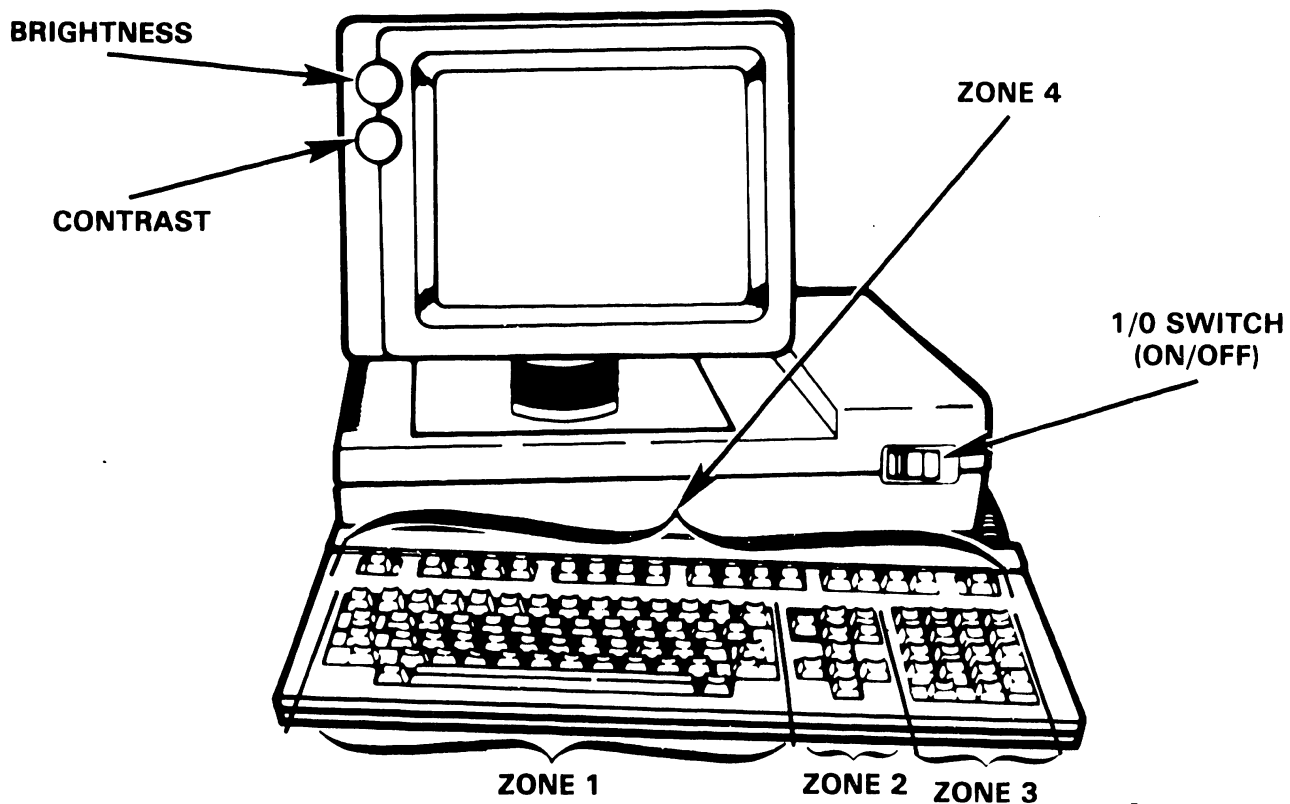
B-01593-FY84-17

Figure 3-1. Controls and Indicators

3.2 KEYBOARD (Continued)

The following paragraphs describe the actions associated with each group of keys. For convenience of discussion, the keyboard has been divided into four zones as shown in the figure below.

Zone 1 - Typewriter Keyboard: Similar to a standard typewriter, this zone contains the alphanumeric characters, the special purpose characters such as @ # \$ % and the arithmetic operators (+ - * / =). Also included are the TAB, GL, RETURN and SHIFT keys which perform the following WP functions:

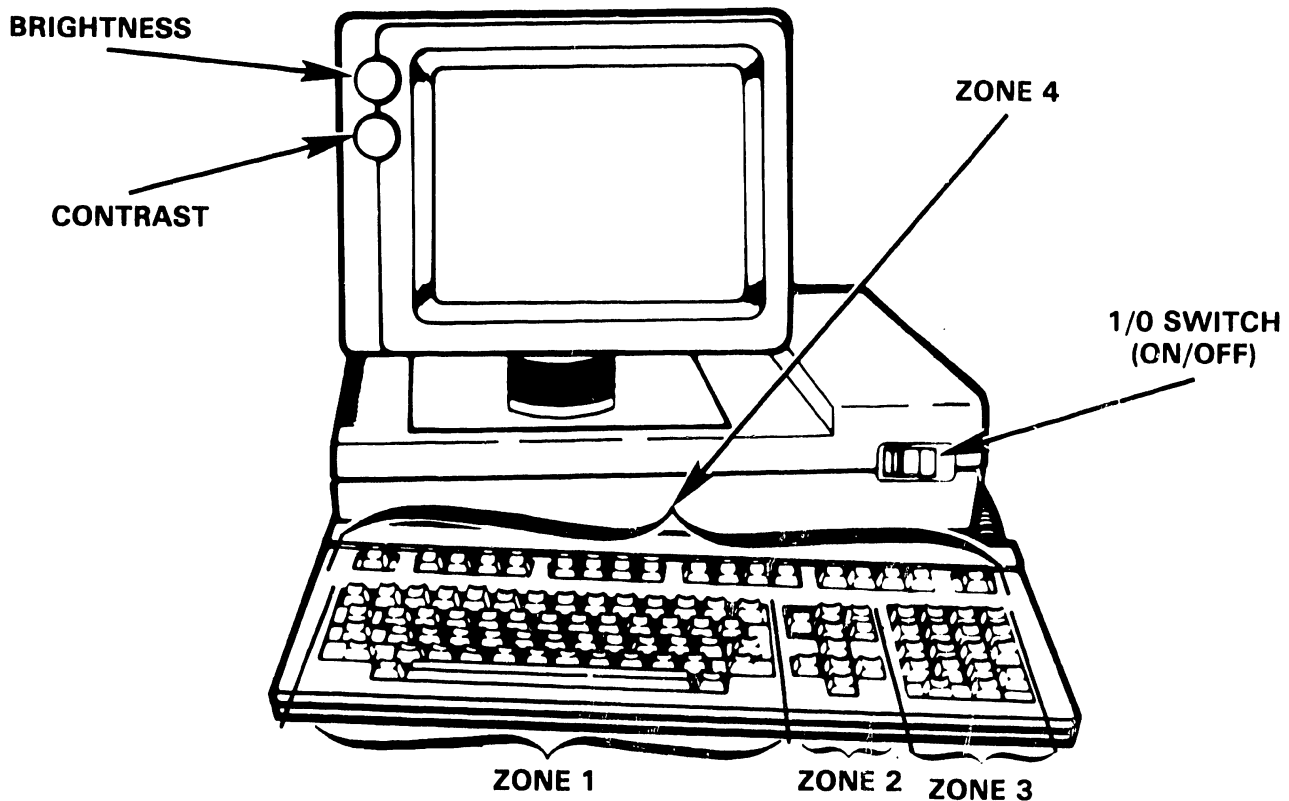


3.2 KEYBOARD (Continued)

-TAB sets the format line zone and advances the cursor through successive zones on the screen to facilitate table creation.

-GL (glossary) is a useful function in Word Processing whereby repeatedly used text may be created once, stored on disk and retrieved again with two keystrokes, GL followed by the glossary number.

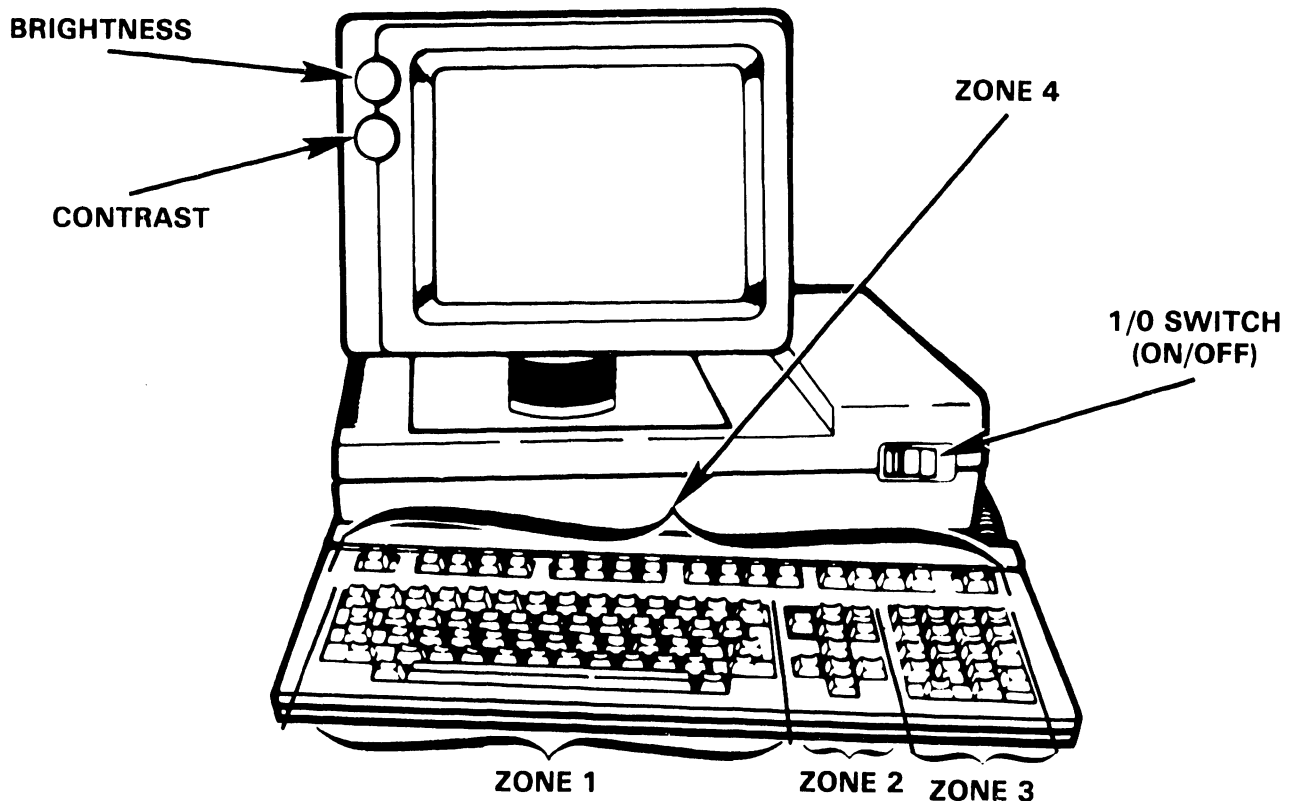
-RETURN terminates the present text line and repositions the cursor at the beginning of the next line.



3.2 KEYBOARD (Continued)

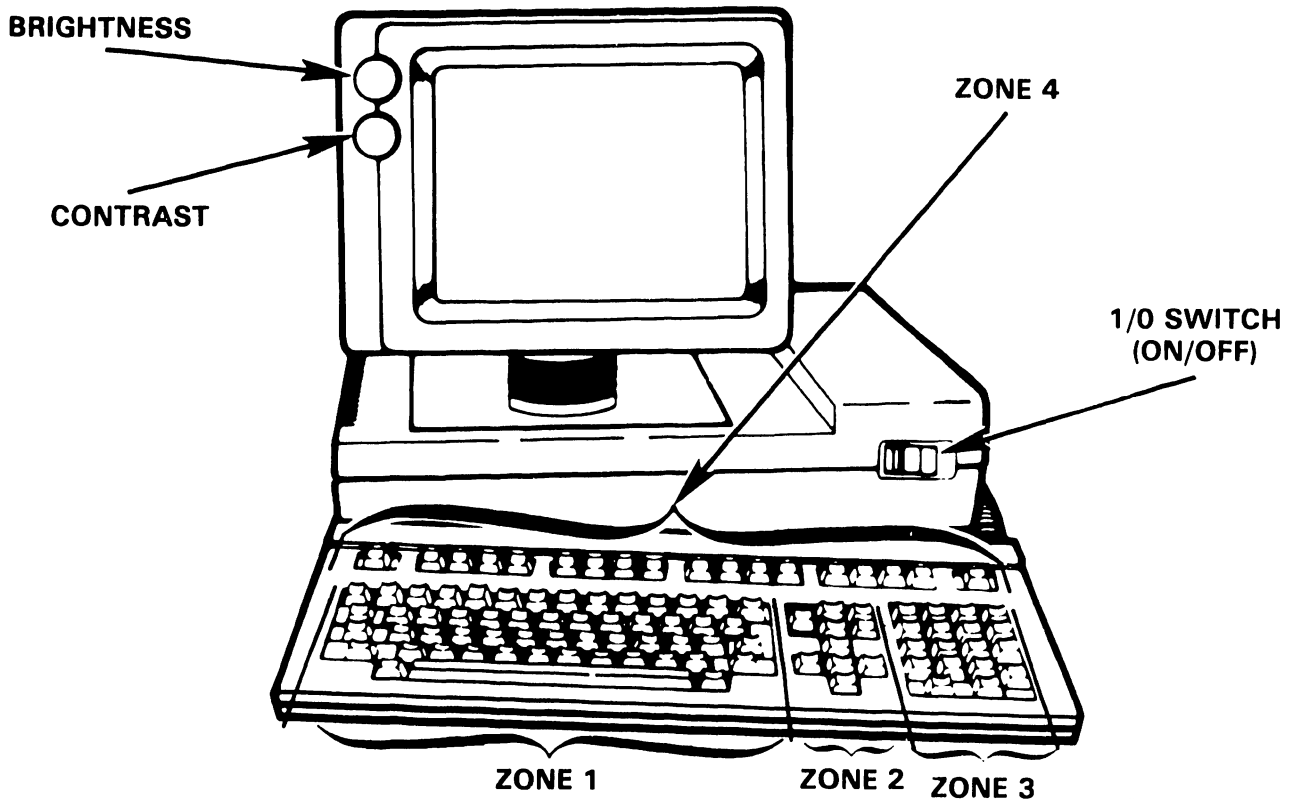
Zone 2 - Cursor Control and Editing Keys: This zone contains editing keys (INSERT and DELETE), location keys (NEXT SCRN and PREV SCRN), and cursor control keys which control movement of the cursor in the indicated direction, up, down, right, left and home (top left corner of screen).

Zone 3 - Numeric Keypad: The keys in the numeric zone allow rapid entry of numeric characters, grouped here for convenience. Digits can be entered by using the numeric keys in either the numeric or the alphanumeric zone. In addition to the standard ten numeric keys are arithmetic operator keys (+, -, x, divide-by) and PRINT, ERASE, RETURN and decimal point (.) keys used in some data processing applications.



3.2 KEYBOARD (Continued)

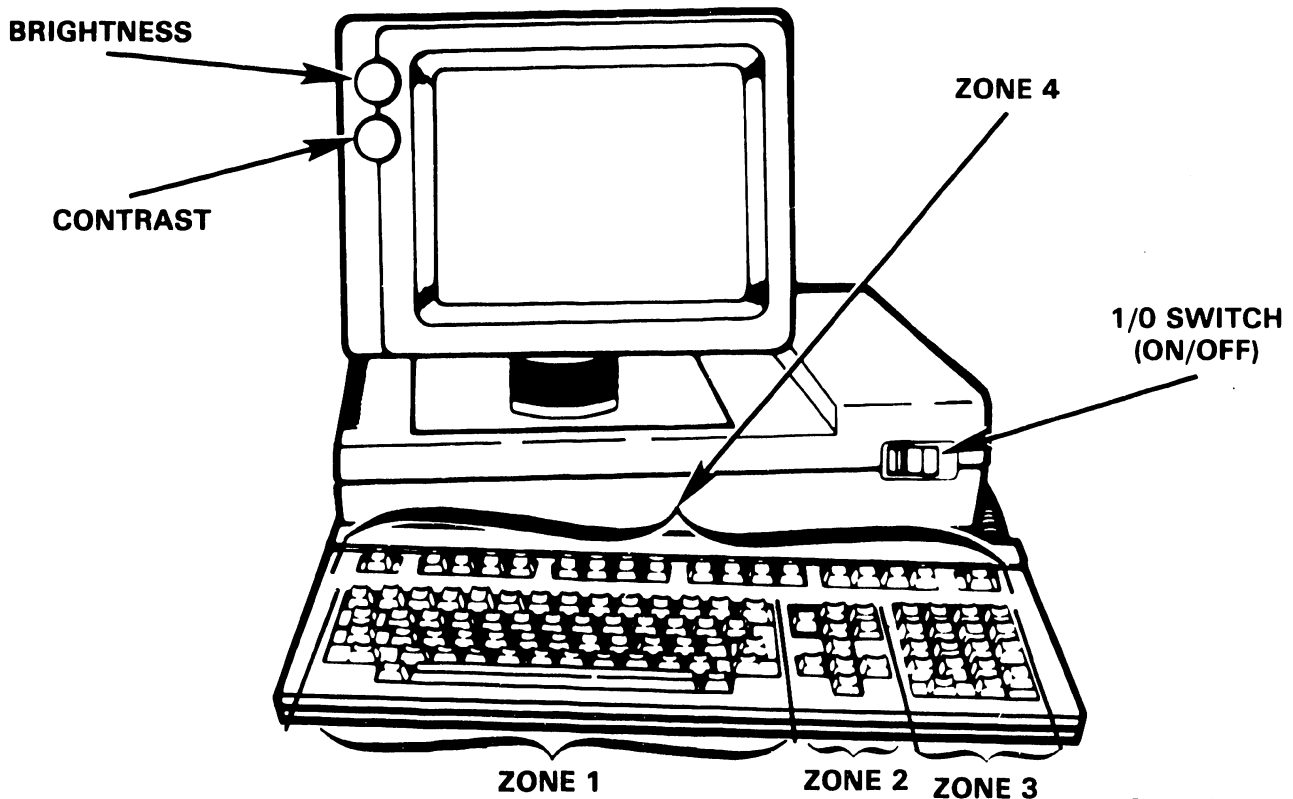
Zone 4 - Special Function Keys: Across the top of the Keyboard are 16 Special Function keys. These keys provide the special Word Processing functions which simplify document creation and revision. For example, the CENTER key automatically centers a line of text, the MOVE key allows any amount of consecutive text to be moved within a document, and the REPLC key allows a character-defined sequence to be replaced with another within a document. For data processing, these keys can call any of 32 special Program Functions (PF1 through PF32). The LOCK key acts either as a caps-lock feature in a data processing environment or as a shift-lock feature in an office automation environment.



3.2 KEYBOARD (Continued)

The caps-lock feature allows letters to be capitalized but does not cause the numeric/symbolic characters to be upshifted. When the LOCK key is pressed, an LED built into the key is illuminated. Pressing either SHIFT key unshifts the keyboard and extinguishes the LED. The Keyboard allows characters to be underlined and all displayable characters can be made to repeat. A "2ND" key is present which allows special operating features of the workstation to be exercised. Refer to section 3.6 for a description of these features.

Located across the function strip on the Keyboard are five LEDs. These LEDs are software programmable and are used to display diagnostic error codes when the Built-In Test (BIT) is running.



3.3 INITIAL CONTROL SETTINGS

The only initial setting that requires attention is the external 115V/230V Power Supply switch detailed in Chapter 4 (Installation) of this manual.

3.4 INITIAL TURN-ON PROCEDURE

Prior to turning on the workstation, ensure that all packing materials (tape, plastic wrap, etc.) are removed from the unit. Inspect the unit to ensure that all cables are properly attached and verify the ac input voltage switch setting as described in Chapter 4.

The following procedure is recommended for initial system turn-on:

Set the I/O switch on the front of the Electronics Base to the 1 (on) position. When power is first applied the following actions will ensue:

-The workstation's internal fan starts

-A short beep sounds

-The BIT begins to run

-the Keyboard LEDs flash on and off in accordance with the BIT

3.4 INITIAL TURN-ON PROCEDURE (Continued)

-The monitor begins to display various test patterns, although this may not be visible if the CRT has not warmed up sufficiently. Refer to Chapter 4 for details on the particular model's BIT.

After successful completion of the BIT, the host CPU will execute the IPL (Initial Program Load) sequence. When the IPL is completed, the Monitor will display the LOGON screen in VS systems, or the DOS menu in OIS systems (4230 only). If the unit is not on line, the ID field message of the BIT will appear on the first line of the CRT.

3.5 SPECIAL OPERATING FEATURES

4200-Series Workstations in Data Processing mode employ the "2ND" key to call up special operating features unique to each model. These features are secondary functions of other keys on the Keyboard. The features applicable to the 4230/05 Workstation are described below.

-2ND, PF5 (FORMAT) - Places the workstation in the setup mode for setting the audio prompt and clicker volume, and selecting/deselecting the type-ahead feature. Pressing PF16 clears the setup mode. Operation of the 4230/4205 setup mode is described below.

3.5 SPECIAL OPERATING FEATURES (Continued)

The setup mode is entered by pressing in sequence, 2ND, PF5 (FORMAT). The CRT screen will produce a one line reverse video field at the bottom of the workstation display, with symbols indicating the setup options shown below.

BELL VOLUME	CLICKER VOLUME	TYPE-AHEAD

One of the function symbols will be highlighted with a special setup mode cursor; this cursor can be moved over any one of the options by using the cursor east/west keys. Placing the cursor over an option selects that option to be modified, either in volume for the audio prompt and clicker, or on/off as with the type-ahead feature. The option is modified with the cursor north/south keys.

To adjust/select any of the setup options, proceed as follows:

1. Enter the setup mode by pressing in sequence 2ND, PF5 (FORMAT). (This can be done anytime after the workstation microcode has been down-loaded from the host CPU.)
2. Using the cursor east/west keys, move the setup cursor over the option to be adjusted/selected.

3.5 SPECIAL OPERATING FEATURES (Continued)

3. Use the cursor north/south keys to adjust/select the option. For audio prompt and clicker volume, pressing the north key steps the volume to the next higher level. Pressing the south key lowers the volume to the next lower level. For the type-ahead feature, pressing the north key enables the option, pressing the south key disables the option.
4. Press PF16 to return to the previous display.

A description of the type-ahead option follows.

Type-ahead - The type-ahead feature allows the user to enter data from the keyboard while, at the same time, executing data I/O to and from the host CPU. For the user familiar with the next screens, this eliminates a wait for the screens to change.

3.6 TELECOMMUNICATIONS OPERATION

Telecommunications operation for the 4230 Workstation is standard, as described in PSN 729-0689: TC Software Utility Option.

3.7 NORMAL SHUT-DOWN PROCEDURE

Before turning off the workstation on VS systems, be sure to LOGOFF (PF16). On OIS systems, return to the DOS menu. Turn off the workstation by setting the I/O power switch to the 0 (off) position.

3.8 EMERGENCY SHUT-DOWN PROCEDURE

In case of an emergency situation when the normal shut-down procedure cannot be used, proceed as follows:

1. Set the I/O (on/off) switch to the 0 (off) position.
2. Remove the ac power plug from the outlet.

CHAPTER

4

INSTAL-

LATION

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CHAPTER 4

INSTALLATION

This chapter contains information required to properly install the 4230/05 Workstations. The 4230/05 Workstations are shipped with their internal switches preset for proper operation. This eliminates the need to disassemble units of the workstation during the installation process. Hence, the switch setting information usually found in this chapter will be found in Chapter 5, Maintenance, for these workstations.

4.1 INSTALLATION SITE CHECK

4.1.1 ENVIRONMENTAL

The environment in which the workstations operate can greatly affect their performance. Considerations of temperature, humidity and cleanliness are discussed below.

4.1.1.1 Temperature Considerations

The recommended operating temperature range for the workstations is from 60°F to 80°F (15°C to 27°C), but a range from 50°F to 90°F (10°C to 32°C) is allowable. Since nearly all locations are heated, low outside temperatures are usually not a problem. High temperatures can be a problem, however, in locations that do not have air conditioning. If the system is used where temperatures exceed the maximum specified, component failure rates may increase, resulting in costly downtime.

4.1.1 ENVIRONMENTAL (Continued)

4.1.1.1 Temperature Considerations (Continued)

If an air conditioning unit is already installed or if one is to be installed, such equipment must be powered on a power line separate from the one connecting to the workstation. If separate power is not used, data errors can occur when the air conditioner is in use.

Air conditioning also removes moisture and dust from the air by lowering the humidity. Lower humidity levels along with static build-up from carpets and synthetic clothing can impart a static electrical charge on operating personnel. When the operator comes in contact with the unit, the resultant static discharge can cause unit failures.

4.1.1.2 Humidity Considerations

The recommended relative-humidity range is from 35% to 65%. Humidifiers or dehumidifiers should be installed to increase or decrease the humidity as required. If carpeting is to be installed, be sure it is a non-static variety. If carpeting already exists which is not of the non-static type, it will either have to be treated with a non-static spray or an electrically conductive mat must be installed to prevent a static charge build-up. Carpets treated with non-static spray should be thoroughly cleaned before the first treatment.

4.1.1 ENVIRONMENTAL (Continued)

4.1.1.2 Humidity Considerations (Continued)

If an electrically conductive mat is used, it should be installed under the unit's operating area and must be properly connected to an earth ground.

4.1.1.3 Cleanliness Considerations

Dust can accumulate within the workstations since they contain no air filters. Dirt and grease form a film that prevents proper heat dissipation from components and can also create a leakage path for signals. To prevent this type of failure, all air conditioning, heating and ventilating units should have air filters installed; these filters should be cleaned or replaced regularly.

4.1 INSTALLATION SITE CHECK (Continued)

4.1.2 ELECTRICAL SERVICE CONSIDERATIONS

The workstations are designed to operate domestically with a 115V, 60 Hz power source, or internationally with a 230V, 50 Hz power source. The source outlet should not be electrically connected to other equipment capable of generating voltage fluctuations on the power line (such as paper shredders, electrical stamp machines/staplers, coffee makers, etc.) The workstation is outfitted with a three-wire power cord, designed for connection to a standard grounded outlet (NEMA 5-15IG receptacle).

4.1 INSTALLATION SITE CHECK (Continued)

4.1.3 EQUIPMENT POSITIONING

Equipment positioning is limited only by the following cable lengths:

-A maximum of 2000 feet from the 4230/05 Workstation to the host CPU.

-A maximum of 50 feet from the 4230 TC Workstation to its modem if it is remote from the OIS Master.

-A maximum of 50 feet from the 4230 TC Workstation to the OIS Master if it is connected locally via a null modem.

Other than the above considerations, no special requirements apply with respect to positioning the workstations except for common-sense considerations of operator convenience and non-interference with traffic flow.

4.2 UNPACKING AND INSPECTION

4.2.1 INSPECTION UPON ARRIVAL

When the equipment arrives, immediately locate the packing slip and note the work order number. Verify the equipment model and serial number as listed on the packing slip.

Before opening the container, inspect it carefully for signs of damage (crushed edges, puncture holes, tears, etc.) If damage is noted, promptly file a claim with the carrier and notify the factory:

WLI DISTRIBUTION CENTER
Department #90
Quality Assurance Department
Tewksbury, MA 01876

State the nature and extent of damage and make arrangements for replacement equipment, if necessary. Be certain to include the following information:

WORK ORDER # _____
CUSTOMER NAME _____ CUSTOMER # _____
MODEL # _____
SERIAL # _____

4.2.2 UNPACKING

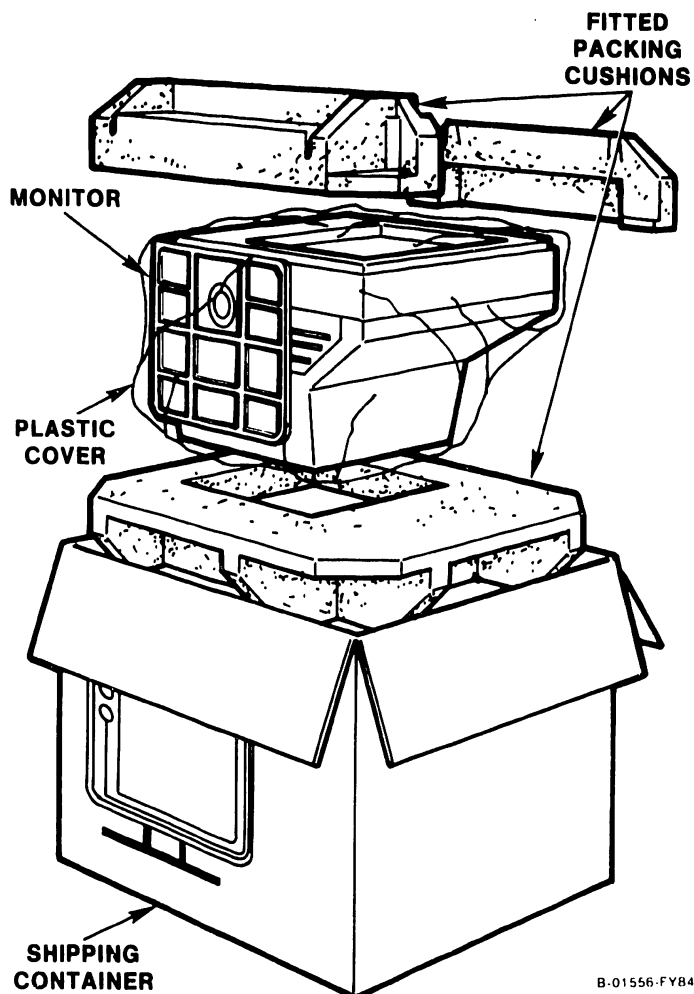
The 4230/05 Workstations come packaged in three containers, one for the 12-inch Monitor, one for the Keyboard and one for the Electronics Base.

4.2.2 UNPACKING (Continued)

4.2.2.1 Unpacking the Monitor

Figure 4-1 shows the method used to pack the Monitor. Use the following procedure to unpack it. Save all packing material until the unit has been found to perform satisfactorily.

1. Carefully cut the tape sealing the top of the shipping container, being careful not to penetrate so deeply as to contact the contents. Open the shipping container.
2. Remove the fitted packing cushions.
3. Lift the Monitor out of the shipping container and remove the plastic wrapping.



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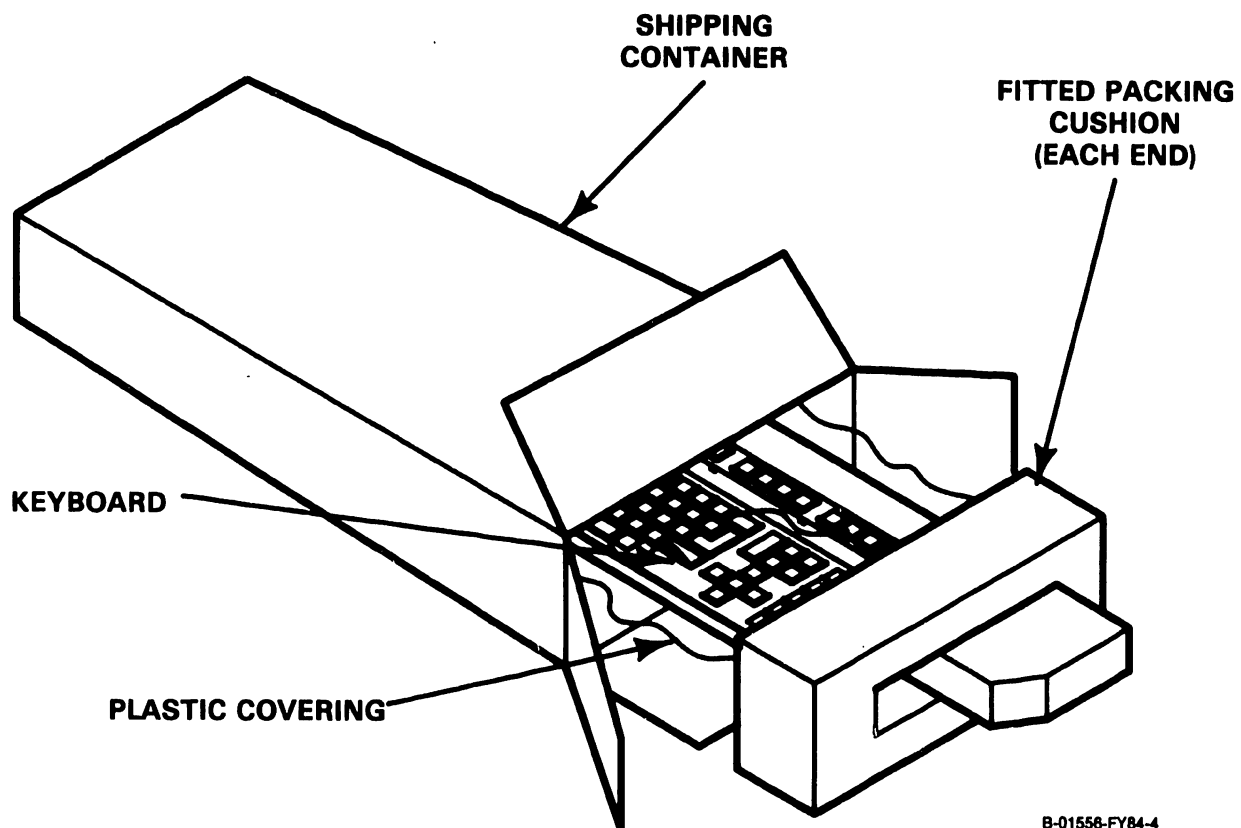
Figure 4-1. Unpacking the Monitor

4.2.2 UNPACKING (Continued)

4.2.2.2 Unpacking the Keyboard

Figure 4-2 shows the method used to pack the Keyboard. Use the following procedure to unpack it. Save all packing material until the unit has been found to function satisfactorily.

1. Carefully cut the tape sealing the end of the shipping container, being careful not to penetrate so deeply as to contact the contents. Open the shipping container.
2. Slide the Keyboard out of the shipping container and remove the plastic wrapping.



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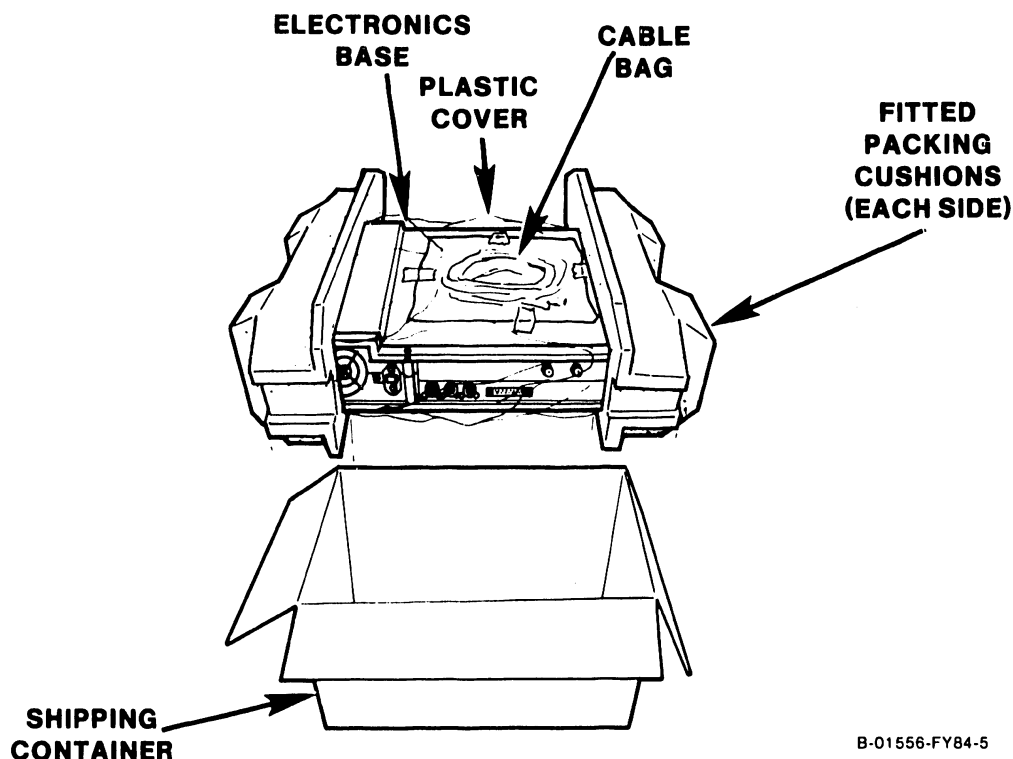
Figure 4-2. Unpacking the Keyboard

4.2.2 UNPACKING (Continued)

4.2.2.3 Unpacking the Electronics Base

Figure 4-3 shows the method used to pack the Electronics Base. Use the following procedure to unpack it. Save all packing material until the unit has been found to function satisfactorily.

1. Carefully cut the tape sealing the top of the shipping container, being careful not to penetrate so deeply as to contact the contents. Open the shipping container.
2. Lift the Electronics Base out of the shipping container along with its fitted packing cushions and the cable bag (taped to the Electronics Base wrapping).
3. Remove the fitted packing cushions and plastic wrapping from around the Electronics Base.



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Figure 4-3. Unpacking the Electronics Base

4.3 4230/05 WORKSTATION INSTALLATION PROCEDURES

The following subsections detail the installation procedures for the 4230/05 Workstations:

Section 4.3.1	Switch Settings
Section 4.3.2	System Interconnections
Section 4.3.3	Monitor Arm Option
Section 4.3.4	WS Interconnections

4.3.1 SWITCH SETTINGS

4.3.1.1 Internal Switches

The 4230/05 Workstations are shipped with all internal switches preset for proper operation. This eliminates the need to disassemble the Electronics Base unit and Keyboard at installation in order to access the internal switches. Switch settings are given in section 5.7 in Chapter 5 and are for reference only, as may be required when setting up a replacement or optional PCA or Keyboard.

4.3.1 SWITCH SETTINGS (Continued)

4.3.1.2 115V/230V Power Supply Switch

The setting of the 115V/230V Power Supply switch is required to ensure that the Power Supply is set for the ac voltage in use at the installation site. This is an easily accessible switch on the rear of the Electronics Base and is considered below.

CAUTION

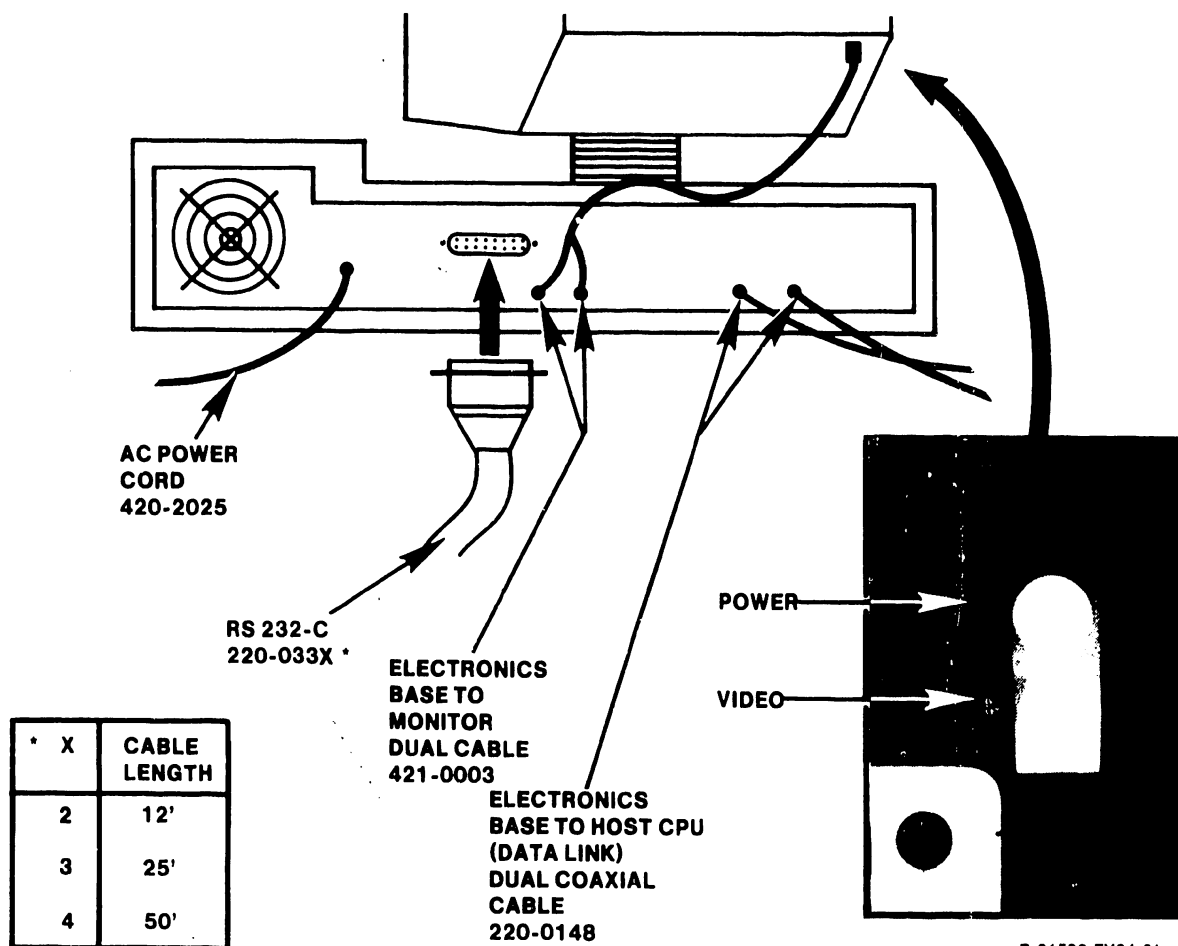
Applying power to the workstation with an incorrectly set Power Supply switch will damage the switching Power Supply. Warning stickers will be found placed over the I/O switch on the front of the Electronics Base and over the power cord receptacle on the rear of the Electronics Base to alert installation personnel to check the Power Supply switch setting before applying power to the unit.

4.3.1 SWITCH SETTINGS (Continued)

4.3.1.2 115V/230V PS Switch (Continued)

The workstation, powered from a single power supply in the Electronics Base, can be used with domestic power of 115 Vac at 60 Hz, or internationally with power of 230 Vac at 50 Hz. Switching between the two types of power is accomplished by means of a single switch accessible on the rear of the Electronics Base (refer to Figure 4-4). Proceed as follows:

- Slide the 115V/230V switch either up or down so that the power at the installation site is readable on the switch, either 115V or 230V.



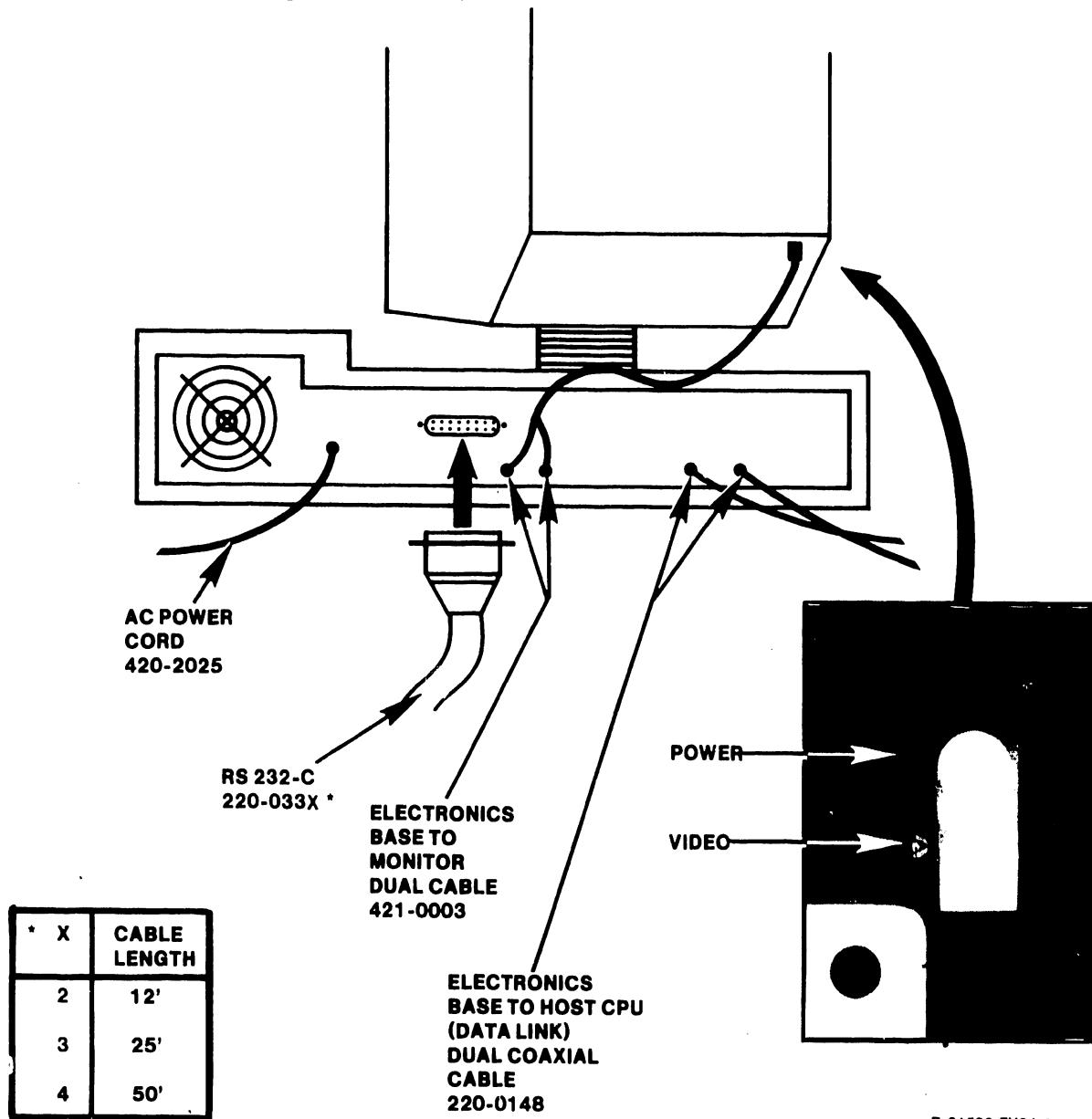
Note: RS232-C connector is available only on 4230 workstations.

Figure 4-4. 4230/4205 WS Interconnections

4.3.1 SWITCH SETTINGS (Continued)

4.3.1.2 115V/230V PS Switch(Continued)

2. Remove the warning sticker over the power cord receptacle on the rear of the Electronics Base unit.
3. Remove the warning sticker over the 1/0 (on/off) switch on the front of the Electronics Base.



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Note: RS232-C connector is available only on 4230 workstations.

4.3.2 SYSTEM INTERCONNECTIONS

4.3.2.1 Workstation to Host CPU Cable

The standard interconnecting cable supplied for connecting the workstation to the host CPU is a 25-foot, dual coaxial cable with a BNC/TNC connector pair at each end. The standard cable, part number 220-0148, is packed with the Electronics Base.

The distance between the workstation and the host CPU can be extended from the standard 25 feet to 2000 feet by using optional dual coaxial cables available under the following part numbers: (Refer to Customer Site Planning Guide, 700-5978.)

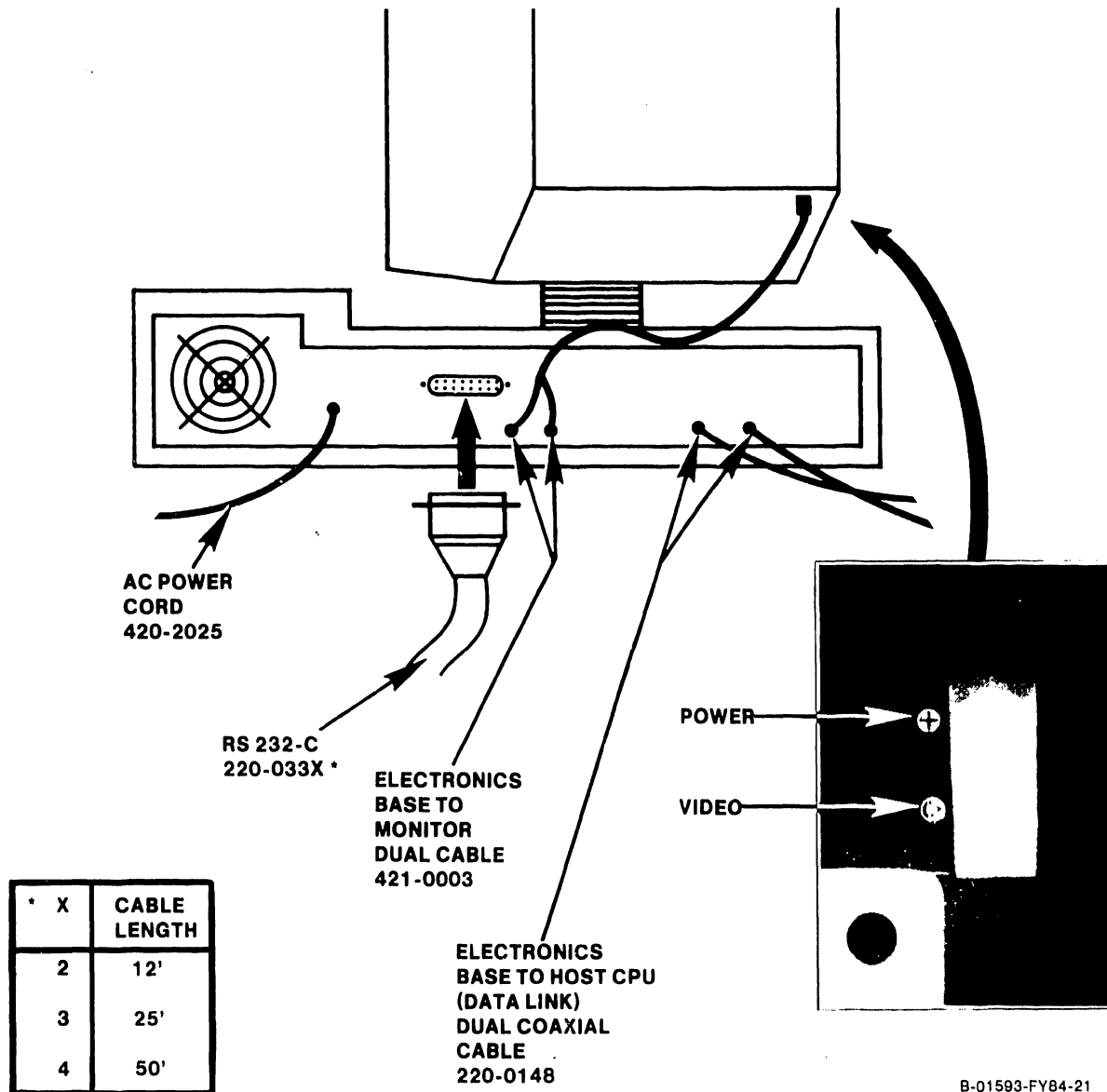
LENGTH (FT.) PART NUMBER

50	120-2300-1
100	120-2300-2
150	120-2300-3
-	-
-	-
2000	120-2300-40

4.3.2 SYSTEM INTERCONNECTIONS (Continued)

4.3.2.2 Connecting the WS to the Host CPU

In VS systems, connect a dual coaxial cable from the DATA LINK connectors on the rear of the Electronics Base, to the serial IOP dual BNC/TNC connector panel of the host CPU. In WP/OIS systems (4230 only), the dual coaxial cable connects directly to the host CPU (OIS Master). These connections are a BNC/TNC pair and can only be connected BNC to BNC, TNC to TNC. The length of this cable is not to exceed 2000 feet.



Note: RS232-C connector is available only on 4230 workstations.

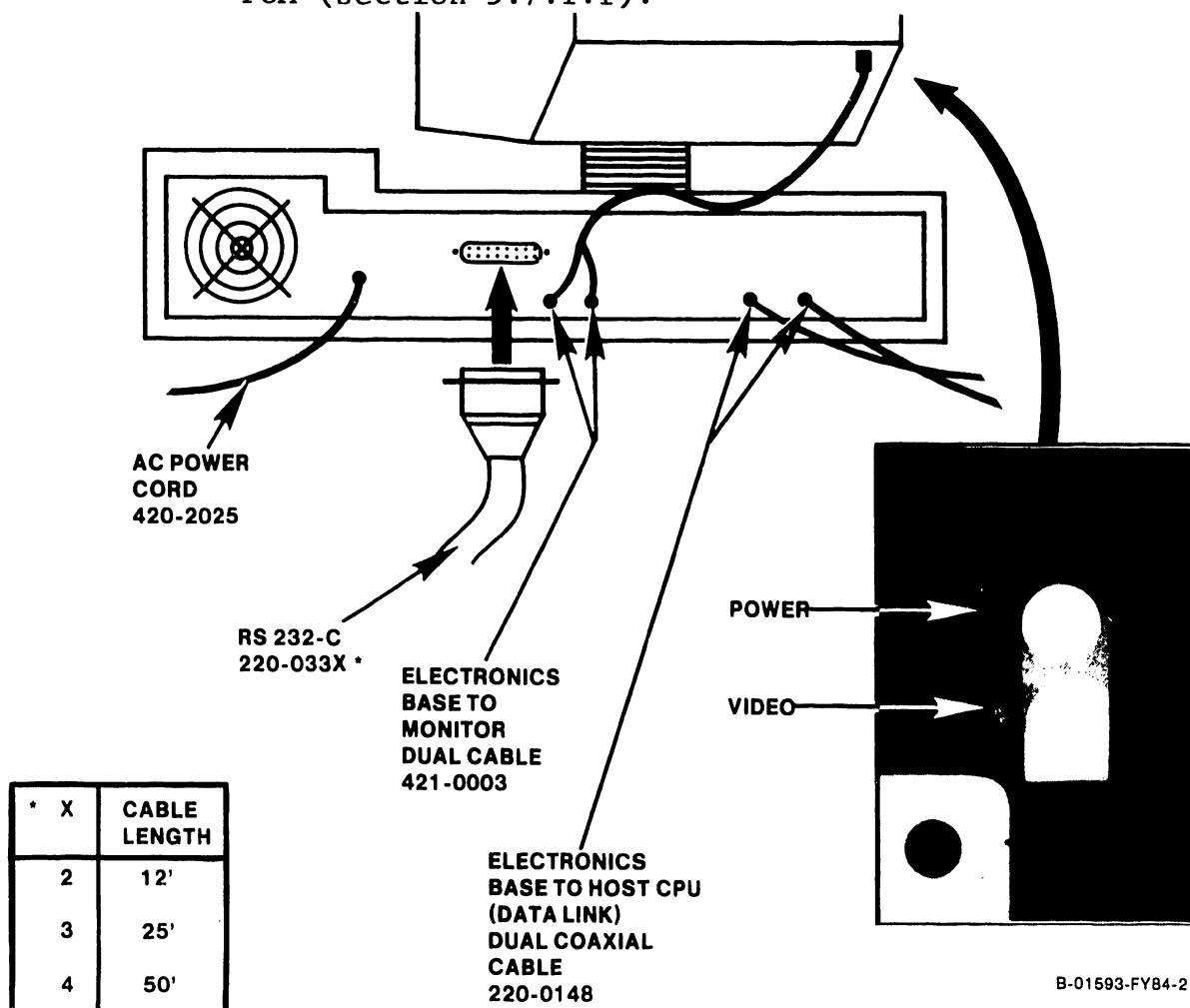
4.3.2 SYSTEM INTERCONNECTIONS (Continued)

4.3.2.3 4230 Telecommunications Installation

If the workstation has been ordered with the telecommunications (TC) option, a 210-8298 PCA will have been installed and tested at the factory.

For field installation of the 4230 TC option:

- o connect the TC cable between the TC connector on the rear of the workstation and to the appropriate modem (figure 4-4).
- o set the TC option switches on the 210-8287 PCA (section 5.7.1.1).

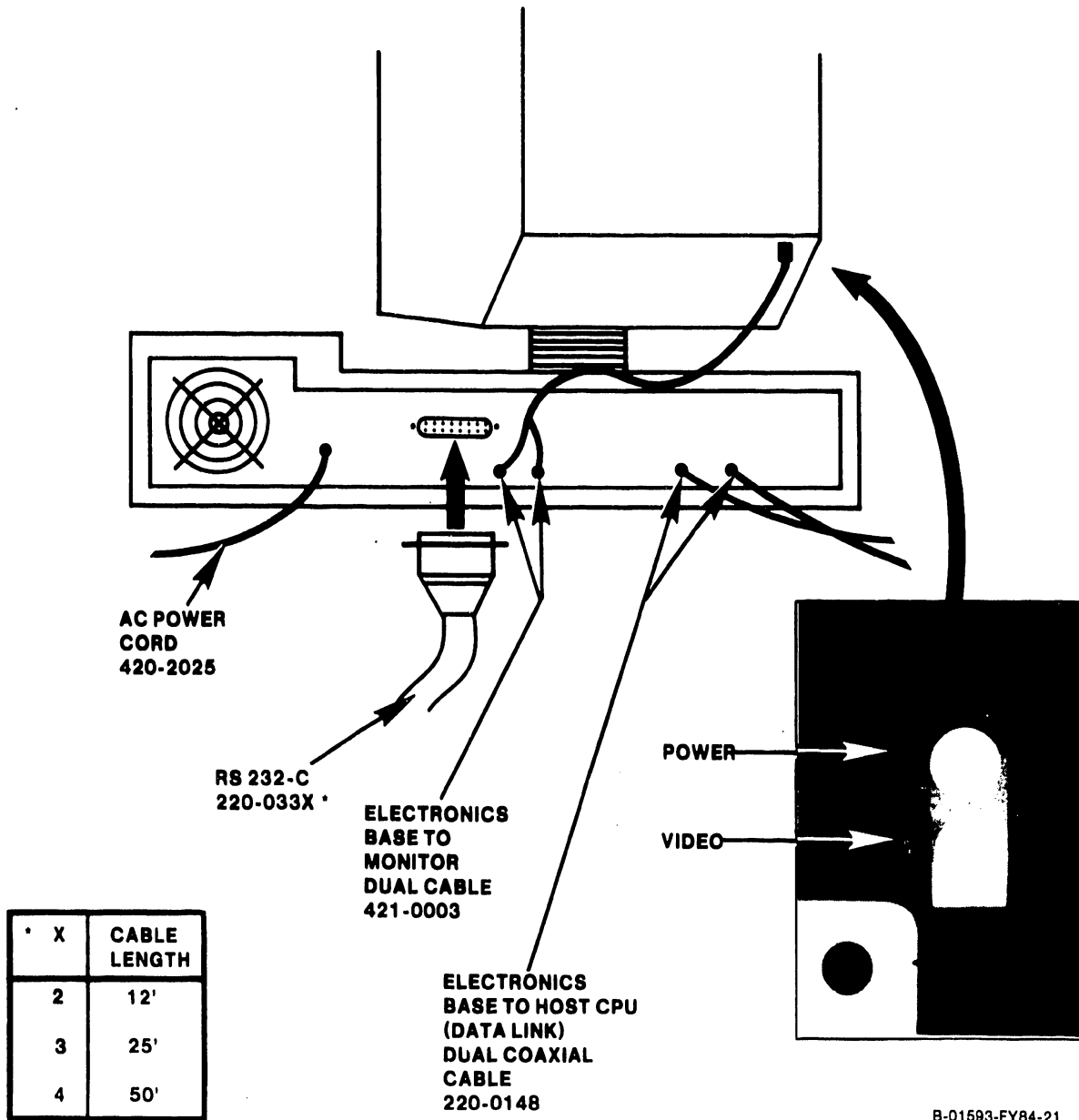


Note: RS232-C connector is available only on 4230 workstations.

4.3.2 SYSTEM INTERCONNECTIONS (Continued)

4.3.2.3 4230 TC Installation(Continued)

- o set the switch on the 210-8298 PCA (section 5.7.1.1).
- o ensure that the proper software has been loaded into the system.



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Note: RS232-C connector is available only on 4230 workstations.

4.3.2.3 4230 TC Installation (Continued)

4.3.2.3.1 Telecommunications Cabling

Modem Cable

25-conductor cable with 25-pin RS-232-C male connectors on each end for connection of the workstation to a modem.

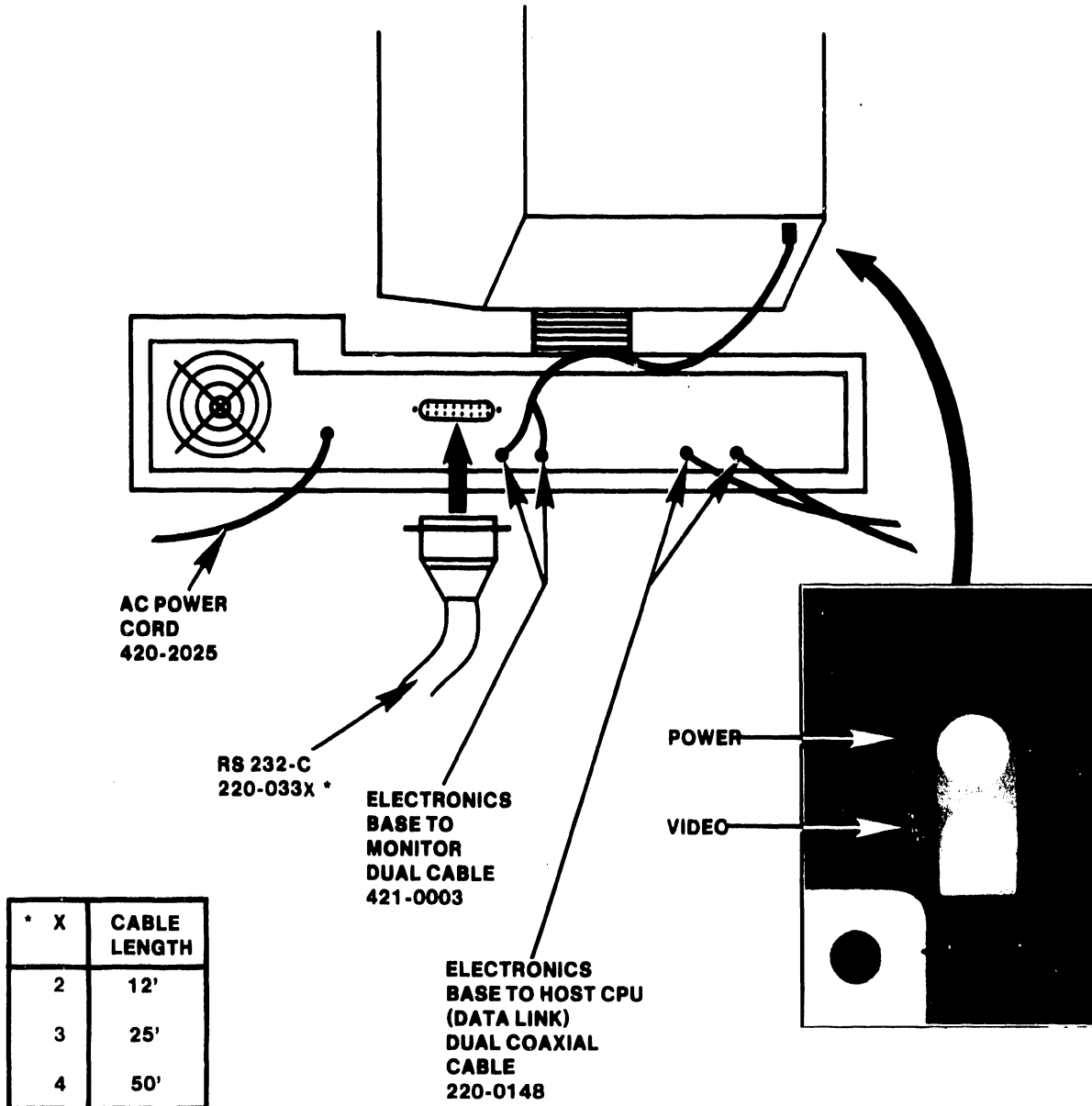
Direct Connection Jumper

(Null Modem) - When connecting the workstation to another computer or terminal device in physical proximity to the workstation, this jumper renders the use of modems unnecessary. A normal modem cable may be used between the workstation and the computer/terminal/word processor.

4.3 4230/05 WS INSTALLATION (Continued)

4.3.3 MONITOR ARM OPTION

The Monitor arm option installation guide, document part number 700-8695, is packed with the option. Note that an 8-foot Monitor-to-Electronics Base cable is supplied as part of that option and is used instead of the shorter 2-foot cable supplied with the workstation as standard equipment. The option is customer-installable.



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Note: RS232-C connector is available only on 4230 workstations.

4.3 4230/05 WS PROCEDURES (Continued)

4.3.4 Workstation Interconnecting Cables

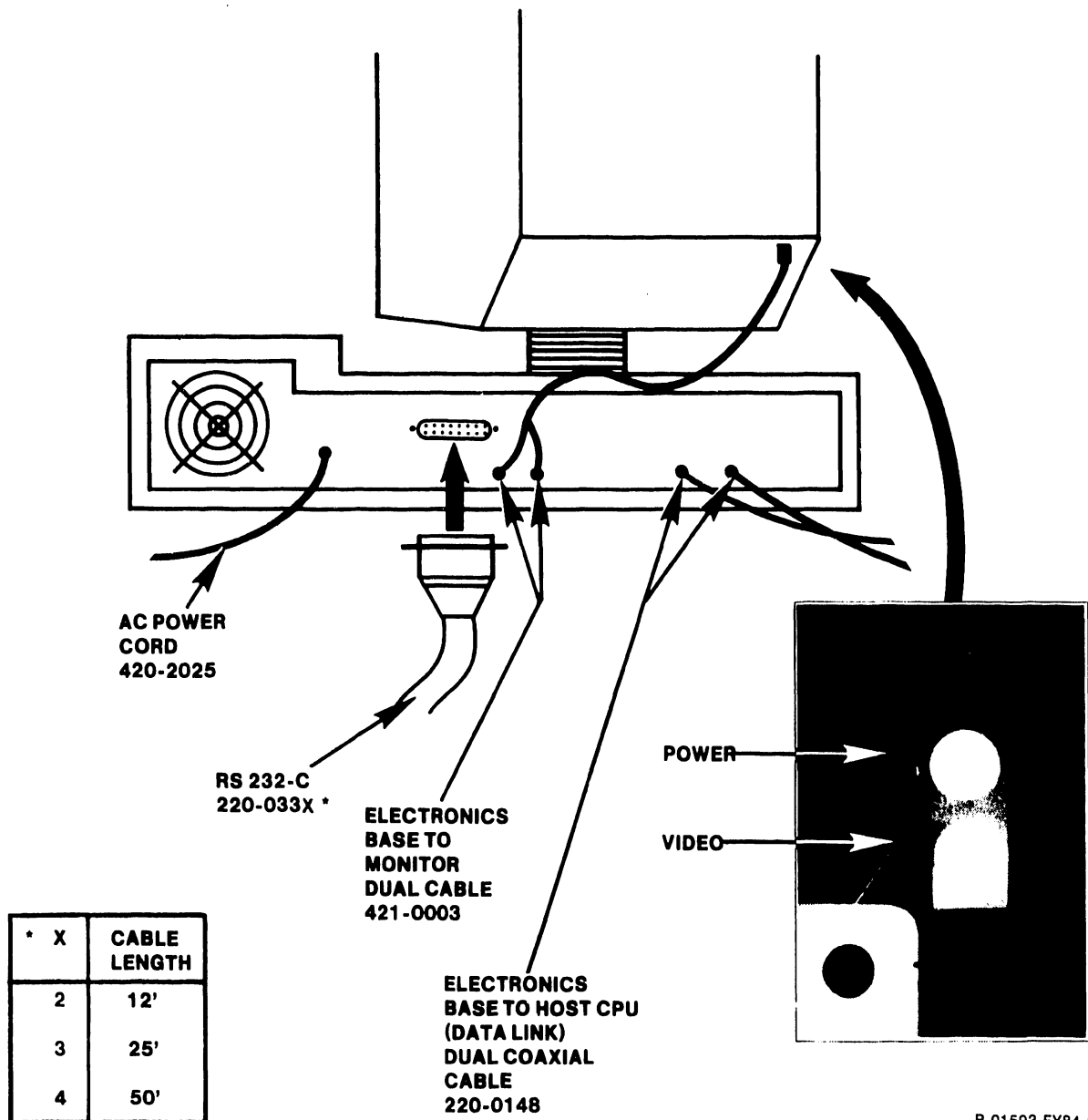
The cables required to interconnect the Monitor, Keyboard and Electronics Base are supplied with the workstation. Information regarding these cables is given below.

<u>CABLE DESCRIPTION</u>	<u>PACKED WITH</u>	<u>LENGTH</u>	<u>PART NUMBER</u>
Elec. Base-to-Monitor Cable, Monitor Power: 3-Pin DIN Monitor Video: 8-Pin DIN	Electronics Base	2 Feet	421-0003
Keyboard-to-Electronics Base, 4-Pin DIN one end, hard-wired internally to Keyboard, coiled	Keyboard	1 Foot, Retracted	220-0305
Electronics Base-to-AC Power, 3-Prong male one end, 3-Prong female other end	Electronics Base	6 feet	420-2025

4.3 4230/05 WS INSTALLATION (Continued)

4.3.5 INTERCONNECTING MONITOR, KB, BASE

1. Insert the Keyboard 4-pin DIN plug into the KYBD connector on the rear of the Electronics Base.
2. Place the Monitor on its top and locate the power and video connectors on its underside. These connectors are identified by symbols as shown in below.



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Note: RS232-C connector is available only on 4230 workstations.

4.3 4230/05 WS INSTALLATION (Continued)

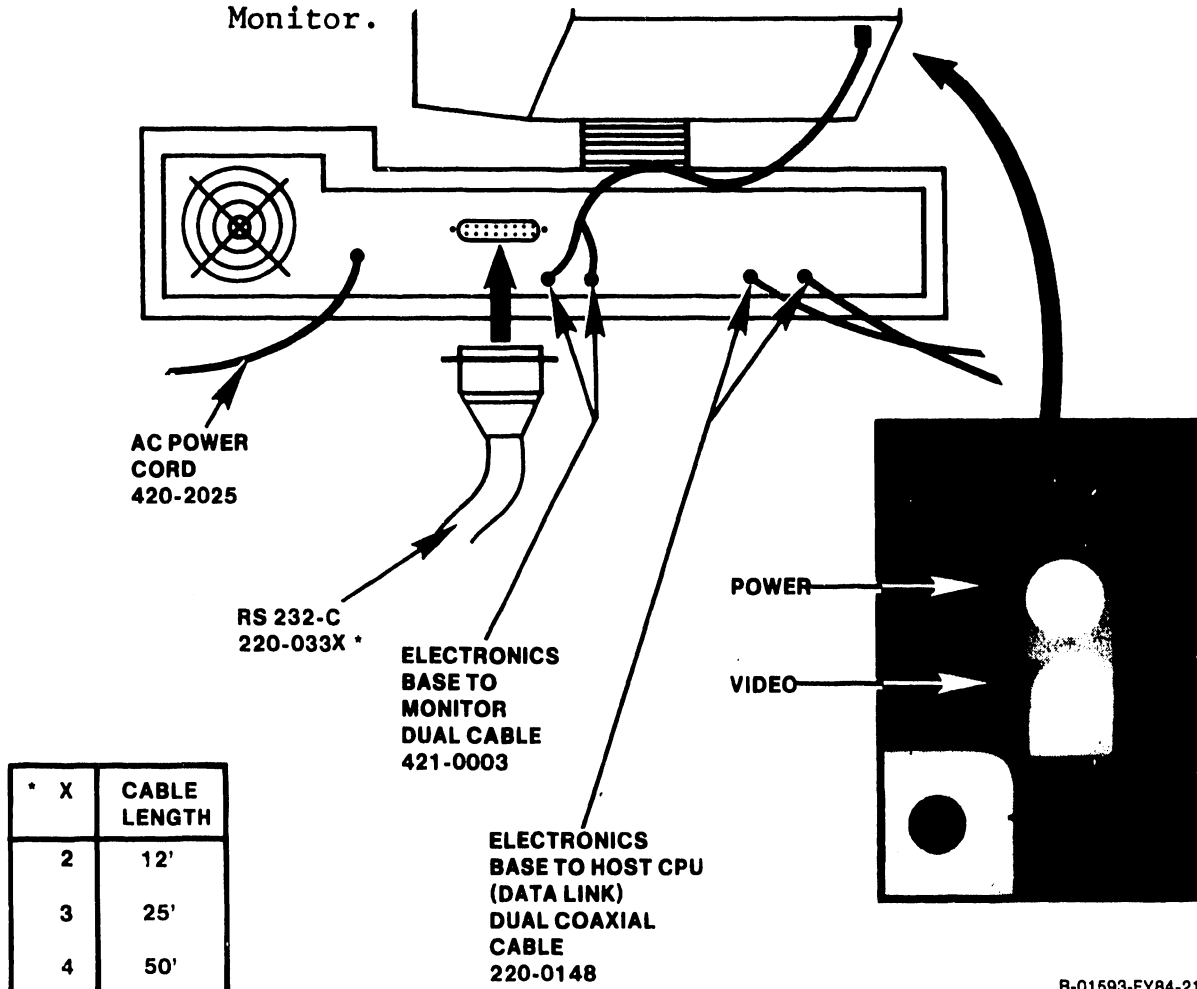
4.3.5 INTERCONNECTING MON., KB, BASE (Cont'd)

NOTE

In the following steps, make certain that the cable connectors are fully seated by pushing them in to the full extent of their travel.

3. Insert the Monitor video 8-pin DIN plug into the video connector on the underside of the Monitor.

4. Insert the Monitor power 3-pin DIN plug into the power connector on the underside of the Monitor.



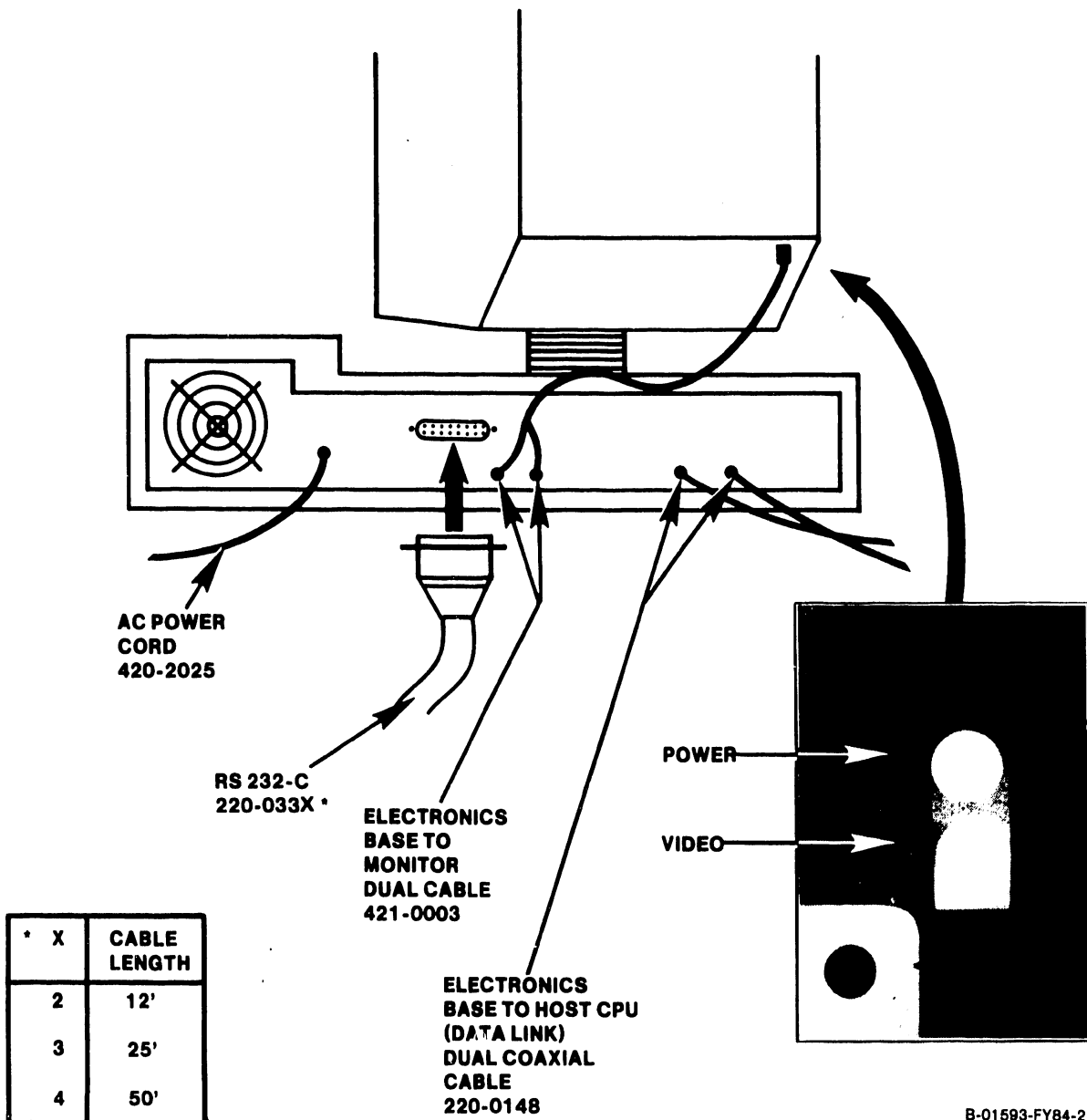
B-01593-FY84-21

Note: RS232-C connector is available only on 4230 workstations.

4.3 4230/05 WS INSTALLATION (Continued)

4.3.5 INTERCONNECTING MONITOR, KB, BASE (Cont'd)

5. Place the Monitor platform in the depression in the top of the Electronics Base, cables toward the rear of the Electronics Base.
6. Insert the Monitor video 8-pin DIN plug into the VIDEO connector on the rear of the Electronics Base.



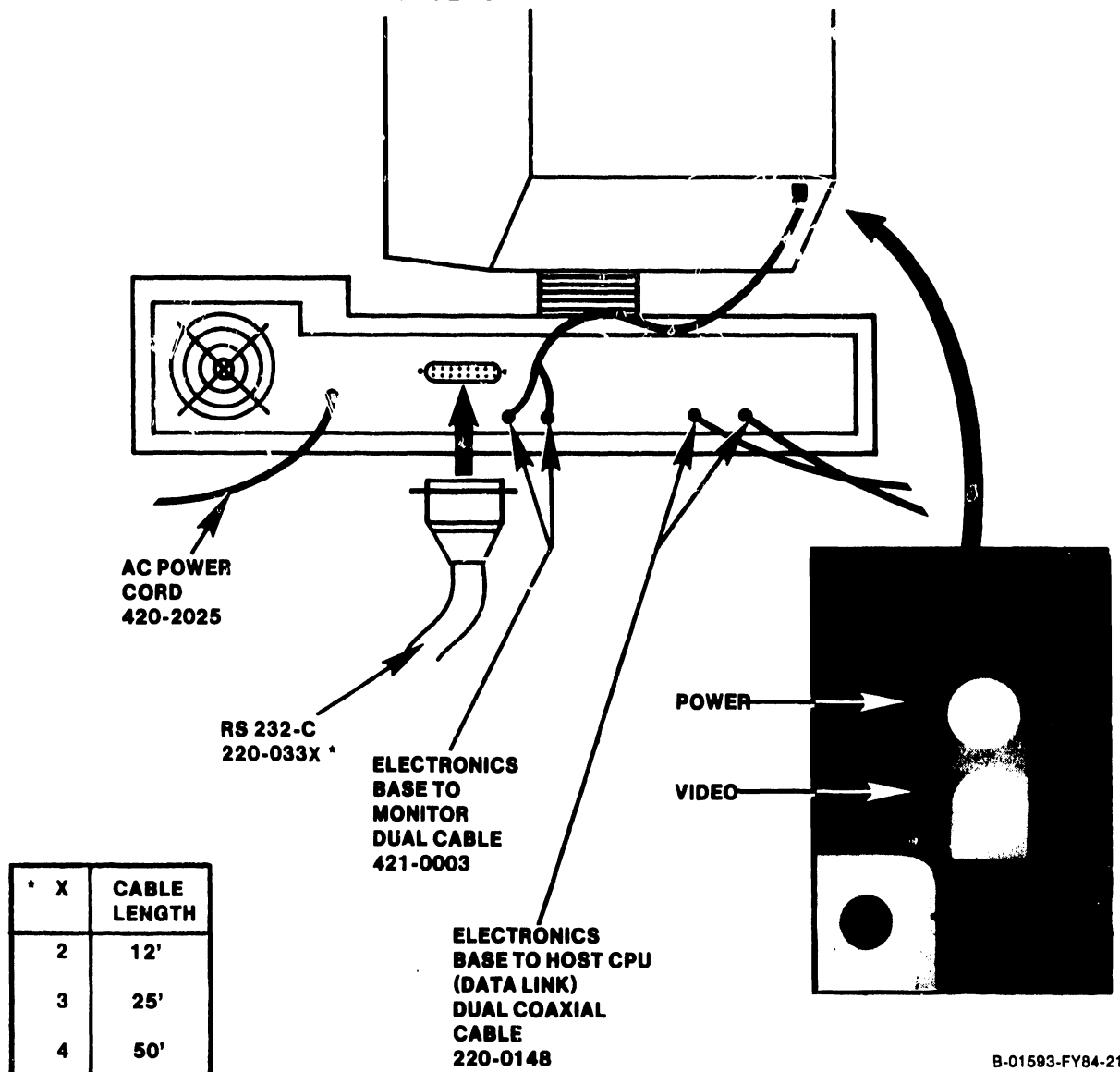
B-01593-FY84-21

Note: RS232-C connector is available only on 4230 workstations.

4.3 4230/05 WS INSTALLATION (Continued)

4.3.5 INTERCONNECTING MONITOR, KB, BASE (Cont'd)

7. Insert the Monitor power 3-pin DIN plug into the PWR CRT connector on the rear of the Electronics Base.
8. Plug the female end of the power cord into its receptacle on the rear of the Electronics Base. Secure with two screws. Do not overtighten. Plug the ac power cord into a suitable outlet.



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Note: RS232-C connector is available only on 4230 workstations.

4.4 POST-INSTALLATION CHECKS4.4.1 SYSTEM SOFTWARE COMPATIBILITY

The table below defines the minimum release levels of VS, OIS and Alliance operating systems which support the 4230/05 Workstations. In addition, for VS systems, the microcode file name and revision is also given for each microcode file. Information given in this manual is compatible with the workstation microcode given below.

<u>MODEL</u>	<u>O/S</u>	<u>VS</u>		<u>OIS</u>	<u>ALLIANCE</u>	
		<u>uCODE</u>	<u>VERSION</u>		<u>O/S</u>	<u>O/S</u>
		<u>FILE NAME</u>				
4230	06.20.00	@MC4230@	06.00.00	8.3	4.J	1.0
4205	06.11.02	@MC4205	06.00.00			

4.4 POST-INSTALLATION CHECKS

4.4.2 SYSGEN CONSIDERATIONS (VS SYSTEMS ONLY)

The 4230/05 Workstations can be entered on the serial IOP screen of the GENEDIT menu by their model numbers. In other words, enter 4230 for the 4230 Workstation and enter 4205 for the 4205 Workstation.

4.4.3 WORKSTATION TURN-ON

To initially turn on the 4230/05 Workstation, simply press 1 (on) on the 1/0 (on/off) switch on the front panel of the Electronics Base. When power is applied the following actions ensue:

- The workstation's internal fan starts
- A short beep sounds
- The BIT (Built-In Test) begins to run
- the Keyboard LEDs will flash on and off
- The monitor will begin to display various test patterns, although this may not be visible if the CRT has not warmed up sufficiently. Refer to section 4.5 or 4.6 for details on the 4230 or 4205 BIT respectively.

After successful completion of the BIT, the host CPU will execute the IPL (Initial Program Load) sequence. When the IPL is completed, the Monitor will display the LOGON/DOS screen.

4.4 POST-INSTALLATION CHECKS (Continued)

4.4.3 WORKSTATION TURN-ON (Continued)

If the LOGON/DOS screen does not appear, adjust the Brightness and Contrast controls at the upper left edge of the Monitor front panel (Figure 3-1).

NOTE

If the LOGON/DOS screen does not appear, refer to Chapter 8 of this manual for troubleshooting procedures.

After the LOGON/DOS screen has been obtained, the unit can be turned over to the customer.

4.5 4230/05 POWER UP DIAGNOSTICS

4.5.1 DESCRIPTION

The 4230/05 Workstation BIT program resides in a 4k PROM at location L38 on the 8287 PCA. The BIT can be used for fault isolation to the board or subassembly level.

The BIT runs certain tests automatically each time the workstation is powered on (section 4.5.4.1), and error messages resulting from failed tests are displayed on the Monitor CRT (section 4.5.6). Test status and results can also be determined by the state of the Keyboard LEDs (section 4.5.5). Additionally, a diagnostic LED on the 8287 PCA indicates the state of the diagnostic testing, whether in progress, passed or failed (section 4.5.7).

In addition to the tests that run automatically at each power-up, other modes are included which are selected by entering the appropriate keystrokes after power-up of the workstation (sections 4.5.4.2 through 4.5.4.7).

4.5.2 REVISION HISTORY AND ORDERING INFORMATION

	<u>4230</u>	<u>4205</u>
Release Date:	Jan. 03, 1984	Jan. 26, 1984
Package Part Number:	195-2697-3	195-2838-3
Documentation Revision:	93C4	93C5
Documentation Part Number:	760-1206A	760-1219A
Software Revision:	53C4	53C5
Software Part Number:	702-0270A	702-0279A
PROM Part Number:	378-8046R1	378-8051R1

4.5 4230/05 POWER UP DIAGNOSTICS (Continued)

4.5.3 TESTS IN THE PROGRAM

The tests provided in the BIT are listed below.
Note that the data link is not tested by the BIT.

<u>NO.</u>	<u>NAME OF TEST</u>	<u>HARDWARE TESTED</u>
2	PROM Checksum	Diagnostic PROM
3	Parity generating	Parity generation and detection
4	Main memory	Main memory
5	Memory select	Memory select logic
6	Char. and attribute RAM	CRT RAM
7	Font memory	Font RAM
8*	Secondary font memory	Secondary font RAM
9	Memory refresh	Main memory refresh logic
A*	TC	Tests for presence of TC PCA
B	Keyboard	Tests for presence of Keyboard
C	Keyboard strike	Keyboard
D*	TC loopback	TC drivers
E	Video Display Pattern	Visual display test of video circuits; attributes exercised. In 4230, scrolling exercised.

* 4230 Only

4.5.4 OPERATING INSTRUCTIONS

The following sections describe the currently supported modes of the 4230/05 Workstation BIT and how to implement them.

When power is initially applied to the unit, it will idle for two seconds waiting for the CANCEL key to be pressed. If CANCEL is not pressed within two seconds of power-up, normal power-up mode will be entered (section 4.5.4.1).

4.5 4230/05 POWER UP DIAGNOSTICS (Continued)

4.5.4 OPERATING INSTRUCTIONS (Continued)

If CANCEL is pressed within two seconds of power-up, the operator will have an additional two seconds to press a key associated with one of the other modes (sections 4.5.4.2 through 4.5.4.7), thus entering that mode. If an additional key is not pressed to select one of the other BIT modes, normal power-up mode will be entered.

4.5.4.1 Normal Power-Up

The normal power-up sequence performs tests 2 through B as listed in section 4.5.3, essentially testing all circuitry visible to the CPU. If an error is found, testing stops and an error indication is given on the CRT (section 4.5.6) and on the Keyboard (section 4.5.5), and IPL is inhibited. If the unit is good, the host CPU will down-load workstation microcode and the LOGON/DOS screen will appear.

4.5.4 OPERATING INSTRUCTIONS (Continued)

4.5.4.2 Skip BIT

This mode allows the unit to be used if it has a non-fatal hardware fault. No testing is performed, and the host processor can IPL the unit. To skip the BIT:

1. Power on the unit, wait for the LED adjacent to the CANCEL key to light and immediately press CANCEL.
2. Within two seconds after pressing CANCEL, press INDENT. The LOGON/ DOS screen will appear.

4.5.4.3 Loop on BIT

This provision allows the normal power-up test to repeat indefinitely, as long as no errors are detected. No loop count is provided.

To loop on the BIT:

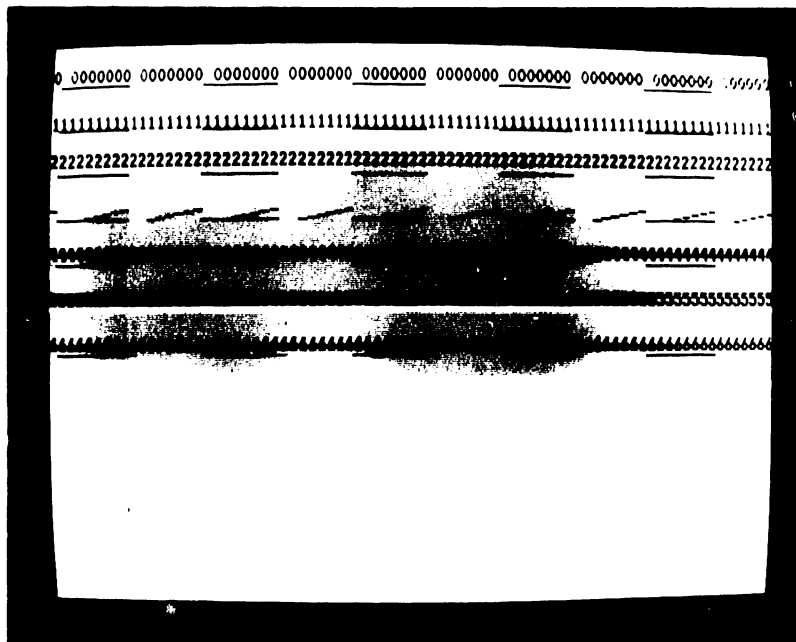
1. Power on the unit, wait for the LED adjacent to the CANCEL key to light and immediately press CANCEL.
2. Within two seconds after pressing CANCEL, press PAGE.

If an error is found, testing stops and an error indication is given on the CRT (section 4.5.6) and on the Keyboard (section 4.5.5). To cancel the test, shut unit off (1/0 switch to 0).

4.5.4 OPERATING INSTRUCTIONS (Continued)

4.5.4.4 Video Test Patterns

This mode presents a pattern on the Monitor's CRT screen for verifying that the video controller logic in the Electronics Base is functional. Eight lines of numeric characters are displayed, numbered 0-7, with the exception of line three which is not numbered. Video attributes such as blink, reverse video, underline and double underline are exercised on some of the lines. In the 4230, line three displays a diagonal bar with and without underline. In the 4205, line three is blank. In the 4230, scroll right and scroll left are also exercised (Figure 4-5a).



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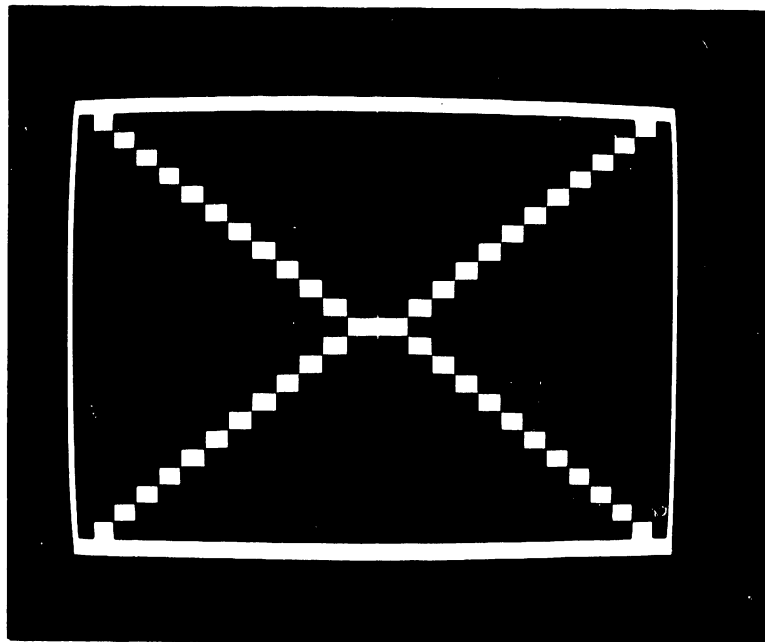
Figure 4-5a. 4230/05 BIT Video Test Patterns
Dynamic Test Pattern (4230 Shown)

4.5.4 OPERATING INSTRUCTIONS (Continued)

4.5.4.4 Video Test Patterns (Continued)

An alternate pattern accessible in this mode provides a large X painted on the screen with a perimeter outline of the 6 x 8-inch area in which video is displayed. (Refer to Figure 4-5b.) This perimeter outline can be used for some Monitor adjustments as noted in Chapter 5.

During the video pattern display, no internal testing is performed. The display must be viewed for proper display of the test patterns.



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Figure 4-5b. 4230/05 BIT Video Test Patterns
Static Test Pattern

4.5.4 OPERATING INSTRUCTIONS (Continued)

4.5.4.4 Video Test Patterns (Continued)

To display the BIT video patterns:

1. Power on the unit, wait for the LED adjacent to the CANCEL key to light and immediately press CANCEL.
2. Within two seconds after pressing CANCEL, press CENTER.
3. If desired, press any key except CANCEL to switch between the test patterns and the large X with perimeter outline.
4. If desired, press CANCEL to return to the beginning of the normal power-up test sequence.
5. If desired, press SHIFT/CANCEL to release the workstation to the operating system for IPL.

4.5.4.5 External Loopback (4230 Only)

This mode tests the telecommunications (TC) circuitry on the 8298 TC board, thus allowing TC faults to be isolated between the workstation and external TC equipment.

4.5.4 OPERATING INSTRUCTIONS (Continued)

4.5.4.5 External Loopback (4230 Only) (Cont'd)

The test requires a standard RS-232 loopback connector (WLI P/N 420-1040) to be connected to the RS-232 connector on the rear panel of the Electronics Base unit. Once the test is initiated, it continuously loops and the pass count is displayed on the second line of the CRT in hexadecimal notation. If an error is found, testing stops and an error indication is given on the CRT (section 4.5.6), and the Keyboard LEDs display the failed test number (section 4.5.5). Additionally, the pass count freezes, displaying the number of times the test was run before the error occurred.

To run the external loopback test:

1. Power on the unit, wait for the LED adjacent to the CANCEL key to light and immediately press CANCEL.
2. Within two seconds after pressing CANCEL, press FORMAT.
3. If desired, press CANCEL to return to the beginning of the normal power-up test sequence.
4. If desired, press SHIFT/CANCEL to release the workstation to the operating system for IPL.

4.5.4 OPERATING INSTRUCTIONS (Continued)

4.5.4.6 Refresh Test (4205 Only)

This mode tests the memory refresh circuits of the 8287 PCA. The test writes a 55 pattern in memory, waits 15 seconds and then reads memory to check memory integrity. Once the test is initiated, it continuously loops and the pass count is displayed on the second line of the CRT in hexadecimal notation. If an error is found, testing stops and an error indication is given on the CRT (section 4.5.6), and the Keyboard LEDs display the failed test number (section 4.5.5). Additionally, the pass count freezes, displaying the number of times the test was run before the error occurred. To run the refresh test:

1. Power on the unit, wait for the LED adjacent to the CANCEL key to light and immediately press CANCEL.
2. Within two seconds after pressing CANCEL, press DECTAB.

To cancel the test, shut unit off (1/0 switch to 0).

4.5.4 OPERATING INSTRUCTIONS (Continued)

4.5.4.7 Keyboard Test

Selection of this test clears the CRT for display of the hexadecimal keycode of any key the operator presses. The test displays the keycode exactly as it is received. To run the Keyboard test:

1. Power on the unit, wait for the LED adjacent to the CANCEL key to light and immediately press CANCEL.
2. Within two seconds after pressing CANCEL, press SEARCH.
3. Press any key and compare the CRT display with the hexadecimal code assigned to that key as shown in Table 4-1 (Next Frame).
4. If desired, press SHIFT/CANCEL to return to the beginning of the normal power-up test sequence.

4.5.4 OPERATING INSTRUCTIONS (Continued)

4.5.4.7 Keyboard Test

Table 4-1. Universal Serial KB Hex (XY) Codes

CODE	COMMENT	CODE	COMMENT	CODE	COMMENT	CODE	COMMENT
00		20	Int'l	40	5 (P)	60	Unuseable
01	Query Response	21	Int'l	41	4 (P)	61	Prev
02		22	Int'l	42	- (P)	62	Insert
03		23	Int'l	43	+ (P)	63	Multiply(P)
04		24	Control	44	Return	64	=
05		25	2nd	45	'	65	0
06		26	Home	46	;	66	9
07		27	Unuseable	47	L	67	8
08		28	S Cursor	48	K	68	7
09		29	N Cursor	49	J	69	6
0A		2A	.	4A	H	6A	5
0B		2B	Backspace	4B	G	6B	4
0C		2C	Space bar	4C	F	6C	3
0D		2D	W Cursor	4D	D	6D	2
0E		2E	E Cursor	4E	S	6E	1
0F		2F	-	4F	A	6F	Tab
10	3 (P)	30	2 (P)	50	7 (P)	70	Blank Key
11	Go to	31	1 (P)	51	Next	71	Sub/super
12	Cancel	32	Unuseable	52	Delete	72	Command
13	Unuseable	33	Period (P)	53	Execute	73	Move
14	Unuseable	34	O (P)	54	Glossary	74	Copy
15	8 (P)	35	Right Shift	55]	75	Replace
16	9 (P)		(not visible)	56	P	76	Search
17	6 (P)	36	Help	57	O	77	Stop
18	Divide (P)	37	/	58	I	78	Note
19	Print	38	,	59	U	79	Merge
1A	Erase	39	M	5A	Y	7A	Format
1B	Left Shift	3A	N	5B	T	7B	Dec Tab
	(not visible)	3B	B	5C	R	7C	Center
1C	Return (P)	3C	V	5D	E	7D	Page
1D	Int'l	3D	C	5E	W	7E	Indent
1E	Lock (not visible)	3E	X	5F	Q	7F	Unused
1F	Back Tab	3F	Z				

NOTES:

Keys marked "Unuseable" are in defined locations.

The codes 00 to 0F are reserved for control functions.

4.5.4 OPERATING INSTRUCTIONS (Continued)

4.5.4.7 Keyboard Test

These codes cannot be sent by pressing a key on the keyboard.

Codes marked "Int'l" are reserved for the International keyboard and exist only on the universal expanded keyboard.

The keyboard defaults to having the left and right shift keys generate make and break codes. The break code will be the x/y value of the depressed key OR-ed with an 80 bit.

Keys designated (P) are keypad keys.

4.5.4.8 Summary of Operator-Invoked BIT Functions

<u>Function</u>	<u>Press</u>	<u>Remarks</u>
Skip BIT	CANCEL, INDENT	
Loop on BIT	CANCEL, PAGE	
Video Pattern	CANCEL, CENTER	
External Loopback	CANCEL, FORMAT	4230 Only
Refresh	CANCEL, DECTAB	4205 Only
Keyboard	CANCEL, SEARCH	

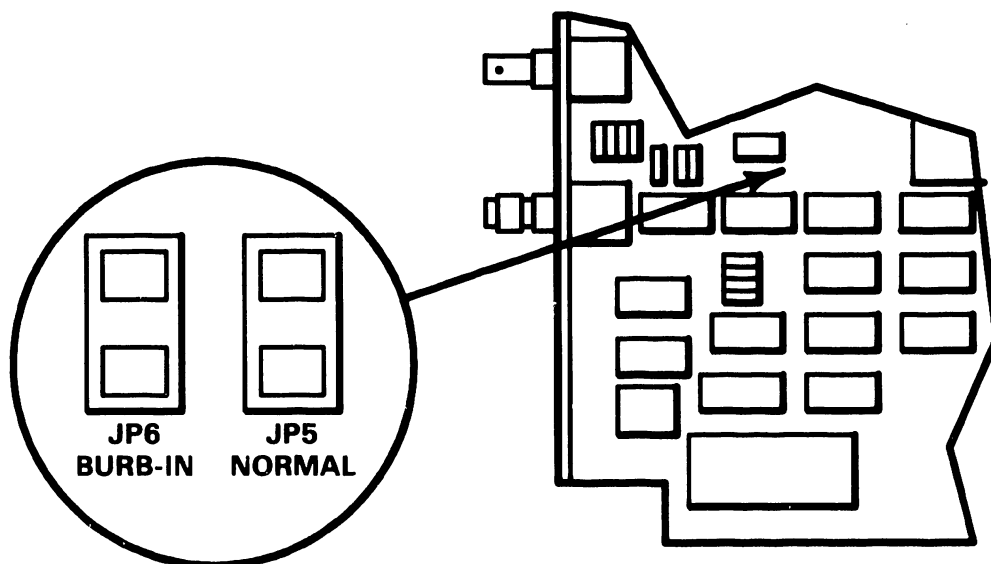
4.5.4 OPERATING INSTRUCTIONS (Continued)

4.5.4.9 Burn-In Mode

This mode causes the the normal power-up sequence to be repeated indefinitely, as long as no errors occur. In addition, the Keyboard controller is tested. A loop count is displayed on the second line of the CRT display in hexadecimal notation.

To activate the burn-in mode in the 4230 Workstation (Refer to Figure 4-6):

1. Remove the jumper link from JP5 and connect it to JP6.
2. Power on the workstation.



JUMPER CONFIGURATION 210-8287

J	IN	OUT
JP1	X	
JP2	X	
JP3	---- DOES NOT EXIST ----	
JP4		X
JP5	X	
JP6		X
JP7	X	
JP8	X	

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Figure 4-6. Burn-In Mode Jumpers, J5 and J6

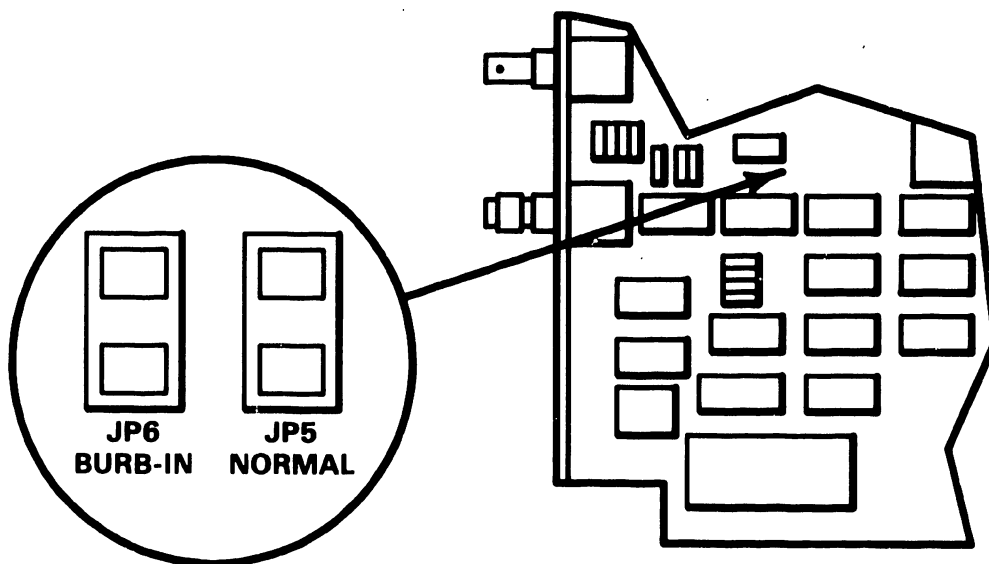
4.5.4 OPERATING INSTRUCTIONS (Continued)

4.5.4.9 Burn-In Mode (Continued)

If an error is found, testing stops and an error indication is given on the CRT (section 4.5.6) and on the Keyboard (section 4.5.5). To cancel the burn-in mode, power off the workstation and reinstall the jumper link on JP5.

To activate the burn-in mode in the 4205 Workstation:

1. Power on the unit, wait for the LED adjacent to the CANCEL key to light and immediately press CANCEL.



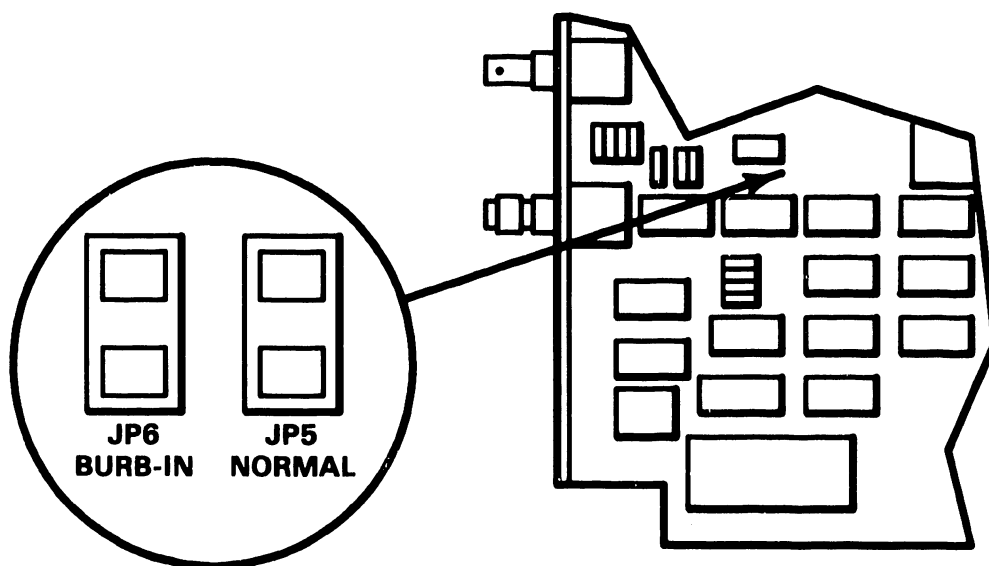
JUMPER CONFIGURATION 210-8287

J	IN	OUT
JP1	X	
JP2	X	
JP3	---- DOES NOT EXIST ----	
JP4		X
JP5	X	
JP6		X
JP7	X	
JP8	X	

4.5.4 OPERATING INSTRUCTIONS (Continued)

4.5.4.9 Burn-In Mode (Continued)

2. Within two seconds after pressing CANCEL, press PAGE.
3. Remove the jumper link from JP5 and connect it to JP6. Note that if the jumper link is connected to JP6 before powering on the unit, the burn-in test will exit after one pass.



JUMPER CONFIGURATION 210-8287

J	IN	OUT
JP1	X	
JP2	X	
JP3	---- DOES NOT EXIST ----	
JP4		X
JP5	X	
JP6		X
JP7	X	
JP8	X	

4.5.4 OPERATING INSTRUCTIONS (Continued)

4.5.4.9 Burn-In Mode (Continued)

If an error is found, testing stops and an error indication is given on the CRT (section 4.5.6) and on the Keyboard (section 4.5.5). To cancel the burn-in mode, power off the workstation and reinstall the jumper link on JP5.

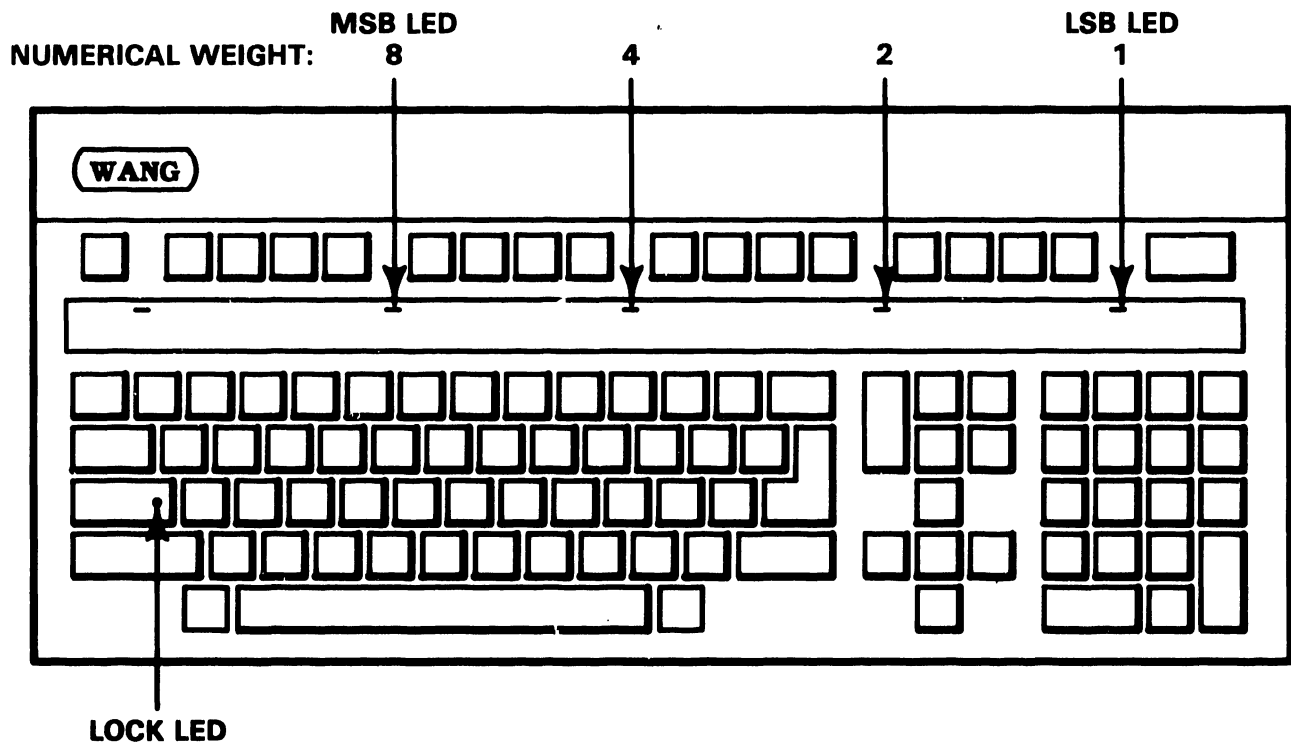
4.5 4230/05 POWER UP DIAGNOSTICS (Continued)

4.5.5 KEYBOARD LED DISPLAYS

The Keyboard contains light-emitting diodes (LEDs) used by the BIT program for displaying BIT testing status. Five of these LEDs are between the program function/edit key row and the top key row of the standard typewriter keys. A sixth LED is built into the shift LOCK key.

Referring to the diagram below, the four right-most LEDs along the top of the Keyboard display, in binary, the number of the test being run. (The burn-in mode is excepted from this description. See section 4.5.4.9.) The right-most LED is the LSB while the LED fourth from the right is the MSB in the binary numbering scheme. The test numbers are listed in section 4.5.3.

The table on the next frame outlines how the LEDs are used to convey the current status of the BIT program.



4.5 4230/05 POWER UP DIAGNOSTICS (Continued)4.5.5 KEYBOARD LED DISPLAYS (Continued)

<u>BIT PROGRAM STATUS</u>	<u>LED ACTIVITY</u>
Initial 2-second delay after turn-on (waiting for CANCEL to be pressed):	LSB LED lit
Next 2-second delay after CANCEL is pressed (as above):	Left-most LED lit
During testing in any mode:	LEDs display test number in binary, lsb & msb per diagram above, see section 4.5.3 for test numbers
Error detected in any test:	LEDs display failed test number as above, LOCK LED blinks at approx. 1-2/second rate
All tests completed without error:	LEDs extinguished

4.5.6 CRT DISPLAY SCREEN STANDARDS4.5.6.1 ID Field

Before testing starts and immediately following any test that modifies the screen, the BIT will clear the screen and display the ID field. The ID field will be displayed on the top line of the screen and has the following format:

R5370 07 xx 08 xx

"R" indicates that this is the revision line, and that the digits following are the revision number of the BIT.

5370

is the 4-digit revision number of the BIT (4230 shown).

4.5.6 CRT DISPLAY SCREEN STANDARDS (Continued)

4.5.6.1 ID Field (Continued)

07 xx 08 xx

07 and 08 are the two DIP switches readable by software on the 8287 PCA and xx are the values read. "07 xx" is switch 1, "08 xx" is switch 2.

4.5.6.2 Error Messages for Errors Detected
During BIT

When an error is detected during a BIT test, the screen will be cleared, the ID field displayed and the error message displayed with the format shown below. Once a failure has been detected and an error message displayed, pressing SHIFT/HELP will return the workstation to the beginning of the normal power-up test sequence.

ERR xx BOARD bb cc dd ee hhll

"ERR" indicates an error has occurred and that the information on the rest of the line is error information.

xx BOARD

xx is the last two digits of the PC board number most likely to have caused the error. xx is "KE" if the keyboard is indicated as the failed item.

4.5.6 CRT DISPLAY SCREEN STANDARDS (Continued)

4.5.6.2 Error Messages for Errors Detected
During BIT (Continued)

bb cc dd ee hhl1

the contents of the Z80 B, C, D, E and HL registers, respectively. 'ee' represents error code where the first digit of the code is the test number failed (also shown on the Keyboard LEDs) and the second is the error number in the particular test.

4.5.6.3 Examples of CRT Displays

NOTE

CRT displays shown below are typical of the 4230 Workstation. 4205 displays are structured the same but will display the ID field information in accordance with the 4205 BIT revision, IN07 and IN08 values.

```
R 5370    07 4C    08 58
```

Typical ID field showing revision of the BIT PROM, switch setting 4C for IN07 and 58 for IN08.

```
R 5370    07 4C    08 58
```

```
ERR  KE BOARD 00 00 00 B3 0000
```

Typical BIT error message showing a failure of test B, the keyboard test, and indicating a failure of the Keyboard.

4.5.6 CRT DISPLAY SCREEN STANDARDS (Continued)

4.5.6.3 Examples of CRT Displays (Continued)

```
R 5370    07 4C    08 58 .  
0001  
ERR  98 BOARD 00 00 00 D1 0000
```

Typical BIT error message showing a failure of test D, the external loopback test, and indicating a failure of the 8298 board. The pass counter shows the failure occurred the first time through the test.

4.5.6.4 Memory Parity Errors Detected On-Line

The workstation also checks memory parity during on-line operation. If a memory parity error is detected, control is passed to the BIT which preserves (freezes) the contents of the screen. This is immediately evidenced by the cursor which stops flashing. Additionally, the LOCK LED on the Keyboard blinks at approximately a 1 - 2 per second rate.

4.5 4230/05 POWER UP DIAGNOSTICS (Continued)

4.5.7 DIAGNOSTIC LED

The diagnostic LED gives a visual indication of the status of the BIT, whether in progress, passed or failed. The LED can be viewed through the ventilation slots in the Electronics Base bottom, on the left side toward the front of the unit. The code is as follows:

LED Blinking = BIT is in progress

LED Off = BIT was passed

LED On = BIT was failed

CHAPTER

5

**MAINT-
ENANCE**

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CHAPTER 5

PREVENTIVE AND CORRECTIVE MAINTENANCE

This chapter contains routine maintenance procedures required to align and adjust the 4230/05 Workstation for best performance (section 5.3). Removal and reinstallation procedures are also included (sections 5.4, 5.5 and 5.6). Section 5.7 details the switch settings for the 210-8287 PCA, 210-8298 PCA and the Keyboard. Please note that throughout this section, reference to the 8287 PCA also includes the -1 version of the PCA used in the 4205 Workstation and the -3 version used in the Arabic workstation.

5.1 REQUIRED TOOLS, TEST EQUIPMENT AND ACCESSORIES

The following items are required to carry out the preventive and corrective maintenance activities described in this chapter or elsewhere in this manual.

<u>DESCRIPTION</u>	<u>PART NUMBER</u>
Wang CE Tool Kit	726-9401
Digital Multimeter	N/A
RS-232C Loopback Connector	420-1040

5.2 PREVENTIVE MAINTENANCE

Preventive Maintenance should be performed on a regular basis to help prevent workstation equipment failures. The suggested plan for regular preventive maintenance follows.

5.2 PREVENTIVE MAINTENANCE (Continued)

5.2.1 SEMI-ANNUALLY (QUARTERLY IN AN INDUSTRIAL ENVIRONMENT) OR DURING AN UNSCHEDULED TROUBLE CALL

5.2.1.1 Cleaning

Remove power from the workstation and clean as follows:

1. Dust keyboard with a soft-bristled brush.
2. Clean the CRT screen, using a good quality glass cleaner and a soft, lint-free cloth.
3. Wipe exterior of workstation components, using a damp, lint-free cloth.
4. Vacuum dust from the ventilating slots in the Monitor cover and the Electronics Base cover, and from around the fan at the rear of the Electronics Base.

5.2.1.2 Checks and Adjustments

Apply power to the workstation and proceed as follows:

1. Check the workstation power supply voltages, as described in section 5.3.1.
2. Check for proper character display. Perform the Monitor Alignment Procedure (section 5.3.2), if required.

5.2.1 SEMI-ANNUALLY (QUARTERLY IN AN INDUSTRIAL ENVIRONMENT) OR DURING AN UNSCHEDULED TROUBLE CALL (Continued)

5.2.1.3 Diagnostics

The Built-In Test (BIT) diagnostics run automatically and a routine check of the workstation internal functions is accomplished each time the unit is powered up. No additional diagnostic tests are routinely required.

5.2.2 ANNUALLY (SEMI-ANNUALLY IN AN INDUSTRIAL ENVIRONMENT)

Check all cables and connectors for proper seating. Loose or damaged connectors should be repaired or replaced.

5.3 CORRECTIVE MAINTENANCE

This section contains adjustment and alignment procedures required in the units of the 4230/05 Workstation. The tools, test equipment and accessories required for these procedures are listed in section 5.1. To access the components as directed in the procedures, refer to the removal/reinstallation procedures in sections 5.4, 5.5 or 5.6. Adjustment/alignment procedures included in this section are listed below.

<u>SECTION</u>	<u>PROCEDURE</u>
5.3.1	Voltage Checks
5.3.2	Monitor Alignment

5.3.1 VOLTAGE CHECKS

The 4230/05 Workstation is powered by a single switching power supply in the Electronics Base unit which supplies +5 and ± 12 Vdc to the workstation components. A series-regulator device on the 8287 board derives a -5 Vdc supply from the -12 Vdc power supply output.

To check the internal power supplies, proceed as follows:

NOTE

There are no adjustments to be performed in the field in the switching Power Supply. If the voltage outputs are not within tolerance, replace the power supply.

5.3 CORRECTIVE MAINTENANCE (Continued)

5.3.1 VOLTAGE CHECKS (Continued)

Referring to Figure 5-1 and the table below, measure the following voltages on the 8287 PCA, grounding your meter to J5-6 on that board.

<u>DC VOLTAGE</u>	<u>MONITORING TEST POINT</u>	<u>ACCEPTABLE RANGE</u>
+5 Vdc	J5-3	+4.9 through +5.1 Vdc
+12 Vdc	J5-1	+11.8 through +12.2 Vdc
-12 Vdc	J5-8	-11.4 through -12.6 Vdc

Check the -5 Vdc supply at VR1-2 as shown in Figure 5-1. The allowable range of this supply is -4.9 through -5.1 Vdc.

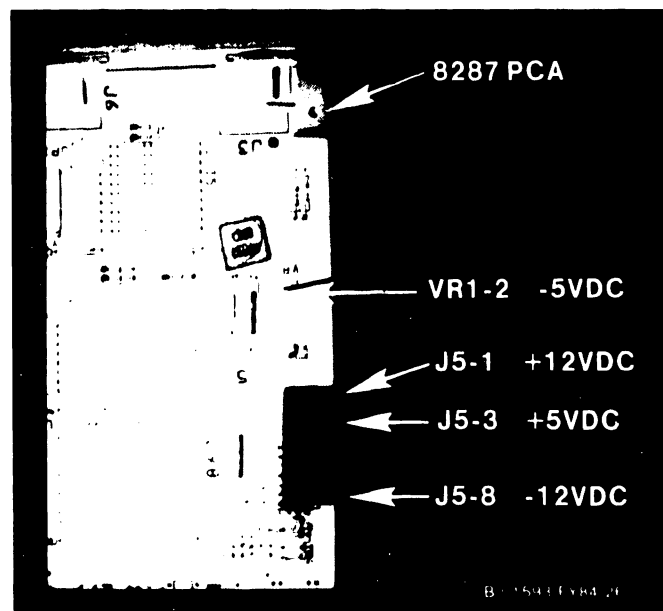


Figure 5-1. Power Supply Checks

5.3 CORRECTIVE MAINTENANCE (Continued)

5.3.2 MONITOR ALIGNMENT, DESCRIPTION OF SOFTWARE SUPPORT

The Monitor alignment can be carried out using either the Built-In Test (BIT) video pattern or with the on-line VS or OIS diagnostic test operating system (DTOS) series of test patterns. Monitor alignment with the BIT pattern allows for all adjustments except horizontal and vertical linearity. Alternatively, the DTOS, with its available grid and circle patterns, allows for the linearity to be set precisely and visually checked. Monitor alignment using BIT support is given in section 5.3.3 while section 5.3.4 details the Monitor alignment using DTOS support.

5.3.3 MONITOR ALIGNMENT USING BIT SUPPORT

The following alignment of the 4230/05 Monitor is carried out with the support of the video pattern in the Built-In Test. Please note that the procedure below does not cover the Monitor's linearity adjustments and that a complete alignment can be obtained with the support of the VS or OIS DTOS package, as detailed in section

5.3.3. MONITOR ALIGNMENT USING BIT SUPPORT

5.3.3.1 8244 PCA

Pre-Alignment Conditions:

- Remove cover from Monitor (section 5.5).
- Connect dual cable between Monitor and Electronics Base.

WARNING

High voltage is present in the vicinity of the Monitor PCA. Most adjustments will be made from the non-component side of the PCA through labeled access holes. Exercise extreme caution in making these adjustments to prevent coming in contact with dangerous voltages.

5.3.3. MONITOR ALIGNMENT/BIT SUPPORT (Cont'd)

5.3.3.1 8244 PCA (Continued)

1. Power on the unit, wait for the LED adjacent to the CANCEL key to light and immediately press CANCEL. Within two seconds after pressing CANCEL, press CENTER. Then, press any key except CANCEL to display the pattern shown below.
2. Allow approximately five minutes warm-up time for the Monitor to stabilize.
3. Adjust the Monitor Brightness control to adequately display the video alignment pattern. Do not adjust Brightness so high as to cause display of the raster or cause blooming.

5.3.3. MONITOR ALIGNMENT/BIT SUPPORT (Cont'd)

5.3.3.1 8244 PCA (Continued)

4. Adjust vertical hold control R45 to the center of its stable range.
5. Adjust horizontal hold control R26 to the center of its stable range.
6. Adjust focus control R6 for the sharpest overall display pattern.

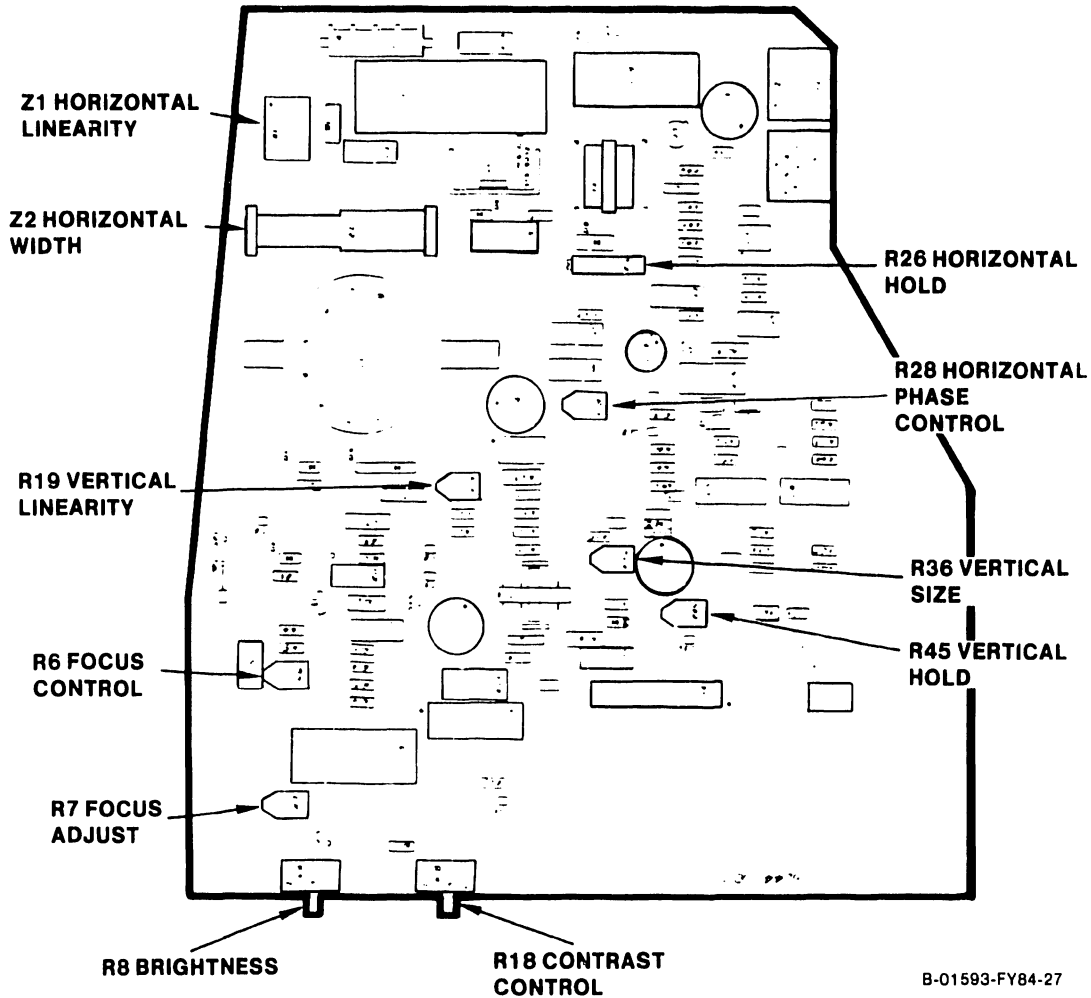
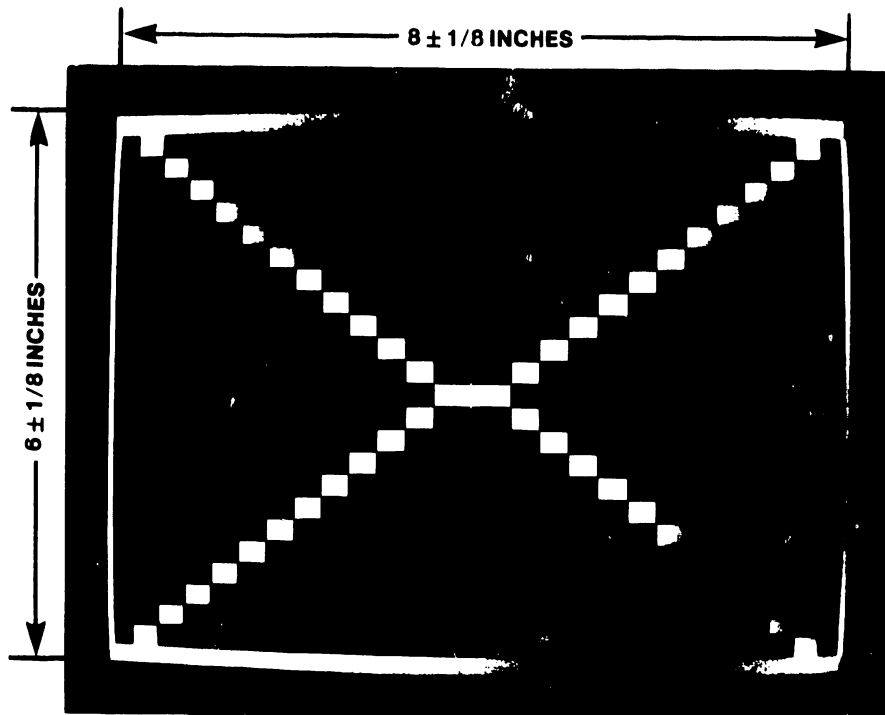


Figure 5-2. 8244 PCA Video Alignment
Test Points and Adjustments

5.3.3. MONITOR ALIGNMENT/BIT SUPPORT (Cont'd)

5.3.3.1 8244 PCA (Continued)

7. Adjust vertical size control R36 so that the display pattern is $6 \pm 1/8$ inches ($15.2 \text{ cm} \pm 3 \text{ mm}$) high. See Figure 5-4. Use a standard or metric scale.



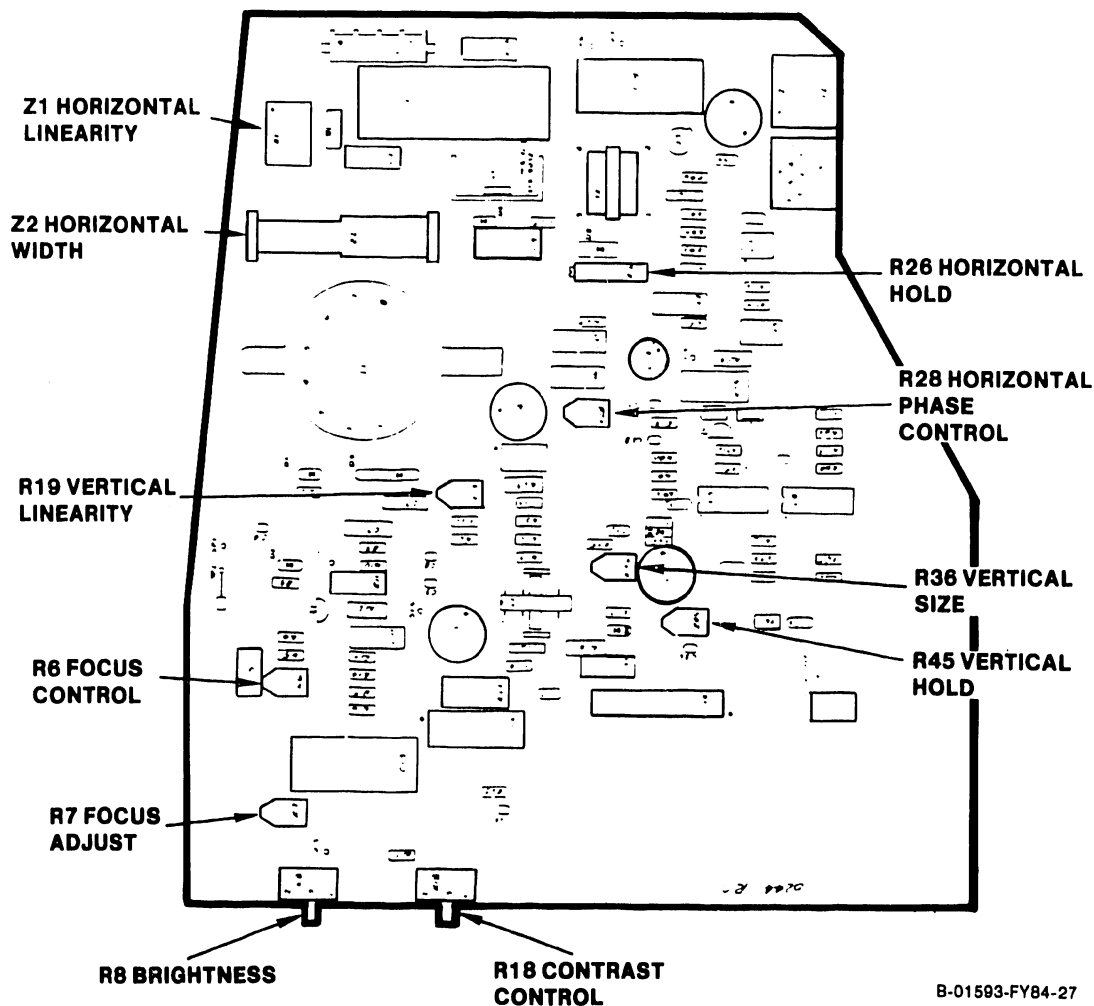
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Figure 5-4. Video Display Pattern of Built-In Test

5.3.3. MONITOR ALIGNMENT/BIT SUPPORT (Cont'd)

5.3.3.1 8244 PCA (Continued)

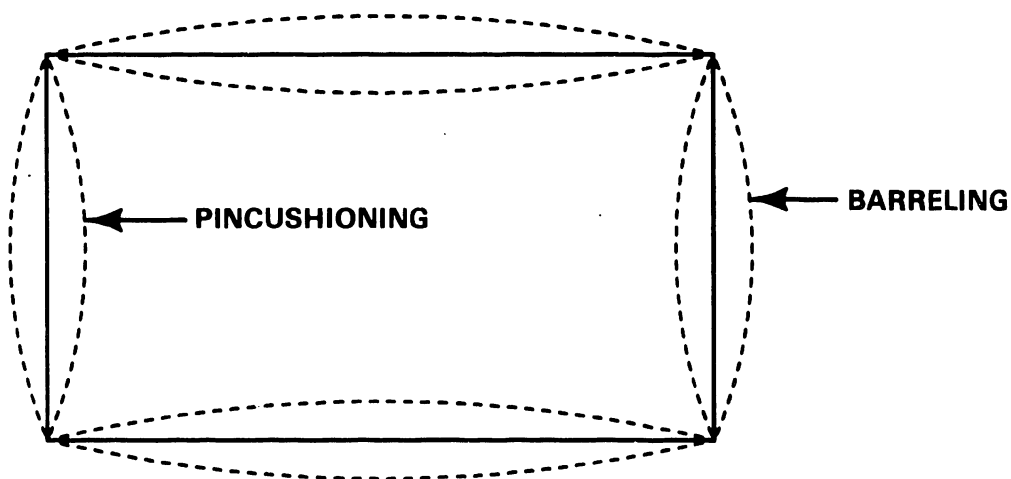
8. Adjust horizontal width coil Z2 so that the display pattern is $8 \pm 1/8$ inches ($20.3 \text{ cm} \pm 3 \text{ mm}$) wide. Use a standard or metric scale.
9. Adjust the Brightness control to display the raster, but not so high as to cause blooming. Adjust horizontal phase control R28 to center the display pattern in the raster.
10. Adjust the two tabs on the rear cover of the deflection yoke around the CRT neck one at a time to center the raster on the face of the CRT.



5.3.3. MONITOR ALIGNMENT/BIT SUPPORT (Cont'd)

5.3.3.1 8244 PCA (Continued)

11. Using a non-metallic straight-edge (plastic ruler, envelope, etc.) for comparison, check each perimeter line of the video display pattern for pincushioning or barreling distortion (Figure 5-5a). The lines should be straight to within $\pm 1/16$ inch (1.5 mm).



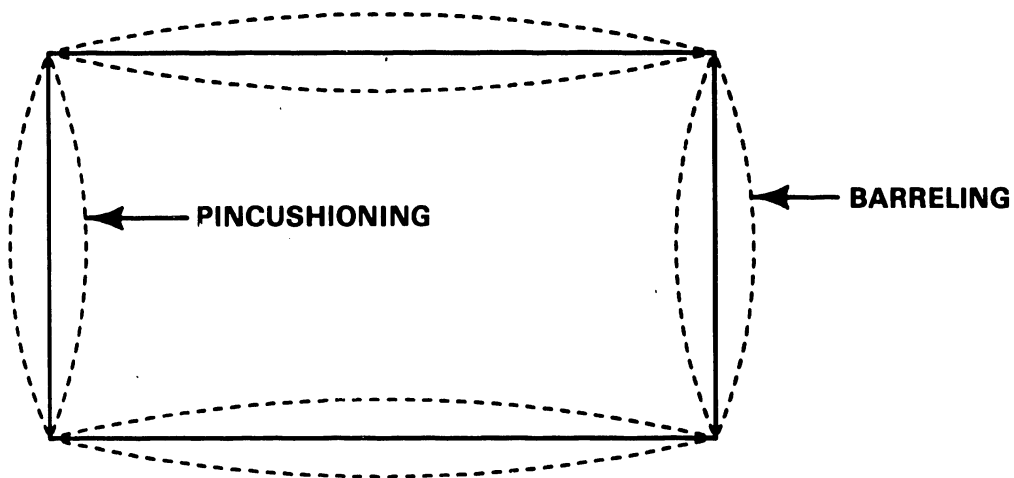
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Figure 5-5a. Pincushioning and Barreling,
Distortion

5.3.3. MONITOR ALIGNMENT/BIT SUPPORT (Cont'd)

5.3.3.1 8244 PCA (Continued)

12. If either type of distortion exceeds $\pm 1/16$ inch (1.5 mm), adjustment of the magnets mounted on the posts around the perimeter of the deflection yoke is required (Figure 5-5b). Rotate the magnet closest to the area of greatest distortion to make the correction.



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Figure 5-5b. Pincushioning and Barreling,
Correction

5.3.3. MONITOR ALIGNMENT/BIT SUPPORT (Cont'd)

5.3.3.1 8244 PCA (Continued)

13. If correction is not possible with the magnets mounted around the yoke, magnets can be added as required to correct the distortion. This generally involves replacing an existing magnet with one of a higher gauss value. The magnets, their color-coding and part numbers are listed below.

<u>COLOR CODE</u>	<u>VALUE</u>	<u>PART NUMBER</u>
Green	Gauss 11	320-0126
Blue	Gauss 15	320-0128
White	Gauss 20	320-0127

If the above procedure does not bring the Monitor into tolerance, replacement is recommended. If the Monitor can be aligned satisfactorily, power off the workstation and reassemble the Monitor.

5.3.3. MONITOR ALIGNMENT USING BIT SUPPORT

5.3.3.2 8344 PCA

Pre-Alignment Conditions:

- Remove cover from Monitor (section 5.5).
- Connect dual cable between Monitor and Electronics Base.

WARNING

High voltage is present in the vicinity of the Monitor PCA. Most adjustments will be made from the non-component side of the PCA through labeled access holes. Exercise extreme caution in making these adjustments to prevent coming in contact with dangerous voltages.

5.3.3. MONITOR ALIGNMENT/BIT SUPPORT (Cont'd)

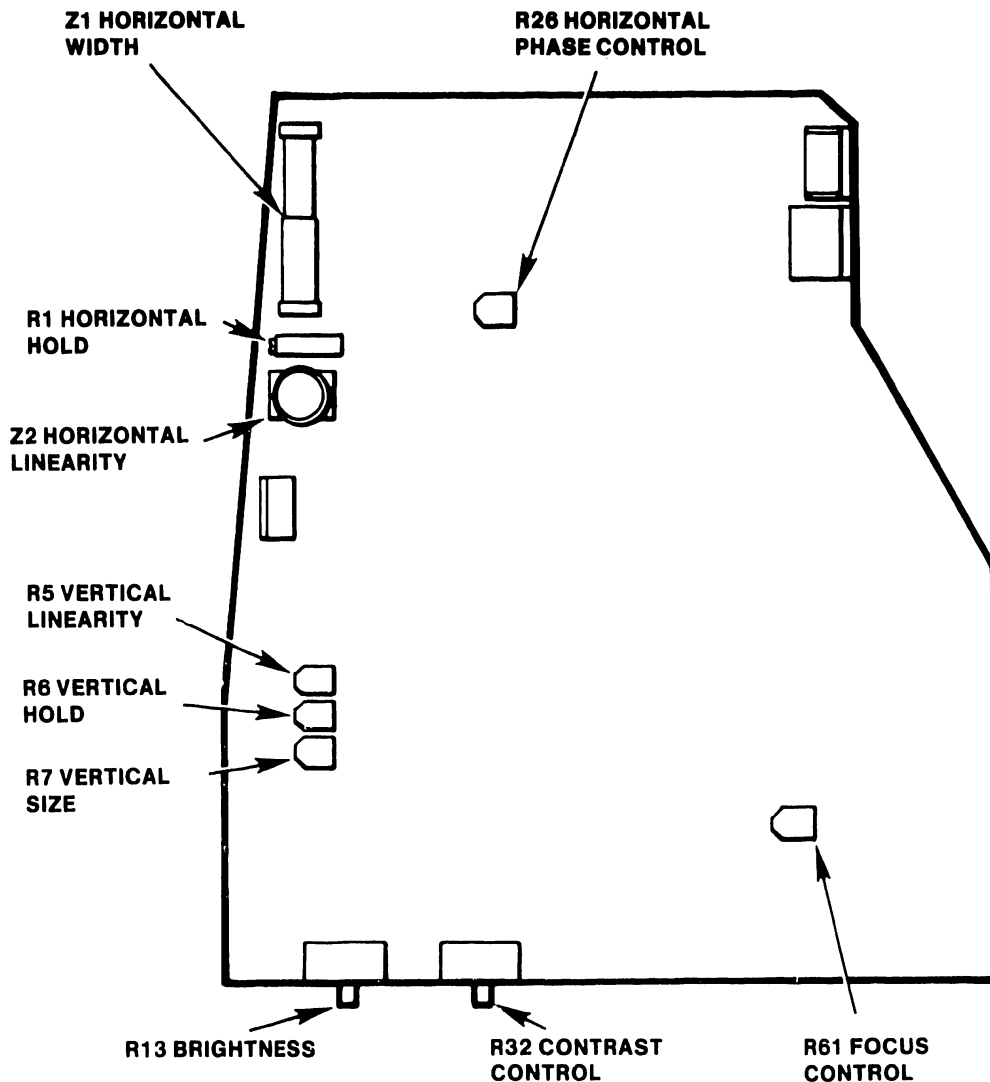
5.3.3.2 8344 PCA (Continued)

1. Power on the unit, wait for the LED adjacent to the CANCEL key to light and immediately press CANCEL. Within two seconds after pressing CANCEL, press CENTER. Then, press any key except CANCEL to display the pattern shown below.
2. Allow approximately five minutes warm-up time for the Monitor to stabilize.
3. Adjust the Monitor Brightness control to adequately display the video alignment pattern. Do not adjust Brightness so high as to cause display of the raster or cause blooming.

5.3.3. MONITOR ALIGNMENT/BIT SUPPORT (Cont'd)

5.3.3.2 8344 PCA (Continued)(Figure 5-3)

4. Adjust vertical hold control R6 to the center of its stable range.
5. Adjust horizontal hold control R1 to the center of its stable range.
6. Adjust focus control R6 for the sharpest overall display pattern.



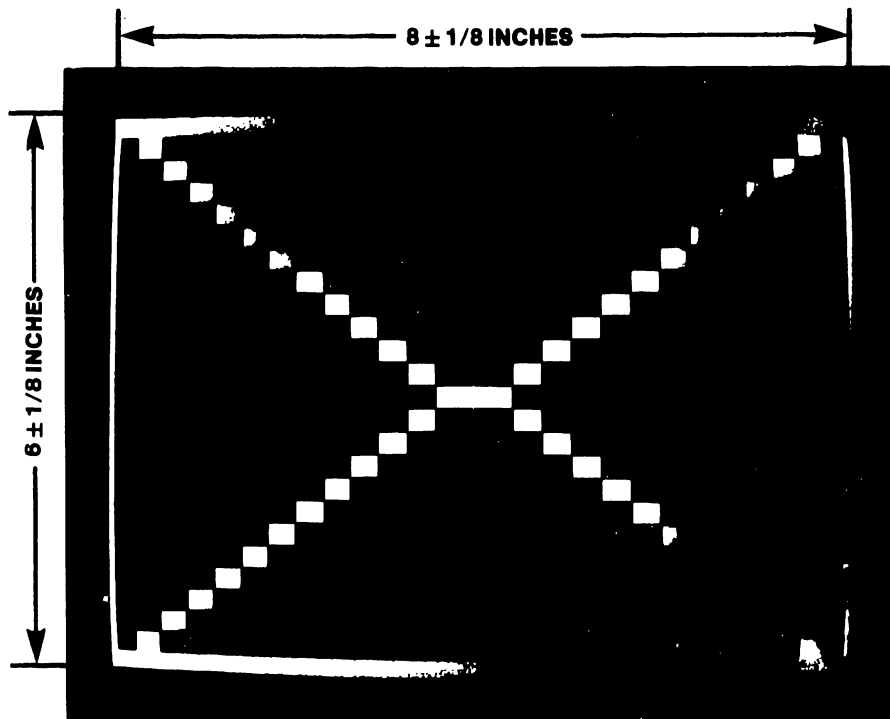
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Figure 5-3. 8344 PCA Video Alignment
Test Points and Adjustments

5.3.3. MONITOR ALIGNMENT/BIT SUPPORT (Cont'd)

5.3.3.2 8344 PCA (Continued)

7. Adjust vertical size control R7 so that the display pattern is $6 \pm 1/8$ inches ($15.2 \text{ cm} \pm 3 \text{ mm}$) high. Use a standard or metric scale.

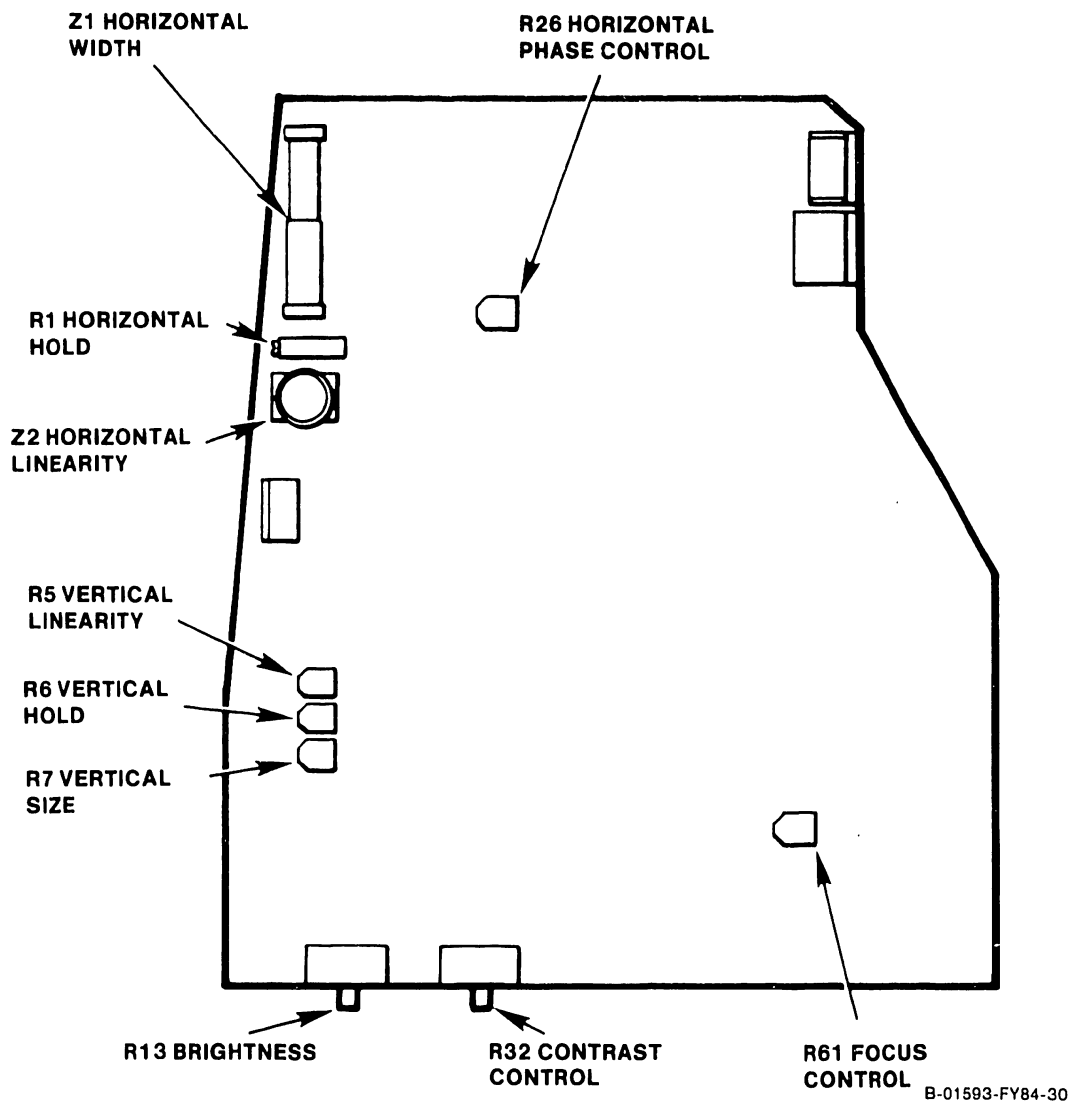


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5.3.3. MONITOR ALIGNMENT/BIT SUPPORT (Cont'd)

5.3.3.2 8344 PCA (Continued)

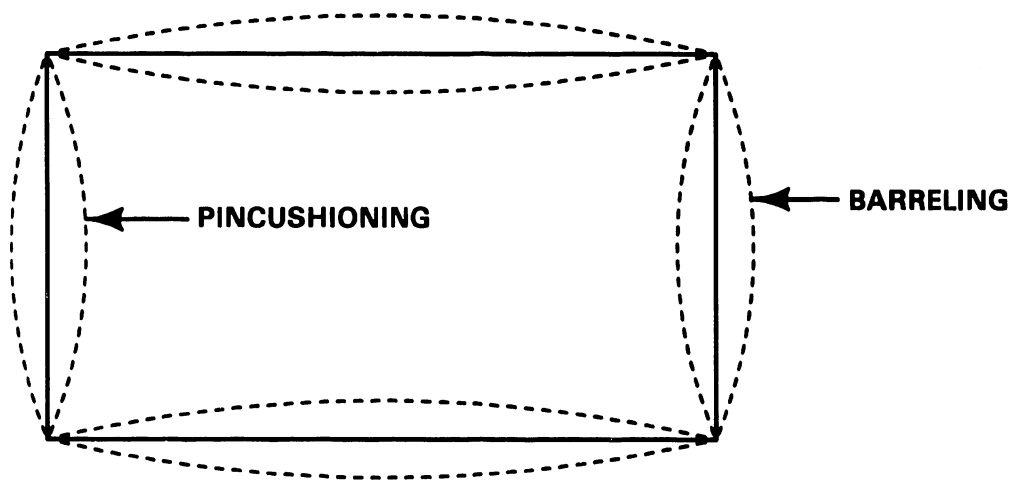
8. Adjust horizontal width coil Z1 so that the display pattern is $8 \pm 1/8$ inches ($20.3 \text{ cm} \pm 3 \text{ mm}$) wide. Use a standard or metric scale.
9. Adjust the Brightness control to display the raster, but not so high as to cause blooming. Adjust horizontal phase control R26 to center the display pattern in the raster.
10. Adjust the two tabs on the rear cover of the deflection yoke around the CRT neck one at a time to center the raster on the face of the CRT.



5.3.3. MONITOR ALIGNMENT/BIT SUPPORT (Cont'd)

5.3.3.2 8344 PCA (Continued)

11. Using a non-metallic straight-edge (plastic ruler, envelope, etc.) for comparison, check each perimeter line of the video display pattern for pincushioning or barreling distortion. The lines should be straight to within $\pm 1/16$ inch (1.5 mm).

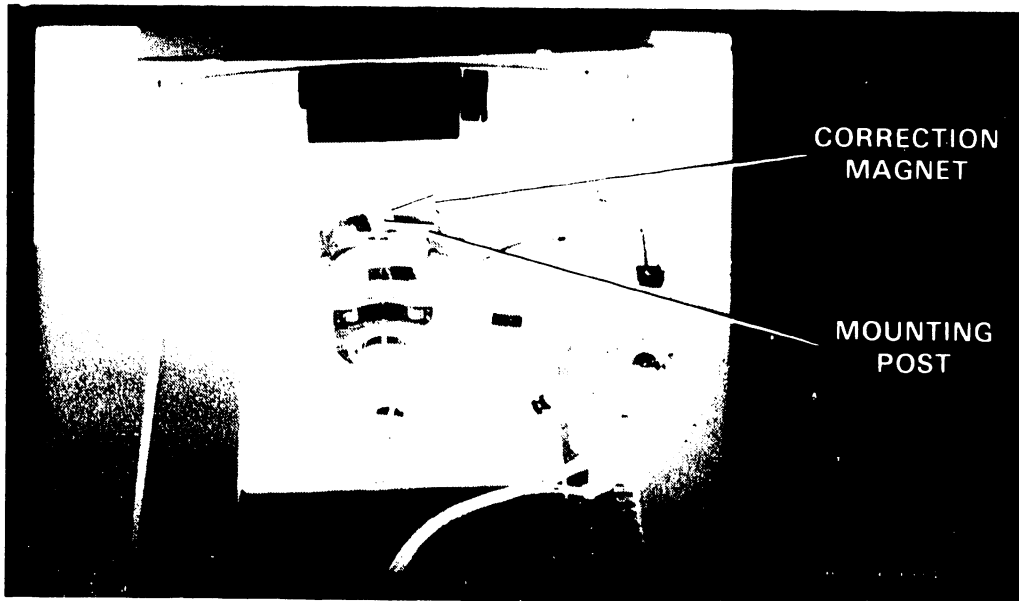


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5.3.3. MONITOR ALIGNMENT/BIT SUPPORT (Cont'd)

5.3.3.2 8344 PCA (Continued)

12. If either type of distortion exceeds $\pm 1/16$ inch (1.5 mm), adjustment of the magnets mounted on the posts around the perimeter of the deflection yoke is required. Rotate the magnet closest to the area of greatest distortion to make the correction.



5.3.3. MONITOR ALIGNMENT/BIT SUPPORT (Cont'd)

5.3.3.2 8344 PCA (Continued)

13. If correction is not possible with the magnets mounted around the yoke, magnets can be added as required to correct the distortion. This generally involves replacing an existing magnet with one of a higher gauss value. The magnets, their color-coding and part numbers are listed below.

<u>COLOR CODE</u>	<u>VALUE</u>	<u>PART NUMBER</u>
Green	Gauss 11	320-0126
Blue	Gauss 15	320-0128
White	Gauss 20	320-0127

If the above procedure does not bring the Monitor into tolerance, replacement is recommended. If the Monitor can be aligned satisfactorily, power off the workstation and reassemble the Monitor.

5.3.4 MONITOR ALIGNMENT USING DTOS SUPPORT

5.3.4.1 8244 PCA

The following alignment of the 4230/05 Monitor is carried out with the support of the video patterns in the VS or OIS DTOS package.

Pre-Alignment Conditions:

- Remove cover from Monitor (section 5.5).
- Connect dual cable between Monitor and Electronics Base.
- Set workstation I/O switch to 1 (on). Allow approximately five minutes warm-up time for the Monitor to stabilize.

WARNING

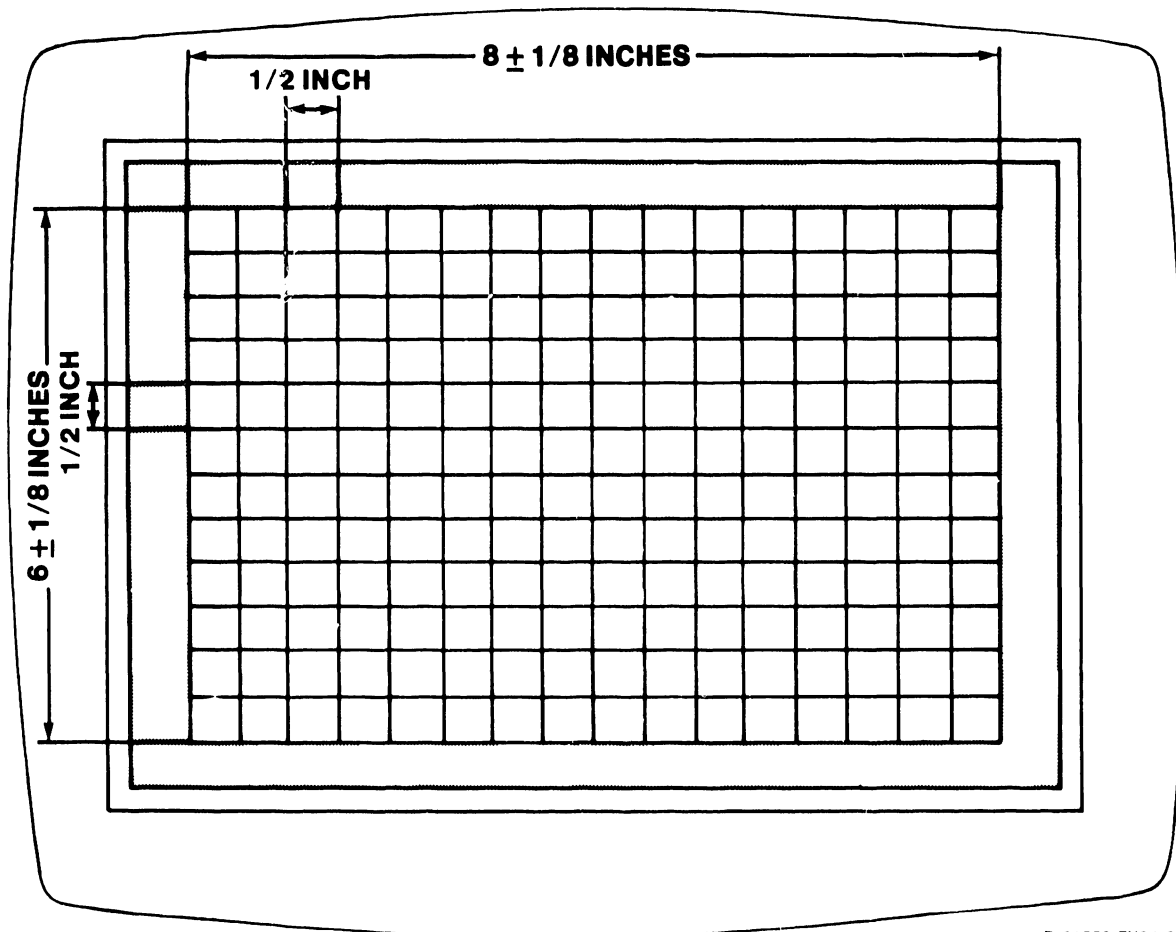
High voltage is present in the vicinity of the Monitor PCA. Most adjustments will be made from the noncomponent side of the PCA through labeled access holes. Exercise extreme caution in making these adjustments to prevent coming in contact with dangerous voltages.

1. Select the Monitor alignment routine resident in the DTOS package. This routine contains four different patterns for use in aligning the Monitor. Only two patterns, the grid pattern and the circle pattern, will be used in the following procedure.

5.3.4 MONITOR ALIGNMENT/DTOS SUPPORT (Continued)

5.3.4.1 8244 PCA

2. Select the grid alignment pattern (Figure 5-6) for display on the workstation Monitor.



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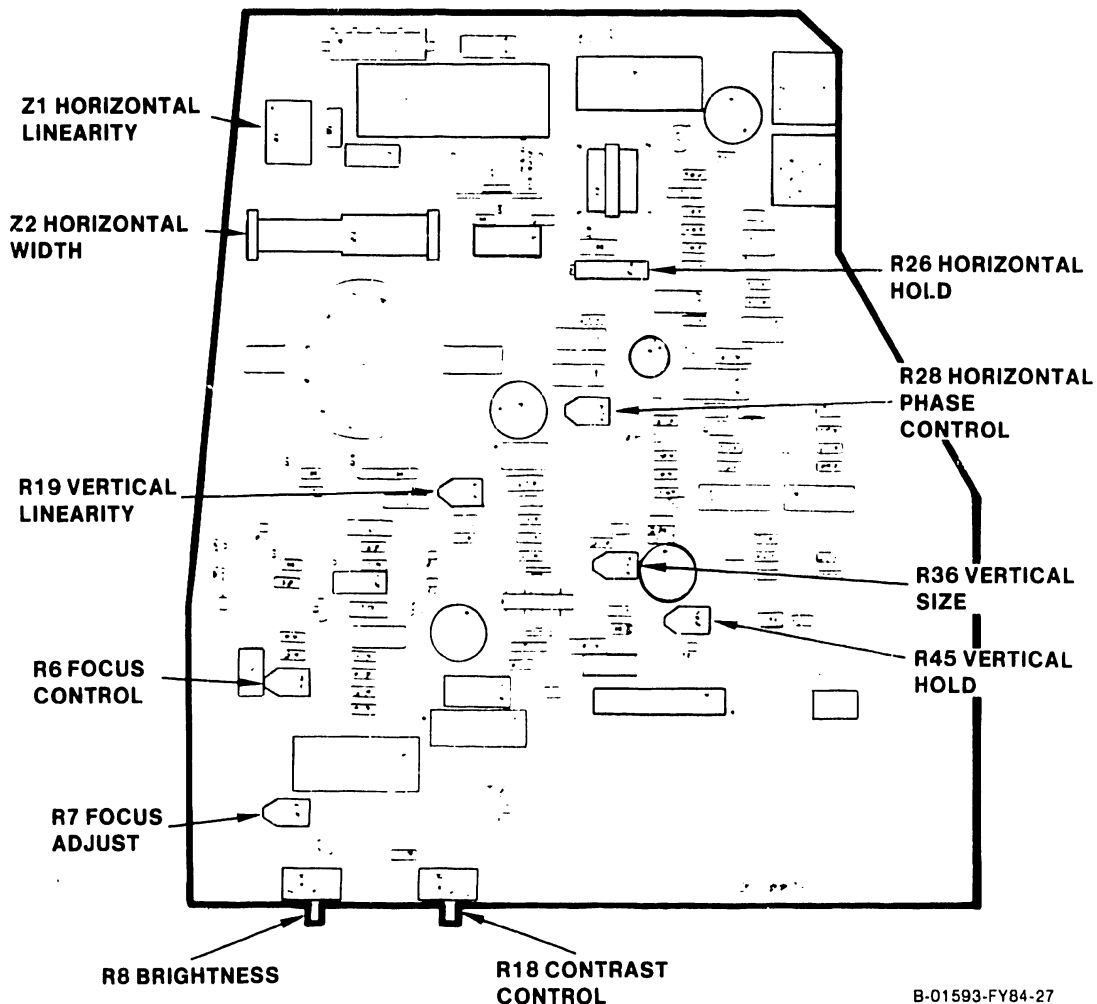
Figure 5-6. VS and OIS DTOS Grid Display Pattern

3. Adjust the Monitor brightness control to adequately display the grid alignment pattern. Do not adjust brightness so high as to cause display of the raster or cause blooming.

5.3.4 MONITOR ALIGNMENT/DTOS SUPPORT (Continued)

5.3.4.1 8244 PCA

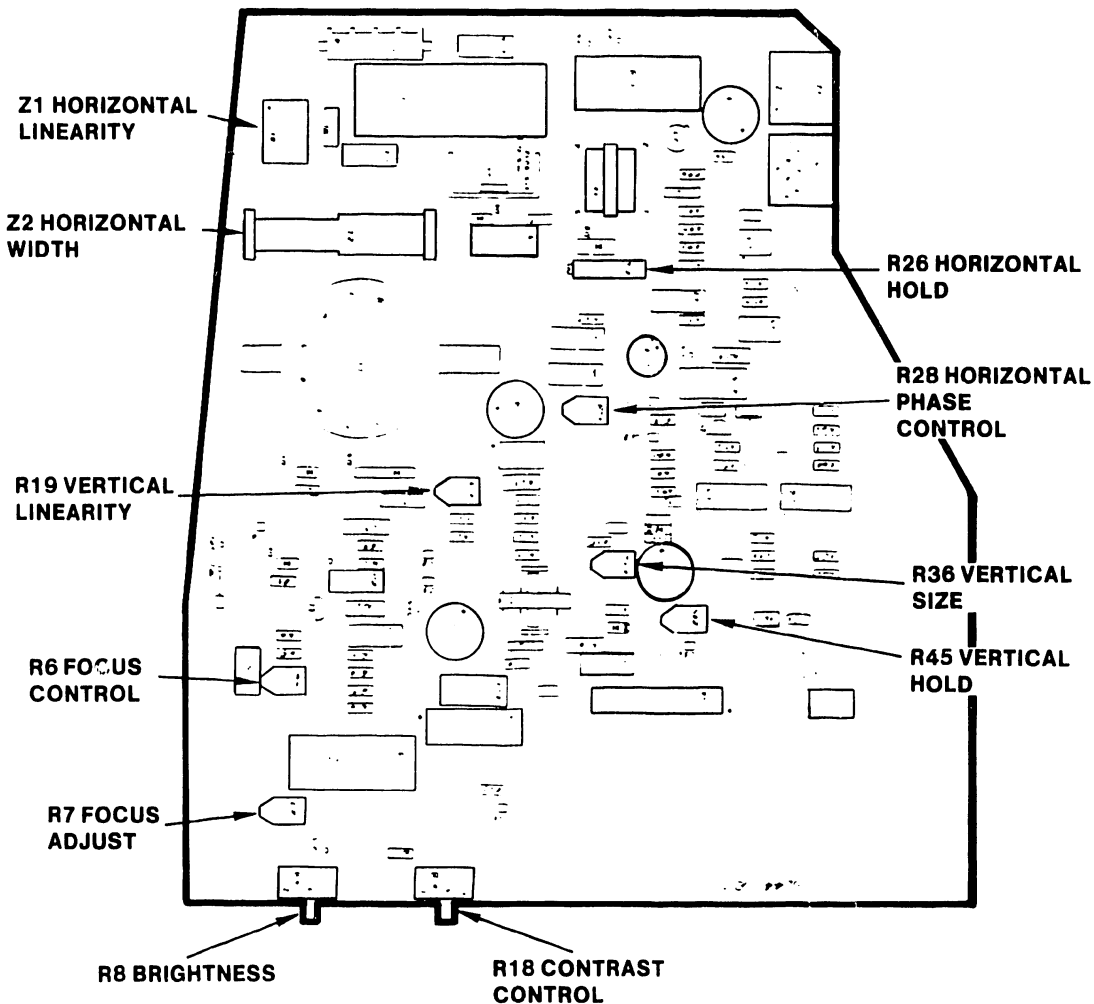
4. Adjust vertical hold control R45 to the center of its stable range.
5. Adjust horizontal hold control R26 to the center of its stable range.
6. Adjust focus control R6 for the sharpest overall display pattern.
7. Adjust vertical size control R36 so that the display pattern is $6 \pm 1/8$ inches ($15.2 \text{ cm} \pm 3 \text{ mm}$) high. Use a standard or metric scale.



5.3.4 MONITOR ALIGNMENT/DIOS SUPPORT (Continued)

5.3.4.1 8244 PCA

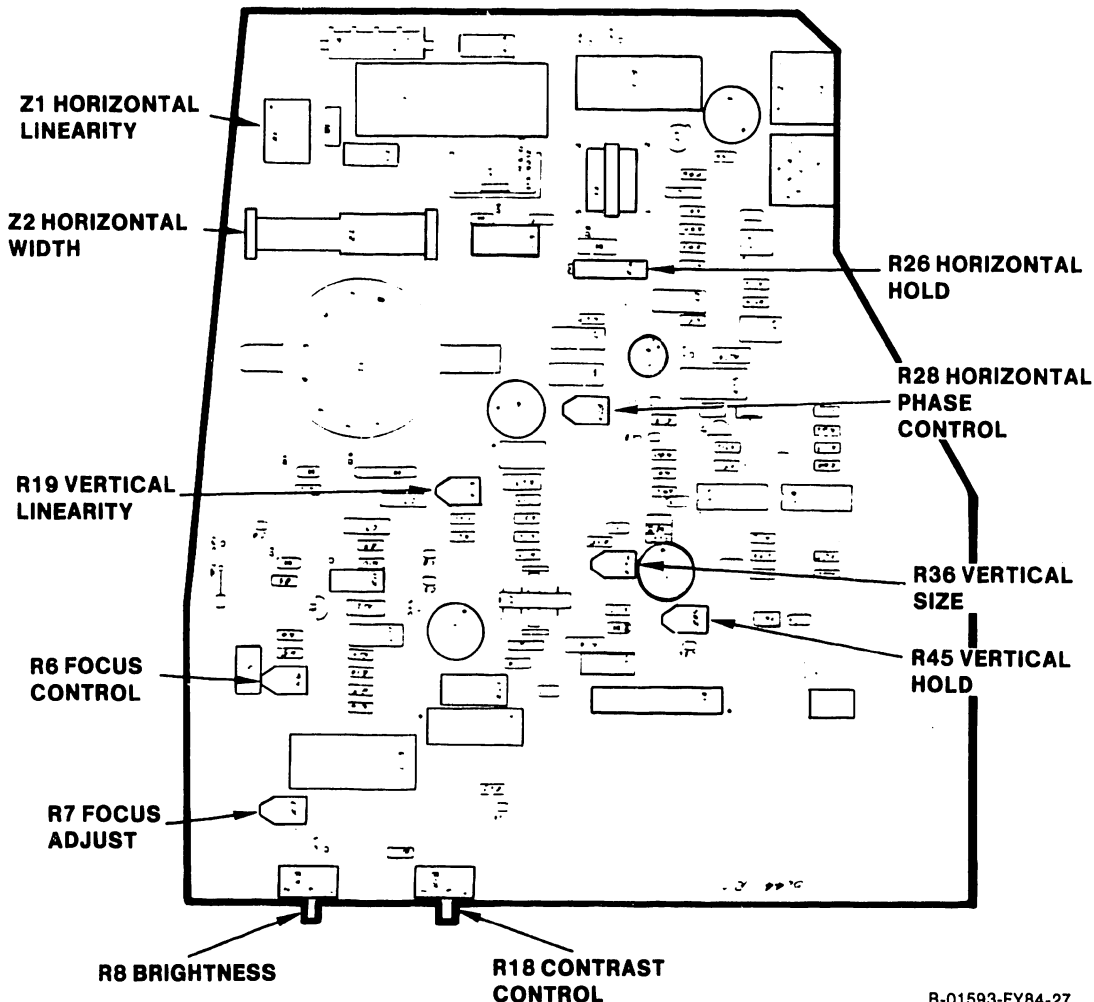
8. Adjust vertical linearity control R19 so that the squares at the top of the display are the same vertical size as the squares at the bottom of the display. This adjustment may affect the vertical height adjustment. Repeat step 7 if required.
9. Adjust horizontal width coil Z2 so that the display pattern is $8 \pm 1/8$ inches ($20.3 \text{ cm} \pm 3 \text{ mm}$) wide. Use a standard or metric scale.



5.3.4 MONITOR ALIGNMENT/DTOS SUPPORT (Continued)

5.3.4.1 8244 PCA

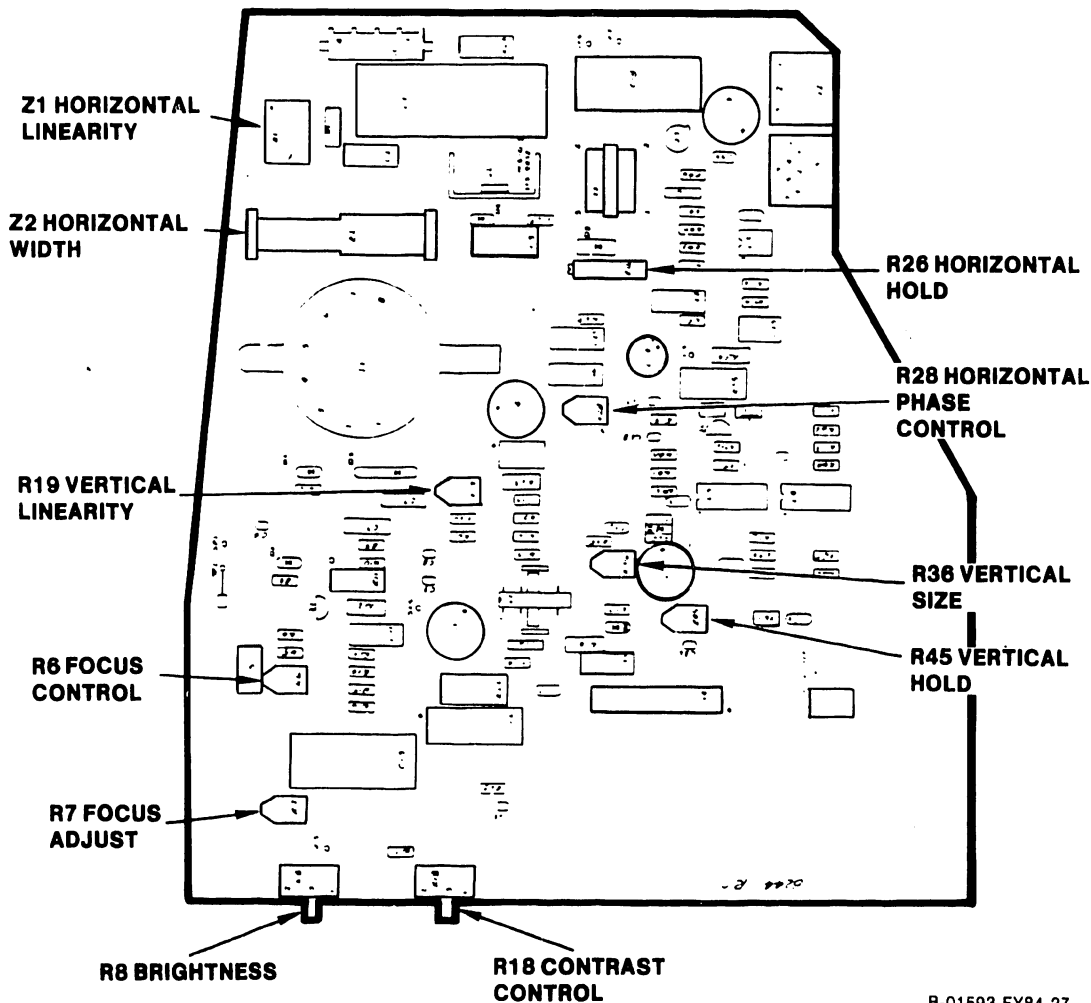
10. Adjust horizontal linearity coil Z1 so that the squares at the left of the display are the same horizontal size as the squares at the right of the display. This adjustment may affect the horizontal width adjustment. Repeat step 9 if required.
11. Select the circle alignment pattern in the Monitor alignment routine in the VS DTOS package. A visual check of the circles displayed should reveal no noticeable distortion, i.e., no egg-shaped or oblong forms. Repeat steps 7 through 11 if necessary.



5.3.4 MONITOR ALIGNMENT/DIOS SUPPORT (Continued)

5.3.4.1 8244 PCA

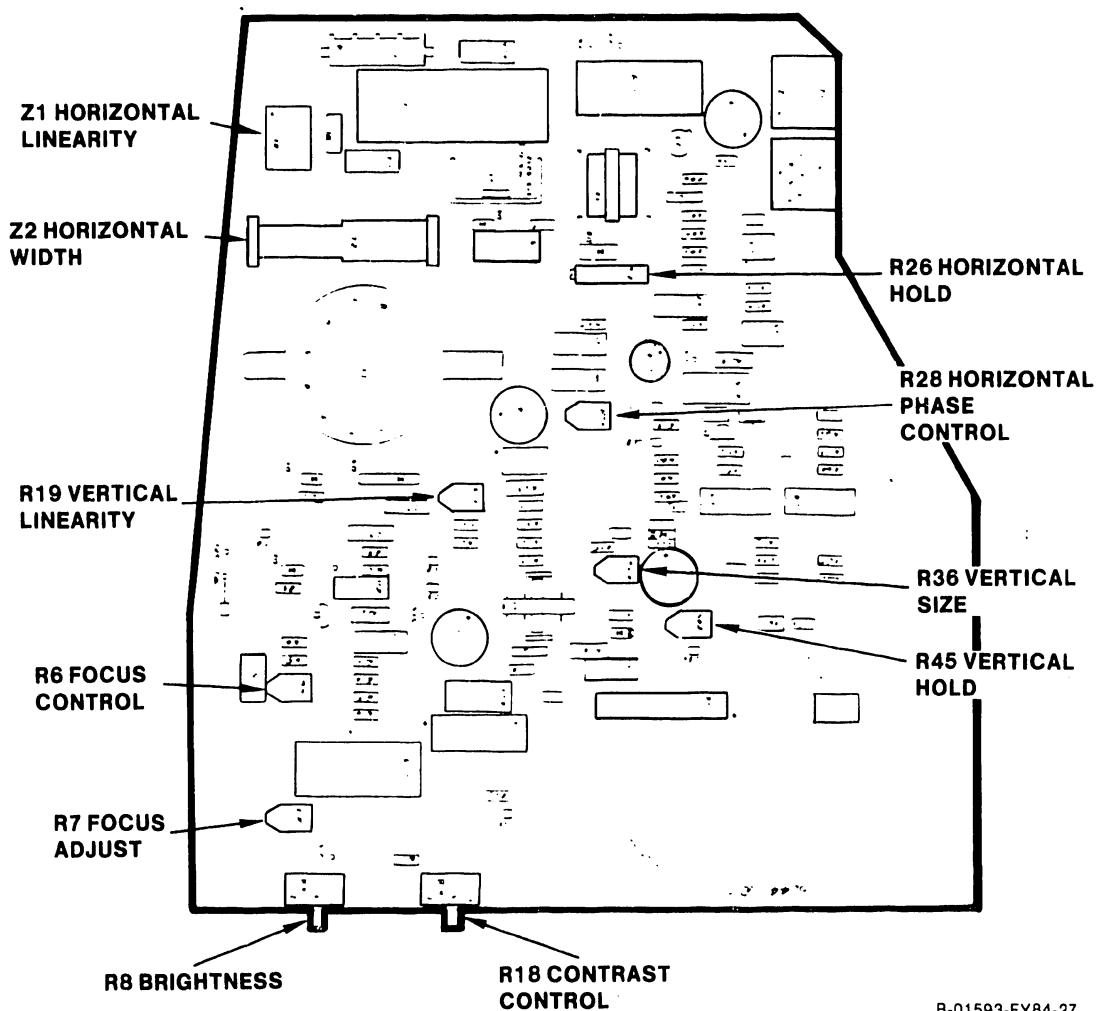
12. With the circle alignment pattern still selected, adjust the Brightness control to display the raster, but not so high as to cause blooming. Adjust horizontal phase control R28 completely counterclockwise.
13. Adjust horizontal hold control R26 clockwise so that the video pattern overlaps at the left edge of the display, and touches the left edge of the two left-most circles.



5.3.4 MONITOR ALIGNMENT/DTOS SUPPORT (Continued)

5.3.4.1 8244 PCA

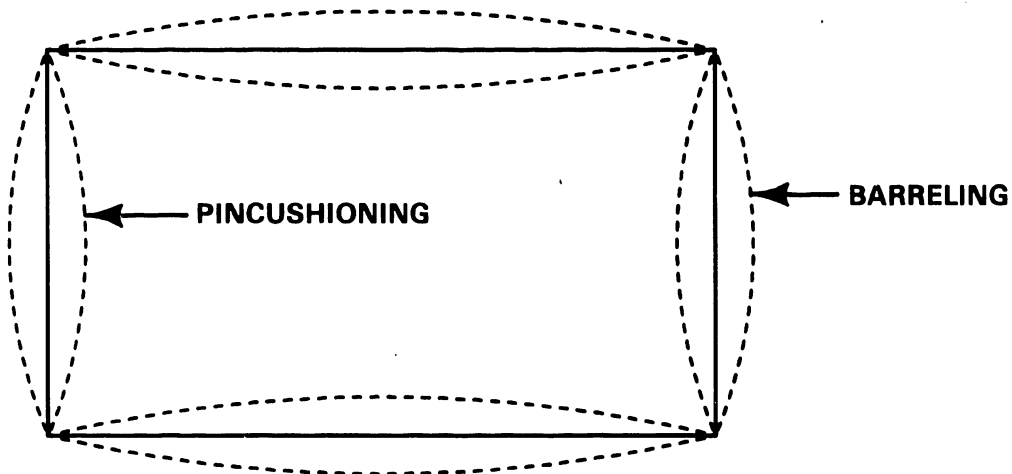
14. Adjust horizontal phase control R28 to center the display pattern in the raster. Return to the grid pattern and proceed with the next step.
15. Adjust the two tabs on the rear cover of the deflection yoke around the CRT neck one at a time to center the raster on the face of the CRT.



5.3.4 MONITOR ALIGNMENT/DTOS SUPPORT (Continued)

5.3.4.1 8244 PCA

16. Using a non-metallic straight-edge (plastic ruler, envelope, etc.) for comparison, check each perimeter line of the video display pattern for pincushioning or barreling distortion. The lines should be straight to within $\pm 1/16$ inch (1.5 mm).

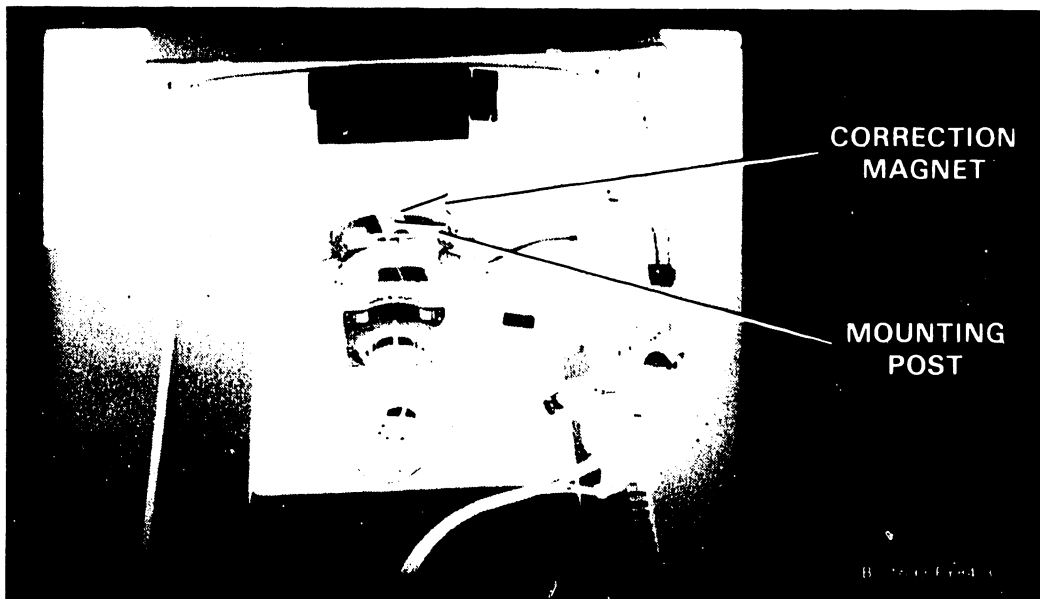


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5.3.4 MONITOR ALIGNMENT/DTOS SUPPORT (Continued)

5.3.4.1 8244 PCA

17. If either type of distortion exceeds $\pm 1/16$ inch (1.5 mm), adjustment of the magnets mounted on the posts around the perimeter of the deflection yoke is required. Rotate the magnet closest to the area of greatest distortion to make the correction.



5.3.4 MONITOR ALIGNMENT/DTOS SUPPORT (Continued)

5.3.4.1 8244 PCA

18. If correction is not possible with the magnets mounted around the yoke, magnets can be added as required to correct the distortion. This generally involves replacing an existing magnet with one of a higher gauss value. The magnets, their color-coding and part numbers are listed below.

<u>COLOR CODE</u>	<u>VALUE</u>	<u>PART NUMBER</u>
Green	Gauss 11	320-0126
Blue	Gauss 15	320-0128
White	Gauss 20	320-0127

If the above procedure does not bring the Monitor into tolerance, replacement is recommended. If the Monitor can be aligned satisfactorily, power off the workstation and reassemble the Monitor.

5.3.4 MONITOR ALIGNMENT USING DTOS SUPPORT

5.3.4.2 8344 PCA

The following alignment of the 4230/05 Monitor is carried out with the support of the video patterns in the VS or OIS DTOS package.

Pre-Alignment Conditions:

- Remove cover from Monitor (section 5.5).
- Connect dual cable between Monitor and Electronics Base.
- Set workstation I/O switch to 1 (on). Allow approximately five minutes warm-up time for the Monitor to stabilize.

WARNING

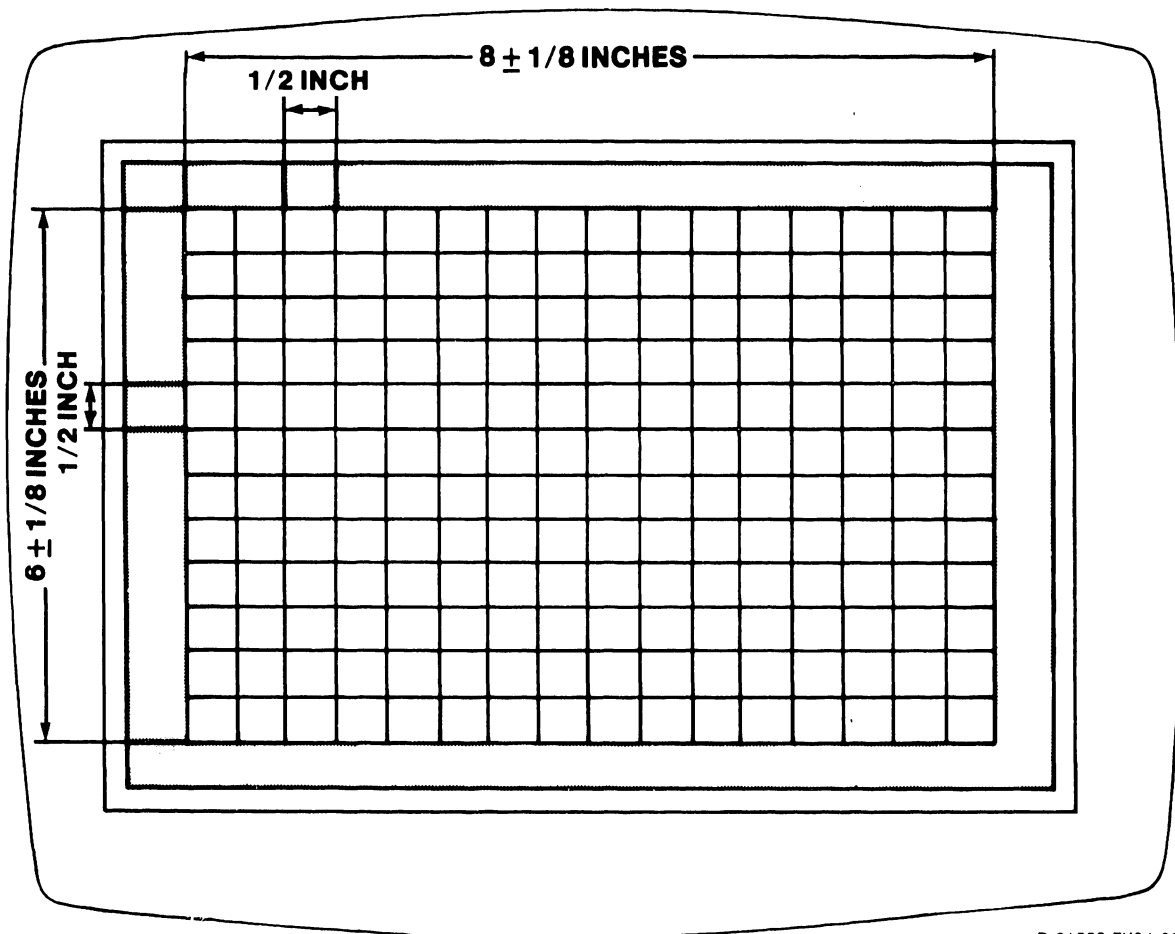
High voltage is present in the vicinity of the Monitor PCA. Most adjustments will be made from the noncomponent side of the PCA through labeled access holes. Exercise extreme caution in making these adjustments to prevent coming in contact with dangerous voltages.

1. Select the Monitor alignment routine resident in the DTOS package. This routine contains four different patterns for use in aligning the Monitor. Only two patterns, the grid pattern and the circle pattern, will be used in the following procedure.

5.3.4 MONITOR ALIGNMENT/DTOS SUPPORT (Continued)

5.3.4.2 8344 PCA

2. Select the grid alignment pattern for display on the workstation Monitor.



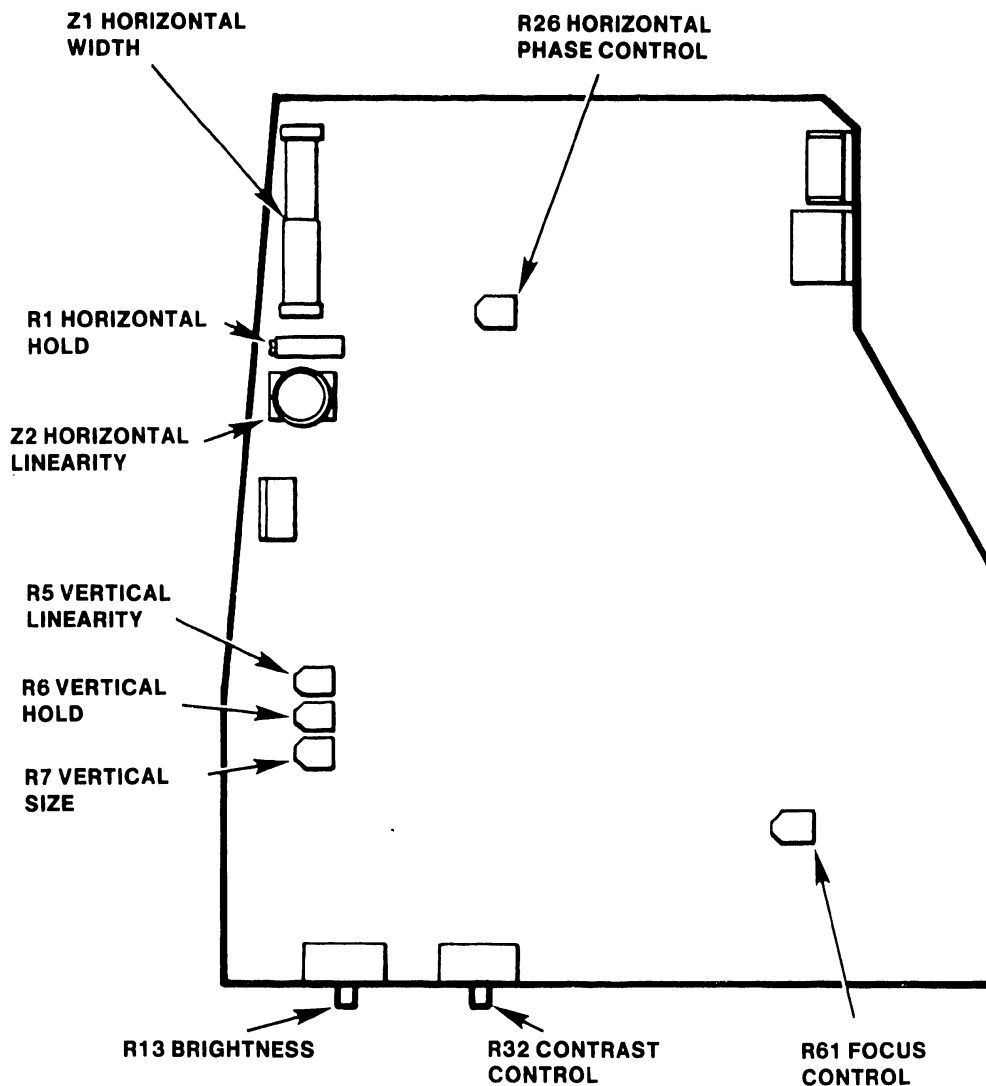
B-01556-FY84-62

3. Adjust the Monitor brightness control to adequately display the grid alignment pattern. Do not adjust brightness so high as to cause display of the raster or cause blooming.

5.3.4 MONITOR ALIGNMENT/DTOS SUPPORT (Continued)

5.3.4.2 8344 PCA

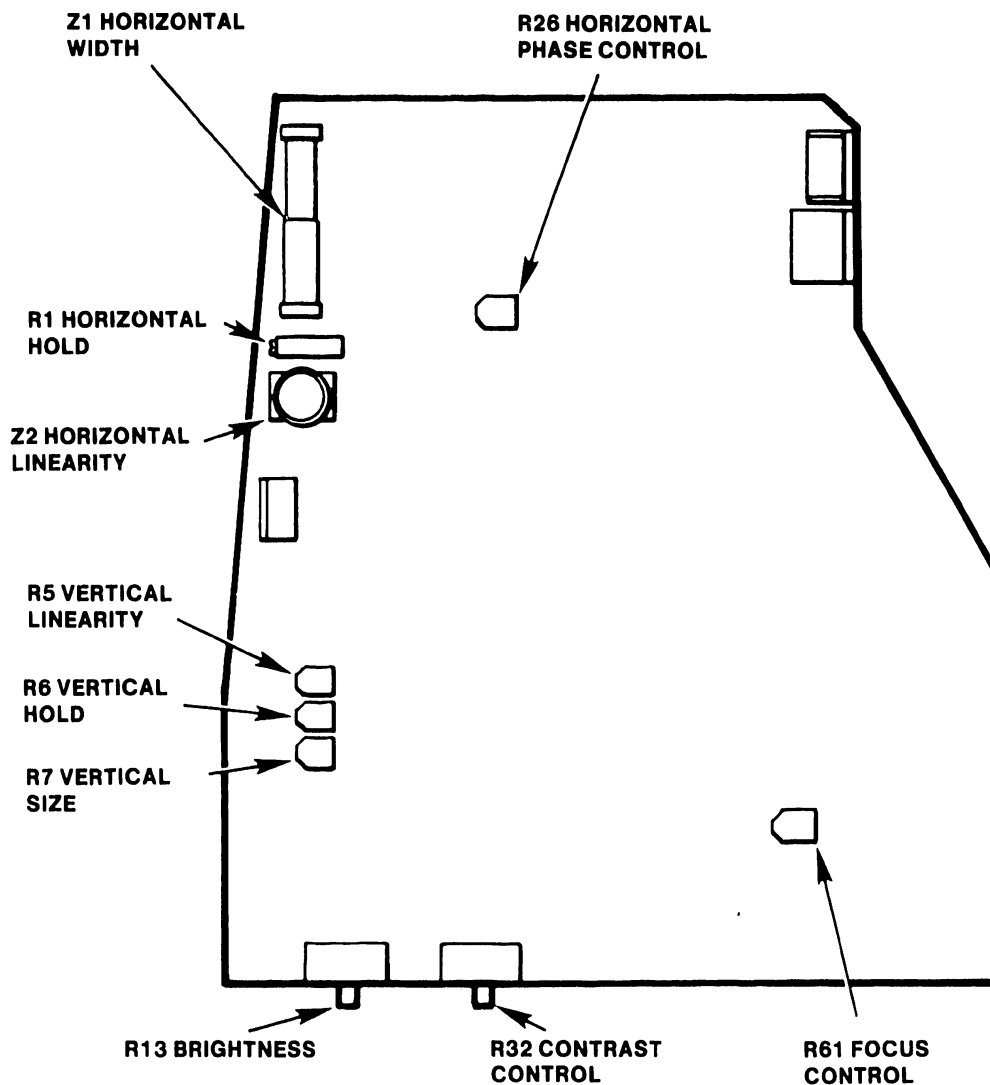
4. Adjust vertical hold control R6 to the center of its stable range.
5. Adjust horizontal hold control R1 to the center of its stable range.
6. Adjust focus control R61 for the sharpest overall display pattern.
7. Adjust vertical size control R7 so that the display pattern is $6 \pm 1/8$ inches ($15.2 \text{ cm} \pm 3 \text{ mm}$) high. Use a standard or metric scale.



5.3.4 MONITOR ALIGNMENT/DIOS SUPPORT (Continued)

5.3.4.2 8344 PCA

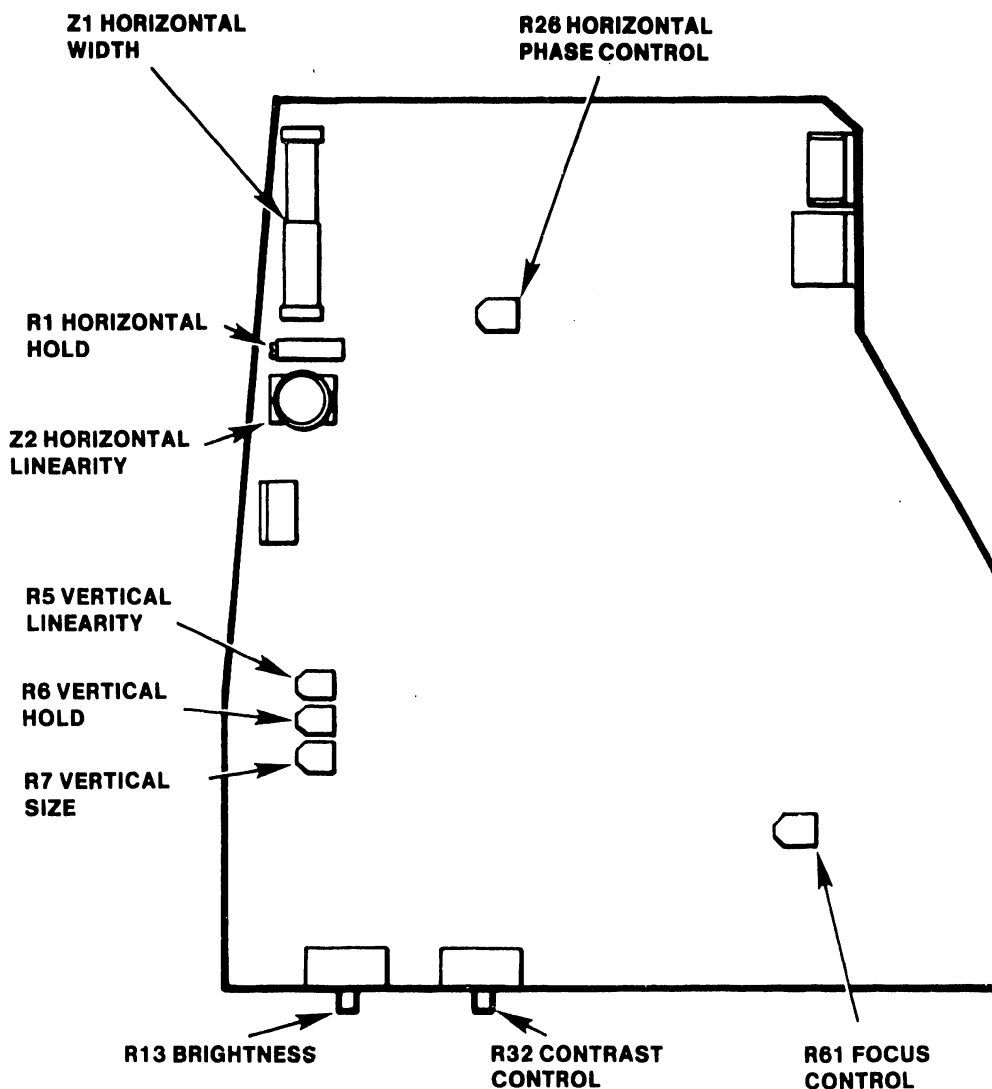
8. Adjust vertical linearity control R5 so that the squares at the top of the display are the same vertical size as the squares at the bottom of the display. This adjustment may affect the vertical height adjustment. Repeat step 7 if required.
9. Adjust horizontal width coil Z1 so that the display pattern is $8 \pm 1/8$ inches ($20.3 \text{ cm} \pm 3 \text{ mm}$) wide. Use a standard or metric scale.



5.3.4 MONITOR ALIGNMENT/DTOS SUPPORT (Continued)

5.3.4.2 8344 PCA

10. Adjust horizontal linearity coil Z2 so that the squares at the left of the display are the same horizontal size as the squares at the right of the display. This adjustment may affect the horizontal width adjustment. Repeat step 9 if required.
11. Select the circle alignment pattern in the Monitor alignment routine in the VS DTOS package. A visual check of the circles displayed should reveal no noticeable distortion, i.e., no egg-shaped or oblong forms. Repeat steps 7 through 11 if necessary.

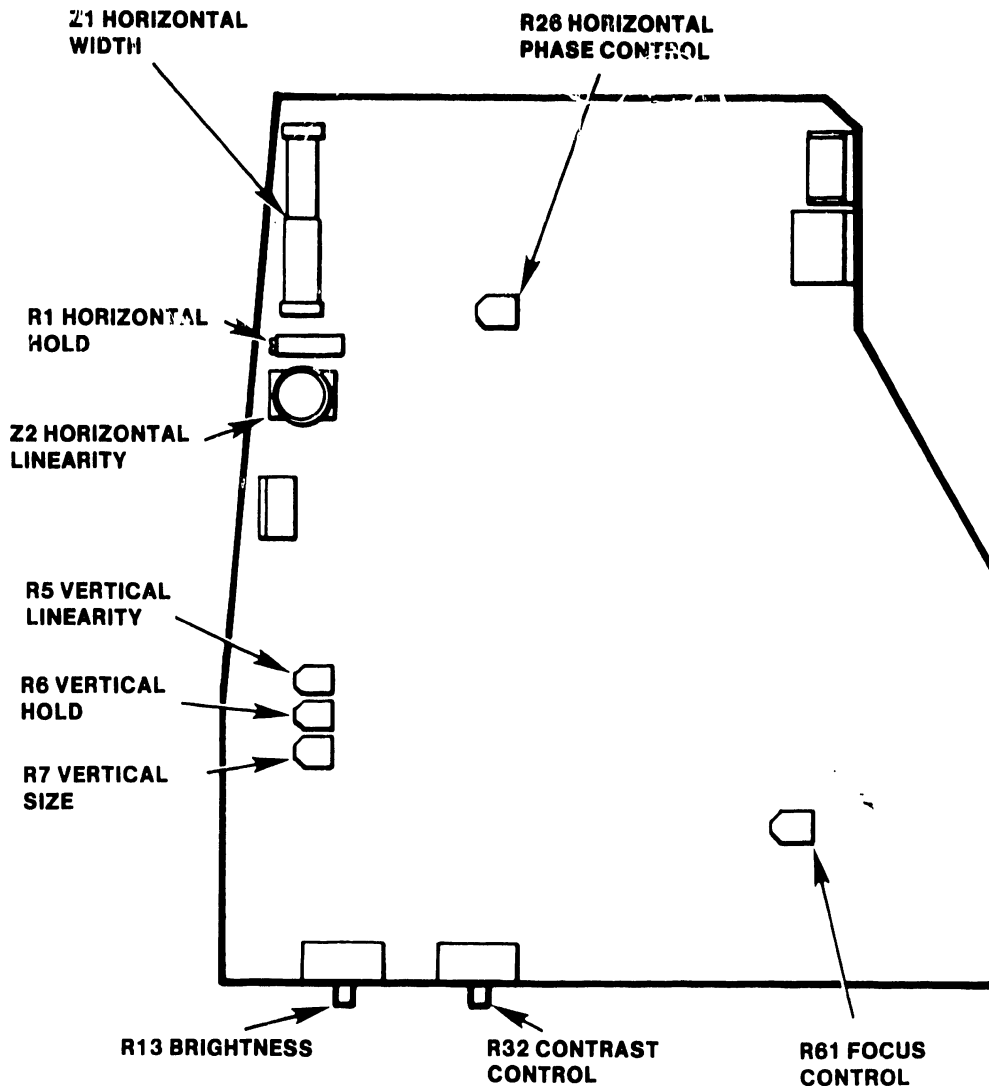


5.3.4 MONITOR ALIGNMENT/DTOS SUPPORT (Continued)

5.3.4.2 8344 PCA

12. With the circle alignment pattern still selected, adjust the Brightness control to display the raster, but not so high as to cause blooming. Adjust horizontal phase control R26 completely counterclockwise.

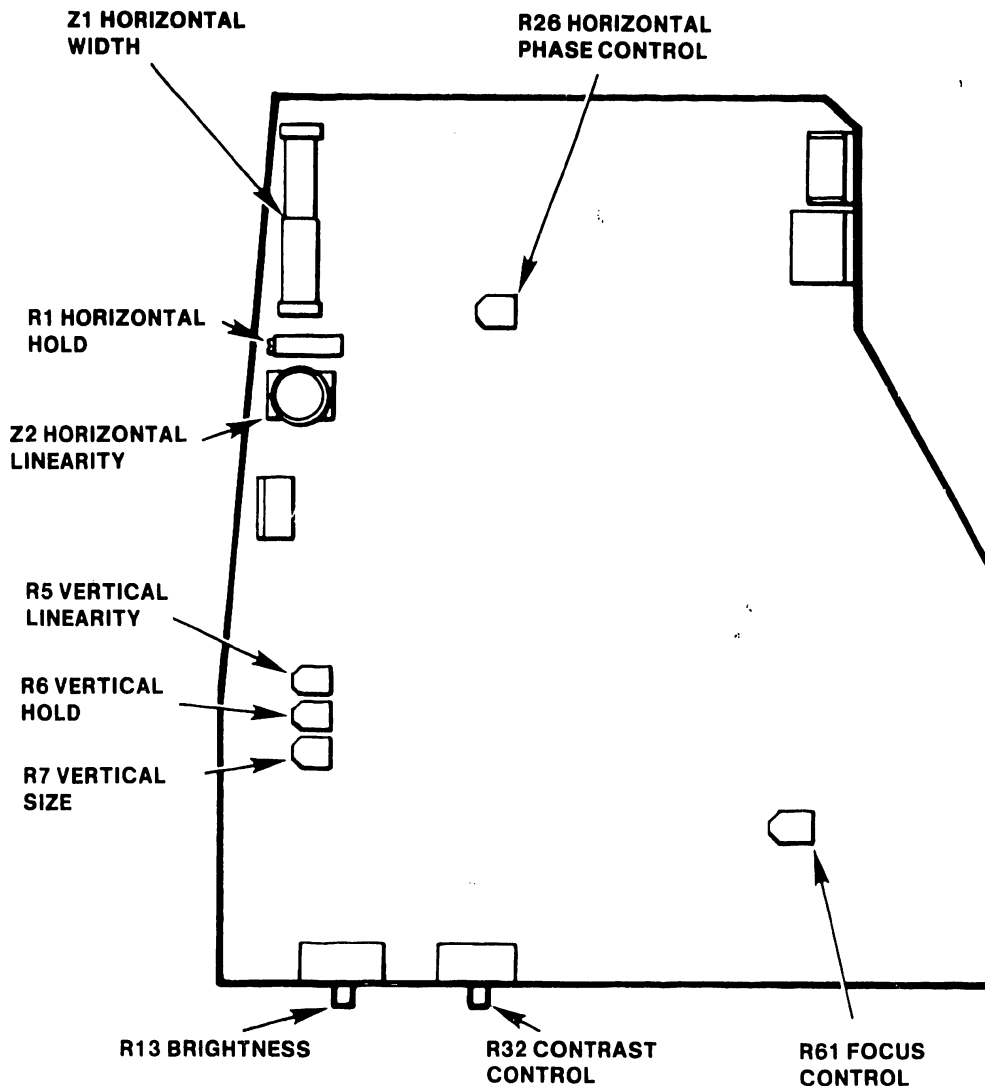
13. Adjust horizontal hold control R1 clockwise so that the video pattern overlaps at the left edge of the display, and touches the left edge of the two left-most circles.



5.3.4 MONITOR ALIGNMENT/DTOS SUPPORT (Continued)

5.3.4.2 8344 PCA

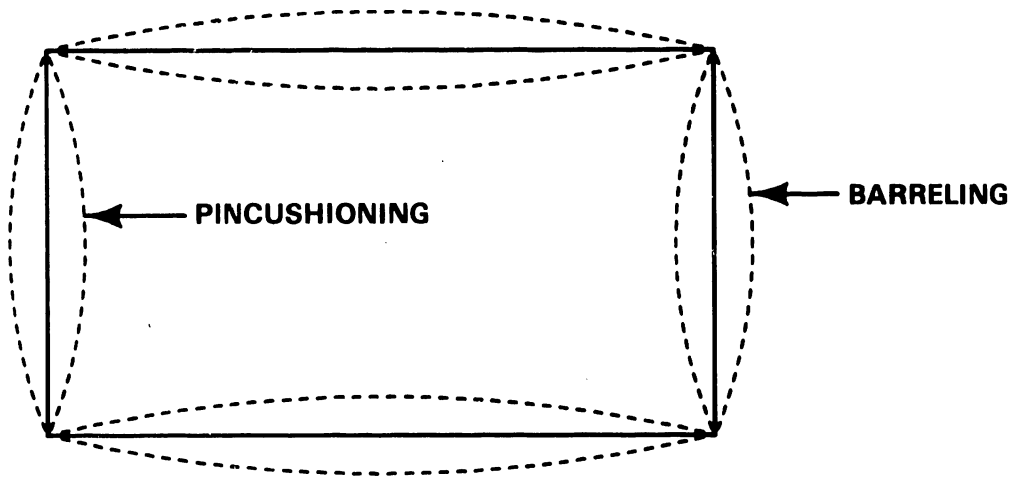
14. Adjust horizontal phase control R26 to center the display pattern in the raster. Return to the grid pattern and proceed with the next step.
15. Adjust the two tabs on the rear cover of the deflection yoke around the CRT neck one at a time to center the raster on the face of the CRT.



5.3.4 MONITOR ALIGNMENT/DTOS SUPPORT (Continued)

5.3.4.2 8344 PCA

16. Using a non-metallic straight-edge (plastic ruler, envelope, etc.) for comparison, check each perimeter line of the video display pattern for pincushioning or barreling distortion. The lines should be straight to within $\pm 1/16$ inch (1.5 mm).

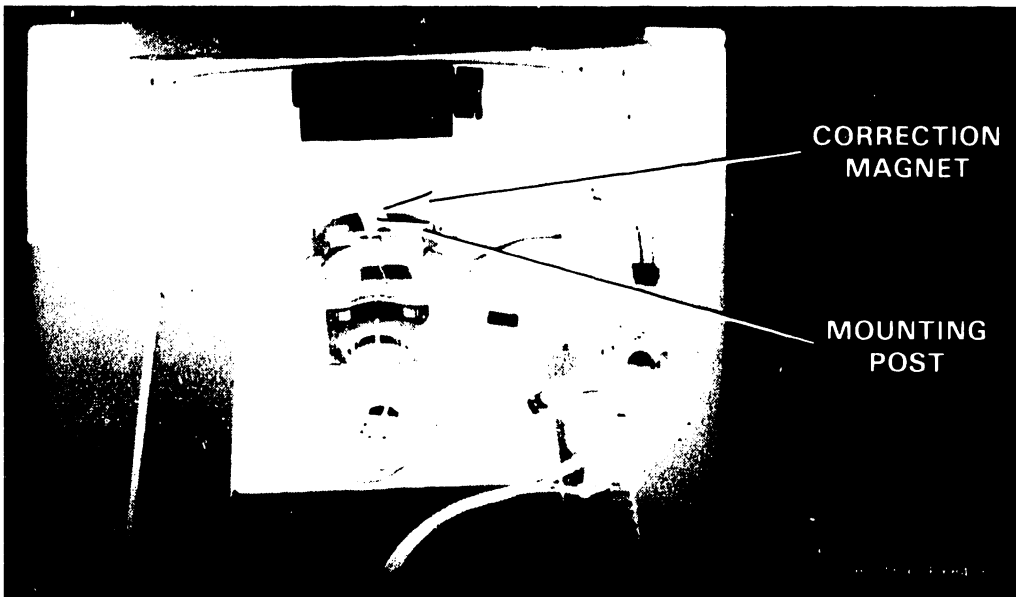


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5.3.4 MONITOR ALIGNMENT/DTOS SUPPORT (Continued)

5.3.4.2 8344 PCA

17. If either type of distortion exceeds $\pm 1/16$ inch (1.5 mm), adjustment of the magnets mounted on the posts around the perimeter of the deflection yoke is required. Rotate the magnet closest to the area of greatest distortion to make the correction.



5.3.4 MONITOR ALIGNMENT/DTOS SUPPORT (Continued)

5.3.4.2 8344 PCA

18. If correction is not possible with the magnets mounted around the yoke, magnets can be added as required to correct the distortion. This generally involves replacing an existing magnet with one of a higher gauss value. The magnets, their color-coding and part numbers are listed below.

<u>COLOR CODE</u>	<u>VALUE</u>	<u>PART NUMBER</u>
Green	Gauss 11	320-0126
Blue	Gauss 15	320-0128
White	Gauss 20	320-0127

If the above procedure does not bring the Monitor into tolerance, replacement is recommended. If the Monitor can be aligned satisfactorily, power off the workstation and reassemble the Monitor.

5.4 ELECTRONICS BASE REMOVAL/REINSTALLATION PROCEDURES

This section contains instructions regarding the removal and reinstallation of the major components of the Electronics Base. Before attempting any of these procedures, make the following preparations:

- Set the workstation I/O switch to 0 (off) and remove the ac power cord from the ac outlet.
- Disconnect the Monitor and Keyboard from the Electronics Base and move them out of the working area.
- Disconnect the dual coaxial cable from the DATA LINK connectors on the rear of the Electronics Base.

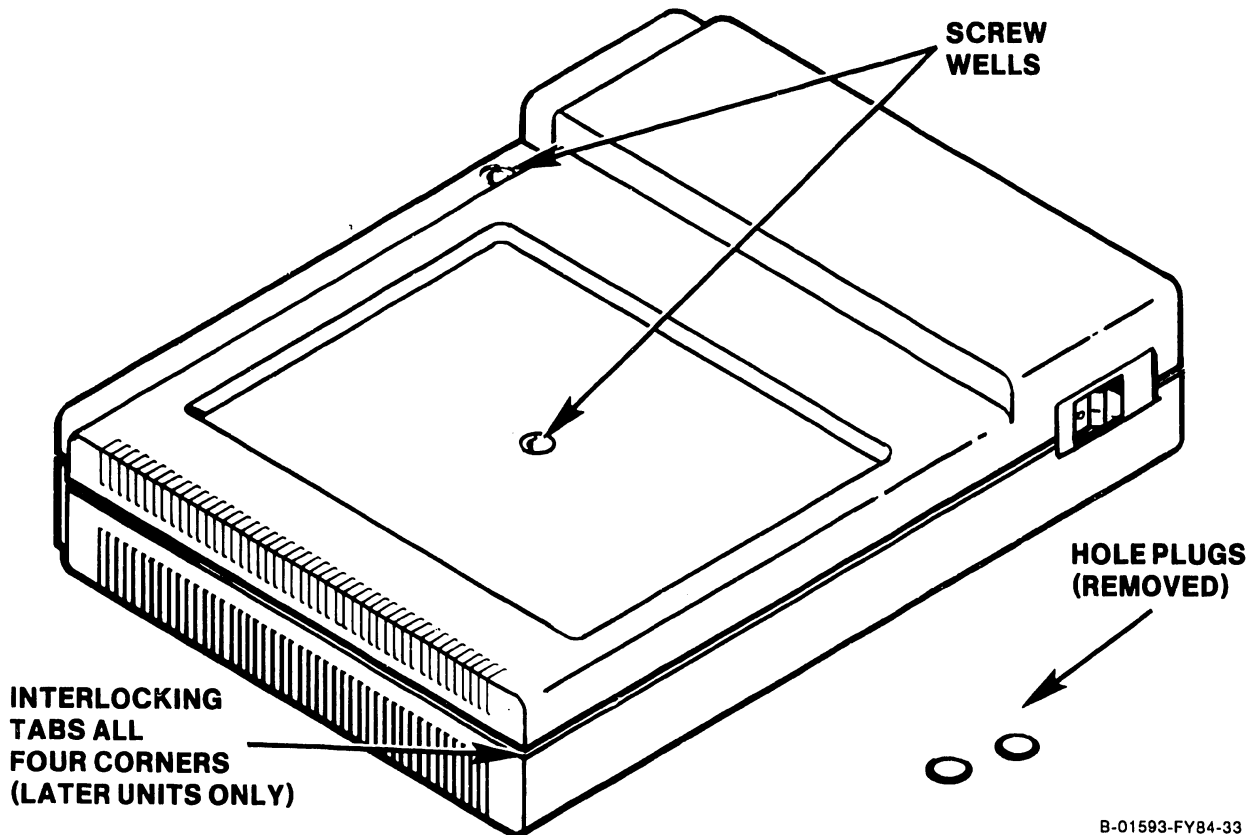
5.4.1 ELECTRONICS BASE COVER

Two types of base covers are presently in the field. Early units have covers equipped with a Velcro^R patch affixed to their front right corner. This patch interlocks with a mating patch of Velcro on the top of the Power Supply. Later units have covers with extensions that reach down into the base to interlock with the ventilation slots in each corner. The following procedure addresses both cover designs.

5.4 ELECTRONICS BASE REMOVAL/REINSTALLATION
PROCEDURES (Continued)

5.4.1 ELECTRONICS BASE COVER (Continued)

1. Referring to Figure 5-7, lift two decorative hole plugs out of the Electronics Base top cover and completely loosen, but do not remove, two phillips screws located in the screw wells under the hole plugs.



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Figure 5-7. Removing the Electronics Base Cover

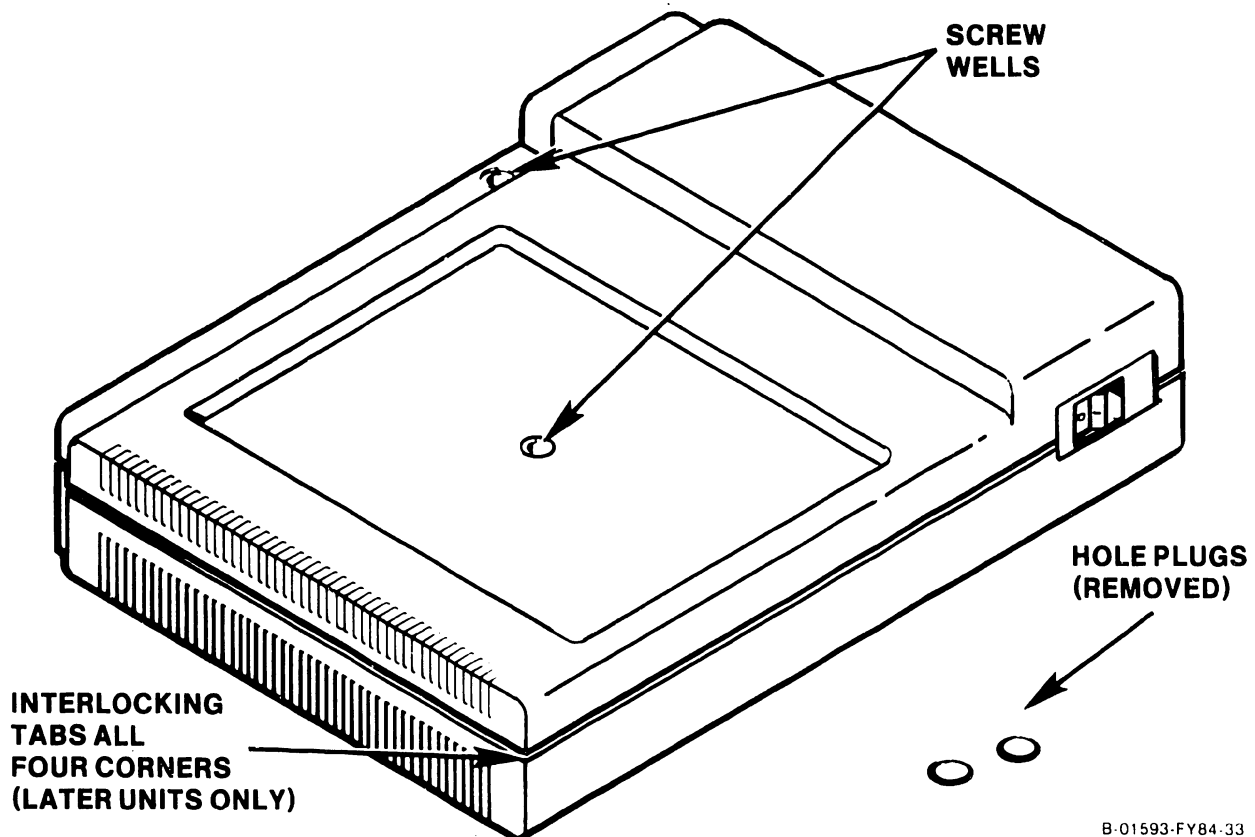
NOTE

In models with two boards, the connector headers on the rear of the boards which form the rear panel of the workstation interlock with each other and the cover and base parts of the Electronics Base unit. In the next step, be certain to separate the cover from the PCAs by holding the PCA connector headers in position when lifting the cover off.

5.4 ELECTRONICS BASE REMOVAL/REINSTALLATION
PROCEDURES (Continued)

5.4.1 ELECTRONICS BASE COVER (Continued)

2. On later units, use a small coin or flat-bladed screwdriver to disengage the cover extensions from the ventilation slots in each corner of the base. Push the interlocking tabs inward while pulling the corner away from the base.



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3. Lift the cover off of the Electronics Base. On early units the front right corner of the cover is secured to the top of the Power Supply internally by a patch of Velcro and will offer some resistance when removing the cover.

^R Velcro is a registered trademark of Velcro Industries, N.V.

5.4 ELECTRONICS BASE REMOVAL/REINSTALLATION
PROCEDURES (Continued)

5.4.1 ELECTRONICS BASE COVER (Continued)

To reinstall the Electronics Base cover, reverse the above procedure giving special attention to the following items:

- Check around the perimeter of the Electronics Base cover to make sure that the cover interlocks properly with the base, the PCA connector headers or blank filler plate at the rear and the insert around the Power Supply 1/0 switch.
- On later units, ensure that the cover extensions are interlocked in the ventilating slots in each corner of the base.
- Do not over-tighten the cover screws when reinstalling the Electronics Base cover. Tighten the screws until they are just snug.
- After the cover is installed and the screws are secured, press down on the front right corner of the cover to interlock the Velcro patch (early units).

5.4 ELECTRONICS BASE REMOVAL/REINSTALLATION
PROCEDURES (Continued)

5.4.2 POWER SUPPLY

WARNING

Do not open the switching Power Supply under any circumstance. Extremely dangerous voltage and current levels (in excess of 300 volts and unlimited current) are present within the Power Supply. Do not attempt to repair the switching Power Supply; it is field replaceable only. After powering the unit down and disconnecting the ac power plug from the wall outlet, allow one minute before removing the Power Supply to provide adequate time for any residual voltage to drain through the bleeder resistors.

1. Remove the Electronics Base cover per section 5.4.1.

5.4 ELECTRONICS BASE REMOVAL/REINSTALLATION
PROCEDURES (Continued)

5.4.2 POWER SUPPLY (Continued)

2. Referring to Figure 5-8, remove two screws securing the Power Supply to the Electronics Base, and lift the Power Supply out to the extent of its connecting harness.

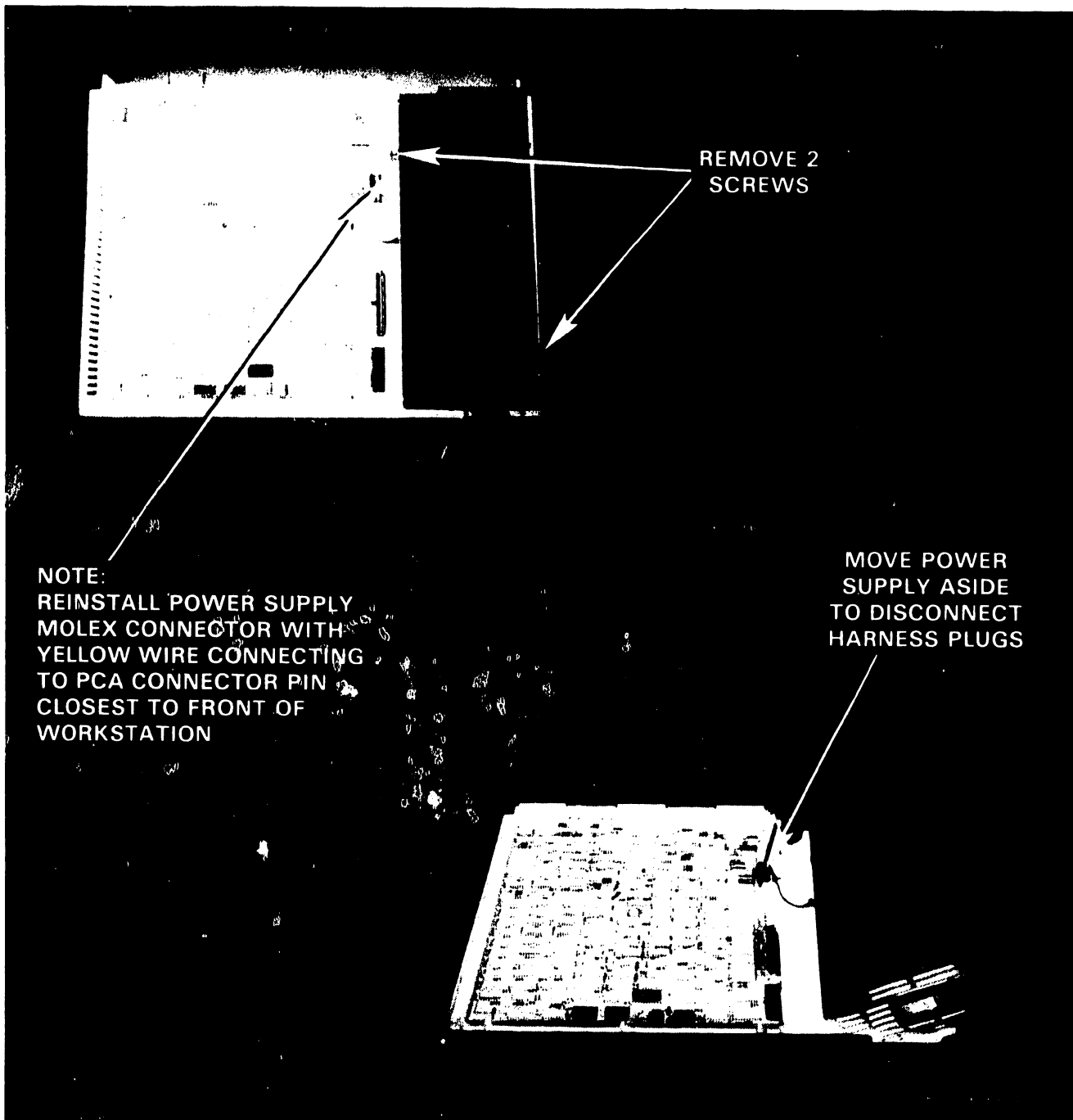


Figure 5-8. Removing the Power Supply

5.4 ELECTRONICS BASE REMOVAL/REINSTALLATION
PROCEDURES (Continued)

5.4.2 POWER SUPPLY (Continued)

3. Unplug the Power Supply harness from the 8287 board and, if used in the 4230, the 8298 board and remove the Power Supply.

To reinstall the Power Supply, reverse the removal procedure giving special attention to the following items:

CAUTION

Reconnect the Power Supply plug with the yellow wire to the pin closest to the front of the workstation. Ensure that the molex connectors mate with the pins on the PCAs correctly. Shifting the connectors to the left or right could seriously damage the PCAs.

- If the Power Supply is being replaced, transfer the ac power cord from the original unit to the replacement. If the replacement Power Supply does not have a Velcro patch attached on the top front of its cover, install one (early units). The part number for this patch is 458-3309.
- Replacement power supplies will also need to have the insert around the I/O switch installed. This is a snap-in type plastic insert which, in most cases, will not be able to be removed from the original unit without damage. Order an extra insert for each replacement power supply.

5.4 ELECTRONICS BASE REMOVAL/REINSTALLATION
PROCEDURES (Continued)

5.4.2 POWER SUPPLY (Continued)

- Do not over-tighten the Power Supply screws when reinstalling the Power Supply. Tighten the screws until they are just snug.

5.4.3 PRINTED CIRCUIT ASSEMBLIES (PCAs)

Please note that the following procedure addresses all models of the 4200-Series Workstations, both one and two-board models. The 4205 uses a single board only while the 4230 can have two boards if the TC option is present.

5.4 ELECTRONICS BASE REMOVAL/REINSTALLATION
PROCEDURES (Continued)

5.4.3 PRINTED CIRCUIT ASSEMBLIES (PCAs)

1. Remove the Electronics Base cover per section 5.4.1.
2. Remove the switching Power Supply per section 5.4.2.

5.4 ELECTRONICS BASE REMOVAL/REINSTALLATION PROCEDURES (Continued)

5.4.3 PRINTED CIRCUIT ASSEMBLIES (Continued)

3. For a single board model, lift out the filler panel (Figure 5-9) resting on top of the bottom PCA connector header. Proceed to step 5. For two board models, press the locking arms on both sides of the I/O ribbon cable connector outward to disengage the cable from the connector on the top PCA. Disconnect the cable from the connector. Proceed to step 4.

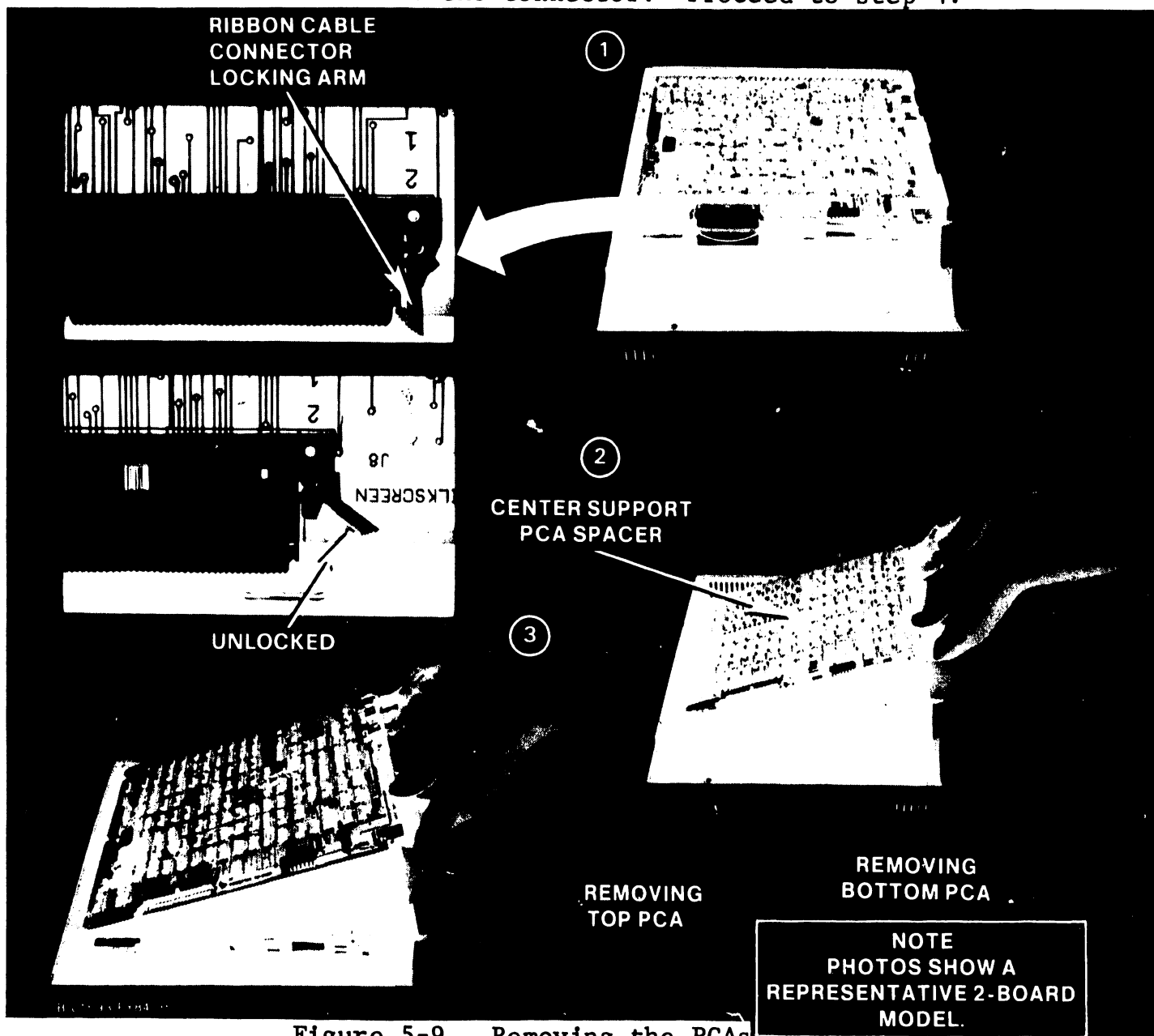


Figure 5-9. Removing the PCAs

5.4 ELECTRONICS BASE REMOVAL/REINSTALLATION
PROCEDURES (Continued)

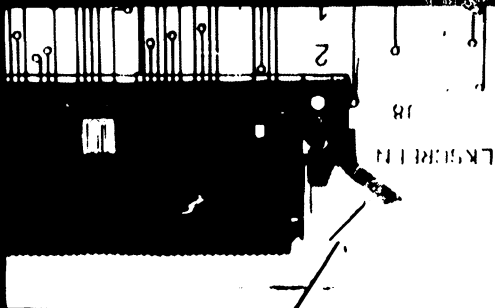
5.4.3 PRINTED CIRCUIT ASSEMBLIES (Continued)

4. Lift up the rear edge of the top PCA and move it rearward to disengage it from its capture slots in the front of the base.

CAUTION

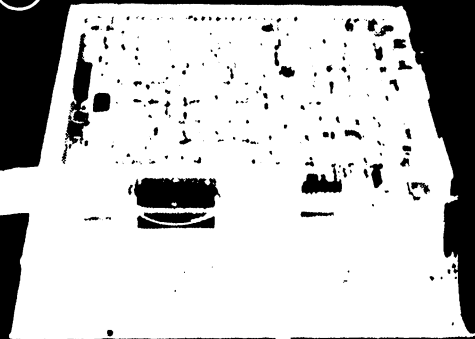
Do not misplace the center support/spacer. It serves the specific purpose of providing mechanical support for the Monitor placed atop the Electronics Base as well as maintaining proper spacing of the PCAs within the Base.

RIBBON CABLE
CONNECTOR
LOCKING ARM



UNLOCKED

1



2

CENTER SUPPORT
PCA SPACER



3

REMOVING
TOP PCA

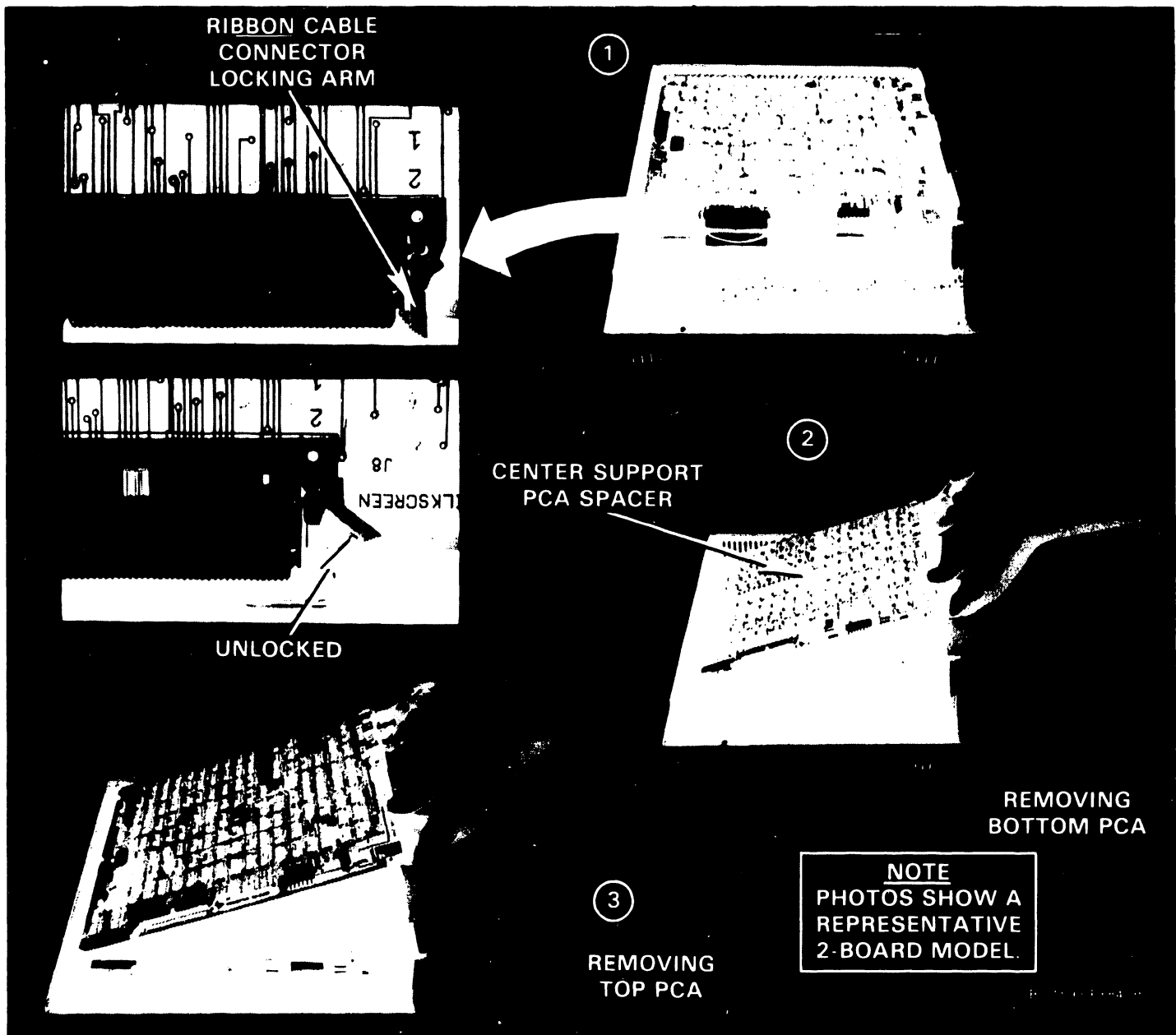
REMOVING
BOTTOM PCA

NOTE
PHOTOS SHOW A
REPRESENTATIVE
2-BOARD MODEL

5.4 ELECTRONICS BASE REMOVAL/REINSTALLATION
PROCEDURES (Continued)

5.4.3 PRINTED CIRCUIT ASSEMBLIES (Continued)

5. Remove the center support/PCA spacer from its center hole in the bottom PCA. Retain the support/spacer for reinstallation.
6. For two board models, press the locking arms on both sides of the I/O ribbon cable connector outward to disengage the cable from the connector on the bottom PCA. Disconnect the cable from the connector.

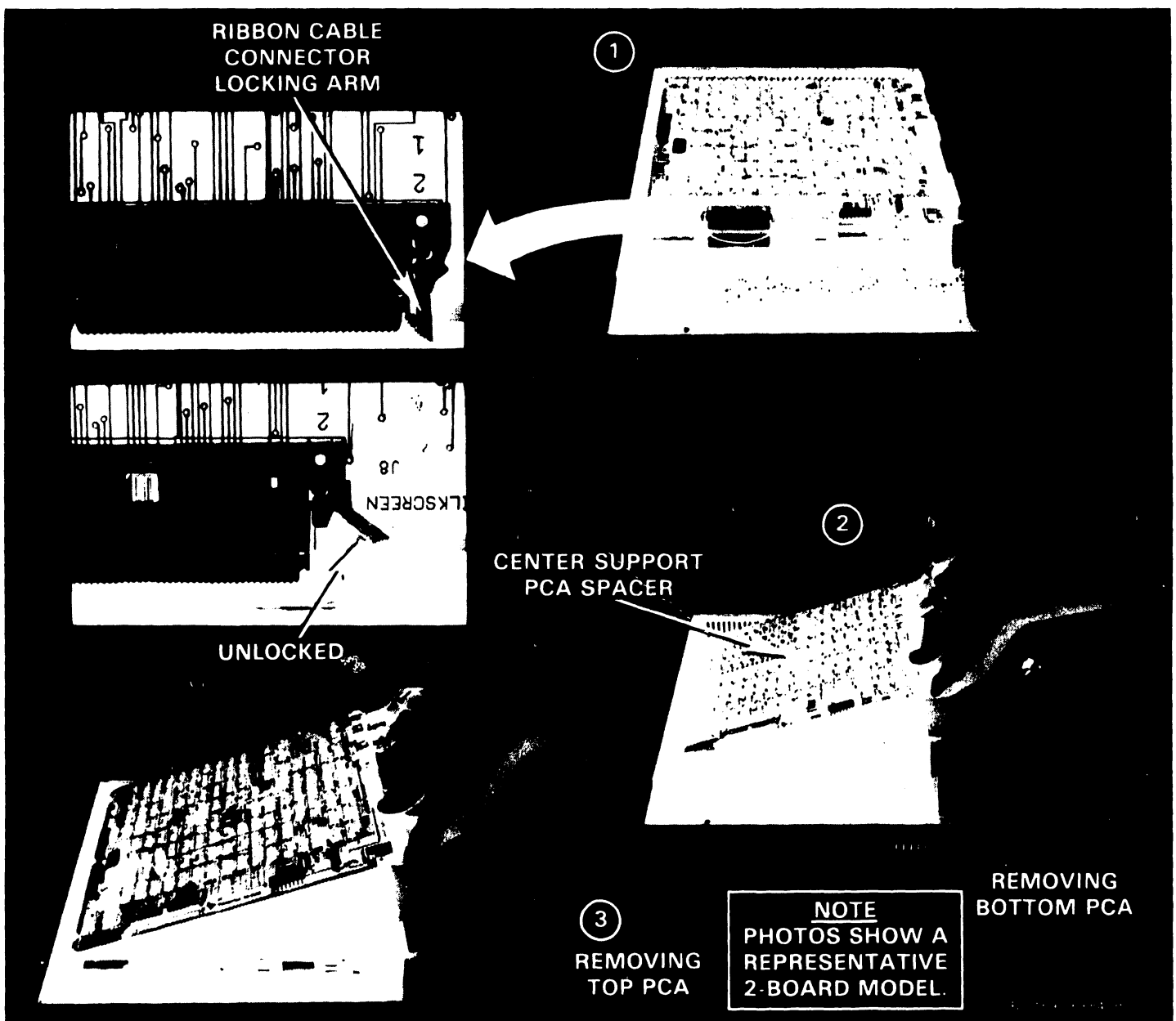


5.4 ELECTRONICS BASE REMOVAL/REINSTALLATION
PROCEDURES (Continued)

5.4.3 PRINTED CIRCUIT ASSEMBLIES (Continued)

7. Lift up the rear edge of the bottom PCA and move it rearward to disengage it from its capture slots in the front of the base.

To reinstall the PCAs, reverse the removal procedure, giving special attention to the reinstallation of the center support/spacer.



5.5 MONITOR REMOVAL/REINSTALLATION PROCEDURES

This section contains instructions regarding the removal and reinstallation of the major components of the Monitor. Before attempting any of these procedures, make the following preparations:

- Set the workstation I/O switch to 0 (off).
- Disconnect the Monitor dual interconnection cable from the underside of the Monitor, and move the Monitor to a suitable work area.

5.5.1 REMOVING THE MONITOR COVER

1. Turn the monitor upside down, resting it on its top. Remove the two screws that hold the cover to the faceplate (Figure 5-10). Stand the monitor up on its pedestal.

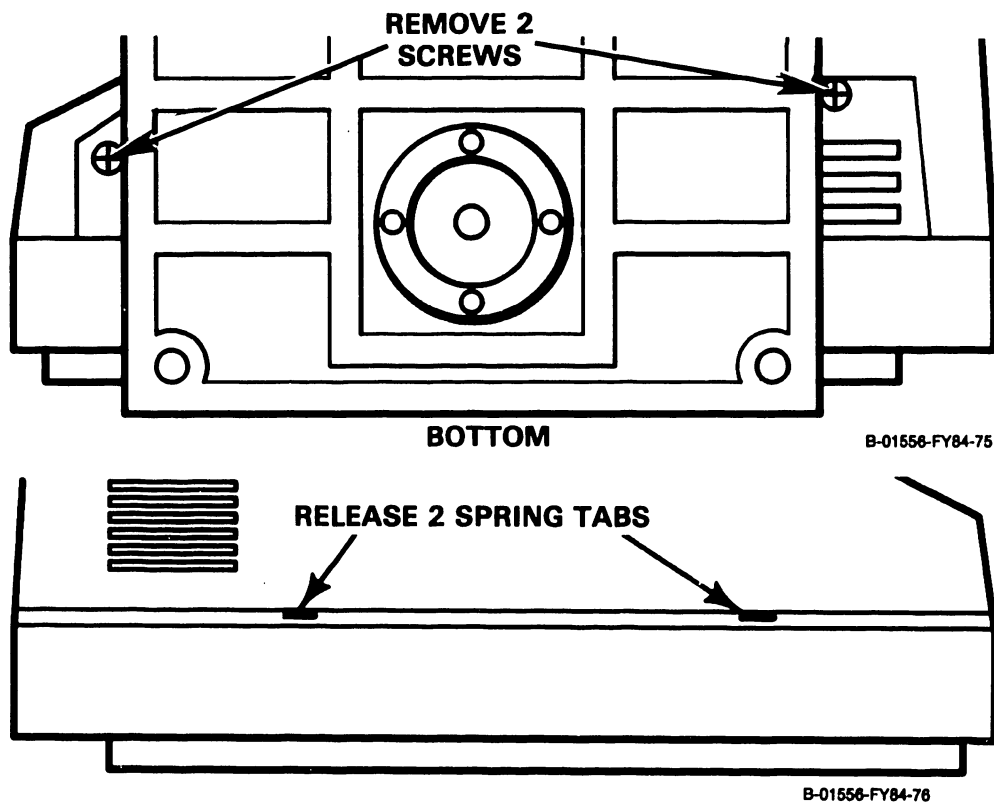


Figure 5-10. Removing the Monitor Cover

5.5 MONITOR REMOVAL/REINSTALLATION (Continued)

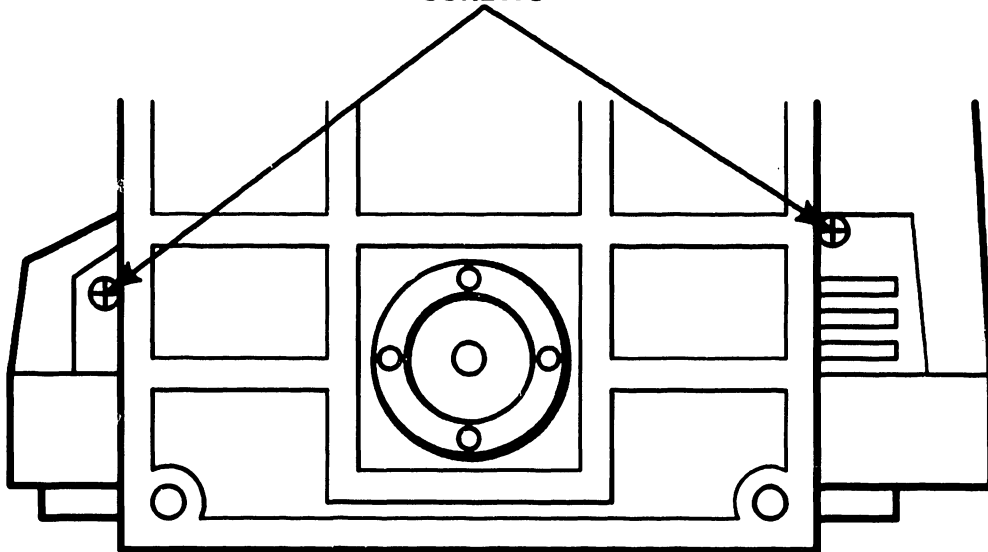
5.5.1 REMOVING THE MONITOR COVER (Continued)

CAUTION

Do not twist the screwdriver while performing the monitor cover removal in the next step, or else the cover will be damaged.

2. Locate the two spring locking tabs on the top of the Monitor along the seam where the cover meets the faceplate.
3. Using a small, flat-blade screwdriver, push the right-hand spring tab down through its slot to free the cover on the right side.

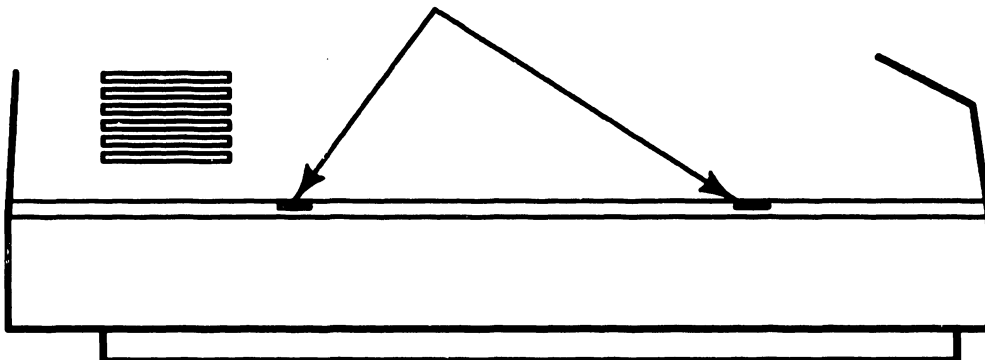
**REMOVE 2
SCREWS**



BOTTOM

B-01558-FY84-75

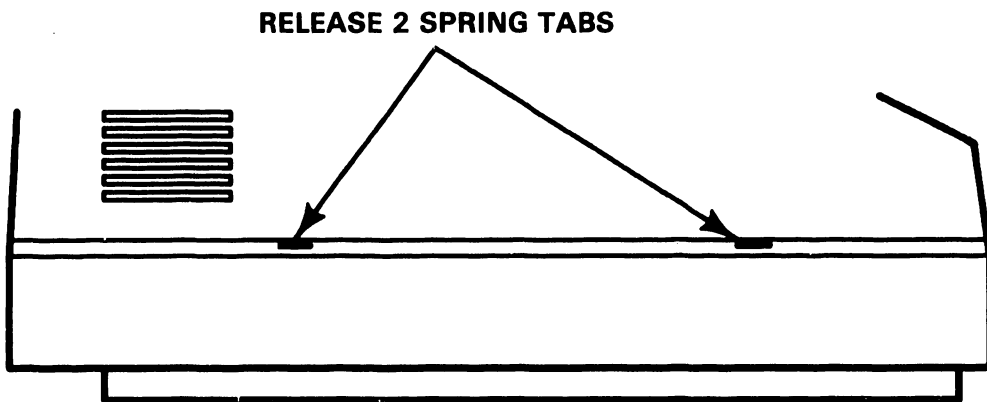
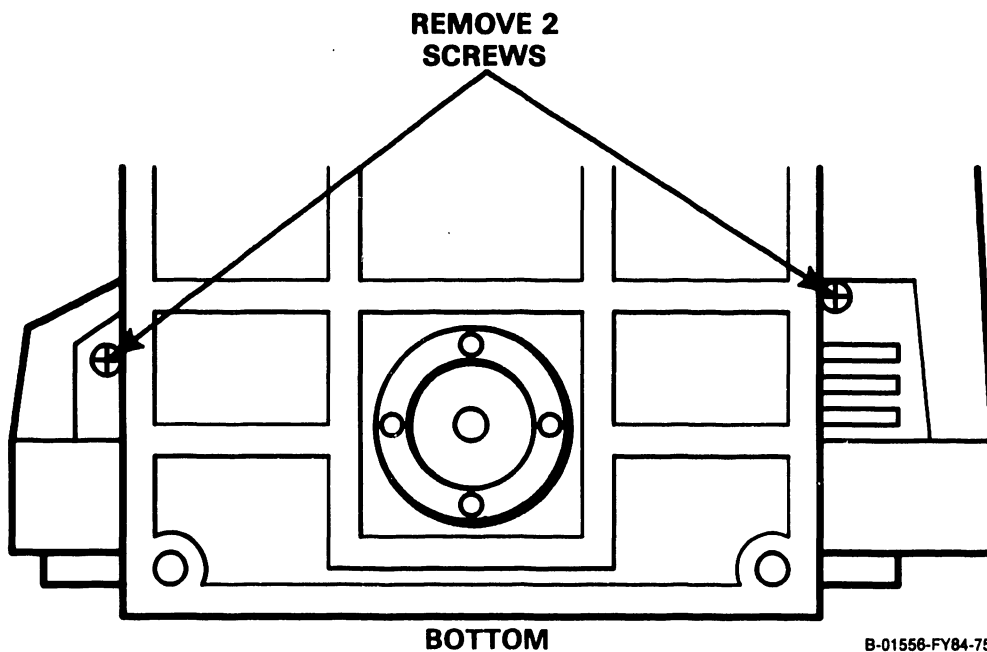
RELEASE 2 SPRING TABS



B-01558-FY84-76

5.5 MONITOR REMOVAL/REINSTALLATION (Continued)**5.5.1 REMOVING THE MONITOR COVER (Continued)**

4. Holding the right side of the cover free, push the left-hand spring tab down through its slot to free the cover on the left side.
5. Remove the cover by pulling it straight back, clearing the neck of the CRT.



5.5 MONITOR REMOVAL/REINSTALLATION (Continued)

5.5.1 REMOVING THE MONITOR COVER (Continued)

WARNING

Before proceeding with any further removal/reinstallation work inside the Monitor, perform the CRT Anode Discharge Procedure in section 5.5.2.

To reinstall the cover, reverse the removal procedure, with the exception of steps 2, 3 and 4. Simply slide the cover back in place, pressing it gently against the face plate, causing the spring tabs to lock in place.

5.5 MONITOR REMOVAL/REINSTALLATION (Continued)

5.5.2 CRT ANODE DISCHARGE PROCEDURE

Even with power removed, the Monitor cathode ray tube (CRT) can hold a charge of several thousand volts. To eliminate the risk of accidental CRT discharge which can result in serious injury, discharge the CRT anode as follows:

1. Attach one end of a length of insulated wire to the metal shaft of a plastic-handled, heavy-duty screwdriver.
2. Attach the other end of the wire to chassis ground.
3. Using a non-conductive tool such as a plastic alignment tool, carefully raise the edge of the rubber anode cap high enough to insert the screwdriver.
4. Taking care not to touch the metal shaft of the screwdriver or any metal part of the workstation, discharge the CRT anode by touching the anode clip with the grounded screwdriver.
5. After discharging the CRT, remove the grounding wire and reseal the rubber anode cap.

5.5 MONITOR REMOVAL/REINSTALLATION (Continued)

5.5.3 MONITOR PCA

1. Remove the cover per section 5.5.1.
2. Remove the Brightness and Contrast control knobs located on the front upper left of the Monitor by pulling them straight out.
3. Unplug the CRT cable connector from J1 located at the rear of the Monitor PCA.
4. Disconnect the FASTON clip from the retaining screw ground lug located at the top left side near the Brightness and Contrast potentiometers.
5. Disconnect the CRT socket connector.
6. Disconnect the high-voltage anode connector from the CRT.
7. Using a flat-bladed screwdriver with a long shaft, unscrew the Monitor PCA holding screw securing the PCA to the faceplate.
8. Remove the Monitor PCA.

To reinstall the Monitor PCA, reverse the removal procedure.

5.6 KEYBOARD REMOVAL/REINSTALLATION PROCEDURES

The only removal/reinstallation procedure for the Keyboard is for its cover. The procedure is presented below.

1. Disconnect the Keyboard cable from its connector on the rear of the Electronics Base.
2. Referring to Figure 5-11, turn the Keyboard top down on a suitable work surface and remove two screws on the bottom.

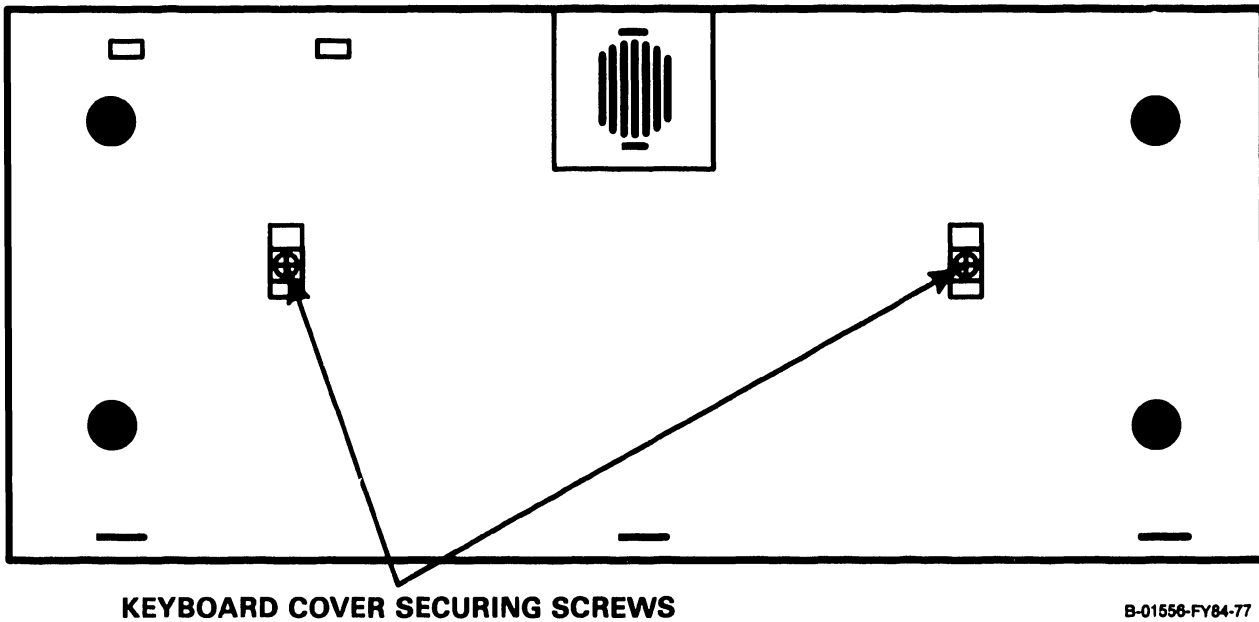
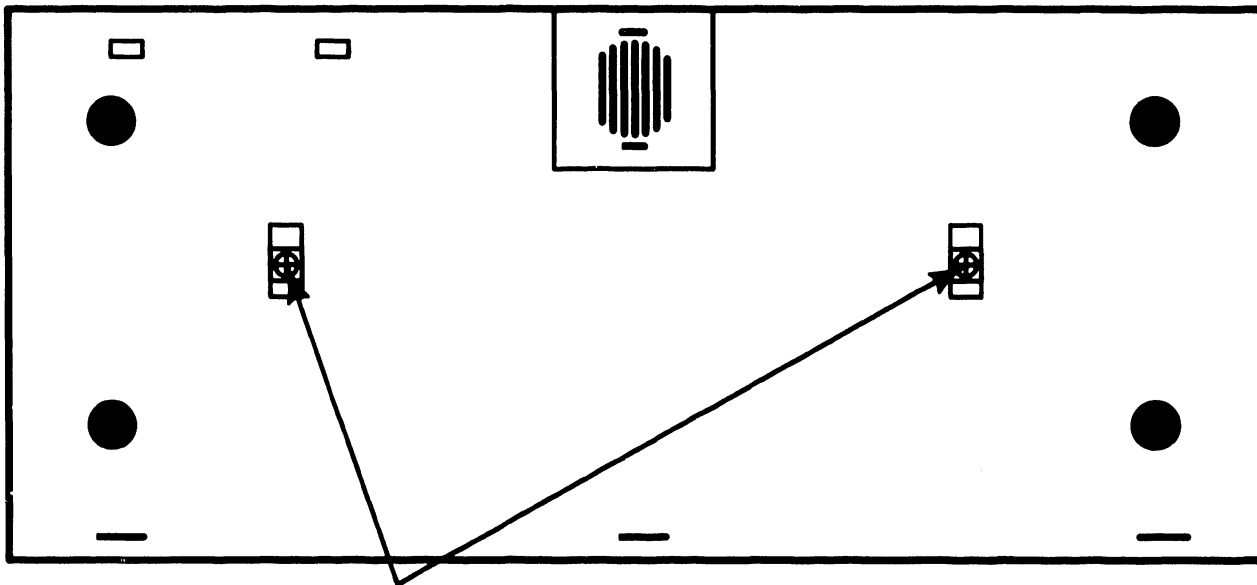


Figure 5-11. Removing the Keyboard Cover

5.6 KEYBOARD REMOVAL/REINSTALLATION (Continued)

3. Holding the top and bottom halves of the Keyboard together, turn the unit face up and place on the work surface.
4. Lift the top cover off of the Keyboard, being careful to retain the two circular collars around each of the screw holes.

To reinstall the Keyboard cover, reverse the removal procedure being sure that the circular collars around the Keyboard screw holes are in place.



KEYBOARD COVER SECURING SCREWS

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5.7 SWITCH SETTINGS

The 4230/05 Workstations are shipped with all internal switches preset for proper operation. This eliminates the need to disassemble the Electronics Base unit and Keyboard at installation in order to access the internal switches. The switch settings given in sections 5.7.1 and 5.7.2 are for reference only, as may be required when setting up a replacement 8287, 8287-1 or 8287-3 board, a new Keyboard or installing an option board.

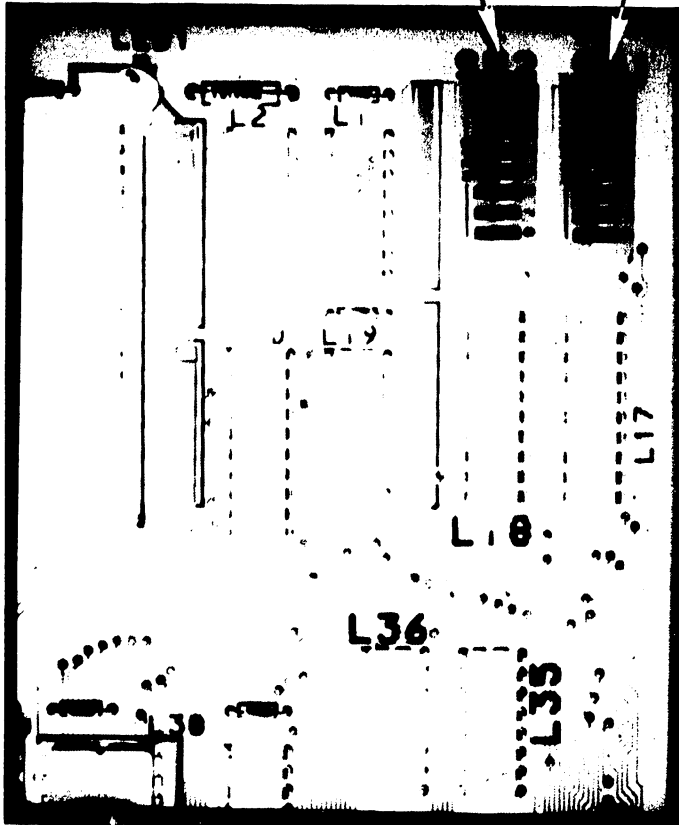
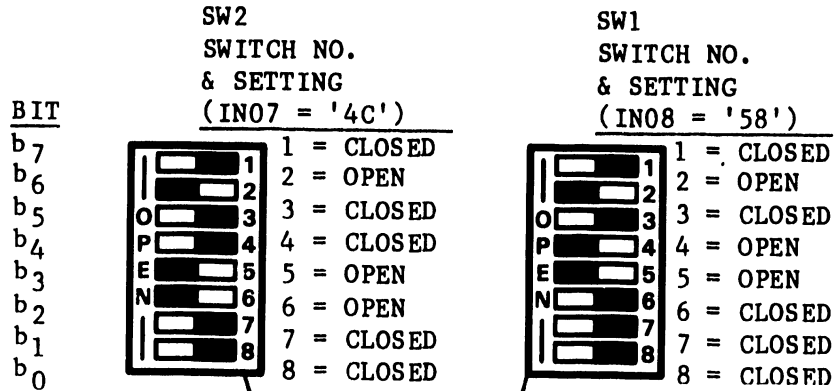
5.7.1 PCA SWITCH SETTINGS

The 210-8287, 210-8287-1 and 210-8287-3 boards each contain two switchbanks which must be set to define the type of workstation for the host system. These switches are SW2 and SW1 which are read during instructions IN07 and IN08 respectively. The required switch settings for the 8287 PCA (4230), 8287-1 PCA (4205) and the 8287-3 PCA (4230/05 Arabic) are shown on the next two frames.

5.7 SWITCH SETTINGS (Continued)

5.7.1 PCA SWITCH SETTINGS (Continued)

8287 PCA-4230 W.S. / 8287-3 PCA-4230 ARABIC W.S.:



■ = ACTUAL SWITCH POSITION

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Figure 5-12. 210-8287 PCA Switch Settings (4230)

5.7 SWITCH SETTINGS (Continued)

5.7.1 PCA SWITCH SETTINGS (Continued)

8287-1 PCA - 4205 W.S. (OR) 8287-3 PCA - 4205 ARABIC W.S.:

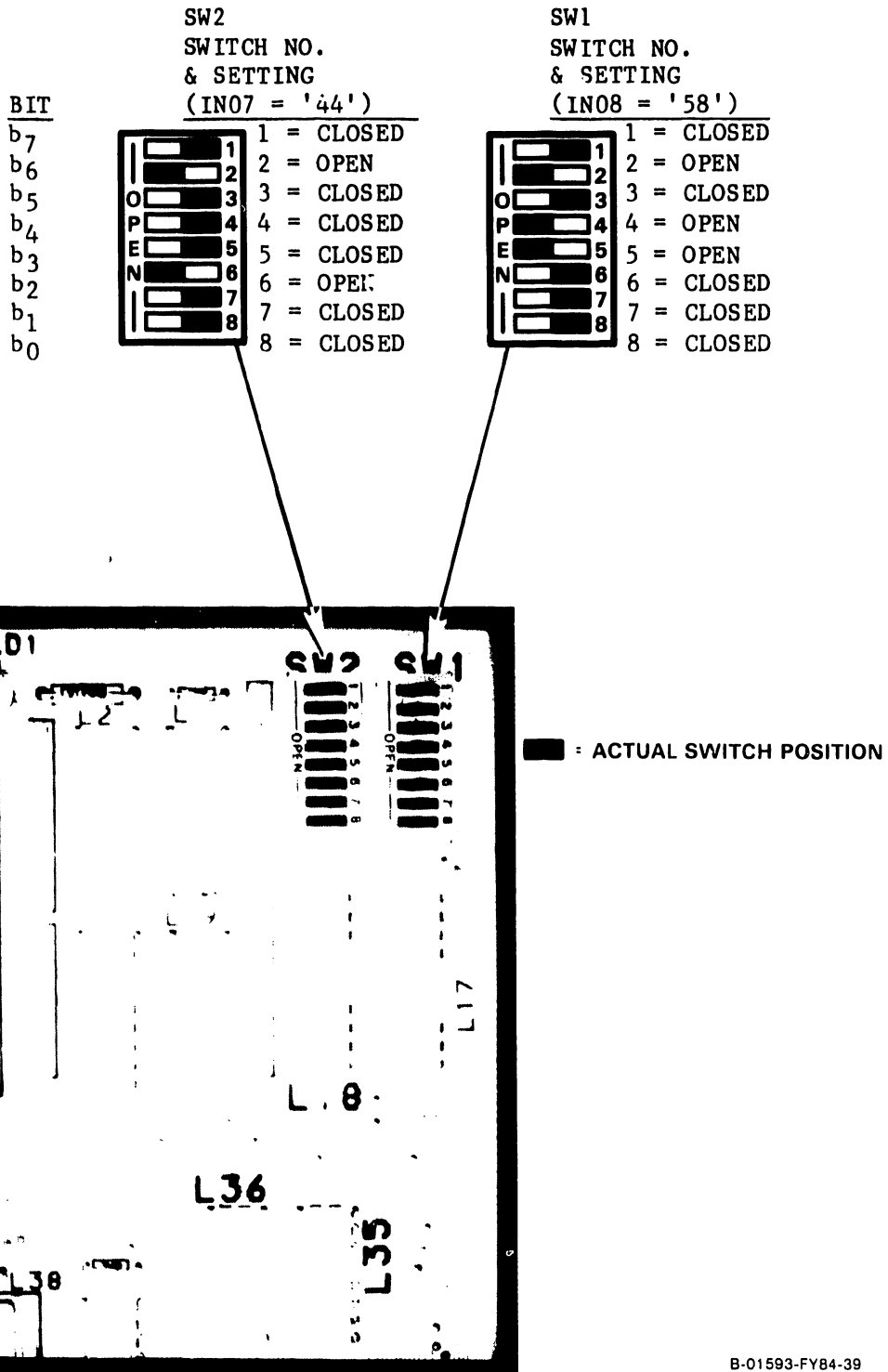
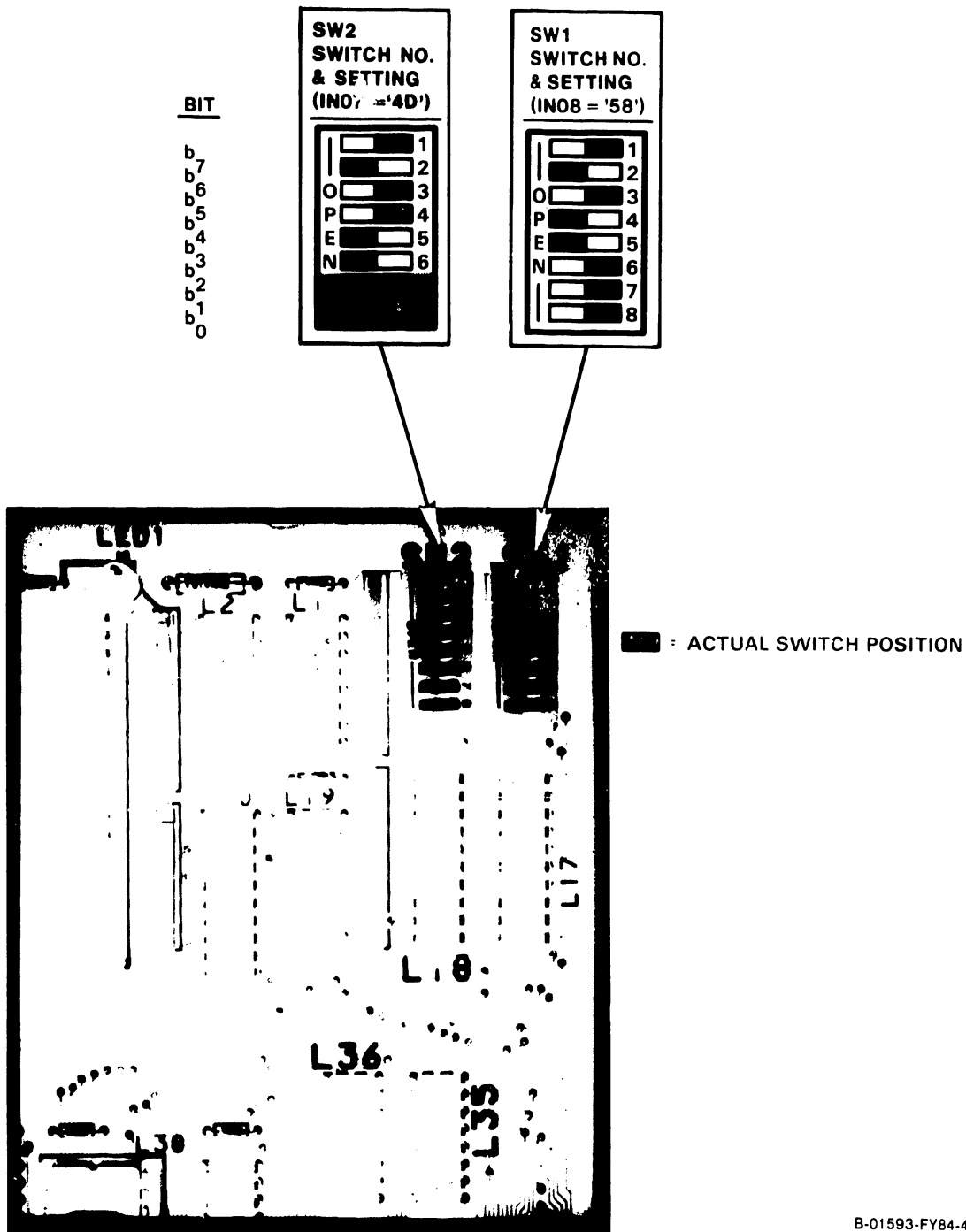


Figure 5-13. 210-8287-1 PCA SW. Settings (4205)

5.7.1 PCA SWITCH SETTINGS (Continued)

5.7.1.1 TC Switch Settings

To allow proper operation of the TC option on the 4230 workstation, SW 1 on PCA 210-8287 must be selected as shown in Figure 5-14.



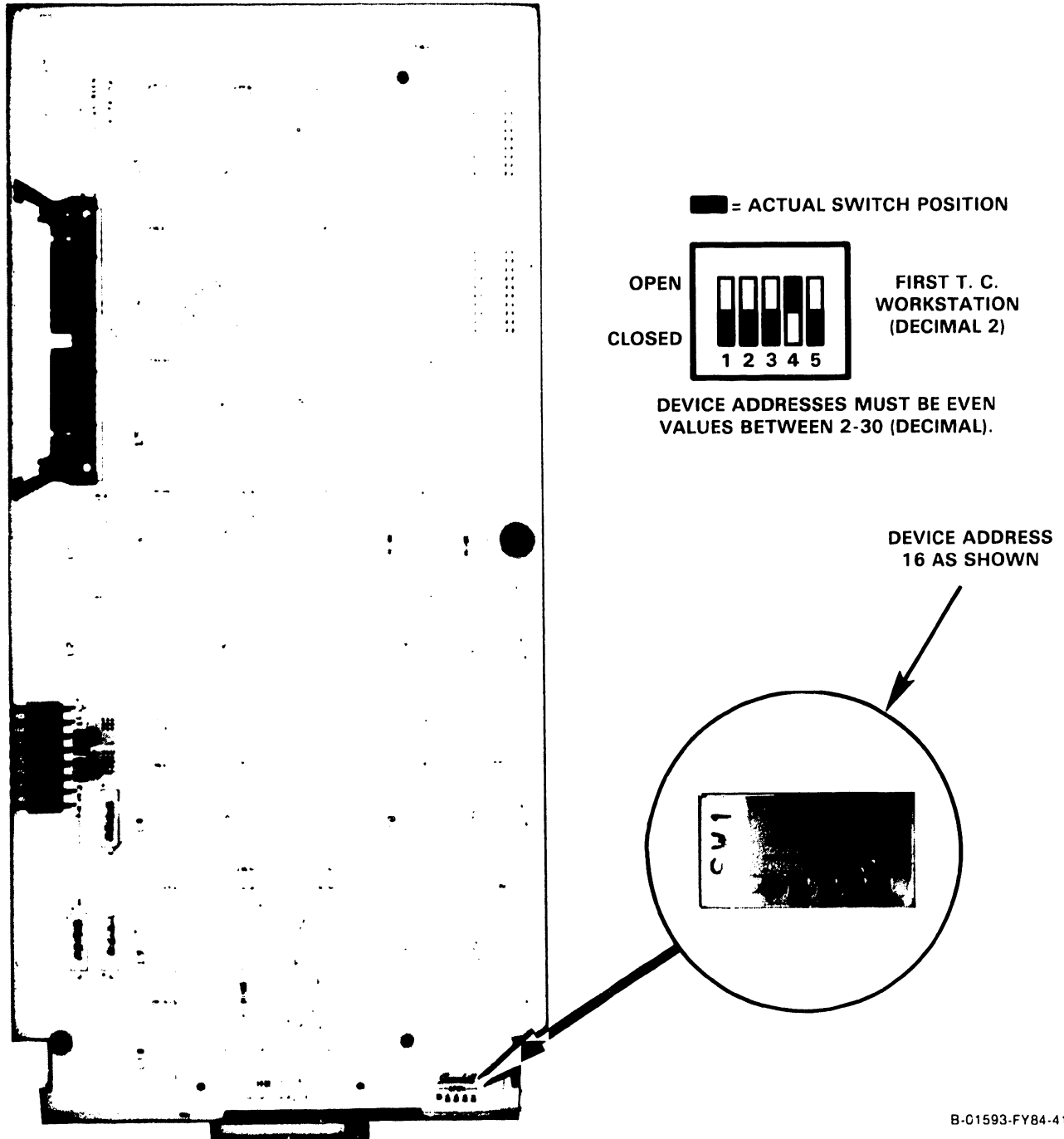
B-01593-FY84-40

Figure 5-14. 210-8287 Switch Settings for TC

5.7.1 PCA SWITCH SETTINGS (Continued)

5.7.1.1 TC Switch Settings

In addition, SW1 on 210-8298 must be set as shown in Figure 5-15.



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Figure 5-15. 210-8298 PCA Switch Setting

5.7 SWITCH SETTINGS (Continued)

5.7.2 KEYBOARD SWITCH SETTINGS

The universal, low profile keyboard (figure 5-16) used with the 4230/05 Workstation contains two 8-bit DIP switches totaling 16 bits in length. Each universal keyboard is assigned a 15-bit number (bits 0 - 14) that uniquely identifies it. Models of the Keyboard which are available in expanded format are indicated in the table. The expanded universal keyboard of a particular language is defined by setting the most significant bit (bit 15).

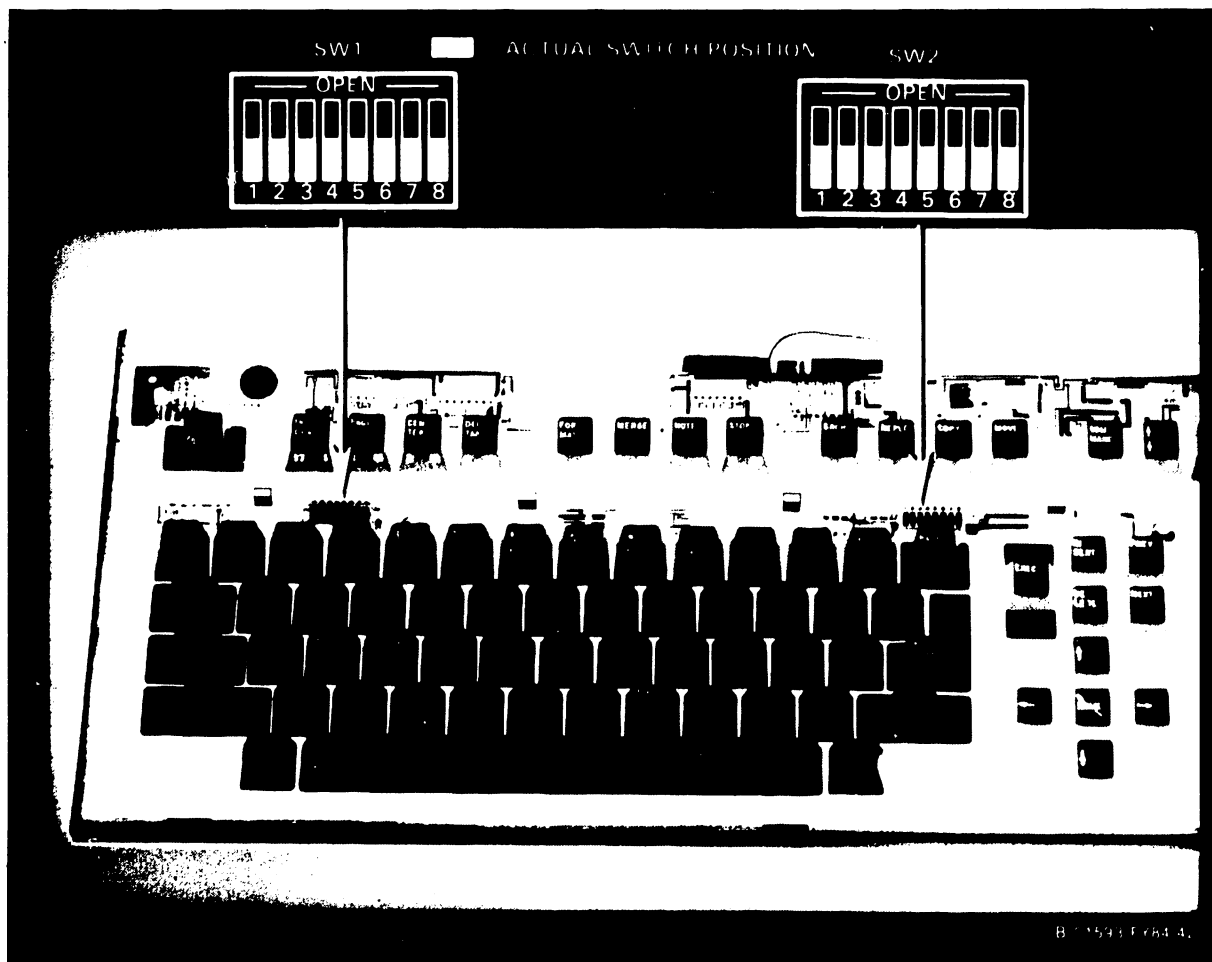
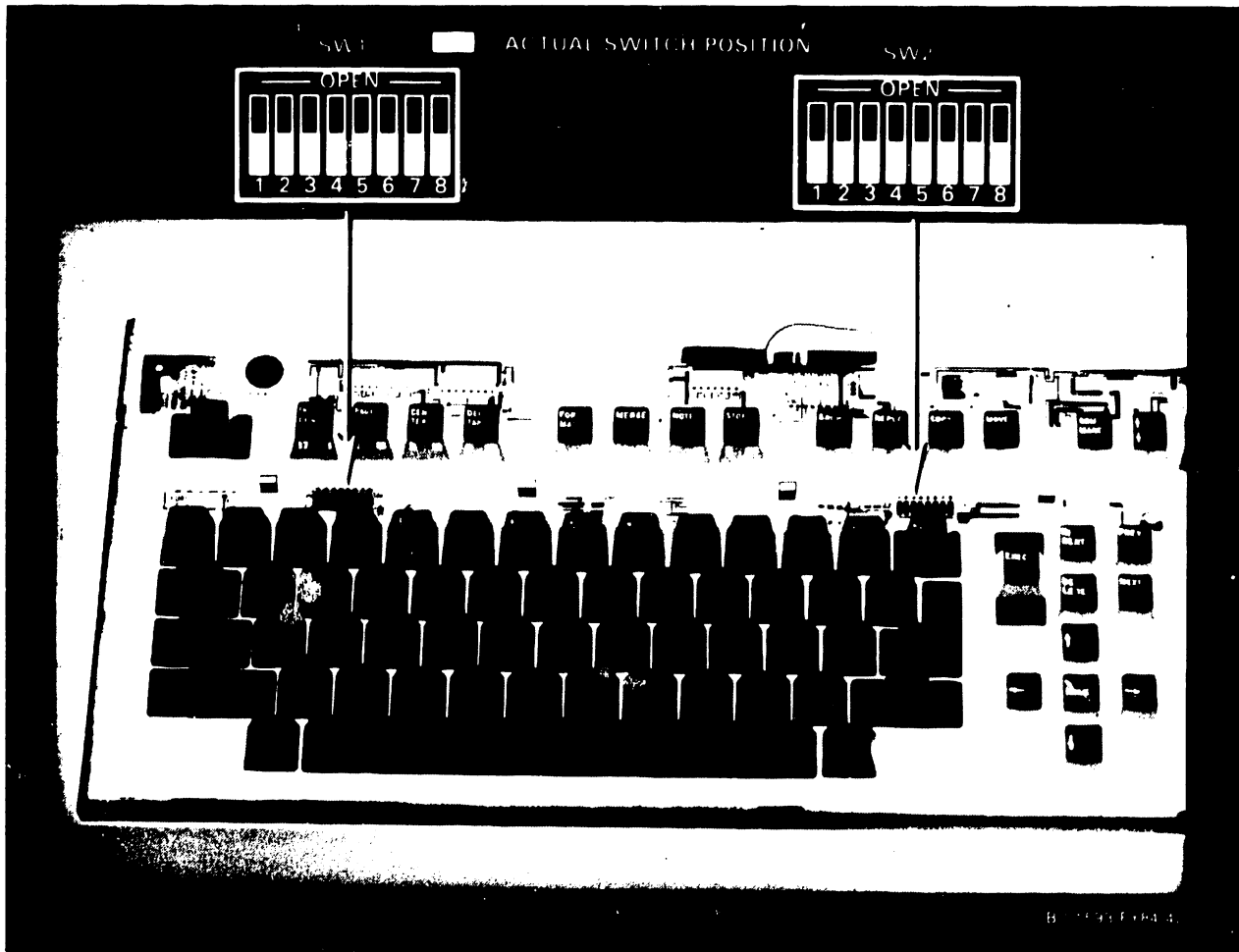


Figure 5-16. Keyboard Switch Settings

5.7 SWITCH SETTINGS (Continued)

5.7.2 KEYBOARD SWITCH SETTINGS

For example, switches SW1/SW2 must be set to hex 0000, that is, all switches set to the off position for use as a Qwerty: US Standard keyboard.



5.7 SWITCH SETTINGS (Continued)

5.7.2 KEYBOARD SWITCH SETTINGS

Set switches SW1/SW2 for other language options in accordance with Table 5-1.

Table 5-1. Universal Keyboard Options

KEYBOARD	SYMBOL	HEX		BINARY SWITCH			
		SWITCH					
Qwerty:US Standard		0000		0000	0000	0000	0000
Azerty	AZ	0001		0000	0000	0000	0001
Canadian English	CE	0002		0000	0000	0000	0010
Canadian French	CA	0003		0000	0000	0000	0011
German (Exp)	EGE	8004		1000	0000	0000	0100
Spanish Latin	SL	0005		0000	0000	0000	0101
Swedish (Exp)	ESW	8006		1000	0000	0000	0110
Swiss French	SF	0007		0000	0000	0000	0111
Swiss French(Exp)	ESF	8007		1000	0000	0000	0111
Swiss German	SG	0008		0000	0000	0000	1000
Swiss German(EXP)	ESG	8008		1000	0000	0000	1000
United Kingdom	UK	0009		0000	0000	0000	1001
Danish	DA	000A		0000	0000	0000	1010
Danish (Exp)	EDA	800A		1000	0000	0000	1010
Dutch (Exp)	ENL	800B		1000	0000	0000	1011
Finnish (Exp)	EFI	800C		1000	0000	0000	1100
Flemish	FL	000D		0000	0000	0000	1101
Italian	IT	000E		0000	0000	0000	1110
Norwegian (Exp)	ENO	800F		1000	0000	0000	1111
South African	SE	0010		0000	0000	0001	0000
Spanish/Catalan	SP	0011		0000	0000	0001	0001
Fnnsh./Cyrll.(EXP)	EFC	8012		1000	0000	0001	0010
Greek	GR	0013		0000	0000	0001	0011
Portuguese (Exp)	EPO	8014		1000	0000	0001	0100
Arabic (Exp)	EAR	8015		1000	0000	0001	0101
Cyrillic (Exp)	ECY	8017		1000	0000	0001	0111
Icelandic (Exp)	EIC	801C		1000	0000	0001	1100
Turkish (Exp)	ETU	8023		1000	0000	0010	0011
World Lang.	WL	0028		0000	0000	0010	1000
Katakana	KA	002C		0000	0000	0010	1100
Azerty/English	AE	002D		0000	0000	0010	1101
Dvorak	DV	002E		0000	0000	0010	1110

CHAPTER

6

SCHE-

MATICS

THE SCHEMATICS, WHEN AVAILABLE, ARE ON THE LAST FICHE IN THIS SET.

CHAPTER

7

IPB

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CHAPTER 7

ILLUSTRATED PARTS BREAKDOWN

This chapter contains illustrated parts breakdowns (IPBs) for the 4230/05 Workstation. The illustrations identify the part numbers of sub-assemblies referred to throughout the manual in the various maintenance procedures. Some sub-assemblies are further broken down to identify piece parts for replacement purposes as may be necessary.

7.1 LIST OF ILLUSTRATED PARTS BREAKDOWNS

<u>TITLE</u>	<u>FIGURE</u>	<u>TABLE</u>
Electronics Base Assembly	7-1	7-1
Monitor Assembly	7-2	7-2
Keyboard Assembly	7-3	7-3

7.2 CORPORATE END ITEM (CEI) NUMBERS

Corporate end item part numbers for the major units comprising the 4230/05 Workstation are listed below and should be used when ordering complete assemblies for replacement in the field.

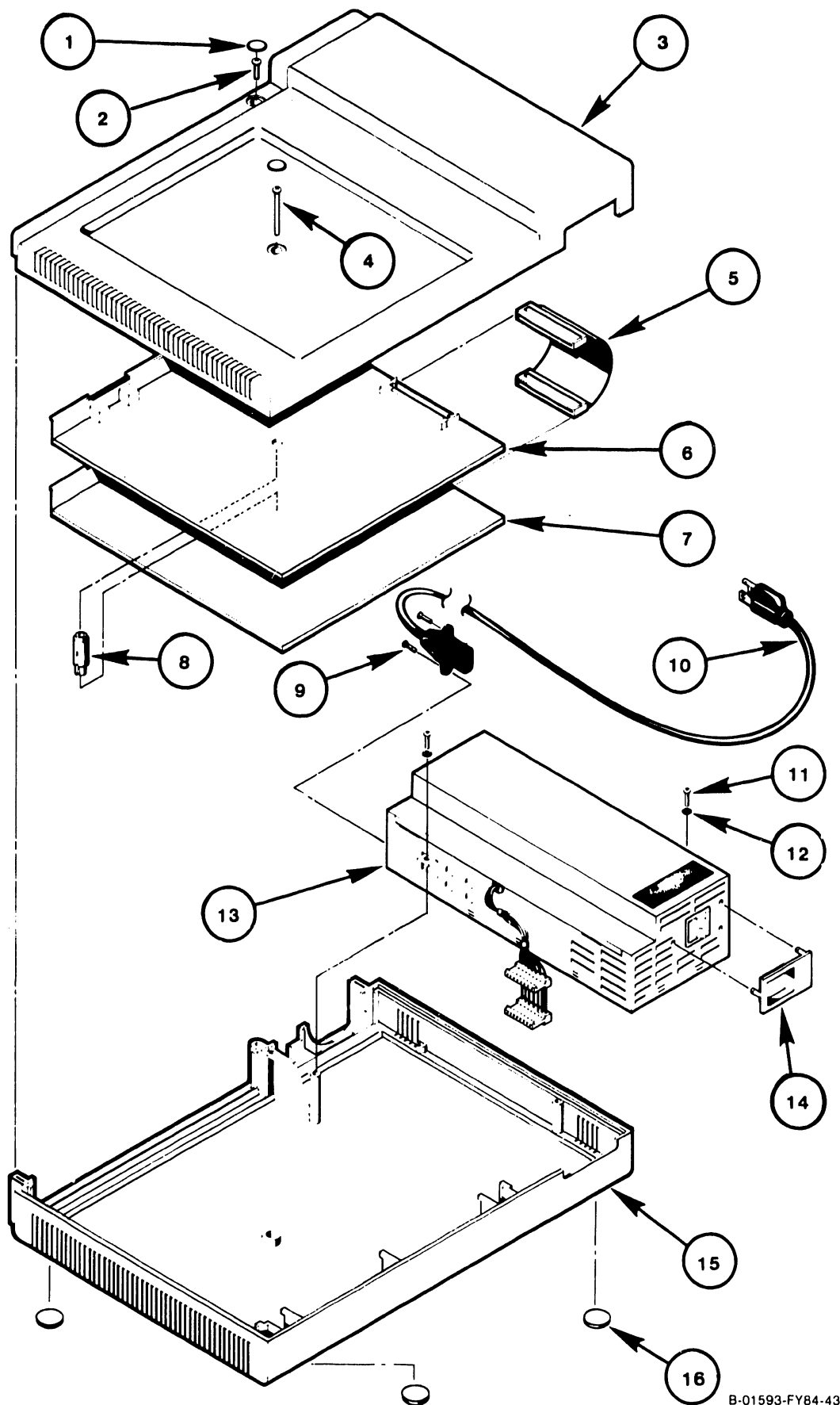
<u>DESCRIPTION</u>	<u>PART NUMBER</u>
4230 Electronics Base Assembly	187-7237
4205 Electronics Base Assembly	177-7265
4200-Series Monitor Assembly	279-0541*
4200-Series Keyboard Assembly	279-2042*
	279-2044* (Ex)

(* Denotes an RSL item.

Table 7-1. Electronics Base Assembly
(Refer to Figure 7-1)

<u>LOCATION</u>	<u>DESCRIPTION</u>	<u>PART NUMBER</u>
1	Decorative Hole Plugs	655-0293
2	Screw, #8-32 x 3/8, PH PHIL	650-4135
3	Top Cover	450-0917-XB
4	Screw, #8-32 x 2, PH PHIL	650-4643
5	I/O Interconnect Cable	220-3282*
6	4230 Workstation TC PCA	210-8298-A*
	Filler Panel (4205 & 4230 w/o TC)	451-3678
7	4230 Workstation Electronics PCA	210-8287-A*
	4205 Workstation Electronics PCA	210-8287-1*
8	Center Support, PCA Spacer	449-0674*
9	Screw, AC Power Cord Mounting	Part of Item 10
10	AC Power Cord (w/screws item 9)	420-2025
11	Screw, #8-32 x 1/4, PH PHIL	650-4080
12	Washer (used with item 11)	
13	Switching Power Supply	725-2749-11*
14	Switch Insert	449-0676-XC*
15	Base Bottom	450-0916-XC
16	Foot, Self-Adhesive	655-0286

(*) Denotes an RSL item.



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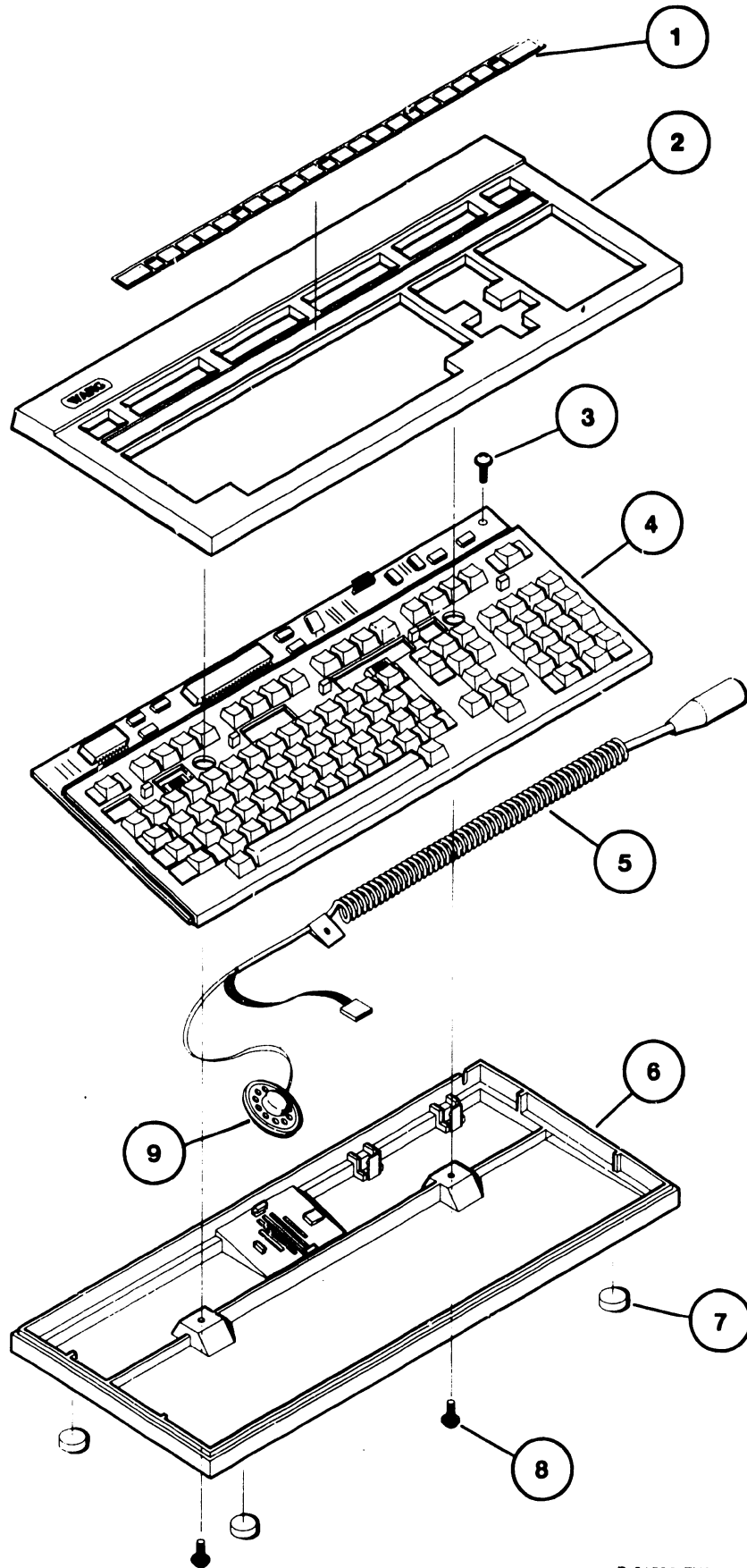
Figure 7-1. Electronics Base Assembly

Table 7-2. Keyboard Assembly
(Refer to Figure 7-2)

<u>LOCATION</u>	<u>DESCRIPTION</u>	<u>PART NUMBER</u>
	UNI/KBD-US (United States)	279-2042-US*
	UNI/KBD-UK (United Kingdom)	279-2042-UK*
	UNI/KBD-SL (Span.-Latin American)	279-2042-SL*
	UNI/KBD-AZ (AZERTY)	279-2042-AZ*
	UNI/KBD-GE (German Expanded)	279-2044-GE*
	(Arabic Expanded)	**
1	Function Strip	615-2059
2	Cover, Top (Non-Expanded)	449-0608
	Cover, Top (Expanded)	449-0611
3	Screw, 8-32 X 3/8 PAN HD PHIL	650-4120
	Locknut (use with item 3)	652-0029
4	Keyboard, Universal (US)	725-2738-US
	Keyboard, Universal (UK)	725-2738-UK
	Keyboard, Universal (SL)	725-2738-SL
	Keyboard, Universal (AZ)	725-2738-AZ
	Keyboard, Universal Exp. (GE)	725-2739-GE
5	Cable Assembly	220-0305
6	Base, Keyboard	449-0607
7	Foot, Self Adhesive	655-0286
	Foot, Self Adhesive	655-0291
8	Screw, 8-32 X 1/2 Pan Hd Phil	650-4160
9	Speaker, Round 2-in., 8 Ohm	320-0306

(*) Denotes an RSL item.

(**) The Arabic keyboard consists of the Expanded German keyboard (P/N 279-2044-GE) and the Arabic Key Top Kit (P/N 200-4102-ME).



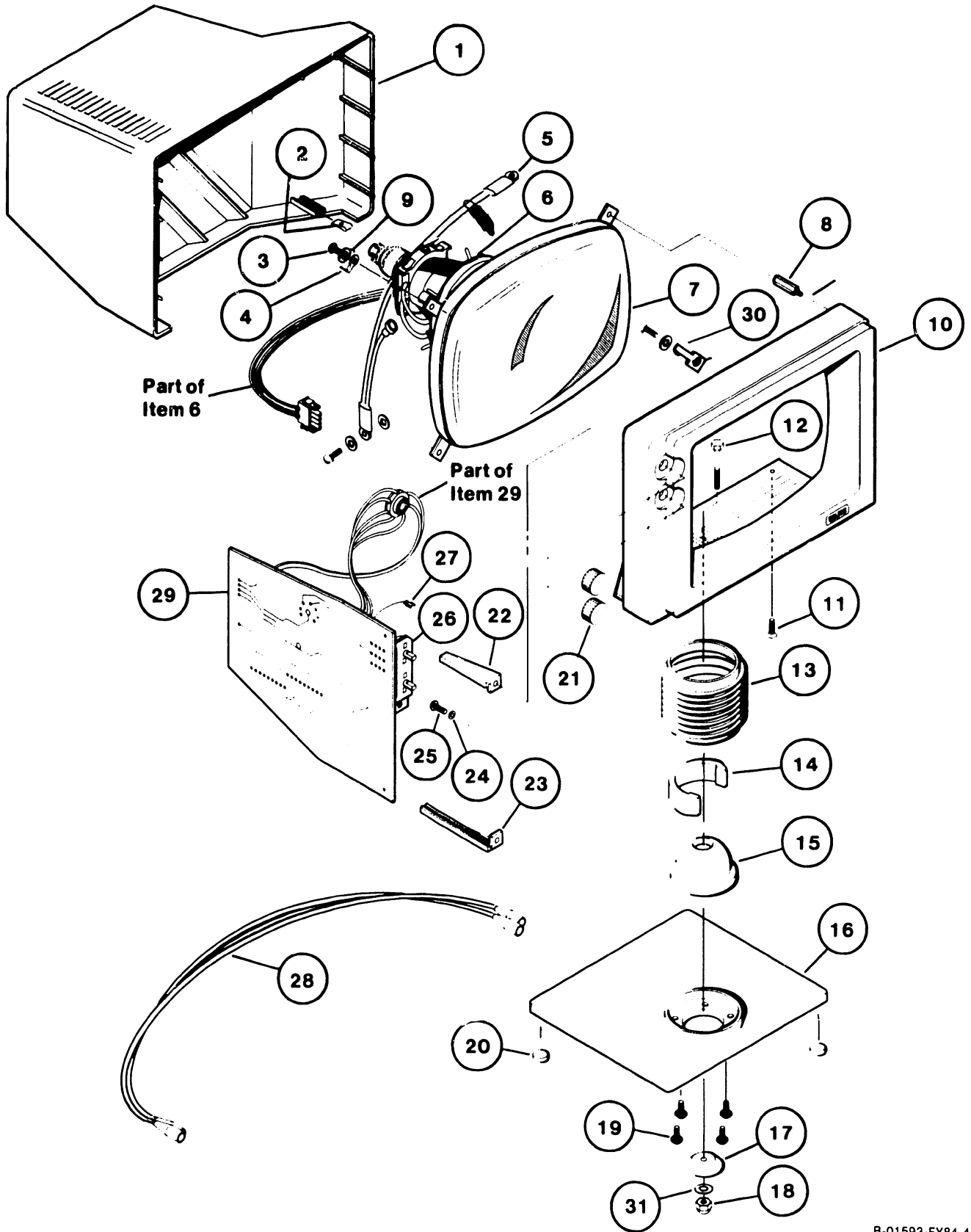
B-01593-FY84-44

Figure 7-2. Keyboard Assembly

Table 7-3. Monitor Assembly (279-0541)
(Refer to Figure 7-3)

<u>LOCATION</u>	<u>DESCRIPTION</u>	<u>PART NUMBER</u>
1	Cover, Monitor	449-0630
2	Fastener, #8-32 U-Type	651-0268
3	Screw, 10-32 X 1/2 Truss Hd Phil	650-6160
4	Terminal Lug, Spade	654-0125
5	Grounding Cable Assembly (requires item 30 for installation)	220-1964
6	Yoke Assy (Less Magnets)	270-3289
	Magnet, 11 Gauss	320-0126
	Magnet, 20 Gauss	320-0127
	Magnet, 15 Gauss	320-0128
7	Tube, C/R 12-in. (Less Yoke Assy)	340-0111
8	Standoff, 3/8 Hex X 1-5/8-in. Long	462-0610
9	Washer	653-6000
10	Bezel, Monitor	449-0631
11	Screw, 8-32 X 3/8 Phil Hd Flt	650-4121
12	Screw, 1/4-28 X 1-3/4 Hex	650-9077
13	Bellow, Sleeve	449-0635
14	Collar, Ball Joint	449-0626
15	Ball Joint	478-0805
16	Base, Monitor	449-0627
17	Cap Spring	449-0625
18	Stop Nut, 1/4-28	652-0064
19	Screw, 6-32 X 1/2 Pan Hd Phil	650-3160
20	Foot, 5/8 X 1/8 Self-Adhesive	655-0286
21	Knob	449-0596
22	Holder, PCB Upper	449-0629
23	Holder, PCB Lower	449-0628
24	Washer	653-4001
25	Screw, 8 X 1/2 Self Tap Pan Hd Phil	651-0052
26	Bracket (included with item 29)	451-4985
27	Wire and Lug Assy (included with item 29)	220-1263
28	Cable Assy, I/O	421-0002*
29	PCA, Monitor (early units)	210-3244*
	PCA, Monitor (later units)	210-8344*
30	Clip, Spring	452-2737
31	Washer	653-6006
32	Spring (included With item 5)	465-1637

(*) Denotes an RSL item.



B-01593-FY84-45

Figure 7-3. Monitor Assembly

CHAPTER

8

**TROUBLE-
SHOOTING**

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8.4	Pin Assignments of Rear Panel Connectors	8-10
8.5	Switching Power Supply Overcurrent Trip	8-12

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8-4	RS-232C Connector Pin Assignments	8-11

CHAPTER 8

TROUBLESHOOTING

Figure 8-1 is a troubleshooting flowchart for the single-board 4230 Workstation without TC, the single-board 4205 Workstation and the 4230/05 Arabic workstations. Figure 8-2 is the TC troubleshooting flowchart. Use the flowcharts to isolate a field replaceable unit relating to an observed symptom.

During the course of investigation, alignments or other procedures may be referred to as a means of verification or isolation. Following the flowchart through on these points will prevent replacement of field replaceable units where they only require alignment or some other adjustment.

Remember, no procedure can list every problem that could occur in even a very simple device. Use the troubleshooting flowchart as a guide in the systematic investigation, diagnosis and repair of failures in the 4230/05 Workstation.

8.1 GENERAL TROUBLESHOOTING CHECKS

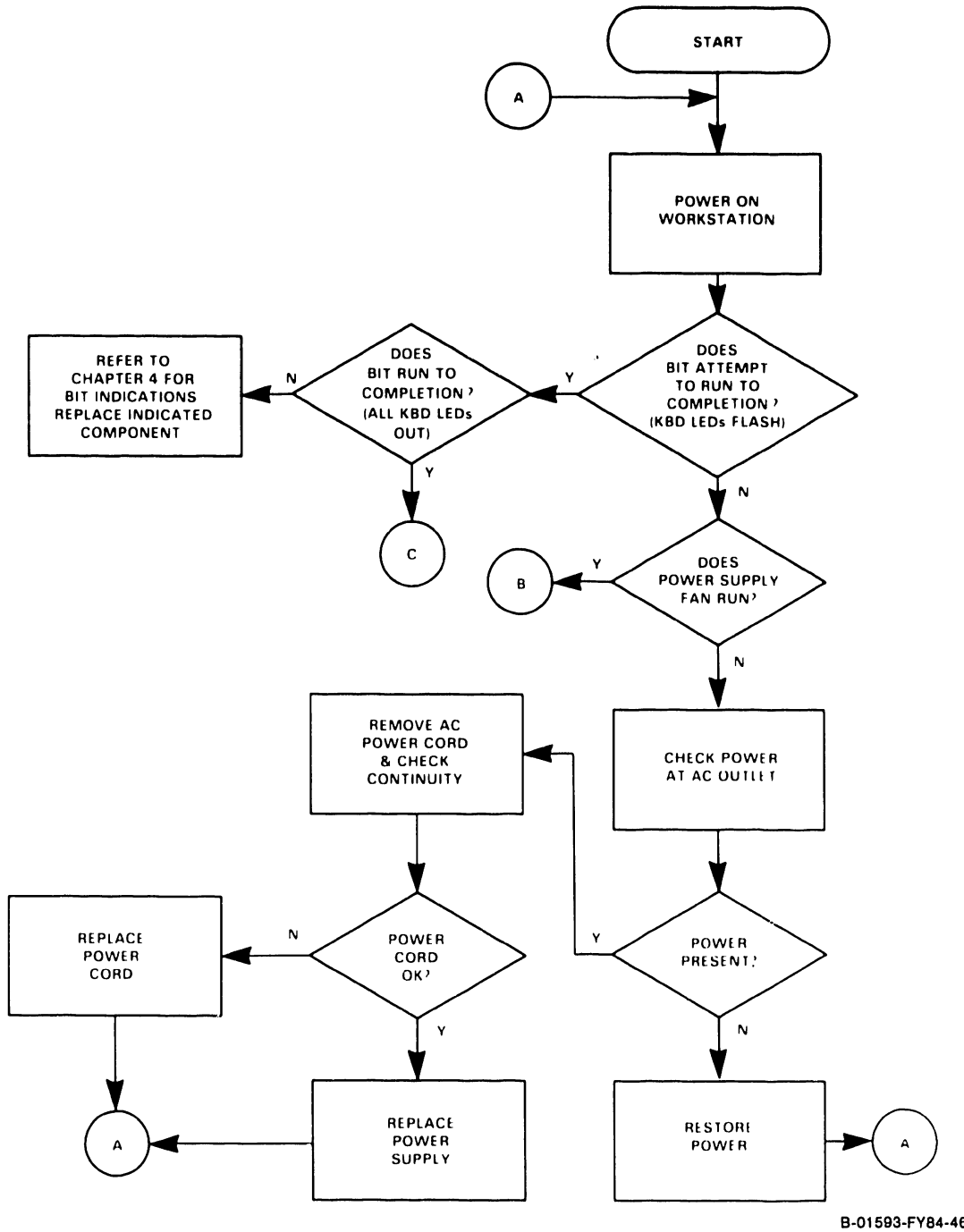
Before proceeding with the more in-depth troubleshooting outlined in other sections of this chapter, make a careful visual inspection of the workstation and check the items listed below.

- Is the ac power cord securely plugged into its power outlet?

- Are the VIDEO, PWR, and KYBD cables between the Monitor, Keyboard and Electronics Base securely connected to their respective connectors?

8.1 GENERAL TROUBLESHOOTING CHECKS (Continued)

Is the DATA LINK dual-coaxial cable from the workstation to the host CPU securely connected at both units?



B-01593-FY84-46

Figure 8-1. 4230/05 WS Troubleshooting Flowchart (Sheet 1 of 4)

8.1 GENERAL TROUBLESHOOTING CHECKS (Continued)

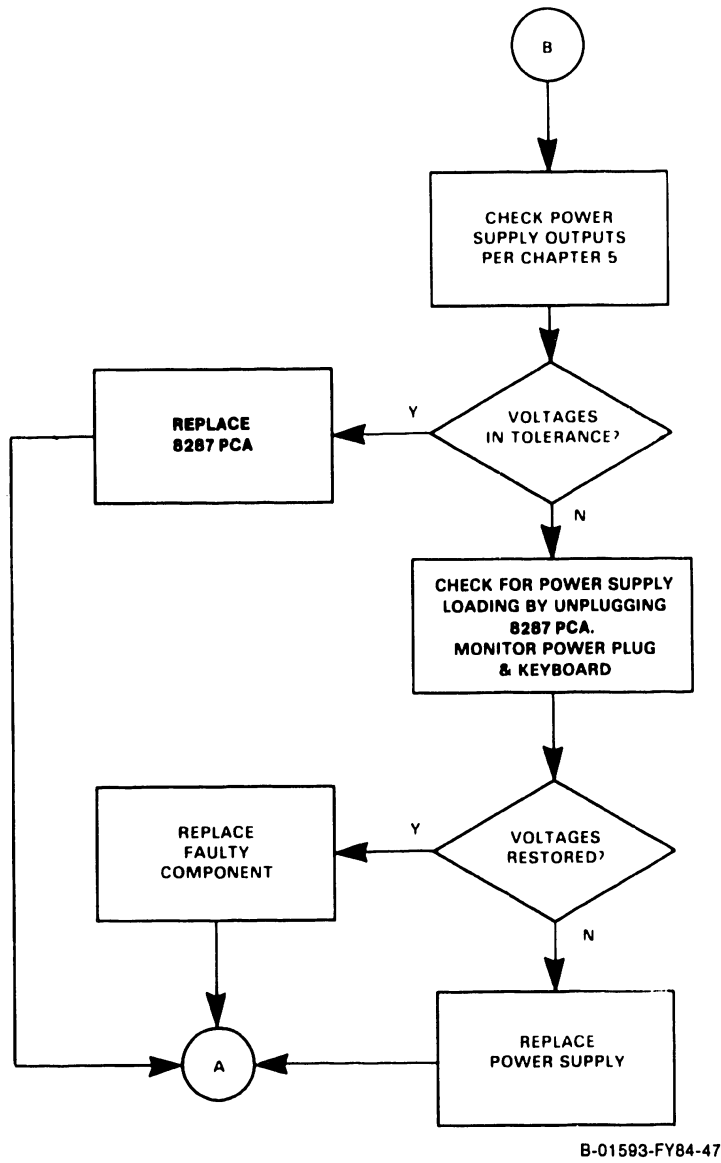
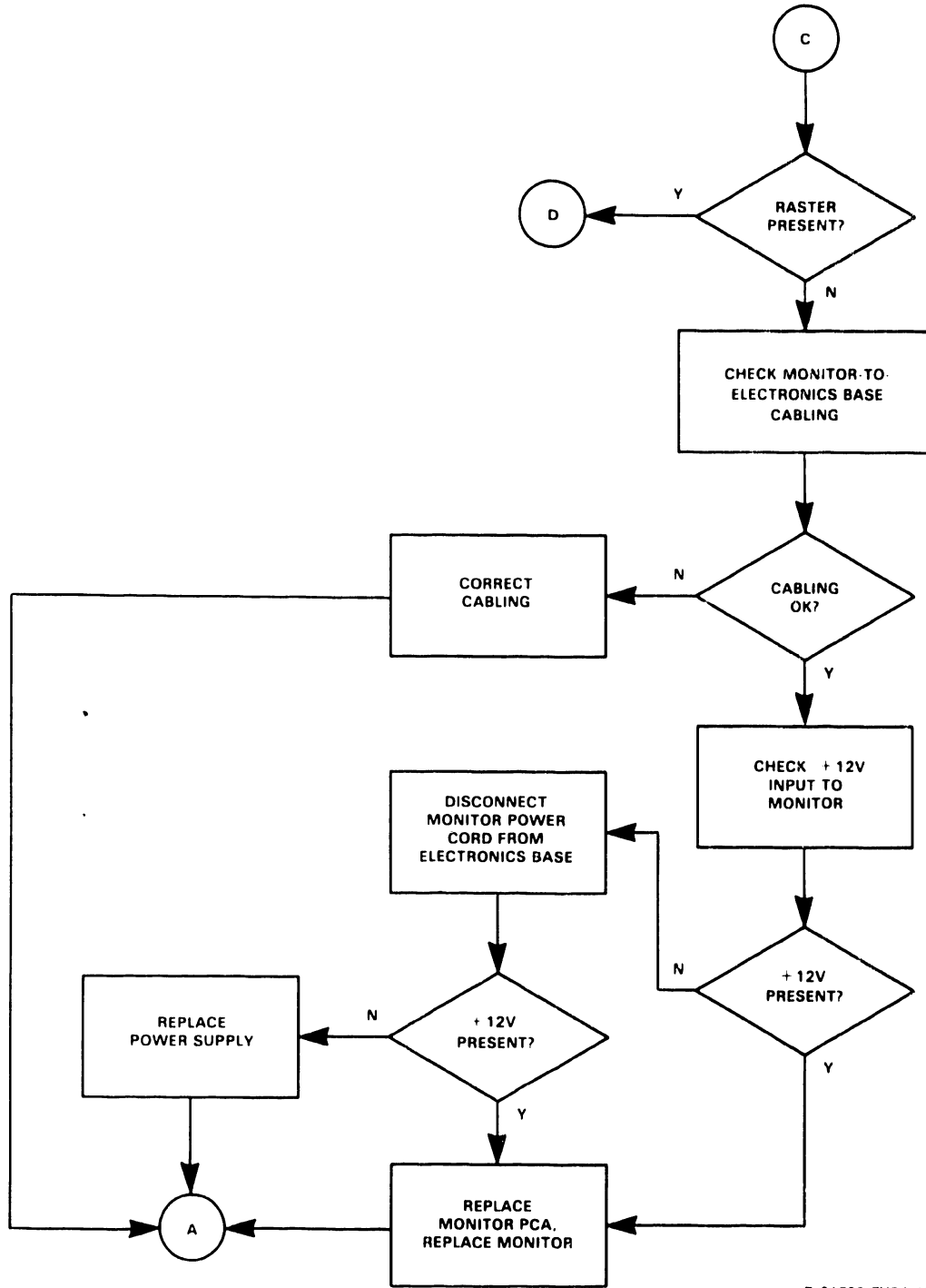


Figure 8-1. 4230/05 WS Troubleshooting Flowchart
(Sheet 2 of 4)

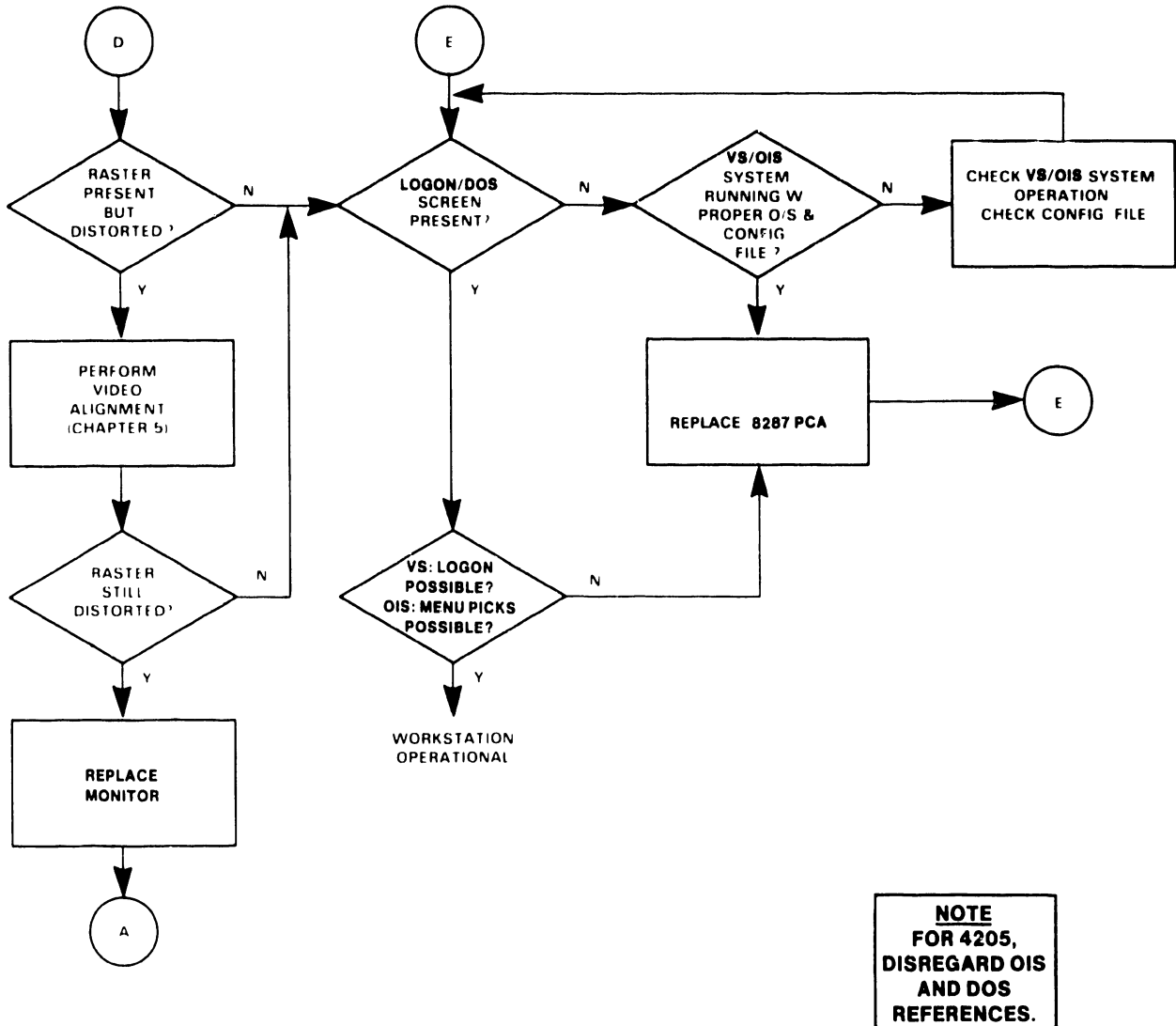
8.1 GENERAL TROUBLESHOOTING CHECKS (Continued)



B-01593-FY84-48

Figure 8-1. 4230/05 WS Troubleshooting Flowchart
(Sheet 3 of 4)

8.1 GENERAL TROUBLESHOOTING CHECKS (Continued)



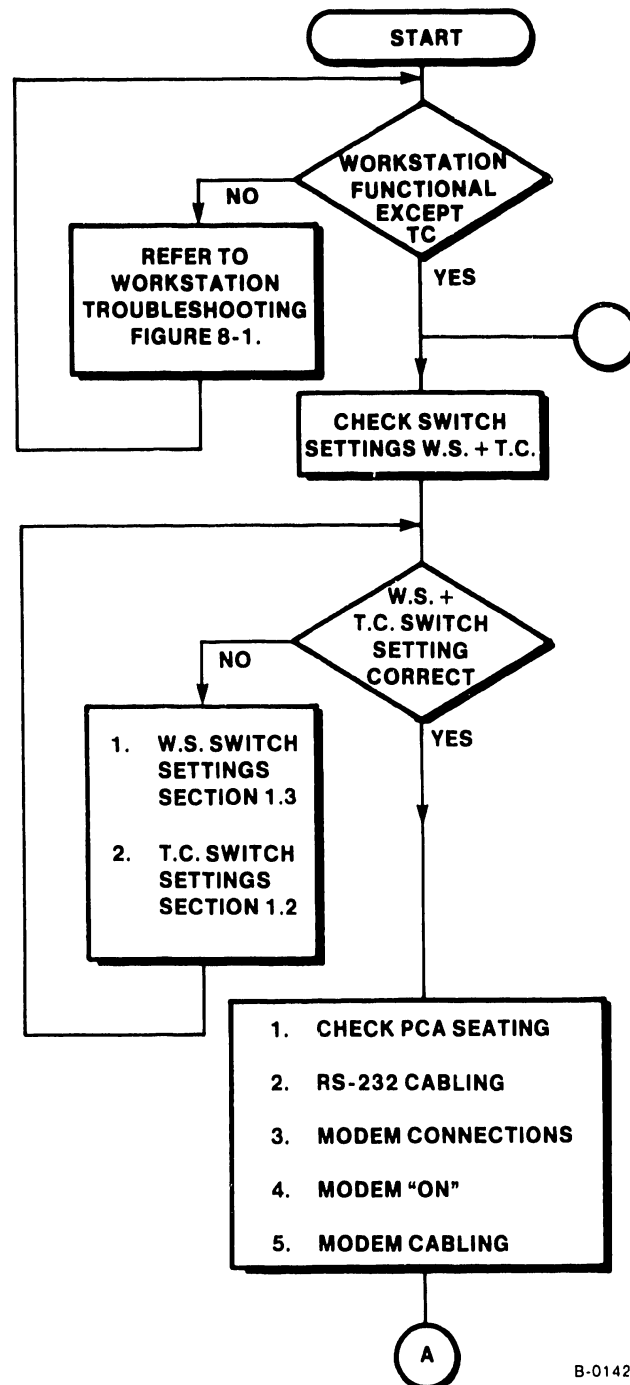
NOTE
FOR 4205,
DISREGARD OIS
AND DOS
REFERENCES.

B-01593-FY84-49

Figure 8-1. 4230/05 WS Troubleshooting Flowchart
(Sheet 4 of 4)

8.2 TELECOMMUNICATIONS TROUBLESHOOTING

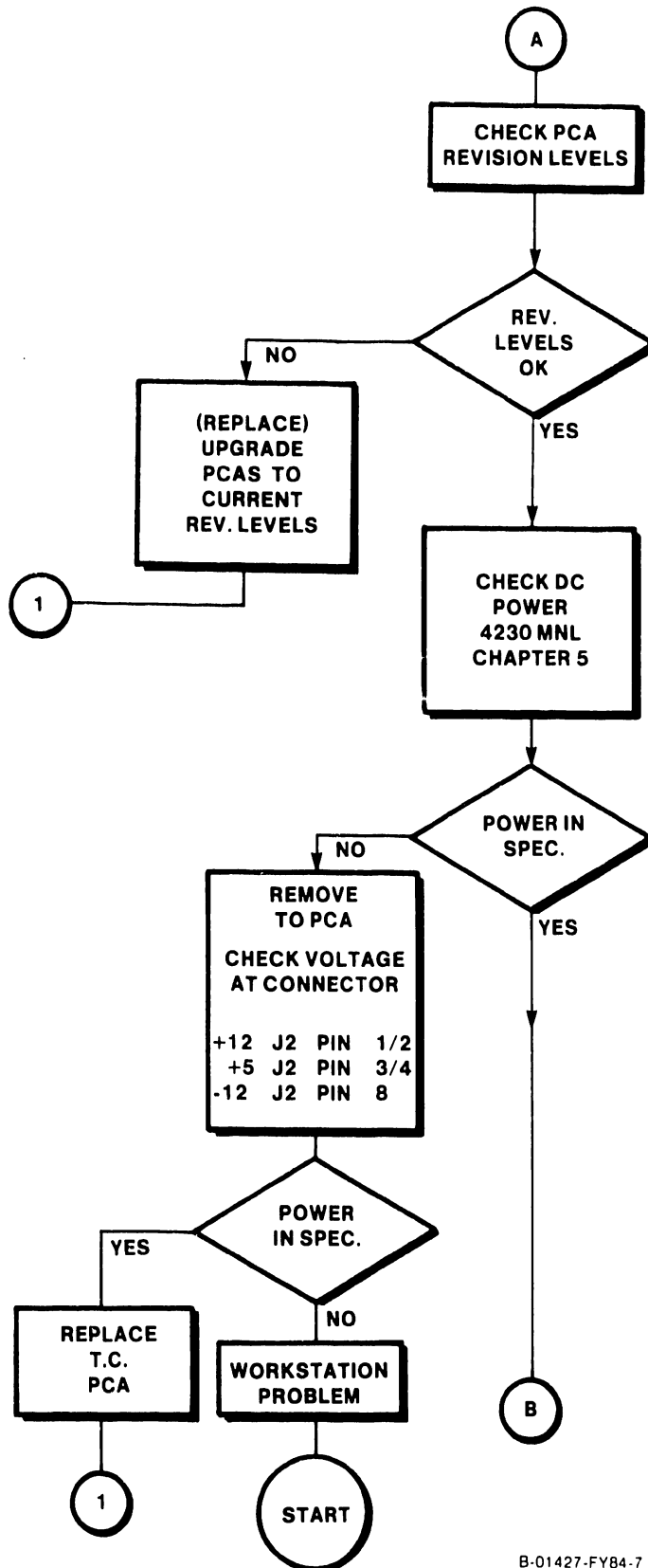
The troubleshooting flowchart provided on the next three pages is intended to aid in the systematic investigation, diagnosis, and repair of the 4230 Telecommunications option.



B-01427-FY84-6

Figure 8-2. 4230 WS TC Troubleshooting Flowchart
(Sheet 1 of 3)

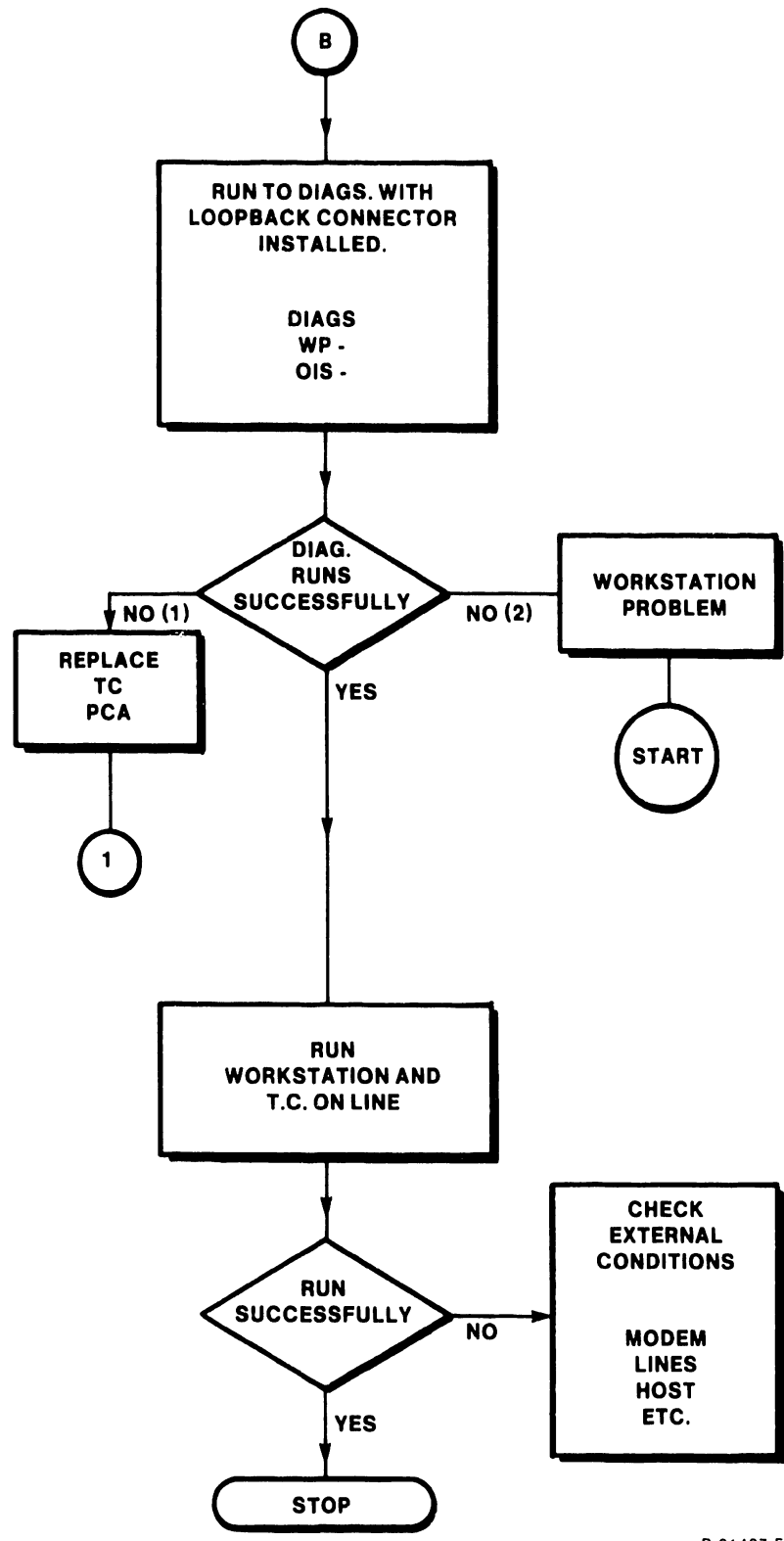
8.2 TELECOMMUNICATIONS TROUBLESHOOTING (Continued)



B-01427-FY84-7

Figure 8-2. 4230 WS TC Troubleshooting Flowchart (Sheet 2 of 3)

8.2 TELECOMMUNICATIONS TROUBLESHOOTING (Continued)



B-01427-FY84-5

Figure 8-2. 4230 WS TC Troubleshooting Flowchart
(Sheet 3 of 3)

8.3 MONITOR QUICK CHECKS

The VS or OIS diagnostic test operating system (DTOS) contains two video display patterns which are useful for quick evaluation of the Monitor's performance. These are the inverse video display and the circular alignment pattern.

Inverse Video Display Pattern

Select the inverse video display pattern of the DTOS Monitor alignment routine. All pixels on the CRT will be active (lit) except for those which display the words 'INVERSE VIDEO.' This display is useful in determining the condition of the high voltage circuits of the Monitor. Typical symptoms which may be observed with this full display are given below.

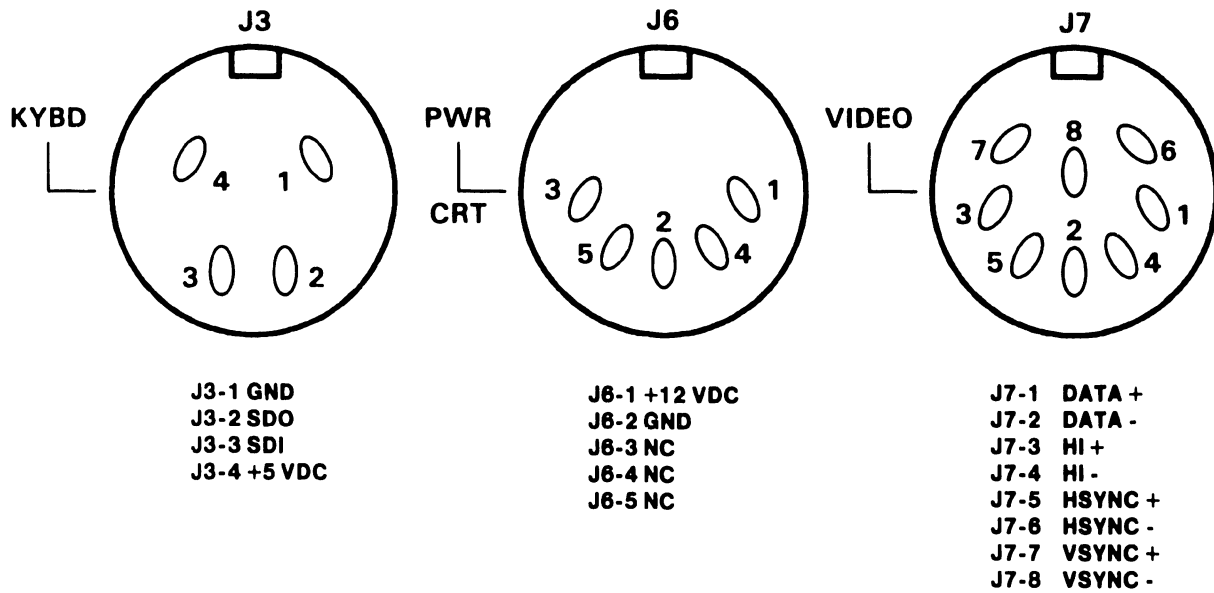
- Blooming: Indicates possible failure of high voltage circuitry to maintain adequate current for full illumination of CRT phosphors.
- Noise or Breakup: Indicates possible high voltage arcing or other source of interference.

Circular Alignment Pattern

Select the circular alignment pattern of the DTOS Monitor alignment routine. Five circles of equal size will be displayed on the CRT. The circles are a good visual check of the linearity of the CRT display. If the circles are out of round or egg-shaped, the Monitor is in need of alignment. Refer to the alignment procedure in Chapter 5 of this manual.

8.4 PIN ASSIGNMENTS OF REAR PANEL CONNECTORS

Figures 8-2 and 8-3 illustrate some of the key rear panel connectors of the Electronics Base, each of their pins and the signals associated with those pins.



CONNECTORS VIEWED FROM REAR OF ELECTRONICS BASE.

B-01593-FY84-53

Figure 8-2. PWR, VIDEO and KB Connector
Pin Assignments

8.4 PIN ASSIGNMENTS OF REAR PANEL CONNECTORS (Continued)

<u>PIN</u>	<u>EIA</u>	<u>CCITT</u>	<u>SIGNAL DESCRIPTION</u>	<u>SOURCE</u>
1	AA	101	Protective Ground	
2	BA	103	Transmitted Data	DTE
3	BB	104	Received Data	DCE
4	CA	105	Request to Send	DTE
5	CB	106	Clear to Send	DCE
6	CC	107	Data Set Ready	DCE
7	AB	102	Signal Ground	
8	CF	109	Carrier Detect	DCE
9	--	---	Reserved for Data Set testing	
10	--	---	Reserved for Data Set testing	
11	SCA	120	Secondary Request to Send	SCA
12	SCF	122	Secondary Carrier Detect	DCE
13	SCB	121	Secondary Clear to Send	DCE
14	SBA	118	Secondary Transmitted Data	DTE
15	DB	115	Transmit Clock	DCE
16	SBB	119	Secondary Received Data	DCE
17	DD	115	Receive Clock	DCE
18			Not Assigned	
19	SCA	120	Secondary Request to Send	DTE
20	CD	108.2	Data Terminal Ready	DTE
21	CG	110	Signal Quality Detector	DCE
22	CE	125	Ring Indicator	DCE
23	CH/CI	111/112	Data Signaling Rate Selector	DTE/DCE
24	DA	113	Transmit Clock	DTE
25			Unassigned	

Figure 8-3. RS-232C Connector Pin Assignments

8.5 SWITCHING POWER SUPPLY OVERCURRENT TRIP

The switching power supply senses overcurrent conditions in the workstation and responds by shutting itself down momentarily and then recycling itself back on. If the overcurrent condition still exists, the cycle is repeated. The result is a distinctive, repetitive clicking sound which emanates from the power supply in the event of a hard short in the workstation.

In the event of a condition such as this, check for shorts across the +5 and +12 Vdc lines in the workstation. Also, be sure that the power supply plug has been connected properly to the workstation PCAs. The yellow wire on the molex connector from the power supply must be connected to the PCA connector pin closest to the front of the workstation.

CHAPTER

6

SCHE-

MATICS

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CHAPTER 6	SCHEMATICS	<u>Page</u>
6.1	Schematic Diagrams	6-1

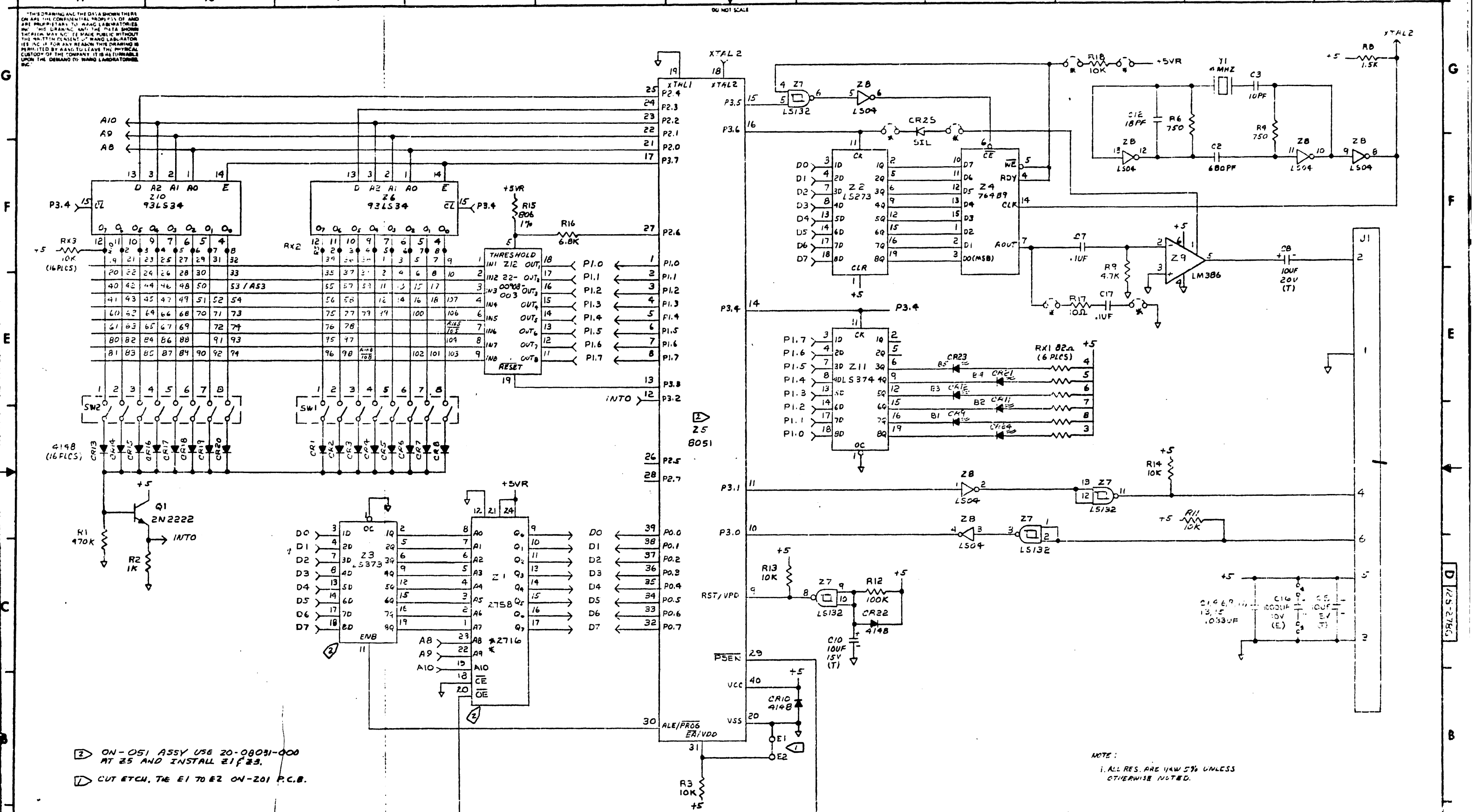
6.1 SCHEMATIC DIAGRAMS

Schematic diagrams for the component parts of the 4230/05 Workstations are included in this chapter of the manual. The schematics reflect the latest revisions at the time of printing.

The following is a list of the schematics contained in this chapter, the titles, drawing numbers and revisions at time of printing.

<u>TITLE</u>	<u>DWG. NO.</u>	<u>REV.</u>	<u>COMMENTS</u>
Monitor PCA	210-8244	11	Common, Early Units
WS Electronics PCA	210-8287	4	Common
Arabic WS Elec. PCA	210-8287-3	0	Common
Monitor PCA	210-8344	2	Common, Later Units
Keyboard PCA	725-2786	1	Common
TC PCA	210-8298	0	Optional

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② ON-051 ASSY USE 20-08031-000 AT Z5 AND INSTALL Z1F23.
 ① CUT ETCH, THE E1 TO E2 ON-201 P.C.B.

NOTE:
 1. ALL RES. ARE 1/4W 5% UNLESS OTHERWISE NOTED.

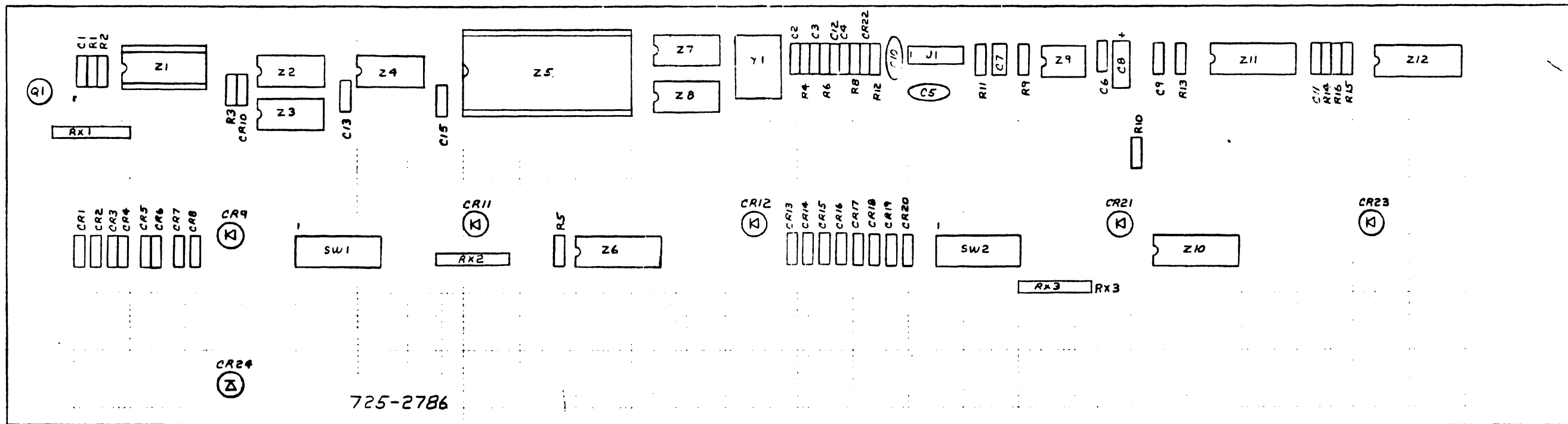
REV	DATE	BY	DESCRIPTION
0	1-18-83
1
2

* ADD JUMPERS + COMPONENTS PER ECO# 26683
 ** CHANGE Z1 FROM 2758 TO 2716 PER ECO# 26683

WANG PART NO.	DRAWING NO.	DESCRIPTION	BY	DATE	APPROVED BY	DATE
WANG LABORATORIES, INC. LOWELL, MASS.			DIVN 4 ENGRY. DESKTOP M ENGR			
MATERIAL MODIF. NO. SEE ENGRG. SPECIFICATIONS			TITLE KEYBOARD SCHM.			
FINISH TD. EN. AS NOTED XXX = 005 ANG. = 11.25° FINISH			SCALE 1:1			

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DO NOT SCALE



COMPONENT	TYPE	W.L. PART NO.
Z1	2716	377-0398
Z2	74LS273	376-0302
Z3	74LS373	376-0310
Z4	76489	376-0586
Z5	8051	377-1000
Z6,10	93LS34	
Z7	74LS132	376-0473
Z8	74LS04	376-0180
Z9	LM386	376-0585
Z11	74LS374	376-0286
Z12	908	377-0467
R1	470Ω 1/4W 5%	330-5048
R2	1K 1/4W 5%	330-3011
R3,5,10,11,13,14,18	10K 1/4W 5%	330-4011
R4,6	750Ω 1/4W 5%	330-2076
R8	1.5K 1/4W 5%	330-3016
R9	4.7K 1/4W 5%	330-3048
R12	100K 1/4W 5%	330-5011
R15	806Ω 1/4W 1%	333-0221
R16	6.8K 1/4W 5%	330-3069
Rx1	82Ω SIP	333-0850
Rx2,3	10K SIP	333-0827
R17	10Ω 1/4W 5%	300-1011
C1,4,6,9,11,13,15	.033UF 400V	300-2412
C2	680PF	300-1682

COMPONENT	TYPE	W.L. PART NO.
C3	10PF 500V	300-1010
C5,10	10UF 35V (T)	300-4032
C7	.1UF 100V	300-1923
C8	10UF 20V (T)	300-4065
C12	180PF 50V	300-1969
C16	1000UF 10V (T)	300-3146
CR1-8,10,13-20,22	1N4148	380-1014
CR9,11,12,21,23	LAMP, RED	370-0031
CR9,11,12,21,23	SPACER RD	462-0638
CR24	LED, RED	370-0064
CR25	SIL	380-1001
C17	.1UF 12V	300-1901
J1	6 PIN CONN	726-2454
SW1,2	8 POS DIP	325-1503
Y1	4.00MHZ	321-0039
Z1	24 PIN SKT	376-9003
Z5	40 PIN SKT	376-9011
Q1	2N2222	375-1005

725-2786

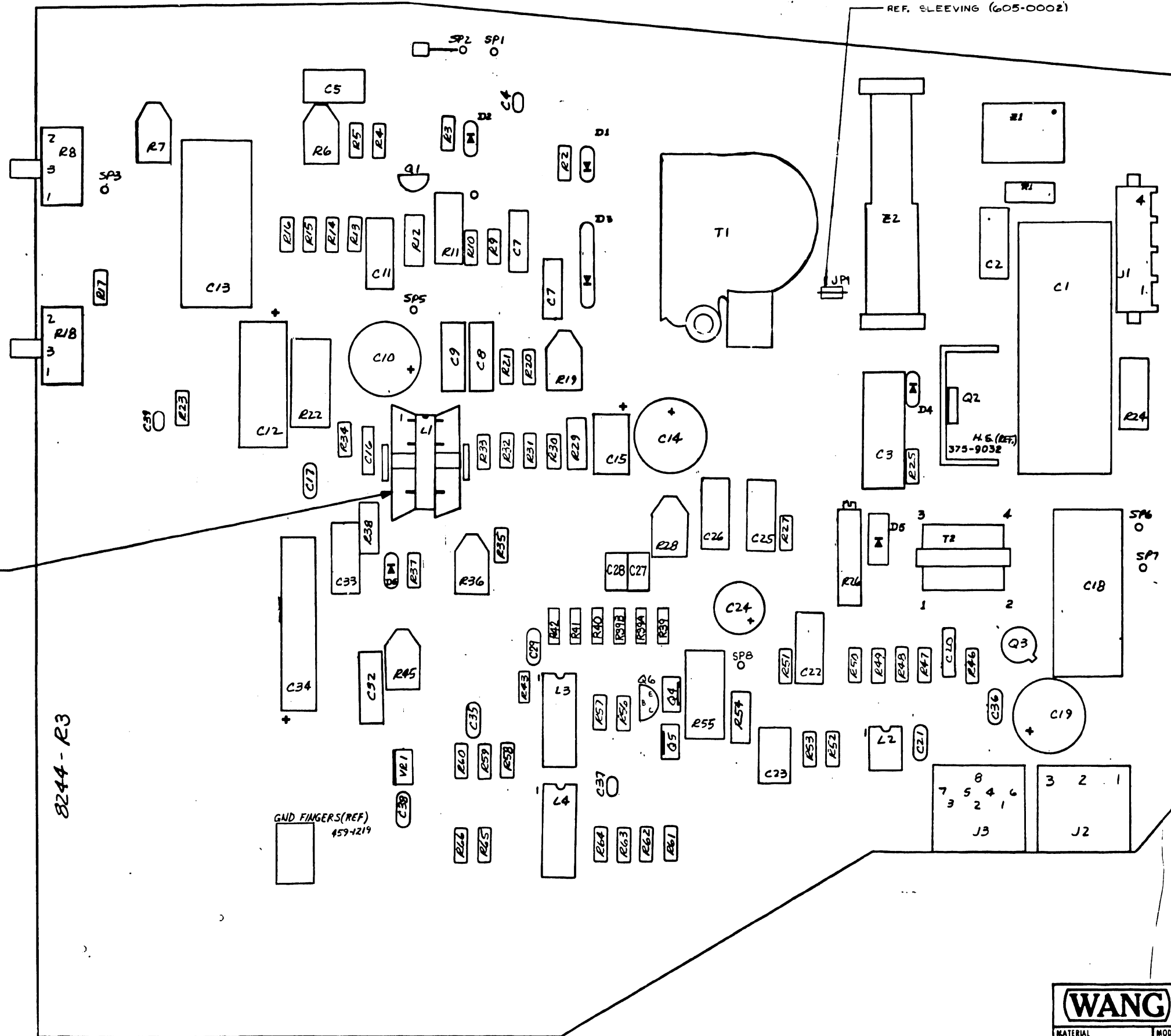
REVISION
NO. DATE
1 SEE SHT 1

WANG PART NO	DRAWING NO	DESCRIPTION	BY	DATE	APPROVED BY	DATE
			DWN	9/83	E ENGR	
			CHK		M ENGR	3/9/84
					MFG ENGR	
MATERIAL	MODEL NO R067 FBC	TITLE	KEYBOARD PC ASSY			
FINISH	TOL EX AS NOTED XX = 010 FRAC = 1/64 XXX = 005 ANG = 1°30' MIN MAX V	725-2786	D	725-2786	2	
SCALE	1:1	WANG PART NUMBER	725-2786	DRAWING NUMBER	2	REV

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DO NOT SCALE

REF. SLEEVING (605-0002)



VERTICAL HEAT SINK
376-9066
REF.

8244-R3

GND FINGERS(REF)
459-4219

NO.	REVISION
	SEE SH1.3

(WANG) LABORATORIES, INC. LOWELL, MASS. U.S.A.		BY	DATE	APPROVED BY	DATE
		DWN EM	10/13/62	E ENGR	
MATERIAL		MODEL NO.	TITLE		
		PC7A PBC	MONITOR BOARD		
FINISH		SEE ENGR SPECIFICATIONS			
		TOL ER AS NOTED		210-8244	D
		81 ±	FRAC ±	375-9032	12
		82 ±	ANG ±	WANG PART NUMBER	SIZE
		83 ±	FINISH	DRAWING NUMBER	REV
		SCALE	SH1.3		

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DO NOT SCALE

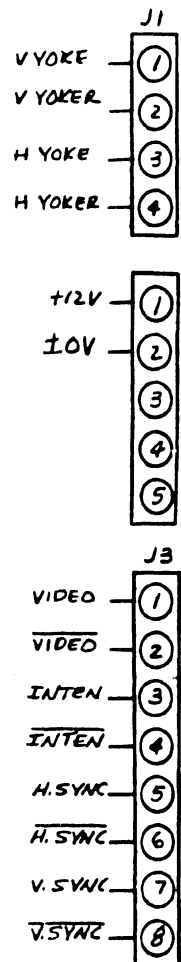
COMPONENT	TYPE	W.L. PART NO.
R1	1K 1/4W 5%	331-3011
R2,37	100K 1/4W 5%	330-5019
R3	100K 1/4W 5%	330-5011
R4,30	47K 1/4W 5%	330-4048
R5	330K 1/4W 5%	330-2034
R6	10K POT 700	336-1067
R7	5K POT 700	336-1068
R8	250K 2W POT	336-0048
R9,10	1.8MEG 1/4W 5%	330-6019
R11	1.5MEG 1W 10%	332-6015
R12	47K 1/2W 10%	331-4047
R13	3.3K 1/4W 5%	330-3034
R14	8.2K 1/4W 5%	330-3083
R15,41	470K 1/4W 5%	330-2048
R16	18K 1/4W 5%	330-4019
R17,56,57	22K 1/4W 5%	330-1023
R18	1K 2W POT	336-0049
R19	50K POT 700	336-1066
R20,27	22K 1/4W 5%	330-4023
R21	390K 1/4W 5%	330-5040
R22	56K 2W 10%	337-1056
R23	680K 1/4W 5%	330-2069
R24	33K 1W 10%	332-1033
R25,46	47K 1/4W 5%	330-1048
R26	2K TRIM POT	336-0036
R28	100K POT 700	336-1069
R29,38	2.2K 1/2W 10%	331-0022
R31	27K 1/4W 5%	330-4028
R32	56K 1/4W 5%	330-3057
R33	2.2K 1/4W 5%	330-3023
R34	220K 1/4W 5%	330-5023
R35	68K 1/4W 5%	330-4069
R36,45	100K POT 700	336-1065
R39	200K 1/4W 5%	330-2020
R39A,39B	60K 1/4W 5%	330-1069
R40	130K 1/4W 5%	330-2014
R42,43	270K 1/4W 5%	330-2028
R47	820K 1/4W 5%	330-2083
R48	150K 1/4W 5%	330-2016
R49	10.5K 1/2W 1%	333-0112
R50	24K 1/4W 5%	330-3025
R51	1.8K 1/4W 5%	330-3019
R52	33K 1/4W 5%	330-4034

COMPONENT	TYPE	W.L. PART NO.
R53	47K 1/4W 5%	330-3048
R54	270K 1/2W 10%	331-2027
R55	820K 2W 5%	337-2083
R58-62,65,66	1K 1/4W 5%	330-3011
R61-64	100K 1/4W 5%	330-2011
C1	4uf 200V POLY	300-2413
C2	.001uf 500V MKR	300-5038
C3	.008uf 400V POLY	300-2076
C4	.05uf 500V	300-1946
C5	.047uf 50V	300-1962
C6,7	.02uf 140V	300-1916
C8,9,22,25,32,33	.1uf 100V MTLBU	300-2217
C10,14	100uf 35V(E)	300-3020
C11	.015uf 100V(M)	300-2115
C12	50uf 50V(E)	300-3010
C13,18	.47uf 100V (M)	300-2247
C15	10uf 16V (E)	300-3006
C16	15uf 500V	300-1015
C17,21,23,35,36,38	.1uf 50V H.F.	300-1930
C19	220uf 25V(E)	300-3031
C20	.0068uf 100V	300-1911
C23	.0068uf POLY	300-2067
C24	47uf 100V(E)	300-3143
C26	.022uf 100(M)	300-2122
C27,28	180uf 500V MKR	300-5001
C34	100uf 50V(E)	300-3052
C37,39	1uf 50V	300-1931
VR1	4A7805	374-0001
D1,2,4	351F4	380-3010
D3	VG1X	380-3009
D5	351F2	380-3012
D6	1N4004	380-4000

COMPONENT	TYPE	W.L. PART NO.
Q1	T50MW 450V	375-1143
Q2	BV407	375-1057
Q3	2N3725	375-1027
Q4,5	MPSU04	375-1056
Q6	MPS6514	375-1062
T1	FLY BACK	410-0238
T2	XFMR DRIVER	410-1006
Z1	ADJUSTABLE	320-0107
Z2	WIDTH	320-0053
J1	4PIN CONN.	350-0215
J2	5PIN CONN.	350-0539
J3	8PIN CONN.	350-0542
JPI	18 GA BUS WIRE	600-9018
REF.	SLEEVING	605-0002
REF.	POT BRACKET	451-4985 XB
REF.	CRT GND STRIP	458-1219
REF.	HEAT SHRINK .1FT	605-0123
REF.	HEAT SHRINK .1FT	605-0143
REF.	ZOGA WIRE .1FT	600-9027
REF.	BRIDTUBULAR 5/32 ID .7083FT	420-0091
REF.	FLAT BRAID 1/2 WIDE .9166 FT	420-0074

I.C. LOCATION	TYPE	W.L. PART NO.
L1	TDA1170	376-0552
L2	MC1391	376-0578
L3	74500	376-0228
L4	266532	376-0471

MNEMONIC	COORD.
H.SYNC	1E11
H.SYNC	1E11
H YOKE	1C4
H YOKER	1C4
INTEN	1E11
INTEN	1E11
VIDEO	1F11
VIDEO	1E11
V.SYNC	1D11
V.SYNC	1D11
V YOKE	1E4
VYOKER	1E4



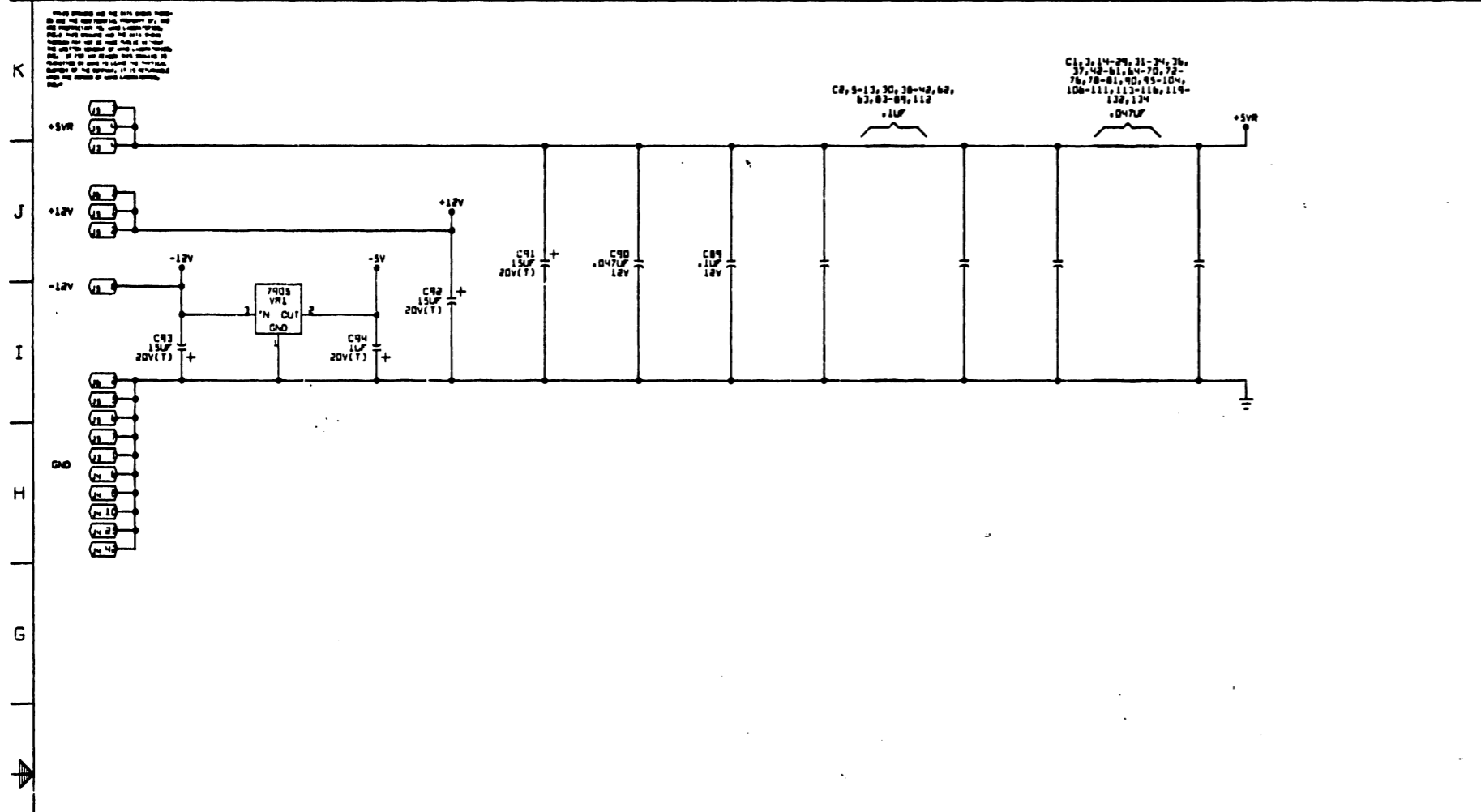
NOTE: 1. ALL RES ARE 1/4W 5% UNLESS OTHERWISE SPECIFIED.

E-REV
4

REV	DATE	BY	DESCRIPTION
1	10/27/82	KMT	ORIGINATED PER DWG # 8244-01-EL
2	11-9-82	DSS	REVISION PER ECO # 25274
3	12-9-82	KMT	REVISION PER ECO # 25442
4	1-11-83	KMT	REVISION PER ECO # 25489
5	2-11-83	RBP	REVISION PER ECO # 26154
6	3-11-83	KMT	REVISION PER ECO # 26858
7	4-11-83	T.S.	REVISION PER ECO # 27512
8	5-3-83	RBP	REVISION PER ECO # 27378
9	5-17-83	KMT	REVISION PER ECO # 28009
10	6-23-83	Emu	REVISION PER ECO # 29161
11	7-10-83	KMT	REVISION PER ECO # 29161
12	8-11-83	CAM	REVISION PER ECO # 29221

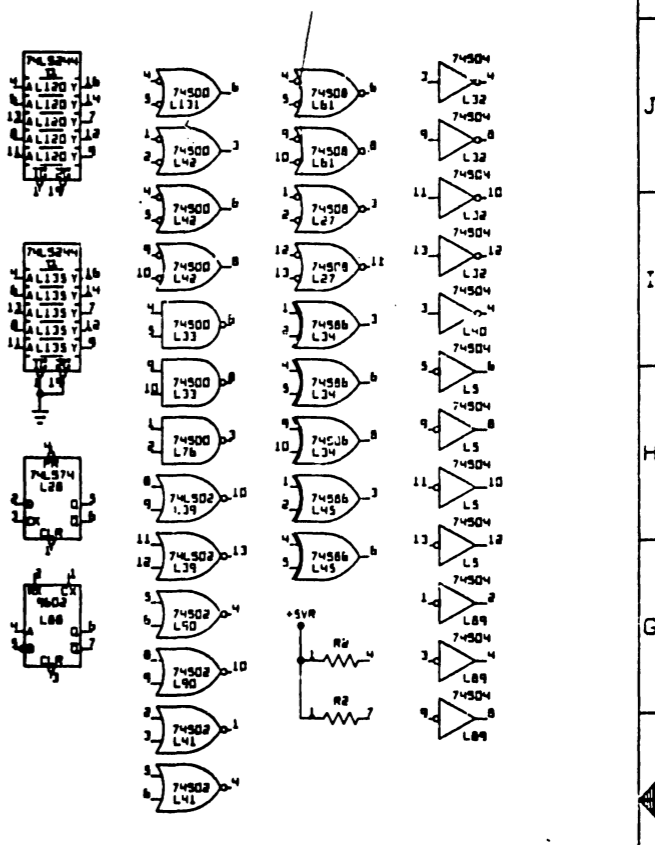
WANG PART NO	DRAWING NO	DESCRIPTION	BY	DATE	APPROVED BY	DATE
			DWN KMT	11/1/83	E ENGR J.F. HAN	12/1/82
			CHK		M ENGR	
					MFG ENGR	
MATERIAL		MODEL NO F27A PFC	TITLE MONITOR BOARD			
FINISH		TOL EX AS NOTED XX ± 0.10 INCH ± 1/64 XXX ± 0.05 ANG ± 1° 30' FINISH	210-8244	D	8244	12
SCALE		1/8" = 1"	WANG PART NUMBER	221	DRAWING NUMBER	REV

14 13 12 11 10 9 8 7 6 5 4 3 2 1



NOTES

1. ALL RESISTOR VALUES IN OHMS.
2. ALL CAPACITOR VALUES IN MICROFARADS UNLESS OTHERWISE INDICATED.
3. ALL RESISTORS 1/4W 5% UNLESS OTHERWISE INDICATED.



210 + 209 + 377 OR 378						
210	209	L3	L72	L73	L116	L38
8287-A	8287	377-036B	377-0427	378-6099-R3	377-0508	378-8046
8287-1A	8287-1	377-036B	377-0427	378-6099-R3	377-0508	377-0418

* VARIATION CHART

BOARD NO.	LOCATION	M.L. PART NO.
8287 (4230)	L46-49, 93-98	397-0476
	L50	377-3044
	L69	377-3043
8287-1 (4205)	L93, 96, 97	DO NOT LOAD
	L50	377-3065
	L69	377-3066

REV	DATE	BY	CHKD	APPRE	REV	DATE	BY	CHKD	APPRE	REV	DATE	BY	CHKD	APPRE
1	3/23/83	JSM			1	9/19/83	KTH			2	10/12/83	KTH		
2	6/27/83	JSM			3	10/12/83	KTH			3	12/7/83	PGD		
3					4					4				
4					5					5				
5					6					6				
6					7					7				

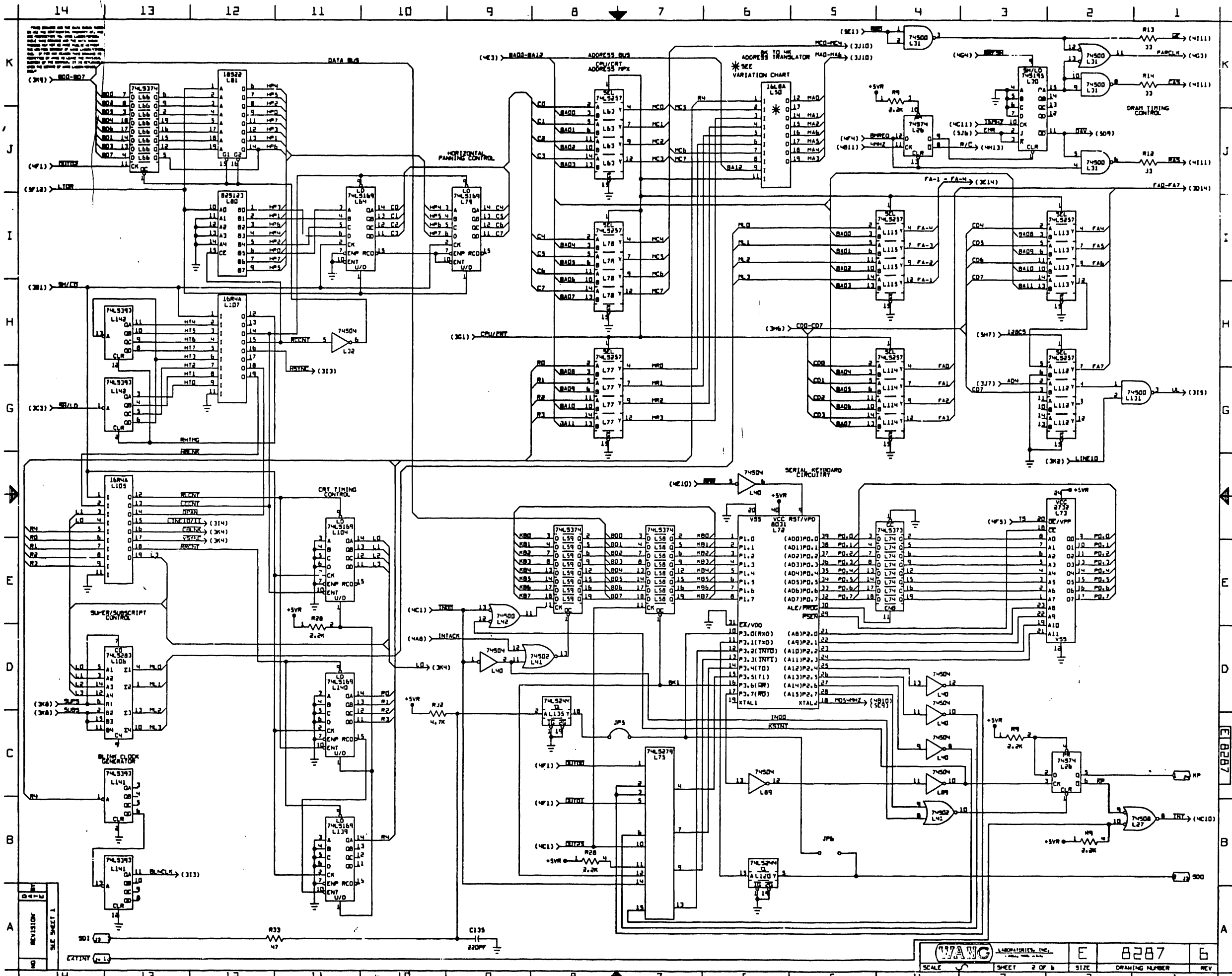
8287-1
C REV
1

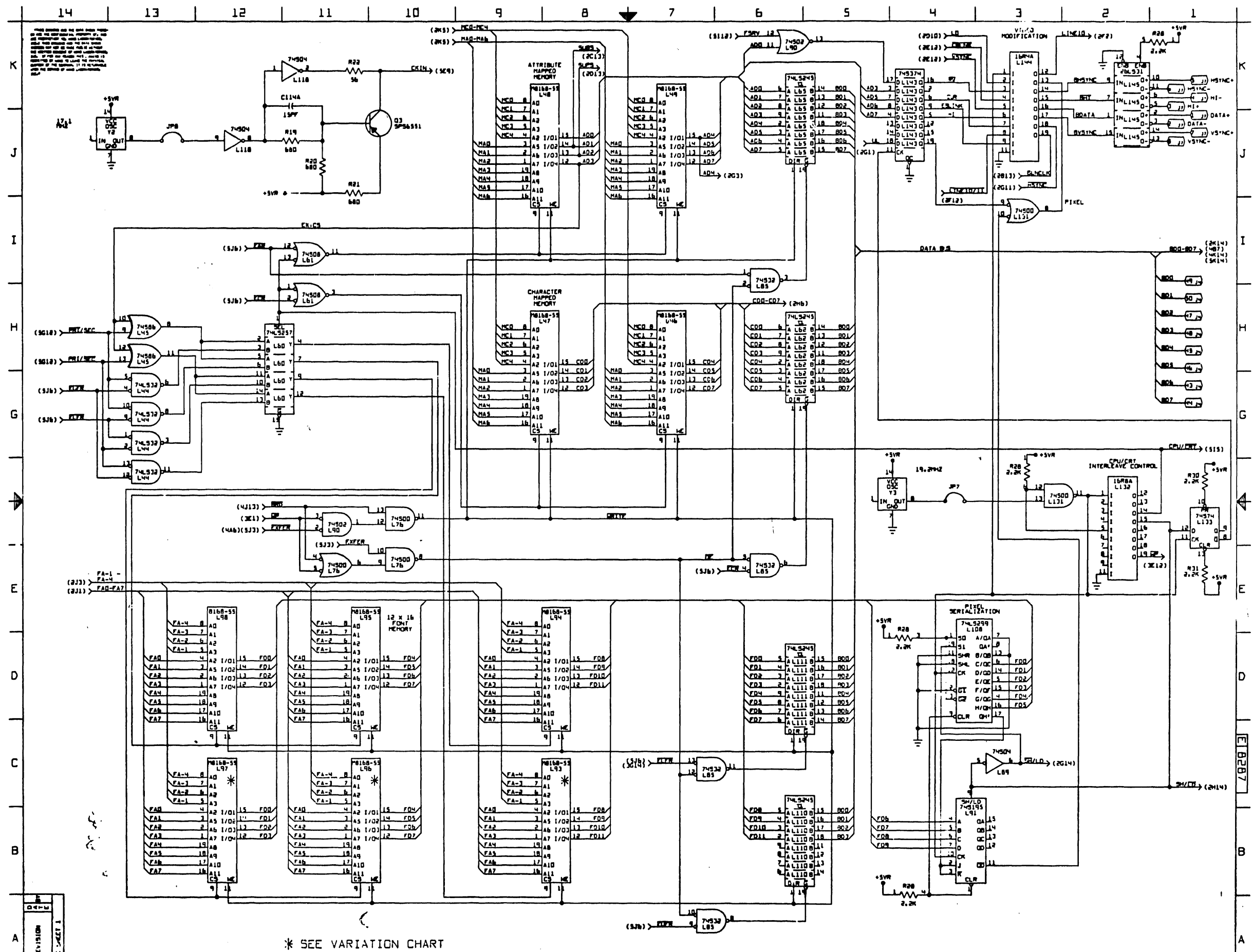
8287
E REV
4

N

WANG LABORATORIES, INC.		SCHEMATIC DIAGRAM	
TITLE		SINGLE BD WS M/L	
MODEL NUMBER H0095C 4230	NAME PART NUMBER SEE CHART	CHKD JSM	ENG TP DTR
SCALE	SHEET 1 OF 6	SIZE E	DRAWING NUMBER 8287
			REV 6

E 8287

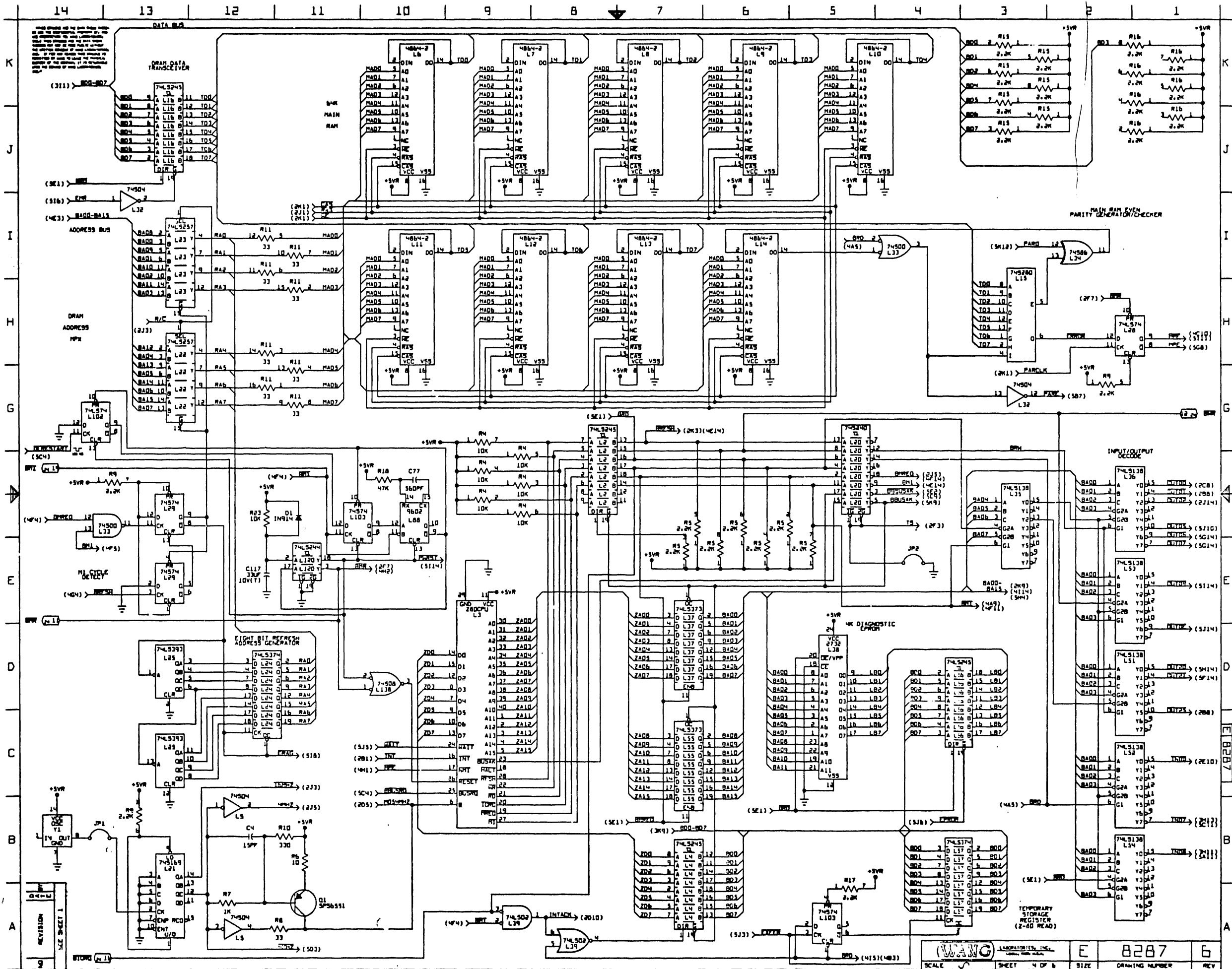




NOTE: THIS CIRCUIT IS DESIGNED TO OPERATE WITH THE FOLLOWING ASSUMPTIONS: 1. THE SYSTEM CLOCK IS 10 MHz. 2. THE SYSTEM BUS IS 16 BITS WIDE. 3. THE MEMORY IS 16 KBYTES. 4. THE MEMORY IS ORGANIZED AS 4096 WORDS BY 16 BITS. 5. THE MEMORY IS ORGANIZED AS 256 WORDS BY 16 BITS. 6. THE MEMORY IS ORGANIZED AS 16 WORDS BY 16 BITS. 7. THE MEMORY IS ORGANIZED AS 1 WORD BY 16 BITS. 8. THE MEMORY IS ORGANIZED AS 1 WORD BY 16 BITS. 9. THE MEMORY IS ORGANIZED AS 1 WORD BY 16 BITS. 10. THE MEMORY IS ORGANIZED AS 1 WORD BY 16 BITS.

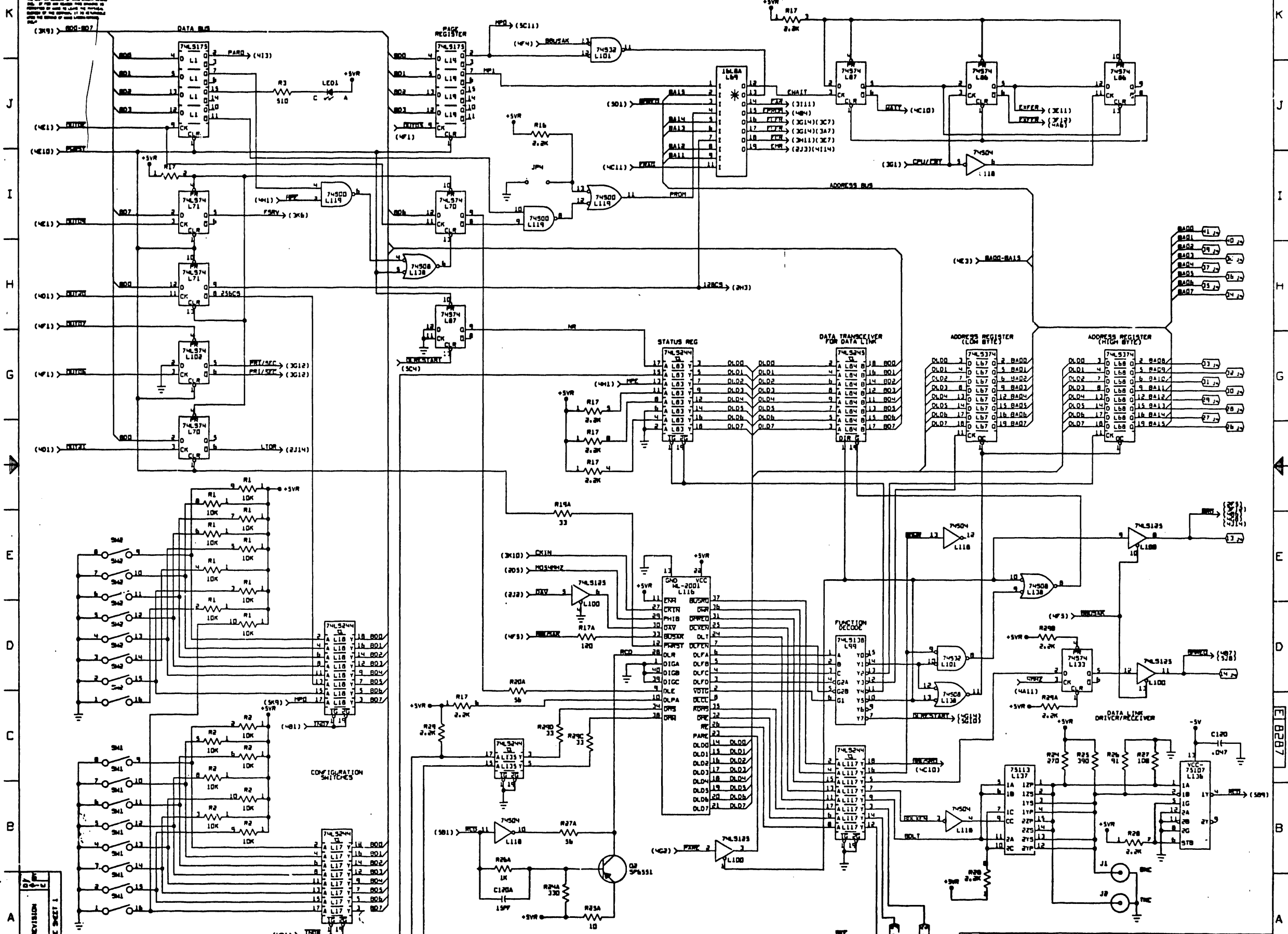
REVISION
SEE SHEET 1

* SEE VARIATION CHART



14 13 12 11 10 9 8 7 6 5 4 3 2 1

*SEE VARIATION CHART



NOTES:
 1. THIS CIRCUIT IS DESIGNED TO OPERATE WITH THE WANG 720C COMPUTER SYSTEM.
 2. THE WANG 720C COMPUTER SYSTEM IS A MICROPROGRAMMED CONTROL SYSTEM.
 3. THE WANG 720C COMPUTER SYSTEM IS A MICROPROGRAMMED CONTROL SYSTEM.
 4. THE WANG 720C COMPUTER SYSTEM IS A MICROPROGRAMMED CONTROL SYSTEM.
 5. THE WANG 720C COMPUTER SYSTEM IS A MICROPROGRAMMED CONTROL SYSTEM.

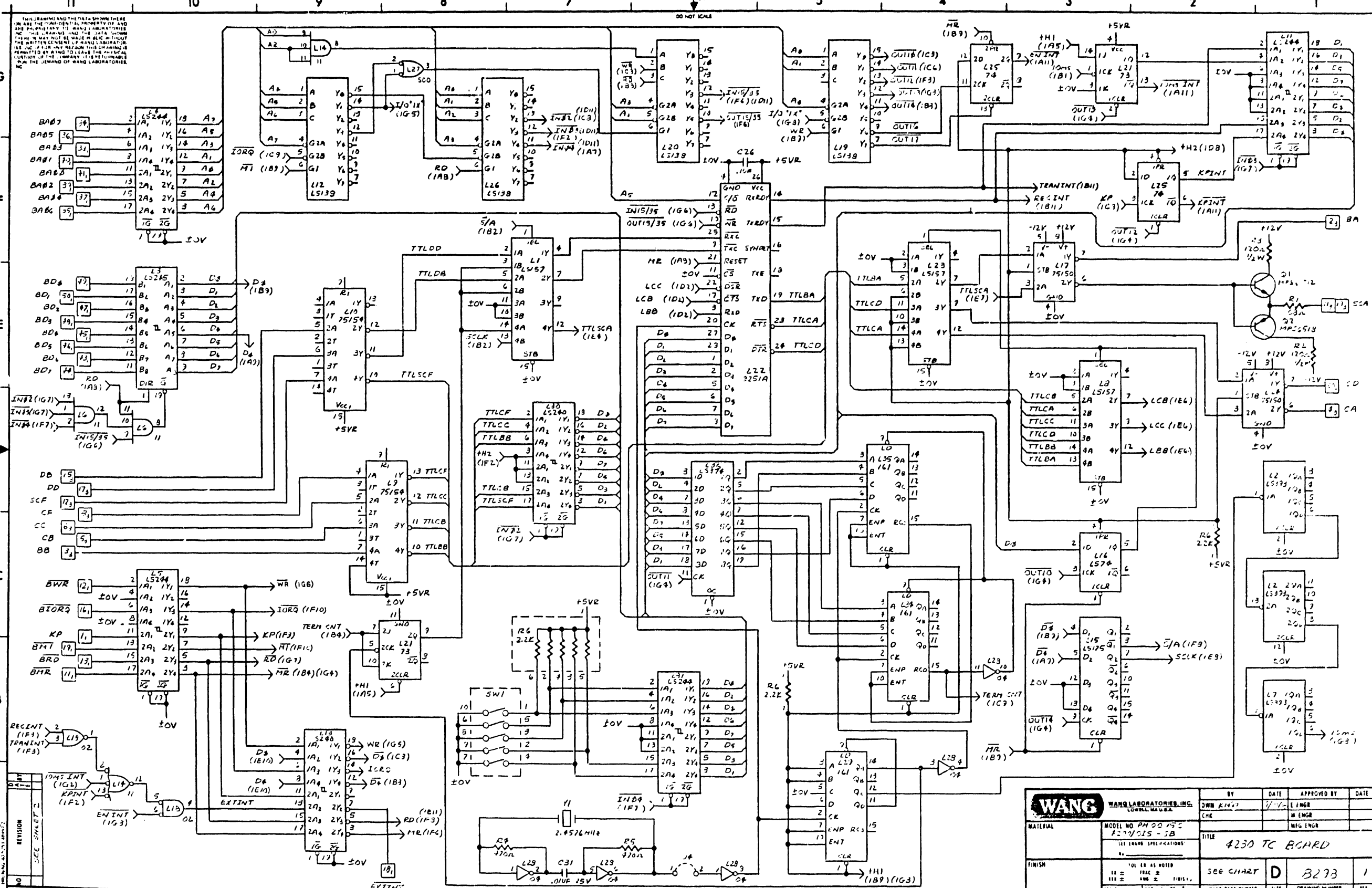
REVISION
 1. 12/27/71
 2. 1/10/72

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ITEM	I.C. LOCATION	TYPE	M.L. PART NO.	QTY
1	L1, L19	74LS175	376-0160	2
2	L2, L4, L16, L16a, L62, L63, L64, L110, L111	74LS245	376-0285	9
3	L3	DACPU	SEE CHART	1
4	L5, L22, L40, L49, L118	74LS1	376-0197	5
5	L6-L14	4864-2	377-0417	9
6	L15	74S280	376-0246	1
7	L17, L18, L83, L117, L120, L135	74LS244	376-0288	6
8				
9	L20	74S240	374-0324	1
10	L21	74S169	375-0331	1
11	L22, L23, L60, L63, L77, L78, L112-L115	74LS257	376-0204	10
12	L24, L27-29, L66-L68	74LS374	376-0286	7
13	L25, L141, L142	74LS393	376-0307	3
14	L26, L29, L86, L87, L103, L133	74S74	376-0202	6
15	L27, L61, L138	74S08	376-0200	3
16	L28, L70, L71, L102	74LS74	376-0155	4
17	L30, L91	74S195	376-0427	2
18	L31, L33, L42, L76, L119, L131	74S00	376-0228	6
19	L34, L45	74S86	376-0271	2
20	L35, L36, L51-L54, L99	74LS138	376-0294	7
21	L37, L55, L74	74LS373	376-0310	3
22	L38	2732A	SEE CHART	1
23	L39	74LS02	376-0208	1
24	L41, L90	74S02	376-0199	2
25	L43, L81, L82, L92, L109, L134	SPARES		
26	L44	74LS32	376-0211	1
27	L46-L49, L93-L98	8168-55	377-0476	10
28	L50	16L8A	377-3044	1
29	L69	16L8A	377-3043	1
30	L64, L79, L104, L139, L140	74LS169	376-0314	5
31	L72	8031	SEE CHART	1
32	L75	74LS279	376-0188	1
33	L80	825123	377-3048	1
34				
35	L85, L101	74S32	376-0205	2
36	L88	9602	376-0104	1
37	L100	74LS125	376-0486	1
38				
39	L105	16R4A	377-3046	1
40	L106	74LS283	376-0332	1
41	L107	16R4A	377-3045	1
42	L108	74LS299	376-0303	1
43	L116	HL-2001	SEE CHART	1
44	L132	16R8A	377-3042	1
45	L136	75107	376-0146	1
46	L137	75113	376-0256	1
47	L143	74S374	376-0305	1
48	L144	16R4A	377-3047	1
49	L145	26LS31	376-0470	1
50	L73	2732	SEE CHART	1

ITEM	LOCATION	TYPE	M.L. PART NO.	QTY
1	R1, R2, R4	10K	332-0809	3
2	R3	510 1/4W 5%	330-2052	1
3	R5, R9, R15-R17, R28	2.2K 51P	332-0806	6
4	R6, R25A	10 1/4W 5%	330-1011	2
5	R7, R26A	1K 1/4W 5%	330-3011	2
6	R8, R12-R14, R19A, R29C, R29D	33 1/4W 5%	330-1034	7
7	R10, R24A	330 1/4W 5%	330-2034	2
8	R11	33 DIP	332-0835	1
9	R17A	120 1/4W 5%	330-2013	1
10	R18	47K 1/4W 5%	330-4048	1
11	R19-R21	680 1/4W 5%	330-2069	3
12	R20A, R22, R27A	56 1/4W 5%	330-1057	3
13	R22, R23	10K 1/4W 5%	330-4011	2
14	R24	270 1/4W 5%	330-2028	1
15	R25	390 1/4W 5%	330-2040	1
16	R26	91 1/4W 5%	330-1092	1
17	R27	100 1/4W 5%	330-2011	1
18	R29-R31	2.2K 1/4W 5%	330-3023	3
19	R32	4.7K 1/4W 5%	330-3048	1
20	R33	47 1/4W 5%	330-1048	1
21				
22	C1, C3, C14-C29, C31-C34, C36, C37, C43-C45, C47-C50, C72-C76, C78-C81, C83, C93-C104, C108-C111, C113-C116, C118-C132, C134	.247UF 50V	300-1966	95
23	C2, C8-C13, C30, C38-C42, C62, C63, C83-C89, C112	.1UF 12V	300-1901	26
24	C4, C14A, C20A	15PF 500V	300-1015	3
25	C77	560PF 500V	300-1560	1
26	C91-C93	15UF 20V (T)	300-4022	3
27	C94	1UF 35V (T)	300-4000	1
28	C117	33UF 10V (T)	300-4024	1
29	C135	220PF 500V	300-5004	1
30				
31	D1	1M14A	380-1012	1
32	LED1	LED RED	370-0075	1
33				
34	J1	CONN BMC RTANG	350-3070	1
35	J2	CONN TMC RTANG	350-3071	1
36	J3	CONN RECEPT	350-0540	1
37	J4	CONN PC	350-0228	1
38	J5	CONN PC HOR	350-0210	1
39	J6	3 POS	350-0539	1
40	J7	8 POS	350-0542	1
41				
42	JP1, JP2, JP4-JP8	CONN HOR 2 POS PIN	350-0203	7
43	JP1, JP2, JP5, JP7, JP8	2 POS SHUNT	350-4506	5
44	Q1, Q2, Q3	9PS5511	375-1050	3
45				
46	SK1, SK2	SPST 8 POS	325-1503	2
47				
48	VRI	755	374-0002	1
49				
50	Y1	31.9488 MHZ	321-1002	1
51	Y2	17.1 MHZ	321-1006	1
52	Y3	19.2 MHZ	321-1007	1
53				
54	L3, L72, L116	SKT 40 PIN	376-9011	3
55	Y1-Y3	SKT 14 PIN	376-9008	3
56				
57				
58				

REVISION
2
SEE SHEET 1



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 THE INFORMATION CONTAINED HEREIN
 FROM THE DEMAND OF WANG LABORATORIES

REVISION	DATE	BY	APPROVED BY
1			
2			
3			
4			
5			
6			
7			
8			
9			
10			
11			

WANG LABORATORIES, INC.		BY	DATE	APPROVED BY	DATE
MODEL NO. PA 00 15 C P. 27015-5B		SWN KIN	7/77	E ENGR	
TITLE		CHK		M ENGR	
4230 TC BOARD					
FINISH					
SCALE					
DRAWING NUMBER					
SIZE					
PART NUMBER					
REV					

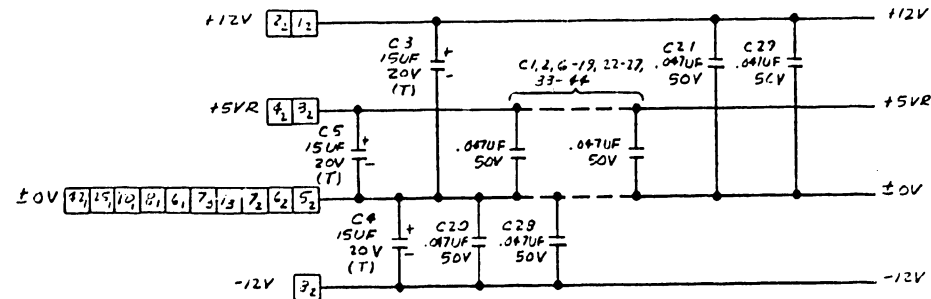
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DO NOT SCALE

IC TYPE	LOCATION	SPARES
74500	L27	3
7402	L18	2
7404	L18	1
7411	L6	1
	L14	1
74LS74	L16	1
74LS333	L7	1

MEMONICS	COORD
EA	1F1
BA13-BA07	1F11
BB	1C11
BD6-BD7	1E11
AZCRQ	1C11
BMT	1B11
BFR	1B11
BRO	1B11
BWR	1C11
CA	1D1
CB	1C11
CC	1C11
CO	1E1
CF	1D11
DB	1D11
DD	1D11
EXT INT	1A3
KP	1C11
SCA	1E1
SCF	1D11

210 = 209 + 377 OR 378		
210	209	222
3273-A	3273	377-0152



NOTE:
 1.) C40 (C41) NOT LOADED BUT TIED TO INNER LAYERS.
 2.) UNLESS OTHERWISE SPECIFIED ALL RESISTORS ARE 1/2W 5%.

E-REV
 []

REV	DATE	BY	CHK	APP	DESCRIPTION
1	11/17/77	WJ	WJ	WJ	INITIAL PER
2	11/17/77	WJ	WJ	WJ	REVISED PER
3	11/17/77	WJ	WJ	WJ	REVISED PER
4	11/17/77	WJ	WJ	WJ	REVISED PER
5	11/17/77	WJ	WJ	WJ	REVISED PER

WANG WANG LABORATORIES, INC. LOWELL, MA U.S.A.		BY	DATE	APPROVED BY	DATE
MODEL NO PH0075C 4230/215-78		OWN	11/17/77	ENG	1/10
SEE INGER SPECIFICATIONS		CHK	WJ	WJ	
TITLE		4230 TC BOARD			
FINISH		101 EE AS NOTED			
SCALE		SEE CHART			
DRAWING NUMBER		D 8233 1			

(FINAL BILL-OF-MATERIALS)

BOARD NO. & TITLE: C8298 4230 TC BOARD
 ASSEMBLY: 209
 ARTWORK REVISION (R): 00
 ASSEMBLY REVISION (A): 01
 SCHEMATIC REVISION (S): 01
 DWR OR MOST RECENT ECO: 111950
 CREATED: 11/21/83 09:19
 LAST MODIFIED: 03/05/84 08:21 BY: LEG
 EDITING REVISION: 4

REF. DES.	WANG PART NO.	VALUE/TYP	DESCRIPTION	DRAWING NO.	QTY.
C26	300-1833-	.1U	CAP CERAMIC MONO AXIA LEADED +80%-20% 50V 25U		1
C31	300-1903-	.01U	CAP CERAMIC DISC +80% -20% 25V 25F		1
C1 - C2	300-1966-	.047U	CAP CERAMIC MONO AXIAL +80 %-20% 50V 25U		38
C6 - C25					
C27 - C29					
C33 - C39					
C42 - C44					
C3 - C5	300-4022-	15U	CAP TANT AXIAL 10% 20V		3
Y1	121-0027-	2.4576	CRYSTAL QUARTZ 2.4576MHZ .005% HC-18/U		1
SW1	125-0062-		SWITCH		1
R1	130-1069-	68.000	RES FIXED 1/4W 5%		1
R4 - R8	130-2048-	470.000	RES FIXED 1/4W 5%		2
R2 - R3	131-2013-	120.000	RES FIXED 1/2W 5%		2
R6	133-0806-	2.200KM	RESISTOR NETWORK TYPE: 08/07/C/SS		1
J4	150-0203-	2 CONT	CONN PC HEADER SINGLE ROW .100 R/A		1
J2	150-0210-	8 CONT	CONN PC HEADER SINGLE ROW .156 R/A W/LOCK		1
J1	150-0228-	50 CONT	CONN PC HEADER W/LOCK/EJECT R/A		1
J3	150-1047-	25 CONT	CONN D-TYPE RECEPTACLE R/A PC MOUNT		1
R1	150-4506-	2 CONT	CONN SHUNT .100 CTR		1
Q1	175-1012-	MPS6512	TSTR NPN TO-92 350MA 10V 2MA		1
Q2	175-1014-	MPS6518	TSTR PNP TO-92 350MA 40V 2MA		1
L21	176-0008-	7473	IC DUAL J-K FLIP-FLOP		1
L28	176-0006-	7474	IC DUAL D-TYPE POSITIVE EDGE-TRIG FLIP-FLOP		1
L28	176-0010-	7404	IC HEX INVERTER		1
L18	176-0016-	7402	IC QUAD 2-INPUT NOR GATE		2
L17	176-0076-	75150	IC DUAL LINE DRIVER 8 PIN DIP		2
L24					
L9 - L10	176-0077-	75154	IC QUAD LINE RECEIVER 16 PIN DIP		2
L29	176-0094-	74151	IC SYN 4-BIT BINARY COUNTER W/DIRECT CLEAR		3
L14 - L15					
L16	176-0155-	74LS74	IC DUAL D-TYPE POSITIVE EDGE TRIG FLIP-FLOP		1
L15	176-0160-	74LS178	IC QUAD D-TYPE FLIP-FLOP		1
L6	176-0194-	7411	IC TRIPLE 3-INPUT AND GATE		2
L14					
L1	176-0216-	74LS157	IC QUAD 2-INPUT MULTIPLEXER		3
L8					
L23					
L27	176-0228-	74500	IC QUAD 2-INPUT NAND GATE		1

BOARD NO. & TITLE: C8298 4230 TC BOARD SCHEMATIC REVISION (S): 01 SHEET OF PAGE 3

WANG PART NO.	VALUE/TYP	DESCRIPTION	DRAWING NO.	QTY.
176-0334-	745240	IC OCTAL BUFFER/LINE DRIVER		1

*** END-OF-REPORT ***

BOARD NO. & TITLE: C8298 4230 TC BOARD SCHEMATIC REVISION (S): 01 SHEET OF PAGE 1

REF. DES.	WANG PART NO.	VALUE/TYP	DESCRIPTION	DRAWING NO.	QTY.
L3	176-0288-	74LS248	IC OCTAL BUS TRANSCIEVER TRI-STATE OUTPUTS		1
L36	176-0286-	74LS374	IC OCTAL D-TYPE FLIP-FLOP TRI-STATE		1
L4 - L8	176-0288-	74LS244	IC OCTAL BUFFER/LINE DRIVER W/TRI STATE		4
L11					
L12	176-0294-	74LS138	IC 3-LINE TO 8-LINE DECODER/W. PLEAER		4
L19 - L20					
L26					
L30	176-0297-	74LS248	IC OCTAL BUFFER/LINE DRIVER/LINE RECEIVER		1
L2	176-0307-	74LS393	IC DUAL 4-BIT BINARY COUNTER		2
L7					
L13	176-0334-	745240	IC OCTAL BUFFER/LINE DRIVER		1
L22	176-9015-	SKT 28	IC SOCKET 28 PIN DIL MOUNT		1
01	513-8298-		PCB		1

(FINAL BILL-OF-MATERIALS)

BOARD NO. & TITLE: C8298 4230 TC BOARD
 ASSEMBLY: 210-A
 ARTWORK REVISION (R): 00
 ASSEMBLY REVISION (A): 01
 SCHEMATIC REVISION (S): 01
 DWR OR MOST RECENT ECO: 111950
 CREATED: 11/21/83 09:19
 LAST MODIFIED: 03/05/84 08:21 BY: LEG
 EDITING REVISION: 4

REF. DES.	WANG PART NO.	VALUE/TYP	DESCRIPTION	DRAWING NO.	QTY.
01	209-8298-		PCB		1
L22	377-0352-	8251A	IC PROGRAMMABLE COMMUNICATION INTERFACE		1
02	451-5232-		BRACKET		1
05	615-2174-		TABLE		1
03 - 04	651-0408-		RIVET NO 3		2


WANG	WANG LABORATORIES, INC. LOWELL, MA U.S.A.	BY	DATE	APPROVED BY	DATE
		DWN		E ENGR	
MATERIAL	MODEL NO.	CHK		M ENGR	
				MFG ENGR	
SEE ENGR SPECIFICATIONS No. _____		TITLE 4230 TC BOARD			
FINISH	TOL EX AS NOTED XX ± 010 FRAC ± 1/64 XXX ± 005 ANG ± 1'30" FINISH	SEE CHART	D	8298	1
	SCALE	SHT 3 OF 4	WANG PART NUMBER	SIZE	DRAWING NUMBER

BOARD NO. & TITLE: C8298 4230 TC BOARD SCHEMATIC REVISION (S): 01 SHEET 4 OF 4 PAGE 2 M

WANG PART NO.	VALUE/TYPE	DESCRIPTION	DRAWING NO.	QTY.
377-0182-	8251A	IC PROGRAMMABLE COMMUNICATION INTERFACE		1

(CAUTION - THE FOLLOWING PARTS/COMPONENTS CONTAINED IN THIS B.O.M. ARE NOT RECOMMENDED FOR NEW DESIGNS)

*** END-OF-REPORT ***

 WANG LABORATORIES, INC. LOWELL, MA U.S.A.		BY	DATE	APPROVED BY	DATE
		DWN		E ENGR	
MATERIAL		CHK		M ENGR	
				MFG ENGR	
MODEL NO.		TITLE			
SEE ENGRG SPECIFICATIONS No. _____		4230 TC BOARD			
FINISH	TOL EX AS NOTED	SEE CHART	D	8298	1
	XX ± 010 FRAC ± 1/64 XXX ± 005 ANG ± 1°30' FINISH				
SCALE		SHT 4 OF 4	WANG PART NUMBER	SIZE	DRAWING NUMBER

8.5"

11"

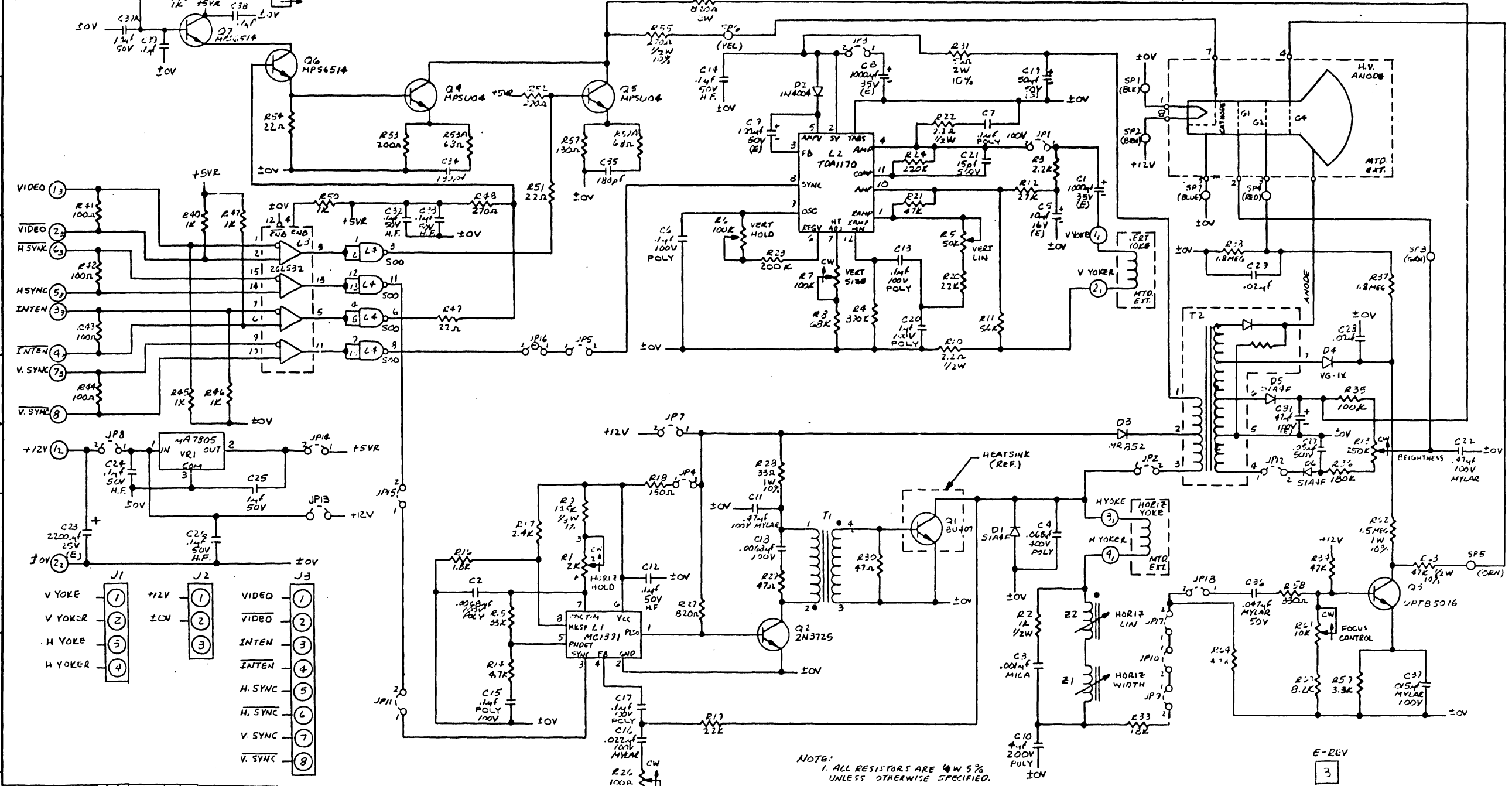
17"

8.5"

11"

17"

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NOTE: ALL RESISTORS ARE 1/4W 5% UNLESS OTHERWISE SPECIFIED.

REV	DATE	DESCRIPTION
1	11-27-77	ORIGINAL PLS
2	12-15-77	CHG R25 TO 200Ω
3	1-12-78	REVISED PER
4	2-15-78	REVISED PER
5	3-15-78	REVISED PER
6	4-15-78	REVISED PER
7	5-15-78	REVISED PER
8	6-15-78	REVISED PER
9	7-15-78	REVISED PER
10	8-15-78	REVISED PER
11	9-15-78	REVISED PER
12	10-15-78	REVISED PER
13	11-15-78	REVISED PER
14	12-15-78	REVISED PER
15	1-15-79	REVISED PER
16	2-15-79	REVISED PER
17	3-15-79	REVISED PER
18	4-15-79	REVISED PER
19	5-15-79	REVISED PER
20	6-15-79	REVISED PER
21	7-15-79	REVISED PER
22	8-15-79	REVISED PER
23	9-15-79	REVISED PER
24	10-15-79	REVISED PER
25	11-15-79	REVISED PER
26	12-15-79	REVISED PER
27	1-15-80	REVISED PER
28	2-15-80	REVISED PER
29	3-15-80	REVISED PER
30	4-15-80	REVISED PER
31	5-15-80	REVISED PER
32	6-15-80	REVISED PER
33	7-15-80	REVISED PER
34	8-15-80	REVISED PER
35	9-15-80	REVISED PER
36	10-15-80	REVISED PER
37	11-15-80	REVISED PER
38	12-15-80	REVISED PER
39	1-15-81	REVISED PER
40	2-15-81	REVISED PER
41	3-15-81	REVISED PER
42	4-15-81	REVISED PER
43	5-15-81	REVISED PER
44	6-15-81	REVISED PER
45	7-15-81	REVISED PER
46	8-15-81	REVISED PER
47	9-15-81	REVISED PER
48	10-15-81	REVISED PER
49	11-15-81	REVISED PER
50	12-15-81	REVISED PER

WANG PART NO	DRAWING NO	DESCRIPTION	BY	DATE	APPROVED BY	DATE
			OWN E.M.T.	11/27/77	ENGR J.S.L.	11/27/77
			CHK J.S.L.	11/27/77	M ENGR	11/27/77
					WFG ENGR	
MATERIAL		MODEL NO PH 267A	TITLE MONITOR BOARD			
FINISH		TO 16 45 10710	210 8-44	D	8344	
		SCALE 1/8" = 1"	WANG PART NUMBER	REV	DATE	REV

(FINAL BILL-OF-MATERIALS)

Table with columns: REF. DES., WANG PART NO., VALUE/TYPE, DESCRIPTION, DRAWING NO., QTY. Includes parts like CAP CERAMIC DISC, CAP CERAMIC MONO AXIAL, CAP OSU, CAP ALUM ELEC, etc.

Table with columns: REF. DES., WANG PART NO., VALUE/TYPE, DESCRIPTION, DRAWING NO., QTY. Includes parts like RES FIXED 1/4W 5%, RES FIXED METAL FILM, etc.

Table with columns: REF. DES., WANG PART NO., VALUE/TYPE, DESCRIPTION, DRAWING NO., QTY. Includes parts like RES VAR 100K OHM, IC REG 7805, TRANSFORMER, etc.

Table with columns: REF. DES., WANG PART NO., VALUE/TYPE, DESCRIPTION, DRAWING NO., QTY. Includes part 376-0228-74500 IC QUAD 2-INPUT NAND GATE.

*** END-OF-REPORT ***

WANG LABORATORIES, INC. LOWELL, MA U.S.A. BY: DWN DATE: CHK: M ENGR DATE: MFG ENGR MATERIAL: MODEL NO: TITLE: MONITOR BOARD FINISH: TOL EX AS NOTED XX ± 010 FRAC ± 1/64 XXX ± 005 ANG ± 1°30' FINISH ✓ 210-8344 C 8344 7 SCALE: SHY Z OF 2 WANG PART NUMBER SIZE DRAWING NUMBER REV

END