PROGRAMMABLE TRACKING FILTER IMP42C455-13

General Description

The IMP42C455-13 is a programmable continuous-time filter operating in the 2MHz to 13MHz cutoff frequency range. Its amplitude and phase response may be modified via a digital serial interface. This makes the 42C455-13 suitable for a variety of applications requiring modifiable responses such as disk drive read channels, telecom, video systems and other signal processing applications.

The filter consists of a 6th order Bessel lowpass filter and an asymmetrical pulse slimmer. The pulse slimmer zeros and the frequency scaling can be programmed through the serial interface. Matched normal and differentiated outputs are provided.

The general form of the filter transfer function is given by:

$$H_{NORM}(s) = A_{NORM}\left[1+\frac{s}{\omega_{z_a}}\right]\left[1-\frac{s}{\omega_{z_b}}\right]H_{Lowpass}(s)$$

$$H_{DIFF}(s) = A_{DIFF}[s]\left[1+\frac{s}{\omega_{z_a}}\right]\left[1-\frac{s}{\omega_{z_b}}\right]H_{Lowpass}(s)$$

where A_{NORM} & A_{DIFF} are used to set DC gains and ω_{z_a} & ω_{z_b} represent the slimmer zeros.

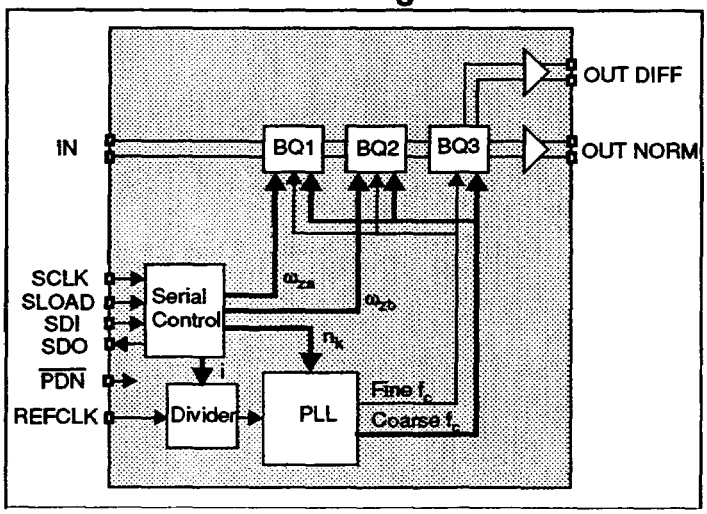
The IMP42C455-13 uses an external reference frequency and an internal Phase-Lock Loop to assure accuracy over process and environmental conditions. It also provides high accuracy pole and zero placement.

The IMP42C455-13 is based upon a transconductance-C filter technology and implemented in IMP's proprietary MxCMOS 1.2µm process.

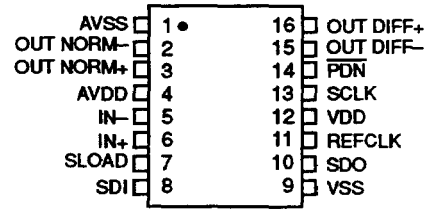
Features

- 6th order Bessel Lowpass Filter
- Unboosted cutoff frequency programmable between 2MHz and 13MHz
- Programmable zeros for both symmetric and asymmetric pulse slimming
- Accurate (10%) pole placement using reference frequency and PLL tuning
- No external components required
- +5 volt operation
- Low-power mode
- Quadrature outputs
- Completely differential signal path
- 16 pin SOIC and DIP packages

Block Diagram



Pin Assignment



Pin Descriptions

NAME	DESCRIPTION
IN+	Filter positive differential input
IN–	Filter negative differential input
OUT NORM+	Filter normal positive differential output
OUT NORM–	Filter normal negative differential output
OUT DIFF+	Filter differentiated positive differential output
OUT DIFF–	Filter differentiated negative differential output
SCLK	Clock input for shifting in serial data for programming the filter characteristics. Input is TTL compatible
SDI	Input for shifting in serial data for setting the filter characteristics. A low level corresponds to a logical "0". Data is sampled on a high-to-low transition of SCLK. Input is TTL compatible.
SLOAD	Input used to latch serial data into internal registers. Data may be shifted in when SLOAD is low. Data is latched in when SLOAD transitions high. Input is TTL compatible.
SDO	Output for shifting out data stored in internal registers. Data changes on the high-to-low transition of SCLK. Output is high-impedance until the low-to-high transition of SLOAD after writing a readback address. The output returns to a high impedance state after the ninth high-to-low transition of SCLK after SLOAD transitions high.
REFCLK	Clock reference for tuning the filter response. Input is TTL compatible.
PDN	A low level on this input causes the IC to go into a low power standby condition. Input is TTL compatible.
AVDD	Positive supply voltage - Analog
AVSS	Ground - Analog
VDD	Positive supply voltage - Digital
VSS	Ground -Digital

Electrical Specifications

Absolute Maximum Ratings

Parameter	Conditions	Min	Nom	Max	Units
Supply Voltage	VDD-VSS	0		8.0	V
Voltage on any input	min relative to VSS	–0.3			V
	max relative to VDD			+0.3	V
Storage temperature		0		150	degrees C

Recommended Operating Conditions

Parameter	Conditions	Min	Nom	Max	Units
Supply Voltage	VDD-VSS	4.5	5.0	5.5	V
Ambient operating temperature		0	25	70	degrees C

DC Characteristics

Parameter	Conditions	Min	Nom	Max	Units
Power supply current				85	mA
Powerdown supply current	PDN=Low		250	1000	µA
High level input voltage	TLL inputs only	2.0			V
Low level input voltage	TTL inputs only			0.8	V
High level output voltage	SDO, IOH=2mA	2.4			V
Low level output voltage	SDO, IOL=3.2mA			0.4	V

AC Characteristics

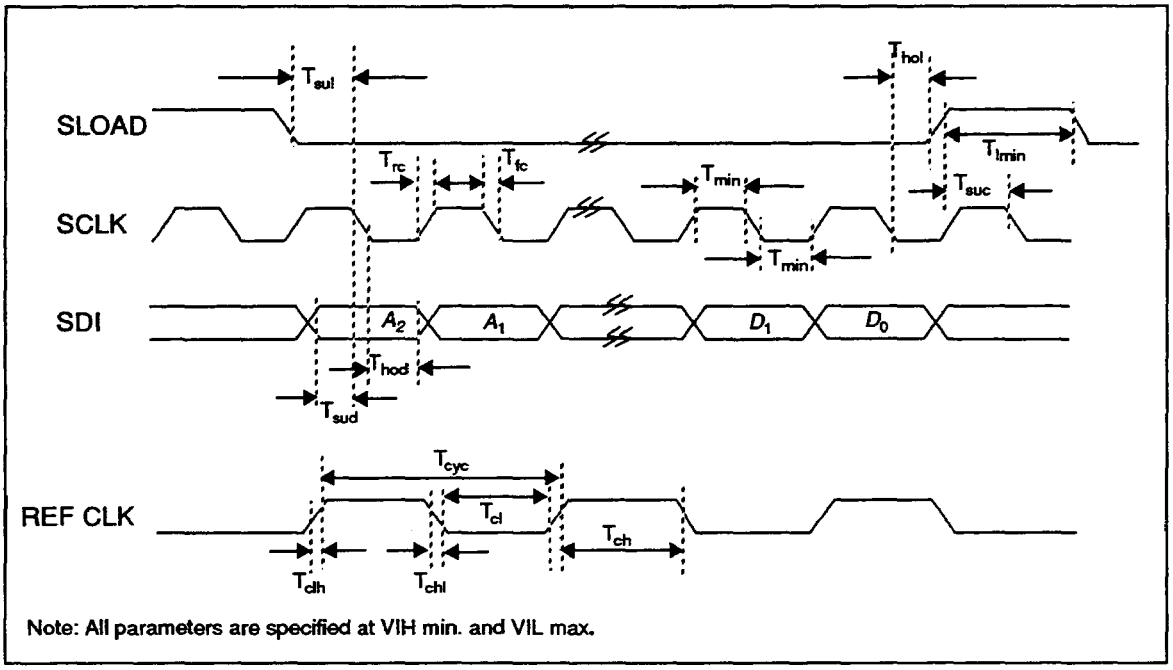
(unless otherwise specified: f_{refclk}=39MHz, No boost, $f_c = f_{refclk}/3$)

Parameter	Conditions	Min	Nom	Max	Units
Filter cutoff frequency (f_C) range		2		13	MHz
Filter cutoff frequency accuracy				± 10	%
Vout norm differential gain	$f = 0.1f_C$	–1.5		+1.5	dB
Vout diff differential gain	$f = 0.67f_C$	–1.5		+1.5	dB
Phase shift between norm and diff	$f = 0.67f_C$	87	90	93	degrees
Programmable boost range at f_C		0		10.6	dB
Boost accuracy		–1		1	dB
Differential group delay without boost	f_C = 13MHz f = 2 to 13MHz	-0.6		0.6	nS
Differential group delay with full boost	f_C = 13MHz f = 2 to 13MHz	-0.6		0.6	nS
Harmonic distortion	2nd, 3rd harmonic Vin,Vout < 1.0Vp-p Vin,Vout < 1.5Vp-p			 –40 –30	 dB dB
Power supply rejection	VDD, 1MHz	35			dB
Common mode rejection	1MHz	45			dB
Output noise	Measurement BW= 30MHz			1.5	mVRMS
Filter output differential offset	Norm and Diff			100	mV
Filter input common-mode level	V_{DD} = 5V	2.0	2.1	2.2	V
Filter input resistance	Differential	3			kohms
Filter input capacitance	C to VSS		10		pF
Filter output common-mode	V_{DD} = 5V	1.5		2.5	V
Resistive load on filter outputs	Differential	2			kohms
Capacitive load on filter outputs	C to VSS			25	pF
Tuning PLL lock capture time	Full range of refclk Change in refclk +/-50%			1.0 100	mS uS
Refclk feedthrough				0.5	mVp-p

Input Timing Specifications

Parameter	Conditions	Min	Max	Units
T_{sul}	SLOAD setup time to SCLK	50		nS
T_{hol}	SLOAD hold time after SCLK	50		nS
T_{rc}	SCLK rise time		10	nS
T_{fc}	SCLK fall time		10	nS
T_{min}	SCLK high time and low time	100		nS
T_{sud}	SDI setup time to SCLK	50		nS
T_{hod}	SDI hold time after SCLK	50		nS
T_{suc}	SLOAD high to SCLK falling edge	50		nS
T_{lmin}	SLOAD high time		100	nS
T_{clh}	REFCLK rise time		10	nS
T_{chl}	REFCLK fall time		10	nS
T_{ch}	REFCLK high time	5		nS
T_{cl}	REFCLK low time	5		nS
T_{cyc}	REFCLK cycle time	20		nS

Timing Diagram



Note: All parameters are specified at VIH min. and VIL max.

Serial Interface Programming

A simple 3 input serial interface is provided to program the filter coefficients. Data is shifted in 8-bit sequences. The 3 bit address (MSB first) is shifted in first, followed by 5 bits of data (MSB first). There are 8 internal register addresses. Data is clocked in on the falling edge of SCLK. Data is loaded to internal registers on the rising edge of SLOAD.

Register Programming (Write)

Data in								Internal register
d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0	written
0	0	0	X	X	b_2	b_1	0	Control
0	0	1	b_4	b_3	b_2	b_1	b_0	ω_{za}
0	1	0	b_4	b_3	b_2	b_1	b_0	ω_{zb}
1	0	1	b_4	b_3	b_2	b_1	b_0	ω_c scaling
1	1	0	X	X	X	X	X	Calibrate on demand
1	1	1	X	X	b_2	b_1	b_0	Readback

Contents of the internal registers may be read back. A register is selected by placing the address of the register to be read in the data field.

During readback, 8-bits of data is shifted out the SDO pin on the falling edge of SCLK. SDO should be sampled on the rising edge of SCLK. Upon receiving a ninth clock pulse, the SDO output will go high impedance.

Register Programming (Readback)

Data in								Data out								Internal register
d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0	d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0	bits read
1	1	1	X	X	0	0	0	0	0	0	0	0	b_2	b_1	0	Control
1	1	1	X	X	0	0	1	0	0	1	b_4	b_3	b_2	b_1	b_0	ω_{za}
1	1	1	X	X	0	1	0	0	1	0	b_4	b_3	b_2	b_1	b_0	ω_{zb}
1	1	1	X	X	1	0	1	1	0	1	b_4	b_3	b_2	b_1	b_0	ω_c scaling

Control

Register address = 000

Data:

$d_0 = 0$	Program to zero	(power up state = 0)
$d_1 = 1$	Continuous calibration enabled	(power up state = 1)
$d_2 = 0$	Power down mode enabled	(power up state = 1)

If continuous calibration is disabled, then a single calibration cycle may be initiated by writing to the address = 110. Data bits are ignored. Calibration begins on the rising edge of SLOAD.

Pulse Slimmer:

$$\omega_{z_a} = 0.65 \cdot \frac{20}{n_a} \cdot \omega_c \qquad n_a \in (0 \ldots 20)$$

Register address = 001

d_4	d_3	d_2	d_1	d_0	n_a
0	0	0	0	0	0 *
0	0	0	0	1	1
~	~	~	~	~	~
1	0	0	1	1	19
1	0	1	0	0	20

$$\omega_{z_b} = 0.65 \cdot \frac{20}{n_b} \cdot \omega_c \qquad n_b \in (0 \ldots 20)$$

Register address = 010

d_4	d_3	d_2	d_1	d_0	n_b
0	0	0	0	0	0 *
0	0	0	0	1	1
~	~	~	~	~	~
1	0	0	1	1	19
1	0	1	0	0	20

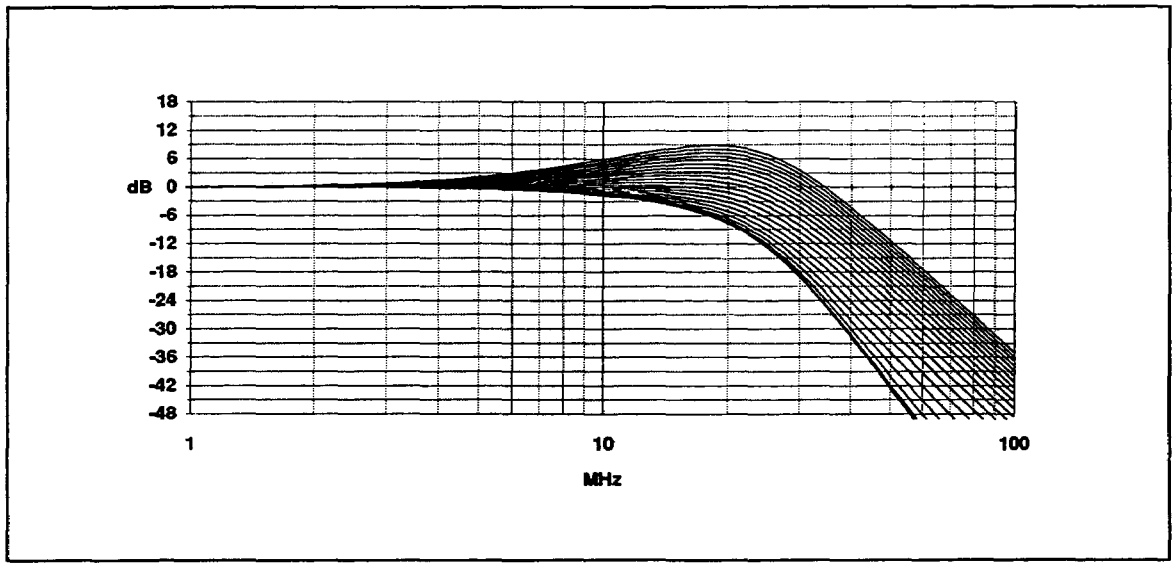
Symmetrical Boost:

n_a	n_b	Boost[1]	ω_{3dB}
0 *	0 *	0dB	1.00 ω_c
1	1	0.05dB	1.01 ω_c
2	2	0.20dB	1.03 ω_c
3	3	0.45dB	1.08 ω_c
4	4	0.79dB	1.15 ω_c
5	5	1.20dB	1.25 ω_c
6	6	1.68dB	1.37 ω_c
7	7	2.21dB	1.52 ω_c
8	8	2.79dB	1.66 ω_c
9	9	3.40dB	1.81 ω_c
10	10	4.04dB	1.94 ω_c
11	11	4.69dB	2.06 ω_c
12	12	5.35dB	2.18 ω_c
13	13	6.02dB	2.29 ω_c
14	14	6.69dB	2.39 ω_c
15	15	7.35dB	2.50 ω_c
16	16	8.01dB	2.59 ω_c
17	17	8.66dB	2.68 ω_c
18	18	9.30dB	2.77 ω_c
19	19	9.93dB	2.85 ω_c
20	20	10.54dB	2.94 ω_c

1. Boost measured at ω_c relative to -3dB

* Default state after powerup

Gain as a function of boost



Frequency Scaling:

ω_c is the lowpass filter 3dB cutoff

$$\omega_c \equiv 2\pi f_c = 2\pi \cdot \frac{2 \cdot f_{refclk}}{3} \cdot \frac{K}{i} \qquad i \in (1, 2, 3, 4)$$

$$K = \frac{7.17}{3.17 + n_K} \qquad n_K \in (0 \ldots 7)$$

Register address = 101

Data:

d_4	d_3	i	
0	0	1	
0	1	2	*
1	0	3	
1	1	4	

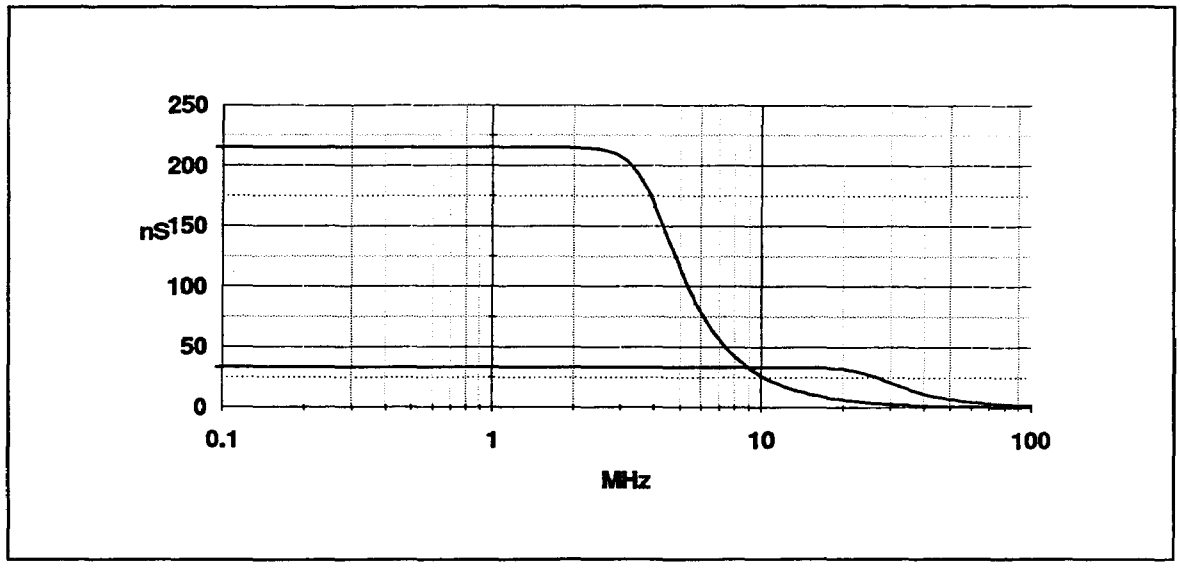
d_2	d_1	d_0	n_K	K
0	0	0	0	2.262
0	0	1	1	1.719
0	1	0	2	1.387
0	1	1	3	1.162
1	0	0	4 *	1.000
1	0	1	5	0.878
1	1	0	6	0.782
1	1	1	7	0.705

* Default state after powerup

f_{cutoff} Look-Up Table - Reg 101

fc/Refclk	i	n	Binary
0.118	4	7	11111
0.130	4	6	11110
0.146	4	5	11101
0.157	3	7	10111
0.167	4	4	11100
0.174	3	6	10110
0.194	4	3	11011
0.195	3	5	10101
0.222	3	4	10100
0.231	4	2	11010
0.235	2	7	01111
0.258	3	3	10011
0.261	2	6	01110
0.287	4	1	11001
0.293	2	5	01101
0.308	3	2	10010
0.333 *	**2**	**4**	**01100 ***
0.377	4	0	11000
0.382	3	1	10001
0.387	2	3	01011
0.462	2	2	01010
0.470	1	7	00111
0.503	3	0	10000
0.521	1	6	00110
0.573	2	1	01001
0.585	1	5	00101
0.667	1	4	00100
0.754	2	0	01000
0.775	1	3	00011
0.925	1	2	00010
1.146	1	1	00001
1.508	1	0	00000

Group Delay vs f_c



Lowpass Characteristics

$$H_{LOWPASS}(s) = \left(\frac{\omega_{P_1}^2}{s^2 + s\frac{\omega_{P_1}}{Q_{P_1}} + \omega_{P_1}^2}\right)\left(\frac{\omega_{P_2}^2}{s^2 + s\frac{\omega_{P_2}}{Q_{P_2}} + \omega_{P_2}^2}\right)\left(\frac{\omega_{P_3}^2}{s^2 + s\frac{\omega_{P_3}}{Q_{P_3}} + \omega_{P_3}^2}\right)$$

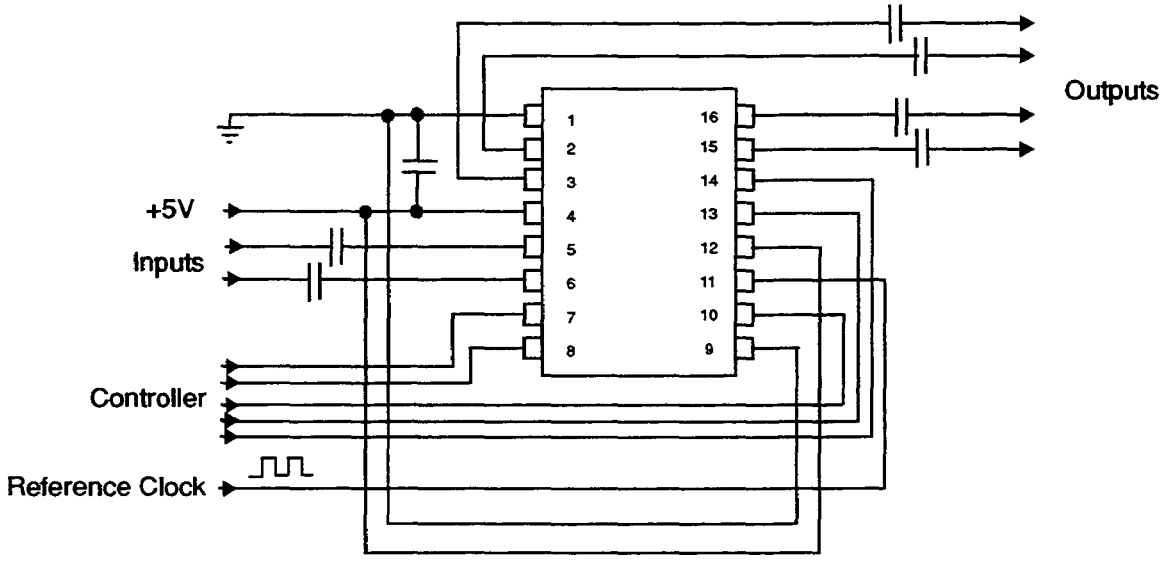
Biquad	ω_p	Q_p
1	1.607	0.510
2	1.692	0.611
3	1.908	1.023

Note: ω_c normalized to 1 rad/sec

Application Information

To allow the inputs to be AC coupled, the differential filter inputs are internally DC biased to the correct common mode voltage. Using 0.1µFcapacitors to couple the IN– and IN+ inputs is recommended.

Analog and digital supplies must be connected together at the point that they are decoupled.



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