

High Speed Input/Output Board

Logic Drawings

HSIO Board

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4. HSIO03.sily - *Display controller parts list*
5. HSIO04.sily - *Disk controller parts list*
6. HSIO05.sily - *Disk controller parts list*
7. HSIO06.sily - *Stichweld layout*
8. HSIO07.sily - *proposed PWB layout*

Display Controller

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2. HSIO23 - *Cycles, Clicks and Display counter*
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4. HSIO25 - *Data FIFO and Border Register*
5. HSIO26 - *Control FIFO Data Path*
6. HSIO27 - *Read Machine; Word Counter & End Conditions*
7. HSIO28 - *LCAS & LRAS' Generation*
8. (p/s)HSIO29 - *Discretes, Connectors*

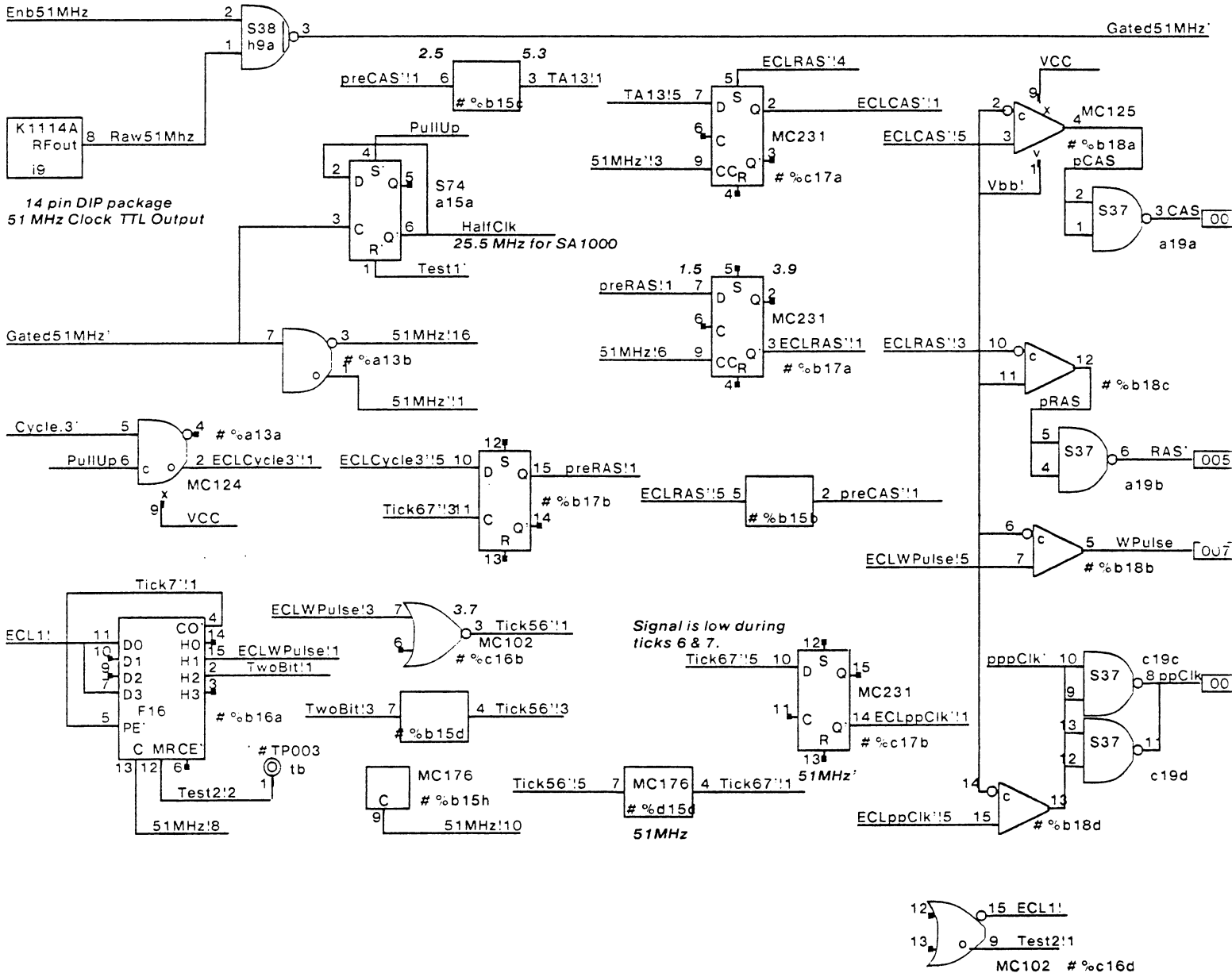
Disk Controller

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24. sHSIO61 - *Discrete Phase comparator, Stichweld Version*
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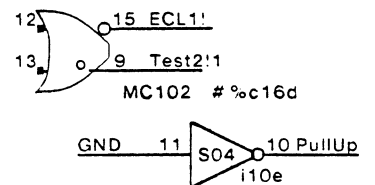
Other Documentation

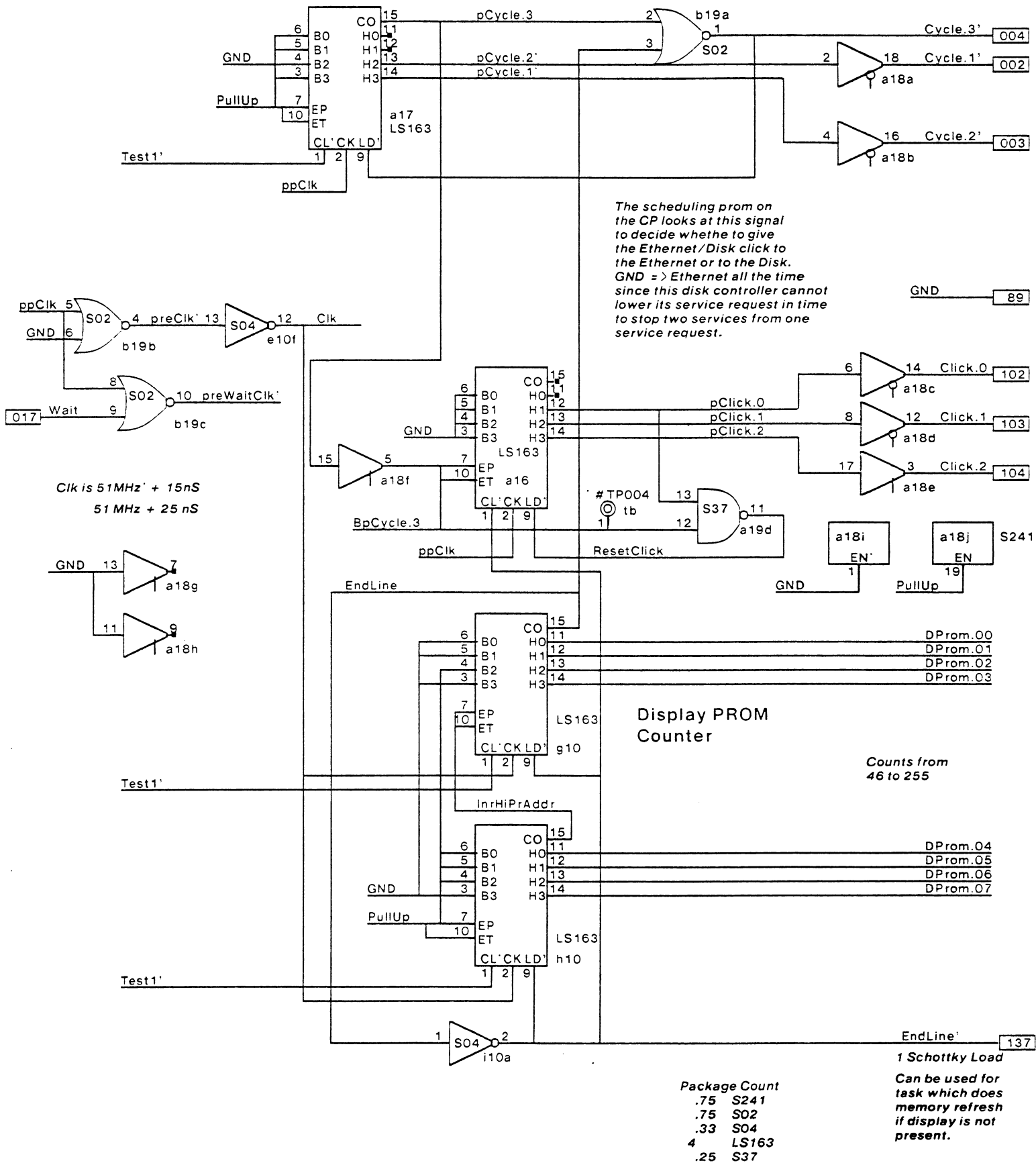
<i>This file is in:</i>	<i>[Iris]<Workstation>HSIO>HSIO-Rev-R.press</i>	<i>All logic drawings in Press format</i>
	<i>[Iris]<Workstation>HSIO>HSIO-R.dm</i>	<i>All design Automation info about HSIO board</i>
	<i>[Iris]<Workstation>HSIO>HSIO-R.wl</i>	<i>Wirelist for this rev of HSIO board</i>
	<i>[Iris]<Workstation>HSIO>DDC-Rev-R.DocDm</i>	<i>Disk Documentation in Sil and Bravo formats</i>
	<i>[Iris]<Workstation>HSIO>DDC-Rev-R.press</i>	<i>All Disk Documentation in Press format</i>
	<i>[IRIS]<Workstation>HSIO>Proms>DDCProms-Rev-A.dm</i>	<i>Disk Prom Programs</i>
	<i>[Iris]<Workstation>HSIO>WSD-Rev-C.DocDm</i>	<i>Display Documentation drawings, Timing Diagrams</i>
	<i>[Iris]<Workstation>HSIO>WSD-Rev-C.press</i>	<i>All Display Logic, Timing diagrams in Press format</i>
	<i>[Iris]<Workstation>HSIO>Proms>DisplayProms-Rev-A.dm</i>	<i>Display Prom Programs</i>

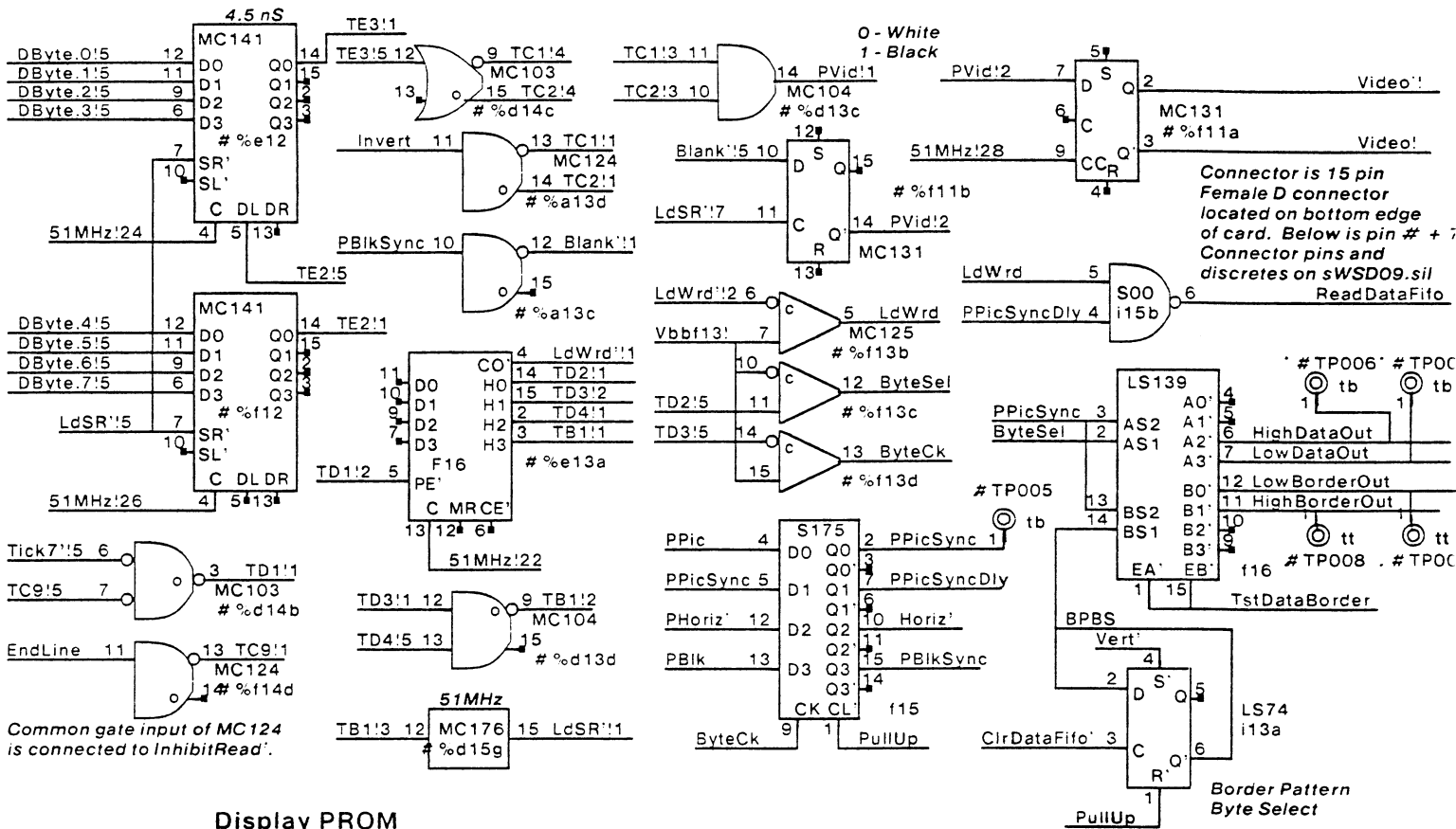
XEROX	Project	Reference	File	Designer	Rev	Date	Page
SDD	Dandelion	High Speed I/O Board	sHSIO00.sil	Crane, Davies	R	10/22/80	0



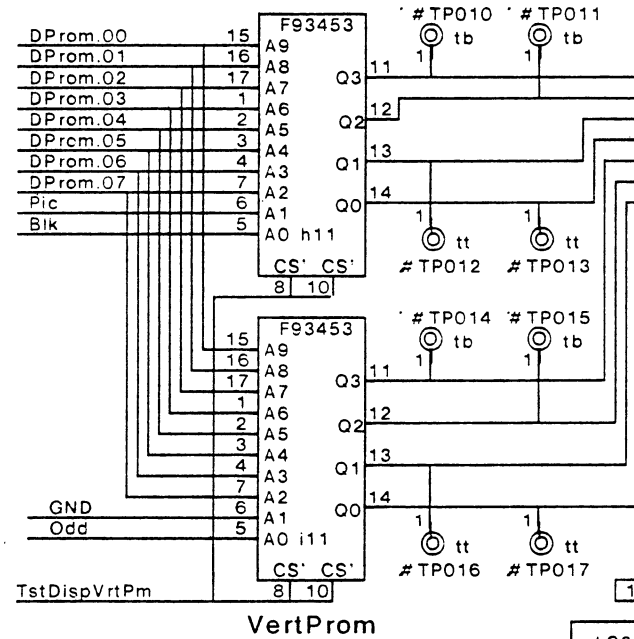
Note: The prefix #% in front of chip position causes the chip to be wired upside down in socket. This prevents cutting of ground connections on stitchweld card. The suffix ! prevents Route from attempting automatic terminator assignment since DO stitchweld card has none defined. Subnet wiring order for a net is done by appending to the net name a ! followed by the wiring sequence number of the node in the net. Automatic terminator assignment is inhibited by use of ! as the last character in the character string of the net. This must occur after the subnet feature if it is also being used.



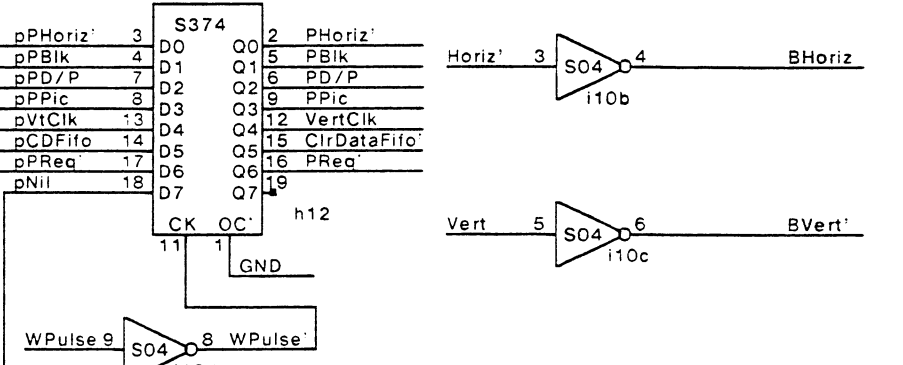




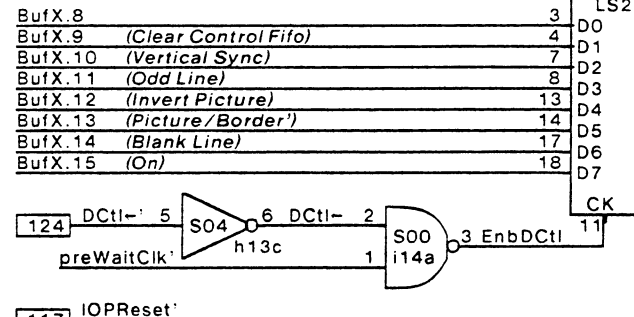
Display PROM



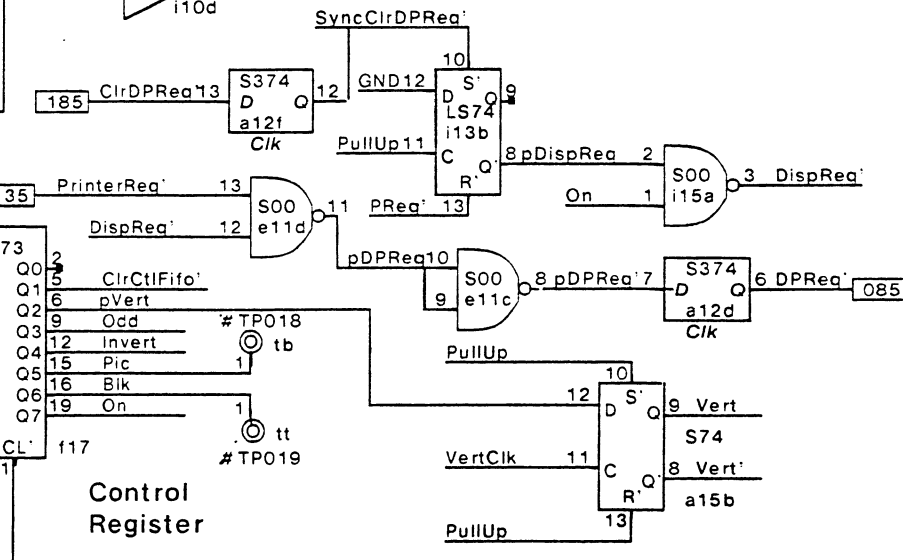
Prom Register



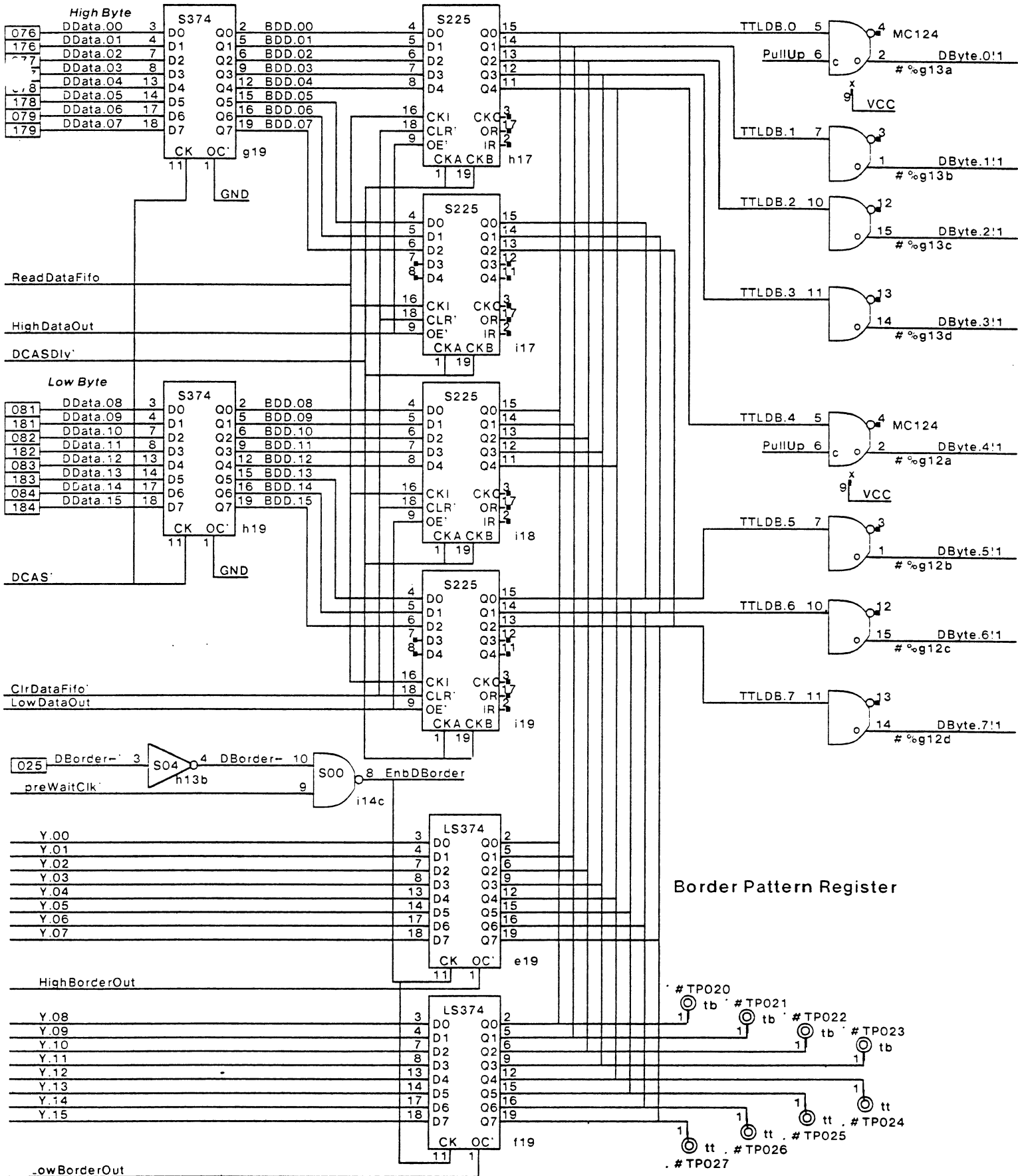
VertProm



Control Register

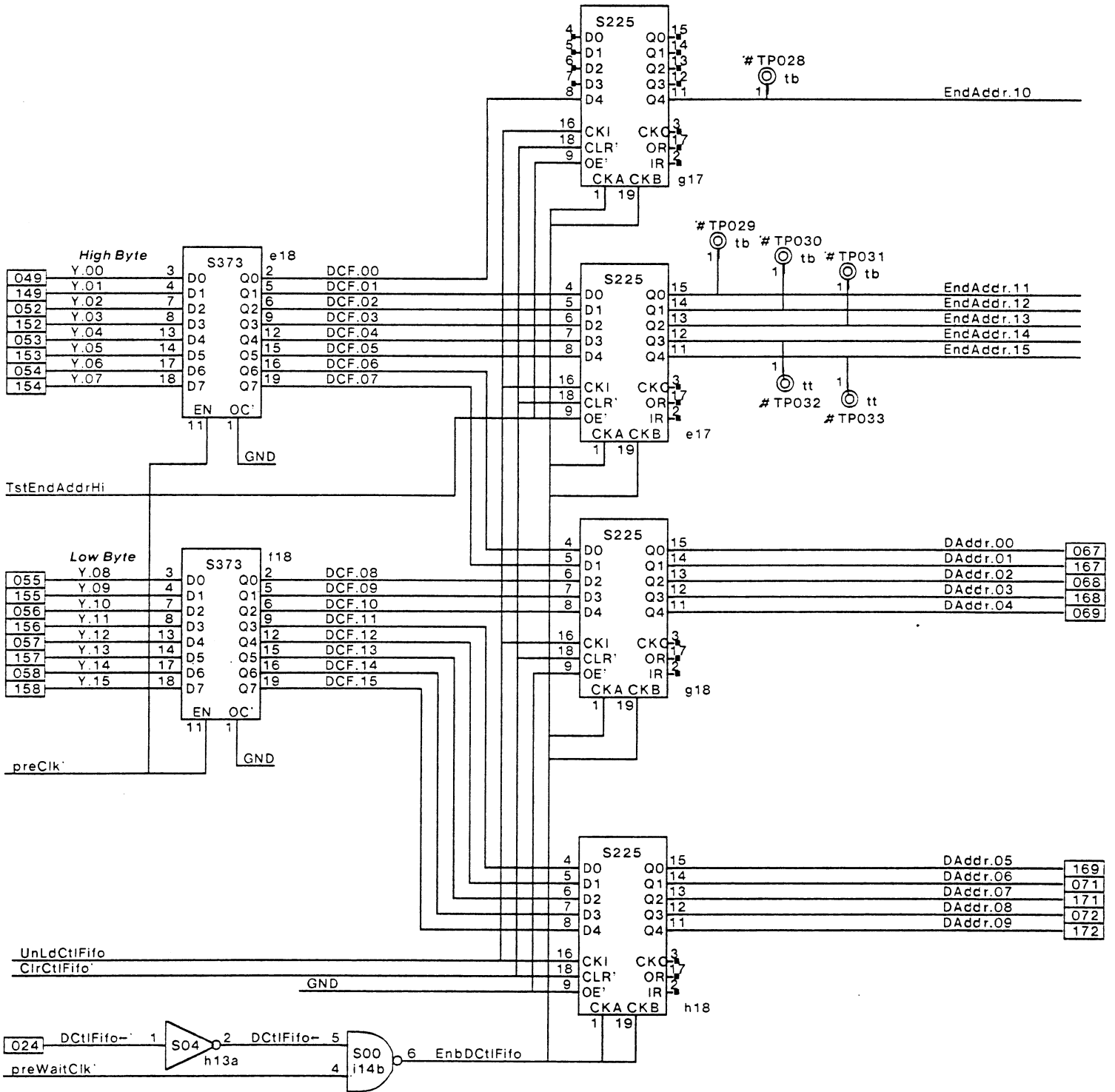


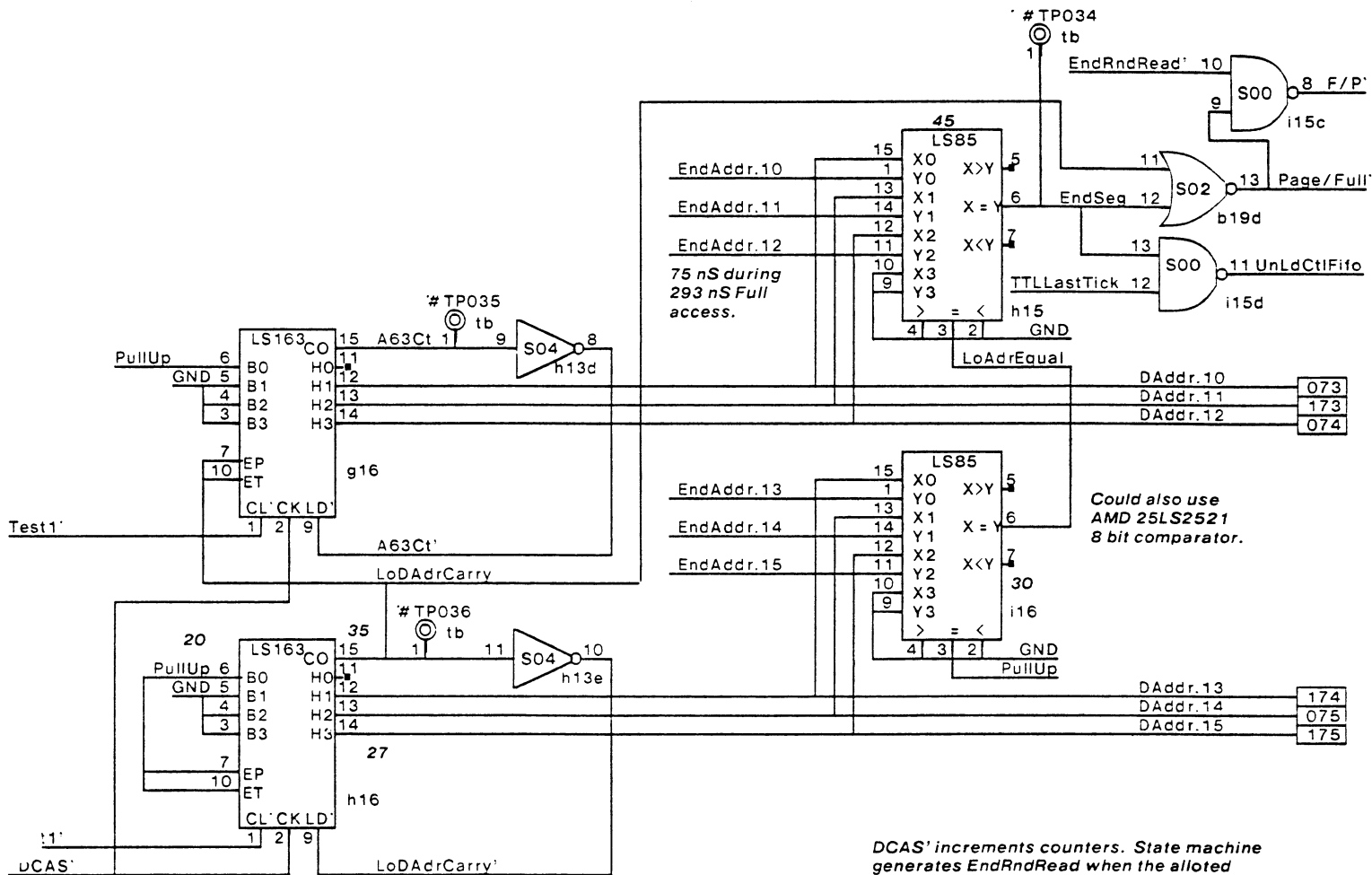
Terminators shown on clock page.



EndLine goes low once per horizontal line.
 DCASDiv' is DCAS' delayed by 20 nS.
 Read signal goes low for 20 nS before low data byte is latched by the shift register.

XEROX SDD	Project WS	Data FIFO and Border Register	File sHSIO25.sil	Designer Crane	Rev R	Date 10/22/80	Page 25
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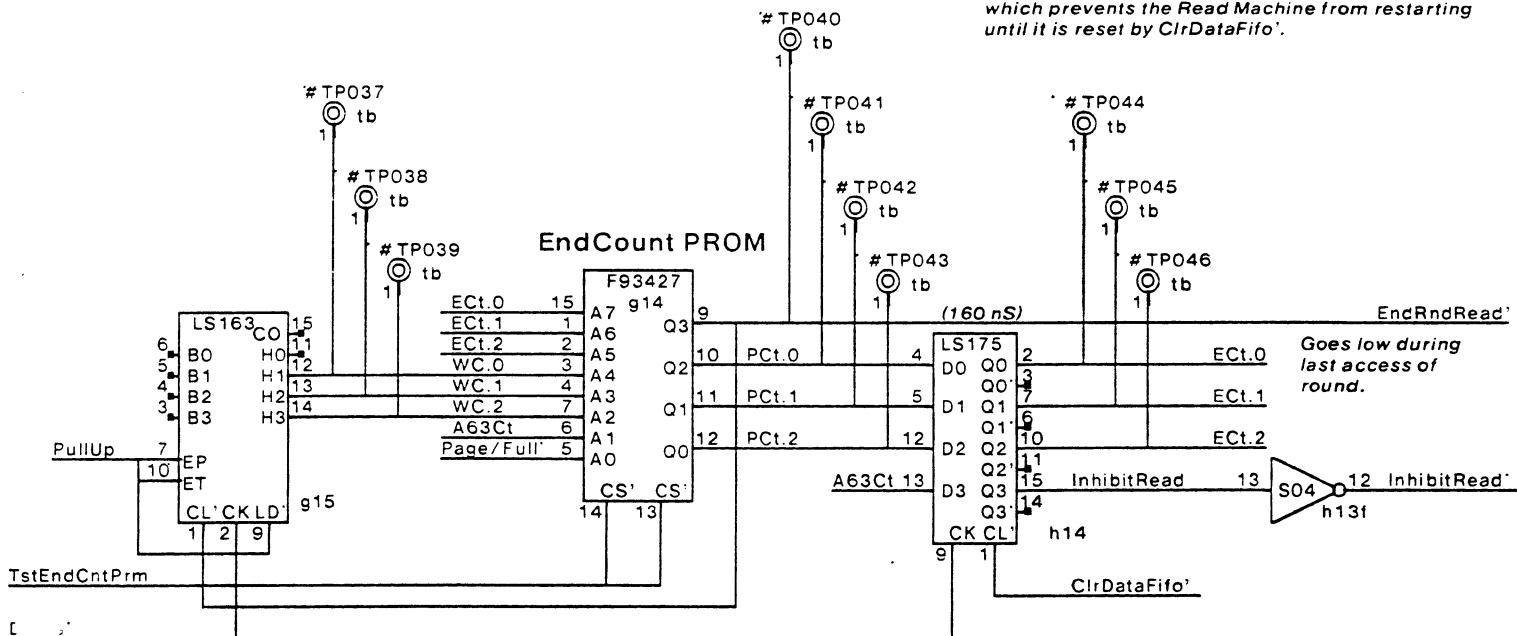




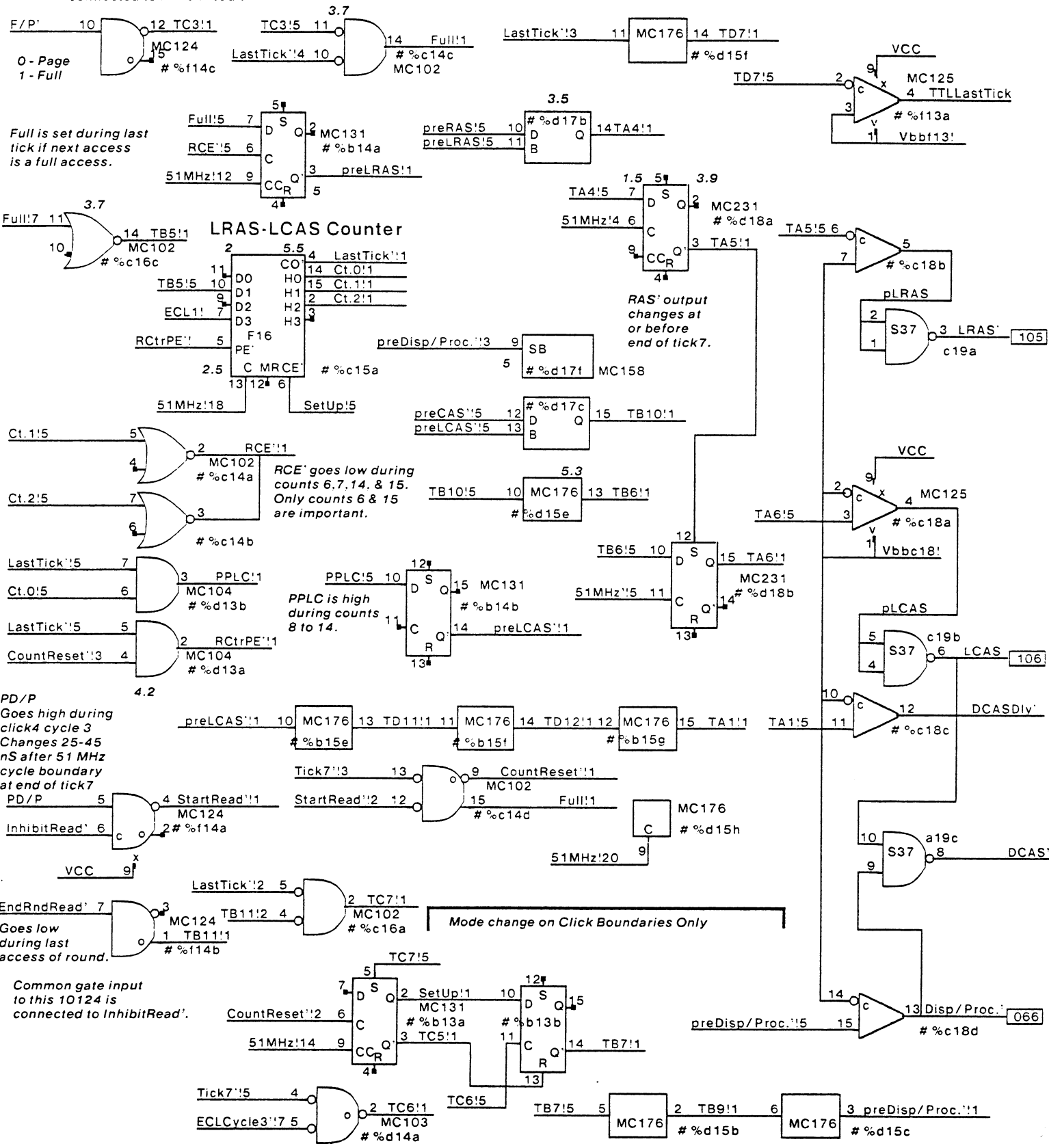
DCAS' is active only when Disp/Proc.' is high.

DCAS' increments counters. State machine generates EndRndRead when the allotted number of accesses for the mix of page and full accesses has been reached for a given round (4 clicks out of 5). Page/Full' goes low whenever the conditions for a full access are met.

When the word counter reaches 63, it resets to 0 and the InhibitRead signal is asserted, which prevents the Read Machine from restarting until it is reset by ClrDataFifo'.



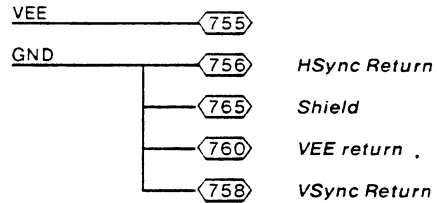
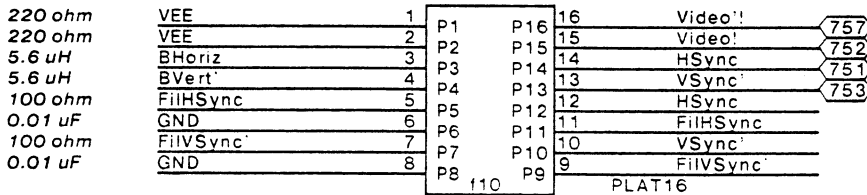
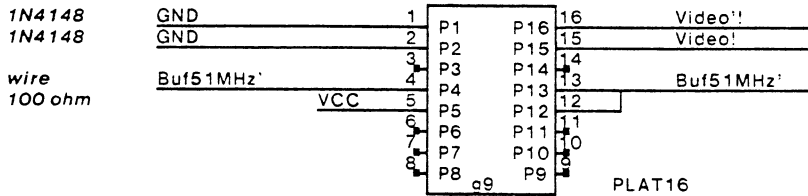
Common gate input to this 10124 is connected to InhibitRead'.



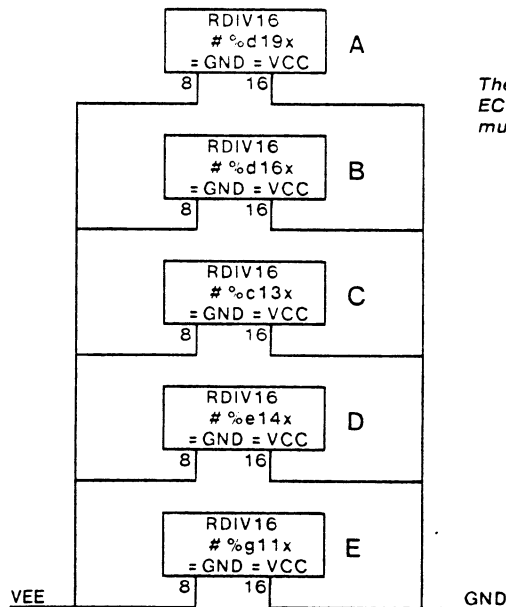
Terminators are shown on the clock page.

XEROX SDD	Project WS	LCAS & LRAS' Generation	File sHSIO28.sil	Designer Crane	Rev R	Date 10/22/80	Page 28
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This is a platform of discretes used to filter the video, Hsync and VSync signals

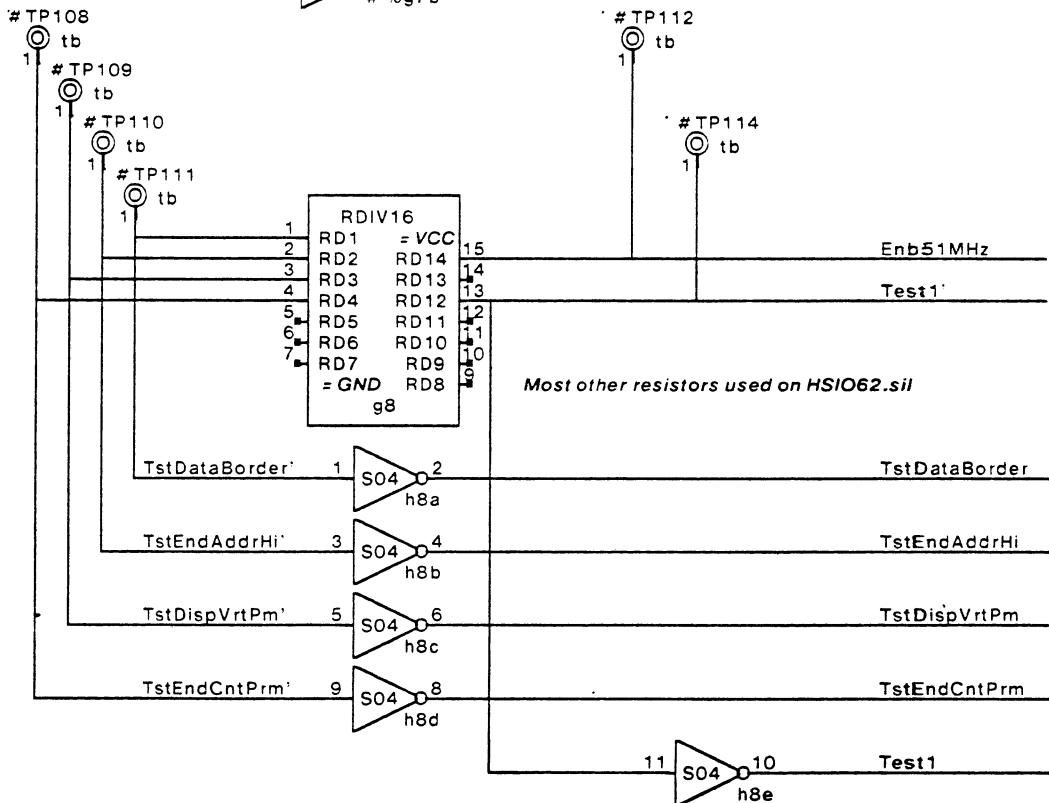
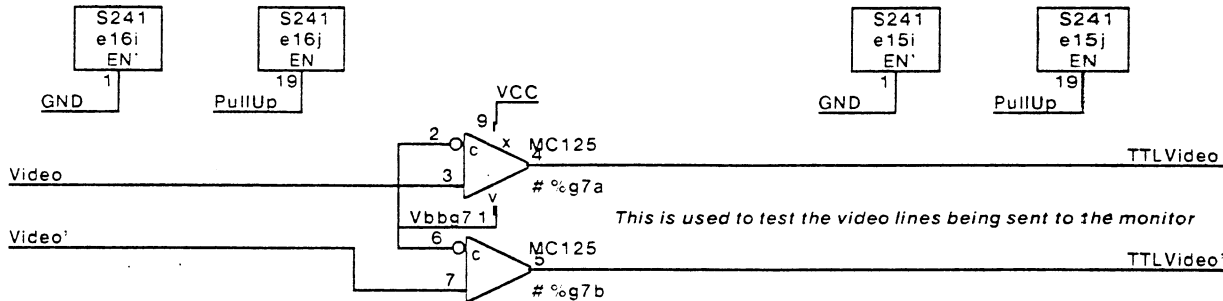
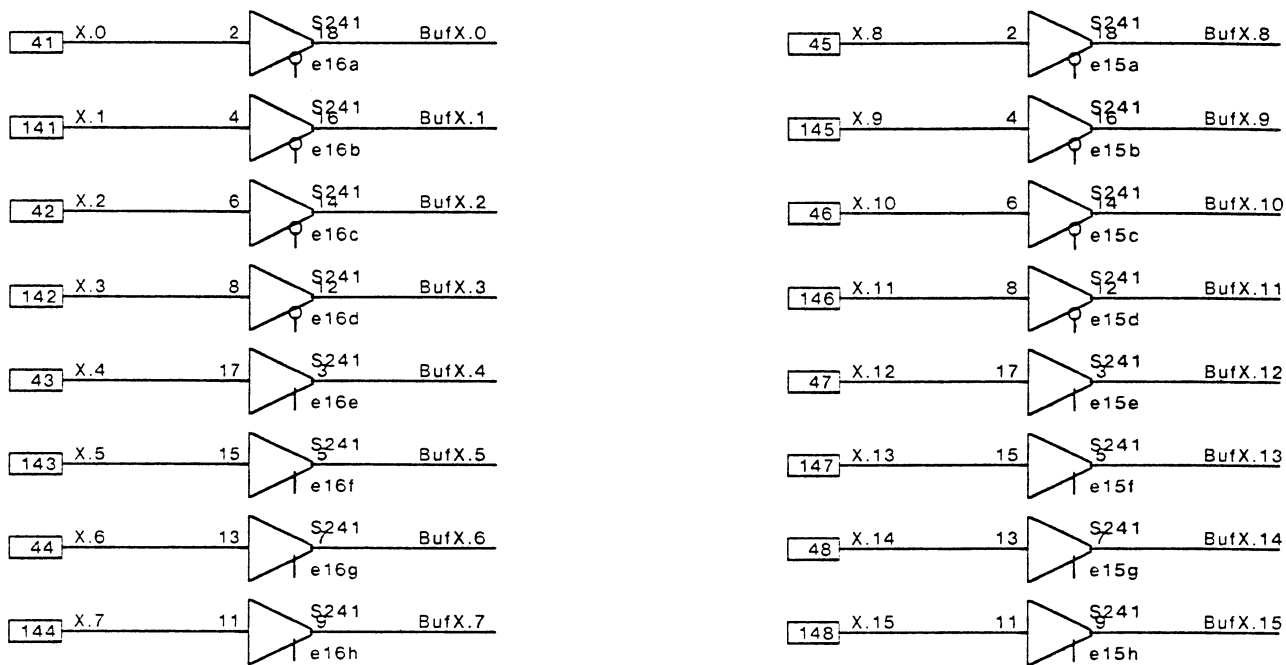


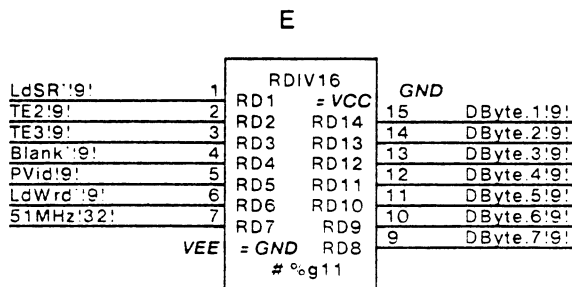
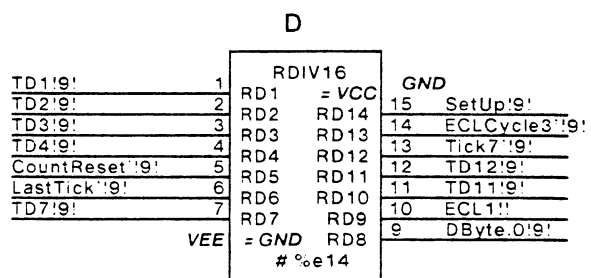
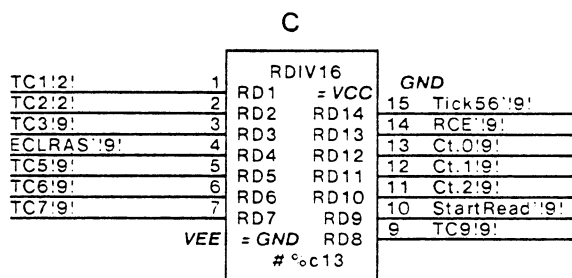
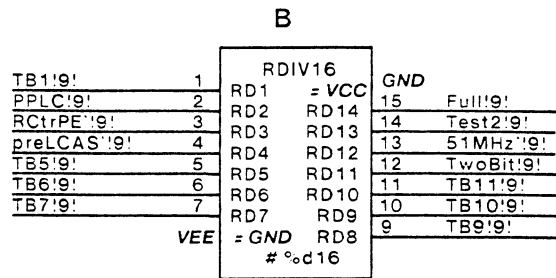
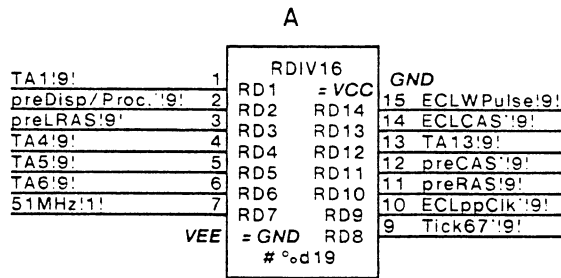
The connector is a 15 pin Female D connector located on the bottom edge of the card. The pin numbers shown are the actual pin number + 750.



These RDIV16's are being used as ECL terminators, so their power connections must change to reflect ECL conventions.

Buffer X bus to reduce loading.

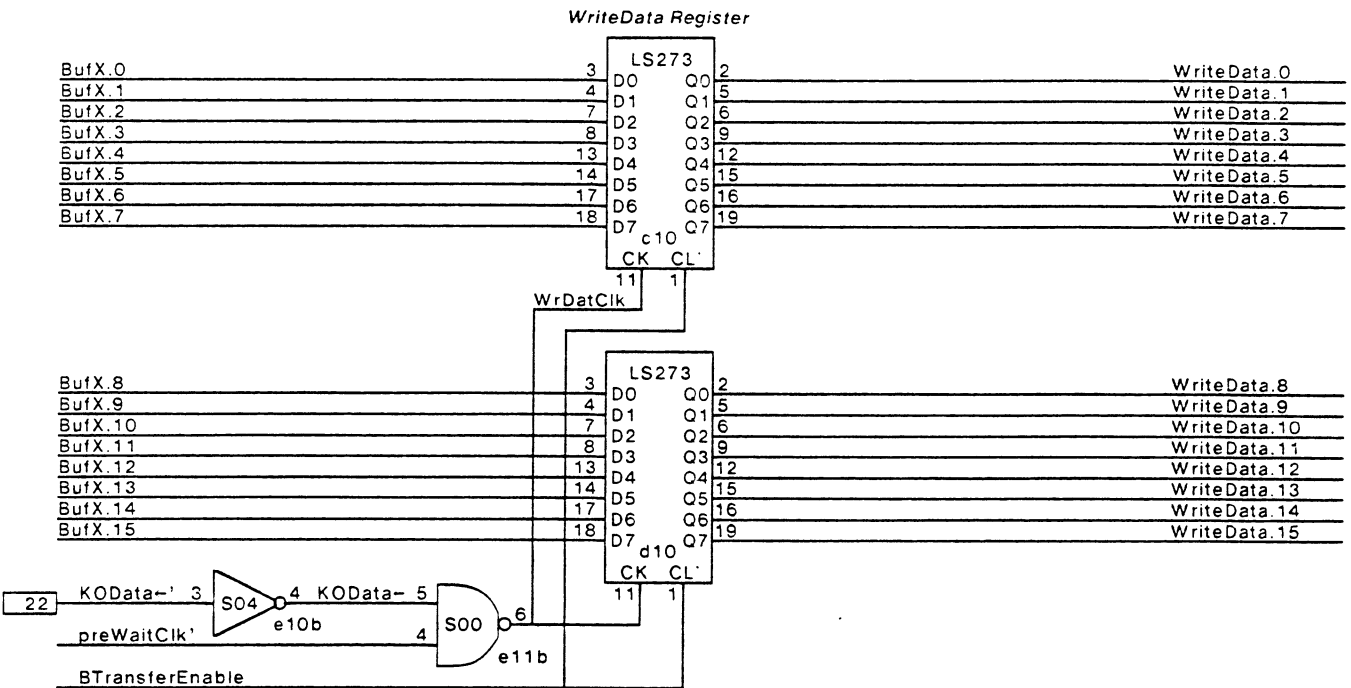
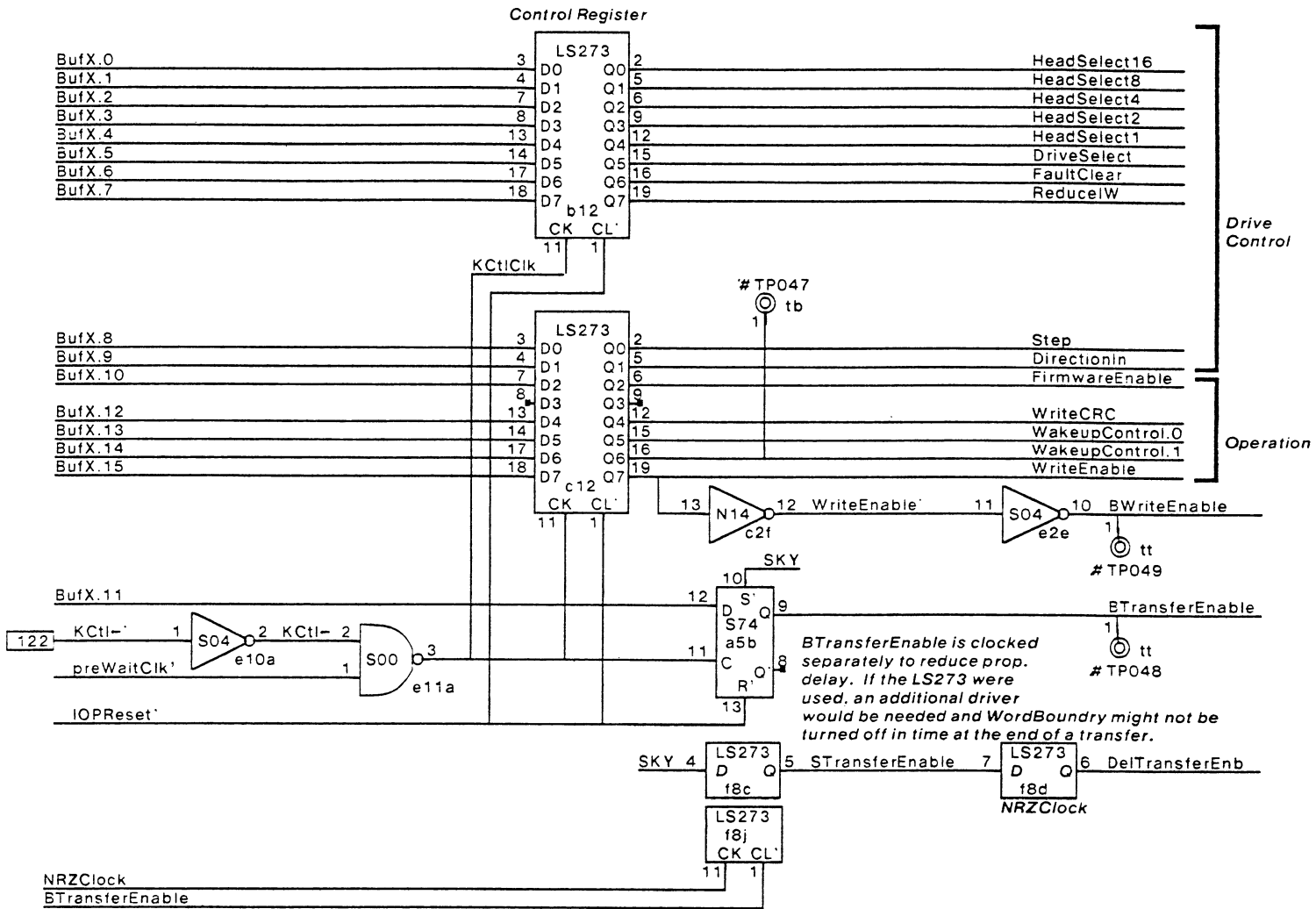




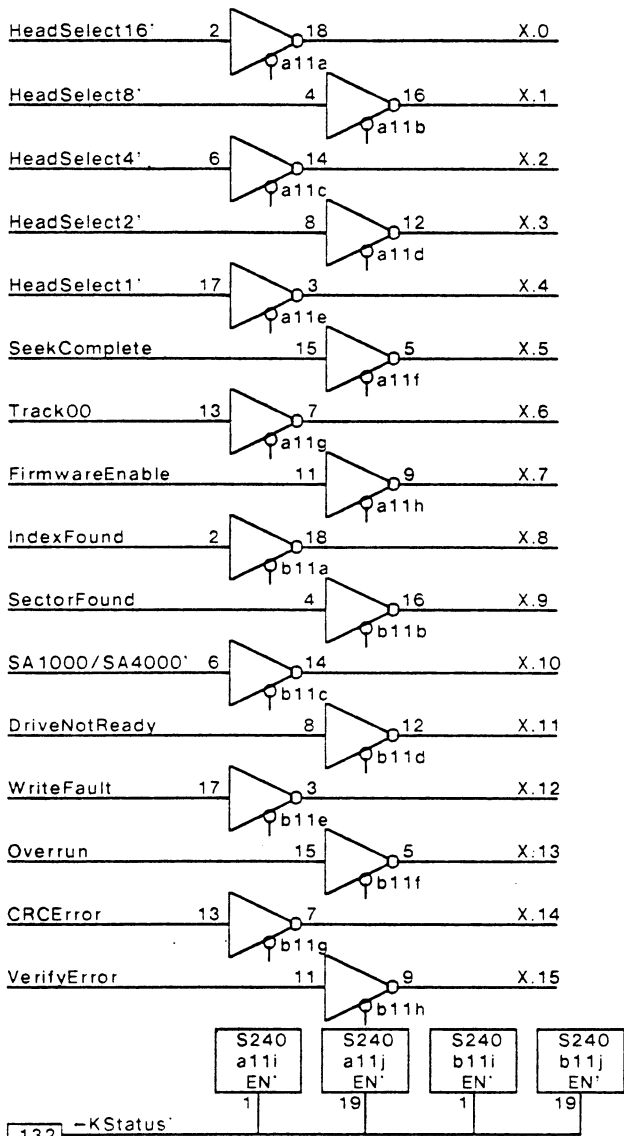
Termination Packages A. B. C. D. E above are 100 ohm termination to -2 V Allen-Bradley part no. 316E161261

Pin 16 on each termination package is connected to GND and Pin 8 to VEE (-5.2 V). This is done on pWSD09.sil and sWSD09.sil where there is more room. This connection make the termination compatible with normal ECL power rules.

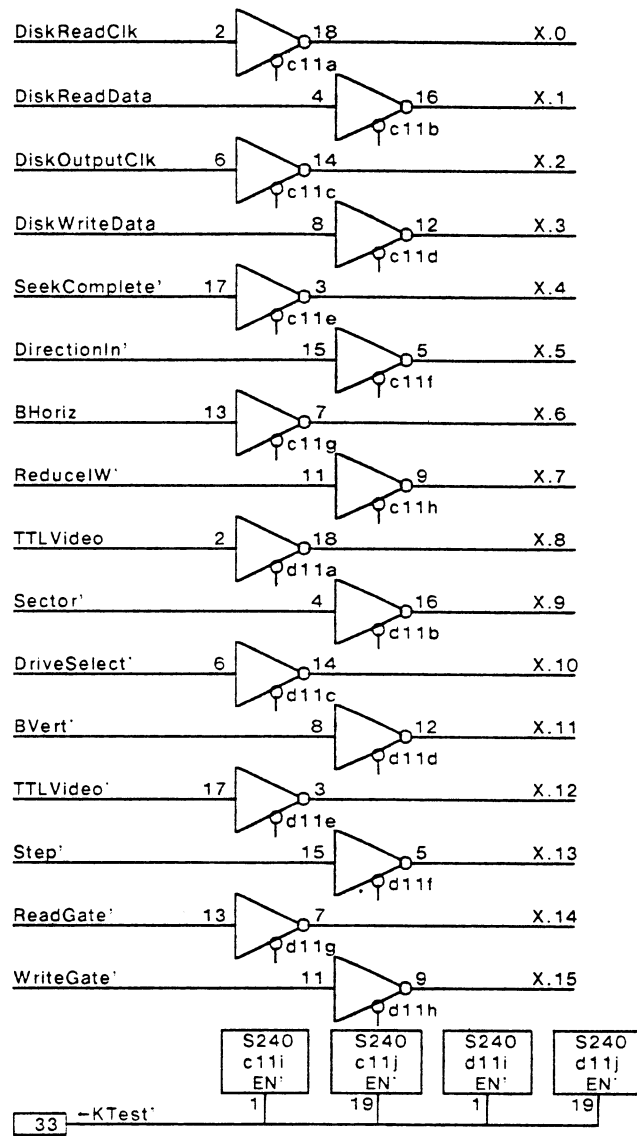
Note: The prefix #% in front of chip position causes the chip to be wired upside down in socket. This prevents cutting of ground connections on stitchweld card. The suffix ! prevents Route from attempting automatic terminator assignment since DO stitchweld card has none defined. Subnet wiring order for a net is done by appending to the net name a ! followed by the wiring sequence number of the node in the net. Automatic terminator assignment is inhibited by use of ! as the last character in the character string of the net. This must occur after the subnet feature if it is also being used.



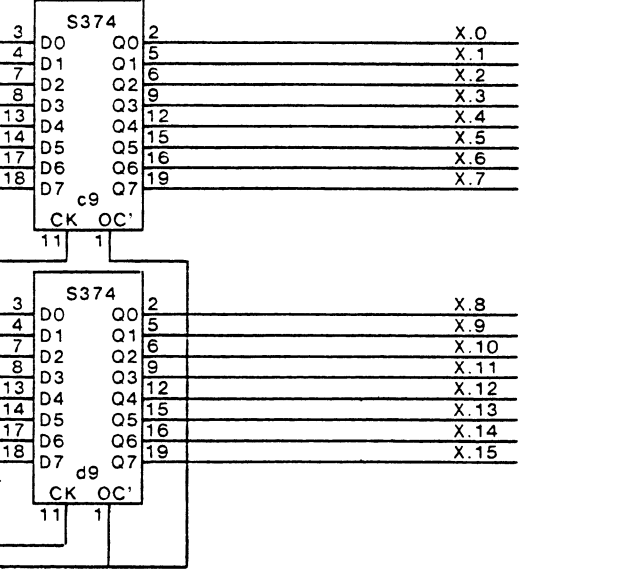
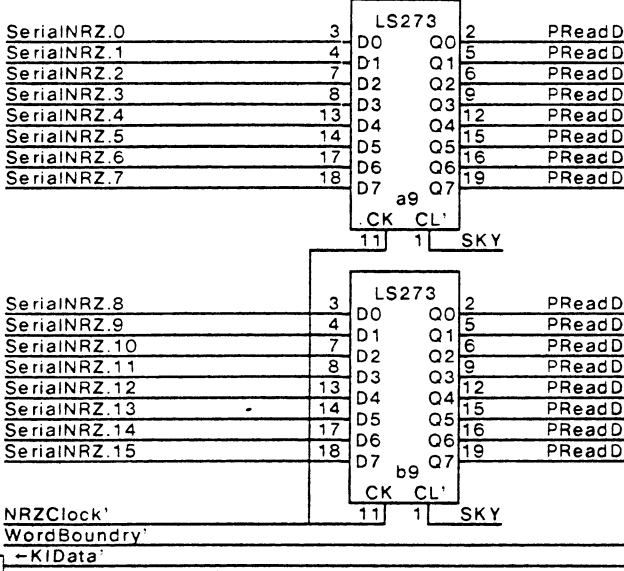
Status/Test Multiplexer

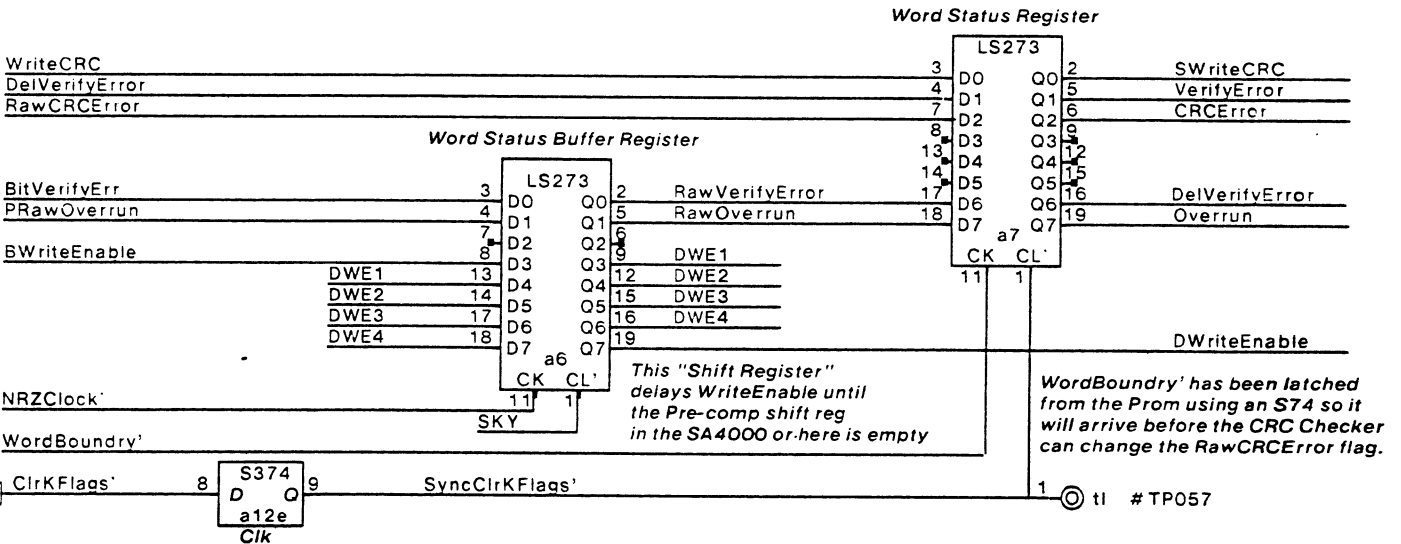
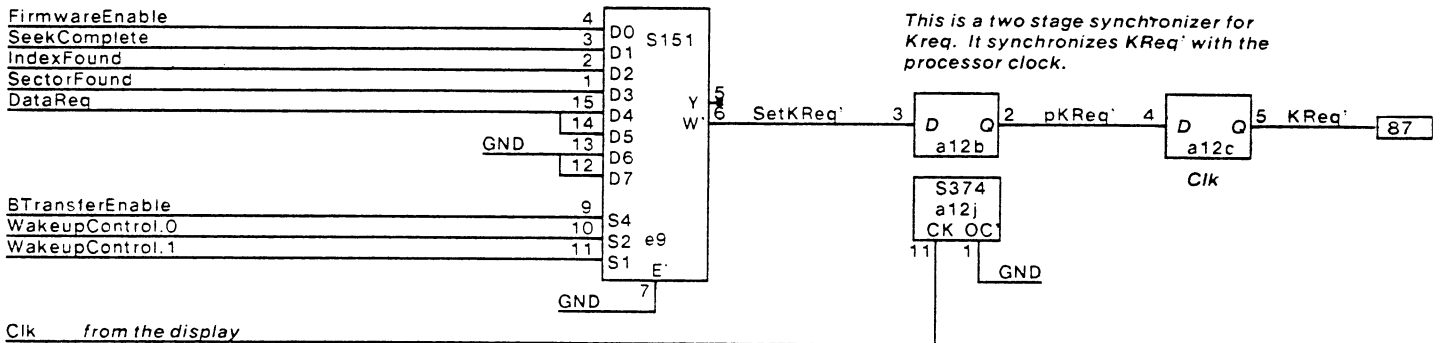
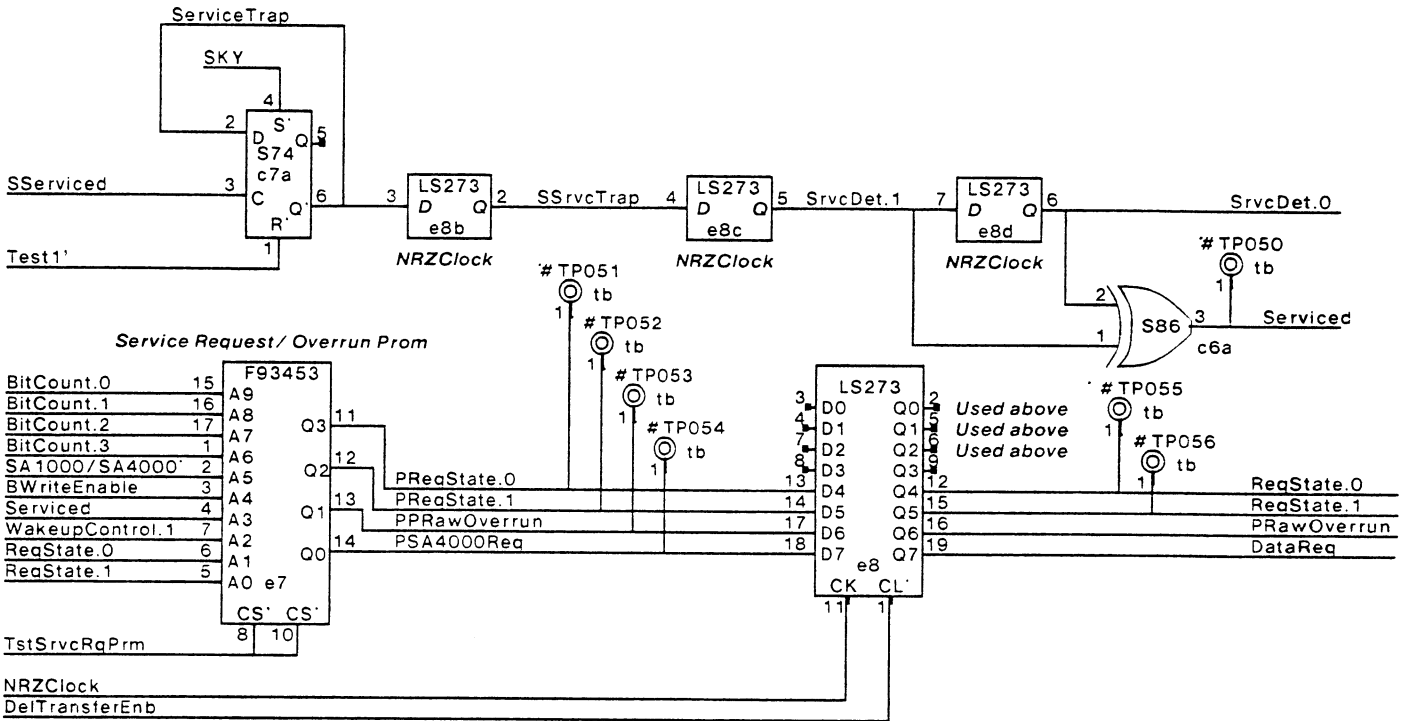
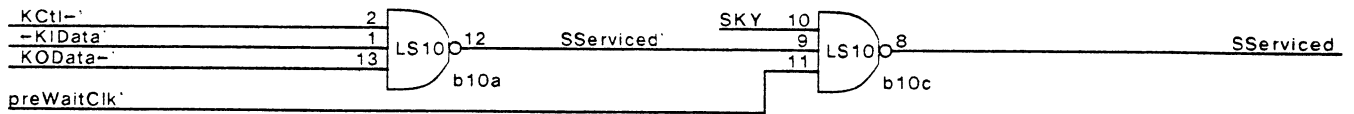


ReadData Buffer Register

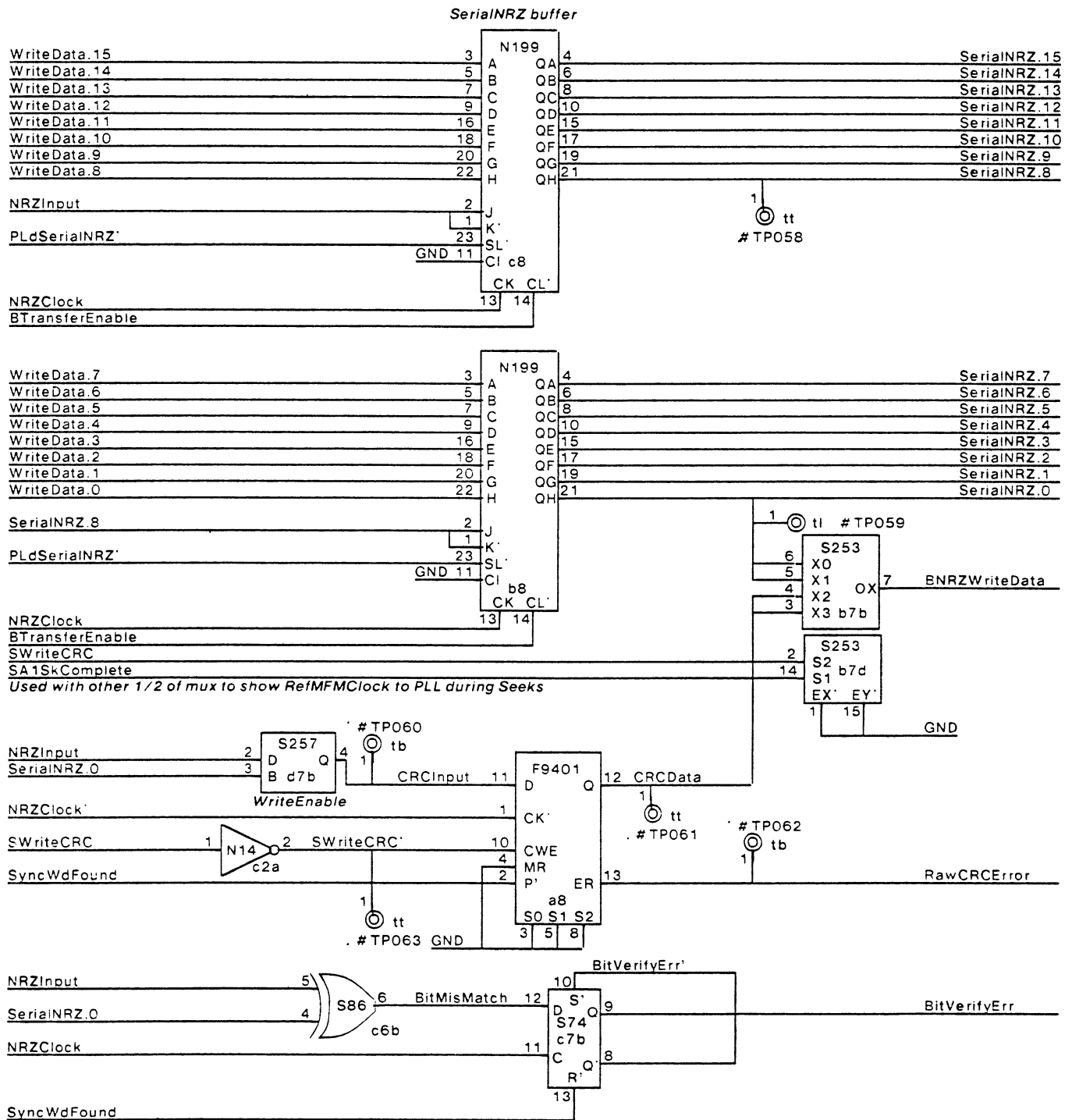


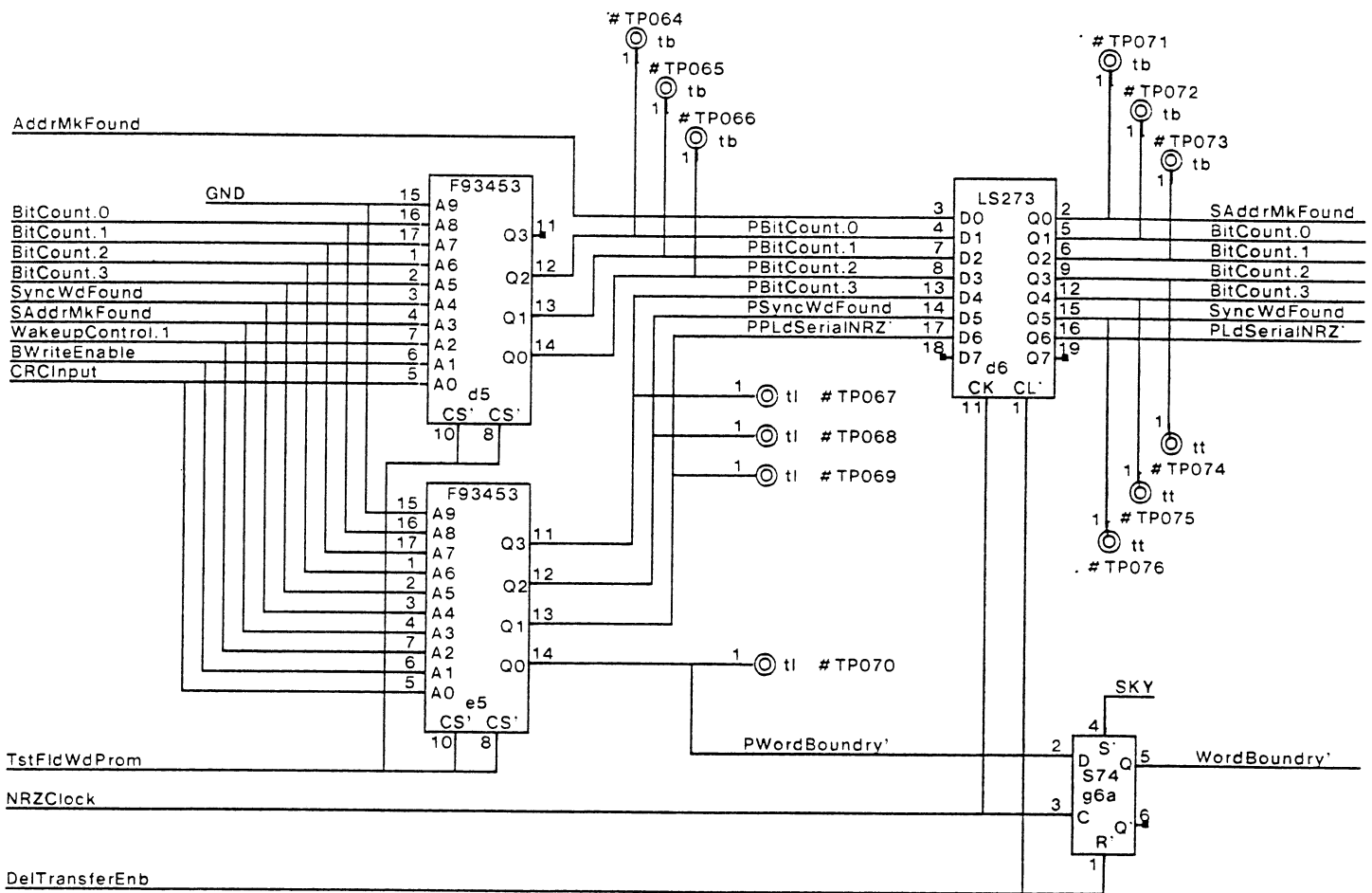
ReadData Register





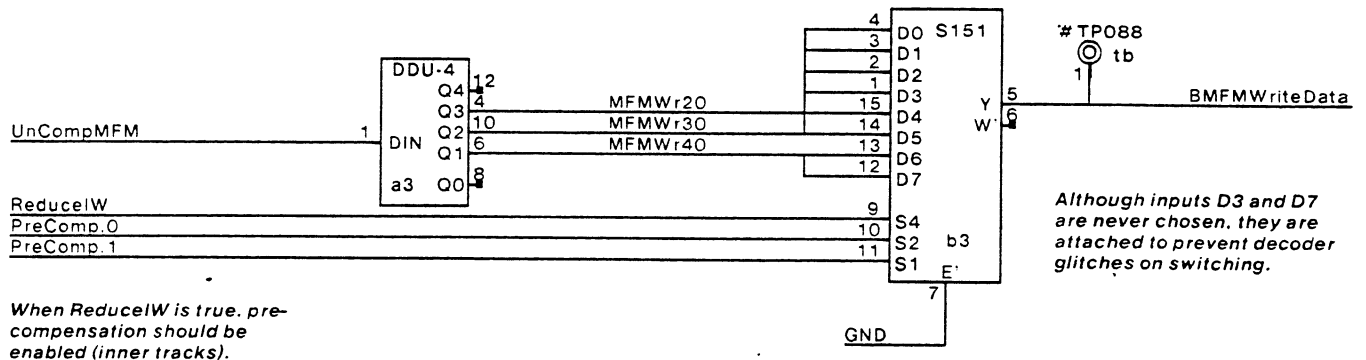
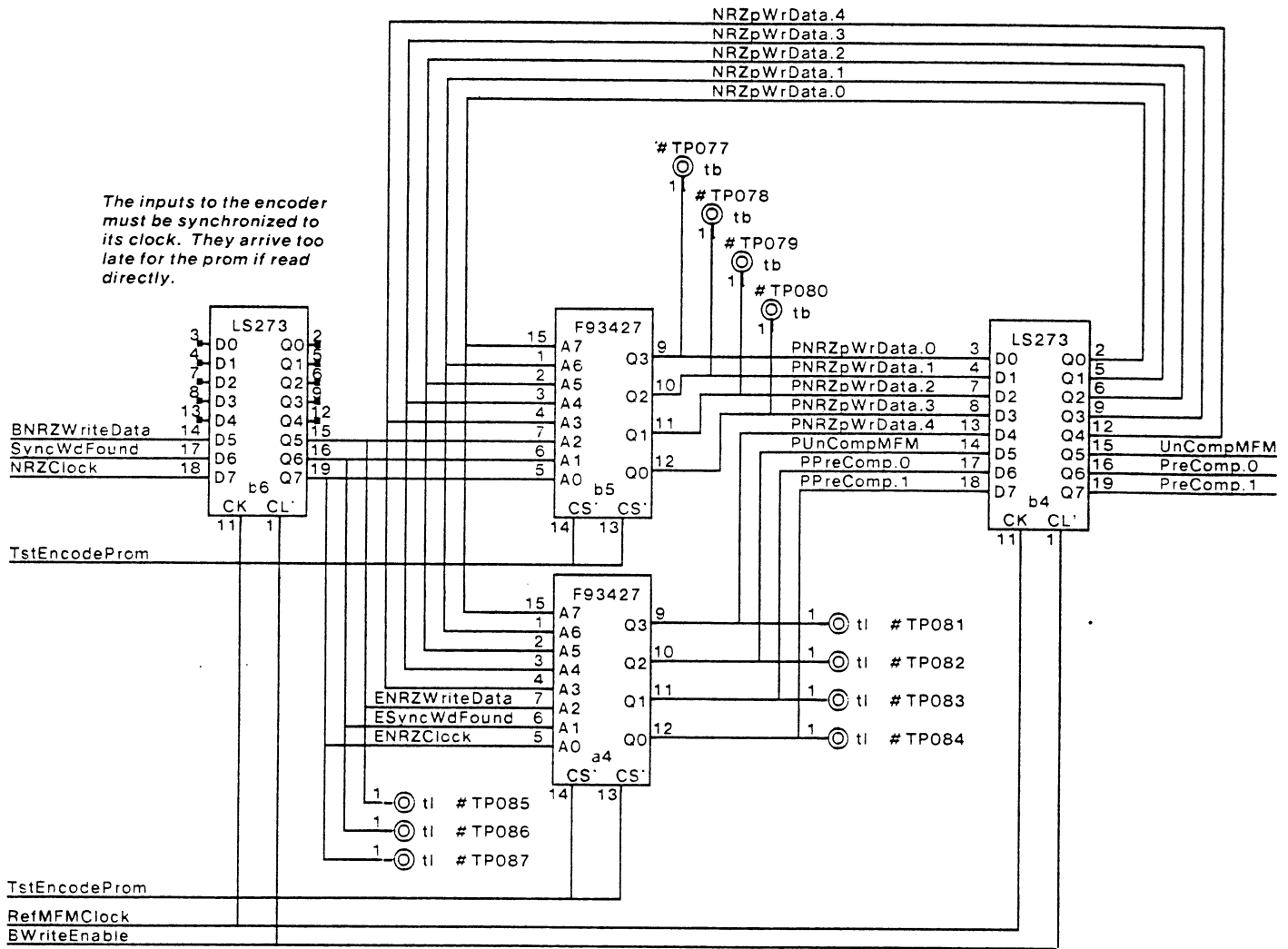
SerialNRZ Shift Register and Error Checking

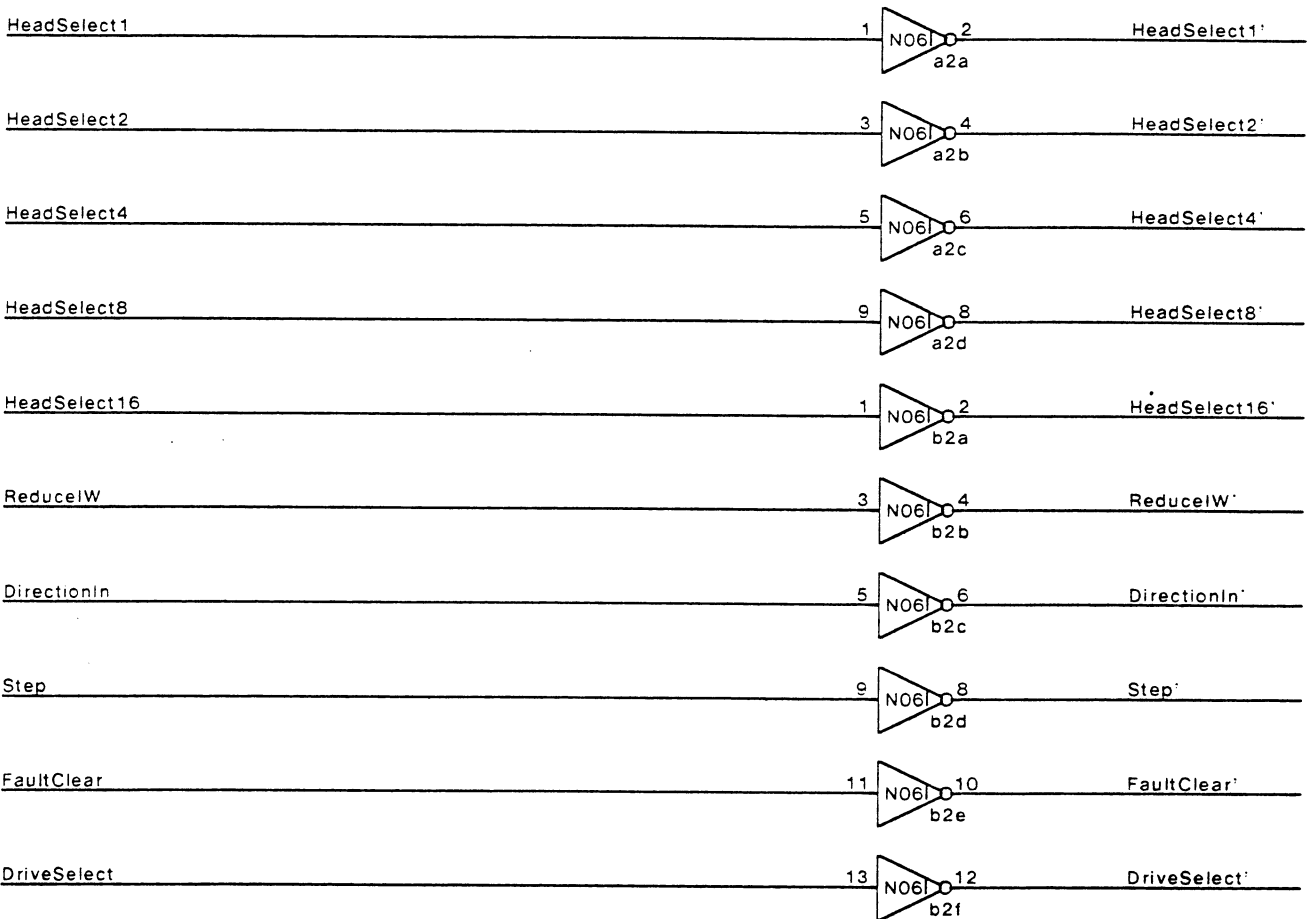
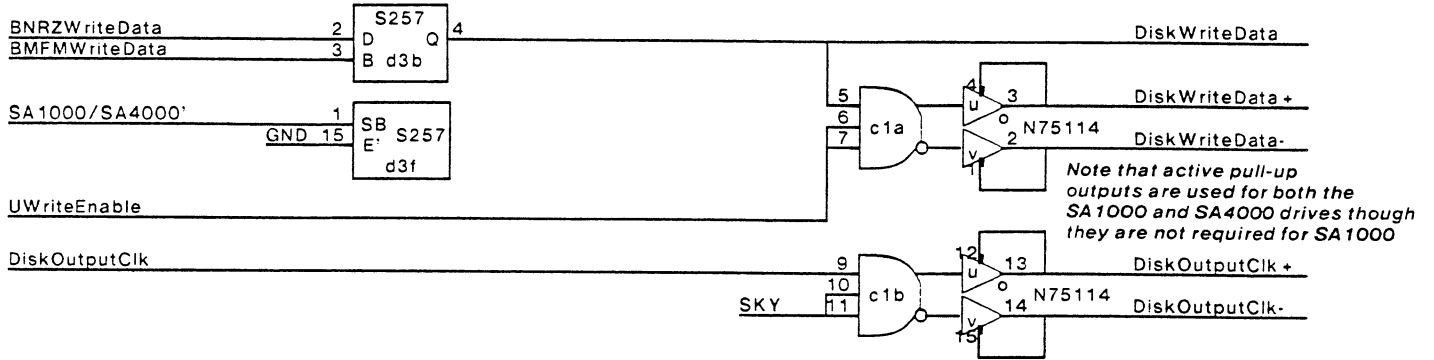




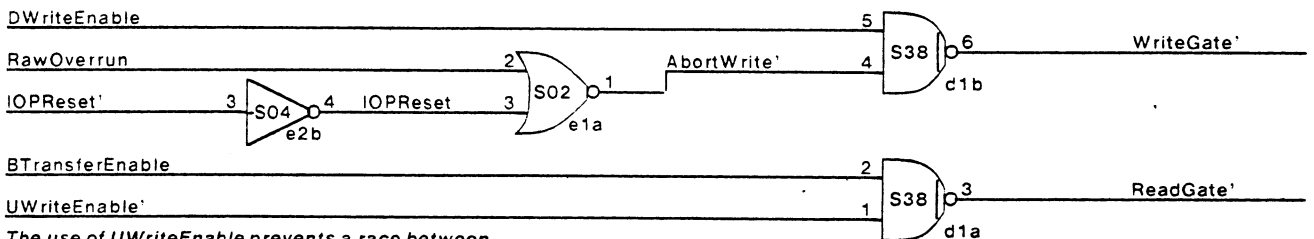
Using an S74 instead of the LS273 speeds up WordBoundary' so it will change before the RawCRCError indicator from the 9401 CRC Checker. This allows us to latch the CRCError signal directly using WordBoundary'. The RawCRCError signal is too slow to latch into the Word Status buffer register using NRZClock'. There is then a race between WordBoundary' and RawCRCError after NRZClock rises. Using the faster S74 here ensures WordBoundary' wins.

XEROX SDD	Project	Dandelion Disk Controller	File	Designer	Rev	Date	Page
	Dandelion	Field and Word State Machine	sHSIO51.sil	Davies	R	10/22/80	51



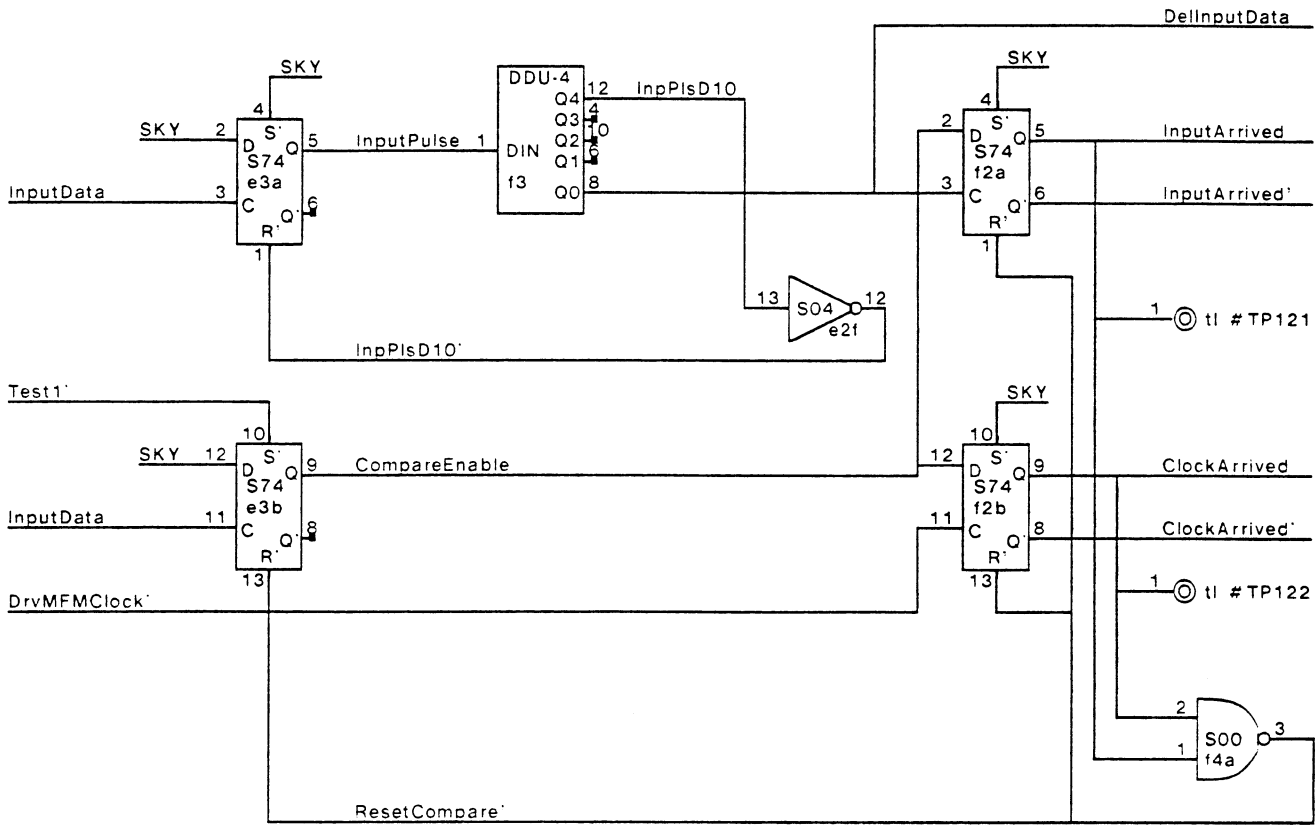


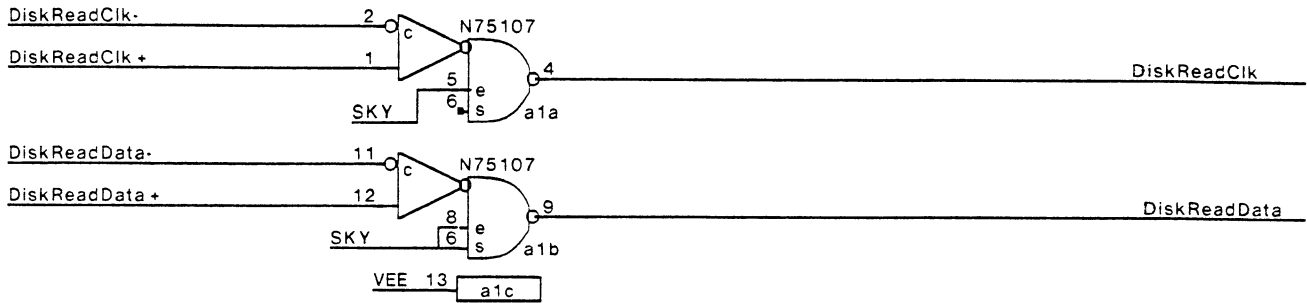
DWriteEnable is delayed 5 bit times to let Pre-comp shift reg clear out at end of write operation.



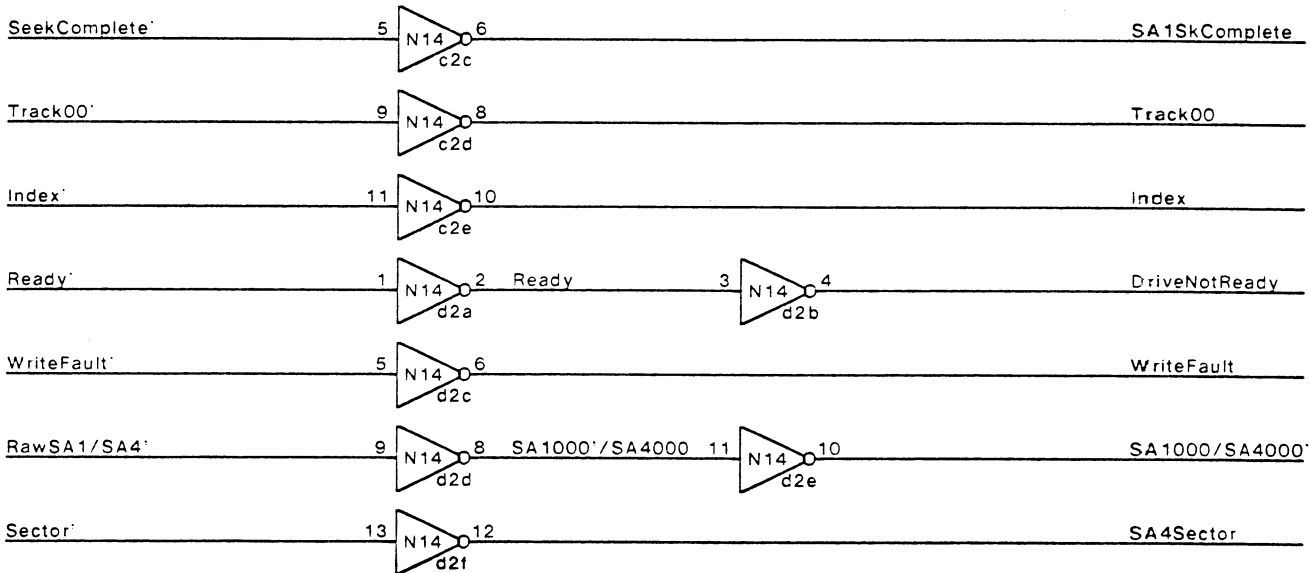
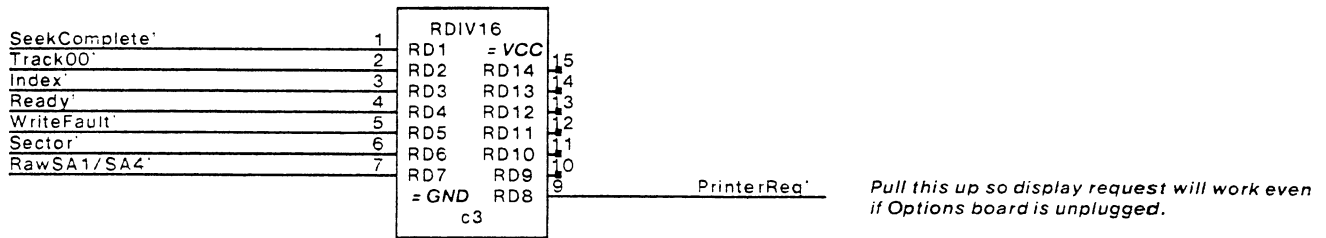
The use of UWriteEnable prevents a race between WriteGate' and ReadGate'. If BWriteEnable were used, there would be a race between BTransferEnable and BWriteEnable when finishing a write op that could glitch ReadGate', causing a WriteFault. Since BTransferEnable is faster than UWriteEnable, there is a ~20 ns glitch in ReadGate' at the beginning of a Write Op. This causes NRZClock to pause, but only temporarily.

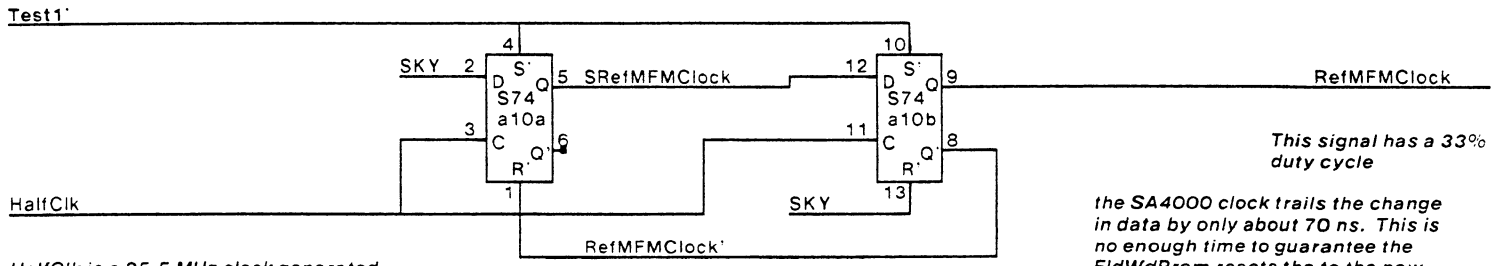
XEROX SDD	Project Dandelion	Dandelion Disk Controller Disk Output Buffers, Drivers	File sHSIO53.sil	Designer Davies	Rev R	Date 10/22/80	Page 53
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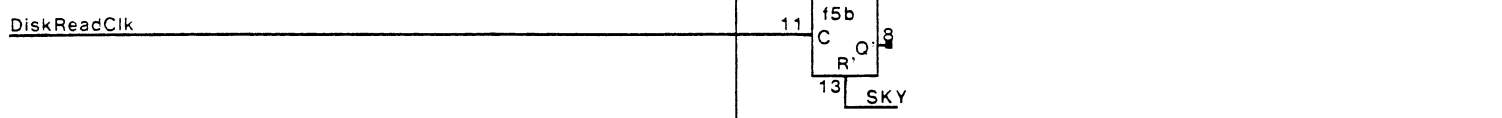
This is a Beckman RPack number
898-5-R220/330.



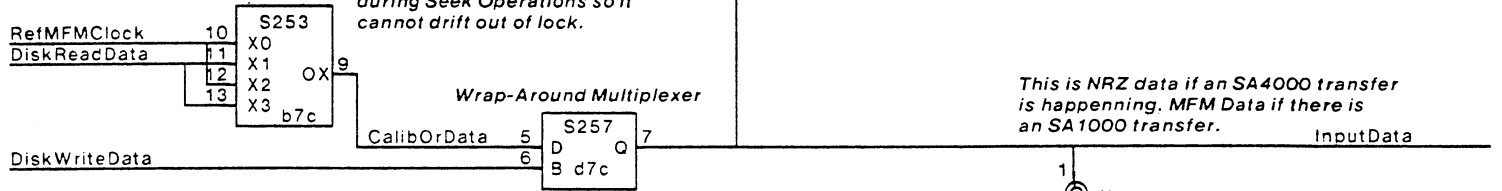


HalfClk is a 25.5 MHz clock generated in the CLOCKS section of the display. It is divided by three here to produce a 117 ns clock to run the disk.

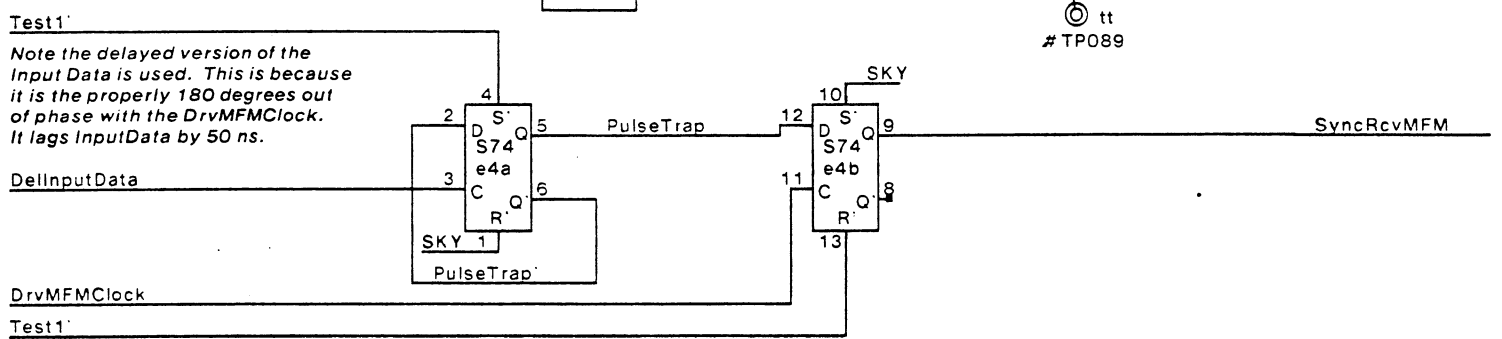
the SA4000 clock trails the change in data by only about 70 ns. This is not enough time to guarantee the FldWdProm reacts to the new data. To fix this, we synchronize the SA4000 data with its clock.



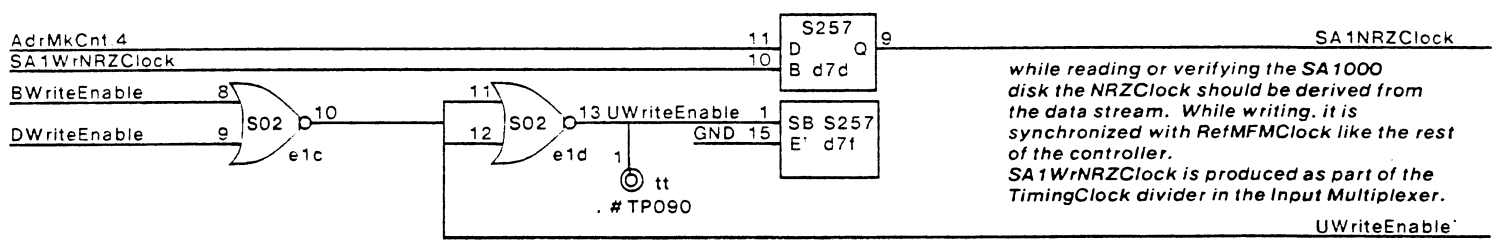
Show Reference clock to PLL during Seek Operations so it cannot drift out of lock.



This is NRZ data if an SA4000 transfer is happening, MFM Data if there is an SA1000 transfer.



Note the delayed version of the Input Data is used. This is because it is the properly 180 degrees out of phase with the DrvMFMClock. It lags InputData by 50 ns.

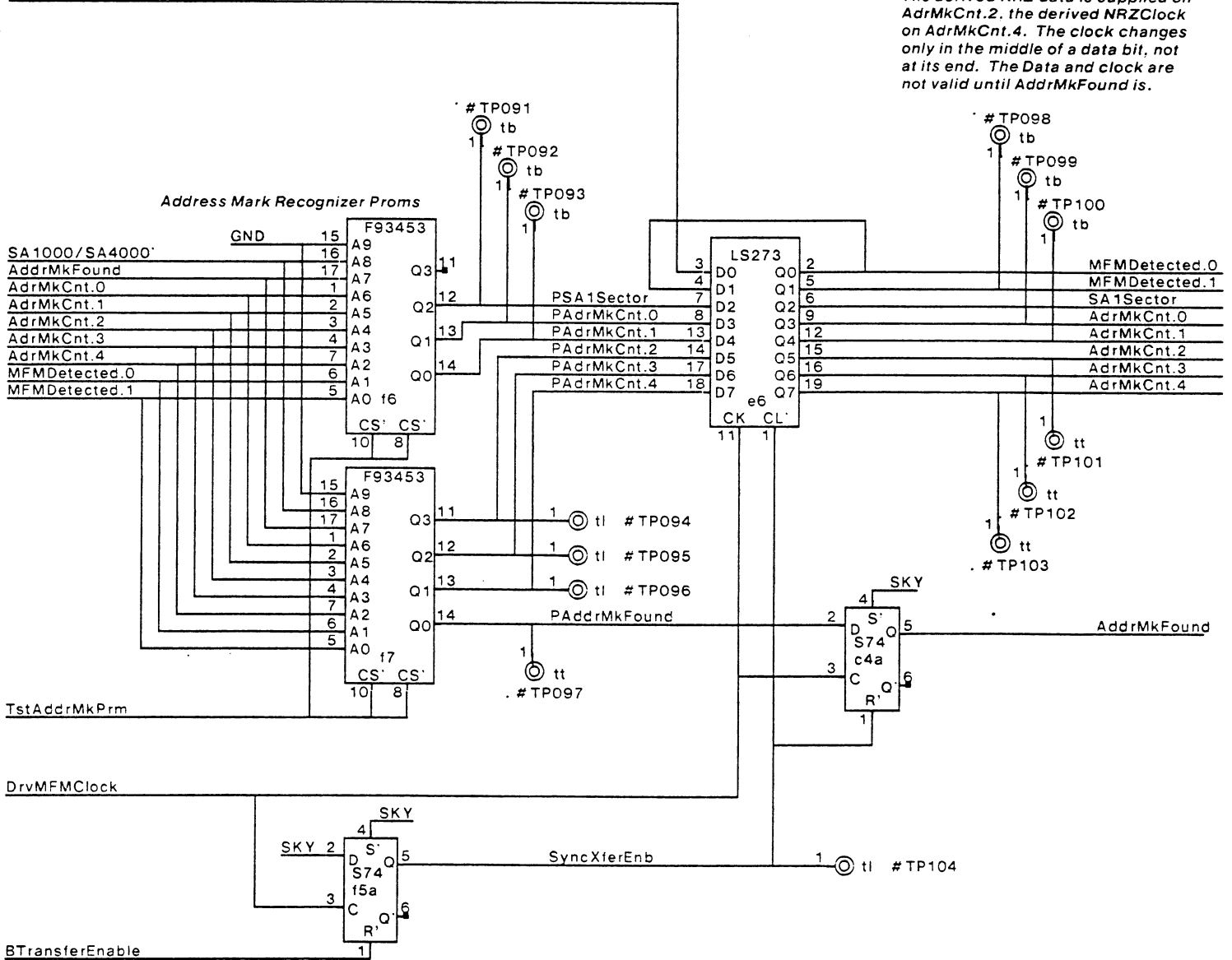


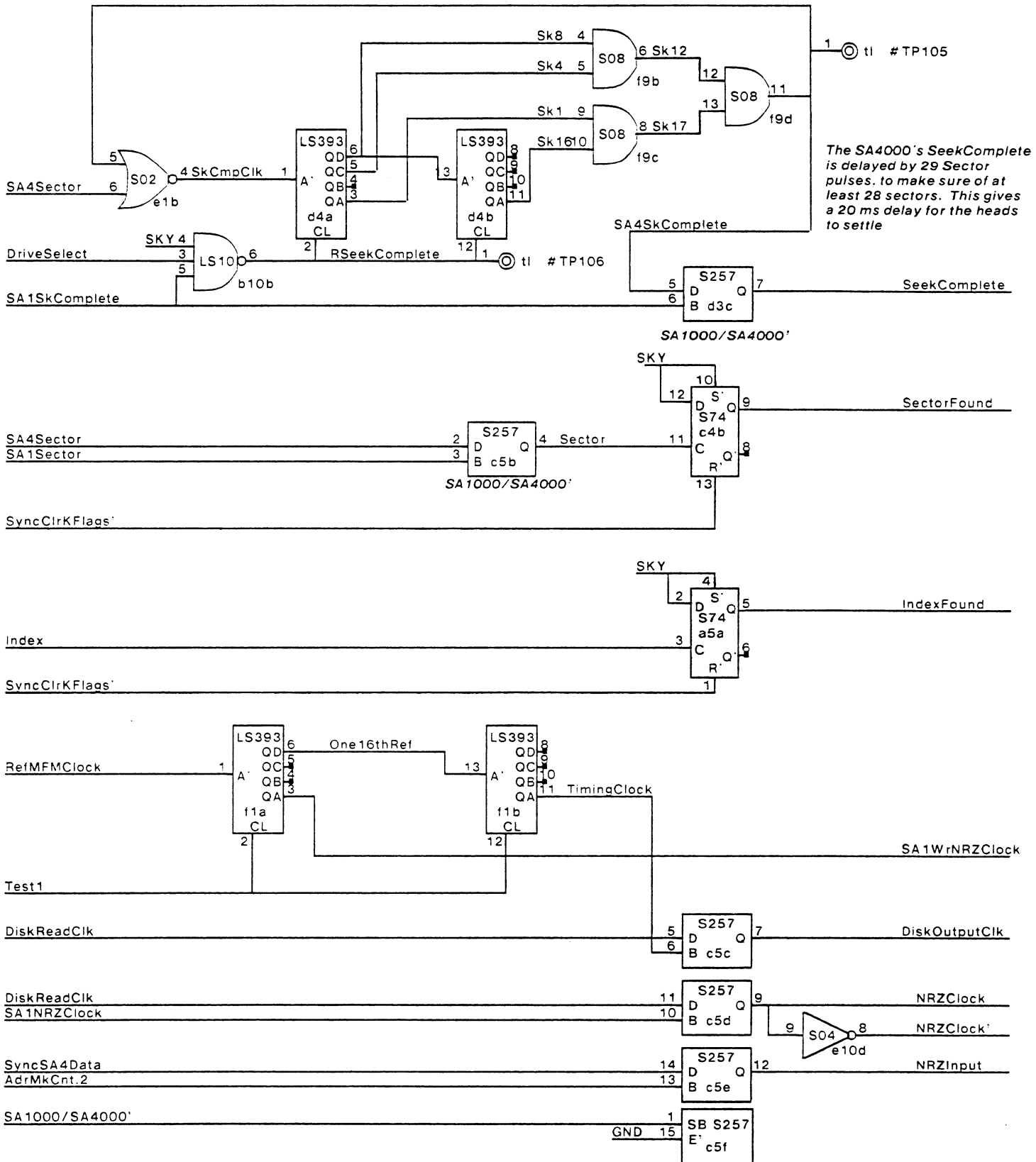
while reading or verifying the SA1000 disk the NRZClock should be derived from the data stream. While writing, it is synchronized with RefMFMClock like the rest of the controller. SA1WrNRZClock is produced as part of the TimingClock divider in the Input Multiplexer.

We note that ADrMkCnt.4 ceases to be active when TransferEnable drops. A clock is needed to start a write operation, so SA1WrNRZClock is set to the always active SA1WrNRZClock as soon as WriteEnable goes active. To ensure the DWriteEnable shift register delay is cleared, we keep SA1WrNRZClock set to SA1WrNRZClock until DWriteEnable goes lo.

SyncRcvMFM

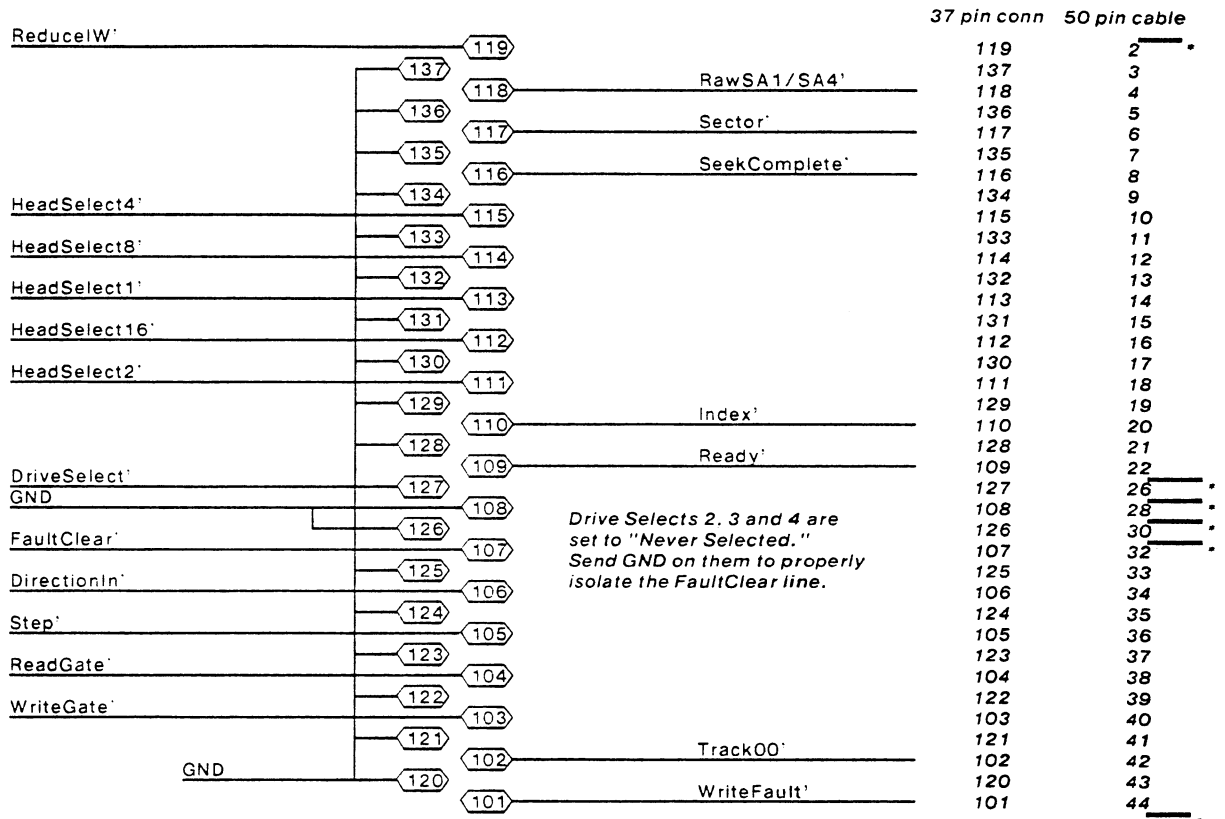
The derived NRZ data is supplied on AdrMkCnt.2, the derived NRZClock on AdrMkCnt.4. The clock changes only in the middle of a data bit, not at its end. The Data and clock are not valid until AdrMkFound is.





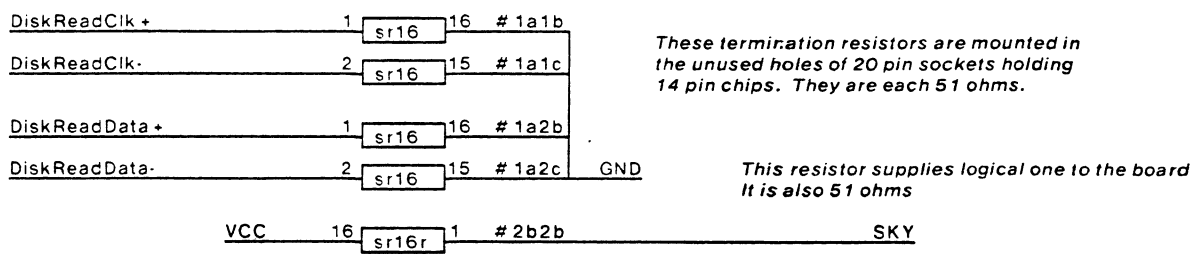
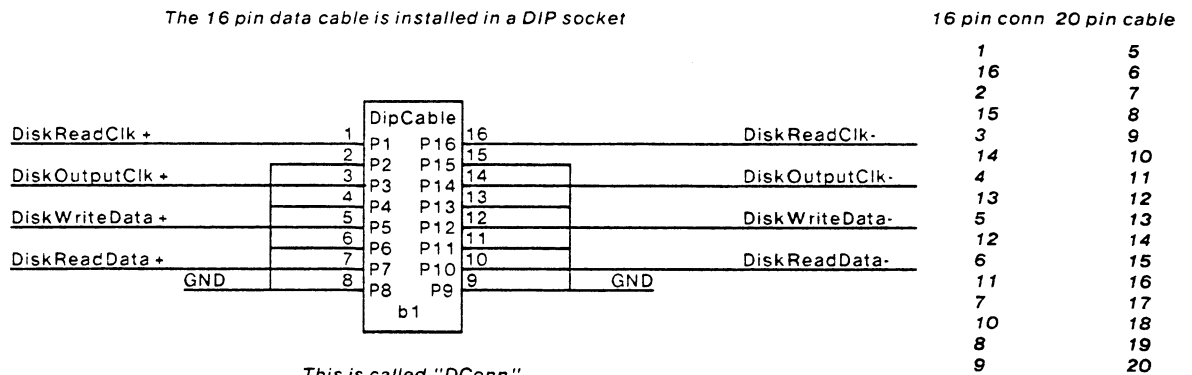
The 50 pin cable to the SA1000 drive has been reduced to 37 lines so the 37 pin connector on the stichweld board may be used.

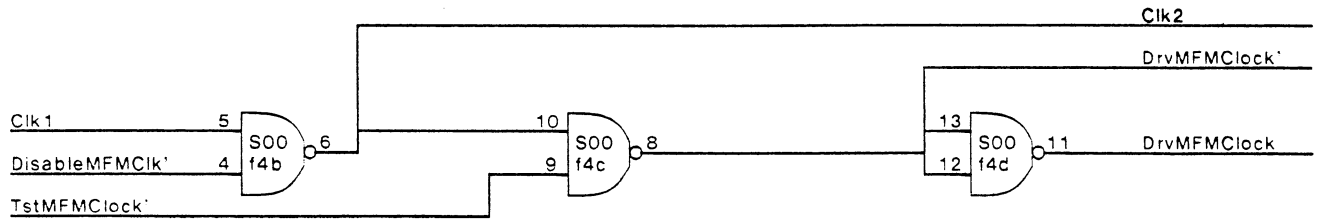
The connector on the stichweld board is a 37 pin female in the TOP position. Its pins are numbered 101-137. Signals not referenced on the drive's 50 pin cable are not connected to the stichweld board.



In addition, GND to pins 1,2,3, 25,27 29, 31 and 45 of 50 conductor cable
 * Breaks in consecutive numbering

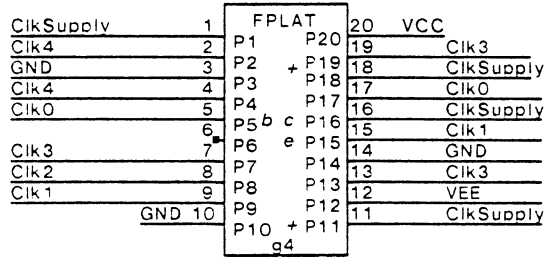
The 16 pin data cable is installed in a DIP socket





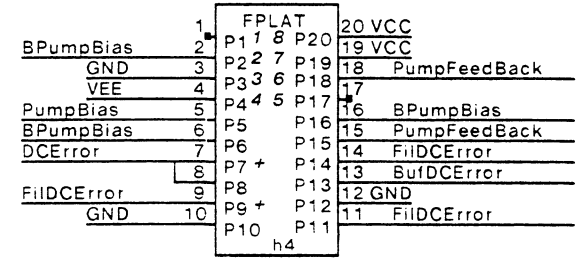
C103 is a 1.0 uF tantalum capacitor

- L101. 22 uH
- L102. 12 uH
- C108. 1.0uF
- R111. 100 ohm
- Q101. 2N5770
- C118. 150 pF
- R110. 470 ohm
- R103. 510 ohm
- C107. 0.1 uF



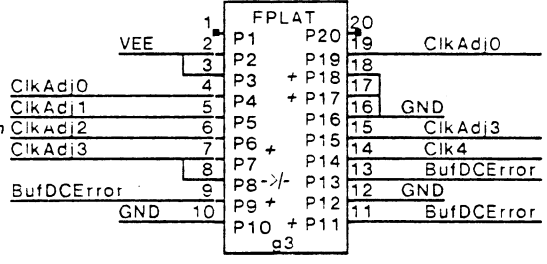
LM741

- R127. 1.0 KOhm
- C134. 0.47 uF
- C132. 0.027 uF
- R117. 510 ohm
- C131. 0.0027 uF
- R126. 110 ohm

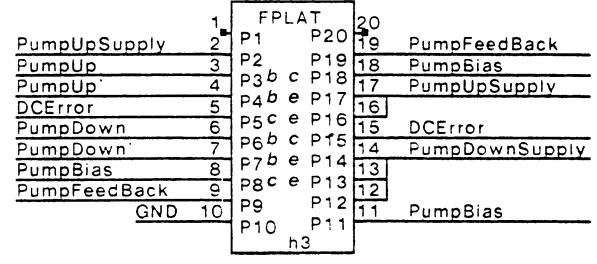


C119 is a 1.0 uF tantalum capacitor
CR103 is an MV1404 VariCap, used to control the oscillator frequency.

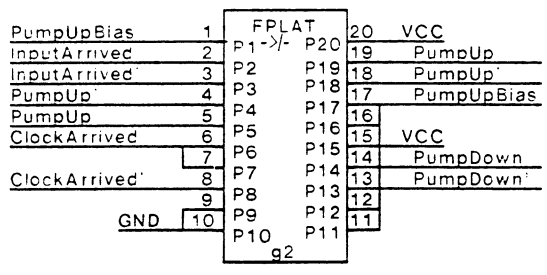
- R112. 510 ohm
- C120. 0.1 uF
- C119. 1.0 uF
- R105. 4.7 KOhm
- R113. 200 KOhm
- 2.0.1 uF
- CR103. MV1404
- C124. 47 pf
- C123. 100 pF



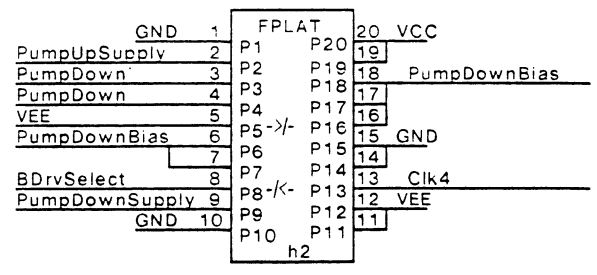
- R125. 2.0 KOhm
- Q103. 2N5771
- Q102. 2N5771
- Q105. 2N5770
- Q104. 2N5770
- R138. 2.0 KOhm
- R128. 100 ohm



- CR102. 1N5221
- R123. 910 ohm
- R122. 910 ohm
- R115. 200 ohm
- R116. 200 ohm
- R120. 510 ohm
- R132. 1.1 KOhm
- R134. 1.1 KOhm
- C121. 0.1 uF
- R114. 150 ohm



- C133. 0.1 uF
- R124. 180 ohm
- R135. 200 ohm
- R133. 200 ohm
- CR104. 1N5221
- C140. 0.1 uF
- R136. 180 ohm
- CR101. 1N4148
- R137. 240 ohm
- C141. 0.1 uF



P100.
5K. 3/4 W
potentiometer

R109. 270 ohm

