Zendex

ZX-200A Single Board Diskette Controller

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WARRANTY

All products are warranted against defects in material and workmanship under normal and proper use and in their original unmodified condition. If found defective by Zendex Corp. within the terms of this warranty, Zendex Corp.'s sole obligation shall be to repair or replace at Zendex Corp.'s option the defective product. If Zendex Corp. determines that the product is not defective within the terms of this warranty, customer shall pay all costs of handling and return transportation. All replaced products become the property of Zendex Corp. As a condition of this warranty, customer must obtain a Zendex Corp. Return Material Authorization Number, and must return all products, transportation prepaid and insured, to Zendex Corp.'s Dublin, CA facility or other specified location.

Transportation charges for the return to customer shall be paid by Zendex Corp. within the contiguous United States only. These warranties outside the contiguous United States are limited to repair or replacement only and exclude all costs of shipping, customs clearance, and other related charges. Except for the express warranties stated above, Zendex Corp. disclaims all warranties on products, including all implied warranties of merchantability and fitness; and the stated express warranties are in lieu of all obligations or liabilities on the part of Zendex Corp. for damages, the use or performance with this product.

Warranty period is one (1) year from date of original shipment. Warranty registration card must be returned to Zendex for warranty to be in effect.

SERVICE POLICY

If a product should fail during the warranty period, it will be repaired for free. There will be a service charge for repair of a product after the warranty period. If a product exhibits misuse, negligence, or user misconnection, the failure will be treated as an out-of-warranty repair.

To return a product for in-warranty repair, first reverify that the unit is indeed at fault. Then, call the factory for Return Material Authorization (RMA) Number. The product should be carefully packaged and shipped prepaid using the provided RMA number on the outside of the package. Include a short statement of the malfunction, along with return address information, and the telephone number of a technical contact, in case the need arises.

For out of warranty repairs, a purchase order for repair charges must also be included.

Items should not be returned freight collect, as they will not be accepted. It is absolutely necessary to return products in the manner stated here, otherwise considerable delay will result in processing the return.

OUT OF WARRANTY REPAIRS

After the warranty has expired, or if no warranty registration is on file, any Zendex board product will be repaired or replaced (at Zendex's option) for a flat fee of $100, provided, in Zendex's opinion, the product has not been abused, misused, modified or damaged. Otherwise there will be a time and materials charge for returning it to original condition. This policy is subject to cancellation, modification, and change without notice.

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Chapter 1 - General Information

1.1 Introduction

The ZX-200A is a single-board floppy disk controller which is able to interface from one to four eight-inch single density (FM) or double density (MMFM) disks to the multibus structure The controller allows up to four single sided drives to be used, thus providing up to two megabytes of storage.

1.2 Description

The ZX-200A utilizes an 8085A microprocessor and 8257 DMA controller to perform all disk controller functions. Single or double density operation is under software control, and full emulation of standard Intel disk systems is possible. The ZX-200A can fully replace the Intel disk controller boards used in the MDS-800 and MDS 220/230 Development Systems, and can operate under ISIS-II software. The ZX-200A uses one Multibus card slot.

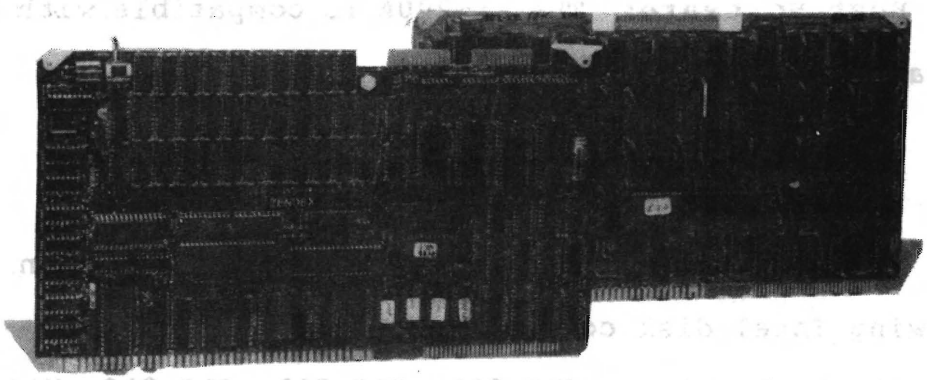


Figure 1 - ZX-200A

Zendex Corporation has been licensed by Micromation Corporation to build the ZX-200A using the Micromation MM-SBC-80F Multibus Floppy Disk Controller printed circuit artwork. Thus the layout, configuration, and features of the ZX-200A match the MM-SBC-80F. The Micromation manufactured board sold by Zendex was known as Model ZX-200

1.3 Equipment Supplied

The following equipment is supplied with the ZX-200A:

ZX-200A Hardware Reference Manual; with
Schematic Diagram D200-01A; and
Assembly Diagram

1.4 Compatible Equipment

CPU: The ZX-200A is compatible with any CPU, which is multibus compatible and is capable of multimaster operation, such as:

ZX-85, 88, 86
SBC-80/10B, 80/20, 80/24, 80/30
SBC-86/12A
ZX-80/05

Disk Drive: The ZX-200A is compatible with the following drives or their equivalents:

Shugart Associates 800/801
Memorex 550/552
CDC 9404

Host Software: The ZX-200A is compatible with the following software:

ISIS-II (Intel)
CP/M for MDS
Intel FORTRAN, BASIC
UCSD PASCAL for CP/M
Intel PLM, RMS-80 (Host)

Emulation: The ZX-200A emulates and can replace the following Intel disk controllers:

Single Density - SBC-201, SBC-211, SBC-212, MDS-2DS, MDS-710
Double Density - SBC-202, MDS-DDS, MDS-720

The ZX-200A when sold in combination with the Zendex ZX-730 Dual Drive Unit, is known as ZX-710/720 Mod 200A.

1.5 Specifications

Table 1

ZX-200 Specifications

Operation Modes	Single Density (FM) Ports 88H-8FH Double Density (MMFM) Ports 78H-7FH
System Bus Interface	Compatible with MULTIBUS specifications See Intel publication 9800083-02
Floppy Disk Dive Interface	Accommodates Shugart 800 Series standard size disk drive (8 inch)
Power Requirement	+5 volts at 2.75A (TYP)
Temperature	0 degrees to 40 degrees Centigrade
Humidity	0 to 90 percent RH non-condensing
Dimensions	12 inches long 6.75 inches wide 0.50 inches deep (one card slot)
Weight	14 ounces

Weight	1. ounces
Dimensions	1x .Inches 6.75 Inches x 0.50 Inches
Humidity	
Temperature	
Power Requirements	
Dive Meter	
Physical Data Interface	
Operation Modes	

Chapter 2 - Preparation for Use

2.1 Introduction

This chapter provides information on preparing and installing the ZX-200A. Included are instructions on unpacking and inspection as well as information on installation procedure.

2.2 Unpacking and Inspection

Inspect the shipping carton immediately upon receipt for evidence of mishandling during transit. If the shipping carton is severely damaged or waterstained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is not present, and the contents of the carton are damaged, keep the carton and packing material for the agent's inspection.

For repair to a product damaged in shipment, contact Zendex, Inc. to obtain further instructions. A purchase order will be required to complete the repair. A copy of the purchase order should be submitted to the carrier with your claim.

It is suggested that salvageable shipping cartons and packing material be saved for future use in the event the product must be shipped.

Please fill out warranty card immediately and return to Zendex. This is your only way to receive regular ECO information and various updates that may become available.

2.3 Installation Considerations

The ZX-200A is intended to replace the two-board Intel Diskette Controller set (Channel and interface boards). It should be inserted into the card slot that would have held the Intel Diskette Interface Board. In order to ensure that the ZX-200A connects properly to the bus resolving multibus signals (BPRN/, BPRO/, BREQ/), it must occupy an odd-numbered card slot in the MDS-800 only. Series II and III can be in any slot.

The user should be aware of the fact that the Intellec MDS 220 has a single density drive mounted in the cabinet next to the CRT. This drive is controlled by the IO controller board, which is located **not in the card cage,** but at the back of the cabinet. The ZX-200A can still be plugged into the card cage, however, the original integrated single drive (ISD) will respond as :F4: under ISIS-II, rather than physical drive zero; and physical drive one will also respond as single density drive :F5:.

Before installing the ZX-200A, turn off all system power and remove the front panel (MDS 220/230), or the top panel (MDS 800). If the Intel channel and interface boards are installed, first remove the cable from the interface board, then remove both boards. Allow the ZX-200A to run both the single and double density systems. The Intel disk controller must be removed.

Before installing the ZX-200A, clean off the multibus and disk drive cable edge connector fingers with alcohol and for MDS-800 plug the ZX-200A controller into an odd-numbered slot of the card cage.

If the ZX-200A has been purchased in conjunction with a ZX-710/720 MOD 200 System, all cabling necessary to connect the ZX-200A to the ZX-730 disk drives is supplied. If the ZX-200A is purchased separately, a fifty-pin ribbon cable must be made. This must have a fifty-pin printed circuit connector in place at each end. This can connect the ZX-200A edge connector directly to four disk drives. The ZX-200A connector is pin for pin compatible with Shugart SA800. The cable supplied with the Intellec MDS is of no use and may be set aside.

Refer to Figure 2, for the jumper options required of a Shugart SA80IR for use with the ZX-200A.

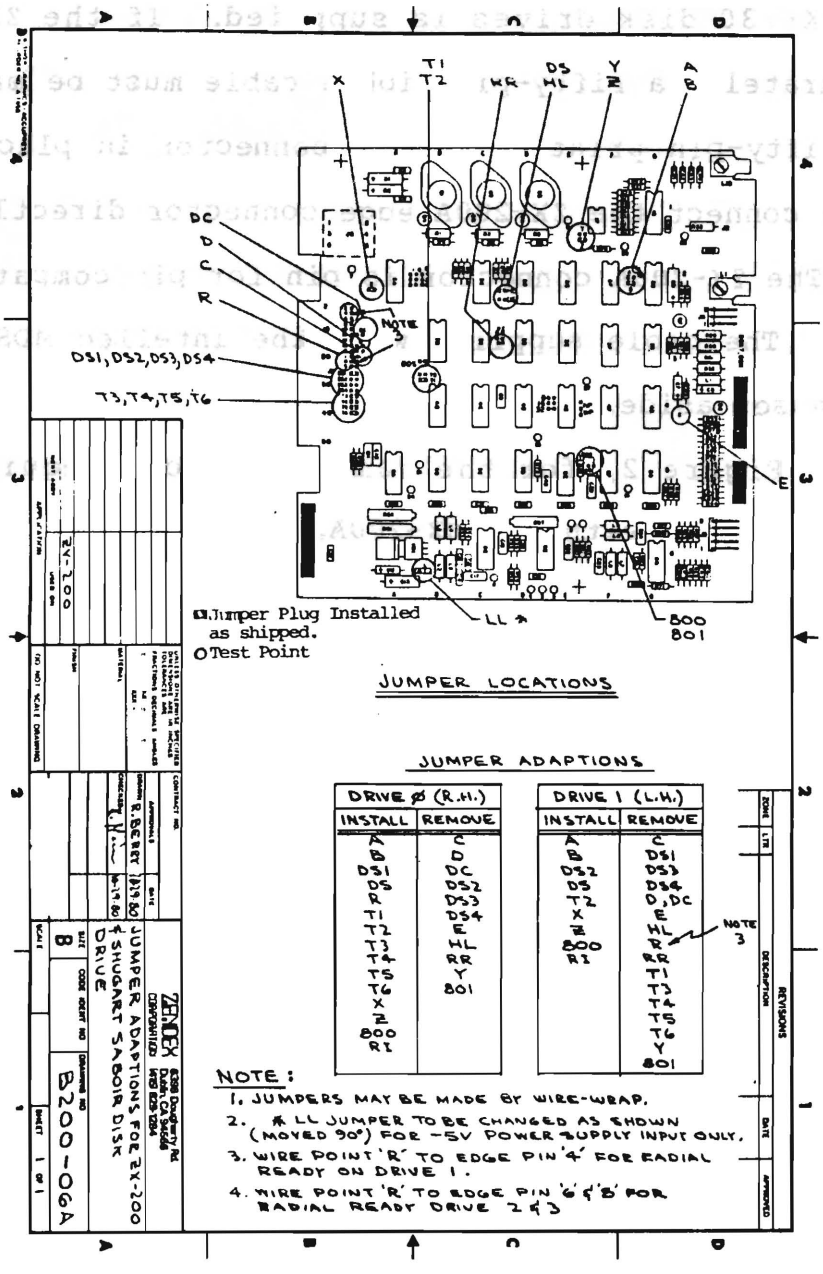


Figure 2 - Jumper Adaptions for ZX-200A

2.4 Jumper/Trace Cut Options

Various jumper and trace cut options are offered to allow maximum flexibility when working with the ZX-200A. These are arranged as follows:

Jumpers			
Label	**Function**	**Factory Default**	**Location**
W1, W2	**Drive Assignment Select** These two jumpers allow four possible choices with respect to the various drive name and density assignments under CP/M or ISIS. However, the present firmware does not make use of these jumper positions; therefore, the user may configure these jumpers as desired and allow the software to read their states and branch accordingly. Remember, the current firmware **does not use** these jumpers.	W1 in W2 in	Near U12
W3	**Reserved for future use**	W3 in	Near U43
(A-B-C)	**Disk Drive Buffer Enable.** This jumper allows the disk drive buffer to be either enabled permanently or to be enabled by the head load signal. Normally, the buffer should be enabled by the head load signal in order to qualify the disk control signals and avoid glitches on the drive select lines.	Head Load	Near U11

Jumpers (continued)

Label	Function	Factory Default	Location
TV	**Daisy Chain Priority Resolution.** The ZX-200A can operate either with daisy chain or parallel resolution. To select daisy chain resolution, install a jumper plug from T to V. For parallel resolution, leave the jumper plug out.	Installed	Near U67
G, H, J, K, L, M, N, P, R, and S	**System Interrupt.** G and H plated through holes are the outputs from the interrupt generator circuitry. A jumper is installed at the factory from G and H, to N (INT2/). This is the standard configuration. G represents an interrupt associated with addresses 88H to 8FH, while H represents the same from 78H to 7FH.	G-H-N U71-U73	Between
	Trace Cut		
A-B, C-D	**Disable Controller for 78H or 88H*.** There are four plated through holes in the PCB next to the U43. Each pair of holes is connected with a trace on the coponent side when shipped from the factory. Cut the trace between the hole pair **closest** to U43 and the ZX-200A will not respond to addresses 78H to 7FH (usually, but not always for double density). Cut the other trace and the ZX-200A will not respondto addresses 88H to 8FH (always single density)	AB Connector CD Connector	Near U43 on component side

Trace Cut (continued)

Label	Function	Factory Default	Location
Write Enable	**Write Protect.** There are two plated through holes between U12 and U13 which are connected by a trace on the solder side. If the trace is cut, the controller will not write to any of the disk drives connected to it.	Connected	Between U12, U13
G-H-J	**Advance Acknowledge** There are three plated through holes between U69 and U70. The one closest to the 86-pin connector goes to the /AACK backplane signal and nowhere else. The other two holes are connected by a trace on the solder side and are connected to the /XACK backplane signal. Normally, the /XACK signal is the one that should be used, since the /AACK signal is being abandoned by various Multibus standards. However, should the user wish to use /AACK, cut the trace on the solder side and connect a jumper between the middle hole and the one closest to the 86-pin connector.	G-H connected H-J open	Between U69, U70

*** Note:** In order to have the ZX-200A respond to addresses other than 78H to 7FH or 88H to 8FH, U43, the I/O MAP PROM, MAP23 at U43, must be changed by the user as desired. Zendex does not offer or support alternate PROMs. It should be kept in mind before changing PROMs that the factory PROM is compatible with CP/M and ISIS-II requirements.

Chapter 3 - Operating System

The ZX-200A will run under either the CP/M or ISIS-II operating systems. An important fact, which needs clarification at this point is how the disk drives are numbered according to recording density and operating system. Table 3-1 shows how the drive numbers are assigned.

Physical Drive	ISIS Drive	CP/M Drive	Single Density	Double Density
0	:F0:	A:		X
1	:F1:	B:		X
2	:F2:	None		X
3	:F3:	None		X
0	:F4:	C:	X	
1	:F5:	D:	X	

Table 3.1 Drive Number Assignments

In order to bring up the operating system for a particular configuration, the double density system disk must be placed in Drive zero.

In a two drive Zendex or Intel double-density system, drive zero is on the right, drive one is on the left, and for the single density system, drive four is on the right, drive five is on the left. However, the situation becomes more complicated than

this, because a total of five drives could be utilized in an MDS-220 system, where the drive next to the CRT is controlled by the I/O controller in the MDS-220 chassis, and up to four external drives may be controlled by the ZX-200A.

The main thing to remember is that the logical number of a physical drive depends on the density of the diskette inserted in it at the time.

If a drive has a single-density diskette inserted in it, the only possible logical numbers for that drive are either :F4: (C:) or :F5: (D:). If it has a double-density inserted in it, the only possible numbers for that drive are: :F0:(A:), :F1:(B:), :F2:, :F3:. An attempt will be made to illustrate various drive number assignments for MDS-800, MDS-220 and MDS-230 Systems as a function of number of drives, density of diskette inserted. See the table on the following page.

Table 3.2

Drive Assignments for MDS-800, MDS-220

	Drive Assignment		Diskette
	RH	LH	Density
MDS-800/ MDS-230 MDS-800 Two-drive System	1 5	0 4	DD SD
MDS-800/ MDS-230 MDS-800 Four-drive System	1 3 5	0 2 4	DD DD SD
MDS-220 MDS-220 Five-drive System	1 3 5	0 2 4*	DD DD SD
MDS-220 MDS-220 Three-drive System	1 5	0 4*	DD SD

*Single-density drive #4 always located in CRT chassis

The above illustration assumes that the ZX-200A is the only disk controller in the system aside from the IOC inside the MDS-Series II or III. The maximum number of drives in this case is five; four controlled by the ZX-200A and one controlled by the MDS-220 IOC.

CAUTION: If the CP/M is used with the MDS-220, and the MDS-220 is controlling two external drives,the MDS-220 drive is always single density and with ISIS is drive four. However, with CP/M this drive is invisible to the operating system and is not accessable.

Once the system configuration is well understood, all cabling is in place and the ZX-200A jumpers and trace cuts are understood and implemented, the operating system may be loaded. This is done according to the type of system being used, as follows:

MDS-220/230 (All Series II or III)

(1) Apply power to the MDS-220/230 and to the floppy disk drives. A prompt will appear on the CRT indicating that the system monitor has been entered.

(2) Insert the double density ISIS or CP/M system disk in Drive zero with the label facing up or left depending on horizontal or vertical drive mounting, and close the door.

(3) Press the system RESET button. A disk access will take place, the operating system gets loaded, and the sign-on message and prompt are displayed.

MDS-800 and Zendex Models 835, 838

(1) Turn the power on/off key to the on position. Apply power to the drives.

(2) Insert the double density ISIS or CP/M system disk in drive zero with the label facing up or left depending on horizontal or vertical drive mounting, and close the door.

(3) Depress the top of the BOOT push button on the MDS-800 panel. This enables the bootstrap PROM.

(4) Press the top of the RESET push button. A disk access will take place and the Interrupt two light on MDS-800 will be illuminated.

(5) After the Interrupt two light turns on, hit the space bar of the system terminal device. The Interrupt two light turns off. A Zendex system will sign on at this point.

(6) Press the bottom of the BOOT push button to disable the bootstrap PROM. The operating system is loaded from disk, and the sign-on message and prompt are displayed.

Chapter 4 - Programming Information

4.1 Introduction

The ZX-200A operates in an Intel Intellec MDS environment and responds to CPU commands issued over the multibus. The ZX-200A therefore, conforms to the software protocol of the Intel controller boards that it replaces.

4.2 Operational Modes

The ZX-200A operates in two modes:

(1) When it hasn't been selected to perform a disk related function, it is in the IDLE MODE. In this mode, it is constantly looping through a routine that checks the status of the disk drives. If a change in the status is noticed (a disk is removed or inserted, for instance), an interrupt is sent to the CPU to register the change.

(2) During program execution, The ZX-200A is selected

- to perform diskette reads and writes
- to be reset
- to stop prematurely a group of linked disk operations (in single density operation only)
- to render diskette drive status to the CPU
- to indicate the result of an operation to the CPU

Each of the above operations is initiated by a CPU input or output to a specific port. There are two base addresses, one for single density operation and one for double density. (Although

the ZX-200A reads or writes in both densities, Intel has separate floppy disk controllers for each density.)

The base address for single density operation is at 88H and the base address for double density operation is 78H.

4.3 I/O Parameter Block (IOPB)

The IOPB consists of ten (in single density operation) or seven (in double density operation) bytes of information which indicate the disk operation to be performed. The former has more bytes per IOPB because the original Intel single density controller permitted the linking of several IOPBs together. Several bits (see the description of the channel word) and bytes are present to accommodate this feature. The Intel double density controller does not include the linking feature.

The ten IOPB bytes are described on the following page. In the description, the first seven commands apply to both single and double density operation. The last three are used in single density only.

The IOPB is stored in main memory and thus is accessible by both the ZX-200A and the CPU.

The ten* IOPB bytes are:

Byte 1: Channel Word

Byte 2: Diskette Instruction

Byte 3: Number of Records

Byte 4: Track Address

Byte 5: Sector Address

Byte 6: Buffer Address (lower)

Byte 7: Buffer Address (upper)

* Byte 8: Block Number

* Byte 9: Next IOPB Address (lower)

* Byte 10: Next IOPB Address (upper)

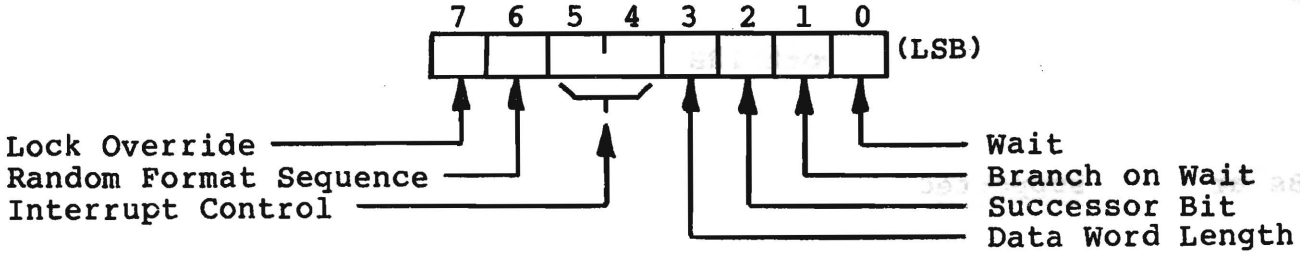
The host CPU must write the IOPB to main memory. Once written, the host CPU instructs the ZX-200A as to the IOPB locations through I/O ports. These instructions are called channel commands and are explained later.

* Single density operations only.

IOPB Byte 1 - Channel Word

Figure 4.1

Channel Word



Bit 0, 1 - Wait, Branch on Wait

Single Density Mode (Port 88):

Bit 1	Bit 0	Action
0	0	Immediately perform the current IOPB.
0	1	Idle for ten MS after which the Wait bit (bit 0) is examined. This loop is executed until the wait bit is reset.
1	0	Illegal
1	1	An unconditional jump to the 16-bit address pointed to by bytes nine and ten of the IOPB. The next IOPB to be performed must be resident at this address.

Double Density Mode (Port 78)

Bits zero and one are not used in the double density mode, since linked IOPBs are not supported in the double density mode. The ZX-200A Controller, therefore, will not wait and will execute only the correct IOPB.

Bit 2 - Sucessor

Single Density Mode (Port 88)

The sucessor bit (Bit 2) is reset if the current IOPB is the last (or only) one to be executed. Setting this bit indicates that a succesor IOPB is to be executed; its address is in IOPB bytes nine and ten. The diskette controller will issue an interrupt when the operation is complete, bit two is reset, and bits four and five of this byte allow interrupt.

Double Density Mode (Port 78H)

Bit two is not used in the double density mode, since linked IOPBs are not supported.

Bit 3 - Data Word Length

Bit three must always be reset to a zero, to specify eight bit word length, since 16-bit word lengths are not allowed on the ZX-200A.

Bit 4, 5 - Interrupt Control

Bit 4	Bit 5	Function
0	0	Generates interrupt: (a) upon completion of an unchained diskette operation; (b) after the last operation in a chain of linked operations; or (c) upon detection of an error in any intermediate operation in a chain of linked operations.
0	1	Disable disk operation complete interrupt to CPU.
1	1	Generates disk operation complete interrupt to CPU after current operation even though it is not the last in a chain of linked IOPBs. This code is illegal in the double density mode.
1	1	Illegal Code.

Bit 6 - Random Format Sequence

A logical zero in this bit assigns sequential sector addresses when a disk is formatted. A logical one writes the sector addreses according to a pattern listed in a 52 byte memory buffer pointed to by bytes six and seven of the IOPB (see below).

Bit 7 - Lock Override

Single Density Mode (Port 88H)

When set (logical one), this bit prevents the "wait" bit from being set upon completion of the current operation specified in the IOPB. When reset (logical zero), this bit alows the ZX-200A to set the "wait" bit.

Double Density Mode (Port 78H)

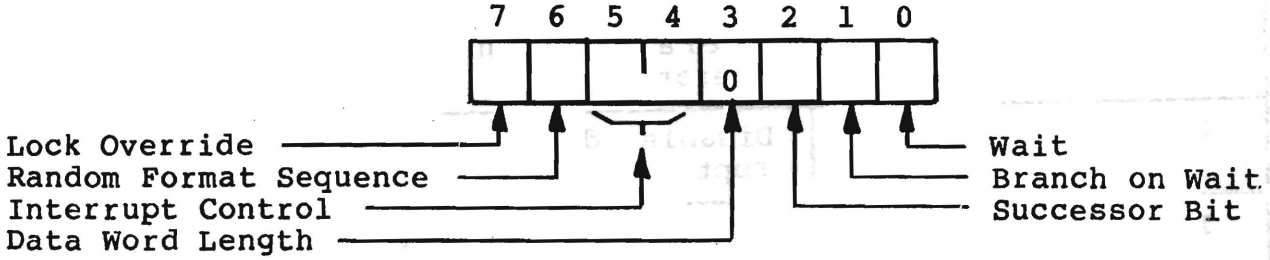
This bit is never used in the double density mode, since the ZX-200A never sets the "wait" bit in double density.

The following figure summarizes byte one of the IOPB, the channel word.

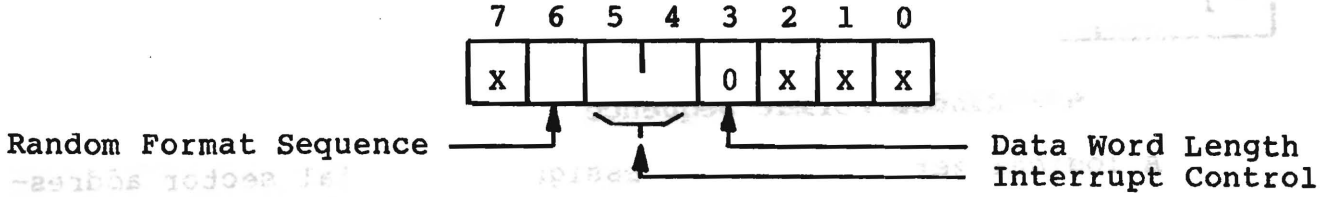
Figure 4.2

Summary of Byte One of the IOPB

Single Density Mode (Port 88)



Double Density Mode (Port 78)



0 = Must be zero
X = Doesn't care

Figure 4.2

Byte Two - Diskette Instruction

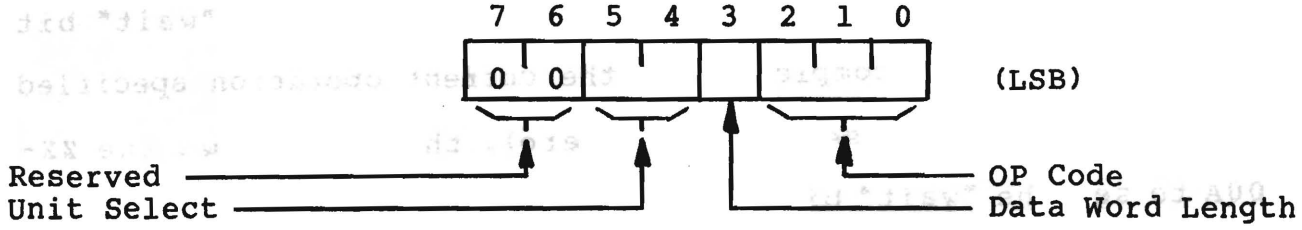


Table 4.1 Op Code

Bits 0, 1, 2 - OP Code

Bits			
2	**1**	**0**	**Operation**
0	0	0	No operation
0	0	1	Seek: move the head to the track indicated in byte four of the IOPB.
0	1	0	Format track: write the address marks, gaps address fields and data fields on the track indicated in byte four of the IOPB. This type of format is determined by bit six of byte one as described below.
0	1	1	Recalibrate: move the head to track 00.
1	0	0	Read data: transfer N sectors (N indicated by byte three of the IOPB) from the disk to system RAM. The destination locations in memory start at the address pointed to by bytes six and seven of the IOPB. If the head is not already positioned over the track indicated by byte four of the IOPB, it is moved automatically. A CRC check is performed,which compares the two bytes of CRC written on the disk with the two generated from the data address mark and data field read.
1	0	1	Verify CRC: check the CRC of the indicated sector(s). The operation is similiar to a READ; however, no data is transferred to memory.
1	1	0	Write Data: write N sectors (N specified in byte three of the IOPB) from the contents of memory that starts at the location indicated in IOPB bytes six and seven. As in read, the head is automatically moved to the desired track (from byte four of the IOPB) if it is not already there. Two bytes of CRC are generated and written to the disk. Note that multi-sector writes (N greater than 1) may not extend beyond a single track.
1	1	1	Write "Deleted" Data: write N sectors as described in the preceding operation except write a "deleted data mark" rather than the "normal" data mark.

Bit 3 - Data Word Length

Bit three must always be reset to a zero to specify eight-bit word length, since the ZX-200A will not handle 16-bit words.

Bits 4, 5 - Unit Select

Single Density Mode (Port 88H)

Bits		Function
5	4	
0	0	Drive 0
0	1	Illegal
1	0	Illegal
1	1	Drive 1

Double Density Mode (Port 78H)

Bits		Function
5	4	
0	0	Drive 0
0	1	Drive 1
1	0	Drive 2
1	1	Drive 3

Table 4.2 - Unit Select, Bits 4 and 5

Bits 6, 7 - Reserved

These bits are not used and should be set to zero at all times.

IOPB Byte 3 - Number of Records

Byte 3 indicates the number of records (sectors) to be written/read. The number must be written in binary and may not exceed 26 in single density operation or 52 in double density operation. (Recall from the description of the Op Code above, that a read write operation may not extend beyond a single track.)

IOPB Byte 4 - Track Address

A binary code in byte 4 indicates the desired track number. Acceptable values are 00 to 4C hex (0 to 76).

IOPB Byte 5 - Sector Address

This byte specifies the first (or only) sector for operation. In single density mode specify $1\text{-}1A_{10}$ (26_{10}) and in double density mode $1\text{-}34_{16}$ (52_{10}). Bit five of this word must equal bit five of byte two in single density mode only.

IOPB Bytes 6, 7 - Buffer Address

These bytes specify the address of the disk buffer block for Read/Write/Format operations. Byte six is the least significant eight bits of the address while byte seven is the most significant portion.

> **Note:** The next three IOPB Bytes (8, 9, 10) are used for single density applications only. They are used when a chain of IOPBs is to be executed. Note that this feature is not used frequently. (In fact, Intel dropped this feature from its double density controller.) If chaining is not used, these three bytes have no effect.

IOPB Byte 8 - Block Number (Single Density Only)

The specific number of the current IOPB is specified in this byte. Only six bits (5-0) are used. The block number allows the CPU to associate an I/O complete interrupt request from an intermediate link in a chain of IOPBs with the IOPB which actually caused the interrupt. The block number need only be initialized for linked IOPBs, since there can be no uncertainty when only a

single IOPB exists. This byte and bytes nine and ten are used for linked IOPBs.

IOPB Byte 9 - Next IOPB (Lower Address) (Single Density Only)

The least significant byte of the 16-bit memory address of the next IOPB is entered in this byte.

IOPB Byte 10 - Next IOPB (Upper Address) (Single Density Only)

The most significant byte of the 16-bit memory address of the next IOPB is entered in this byte. If the successor bit (two) of IOPB byte one is set (logical 1), the controller accesses the IOPB starting at this address upon completion of the current operation. If the successor bit is zero, it is assumed that the current IOPB is the last. The controller also looks at the "branch on wait" and "wait" bits in IOPB byte one. If both are set (logical 1), a jump to the IOPB at the address identified here is performed.

4.4 Disk Commands

The ZX-200A is capable of performing seven distinct operations: Recalibrate, Read, Write, Write Deleted Data, Record, Verify CRC, Seek, and Format. To begin any operation, the host CPU should output both bytes of the 16-bit memory address that point to byte one of the IOPB. The operation to be performed is specified in byte two of the IOPB. After the ZX-200A receives the upper byte of the IOPB address, it accesses the IOPB to interpret the operation to be performed and acquire the various parameters necessary to carry out the execution. The ZX-200A will set the

interrupt flip-flop after it has performed the operation or has halted operation due to errors.

The eight diskette operations are explained in more detail in the following paragraphs.

Recalibrate (Opcode 3 of IOPB Byte 2)

This operation will cause the selected unit's head to move over Track zero. Operation is mechanically verified by detectors in the drive itself.

Seek (Opcode 1 of IOPB Byte 2)

This operation will cause the selected drive to position its head over the specified track. Seek Track zero is tested for and, if issued, Recalibrate is executed instead.

Read (Opcode 4 of IOPB Byte 2)

This operation will return the specified number of data records to be written to the buffer, beginning at the given buffer address and continuing upward, starting with the track and sector given in the IOPB.

Write Data (Opcode 6 of IOPB Byte 2)

This operation is the same as Write Data except that each 128 byte data field is preceded with a deleted data address mark.

Verify CRC (Opcode 5 of IOPB Byte 2)

This operation will read the data records to verify the CRC check word. No data is transferred to the buffer.

Format a Track (Opcode 2 of IOPB Byte 2)

This operation is used to initialize a new disk or restore a "wiped-out" track. Prior track contents will be lost.

It should be noted here that a track can be "wiped-out" if the operator shuts off power to the diskette system while the

diskette is installed or the reset is hit while heads are loaded. Pop out diskettes BEFORE power-down or reset!

The order sector numbers that are assigned in the formatting of a track will depend on the state of the "Random Format" bit in byte one of the IOPB. If the random format bit is set, the pattern of sector addressing and initial sector data contents will be prescribed by the information in the buffer.

For Random Format the buffer contains the sector numbering, in order of assignment on the track, beginning with the first byte of the buffer and continuing through each odd numbered byte. The even numbered byte (one greater than sector address) will be the data to be initially written to all 128 bytes of the sector.

For example, if the buffer was constructed as:

Byte	Contents (Hex)
1	07
2	20
3	05
4	FF

the first physical sector of the track will be numbered seven with 20 as data in each of its 128 bytes. The second physical sector will be numbered five with all ones as initial data.

If the Random Format bit is reset, the order of sector numbering will be that of the physical sector and the initial data written to all sectors will be that of byte one of the buffer.

No Operation (Opcode 0 of IOPB Byte 2)

The No-Op instruction causes the ZX-200A to execute a read drive status and is intended to verify that the controller is functioning.

4.5 Channel Commands

Diskette status, result, and IOPB information are communicated over a set of I/O channels and are called, as a group, the Channel Command.

Once a proper IOPB has been constructed in main memory the controller must be informed of the IOPB address via Channel Commands. Upon completion, or interrupt, result data is available with error indications by way of Channel Commands.

When the Write IOPB Address Upper is executed the disk system will commence the operation specified in the IOPB. Therefore, the lower portion of address and the entire IOPB must have been properly constructed before this Channel Command is executed.

Out Port 7F 8F - Reset

This output channel command causes all logic in the ZX-200A to be reset to an initialized state. This command is intended to clear hang-ups.

Out Port 79 89 - Write IOPB Address Lower

This channel command outputs the low byte of the 16-bit address pointing to byte one in the IOPB.

Out Port 7A 8A - Write IOPB Address Upper

This channel command outputs the high byte of the IOPB's 16-bit address. This command also causes the ZX-200A to begin execution of the IOPB.

Out Port 8B - Stop

The diskette controller will stop operation AFTER completing the current IOPB instruction. It will not proceed to the next IOPB in a link. This channel command has no meaning in double density mode since linked operations are not performed.

In Port 78 88 - Status Input

This input channel command causes the ZX-200A to return the drive and controller ready status.

Table 4.3 - Status Word

Bit 0	Ready Status of Drive 0
Bit 1	Ready Status of Drive 1
Bit 2	Interrupt Pending
Bit 3	Controller Present
*Bit 4	Double Density Controller Present
*Bit 5	Ready Status of Drive 2
*Bit 6	Ready Status of Drive 3
Bit 7	Hard Disk Present

*Active in Port 78 only (double density mode)

Bits zero, one, five and six, allow the host to determine whether the target drive is ready (bit equals one) or not (bit equals zero).

In Port 79 89 - Read Result Type

This input channel command will return a two bit result type (bits 0 and 1) and, for 201 mode only, a block number in bits two through seven. The result type is decoded as:

Bit	1	0	Meaning
	0	0	I/O complete. Result byte contains error bits.
	0	1	Single Density mode only. I/O complete, result byte contains linked error bits.
	1	0	Result byte has drive ready status.
	1	1	Reserved.

Table 4.4 Read Result Type

The Result Type command must be issued to clear the system interrupt and diskette controller interrupt pending bits (which toggle together) in the status word.

In Port 7B 8B - Read Result Byte

The channel command causes the ZX-200A to return eight bits of operation results. The proper interpretation of the result byte depends upon the result type. For result types 00 and 01:

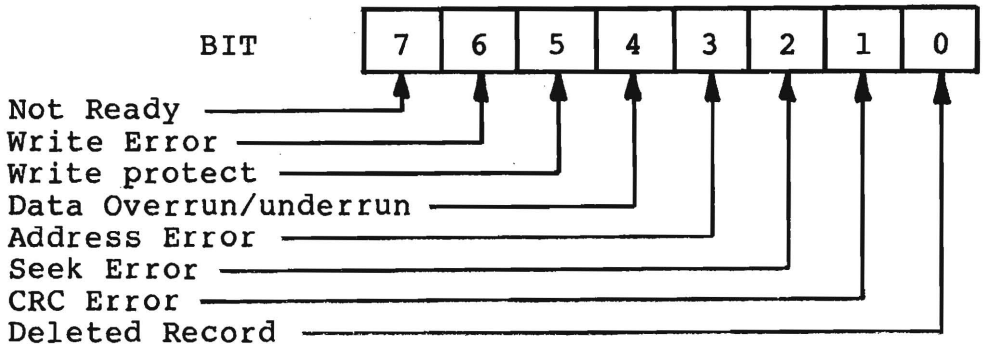


Figure 4.5

Port 7B-8B Read Result Byte for Result Types 00 and 01

If the host executes a 'read result byte' channel command, the diskette channel will return the result word on the system data bus. The bits are defined as follows:

Not Ready:

Bit seven indicates the selected unit was not ready or the selected unit changed to a not ready status during operation.

Write Error:

Bit six indicates that during a write operation a condition existed which precluded data integrity. An example of a condition causing this error is an attempt to write a 'not ready FDD.'

Write Protect:

Bit five indicates the selected drive contains a diskette, which is not write enabled. This condition is checked on format a track, write data (with data address marks) and write data (with deleted data address marks) operations.

Data Overrun/Underrun Error:

Bit four indicates that the ZX-200A controller was not able to service a byte transfer request from the drive before the next request occurred. The data byte is lost.

Address Error:

Bit three indicates that the disk address received from the CPU is invalid; that is:

- track address > 76_{10}
- sector address = 00
- sector address > 52_{10} (202 mode)
- sector address > 26_{10} + number of records >52_{10} (202 mode)
- sector address + number of records > 26_{10} (201 mode)

Seek Error:

Bit two indicates that at the completion of a head movement sequence the head is not positioned over the expected track. This bit indicates the controller and/or FDD are malfunctioning, and a recalibrate diskette operation should be performed. Seek error can occur during any diskette operation.

CRC Error:

Bit one indicates the CRC characters generated during a read data or verify CRC operation were not the same as the two CRC characters appended to the data field when it was originally written on the diskette.

Deleted Record:

Bit zero indicates that a sector addressed during a read data or verify CRC operation was preceded by a deleted data address mark.

Two other error conditions are provided when more than one error bit is true. They are:

ID CRC Error:

If the address error and CRC error (bits 3 and 1, respectively) are true, this indicates the CRC characters generated during the reading of an ID field were not the same as the CRC characters appended to the field when it was written by a format track operation.

Data Mark Error or No Address Mark:

If the address error, seek error, and CRC error (bits 3, 2 and 1, respectively) are true, this indicates no address mark or a data mark error was encountered. This usually means the track has not been formatted.

Chapter 5 - Controller Operation

5.1 Introduction

This chapter is intended to give a brief description of the ZX-200A hardware operation and its external interfaces.

5.2 Interrupts

The ZX-200A will generate interrupt requests when allowed by certain channel commands (see Chapter 4). Any interrupt (INT0 through INT7) may be used, but most operating systems, expecially ISIS, will require INT2/. This may be selected via jumper (see Chapter 2).

5.3 I/O Base Address Selection

The I/O base address is fixed by U43, a bipolar PROM.

For microcomputer development systems using ISIS the required address is 78H - 7FH for logical drives :F0:, :F1:, :F2: and :F3:, which are all double density.

The required address is 88H - 8FH for logical drives :F4: and :F5:, which are both single density, and independently add reusable.

5.4 Drive Interface

The ZX-200A has been designed to interface readily with the Shugart SA800. The 50-pin edge connector is pinned alike with the SA800, thus allowing simple ribbon connectors. More than one

drive may be used by simply paralleling it on a common connector and wire system as shown in the following figure.

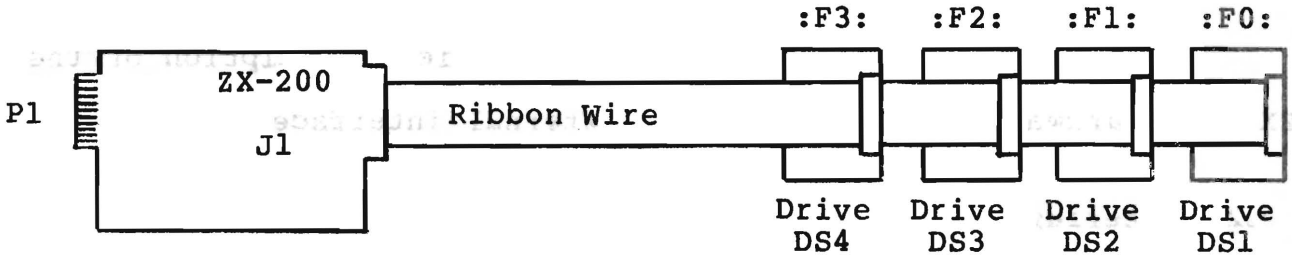


Figure 5.1 Ribbon Connection

Line terminators must be installed for each signal line at the last drive unit to use it. In the figure most lines (except DS1 through DS3) will be terminated at drive one.

The table on the following page lists the signals available at the drive interface connector J1.

Table 5.1 Signals at Drive Interface Connector J1

SIGNAL NAME	FUNCTION
DS1/-DS4/ J1-26 J1-28 J1-30 J1-32	A low state selects the drive. When active DS1/-DS4/ allows drives 0 through 3 to accept the remaining drive input signals and to gate its output back to the ZX-200A.
WRITE ENABLE/ J1-40	A low state will allow the data to be written on the diskette. When this signal is inactive the write electronics are disabled and the drive reads data from the diskette.
STEP/ J1-36	A signal pulsing low will cause the head to step one track, for each low-going, in the direction determined by DIR/.
DIR/ J1-34	When this line is low the step signal will cause the head to move toward the track 76 (step in), and when high the head to step out toward the outermost track 00.
WR DAT/ J1-38	This is the composite data/clock serial write signal. A high-to-low transition on this line indicates a bit to be written on the diskette.
RDY J1-22, 4,6,8	A low on this line indicates the selected drive is ready. This is a radial ready circuit.
WR PROT/ J1-44	An active low on this line indicates a write protected diskette is installed in the selected drive.
TRK0/ J1-42	An active low indicates the selected drive's head is positioned over track 00.
INDEX/ J1-20	A low going pulse is passed on this line that is coincident with the index hole in the diskette.
READ DATA/ J1-46	The composite data and clock signal generated during a diskette read operation. A high-to-low going transition indicates a clock or data one bit.
LOW CURRENT/ J1-2	Signal to the drive to reduce write current through head. Active low for track 43.
FAULT RESET/ J1-4	Reset signal to drive to clear fault indicator.

Table 5.1 Signals at Drive Interface J1 (continued)

SIGNAL NAME	FUNCTION
FAULT/ J1-6	Fault detected by drive. Signal is input to controller to cause fault routines to execute.
TWO SIDED/ J-10	Signal from FDD to indicate presence of a two sided media.
SIDE SELECT/ J1-14	Signal from FDC to FDD to select which side of a two sided media operation is to be performed.
Note: 1-49 odd are all signal grounds.	

5.5 Multibus Interface

The ZX-200A communicates with the master CPU over the bus through the 86-pin connector P1. Table 5.1 defines Multibus signals used and Figures 5.1 and 5.2 describe signal timings.

5.6 Board Location Considerations

The ZX-200A is a Multibus bus master and as such must be located in a backplane slot which provides for the BPRN/, BREQ/, BUSY, and BCLK signals. Other bus master cards in a system will consist of the CPU and DMA boards. Provision must be made for the various bus masters to communicate bus requests and grants through card arrangements and connections of the above bus signals. The most common priority resolution scheme is the serial type and is typically used in systems with less than four bus masters. A jumper should be used at wire wrap position T-V to provide BPRO/ output in serial priority schemes.

Figures 5.1 and 5.2 on the following page show bus access timing and 8219 set-up and hold timing.

Figure 5.2 Bus Access Timing

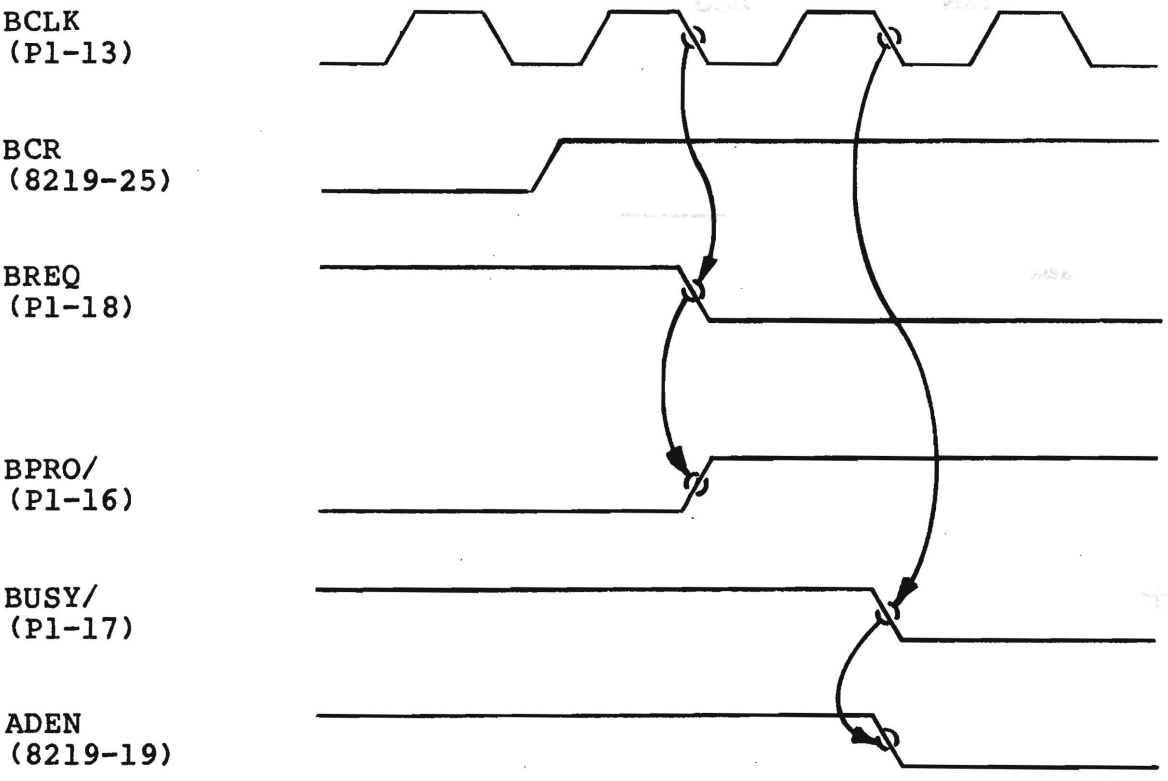


Figure 5.3 8219 Set-up and Hold Timing

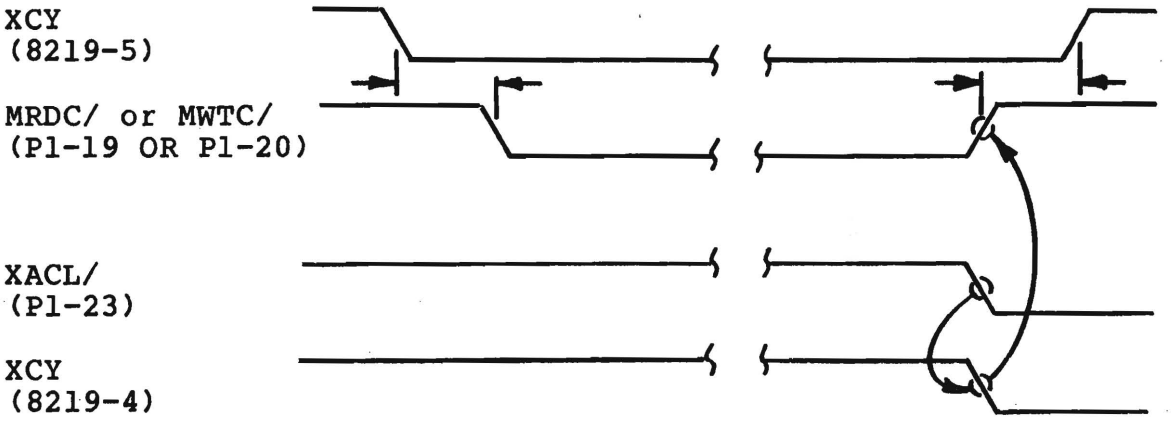


TABLE 5.2 MULTIBUS PIN ASSIGNMENTS

	BOARD COMPONENT SIDE			BOARD CIRCUIT SIDE		
	PIN	MNEMONIC	DESCRIPTION	PIN	MNEMONIC	DESCRIPTION
Power Supplies	1	GND	Signal Ground	2	GND	Signal Ground
	3	+5	+5 VDC	4	+5	+5VDC
	5	+5	+5 VDC	6	+5	+5 VDC
	7	+12	+12 VDC	8	+12	+12 VDC
	9	-5	-5 VDC	10	-5	-5 VDC
	11	GND	Signal Ground	12	GND	Signal Ground
Bus Controls	13	BCLK/	Bus Clock	14	INIT/	Initialize
	15	BPRN/	Bus Priority In	16	BPRO/	Bus Priority Out
	17	BUSY/	Bus Busy	18	BREQ/	Bus Request
	19	MRDC/	Memory Read Command	20	MWTC/	Memory Write Command
	21	IORC/	I/O Read Command	22	IOWC/	I/O Write Command
	23	XACK/	Transfer Acknowledge	24	INH1/	Inhibit (disable) RAM
	25	AACK/	Advance Acknowledge	26	INH2/	Inhibit (disable) ROM or EPROM
	27	BHEN/	Byte High Enable	28	ADR10/	
	29	CBRQ/	Common Bus Request	30	ADR11/	Address
	31	CCLK/	Constant Clock	32	ADR12/	Extension
	33	INTA/	Interrupt Acknowledge	34	ADR13/	Lines
	35	INT6/		36	INT7/	
	37	INT4/	Interrupt Requests	38	INT5/	Interrupt Requests
	39	INT2/		40	INT3/	
	41	INT0/		42	INT1/	
Address	43	ADRE/		44	ADRF/	
	45	ADRC/		46	ADRD/	
	47	ADRA/		48	ADRB/	
	49	ADR8/	Address Lines	50	ADR9/	Address Lines
	51	ADR6/		52	ADR7/	
	53	ADR2/		54	ADR5/	
	55	ADR2/		56	ADR3/	
	57	ADR0/		58	ADR1/	
	59	DATE/		60	DATE/	
	61	DATC/		62	DATD/	
	63	DATA/		64	DATB/	
	65	DAT8/	Data Lines	66	DAT9/	Data Lines
	67	DAT6/		68	DAT7/	
	69	DAT4/		70	DAT5/	
	71	DAT2/		72	DAT3/	
	73	DAT0/		74	DAT1/	
Power Supplies	75	GND	Signal Ground	76	GND	Signal Ground
	77	-10	-10 VDC	78	-10	-10 VDC
	79	-12	-12 VDC	80	-12	-12 VDC
	81	+5	+5 VDC	82	+5	+5 VDC
	83	+5	+5 VDC	84	+5	+5 VDC
	85	GND	Signal Ground	86	GND	Signal Ground

Table 5.3 Multibus Signals Descriptions

Signal Mnemonic	Functional Description
AACK/	Advanced Acknowledge. This signal is an advanced indication that the requested Read or Write operation will be completed in a specified time (t_{AACK}).
ADR0/-ADRF/	Address. These 16 lines are used to transmit the address of the memory location or I/O port to be accessed. ADRF/ is the most significant bit.
ADR10/-ADR13	Address Extension. These four lines are appended to the address to allow accessing of megabyte memories.
BCLK/	Bus Clock. The high-to-low transition of BCLK/ is used to synchronize bus contention resolution circuits. BCLK/ is asynchronous to the CPU clock. It has a minimum period of 100 nanoseconds and a 35% duty cycle. BCLK/ may be slowed, stopped, or single stepped for troubleshooting.
BHEN/	Byte High Enable. Indicates use of data lines DAT8-F.
BPRN/	Bus Priority In. Indicates to a particular master module that no higher priority module is requesting use of the bus. BPRN/ is synchronized with BCLK/. This signal is not bussed on the backplane.
BPRO/	Bus Priority Out. Used with serial (daisy chain) bus priority resolution schemes. BPRO/ is passed to the BPRN/ input of the master module with the next lower busy priority. BPRO/ is synchronized with BCLK/. This signal is not bussed on the backplane.
CBRQ/	Common Bus Request. Indicates a master module, not currently in control, requests use of the bus.
BUSY/	Bus Busy. This signal is driven by the bus master currently in control to indicate that the bus is in use. BUSY/prevents all other master modules from gaining control of the bus. BUSY/ is synchronized with BCLK/.
CCLK/	Constant Clock. Provides a clock signal of constant frequency for unspecified general use by modules on the bus. CCLK/ has a minimum period of 100 nanosconds and a 35% to 65% duty cycle.

Table 5.3 - Multibus Signal Descriptions (continued)

Signal Mnemonic	Functional Description
DAT0/-DATF/	Data. These 16 bi-directional lines transmit or receive information to or from a memory location or I/O port. DATF/ is the most significant bit. In eight bit systems only lines DAT0/-DAT7/ are used, in which case DAT7/ is the most significant bit.
INH1/	Inhibit RAM. Prevents RAM devices from responding to the memory address on the address lines. INH1/ effectively allows ROM devices to override RAM devices when ROM and RAM are assigned the same address space. INH1/ may also be used to allow memory mapped I/O devices to override RAM.
INH2/	Inhibit ROM. Prevents ROM devices from responding to the memory address on the address lines. INH2/ effectively allows start-up software such as ROM based bootstrap programs to override another ROM device when the two ROMs are assigned the same address space. INH2/ may also be used to allow memory mapped I/O devices to override ROM.
INIT/	Initialization. Resets entire system to a known internal state. INIT/ may be driven by one bus master or by an external source such as a front panel reset switch.
INT0/-INT7/	Interrupt. Each of these eight lines causes the master processor to generate INTA as defined below. INT0/ has the highest priority; INT7/ has the lowest priority as assigned by an interrupt priority resolution network.
IORC/	I/O Read Command. Indicates that the address of an input port has been placed on the address lines and that the data is to read from the data lines. IORC/ is asynchronous with BCLK/.
MRDC/	Memory Read Command. Indicates the address of a memory location has been placed on the address line a data word (eight or 16 bits) is to be read from the data lines. MRDC/ is asynchronous with BCLK/.
MWTC/	Memory Write Command. Indicates that the address of a memory location has been placed on the address lines and that a data word (eight or 16 bits) has been placed on the data lines. MWTC/ specifies that the data word is to be written into the addressed memory location. MWTC/ is asynchronous with BCLK/.

Table 5.3 - Multibus Signal Descriptions (continued)

Signal Mnemonic	Functional Description
XACK/	Transfer Acknowledge. The required response of memory location or I/O port to indicate that the specified read/write operation has been completed. That is, data has been placed on, or accepted from, the data lines. XACK/ is asychronous with BCLK/.

Figure 5.3 shows an implemented serial priority network. In this type of arrangement the bus master with the highest priority can be identified by its pin 15 (BPRN/) being grounded.

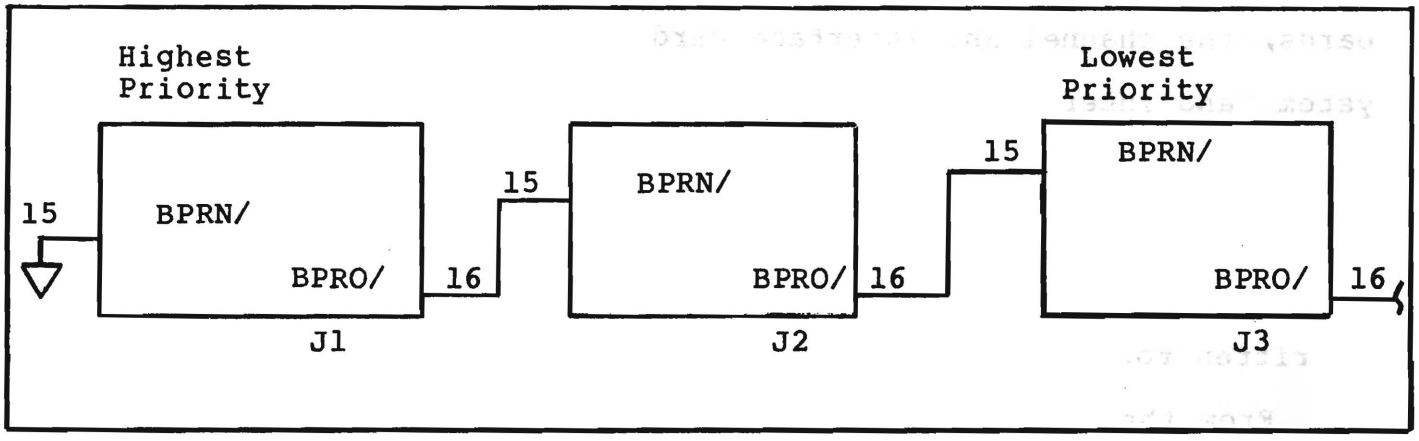


Figure 5.3 Implemented Serial Priority Network

In the above figure, the master in slot J1 will drop BPRO/ low to pass priority grant on to J2 if the master in J1 is NOT requesting the bus. BUSY/ will be high if no master is currently using the bus. If the master J2 doesn't need the bus, it will drop its BPRO/ low to cause J3 BPRN/ to go low and thus grant a J3 request. If J2 requests the bus it will raise its BPRO/ high and wait until its BPRN/ goes low, BUSY/ goes high, and BCLK/ does a negative transition. J2 will then latch BUSY/ low and that will disallow even higher priority master requests until J2 drops its use of the bus.

Higher speed and bus contention resolution schemes involving four or more masters use a parallel priority network. BREQ/ signal is output to an SN74148 (typical) priority encoder. Then an SN74S138 (typical) decoder outputs a master's BPRN/ for input grant.

5.7 Controller Features

The Zendex ZX-200A Multibus floppy disk controller emulates and enhances the Intel iSBC 202 Double Density and iSBC 201 Single Density floppy disk controllers. A single CONTROLLER card can replace both sets of boards (each Intel controller consists of two boards, the channel and interface cards) in an Intel Intellec MDS system and interfaces as many as four floppy disk drives. These drives can be single or double sided with single or double density fomat diskettes. The operator does not need to enter any commands to indicate the recording density of the diskette to be read from or written to.

From the system's perspective, the CONTROLLER appears as two separate controllers, one for single density diskettes and one for double density diskettes. Typically, each of the controllers is accessed via a different port address. Usually, these addresses fall in the following ranges:

Single density: 88 - 8F hex
Double density: 78 - 7F hex

The resident CONTROLLER firmware decodes the address to determine the recording density of the diskette. However, there are circumstances where the address range for the single density controller is 78 - 7FH. The firmware has been written to accommodate this configuration as well. (See Note on following page.)

Note: the first revision of the CONTROLLER firmware does not support single density operation from port 78H.

Data to be read from or written to the disk is fully buffered. The CONTROLLER contains 1K of static RAM temporarily storing the data for transfer. This means two things to the system designer: (1) the chance of a data overrun or underrun is completely removed, and (2) the controller cannot get control of the system bus in time for a byte of data read from the disk to be transferred to system RAM (data is transferred on a byte by byte basis). Consequently, that byte disappears as the next one is read from the disk and moved to RAM (assuming the controller gets control of the bus in time to transfer this byte). Data underrun is similiar, but occurs during a disk write operation. With the CONTROLLER, the entire sector (128 bytes) is written to the on-board RAM independently of the system bus. Data is transferred to system RAM with a DMA controller. If this gets interrupted by a higher priority component, the DMA controller keeps a record of the last location transferred, so that when it has control ofthe bus again, it can begin where it left off.

The rate of data exchange is 250K bits per second in single density and 500K bits per second in double density. Single density recording uses the standard IBM 3740 format. This format uses the frequency modulation (FM) recording technique and specifies 26 sectors of 128 bytes of data per track. In double density, MMFM (modified-modified frequency modulation) recording is used with 52 sectors of 128 bytes per track.

5.8 Controller Operation

The ZX-200A CONTROLLER firmware responds to ten I/O addresses output by the CPU. These addresses typically appear between 78 - 7FH for double density operation, 88 - 8FH for single density operation. In some circumstances 78 - 7H is also used for single density. The CONTROLLER firmware can interpret these addresses as well. **(Note:** these ports can be changed by inserting a different I/O address decode PROM u43**).** Of the eight available ports in each range, only five are used. The CPU selects one of seven disk-related operations by outputting to the port associated with that operation.

The CONTROLLER operates as a system within the system. It contains a 8085A processor, which executes the requested disk operation via a memory-map. For instance, a read sector command from the CPU requires a number of processes be performed in addition to the read operation (for example, move head to track, synchronize with the disk, read data, read and compare CRC, etc.) Each of these functions is enabled by an output to the port within the CONTROLLER dedicated to it.

When the command requests a disk read or write, two DMA operations follow. First, the seven or ten bytes of the I/O parameter block (IOPB) are moved to a 1K RAM buffer on the CONTROLLER RAM buffer. A resident 8257 DMA controller performs this task. Once it has control of the system bus from the CPU, the whole content of the data buffer is transferred to system RAM for a disk read or vice versa for a disk write. The requisite bus signals are generated to access memory. If the controller is

interrupted by a higher priority component in the system, the 8257 "remembers" the last byte transferred. When it has regained control of the bus, the next byte is transferred.

The CONTROLLER operates in two modes:

(1) when it hasn't been selected to perform a disk related function, it is in the IDLE MODE. In this mode, it is constantly looping through a routine,which checks the status of the disk drives. If a change in the status is noticed (a disk is removed or inserted, for instance), an interrupt is sent to the CPU to register the change.

(2) During program execution, the CONTROLLER is selected:

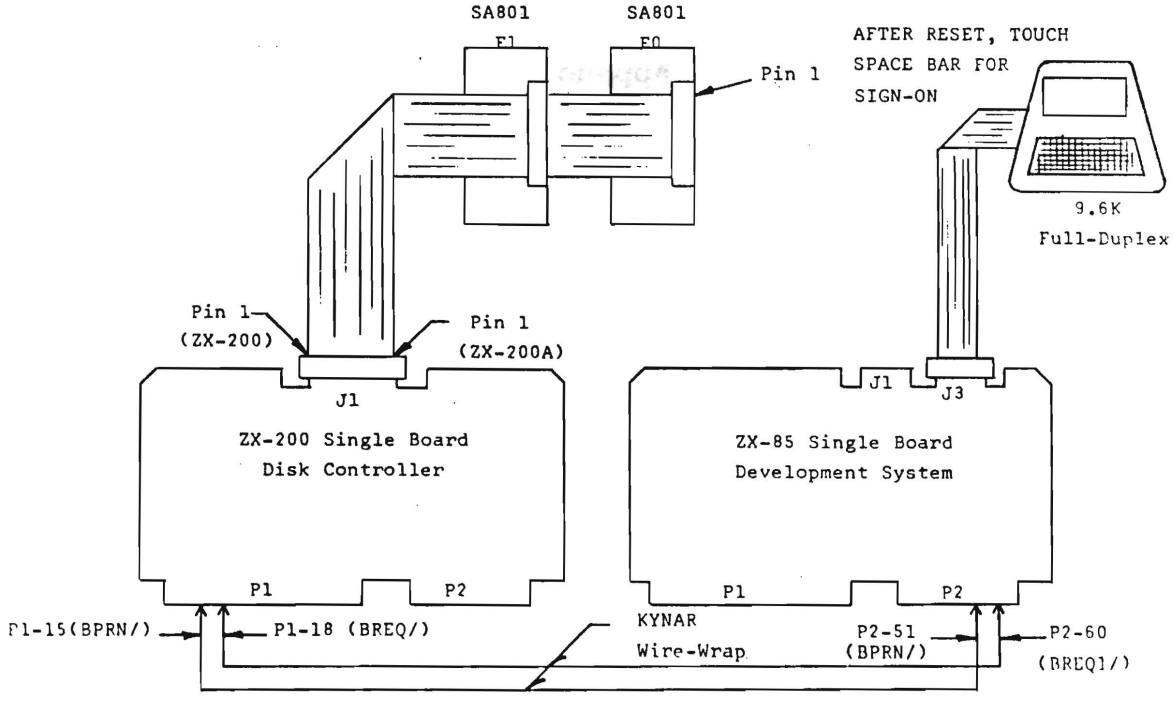
- to perform diskette reads and writes
- to be reset
- to stop permaturely a group of linked disk operations (in single density operation only)
- to render disket drive status to the CPU
- to indicate the result of an operation to the CPU

Each of the above operations is initiated by a CPU output to a specific port. There are two base addresses, one for single density operation and one for double density. (Although the ZX-200A CONTROLLER reads or writes in both densities, Intel has separate floppy disk controllers for each density.)

Note: The base port for the Intel single density controller is address 88H; the base port for the double density controller is at 78H.

Appendix

Figure A - ZX-85 Minimum Diskette System



ZX-85 MINIMUM DISKETTE SYSTEM

ZX-200A MAP 23 LISTING

Addr	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0000	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
0010	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
0020	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
0030	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
0040	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
0050	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
0060	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
0070	F	F	F	F	F	F	F	F	7	7	7	7	F	F	F	5
0080	F	F	F	F	F	F	F	F	A	A	A	A	F	F	F	9
0090	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
00A0	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
00B0	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
00C0	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
00D0	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
00E0	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
00F0	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F

Addr	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0100	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
0110	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
0120	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
0130	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
0140	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
0150	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
0160	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
0170	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
0180	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
0190	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
01A0	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
01B0	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
01C0	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
01D0	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
01E0	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
01F0	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F

ZX-200A MAP PROM LISTING

MAP 20

Addr	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0000	DD	DD	DD	DD	DD	DD	DD	DD	DD	DD	DD	DD	DD	DD	DD	DD
0010	DD	DD	DD	DD	DD	DD	DD	DD	DD	DD	E0	E0	E0	E0	E0	E0
0020	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0030	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0040	DF	DF	DE	DE	DE	DE	DD	DD	DD	DC	DC	DC	DC	DB	DB	DA
0050	DA	DA	DD	DD	DD	DD	DD	DD	DD	DD	DD	DD	DD	DD	DD	DD
0060	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0070	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0080	DD	DD	DD	DD	DD	DD	DD	DD	DD	DD	DD	DD	DD	DD	DD	DD
0090	DD	DD	DD	DD	DD	DD	DD	DD	DD	DD	E0	E0	E0	E0	E0	E0
00A0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
00B0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
00C0	DF	DF	DE	DE	DE	DE	DD	DD	DD	DC	DC	DC	DC	DB	DB	DA
00D0	DA	DA	DD	DD	DD	DD	DD	DD	DD	DD	DD	DD	DD	DD	DD	DD
00E0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
00F0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF

MAP 21

Addr	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0000	DD	5D	DD	5D	5D	DD	5D	D9	5D	5D	5D	5D	61	E1	61	DD
0010	DD	5D	DD	5D	5D	DD	5D	D9	59	5D	59	5D	5D	E1	5D	DD
0020	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0030	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0040	DD	5D	DF	5B	5D	DD	5D	D9	5D	5D	5D	5D	61	E1	61	DD
0050	DB	5F	DD	5D	5D	DD	5D	D9	59	5D	59	5D	5D	E1	5D	DD
0060	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0070	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0080	5D	5D	5D	5D	5D	DD	5D	D9	5D	5D	5D	5D	61	E1	61	DD
0090	5D	5D	5D	5D	5D	DD	5D	D9	59	5D	59	5D	5D	E1	5D	DD
00A0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
00B0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
00C0	DD	5D	DF	5B	5D	DD	5D	D9	5D	5D	5D	5D	61	E1	61	DD
00D0	DB	5F	DD	5D	5D	DD	5D	D9	59	5D	59	5D	5D	E1	5D	DD
00E0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
00F0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF

```
CP/M MACRO ASSEM 2.0    #001    ZX-200A FLOPPY CONTROLLER V1.2

                        TITLE   'ZX-200A FLOPPY CONTROLLER V1.2'
                        MACLIB  I8085
                ;$      MOD85
                ;$      XREF
                ;
                ;
                ;       REVISION: 10/02/81 BY S.R.
                ;       VERSION 1.2
                ;       LAST MODIFIED AUG 6, 1981
                ;       RICK MAIN, PGMR
                ;
                ;-----------------------------------------------------------------------
                ;
                ;       ZENDEX CORPORATION
                ;       6680 SIERRA LANE
                ;       DUBLIN, CA  94566
                ;               (415)829-1284
                ;
                ;               TWX 910-389-4009
                ;
                ;***************************************************************************
                ;
                ;       THIS PROGRAM IS ORGANIZED TO RUN IN THE ZENDEX
                ;       ZX-200A FLOPPY DISK CONTROLLER. THE FIRMWARE IS
                ;       CONTAINED IN A SINGLE 2716 EPROM.
                ;
                ;***************************************************************************
                ;
                ;       PORT EQUATES
                ;
                ;***************************************************************************
0066 =          RDSTAT  EQU     66H     ; READ FDD I/F STATUS
0066 =          WRCONT  EQU     66H     ; WRITE FDD I/F CONTROL
0067 =          RDRDY   EQU     67H     ; READ INT & FDD READY STATUS
0067 =          WRCNT1  EQU     67H     ; WRITE INT CLR & WR ENABLE, HEAD LOAD
0080 =          CLRINT  EQU     80H     ; CLEAR RST INTERRUPT FLIP-FLOP
2000 =          DMADDR  EQU     2000H   ; DMA BASE ADDRESS
2001 =          DMATC   EQU     2001H   ; DMA TERMINAL COUNT ADDRESS
2008 =          DMAMOD  EQU     2008H   ; DMA MODE SET REGISTER
6000 =          MRKCRC  EQU     6000H   ; READ/WRITE MARK/CRC BYTE
6100 =          MARK    EQU     6100H   ; READ/WRITE MARK
6200 =          DISKIO  EQU     6200H   ; IO DISK DATA
6300 =          WRCRC   EQU     6300H   ; WRITE CRC
6300 =          SYNCPL  EQU     6300H   ; READ SYNC PLO
6401 =          PORT8B  EQU     6401H   ; PORT 8B TO HOST
6402 =          PORT79  EQU     6402H   ; PORT 79 TO HOST
6403 =          PORT7B  EQU     6403H   ; PORT 7B TO HOST
6400 =          PORT89  EQU     6400H   ; PORT 89 TO HOST
6500 =          WRCLK   EQU     6500H   ; WRITE CLOCK
6500 =          RDPRT1  EQU     6500H   ; READ 4X4 FILE PORT

07FF                    ORG     7FFH    ; SET VERSION STAMP AT LAST ADDRESS
07FF 12                 DB      12H     ; FOR VERSION 1.2
0000                    ORG     0       ; BEGIN AT RESET POINT
                ZX202:
0000 DB80               IN      CLRINT  ; CLEAR INTERRUPTS TO HOST
```

```
0002 AF             XRA     A
0003 310042         LXI     SP,4200H        ; INITIALIZE STACK POINTER
0006 210040         LXI     H,CHANWD        ; CLEAR BUFFER, FLAGS
                    RAMCLR:
0009 77             MOV     M,A
000A 2C             INR     L
000B C20900         JNZ     RAMCLR  ; LOOP TILL BUFFER CLEARED
000E DB67           IN      RDRDY   ; READ INT. & FDD READY PORT
0010 E60F           ANI     0FH
0012 321440         STA     RDYBIT  ; READY STATUS
                    DSKCLR:
0015 3EFF           MVI     A,0FFH
0017 320D40         STA     UNIT
001A AF             XRA     A       ; CLEAR HOST INTERRUPTS AND UNLOAD HEAD
001B D367           OUT     WRCNT1
001D C35400         JMP     L54
                    ;
                    ;       TRAP INTERRUPT
                    ;
                    INDEX:                  ; TRAP INTERRUPT SOURCE FROM FDD INDEX MARK
0024                ORG     24H
0024 F5             PUSH    PSW
0025 C34A00         JMP     L4A
                    MA78:                   ; MEMORY ADDRESS UPPER WRITTEN BY HOST FOR SD
002C                ORG     2CH
002C 2A0165         LHLD    6501H   ; READ IOPB ADDRESS FROM 4X4
002F DB80           IN      CLRINT  ; RESET RST F-F
0031 C3C000         JMP     LC0
                    ;
                    ;       RESTART 6.5
                    ;
                    MA88:                   ; MEMORY ADDRESS UPPER WRITTEN BY HOST FOR DD
0034 2A0164         LHLD    PORT8B  ; READ IOPB ADDRESS FROM 4X4
0037 DB80           IN      CLRINT  ; RESET RST F-F
0039 C39C00         JMP     L9B
                    L3C:
                    STOP:                   ; STOP OPERATION INTERRUPT FOR SD DRIVES ON 88
003C                ORG     3CH
003C F5             PUSH    PSW
003D 3A0040         LDA     CHANWD  ; RESET LINK BIT IN IOPB CHANNEL WORD
0040 E6FB           ANI     NOT 4
0042 320040         STA     CHANWD
0045 3E10           MVI     A,10H   ; RESET RST 7.5 FF
                    SIM
0047+30             DB      30H
0048 F1             POP     PSW
0049 C9             RET
                    L4A:
004A 3A1340         LDA     INDXCT  ; DECREMENT INDEX COUNT FLAG BY ONE FOR EACH
004D 3D             DCR     A       ; REVOLUTION OF DISK, RST SOURCE INDEX MARK.
004E 321340         STA     INDXCT
                    RIM
0051+20             DB      20H
0052 F1             POP     PSW
0053 C9             RET
                    L54:
```

```
0054 3E08               MVI     A,8     ; OPEN UP ALL RST X.5 INTERRUPTS
0056 FB                 EI
                        SIM             ; SET INTERRUPT MASK
0057+30                 DB      30H
0058 DB67               IN      RDRDY   ; READ INT. & FDD READY PORT
005A 47                 MOV     B,A
005B E6C0               ANI     0C0H    ; ISOLATE INT PND BITS
005D C26A00             JNZ     L6A     ; JUMP IF INT PND
0060 78                 MOV     A,B
0061 E60F               ANI     0FH     ; ISOLATE DRIVE READY BITS
0063 211440             LXI     H,RDYBIT        ; READY STATUS
0066 BE                 CMP     M       ; SEE IF OLD READY=NEW READY
0067 C47400             CNZ     RDYINT  ; JUMP TO DO UPDATE/INTERRUPT IF NOT
                L6A:
006A 3A1340             LDA     INDXCT  ; INDEX COUNT
006D B7                 ORA     A       ; REV COUNT EXPIRED?
006E C25400             JNZ     L54     ; NO, LOOP
0071 C31500             JMP     DSKCLR  ; YES, DESELECT DISK UNIT
                ;
                ;       INTERRUPT HOST ON READY CHANGE
                ;
                RDYINT:
0074 4F                 MOV     C,A     ; FORMAT UNIT READY BITS
0075 0F                 RRC
0076 0F                 RRC
0077 47                 MOV     B,A
0078 79                 MOV     A,C
0079 07                 RLC
007A 07                 RLC
007B B0                 ORA     B
007C F60F               ORI     0FH
007E 2F                 CMA
007F 320164             STA     PORT8B  ; WRPORT 8B, SD RESULT BYTE
0082 320364             STA     PORT7B  ; WRPORT 7B, DD RESULT BYTE
0085 3E02               MVI     A,2     ; RESULT TYPE = 2
0087 320064             STA     PORT89  ; WRPORT 89  RESULT TYPE SD
008A 320264             STA     PORT79  ; WRPORT 79  RESULT TYPE DD
008D 3A0D40             LDA     UNIT    ; TEST FOR INITIALIZATION CODE
0090 3C                 INR     A       ; WAS IT FF?
0091 CA9600             JZ      L95     ; RESET WR2D IF INIT
0094 3E08               MVI     A,8     ; SET WR2D
                L95:                    ; SEND BOTH INTERRUPTS TO HOST
0096 F6C0               ORI     0C0H
0098 D367               OUT     WRCNT1
009A 71                 MOV     M,C
009B C9                 RET
                L9B:                    ; DD PROCEDURE
009C D1                 POP     D       ; DISCARD RST CALL RETURN
009D CD3901             CALL    L13A    ; CALL DD DISK OPERATION
00A0 320364             STA     PORT7B  ; STORE IN 7B, RESULT BYTE
00A3 3E00               MVI     A,0     ; STORE TYPE 0 RESULT
00A5 320264             STA     PORT79  ; PORT 79H(HOST)
00A8 3E04               MVI     A,04H   ; TURN OFF WRITE ENABLE
00AA D367               OUT     WRCNT1
00AC 3E08               MVI     A,8     ; DELAY DESELECT 8 DISK REVS
00AE 321340             STA     INDXCT  ; INDEX COUNT
```

```
00B1 3A0040          LDA     CHANWD  ; ISOLATE INTERRUPT CONTROL
00B4 E610            ANI     10H
00B6 C25400          JNZ     L54     ; RETURN TO MAINLINE IF DISABLED
00B9 3E44            MVI     A,44H
00BB D367            OUT     WRCNT1  ; OTHERWISE SET INT 78
00BD C35400          JMP     L54
                LC0:                 ; SD PROCEDURE
00C0 D1              POP     D       ; DISCARD RST CALL RETURN
                LC1:
00C1 F3              DI              ; DISABLE ALL BUT INDEX TRAP
00C2 CD6101          CALL    L162    ; DO SD DISK OPERATION
00C5 F5              PUSH    PSW     ; SAVE RESULT CODE ON STACK
00C6 320164          STA     PORT8B  ; WRITE RESULT BYTE TO HOST PORT 8BH
00C9 3A0040          LDA     CHANWD
00CC 47              MOV     B,A
00CD E604            ANI     4       ; ISOLATE SUCCESSOR BIT
00CF CAD900          JZ      LODA
00D2 3A0740          LDA     BLOCKN  ; BLOCK NUMBER
00D5 07              RLC             ; MERGE ADJUSTED BLOCK NUMBER IN RESULT TYPE
00D6 07              RLC
00D7 F603            ORI     3       ; EVENTUAL TYPE 2
                LODA:
00D9 3D              DCR     A       ; FINAL RESULT TYPE
00DA 2F              CMA
00DB 320064          STA     PORT89  ; WRITE FOR HOST READ PORT 89H
00DE F1              POP     PSW     ; POP ERROR CODE TO ACC
00DF B7              ORA     A       ; ERRORS=NOT 0
00E0 C43C00          CNZ     STOP    ; CALL LINK CANCEL IF ERROR
00E3 3E0D            MVI     A,0DH   ; MASK ALL BUT RST 6.5(SD CMD)
00E5 FB              EI
                     SIM             ; SET INTERRUPT MASK
00E6+30              DB      30H
00E7 3E04            MVI     A,4
00E9 D367            OUT     WRCNT1  ; CLEAR WRITE ENABLE
00EB 3E08            MVI     A,8
00ED 321340          STA     INDXCT  ; INDEX COUNT
00F0 78              MOV     A,B     ; SAVE CHANWD ON STACK
00F1 F5              PUSH    PSW
00F2 07              RLC             ; TEST LOCK OVERRIDE BIT
00F3 DA0701          JC      L108    ; JUMP IF OVERRIDE SET
00F6 2A0B40          LHLD    400BH   ; SET WAIT BIT IN HOST IOPB CHANWD
00F9 E5              PUSH    H
00FA 2643            MVI     H,43H   ; INDEX 2114 BUFFER
00FC 0F              RRC
00FD F601            ORI     1       ; SET WAIT BIT
00FF 77              MOV     M,A     ; PUT BACK IN 2114 BUFFER
0100 E1              POP     H
0101 010040          LXI     B,CHANWD
0104 CDF901          CALL    DMALOD  ; USE DMAC TO WRITE HOST
                L108:
0107 F1              POP     PSW     ; POP CHANWD
0108 47              MOV     B,A
0109 E620            ANI     20H     ; ISOLATE INTERRUPT CONTROL
010B C21D01          JNZ     L11E    ; JUMP IF INTERRUPT NEEDED BY HOST
010E 2A0840          LHLD    NXIOPB  ; NEXT IOPB ADDRESS
0111 78              MOV     A,B
```

```
0112 E604           ANI     4       ; ISOLATE SUCCESSOR BIT IN CHANWD
0114 C2C100         JNZ     LC1     ; JUMP IF LINKED
0117 78             MOV     A,B
0118 E610           ANI     10H     ; ISOLATE INTERRUPT DISABLE BIT
011A C25400         JNZ     54H     ; JUMP IF INTERRUPTS DISABLED
                L11E:
011D 3E84           MVI     A,84H   ; SET INTERRUPT 88
011F D367           OUT     WRCNT1
                L122:
0121 3A0040         LDA     CHANWD  ; ISOLATE SUCCESSOR BIT
0124 E604           ANI     4
0126 CA5400         JZ      L54     ; RETURN TO IDLE LOOP IF NOT LINKED
0129 3E0A           MVI     A,0AH   ; SET RST 6.5 MASK
                    SIM
012B+30             DB      30H
012C DB67           IN      RDRDY   ; READ INT. & FDD READY PORT
012E E680           ANI     80H     ; ISOLATE INT 88 BIT
0130 C22101         JNZ     L122    ; LOOP TILL FALSE, HOST MUST ACK
0133 2A0840         LHLD    NXIOPB  ; NEXT IOPB ADDRESS
0136 C3C100         JMP     LC1
                L13A:
0139 CDE301         CALL    L1D7    ; FETCH IOPB FROM HOST TO BUFFER
013C 3A0140         LDA     DKINST  ; LOAD UNIT NO. SELECTED BY HOST
013F 0F             RRC
0140 0F             RRC
0141 0F             RRC
0142 0F             RRC
0143 E603           ANI     3       ; ISOLATE UNIT NUMBER
0145 4F             MOV     C,A     ; SAVE  IN C
0146 1E04           MVI     E,4     ; SEND DD MODE TO WRCONT1 PORT
0148 3E0B           MVI     A,0BH   ; SPECIFY DD DATA ADDRESS MARK
014A 321640         STA     DAMARK  ; DATA ADDRESS MARK STORE
014D 3EFF           MVI     A,0FFH  ; SET DD FLAG MODE
014F C38401         JMP     L185    ; GO AROUND L153
                L153:
0152 2A0840         LHLD    NXIOPB  ; NEXT IOPB ADDRESS
0155 0F             RRC             ; TEST BRANCH BIT
0156 DA6101         JC      L162    ; IF SET, BRANCH TO LINKED IOPB
0159 060A           MVI     B,0AH   ; OTHERWISE IDLE 10 MS
015B CDBF02         CALL    DELAY
015E 2A0B40         LHLD    400BH   ; RESTORE ORIGINAL IOPB ADDRESS
                L162:
0161 220B40         SHLD    400BH   ; SAVE AS ADDRESS OF IOPB TO EXECUTE
0164 CDE301         CALL    L1D7    ; MOVE HOST IOPB TO OUR BUFFER
0167 3A0040         LDA     CHANWD  ; FETCH CHANNEL WORD
016A 0F             RRC
016B DA5201         JC      L153    ; JUMP IF WAIT BIT SET
016E 3A0140         LDA     DKINST  ; FETCH OPCODE
0171 0F             RRC             ; POSITION & ISOLATE UNIT SELECT BITS
0172 0F             RRC
0173 0F             RRC
0174 E606           ANI     6
0176 4F             MOV     C,A     ; INTERMEDIATE TO C
0177 0F             RRC
0178 A9             XRA     C       ; COMBINE
0179 E603           ANI     3       ; MASK 00=0, 11=1, 01&10 ILLEGAL
```

```
017B 4F              MOV     C,A
017C 1E05            MVI     E,05H   ; SEND SD MODE CONTROL TO WRCONT1 PORT
017E 3EFB            MVI     A,0FBH  ; SPECIFY SD DATA ADDRESS MARK, FOR USE LATER
0180 321640          STA     DAMARK  ; DATA ADDRESS MARK
0183 AF              XRA     A       ; ACC=0,  FLAG SD OPERATION
                L185:
0184 321240          STA     DDSDFL  ; STORE SD/DD FLAG PASSED IN ACC.
0187 21DB01          LXI     H,UNITAB        ; DO INDEX TO UNIT SELECT TABLE
018A 0600            MVI     B,0     ; MSD=0
018C 09              DAD     B       ; DOUBLE INDEX, TWO ENTRIES PER ITEM
018D 09              DAD     B
018E 56              MOV     D,M     ; MOVE SELECT CODE TO D
018F DB67            IN      RDRDY   ; READ INT. & FDD READY PORT
0191 A2              ANA     D       ; TEST FOR READY ERROR
0192 3E80            MVI     A,80H   ; ANTICIPATE BY WRITING ERROR CODE IN ACC.
0194 C0              RNZ             ; RETURN IF READY ERROR
0195 C5              PUSH    B
0196 23              INX     H       ; OTHERWISE FETCH NEXT ITEM IN UNIT TABLE
0197 7E              MOV     A,M
0198 D366            OUT     WRCONT  ; WRITE FDD CONTROL PORT TO SELECT THAT DRIVE
019A 320A40          STA     400AH   ; ALSO SAVE SELECT CODE FOR LATER USE
019D 3A0D40          LDA     UNIT    ; FETCH LAST UNIT CODE
01A0 B9              CMP     C       ; SAME?
01A1 79              MOV     A,C
01A2 320D40          STA     UNIT    ; SAVE NEW CODE
01A5 7B              MOV     A,E     ; SET DD OR SD MODE AND HEAD LOAD
01A6 D367            OUT     WRCNT1
01A8 0623            MVI     B,23H   ; CALL DELAY FOR HEAD TO SETTLE IF NEW UNIT
01AA C4BF02          CNZ     DELAY
01AD C1              POP     B
01AE 211A40          LXI     H,401AH
01B1 09              DAD     B
01B2 7E              MOV     A,M
01B3 36FF            MVI     M,0FFH
01B5 B7              ORA     A
01B6 CCD502          CZ      RECAL
01B9 21CB01          LXI     H,CTAB  ; BASE INDEX TO COMMAND TABLE
01BC 3A0140          LDA     DKINST  ; FETCH OPCODE
01BF 07              RLC             ; INDEX BY TWO'S
01C0 E60E            ANI     0EH     ; ISOLATE OPCODE BITS
01C2 5F              MOV     E,A     ; ADD TO CTAB BASE ADDRESS
01C3 1600            MVI     D,0
01C5 19              DAD     D
01C6 5E              MOV     E,M
01C7 23              INX     H
01C8 56              MOV     D,M
01C9 EB              XCHG
01CA E9              PCHL            ; JUMP TO COMMAND PROCEDURE
                CTAB:
01CB 0D02            DW      L20C    ; NOP
01CD 7C02            DW      SEEK    ; SEEK
01CF 1605            DW      FORMAT  ; FORMAT
01D1 D502            DW      RECAL   ; RECALIBRATE
01D3 F702            DW      READ    ; READ
01D5 F702            DW      READ    ; VERIFY CRC
01D7 0203            DW      WRITE   ; WRITE
```

```
01D9 FB02               DW      WRITDL  ; WRITE DELETED DATA
                UNITAB:
01DB 01                 DB      1       ; UNIT 1
01DC BF                 DB      NOT 40H
01DD 02                 DB      2       ; UNIT 2
01DE DF                 DB      NOT 20H
01DF 04                 DB      4       ; UNIT 3
01E0 EF                 DB      NOT 10H
01E1 08                 DB      8       ; UNIT 4
01E2 F7                 DB      NOT 8

                L1D7:
01E3 010980             LXI     B,8009H ; SELECT HOST READ, 9 BYTES
01E6 CDF901             CALL    DMALOD  ; INVOKE DMA TRANSFER
01E9 2643               MVI     H,43H   ; ADDRESS ON-BOARD BUFFER
01EB 110040             LXI     D,CHANWD        ; POINT TO IOPB CHANNEL WORD
01EE 0E0A               MVI     C,10    ; MOVE 10 BYTES FROM DMA BUFFER TO IOPB ARRAY
                L1E6:
01F0 7E                 MOV     A,M     ; READ BUFFER
01F1 12                 STAX    D       ; STORE AT IOPB
01F2 13                 INX     D       ; ADJUST POINTERS
01F3 2C                 INR     L
01F4 0D                 DCR     C       ; DECREMENT COUNTER
01F5 C2F001             JNZ     L1E6
01F8 C9                 RET
                DMALOD:
01F9 97                 SUB     A
01FA D365               OUT     65H     ; CLR EXTENDED ADDRESS
01FC E5                 PUSH    H       ; SAVE HL
01FD EB                 XCHG
01FE 210020             LXI     H,DMADDR        ; SEND TO 8257 DMA REG PORT
0201 73                 MOV     M,E
0202 72                 MOV     M,D
0203 23                 INX     H               ; POINT TO TC PORT
0204 71                 MOV     M,C     ; WRITE TC AND CYCLE CODE
0205 70                 MOV     M,B
0206 3E41               MVI     A,41H   ; WRITE MODE WORD, TC STOP BIT & CHAN. 0 ENABLE
0208 320820             STA     DMAMOD
020B E1                 POP     H       ; RESTORE DMA ADDRESS
020C C9                 RET
                L20C:
020D CD7C02             CALL    SEEK    ; DO SEEK
0210 B7                 ORA     A       ; TEST ERROR
0211 C0                 RNZ             ; RETURN IF ERROR
0212 3A0240             LDA     NUMRCD  ; LOAD # RECORDS
0215 E607               ANI     7
0217 07                 RLC
0218 4F                 MOV     C,A
0219 0600               MVI     B,0
021B 212402             LXI     H,L223
021E 09                 DAD     B
021F 5E                 MOV     E,M
0220 23                 INX     H
0221 56                 MOV     D,M
0222 EB                 XCHG
0223 E9                 PCHL            ; EXECUTE PROCEDURE
```

```
                L223:
0224 3402               DW      L233
0226 3B02               DW      L23A
0228 4102               DW      L240
022A 4702               DW      L246
022C 5702               DW      L256
022E 5C02               DW      L25B
0230 6302               DW      L262
0232 6802               DW      L267
                L233:
0234 110062             LXI     D,DISKIO        ; RD DISK
0237 1A         L236:   LDAX    D       ; RD DISK + X
0238 C33702             JMP     L236    ; LOOP
                L23A:
023B 110061             LXI     D,6100H ; RDMRKA
023E C33702             JMP     L236    ; GO INTO LOOP
                L240:
0241 110062             LXI     D,DISKIO        ; RD DISK
0244 C34A02             JMP     L249
                L246:
0247 110061             LXI     D,MARK  ; RDMRKA
024A D5         L249:   PUSH    D
024B CDE602             CALL    WRENBL  ; ENABLE WRITE CONTROLS
024E D1                 POP     D
024F C8                 RZ              ; RETURN IF WRITE PROTECTED
0250 3A0440             LDA     SCTADR  ; LOAD SECTOR ADDRESS
                L252:
0253 12                 STAX    D       ; WRMRK(CRC)
0254 C35302             JMP     L252
                L256:
0257 0E00               MVI     C,0
0259 C35E02             JMP     L25D
                L25B:
025C 0EFF               MVI     C,0FFH  ; DMA 256 BYTES
                L25D:
025E 0680               MVI     B,80H   ; READ FROM HOST RAM
0260 C36C02             JMP     L26B
                L262:
0263 0E00               MVI     C,0     ; NO DATA TRANSFER
0265 C36A02             JMP     L269
                L267:
0268 0EFF               MVI     C,0FFH  ; 256 BYTES
                L269:
026A 0640               MVI     B,40H   ; WRITE TO HOST RAM
                L26B:
026C C5                 PUSH    B
026D 0EFF               MVI     C,0FFH  ; 256 BYTES
026F 2A0540             LHLD    BUFFER  ; LOAD BUFFER ADDRESS
0272 CDF901             CALL    DMALOD  ; MOVE DATA
0275 C1                 POP     B       ; RESTORE BC
0276 AF                 XRA     A       ; ACC=0
0277 B1                 ORA     C
0278 C26C02             JNZ     L26B    ; JUMP IF NOT A VERIFY CYCLE
027B C9                 RET
;*****************************************************************************
;
```

```
                ;       SEEK A TRACK- THE BYTE IN TRKADR IS USED TO DETERMINE THE
                ;       THE TARGET TRACK TO STEP TO. IF ZERO RECALIBRATE IS USED
                ;       INSTEAD. ENTERED DIRECTLY AS A HOST COMMAND OR AS A PRELUDE
                ;       TO ANOTHER OPERATION FOR IMPLIED SEEK.
                ;
                SEEK:
027C 3A0340             LDA     TRKADR  ; SEEK OPERATION.  FETCH TARGET TRACK ADDRESS
027F B7                 ORA     A       ; ZERO?
0280 CAD502             JZ      RECAL   ; DO RECAL IF ZERO
0283 57                 MOV     D,A     ; TRK ADR TO D
0284 FE4D               CPI     4DH     ; TEST FOR ILLEGAL TRACK
0286 3E08               MVI     A,8     ; ANTICIPATE WITH ERROR CODE
0288 D0                 RNC             ; RETURN IF ERROR
0289 7A                 MOV     A,D     ; TRK ADR TO ACC.
028A FE2B               CPI     2BH     ; TRK>43?
028C DA9602             JC      S1      ; JUMP IF NOT
028F 210A40             LXI     H,400AH
0292 7E                 MOV     A,M
0293 E6FB               ANI     0FBH    ; SET LO CURR BIT
0295 77                 MOV     M,A
                S1:
0296 CDCA02             CALL    TRKREG  ; SET HL = TRK REG
                S2:
0299 7A                 MOV     A,D     ; TRK ADR TO ACC.
029A 96                 SUB     M       ; COMPARE TARGET TRACK TO DESTINATION TRACK
029B C8                 RZ              ; RETURN WHEN EQUAL
029C CDA202             CALL    STEP    ; DO A STEP OF HEAD
029F C39902             JMP     S2      ; LOOP
                STEP:
02A2 3A0A40             LDA     400AH   ; LOAD UNIT SELECT
02A5 DAAC02             JC      L2AB    ; JUMP TO DO STEP OUT
02A8 E6FD               ANI     0FDH    ; ELSE STEP IN
02AA 34                 INR     M       ; INCREMENT CURRENT TRACK
02AB 34                 INR     M
                L2AB:
02AC 35                 DCR     M       ; DECREMENT CURRENT TRACK
02AD D366               OUT     WRCONT  ; WRITE FDD CONTROL PORT        ; STEP=1
02AF 3D                 DCR     A
02B0 00                 NOP
02B1 D366               OUT     WRCONT  ; WRITE FDD CONTROL PORT, STEP=0
02B3 00                 NOP
02B4 F601               ORI     1
02B6 D366               OUT     WRCONT  ; WRITE FDD CNT PORT, STEP=1
02B8 00                 NOP
02B9 F602               ORI     2
02BB D366               OUT     WRCONT  ; WRITE FDD CONTROL PORT, DIR=1
                TENMS:                  ; 10 MS TIMING FOR STEP RATE
02BD 0608               MVI     B,8
                DELAY:
02BF 0ED6               MVI     C,0D6H  ; DELAY LOOP
                L2B9:
02C1 0D                 DCR     C
02C2 C2C102             JNZ     L2B9
02C5 05                 DCR     B
02C6 C2BF02             JNZ     DELAY
02C9 C9                 RET
```

```
                ;
                ;       ADDRESS CURRENT UNIT'S TRACK ADDRESS REGISTER, POINTER RETURNED
                ;       IN HL.
                ;
                TRKREG:
02CA 210E40             LXI     H,TRKRG0        ; TRACK REGISTER, UNIT 0, INDEX BASE ADD.
02CD 3A0D40             LDA     UNIT    ; FETCH REQUESTED UNIT NUMBER
02D0 4F                 MOV     C,A     ; ADD TO INDEX
02D1 0600               MVI     B,0
02D3 09                 DAD     B       ; INDEX # ADDED TO BASE= TARGET TRK CURRENT REG
02D4 C9                 RET

                ;*******************************************************************************
                ;
                ;       RECALIBRATE HEAD TO TRACK 0. THE FDD IS STEPPED UNTIL
                ;       THE TRK 0 SIGNAL GOES TRUE FROM THE FDD I/F.
                ;
                RECAL:                  ; RECALIBRATE COMMAND
02D5 CDCA02             CALL    TRKREG  ; SET HL=TRK REG
                L2D0:
02D8 3600               MVI     M,0     ; ZERO TRK REG
02DA DB66               IN      RDSTAT  ; READ FDD STATUS PORT
02DC E640               ANI     40H     ; ISOLATE TRK 0 SIGNAL FROM FDD
02DE C8                 RZ              ; RETURN WHEN TRK=0
02DF 37                 STC             ; SET FLAG FOR STEP
02E0 CDA202             CALL    STEP    ; DO A STEP
02E3 C3D802             JMP     L2D0
                ;*******************************************************************************
                ;
                ;       WRENBL- SET WRITE ENABLE CONTROL TO FDD, LOAD HEAD, TEST
                ;       WRITE PROTECT SIGNAL FROM FDD. IF PROTECTED RETURN ZERO
                ;       FLAG IN ACC SET.
                ;
                WRENBL:
02E6 3A1240             LDA     DDSDFL
02E9 2F                 CMA
02EA E601               ANI     1       ; ISOLATE SD/DD BIT
02EC F606               ORI     6       ; SET WRENA & HEAD LOAD BITS
02EE D367               OUT     WRCNT1  ; WRITE CONTROL PORT
02F0 DB66               IN      RDSTAT  ; READ FDD STATUS PORT
02F2 E620               ANI     20H     ; ISOLATE WRITE PROTECT LINE
02F4 3E20               MVI     A,20H
02F6 C9                 RET             ; RETURN WITH FLAGS SET
                ;*******************************************************************************
                ;
                ;       READ, WRITE, WRITDL- SET RWFLG, SEEK THE TRACK, TEST SECTOR
                ;       ADDRESSING AND RECORD COUNT. RETURN WITH ADDRESS ERROR IF
                ;       SCTADR BAD OR COUNT (NUMRCD) TOO LARGE (MULTI-TRACK).
                ;
                READ:
02F7 AF                 XRA     A       ; READ, VERIFY CRC COMMAND
02F8 C30803             JMP     L300
                WRITDL:
02FB 211640             LXI     H,4016H ; FIX FLAG, WRITE DELETED COMMAND
02FE 7E                 MOV     A,M
02FF E6F8               ANI     NOT 7
```

```
0301 77              MOV     M,A
                WRITE:
0302 CDE602          CALL    WRENBL  ; WRITE COMMAND, CALL WR ENABLE
0305 C8              RZ              ; RETURN ERROR IF WRITE PROTECTED
0306 3EFF            MVI     A,0FFH  ; SET FLAG
                L300:
0308 321540          STA     RWFLG   ; READ WRITE FLAG       ; STORE FLAG
030B CD7C02          CALL    SEEK    ; FIX CNTL, DO SEEK
030E B7              ORA     A
030F C0              RNZ             ; RETURN IF SEEK ERROR
0310 210440          LXI     H,SCTADR        ; POINT TO SECTOR ADDRESS
0313 0636            MVI     B,36H   ; DD EOT SECTOR +1
0315 3A1240          LDA     DDSDFL  ; TEST FOR DD
0318 B7              ORA     A
0319 7E              MOV     A,M     ; FETCH SECTOR ADDRESS
031A C22203          JNZ     L31A    ; JUMP IF DD
031D E61F            ANI     1FH     ; ISOLATE LEGAL SD SECTOR ADDRESSES
031F 77              MOV     M,A     ; RESTORE CORRECTED ADDR
0320 061C            MVI     B,1CH   ; MAX SD ADDR +1
                L31A:
0322 3C              INR     A
0323 321940          STA     FLAGD   ; STORE NEXT SECTOR ADDRESS
0326 3D              DCR     A       ; TEST FOR ZERO
0327 3E08            MVI     A,8     ; ANTICIPATE ADDRESS ERROR
0329 C8              RZ              ; RETURN IF SECTOR ADDR=0, ILLEGAL
032A 110240          LXI     D,NUMRCD        ; FETCH # RECORDS
032D 1A              LDAX    D
032E 86              ADD     M       ; ADD ADDRESS TO # OF RECORDS
032F B8              CMP     B       ; TOO MUCH?
0330 3E08            MVI     A,8     ; ANTICIPATE ERROR
0332 D0              RNC             ; RETURN ERROR IF TOO MUCH
0333 1A              LDAX    D       ; LOAD AGAIN # RECORDS
0334 B7              ORA     A
0335 1F              RAR
0336 321840          STA     FLAGC
0339 CE00            ACI     0
033B 12              STAX    D
                L334:
033C AF              XRA     A
033D 321740          STA     FLAGB
0340 2A0540          LHLD    BUFFER  ; LOAD BUFFER ADDR
0343 017F80          LXI     B,807FH ; DMA CYCLE, TC
0346 3A1540          LDA     RWFLG   ; READ WRITE FLAG, FLAG =0 FOR READ, NZ FOR WRITE
0349 B7              ORA     A
034A C4F901          CNZ     DMALOD  ; DMA LOAD UP
034D 3E04            MVI     A,4     ; COUNT FOUR DISK REVS
034F 321340          STA     INDXCT  ; INDEX COUNT
                L34A:
0352 210065          LXI     H,6500H
0355 110062          LXI     D,DISKIO
0358 3A1240          LDA     DDSDFL
035B B7              ORA     A
035C CAA704          JZ      L49B
                L357:
035F 3600            MVI     M,0     ; WRCLK
0361 DB66            IN      RDSTAT  ; READ FDD STATUS PORT
```

```
                L35B:
0363 3A1340             LDA     INDXCT  ; INDEX COUNT
0366 B7                 ORA     A
0367 FA6604             JM      L45F
                L362:
036A 04                 INR     B
036B CA6303             JZ      L35B
036E 3A0063             LDA     SYNCPL  ; SYNCHPLO
0371 3C                 INR     A
0372 C26A03             JNZ     L362
0375 0E06               MVI     C,06
                L36F:
0377 1A                 LDAX    D       ; DISKRD
0378 3C                 INR     A
0379 C26A03             JNZ     L362
037C 0D                 DCR     C
037D C27703             JNZ     L36F
0380 3670               MVI     M,070H
0382 1A                 LDAX    D       ; DISKRD
0383 3A0061             LDA     MARK    ; RDMRKA
0386 FE0E               CPI     0EH     ; I.D. ADDRESS MARK?
0388 C25F03             JNZ     L357    ; NO, JUMP, TRY AGAIN
                ;
                ;       READ I.D. RECORD
                ;
                L383:
038B 1A                 LDAX    D       ; READ TRACK I.D.
038C 210340             LXI     H,TRKADR        ; COMPARE TRK
038F BE                 CMP     M
0390 C26E04             JNZ     L467
0393 1A                 LDAX    D       ; DISKRD, DISCARD SIDE I.D.
0394 23                 INX     H       ; COMPARE SECTOR ADDR
0395 1A                 LDAX    D       ; DISK READ, SECTOR I.D.
0396 BE                 CMP     M
0397 C25203             JNZ     L34A
039A 1A                 LDAX    D       ; READ SECTOR LENGHT CODE
039B 1A                 LDAX    D       ; READ CRC BYTES
039C 1A                 LDAX    D
039D 1A                 LDAX    D
039E DB66               IN      RDSTAT  ; READ FDD STATUS PORT
03A0 17                 RAL             ; CRCSTAT?
03A1 DA8804             JC      L481    ; JUMP CRC ERROR
03A4 1A                 LDAX    D       ; DISKRD
03A5 34                 INR     M       ; INX SECTOR ADR
03A6 34                 INR     M
03A7 1A                 LDAX    D       ; DISKRD
03A8 3A1240             LDA     DDSDFL  ; TEST SD/DD MODE
03AB B7                 ORA     A
03AC CADF04             JZ      L4D3    ; JUMP IF SD
03AF 1A                 LDAX    D       ; DISKRD
03B0 3A1540             LDA     RWFLG   ; READ WRITE FLAG TEST
03B3 B7                 ORA     A
03B4 C20104             JNZ     L3FB    ; JUMP IF WRITE
03B7 0612               MVI     B,12H
                L3B1:
03B9 1A                 LDAX    D       ; DISKRD
```

```
03BA 05                 DCR     B
03BB C2B903             JNZ     L3B1
03BE 1A                 LDAX    D
03BF 210065             LXI     H,6500H
03C2 3600               MVI     M,0     ; MAKE SYNCHMARK=0
                L3BC:
03C4 00                 NOP
                L3BD:
03C5 3A0063             LDA     SYNCPL  ; SYNCPLO
03C8 3C                 INR     A
03C9 C2C403             JNZ     L3BC
03CC 3670               MVI     M,70H   ; SYNCHMARK=70H
03CE 1A                 LDAX    D
03CF 3A0061             LDA     MARK    ; READ DATA ADDDRESS MARK
03D2 FE0B               CPI     0BH     ; GOOD?
03D4 C29004             JNZ     L489    ; JUMP IF BAD
                ;
                ;       READ DISK RECORD INTO 2114 BUFFER
                ;
                L3CF:
03D7 2A0540             LHLD    BUFFER  ; LOAD BUFFER ADDRESS
03DA 2643               MVI     H,43H
03DC 1A                 LDAX    D       ; READ BYTE ONE
03DD 77                 MOV     M,A     ; STORE IN 2114
03DE 0E7F               MVI     C,7FH   ; SET UP LOOP FOR 127 MORE
                L3D9:
03E0 2C                 INR     L       ; ADJUST 2114 POINTER
03E1 1A                 LDAX    D       ; READ DISK BYTE
03E2 77                 MOV     M,A     ; STORE IN 2114
03E3 0D                 DCR     C
03E4 C2E003             JNZ     L3D9
03E7 1A                 LDAX    D       ; READ CRC BYTES
03E8 1A                 LDAX    D
03E9 1A                 LDAX    D       ; GAP 3 READ
03EA DB66               IN      RDSTAT  ; READ FDD STATUS PORT
03EC 17                 RAL             ; CRCSTAT?
03ED 3E02               MVI     A,2     ; ANTICIPATE CRC ERROR
03EF D8                 RC              ; RETURN IF ERROR
03F0 2A0540             LHLD    BUFFER  ; LOAD BUFFER ADDR
03F3 017F40             LXI     B,407FH ; READ CYCLE, TC, FOR READ COMMAND TO DMAC
03F6 3A0140             LDA     DKINST  ; FETCH OPCODE
03F9 E601               ANI     1       ; SEE IF DATA TRANSFER TYPE
03FB CCF901             CZ      DMALOD  ; LOAD DMAC CHIP
03FE C33B04             JMP     L432
                ;
                ;       WRITE A DISK RECORD, SPLICE GAP 2
                ;
                L3FB:
0401 1A                 LDAX    D       ; READ GAP 2 BYTE
0402 0E09               MVI     C,9
                L3FE:
0404 1A                 LDAX    D       ; READ GAP 2
0405 0D                 DCR     C       ; DECREMENT LOOP
0406 C20404             JNZ     L3FE    ; LOOP TEN TIMES
0409 12                 STAX    D       ; SPLICE IN SAME BYTE READ
040A 12                 STAX    D
```

```
040B 3EFF               MVI     A,0FFH  ; NOW WRITE FF SYNC IN SPLICE
040D 0E08               MVI     C,8
                L409:
040F 12                 STAX    D       ; WRITE 9 BYTES OF FF
0410 0D                 DCR     C
0411 C20F04             JNZ     L409
0414 010061             LXI     B,MARK  ; POINT TO WRMRK
                ;
                ;       WRITE DISK FROM 2114 BUFFER
                ;
                L411:
0417 12                 STAX    D       ; ONE MORE SPLICE BYTE
0418 2A0540             LHLD    BUFFER  ; LOAD BUFFER ADDRESS
041B 2643               MVI     H,43H
041D 12                 STAX    D       ; LAST SPLICE BYTE
041E 3A1640             LDA     DAMARK  ; DATA ADDRESS MARK
0421 02                 STAX    B       ; WRMRK
0422 7E                 MOV     A,M     ; READ BUFFER
0423 12                 STAX    D       ; WRITE FIRST DATA BYTE
0424 0E7F               MVI     C,127   ; LOOP COUNT ONE SECTOR
                L421:                   ; WRITE REMAINING 127 FROM LOOP
0426 2C                 INR     L
0427 7E                 MOV     A,M     ; READ BUFFER
0428 12                 STAX    D       ; WRITE DATA TO DISK
0429 0D                 DCR     C
042A C22604             JNZ     L421
042D 320063             STA     WRCRC   ; WRITE TWO CRC BYTES
0430 3A1240             LDA     4012H
0433 2F                 CMA
0434 320063             STA     WRCRC   ; WRCRC (WRITE CRC BYTE)
0437 12                 STAX    D       ; SPLICE GAP 3
0438 12                 STAX    D
0439 12                 STAX    D
043A 12                 STAX    D
                L432:
043B 210640             LXI     H,BUFFER+1      ; BUFFER MSD
043E 34                 INR     M               ; ADVANCE BUFFER ADDRESS BY ONE BLOCK
043F 210240             LXI     H,NUMRCD
0442 35                 DCR     M               ; DCR # RECORDS
0443 C23C03             JNZ     L334
0446 111840             LXI     D,FLAGC
0449 1A                 LDAX    D
044A B7                 ORA     A
044B C8                 RZ
044C 77                 MOV     M,A
044D AF                 XRA     A       ; A=0
044E 12                 STAX    D
044F 3A1940             LDA     FLAGD
0452 210440             LXI     H,SCTADR
0455 56                 MOV     D,M     ; FETCH SECTOR ADDR
0456 77                 MOV     M,A     ; REPLACE IT
0457 92                 SUB     D
0458 1F                 RAR
0459 57                 MOV     D,A
045A 1E80               MVI     E,128
045C 2A0540             LHLD    BUFFER  ; INX BUFFER ADDR ONE SECTOR COUNT
```

```
045F 19              DAD     D
0460 220540          SHLD    BUFFER
0463 C33C03          JMP     L334
                L45F:
0466 3A1740          LDA     FLAGB
0469 B7              ORA     A
046A C0              RNZ
046B 3E0E            MVI     A,0EH
046D C9              RET
                L467:
046E 1A              LDAX    D
046F 1A              LDAX    D
0470 1A              LDAX    D
0471 1A              LDAX    D
0472 1A              LDAX    D
0473 1A              LDAX    D       ; SIXTH TIME
                L46D:
0474 DB66            IN      RDSTAT
0476 17              RAL             ; CRCSTAT?
0477 DA8804          JC      L481    ; JUMP CRC ERROR
047A 3E04            MVI     A,04
047C 321740          STA     FLAGB
047F CDD502          CALL    RECAL
0482 CD7C02          CALL    SEEK
0485 C35203          JMP     L34A
                L481:
0488 3E0A            MVI     A,0AH
048A 321740          STA     FLAGB
048D C35203          JMP     L34A
                L489:
0490 FE08            CPI     08H
0492 C39704          JMP     L4A2
                L48E:
0495 FEF8            CPI     0F8H
                L4A2:
0497 3E0F            MVI     A,0FH
                L492:
0499 321740          STA     FLAGB
049C 3E01            MVI     A,1
049E C8              RZ
049F 210440          LXI     H,4004H
04A2 35              DCR     M
04A3 35              DCR     M
04A4 C35203          JMP     L34A
                L49B:                   ; SINGLE DENSITY WRITE
04A7 36FF            MVI     M,0FFH
                L49D:
04A9 3A1340          LDA     INDXCT  ; INDEX COUNT
04AC B7              ORA     A
04AD FA6604          JM      L45F
                L4A4:
04B0 04              INR     B       ; INX LOOP COUNT
04B1 CAA904          JZ      L49D
04B4 3A0063          LDA     SYNCPL  ; SYNCPLO
04B7 B7              ORA     A
04B8 C2B004          JNZ     L4A4    ; LOOP TILL 00 READ
```

```
                L4AF:
04BB 1A                 LDAX    D       ; READ GAP TILL 00 READ
04BC B7                 ORA     A
04BD C2B004             JNZ     L4A4
04C0 1A                 LDAX    D
04C1 B7                 ORA     A
04C2 C2B004             JNZ     L4A4
                L4B9:
04C5 36C7               MVI     M,0C7H  ; WRITE C7 SYNCH MARK
                L4BB:
04C7 3A0060             LDA     MRKCRC  ; READ DATA MARK
04CA B7                 ORA     A
04CB CAC704             JZ      L4BB    ; LOOP TILL NON-ZERO
04CE FEFE               CPI     0FEH    ; SEE IF CORRECT DATA MARK
04D0 CA8B03             JZ      L383    ; JUMP IF GOOD
04D3 36FF               MVI     M,0FFH
04D5 3A0063             LDA     SYNCPL
04D8 B7                 ORA     A
04D9 CAC504             JZ      L4B9
04DC C3A704             JMP     L49B
                L4D3:
04DF 3A1540             LDA     RWFLG   ; READ WRITE FLAG
04E2 B7                 ORA     A
04E3 C20405             JNZ     L4F8
04E6 1A                 LDAX    D
04E7 060A               MVI     B,0AH   ; WAS 7, READ IN THREE EXTRA TO IGNORE
                                        ; THANKS TO LARRY BOBERG.
                L4DD:
04E9 1A                 LDAX    D
04EA 05                 DCR     B
04EB C2E904             JNZ     L4DD
04EE 1A                 LDAX    D
04EF 210065             LXI     H,6500H
04F2 36FF               MVI     M,0FFH  ; WRCLK
04F4 3A0063             LDA     SYNCPL
04F7 36C7               MVI     M,0C7H
04F9 3A0060             LDA     MRKCRC
04FC FEFB               CPI     0FBH
04FE C29504             JNZ     L48E
0501 C3D703             JMP     L3CF
                L4F8:
0504 1A                 LDAX    D
0505 1A                 LDAX    D
0506 3EFF               MVI     A,0FFH
0508 12                 STAX    D
0509 12                 STAX    D
050A 12                 STAX    D
050B AF                 XRA     A
050C 12                 STAX    D
050D 12                 STAX    D
050E 12                 STAX    D
050F 12                 STAX    D
0510 010060             LXI     B,MRKCRC
0513 C31704             JMP     L411
                ;*****************************************************************
                ;
```

```
                ;       FORMAT A TRACK- THIS COMMAND WILL SEEK THE TRACK, READ IN
                ;       USER BUFFER, AND EITHER WRITE SEQUENTIAL OR RANDOM NUMBERED
                ;       SECTORS FILLED WITH USER DATA FILLER BYTE. FOR SEQUENTIAL
                ;       SECTORS ONLY THE FIRST BYTE OF USER BUFFER SPECIFIES WHAT
                ;       ALL SECTORS ON THE TRACK WILL HAVE THEIR DATA FIELDS FILLED
                ;       WITH. FORMAT WRITES ALL MARKS, GAPS, AND FIELDS ACCORDING
                ;       TO FM FORMAT OR MMFM FORMAT. MMFM/FM TYPE IS SIGNALLED BY
                ;       FLAG "DDSDFL" .
                ;
                FORMAT:
0516 CD7C02             CALL    SEEK    ; FORMAT COMMAND, DO SEEK
0519 B7                 ORA     A
051A C0                 RNZ             ; RETURN IF ERRORS
051B CDE602             CALL    WRENBL  ; CALL WRITE ENABLE
051E C8                 RZ              ; RETURN IF ERROR
051F 016880             LXI     B,8068H ; DMA CYCLE, TC BYTES
0522 2A0540             LHLD    BUFFER  ; READ FORMAT TABLE FROM HOST AT BUFFER
0525 CDF901             CALL    DMALOD  ; ARM DMA
0528 2643               MVI     H,43H   ; POINT TO PAGE IN 2114
052A 3A0040             LDA     CHANWD  ; FETCH CHANNEL WORD
052D E640               ANI     40H     ; RANDOM FORMAT?
052F C24105             JNZ     L535    ; JUMP IF RANDOM
0532 E5                 PUSH    H       ; ELSE DO SEQUENTIAL SECTORS
0533 7E                 MOV     A,M     ; FILL ALL SECTORS WITH THIS DATA
0534 010134             LXI     B,3401H ; LOOP COUNT =34H, SECTOR #  1
                L52B:
0537 71                 MOV     M,C     ; WRITE SECTOR NUMBER
0538 2C                 INR     L
0539 77                 MOV     M,A     ; WRITE DATA BYTE
053A 2C                 INR     L
053B 0C                 INR     C
053C 05                 DCR     B
053D C23705             JNZ     L52B
0540 E1                 POP     H
                ;
                ;       RANDOM FORMAT. AT THIS POINT THE TABLE OF SECTOR ORDER AND
                ;       FILLER BYTE IS COMPLETE.
                ;
                L535:
0541 011340             LXI     B,INDXCT        ; INDEX COUNT
0544 110062             LXI     D,DISKIO        ; POINTER FOR STAX D TO WRITE DISK
0547 3E01               MVI     A,1     ; INDEX 1 DISK REV.
0549 02                 STAX    B       ; STORE IN FLAG
054A 3A1240             LDA     DDSDFL  ; TEST DD OR SD FORMAT
054D B7                 ORA     A
054E CABB05             JZ      L5B1    ; JUMP IF SD
0551 0A         L545:   LDAX    B       ; FETCH INDEX COUNTER
0552 B7                 ORA     A
0553 C25105             JNZ     L545    ; LOOP TILL INDEX MARK
0556 AF                 XRA     A
0557 0E3F               MVI     C,3FH
                L54D:
                DDGAP1:
0559 12                 STAX    D       ; WRITE GAP 1, 64 ZERO'S
055A 0D                 DCR     C
055B C25905             JNZ     L54D
```

```
055E 12              STAX    D       ; ONE MORE
055F 0634            MVI     B,34H   ; DD SECTOR COUNT
                L555:
0561 DB66            IN      RDSTAT
0563 3EFF            MVI     A,0FFH
0565 0E09            MVI     C,9
                L55B:
0567 12              STAX    D       ; WRITE 0FFH TEN TIMES
0568 0D              DCR     C
0569 C26705          JNZ     L55B    ; LOOP
056C 12              STAX    D       ; ONE MORE
056D 3E0E            MVI     A,0EH   ; WRITE I.D. ADDRESS MARK FOR MMFM
056F 320061          STA     MARK    ; WRMRK
0572 3A0340          LDA     TRKADR  ; LOAD TRACK ADDR
0575 12              STAX    D       ; WRDISK
0576 AF              XRA     A       ; ACC=0
0577 12              STAX    D       ; WRDISK
0578 7E              MOV     A,M     ; FETCH SECTOR I.D.
0579 12              STAX    D       ; WRDISK
057A AF              XRA     A       ; ACC=0
057B 2C              INR     L
057C 12              STAX    D       ; WRDISK
057D 320063          STA     WRCRC   ; WRCRC
0580 320063          STA     WRCRC   ; WRCRC
0583 0E11            MVI     C,11H
              DDGAP2:
              L57A:
0585 12              STAX    D       ; WRITE 11 ZERO'S
0586 0D              DCR     C
0587 C28505          JNZ     L57A
058A 12              STAX    D       ; ONE MORE
058B 3EFF            MVI     A,0FFH  ; WRITE NINE 0FFH'S
058D 0E09            MVI     C,9
              L584:
058F 12              STAX    D       ; WRDISK
0590 0D              DCR     C
0591 C28F05          JNZ     L584
0594 12              STAX    D       ; ONE MORE
0595 3E0B            MVI     A,0BH   ; WRITE DATA MARK
0597 320061          STA     MARK    ; SEND TO DISK
059A 7E              MOV     A,M     ; LOAD DATA BYTE FOR FILL
059B 0E7F            MVI     C,7FH   ; ONE SECTOR COUNT-1
              L593:
059D 12              STAX    D       ; FILL DATA FIELD
059E 0D              DCR     C
059F C29D05          JNZ     L593
05A2 12              STAX    D       ; ONE MORE
05A3 AF              XRA     A
05A4 320063          STA     WRCRC   ; WRITE TWO DATA FIELD CRC BYTES
05A7 2C              INR     L
05A8 320063          STA     WRCRC   ; WRCRC
05AB 0E11            MVI     C,11H
              DDGAP3:
              L5A3:
05AD 12              STAX    D
05AE 0D              DCR     C
```

```
05AF C2AD05             JNZ     L5A3    ; WRITE 17 ZERO'S
05B2 12                 STAX    D       ; ONE MORE
05B3 05                 DCR     B
05B4 C26105             JNZ     L555    ; DO NEXT RECORD
05B7 12                 STAX    D       ; WRITE A ZERO
05B8 C31E06             JMP     L616    ; DO GAP 4 AND RETURN
                ;
                ;       WAIT FOR INDEX MARK
                ;
                L5B1:
05BB 0A                 LDAX    B       ; TEST INDEX FLAG
05BC B7                 ORA     A
05BD C2BB05             JNZ     L5B1    ; LOOP TILL INDEX
05C0 3EFF               MVI     A,0FFH
05C2 0E48               MVI     C,48H
                ;
                ;       SINGLE DENSITY FORMAT RECORD
                ;
                L5BA:
                SDGAP1:
05C4 12                 STAX    D       ; WRITE 48H 0FFH'S
05C5 0D                 DCR     C
05C6 C2C405             JNZ     L5BA
05C9 12                 STAX    D       ; ONE MORE
05CA 061A               MVI     B,26    ; 26 SECTORS LOOP COUNT
                L5C2:
05CC AF                 XRA     A
05CD 12                 STAX    D       ; WRITE 6 ZERO'S
05CE 12                 STAX    D
05CF 12                 STAX    D
05D0 12                 STAX    D
05D1 12                 STAX    D
05D2 12                 STAX    D
05D3 3EFE               MVI     A,0FEH  ; WRITE I.D. RECORD MARK
05D5 320060             STA     MRKCRC
05D8 3A0340             LDA     TRKADR  ; FETCH TRACK ADDRESS
05DB 12                 STAX    D       ; WRITE TRACK I.D.
05DC AF                 XRA     A
05DD 12                 STAX    D       ; WRITE SIDE 0 I.D.
05DE 7E                 MOV     A,M     ; FETCH SECTOR ADDRESS
05DF 12                 STAX    D       ; WRITE SECTOR I.D.
05E0 AF                 XRA     A
05E1 2C                 INR     L
05E2 12                 STAX    D       ; WRITE SECTOR LENGHT CODE=0
05E3 3EFF               MVI     A,0FFH
05E5 320063             STA     WRCRC   ; WRITE TWO CRC BYTES
05E8 320063             STA     WRCRC   ; WRCRC
                ;
                ;       WRITE SD GAP 2
                ;
05EB 0E0A               MVI     C,0AH
                L5E4:
05ED 12                 STAX    D       ; WRITE FF
05EE 0D                 DCR     C
05EF C2ED05             JNZ     L5E4
05F2 12                 STAX    D       ; ONE MORE FF
```

```
05F3 AF                 XRA     A
05F4 12                 STAX    D       ; WRITE ZERO'S
05F5 12                 STAX    D
05F6 12                 STAX    D
05F7 12                 STAX    D
05F8 12                 STAX    D
05F9 12                 STAX    D
                ;
                ;       WRITE DATA FIELD
                ;
05FA 3EFB               MVI     A,0FBH  ; WRITE DATA ADDRESS MARK
05FC 320060             STA     MRKCRC  ; WRMRKCRC
05FF 7E                 MOV     A,M     ; FETCH FILLER DATA
0600 0E7F               MVI     C,7FH
                L5FA:
0602 12                 STAX    D       ; FILL ANOTHER 127 BYTES WITH SAME DATA
0603 0D                 DCR     C
0604 C20206             JNZ     L5FA
0607 12                 STAX    D
0608 3EFF               MVI     A,0FFH  ; WRITE TWO CRC BYTES
060A 320063             STA     WRCRC
060D 2C                 INR     L
060E 320063             STA     WRCRC
0611 0E1A               MVI     C,1AH   ; WRITE GAP 3
                L60B:
                SDGAP3:
0613 12                 STAX    D       ; FILL WITH FF
0614 0D                 DCR     C
0615 C21306             JNZ     L60B
0618 12                 STAX    D       ; ONE MORE FF
0619 05                 DCR     B
061A C2CC05             JNZ     L5C2
061D 12                 STAX    D
                GAP4:
                L616:
061E EB                 XCHG
061F 111340             LXI     D,INDXCT        ; INDEX COUNT
0622 47                 MOV     B,A
                L61B:                   ; WRITE GAP 4 TILL INDEX MARK
0623 70                 MOV     M,B
0624 1A                 LDAX    D       ; FETCH INDEX COUNT
0625 B7                 ORA     A
0626 F22306             JP      L61B
0629 AF                 XRA     A
062A C9                 RET             ; RETURN TO MAINLINE

                ;*******************************************************************************
                ;
                ;       RAM BUFFER
                ;
4000                    ORG     4000H
                IOPB:
4000            CHANWD: DS      1       ; IOPB CHANNEL WORD
4001            DKINST: DS      1       ; DISK INSTRUCTION
4002            NUMRCD: DS      1       ; NUMBER OF RECORDS
4003            TRKADR: DS      1       ; TRACK ADDRESS
```

```
4004            SCTADR: DS      1       ; SECTOR ADDRESS
4005            BUFFER: DS      2       ; BUFFER ADDRESS
4007            BLOCKN: DS      1       ; BLOCK NUMBER, SD LINKED ONLY
4008            NXIOPB: DS      2       ; NEXT IOPB ADDRESS, LINKED
400A            UNITSL: DS      1       ; ADDR=400AH
400D                    ORG     400DH

400D            UNIT:   DS      1
400E            TRKRGO: DS      4       ; UNIT TRACK REGISTER ARRAY
4012            DDSDFL: DS      1       ; SINGLE/DOUBLE DENSITY FLAG
4013            INDXCT: DS      1       ; INDEX COUNTER
4014            RDYBIT: DS      1       ; READY BIT STATUS FROM FDD
4015            RWFLG:  DS      1       ; READ/WRITE FLAG
4016            DAMARK: DS      1       ; DATA ADDRESS MARK
4017            FLAGB:  DS      1
4018            FLAGC:  DS      1
4019            FLAGD:  DS      1


401A                    END     ZX202
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```
4007 BLOCKN     4005 BUFFER     4000 CHANWD     0080 CLRINT     01CB CTAB
4016 DAMARK     0559 DDGAP1     0585 DDGAP2     05AD DDGAP3     4012 DDSDFL
02BF DELAY      6200 DISKIO     4001 DKINST     2000 DMADDR     01F9 DMALOD
2008 DMAMOD     2001 DMATC      0015 DSKCLR     4017 FLAGB      4018 FLAGC
4019 FLAGD      0516 FORMAT     061E GAP4       0020 INDEX      4013 INDXCT
4000 IOPB       00D9 LODA       0107 L108       011D L11E       0121 L122
0139 L13A       0152 L153       0161 L162       0184 L185       01E3 L1D7
01F0 L1E6       020D L20C       0224 L223       0234 L233       0237 L236
023B L23A       0241 L240       0247 L246       024A L249       0253 L252
0257 L256       025C L25B       025E L25D       0263 L262       0268 L267
026A L269       026C L26B       02AC L2AB       02C1 L2B9       02D8 L2D0
0308 L300       0322 L31A       033C L334       0352 L34A       035F L357
0363 L35B       036A L362       0377 L36F       038B L383       03B9 L3B1
03C4 L3BC       03C5 L3BD       003C L3C        03D7 L3CF       03E0 L3D9
0401 L3FB       0404 L3FE       040F L409       0417 L411       0426 L421
043B L432       0466 L45F       046E L467       0474 L46D       0488 L481
0490 L489       0495 L48E       0499 L492       04A7 L49B       04A9 L49D
004A L4A        0497 L4A2       04B0 L4A4       04BB L4AF       04C5 L4B9
04C7 L4BB       04DF L4D3       04E9 L4DD       0504 L4F8       0537 L52B
0541 L535       0054 L54        0551 L545       0559 L54D       0561 L555
0567 L55B       0585 L57A       058F L584       059D L593       05AD L5A3
05BB L5B1       05C4 L5BA       05CC L5C2       05ED L5E4       0602 L5FA
0613 L60B       061E L616       0623 L61B       006A L6A        0096 L95
009C L9B        00C0 LC0        00C1 LC1        0028 MA78       0034 MA88
6100 MARK       6000 MRKCRC     4002 NUMRCD     4008 NXIOPB     6402 PORT79
6403 PORT7B     6400 PORT89     6401 PORT8B     0009 RAMCLR     6500 RDPRT1
0067 RDRDY      0066 RDSTAT     4014 RDYBIT     0074 RDYINT     02F7 READ
02D5 RECAL      4015 RWFLG      0296 S1         0299 S2         4004 SCTADR
05C4 SDGAP1     0613 SDGAP3     027C SEEK       02A2 STEP       003C STOP
6300 SYNCPL     02BD TENMS      4003 TRKADR     02CA TRKREG     400E TRKRG0
400D UNIT       01DB UNITAB     400A UNITSL     6500 WRCLK      0067 WRCNT1
0066 WRCONT     6300 WRCRC      02E6 WRENBL     02FB WRITDL     0302 WRITE
0000 ZX202
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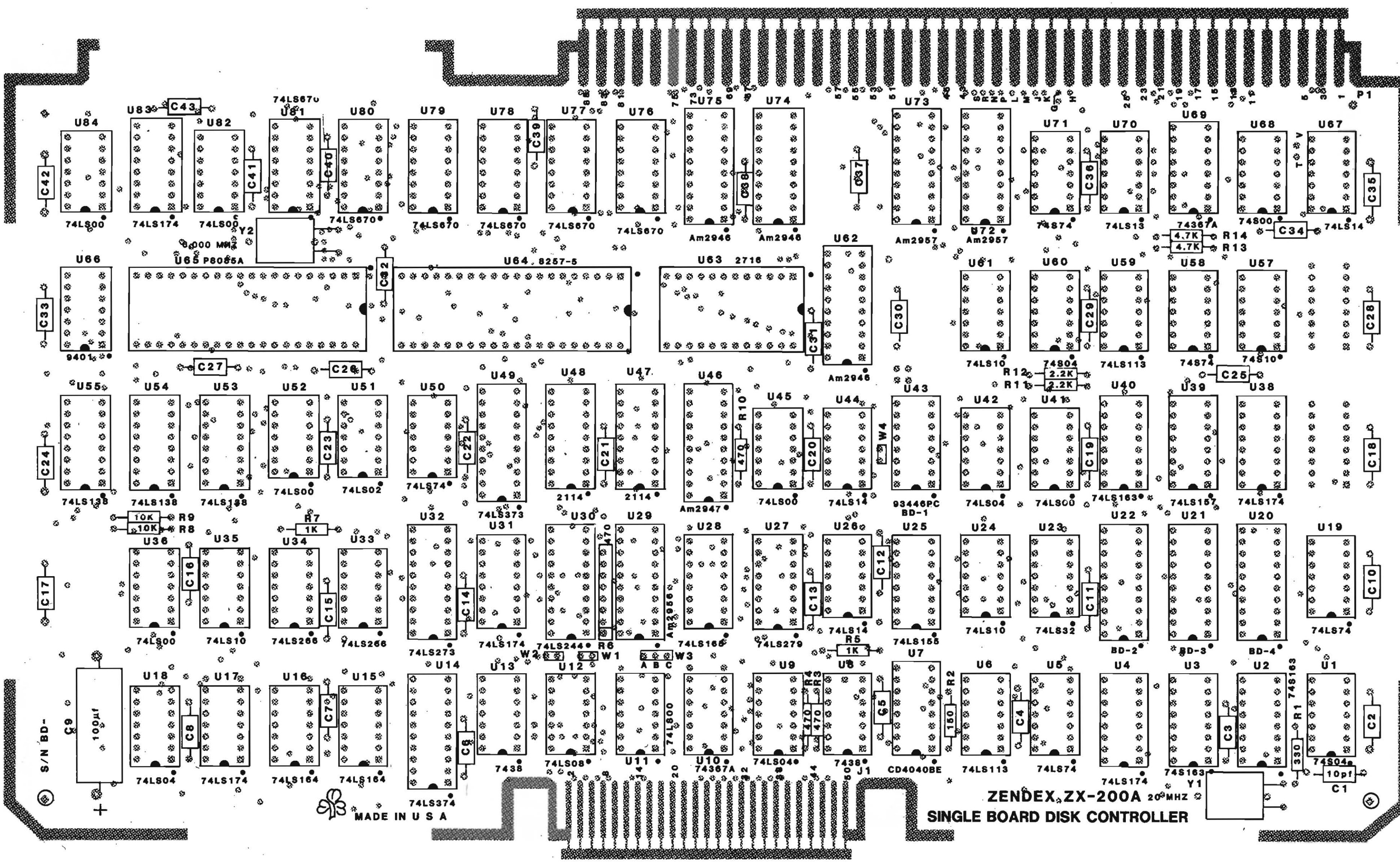
Bill of Materials

Item #	Qty.	Part#	Description
R8, 9	2	10KOHM	Resistor
R2	1	150OHM	Resistor
R5, 7	2	1KOHM	Resistor
R11, 12	2	2.2 KOHM	Resistor
U47, 48	2	2114-3	I. C.
U63	1	2716-ZX200	I.C. EPROM Version 1.1 for ZX-200
R1	1	330OHM	Resistor
R113, 14	2	4308R-101-471	Bourns 8P SIP
R3, 4, 10	3	470OHM	Resistor
XU43	1	516-AG11D	Dip Socket
XU20-22	3	520-AG11D	Dip Socket
XU63	1	524-AG11D	Dip Socket
W3	1	530153-1	Jumper
XU64, 65	2	540-AG11D	Dip Socket
U11, 36, 41, 45, 52, 82, 84	7	74LS00	I.C., LS TTL
U51	1	74LS02	I.C., LS TTL
U9, 18, 42	3	74LS04	I.C., LS TTL
U12	1	74LS08	I.C., LS TTL
U24, 35, 61	3	74LS0	I.C., LS TTL
U6, 59	2	74LS113	I.C., LS TTL
U70	1	74LS13	I.C., LS TTL
U53, 54, 55	3	74LS14	I.C., LS TTL
U25	1	74LS155	I.C., LS TTL
U39	1	74LS157	I.C., LS TTL
U40	1	74LS163	I.C., LS TTL
U15, 16	2	74LS165	I.C., LS TTL
U4, 17, 31, 38, 83	5	74LS174	I.C., LS TTL
U30	1	74LS244	I.C., LS TTL
U33, 34	2	74LS266	I.C., LS TTL
U32	1	74LS273	I.C., LS TTL
U27	1	74LS279	I.C., LS TTL
U23	1	74LS32	I.C., LS TTL
U10, 69	2	74LS367	I.C., LS TTL
U49	1	74LS373	I.C., LS TTL
U14	1	74LS374	I.C., LS TTL
U8, 13	2	74LS38	I.C., LS TTL
U76-81	6	74LS670	I.C., LS TTL
U5, 19, 50	3	74LS74	I.C., LS TTL
U68	1	74S00	I.C. TTL SCHOTTKY
U1, 60	2	74S04	I.C.
U57	1	74S10	I.C. TTL SCHOTTKY
U2, 3	2	74S163	I.C. TTL SCHOTTKY
U20, 21	2	74S471	TI TBP18S22 Bipolar PROM
U58, 71	2	74S74	I.C.

Bill of Materials (continued)

Item #	Qty	Part #	Description
U65	1	8085A-2	I.C., 8-Bit CPU
U64	1	8257-5	DMA CHIP
XW3	3	B7022-A	AMP Wire Wrap Post
U43	1	93446PC	I.C., BIPOLAR PROM
U66	1	9401	IC CRC Generator & Checker
U46, 62, 74, 75	4	AM2946	I.C.
U29	1	AM2956	I.C.
U72, 73	2	AM2957	I.C.
C1	1	C4OC100K	Centralab Cap
C2-8, & 10-12	41	C41C104K	Centralab Cap
U7	1	CD4040BE	I.C. CMOS
Y1	1	CY22A	Crystek 20 MHz Crystal
Y2	1	CY6C	Xtal 6.144 MHz
C9	1	TE-1211	Sprague Cap
--	1	PCZX-200A	PC Board, ZX-200A



ZENDEX ZX-200A
20 MHZ
SINGLE BOARD DISK CONTROLLER
MADE IN U S A
S/N BD-
P1
J1
U84 74LS00
U83 74LS174
C43
U82 74LS00
C41
U81 74LS670
C40
U80 74LS670
U79 74LS670
U78 74LS670
C39
U77 74LS670
U76 74LS670
U75 Am2946
C38
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C37
U73 Am2957
U72 Am2957
U71 74S74
C36
U70 74LS13
U69 74367A
U68 74S00
C34
U67 74LS14
C35
C42
Y2
8.000 MHZ
R14 4.7K
R13 4.7K
U66 9401
C33
U65 P8085A
C32
U64 8257-5
U63 2716
C31
U62 Am2946
C30
U61 74LS10
U60 74S04
C29
U59 74LS113
U58 74S74
U57 74S10
C28
C27
C26
R12 2.2K
R11 2.2K
C25
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U50 74LS74
C22
U49 74LS373
U48 2114
C21
U47 2114
U46 Am2947
R10 470
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U42 74LS04
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C24
R9 10K
R8 10K
R7 1K
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C15
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U32 74LS273
C14
U31 74LS174
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470
U29 Am2956
U28 74LS166
U27 74LS279
C13
U26 74LS14
C12
U25 74LS155
U24 74LS10
U23 74LS32
C11
U22 BD-2
U21 BD-3
U20 BD-4
U19 74LS74
C10
C17
W2
R6
W1
W3
A B C
R5 1K
C9 100µf
U18 74LS04
C8
U17 74LS174
U16 74LS164
C7
U15 74LS164
U14 74LS374
C6
U13 7438
U12 74LS08
U11 74LS00
U10 74367A
U9 74LS04
R4 470
R3 470
U8 7438
C5
U7 CD4040BE
R2 150
U6 74LS113
C4
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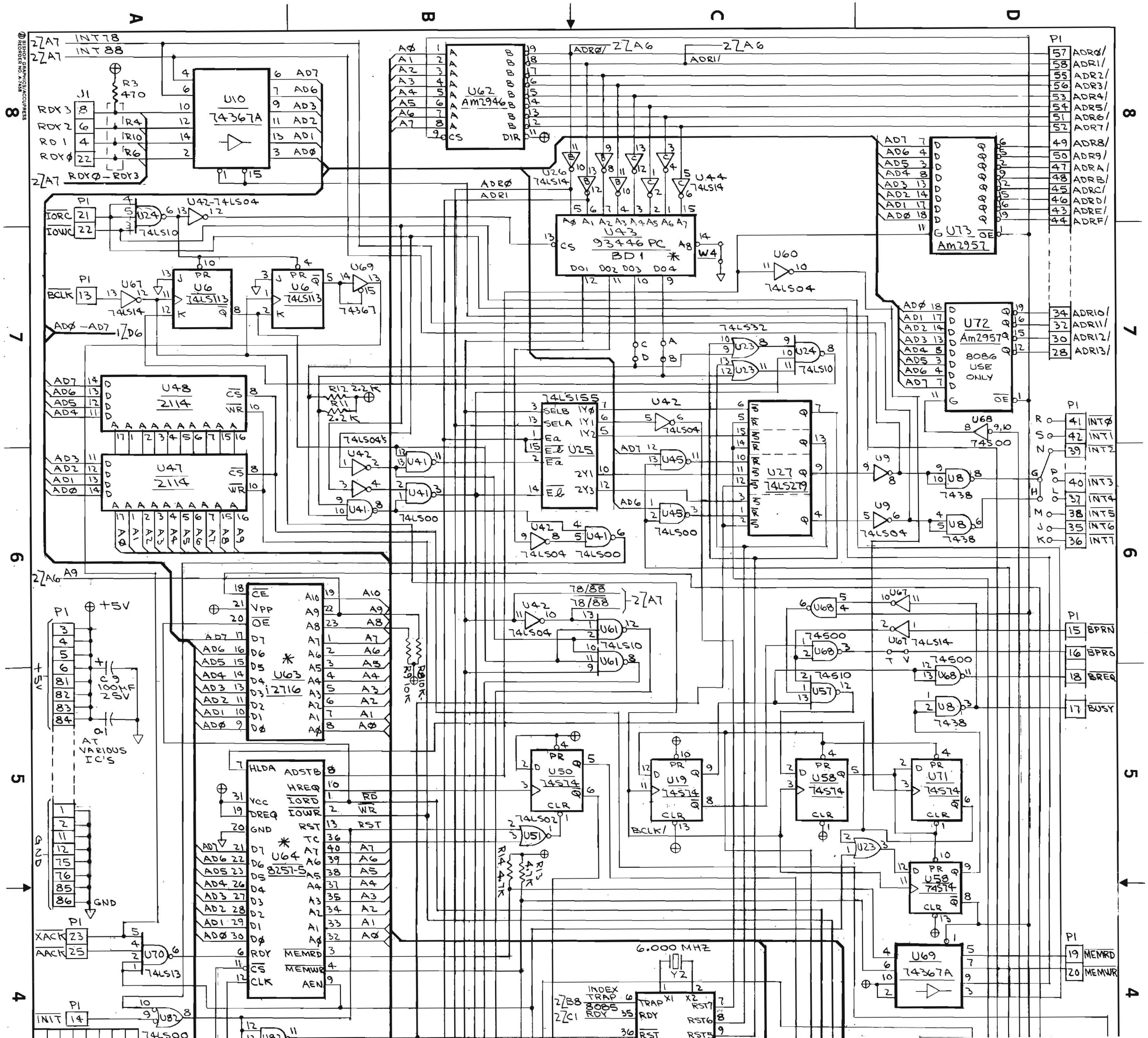
C1



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B
C
D
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U70
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U82
74LS00
U69
74367A
Y2
6.000 MHZ
8085
J1
R3 470
R12 2.2K
R11 2.2K
R9 10K
R10 10K
R14 4.7K
R13 4.7K
C9 100MF 25V
0.1 AT VARIOUS IC'S
+5V
GND
P1
INT78
INT88
RDY3
RDY2
RD1
RDYØ
RDYØ-RDY3
IORC
IOWC
BCLK
ADØ-AD7
ADRØ/
ADR1/
ADR2/
ADR3/
ADR4/
ADR5/
ADR6/
ADR7/
ADR8/
ADR9/
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ADRD/
ADRE/
ADRF/
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ADR12/
ADR13/
INTØ
INT1
INT2
INT3
INT4
INT5
INT6
INT7
BPRN
BPRO
BREQ
BUSY
MEMRD
MEMWR
XACK
AACK
INIT
HLDA
HREQ
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CLK
RDY
CS
INDEX TRAP
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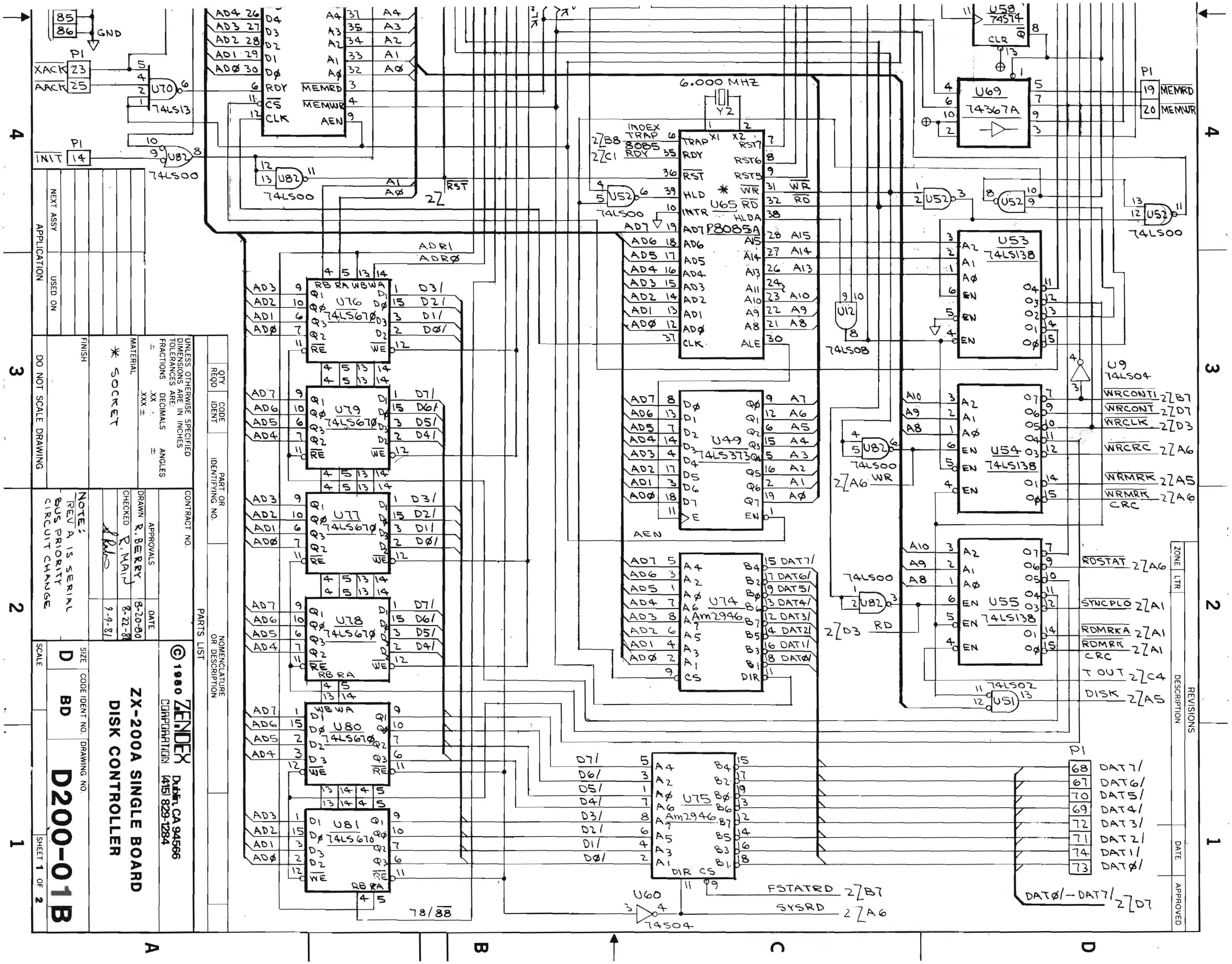
RST5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DISK CONTROLLER
© 1980 ZENDEX CORPORATION
Dublin, CA 94566
(415) 829-1284
D200-01B
SIZE D
CODE IDENT NO.
DRAWING NO.
SCALE
SHEET 1 OF 2
BD
DRAWN R. BERRY 8-20-80
CHECKED R. MAIJ 8-22-80
9-9-81
APPROVALS
DATE
CONTRACT NO.
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ±
DECIMALS .XX ± .XXX ±
ANGLES ±
MATERIAL
FINISH
* SOCKET
DO NOT SCALE DRAWING
NEXT ASSY
USED ON
APPLICATION
QTY REQD
CODE IDENT
PART OR IDENTIFYING NO.
NOMENCLATURE OR DESCRIPTION
PARTS LIST
NOTE: REV A IS SERIAL BUS PRIORITY CIRCUIT CHANGE
REVISIONS
ZONE
LTR
DESCRIPTION
DATE
APPROVED
U65 P8085A
6.000 MHZ
Y2
U49 74LS373
U74 Am2946
U75 Am2946
U76 74LS670
U77 74LS670
U78 74LS670
U79 74LS670
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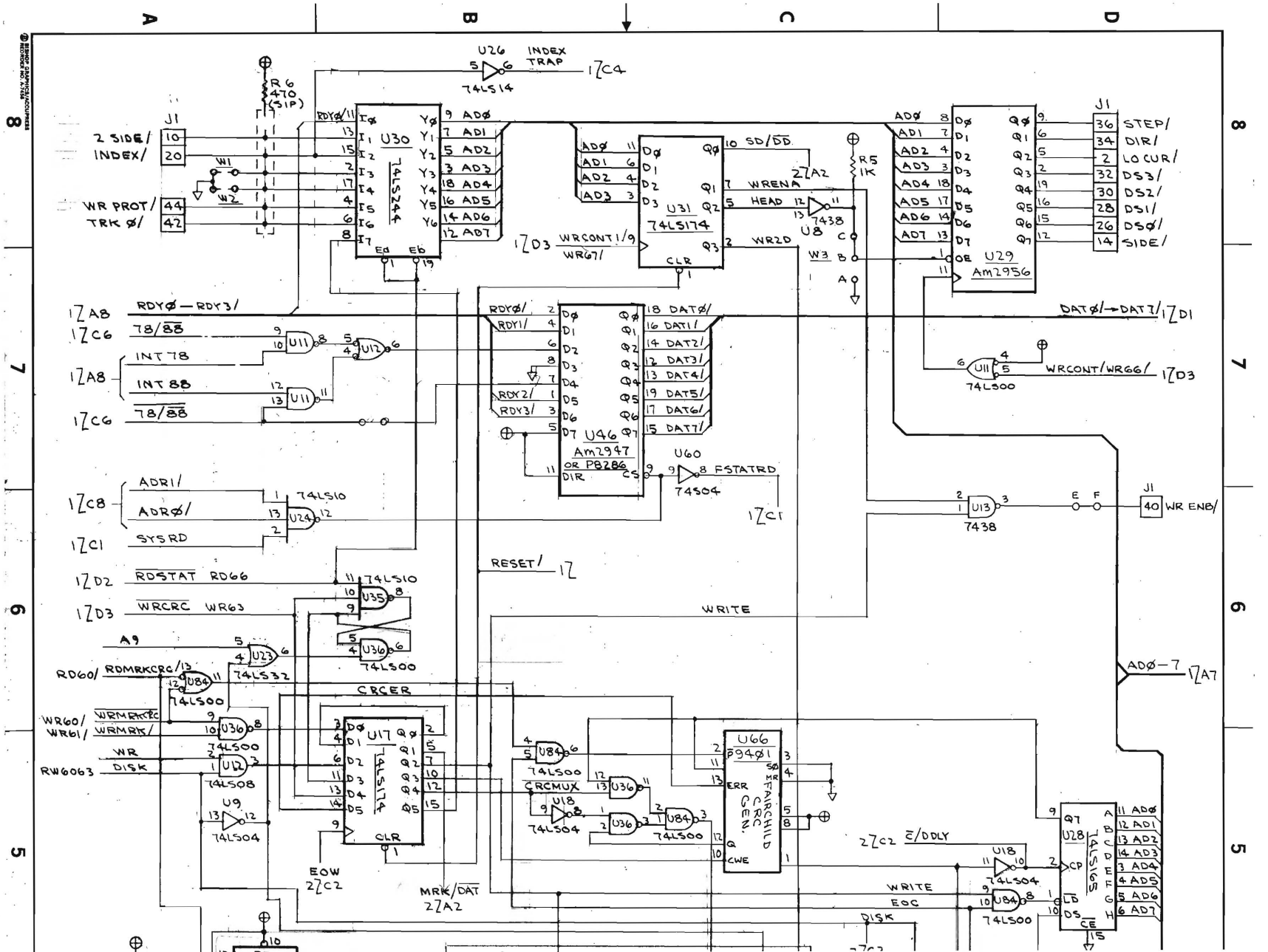
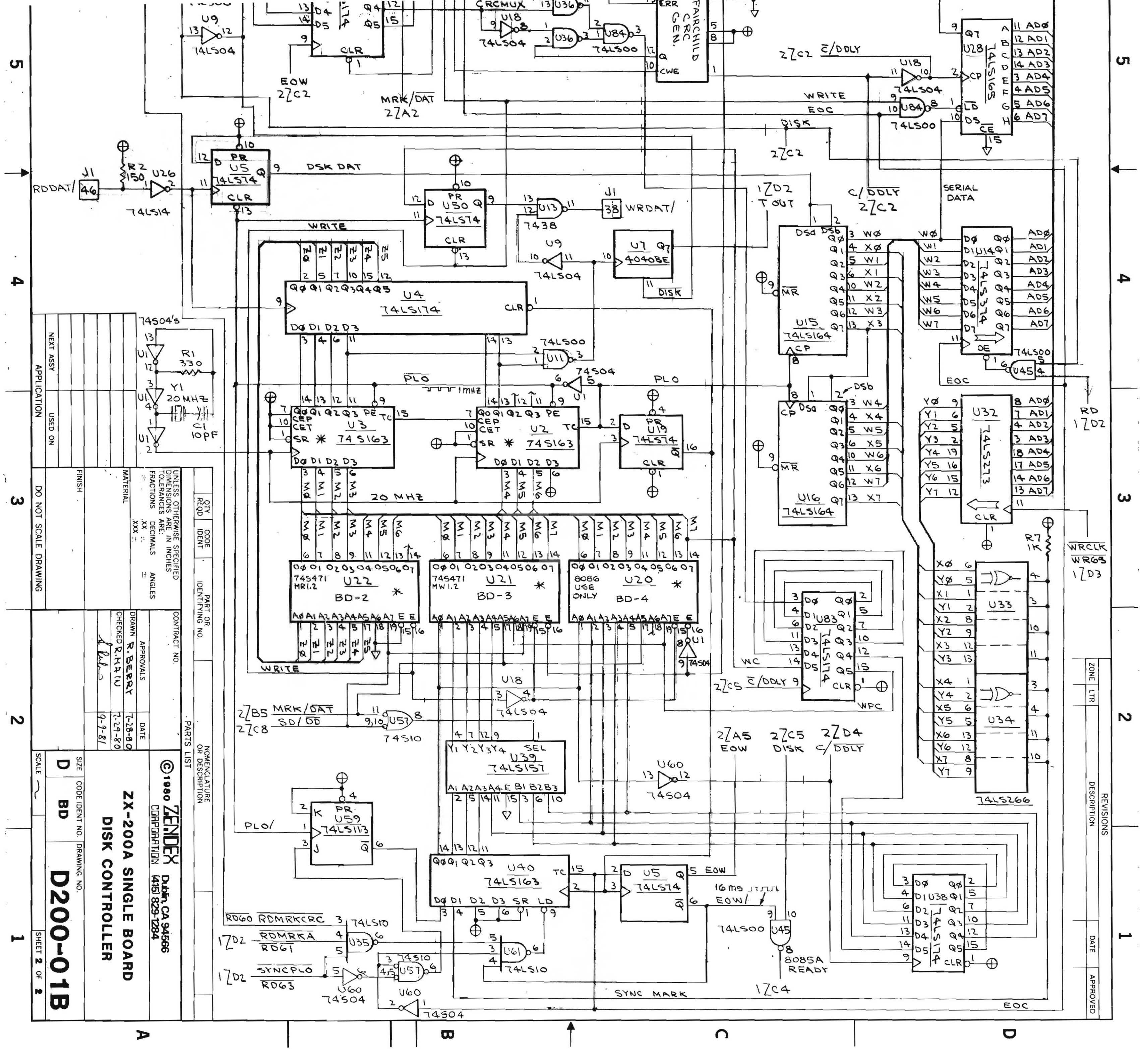
U53 74LS138
U54 74LS138
U55 74LS138
U69 74367A
U58 74S74
U70 74LS13
U82 74LS00
U52 74LS00
U12 74LS08
U9 74LS04
U51 74LS02
U60 74S04
MEMRD
MEMWR
XACK
AACK
INIT
GND
WRCONTI
WRCONT
WRCLK
WRCRC
WRMRK
RDSTAT
SYNCPLO
RDMRKA
T OUT
DISK
FSTATRD
SYSRD
DAT∅/-DAT7/
78/88


U26 INDEX TRAP
74LS14
1ZC4
R6 470 (SIP)
J1
2 SIDE/
INDEX/
WR PROT/
TRK Ø/
W1
W2
U30
74LS244
ADØ
AD1
AD2
AD3
AD4
AD5
AD6
AD7
U31
74LS174
SD/DD
WRENA
HEAD
WR2D
WRCONT1/9
WRG7/
1ZD3
1ZA2
R5 1K
7438
U8
W3
U29
Am2956
STEP/
DIR/
LO CUR/
DS3/
DS2/
DS1/
DSØ/
SIDE/
RDYØ—RDY3/
DATØ/→DAT7/
1ZD1
1ZA8
1ZC6
78/88
INT78
INT88
U11
U12
74LS00
WRCONT/WRG6/
U46
Am2947
OR P8286
DAT0/
DAT1/
DAT2/
DAT3/
DAT4/
DAT5/
DAT6/
DAT7/
RDY0/
RDY1/
RDY2/
RDY3/
U60
74S04
FSTATRD
1ZC1
1ZC8
ADR1/
ADRØ/
SYSRD
74LS10
U24
U13
7438
WR ENB/
RESET/ 1Z
RDSTAT RD66
WRCRC WR63
U35
U36
WRITE
A9
RD60/
RDMRKCRC/13
U23
U84
74LS32
74LS00
CRCER
ADØ—7
1ZA7
WR60/
WR61/
WRMRKCRC
WRMRK/
WR
DISK
RW6063
U12
74LS08
U9
74LS04
U17
74LS174
EOW
2ZC2
MRK/DAT
2ZA2
CRCMUX
U18
U66
P8481
FAIRCHILD
CRC GEN.
ERR
CWE
2ZC2 E/DDLY
U28
74LS165
WRITE
EOC
DISK
11 ADØ
12 AD1
13 AD2
14 AD3
3 AD4
4 AD5
5 AD6
6 AD7



ZX-200A SINGLE BOARD
DISK CONTROLLER
© 1980 ZENDEX CORPORATION
Dublin, CA 94566
(415) 829-1284
D
BD
D200-01B
SHEET 2 OF 2
DRAWN R. BERRY 7-28-80
CHECKED R. MAIU 7-29-80
9-9-81
DO NOT SCALE DRAWING
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
PARTS LIST
NEXT ASSY
USED ON
APPLICATION
REVISIONS
FAIRCHILD CRC GEN.
U5 74LS74
U50 74LS74
U4 74LS174
U3 74S163
U2 74S163
U19 74LS74
U22 74S471 BD-2
U21 74S471 BD-3
U20 8086 USE ONLY BD-4
U39 74LS157
U40 74LS163
U59 74LS113
U28 74LS165
U15 74LS164
U16 74LS164
U14 74LS374
U32 74LS273
U83 74LS174
U38 74LS174
U33
U34
74LS266
U7 4040BE
Y1 20 MHZ
R1 330
R2 150
R7 1K
C1 10pF
RDDAT/
DSK DAT
WRDAT/
WRITE
PLO
20 MHZ
SERIAL DATA
EOC
EOW
DISK
C/DDLY
MRK/DAT
SD/DD
SYNC MARK
8085A READY
16 ms EOW/
RDG0 RDMRKCRC
RDMRKA RDG1
SYNCPLO RDG3
WRCLK
WRG5