HBR-ECC

TRAINING MANUAL

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Section I

INTRODUCTION

1.1 General

The inclusion of Error Correction into the HBR 3000 is a result of two factors. The need for error performance which exceeds the error rate of the data gathering and processing system in order to make the recorder transparent to the user and/or the wish to use otherwise marginal quality tape for digital recording applications.

1.2 History

The need for Error Correction was recognized several years ago by both the users and manufacturers of HDDR equipment. The question became more one of how much was needed and what system would yield the necessary performance with the minimum overhead. We originally proposed a relatively complicated system which would have necessated major system changes but would have provided very high performance with almost any size of error. After a lot of work and some success it was suggested that we try a much simpler system which as it turns out was easier to implement, maintains compatability with the existing format, and provides sufficient correction for most applications.

As time progressed we also were able to better define the error patterns that occur from tape and some of their typical characteristics. Also, parallel efforts in other parts of the system were able to define the source of errors not due solely to tape and many of these areas were corrected.

1.3 Description

The ECC method we have chosen involves two processes. First, we insert information into each channel of parallel data which allows us to detect, with very high reliability, if errors exist in each 480 bit block of data between sync words. A perpendicular parity is also generated and recorded on a separate track, which allows us to correct the bits in error. The limitation of this system is that if two channels have simultaneous data blocks with one or more errors we cannot correct either of them. This has not proven to be a problem as our calculations and tests have shown that simultaneous errors on two tracks are primarily due to improper handling and care of the tape.

Depending on the uncorrected error rate we are consistently achieving 2 to 4 orders of magnitude of error reduction. It is not unusual to go through an entire roll of tape (90,000 megabits of data) with no errors.

In addition to the effectiveness of the correction, we have also maintained compatability with the "standard" HBR 3000 tape format. ECC tapes can be reproduced on existing

systems and tapes made on non-ECC systems can be reproduced on ECC systems without any modification to either the HBR system or the interface to the customer. Upgrading of an existing system to an ECC system is not quite as simple as it requires new digital process bay(s), 13 new PWA's per DPB, and a new Mode Select Panel.

Section II

HBR 3000

2.1 General

The basic HBR system concept and layout has not been changed. The introduction of ECC affects only the Digital Process Bay (DPB) and Mode Select Panel (MSP). See Section III for a discussion of these changes. Improvements in other areas of the system have also been made which, although they do not relate directly to ECC, have improved the raw error rate substantially. ECC of course benefits from this as the Error Correction improves approximately geometrically with improvements in raw error rate. All of the improvements are included or available in the ECC system. In addition most of the improvements can be installed on existing systems to improve their performance.

2.2 Record Electronics

The record system has been improved to minimize the recorded skew and jitter due to the electronics and to minimize the Bias-Data intermodulation products.

2.2.1 Clocked Encoder PWA

PWA 1259673
Sch 1259670

The outputs of the Encoder PWA are now simultaneously clocked so that the residual jitter and timing difference between Encoder chips is eliminated.

2.2.2 13 MHz Bias System

The Bias/Head Driver system used for the 4 MHz at 240 ips system has been incorporated into the ECC system. This minimizes the intermodulation products generated by Bias-Data interaction while retaining the advantages of Bias recording in setup and equalization.

2.2.3 Non Bias Recording.

Due to physical limitations in the Airborne products it is necessary to use non-Bias recording when operating at the higher bit rates (above 4 Mbits per second). While this may require some readjustment for large speed changes, this is not felt to be a limitation as the vast majority of airborne users operate at fixed rates and do not require the

flexability of a laboratory system. The system is designed to be compatable with the same reproduce amplifiers used in the bias recorded systems.

2.2.3.1 Line Driver/Filter PWA

PWA 1261763
Sch 1261760

Several versions of the Filter PWA have been created over the past years in attempts to interface with different Head Drivers. The latest version incorporates line drivers which can be jumpered for Bias or Non-Bias recording and if properly terminated will match the cable and Head Driver input requirements of most systems.

The new Filter PWA also incorporates up to 4 auxillary channels (data, either analog or digital, which is not synchronous to the parallel clock) which can be assigned by means of jumpers to channels 1, 10 to 13, 14, and 23 to 26 (corresponding to tracks 1, 12 to 15, and 25 to 28) in the system. Please remember that ECC systems require a Parity channel which is either Channel 12 or 13 and 25 or 26, be sure you don't remove the Parity channel when selecting Aux. channels.

2.3 Reproduce System

A variety of reproduce options are now available for various data rates and customer requirements.

2.3.1 Bay Assembly

The Bay assembly used for Reproduce and Bit Sync Bays is no longer identical. To improve noise rejection and system interface several changes have been necessary which resulted in making the bays different.

2.3.2 Reproduce Amplifier

Three Reproduce amplifier versions have been used in standard HBR systems. They are physically interchangeable in bays with a Speed Encoder PWA pn 1255930-04. The 6 and 7 speed electronics do not need a Low Speed Secect PWA installed. The Two Speed (pn 1256153) version is being phased out in favor of the 6 speed (pn 1257253) version as the standard. Both of these PWA's are well covered in the standard HBR Manual (pn 1262016).

2.3.2.1 7 Speed

PWA 1257473
Sch 1257470

This PWA is necessary for the higher density systems. It uses active equalization techniques for the band edge equalization and has separate phase adjustments for 120ips.

2.3.3 Bit Sync-Decoder

Two Bit-Sync Decoder boards are available. They are physically interchangeable.

2.3.3.1 4 Mbit

There are several (?) versions of this around with various part numbers and different designs. Most of the variations are in the input limiter stage and DC restoration circuitry. The standard HBR manual description is fairly complete and up to date.

2.3.3.2 5 Mbit

PWA 1261253
Sch 1261250

This PWA was designed to increase the data rate capability of the 4 Mbit version. It accomplishes this by the use of faster chips, a D/A converter chip in place of the discrete version, and a slightly revised clocking scheme. In addition, the selection of BiPhase/Miller code, BiPhase polarity, and DC Restorer On/Off are by means of switches on the front edge of the PWA instead of jumpers.

2.3.4 Serial Clock Delay

PWA 1259623
Sch 1259620

To provide a delay in the serial clock which matches the parallel clock delay in the reproduce signal processing it is necessary to have this board. At a given serial rate the P/S converter can be jumpered to operate properly, but as the rate changes the phase difference of the parallel and serial clocks will change and the P/S converter will not function properly. If the serial clock is delayed the correct amount this problem is eliminated.

Section III

SYSTEM INTERCONNECT

3.1 General

The following pages show the interconnections required in the HBR 3000 ECC systems. The 14 channel system as shown in Figure 3.1, is virtually identical to the non-ECC system. The 28 channel systemas shown in Figure 3.2, is also virtually identical, but if the one- channel parity option is to be used a pair of new interconnect cables, from J48 and J49 in one DPB to J49 and J48 respectively in the other DPB, is required in order to interconnect the A and B bay Error Corrector cards.

3.2 PWA location

Generally the locations of the PWA's is the same as the standard system. As shown in Figure 3.3 . One new PWA (The CRC Generator) is added next to the Sync Inserter, Slave Deskews 7/8, 9/10, 11/12 have been moved one slot to the left to make room for two new cards (the Flag Detector/Delay and the Error Corrector). The Serial Clock Delay PWA has been moved between the Error Corrector and P/S Converter to locate it more logically in the signal path. The last PWA location has been reserved for future requirements.

3.3 Connector designations

3.3.1 Internal

In order to simplify the bay for construction and troubleshooting the J numbers of the PWA mating connectors have been revised. They are now J1 to J21 from left to right as you face the front of the bay, The last slot in the bay is J51. Headers which are used for either system interconnect or customer interface have retained the SAME number so there should be no confusion in cabling a system. Headers have been added for ECC interconnect (J48, J49), Monitor functions (J47), and Speed lines (J50) (for future HBR-ES systems).

3.3.2 Customer interface.

The rear panel of the DPB has been significantly revised. See Figure 3.4 . The I/O functions are now clearly labeled (no more J numbers) and some optional connector

locations have been added, most noteably the Monitor and Spare connectors. The functions have also been grouped in a more logical manner. The DPB assembly is now the same for HBR 3000 and AHBR with only wirewrap differences on the motherboard.

3.4 Mode Select Panel

The Mode Select Panel has been changed to include an ECC ON/OFF switch and an uncorrected error indicator as shown in Figure 3.5 . Certain functions have also been removed (512/256 and SSW/NSSW select) and the location of functions has been revised to improve the functional layout. The functions removed were considered to be unnecessary on the front panel. They are still available by jumper selection on PWB's in the DPB.

Section IV

ERROR CORRECTION SYSTEM

4.1 General

The Error Correction System we have chosen is called an orthogonal or rectangular scheme. This means that we use two error detection systems which are at right angles to each other over a defined field of data. For a multi-track tape recorder this is fairly obvious as we have an error detection method used on each track along the tape and another system checking the data across the tape. At the point where these two checks intersect a single bit can be corrected, which is what we do.

4.1.1 Longitudinal Detection

The longitudinal system we use is implimented by a system called a Cyclical Redundancy Check (CRC). A block of data is manipulated by a shift register with feedback which performs a binary combination of the data with a known formula. This results in a Check Word which is not unique to the data but would be very difficult to duplicate with a data pattern which has errors in it. This system tells us if errors have occurred in any one track during the period between the Check Words.

4.1.2 Orthoginal Detection

To detect errors across the tape we use a simple Parity check which requires only that we add a single bit to tell us whether there was an odd or even number of ones or zeroes in the data when it was recorded. This has the limitation of not being able to determine more than one error, but that is a minor limitation on a tape recorder with the track widths we use.

4.2 System

The following page, Figure 4.1 shows the signal flow in the Digital Process Bay with the changes required for ECC in the dashed outlines. The following sections of this manual deal with these changes in more detail. Figure 4.2 and Figure 4.3 show an overall signal flow for the Record and Reproduce sides of the system. Figure 4.2 is applicable in an overall sense to the AHBR system as well as the HBR 3000.

Section V

SYNC INSERTER (ECC) PWA

Part No 1261623
Schematic No 1261620

5.1 Description.

The sync inserter, shown in Figure 5.1 and Figure 5.2 , is basically the same as the standard sync inserter. The major differences are in the sync word format, the generation of a parity channel for use in the ECC system and the insertion of data in the Channel 15 and 16 sync words.

5.1.1 Compatability

This assembly is compatable with the standard Sync Inserter (pn 1803074) and can be used as a replacement in standard HBR systems, future production will probably adopt this as the standard for all systems. Note that the Sync Inserter (Parity), pn 1257573, is NOT the same as the Sync Inserter (ECC) described here and it cannot be replaced by any other sync inserter if its parity function is used.

5.2 Sync Word Generation.

The sync word generation is the same as the standard HBR except that the the 17th bit of the 32 bit sync word is a one instead of zero, as shown in Figure 5.3 . This creates a sync word which is symmetrical about the center of the last half (ie bit positions 17 thru 32) of the sync word. Since the Deskew logic only reads the last half of the sync word (16 bits) and in fact it ignores the first bit of this pattern the new sync word is compatable with existing systems in the forward direction.

Since the first half of the sync word will be used for ECC functions (see CRC GENERATOR/INSERTER) the pattern still remains compatable with existing systems. When ECC is disabled (ECC/NOECC is low) the sync word reverts to the standard non-ECC 32 bit word with 4 zeroes in the center.

5.3 Parity Channel

The Parity channel is generated as a perpendicular (across the tape) function of the incomming data. It becomes and is treated as a data channel, for the purposes of sync insertion and data distribution, as shown in Figure 5.4 . The Parity generated is called even parity, which means that the Parity Channel will have a one or zero in it such that

the total number of ones, including the Parity Channel, will be even (0,2,4,6,8,etc). This becomes obvious when an even number of parallel data channels is selected. If they all have the same input data (ie. Parallel Test Mode) the Parity Channel will be all zeroes.

5.3.1 14 Track Systems.

The Parity channel is handled as if it is Data Channel 12 or 13. For up to 11 customer data channels it will normally be channel 12, if there are 12 customer data channels (or if channel 12 is selected as a data channel with less than 12 data channels) it will be channel 13.

5.3.2 28 Track Systems.

For a 28 track system there will normally be 2 parity channels, one in each DPB, each generated as if each is a separate 14 track system. The Parity channel will be channel 12 or 13 in the A bay and 25 or 26 in the B bay. Note that the channel numbers are not changed, ie. the first channel in the B bay is still Channel 14.

If it becomes necessary, due to the need for 24 customer channels and an Aux. channel, a single parity channel is generated in the "A" DPB and it is channel 13. The single parity channel is created by taking the parity sum generated in the "B" DPB (PARITY–SI) and combining it with the parity of the "A" DPB channels. While this results in less overhead it also results in less error correction and the corrected error rate may be up to twice (2X) the corrected error rate using two parity channels. The Aux channel will be in the B bay in place of channel 26.

5.4 Parity (ECC) channel selection.

The channels used to create the parity channel (those that will be error corrected) are selected by dip switches on the front of the SYNC INSERTER PWA, as shown in Figure 5.4 . Any combination of channels can be selected, except that Channel 13 can only be uncorrected data (no correction on Channel 12) or the Parity channel (Channel 12 is data to be corrected). When ECC is turned off, all 13 channels are available for Customer Data. It is also important to remember that the Filter PWA can select channels 12 and/or 13 as Aux Channels. If this is done the Parity Channel will not be recorded and no error correction can take place. The B bay follows the same convention as the A bay with channel 14 as channel 1 and channel 25 or 26 as the Parity Channel.

5.5 Auto Channel Select.

The Sync Inserter has 2 sync words generated but not normally inserted in the channel 14 and 15 slots of the Master Channel in each DPB. In order to facilitate the setup and configuration of an ECC system these are replaced with a 16 bit block of system information and a 48 bit block of optional customer information, as shown in Figure 5.5 .

The first 4 bits (of the 16 bit system block) are ECC channel information, formatted as a sync bit, and then 3 channel select bits. It takes 4 blocks to complete the channel select for all 12 channels in each DPB. In addition the next four blocks contain the same information but inverted for data checking in reproduce mode. The channel select information is taken from the format select switches on this card. The next 12 bits are reserved for later expansion.

5.6 48 Bit Customer Data.

This block (one in each DPB) is provided for the customer to store (record) any information that is of a low rate or "blockable" nature. The system provides a gate signal which is 48 bits wide and parallel clock. The first bit of data is clocked into the system on the first positive parallel clock edge after the gate (M48 GATE) goes low. Thus the first bit to be recorded should be at the input before the gate goes low and subsequent data should loaded on positive parallel clock edges.

5.7 Format Compatability.

Compatability and tape interchangeability between ECC and non-ECC systems is as follows:

5.7.1 ECC format tapes

1. Tapes recorded with ECC format are playable with Error Correction in the forward direction only and in the reverse direction without Error Correction on ECC equiped systems.

2. Tapes recorded with ECC format are playable on standard (non-ECC) systems only in the forward direction, and of course there will be no Error Correction.

3. Non-ECC systems built with ECC type Deskews will play ECC format tapes in both forward and reverse directions, without error correction of course.

5.7.2 Non-ECC format Tapes

1. ECC systems are capable of playing non-ECC format tapes in the forward direction.

Section VI

CRC GENERATOR/INSERTER (ECC) PWA

Part No. 1261713
Schematic No. 1261710

6.1 Description.

The function of the CRC generator/inserter PWA is to generate a 16 bit binary check-word from the 480 bits of data between sync words and insert this word into the first 16 bits of the 32 bit sync word, as shown in Figure 6.1 .

6.2 Gate Generation

In order to generate and insert the check word it is necessary to generate a series of gate signals which correspond to the location of the first 16 bits of the sync word in each data channel. See Figure 6.2 .

The counter lines from the Sync Inserter (SI–CTR–A,–B,–C,–D) are used to generate a series of 32 bit gates corresponding to the location of the sync words, they are also used to preset a counter which generates a clock at 1/16 the parallel clock rate. This clock (C16) is used to blank the last half of the 32 bit gate in each channel. This signal, the Check Word Enable (CWE), is used to gate the check word in each channel, but leave the 16 bit sync word intact.

6.3 CRC Generation

The CRC generator is a single IC which performs a binary algebraic operation on incomming serial data. This results in, for the mode we have selected, a 16 bit check sum being generated. The operation is much like a pseudo random data generator. As long as the CWE input is held high and clock is fed into the device it continues to cycle the input data thru a shift register with feedback which controls the algebraic manipulation. When the CWE input is set low, the input data is ignored and during the next 16 clock cycles (the first half of the 32 bit sync period), the remaining states of the shift register are clocked out as a 16 bit CRC check word, as shown in Figure 6.3 . At the end of the CWE, the CRC Generator is reset to start a new computation on the next 480 bit block of data. This results in a check word which is generated by and only related to the last 480 bits of data.

6.4 CRC Insertion

The input data from the Sync Inserter is continuously sent to the CRC generator and the output selector switch, as shown in Figure 6.3 . When the CWE goes low, indicating a CRC checkword is being sent, the output selector is switched to allow insertion of the CRC checkword.

Section VII

MASTER DESKEW (ECC) PWA

Part No. 1261793
Schematic No. 1261790

7.1 Description.

The Master Deskew PWA is functionally equivalent to the Master Deskew presently used in the HBR system. The only differences are that the Master channel data is brought out for use in the error correction process, the CSAA, CSBA, CSCA, and CSDA lines are brought out to allow synchronization of the error correction electronics and the sync blanking and distributed data outputs are turned off in an ECC system. The counter preset logic is modified to read the ECC format sync words in both forward and reverse, however error correction is only performed in forward mode. See Figure 7.1 .

7.1.1 Compatability

This PWA may be used in place of the Master Deskew PWA (pn 1803064) by changing the E26-E27 (ECC) jumper to E27-E28 (nonECC) and removing the CS driver IC (U8).

7.2 Tape Reference Selection

The circuitry which divides the parallel clock and Master Channel Bit Sync clock to drive the transport in Tape Mode has been changed for operational simplicity and compatability with various transports. Divide by 2 is selected with solder jumpers, however this mode is very rarely needed and is considered a special case which would probably on be used on otherwise highly modified systems. There are now a pair of DIP swithes which allow selection of divide by 4, 8, 16, or 32. This allows simple selection of the frequency which the transport would most like to see. Most systems operate well at divide by 8, but at high packing densities divide by 16 might work better. Conversly at low speeds (ie. below 7 1/2 ips) divide by 4 might work better. The Airborne transports also require frequencies lower than the Lab systems, and this allows simple selection of the appropriate division ratio.

7.3 Sync Detection.

In the standard system the sync word is a 32 bit word symmetrical about the center bits. The logic is such that only the last half of the word is read and thus the logic remains the same for both forward and reverse directions. Actually only the last 15 of the 32 bits are read, thus the new 16 bit sync word with a one as the first sync bit is

compatable with standard sync detection logic. By making the first bit of the 16 bit sync word a 1 the sync word is identical in forward or reverse and sync detection identical to the standard system.

In the ECC system, however, the first half (in forward mode) of the 32 bit period is filled with CRC information, thus if reverse mode were attempted the sync word would be read but it would be 16 bits early and the system would ignore the 16 bits of data before the sync word and assume the CRC word is data. Thus it is necessary, in reverse, to add 16 to the counter preset to correct this. This is accomplished by changing the logic in the counter preset circuitry. This does prevent reading standard (32 bit sync) tapes in reverse as the Sync word would be read where the CRC information would be placed and the effect is to displace the logic 16 bits in the opposite direction to the previous discussion.

Section VIII

SLAVE MASTER DESKEW (ECC) PWA

Part No 1261863
Schematic No 1261860

8.1 Description.

Changes to the Slave Master Deskew are identical, functionally, to the Master Deskew changes, except there is no transport reference generated on this board, thus no DIP switch.

8.2 Compatability

The standard Slave Master Deskew (pn 1802995) may be replaced by this PWA if the jumper E9-E10 (ECC) is changed to E10-E11 (nonECC) and the CS driver IC (U20) is removed, except where standard (32 bit sync word) tapes must be read in reverse.

Section IX

SLAVE DESKEW 2 CHANNEL (ECC)

Part No 1261783
Schematic No 1261780

9.1 Description.

The Slave Deskew changes are the same Forward/Reverse logic changes as the Master Deskew.

9.2 Compatability

The sync blanking and data reinsertion circuitry has a jumper added to allow either ECC or nonECC operation. In ECC position the data and sync are sent directly to the output and in nonECC position the Data Reinsertion and reclocking are connected. This PWA can then be used to replace the 2 Channel Slave Deskew (pn 1806063) in standard HBR systems, except where reverse read of a standard (32 bit sync word) tape is required. Remember this is a 2 channel device and therefore there are two jumpers to change.

Section X

512 BIT DELAY AND ERROR DETECTOR (ECC) PWA

Part No 1261633
Schematic No 1261630

10.1 Description.

As the title indicates there are two functions on this card, detection of errors and delay of the data.

10.2 512 Bit Delay.

Since an error cannot be recognized until after the data has passed, it is necessary to delay the data until after the error check occurs. While this is only 496 bits it is easier from a hardware point of view to delay it 512 bits. Figure 10.1 shows how the delay is accomplished by a pair of 256 bit RAM's in each data channel. A series of counters, synchronized to the Master Channel via the CS lines, generates consecutive adresses to the memory. During the first 60 ns. of each address a data bit is read from that address in the memory, then the Write Enable is activated and a new data bit is written into the same address. 512 clocks later the same address is accessed and thus the data will be read out with a 512 bit delay. Since the Memories only have 256 addresses, two memories are used with the most significant address used as a Chip Select. This has the effect of placing the two memories in series.

10.3 Error Detection.

Error Detection makes use of the CRC word inserted in the first 16 bits of the sync word time to detect if an error occurred within the 480 bit data block.

10.3.1 Gate and Counter Logic

The Counter is used as described in the Delay paragraph to generate the memory addresses. The Gate logic, see Figure 10.2 , and Figure 10.3 , generates a series of 16 bit gates similar to the CRC Generator in section VI. These gates are used to latch the error Flag and reset the CRC detector. A signal from the Error Corrector PWA called the Serial Flag is used to determine which channels are active in the ECC process, all other channels are reset continuously and do not produce any Error Flags.

10.3.2 Flag Detection

Error Flags are generated on a per channel basis as shown in Figure 10.4 . There are two flag outputs, one goes to the Error Corrector PWA and the other is a monitor signal.

The data is sent thru a CRC encoder chip, as it was on the CRC Generator card, as shown in Figure 10.5 . At the end of the data block the 16 bit CRC word is also allowed to enter the encoder chip. If there are no errors the shift register stages will all be zeroes and the output of the CRC encoder will be a zero as shown in Figure 10.6 . If there was an error one or more of the shift register stages will not be zero and the output will be a one. The output (one or zero) is latched during the last bit of the CRC word (the only time it is valid), delayed for the 16 bits of the sync word, for a total delay of 32 bits after the last data bit and then held for 480 bits until the next CRC word begins.

Thus after a block containing error(s) is recognized a Flag is generated which is delayed by 16 bits, held for 480 data bits, and reset for 16 bits for a total of 512 bits. Since the data is delayed for 512 bits, the data and flag will occur at the same time.

10.4 M48 Gate.

The gate signal (active low) for the customer 48 bit data block in the Master channel is also generated on this card, as shown in Figure 10.7 . It ocurrs from the middle of the Channel 14 sync time to the end of the Channel 15 sync time. It goes low slightly after the positive edge of the parallel clock, thus the negative or positive edge of the parallel clock occurring after the Gate has gone low can be used to load the M48 data from the Master Channel into registers in the customers equipment.

Section XI

ERROR CORRECTOR AND DATA REINSERTION (ECC) PWA

Part No. 1261903
Schematic No. 1261900

11.1 Description.

The Error Corrector and Data Reinsertion PWA, shown in Figure 11.1 , has three main functions, to determine if one and only one track has errors on it, to correct the errors if that is true, and to recombine the data in the Master Channel with the respective data channels.

11.1.1 Channel Select

Channel selection for error correction can be selected by either the DIP switches on the front of the PWA or by the optional Auto Channel Select PWA. In the manual mode, see Figure 11.2 , the data channels are selected by the DIP switches to match the recorded format. The Parity Channel is automatically determined to be channel 12 or 13 in a manner similar to the CRC Generator. If the format selected does not match the recorded format the Error Correction will probably not work and may in fact be detrimental, since the recorded Parity will be different from the Parity check done in reproduce. After blanking the CRC and Sync word (which were not used in the recorded parity calculation), each channel selected will route its data to the Parity test circuitry.

The Auto Channel Select PWA can select Auto or Manual Mode. In Auto mode the base of the select transistor is grounded which opens the DIP switches. The format read from the tape is then used to select the active channels via the Channel Select inputs.

11.1.1.1 Serial Flag

The Serial Flag (SF) is a signal which consists of a series of 32 bit long signals indicating in a serial fashion which channels are selected. Since the Parity channel was created prior to Sync Insertion, the data which was moved from each Data Channel into the Master Channel must be included in the Parity check. The Serial Flag is used to gate the Master channel data so that data blocks from channels in the ECC format will be included in the Parity check, and all other blocks will be excluded. The Serial Flag is also used by the Delay/Detector PWA to clear the Error Flag circuit on the active channels, See Section X.

11.2 Flag Arbitration Logic.

The Flag signals from the Error Detector PWA are sent to an analog comparator circuit which determines how many flags are present. Each flag has a weight of proportional to the number of flags present as shown in Figure 11.3 .

A FLAG ONE is generated by the first comparator which has a reference of 0.75 units and will change state if one or more Flags are present (1.0 or more units) the ONE Parity channel system along with the FLAG ONE from the other DPB to indicate two channels in error (one in each Bay), which creates a FLAG TWO. For Two Parity channel systems this signal is not used.

A FLAG TWO signal is generated by the second comparator which has a reference of 1.25 units. If 2 or more Flags are present (1.5 units or more) the comparator changes state and the Error Correction is disabled. This signal is also sent to the other DPB for use in ONE Parity Channel systems. This is required as the system is limited to correcting one and only one channel with errors (see description of Parity checking). The TWO/ONE switch selects how many Parity Channels are in use. The A/B switch is used to program whether this card is in the A or B DPB. Since the Parity channel in a ONE Parity system is in the A Bay the B Bay parity channel must not be selected. In Two Parity channel systems the A/B switch has no effect.

11.3 Data Correction/Reinsertion

Data Correction and Reinsertion is performed on a per channel basis, as shown in Figure 11.4 .

11.3.1 Error Correction

The Error Correction circuit does a parity check of all of the data channels, portions of the Master Channel and the Parity Channel. If no error exists the check is ok and no further action is taken. If an odd number of channels have an error the parity checking circuit has an error output. This signal is sent to the correction logic where a decision is made whether or not correction should take place. If only one channel has a FLAG the data in that channel is corrected by inverting its state, if two or more channels have errors the FLAG TWO signal will inhibit the correction.

11.3.2 Sync Blanking.

On the record side the Parity channel was generated before sync words or the CRC words were added to each channel and before the Master Channel was generated done. In addition the data during these periods was part of the parity, so the Master Channel (which now contains the 32 bit blocks removed from the Data Channels) must be included in the parity check (see the description of Serial Flag). If the check is done after data reinsertion, the Error Flag from the Master channel would have to be distributed as well as the data which would severly complicate the logic required.

11.3.3 Parity Checking.

The parity generation in this system is called even parity, where the parity channel contains a one or a zero such that the total number of ones in all the channels (including the parity channel) is a even number (0,2,4,6,8 etc). If an even parity check is then made of all of the channels including the parity channel, the result will always be zero. If an error exists in one channel the result will be one. However, if two channels have simultaneous errors the result will again be zero as if no error existed. The Error Detection PWA only detects error(s) somewhere in a 480 bit block thus if one channel has a block with error(s) overlapping a block with errors in another channel neither can be corrected during the time the blocks (and corresponding Flags) overlap.

In a one parity channel system, the Parity result (PAR–ERR–OUT) of each Corrector is sent to the other Corrector (PAR–ERR–IN) and a final calculation is made independently on each Error Corrector PWA. This reduces the time required to make the calculation.

11.3.4 Data Reinsertion.

Reinsertion of the data from the Master channel into the various Data channels is accomplished in a similar manner to the standard HBR system except that it is done on this PWA instead of the individual Slave Deskew cards.

11.4 Parity Retest.

After the Data channels are corrected and reinserted a parity check is again performed to verify the data. The Parity result is provided on an output pin.

11.5 M48 Data

The master channel data (DATA–CORR–M) is sent to an output connector where, along with a 48 bit gate (fron the Error Detector and Delay PWA) the customer can select his data out of the Master channel with the M48–GATE and parallel clock. The M48 data cells are aligned with the negative going edges of the Parallel clock, thus the first data bit is valid at the first positive going edge of the Parallel after the the M48 GATE goes low.

Section XII

AUTO CHANNEL SELECT PWA

Part No. 1262013
Schematic No. 1262010

12.1 Description

The Auto Channel Select PWA contains a Slave Deskew for Channel 13 and the logic for decoding the channel select information inserted in the first half of the Channel 14 sync time in the Master Channel. A toggle switch on the front of the PWA selects AUTO(up) or MANUAL(down) operation. A series of LED's indicate the ECC active channels.

12.1.1 Compatability

When the Auto Channel Select feature is not used a Slave Deskew (ECC) PWA may be inserted in this card location to perform the Channel 13 deskew function.

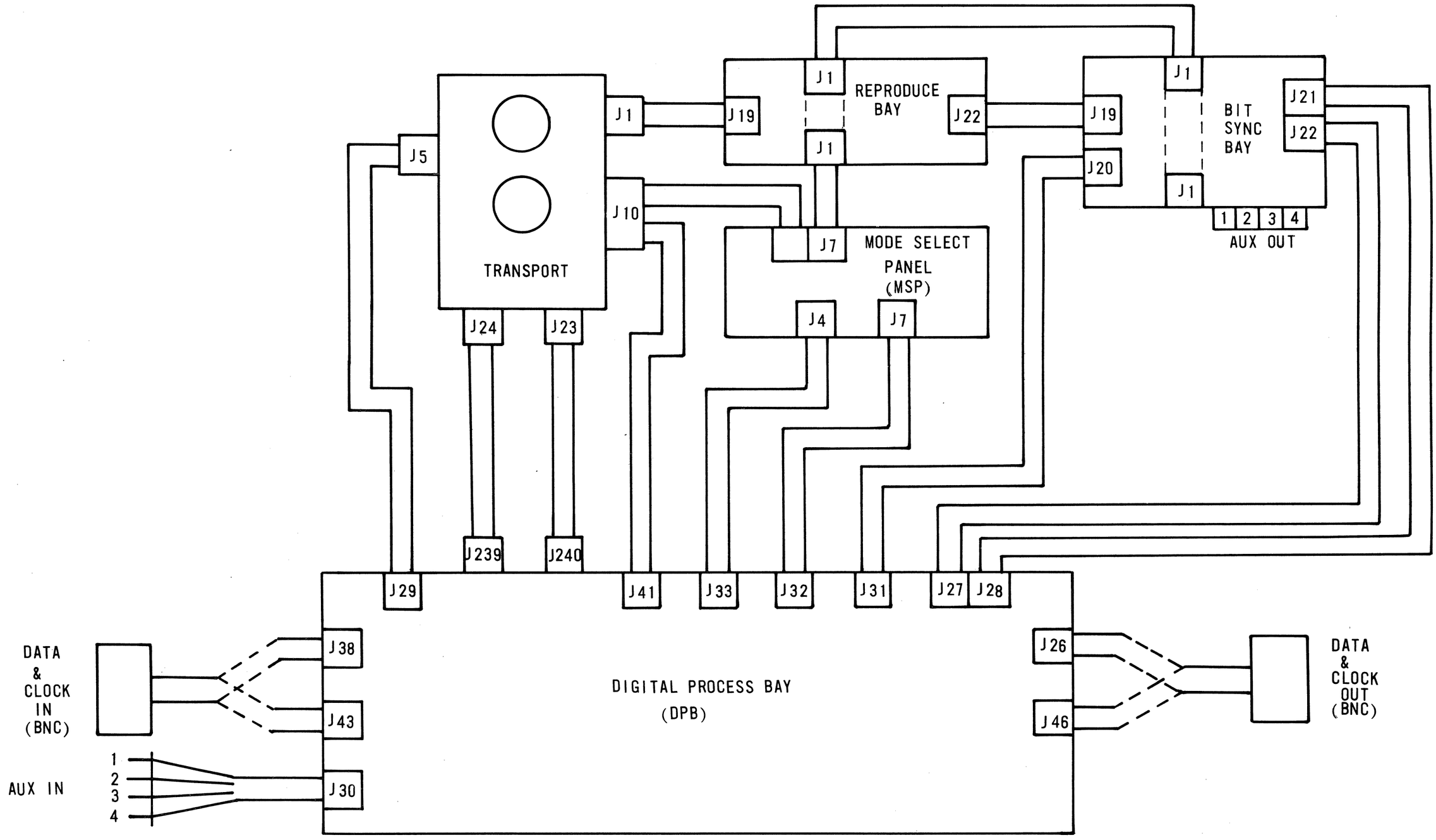
12.2 Auto Channel Select

The first 4 bits of the channel 14 sync period in the Master channel contain information relative to the channels active in ECC (ie. used to create the parity channel) when the tape was recorded. They are formatted in blocks as a sync bit and 3 channel select bits. Since there are a maximum of 12 customer data channels it takes 4 blocks to completely specify the format. In addition, the 4 blocks are repeated with inverted information to decrease the possibility of decoding an incorrect format. The channel select bits are a one for a selected channel when the sync bit is a zero and a zero for a selected channel when the sync bit is a one. Thus it takes 8 blocks to complete the channel select information.

The Channel 14 GATE starts a 4 bit shift register. See Figure 12.1 and Figure 12.2 . The first bit (sync) polarity is detected and sets an exclusive-or gate to pass or invert the following data bits. The sync bit is also sent to a latch which detects a change in the sync bit from a one to a zero. This point is the beginning of an 8 block segment of channel select information. At this point the data from the previous 8 blocks is transferred to the output latches (if there were no errors) and the error detector is reset.

The 3 data bits are shifted into a register and the register is held until the next block. After 4 blocks the first bit will be at the end of the register. When the next block (number 5) comes in the bit at the end of the shift register is compared withe the incomming bit. If they do not agree, a latch is set. This process continues for the next 12 data bits (4 blocks) and if any of the 12 bits do not agree the error latch will prevent the data from being transferred to the output latch.

The output latches drive open collector inverters which illuminate LED's on the front edge of the PWA and drive the channel select circuitry on the Error Corrector PWA. If the toggle switch is in the Manual position (down) the LED's are held off and the normal manual selection switches on the Error Corrector PWA are enabled. in the Auto position the manual selection switches are disabled and can be left in any position.



14 CHANNEL INTERCONNECT

Fig. 3.1

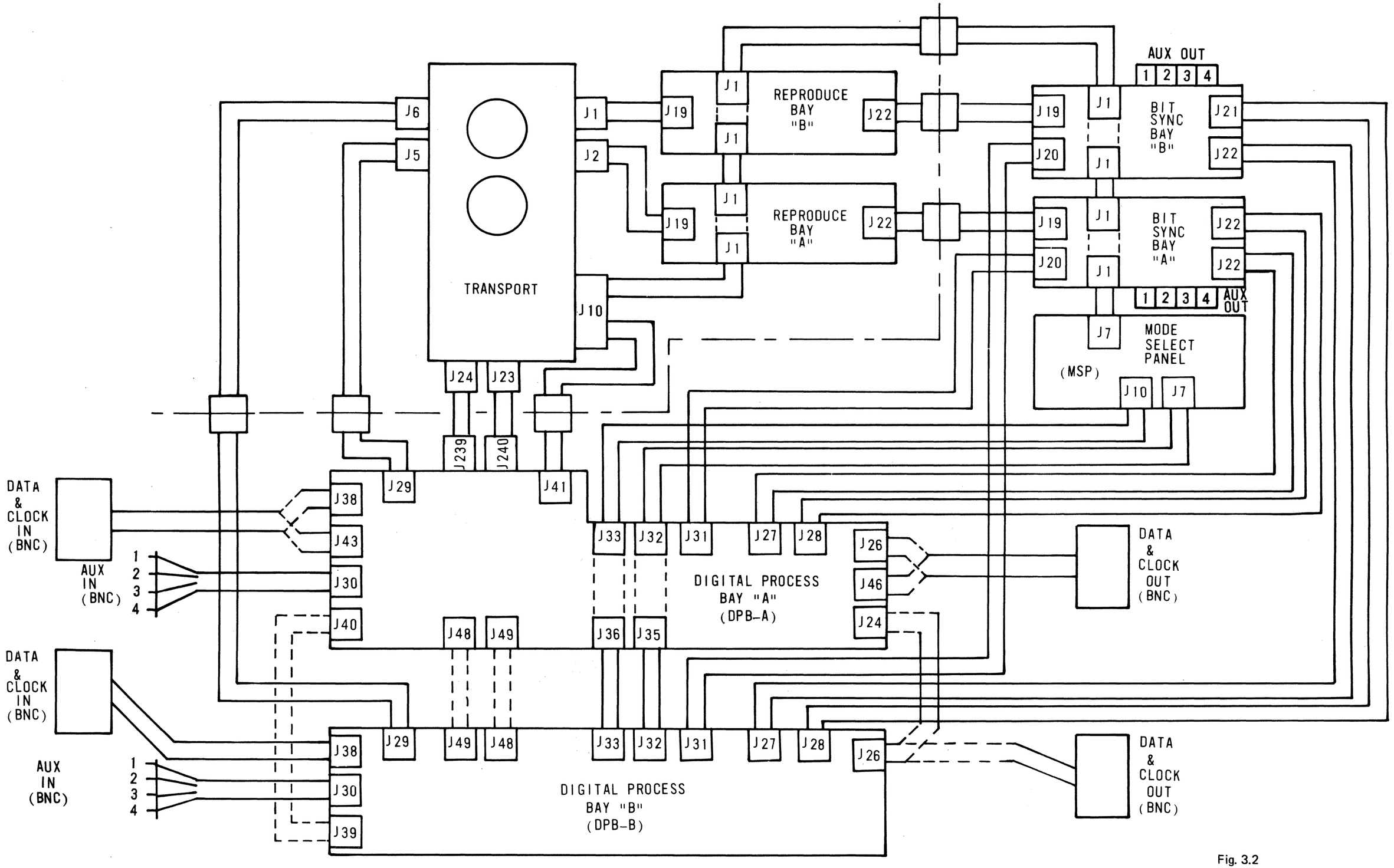
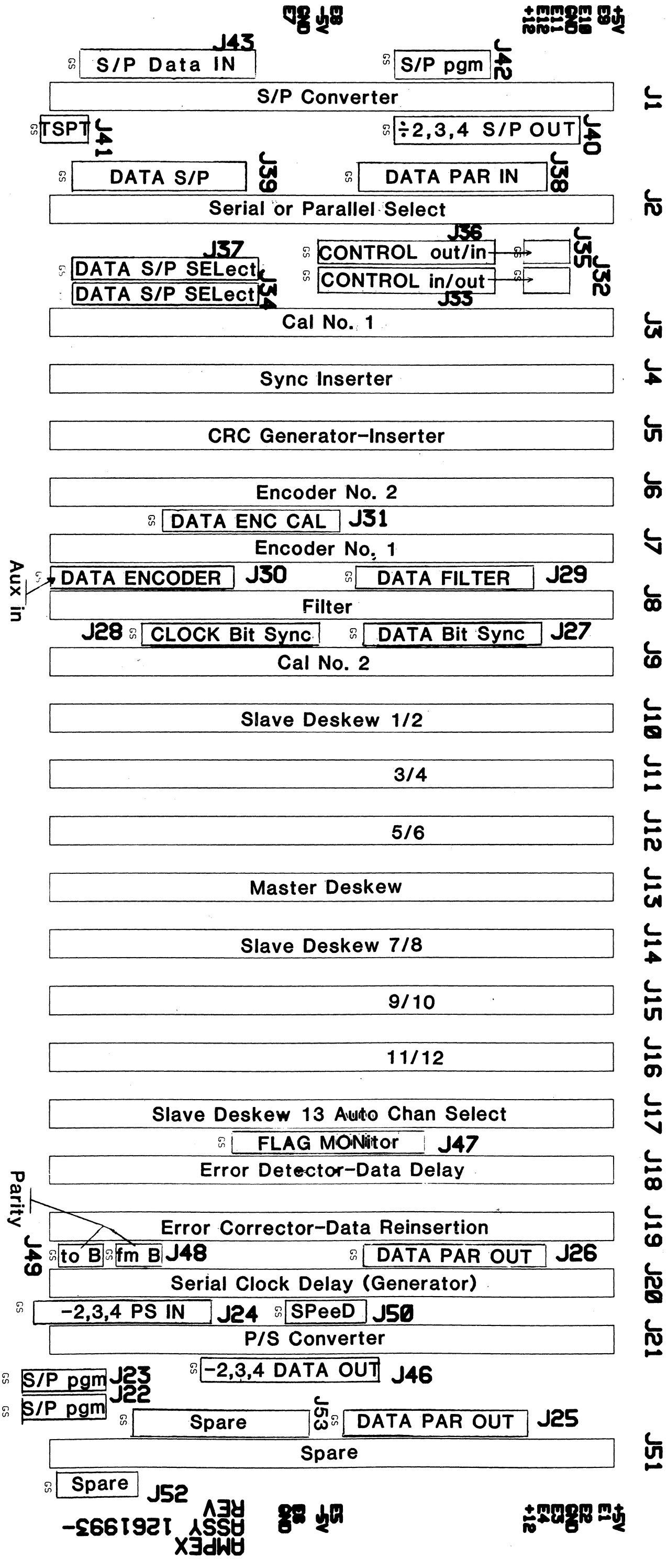


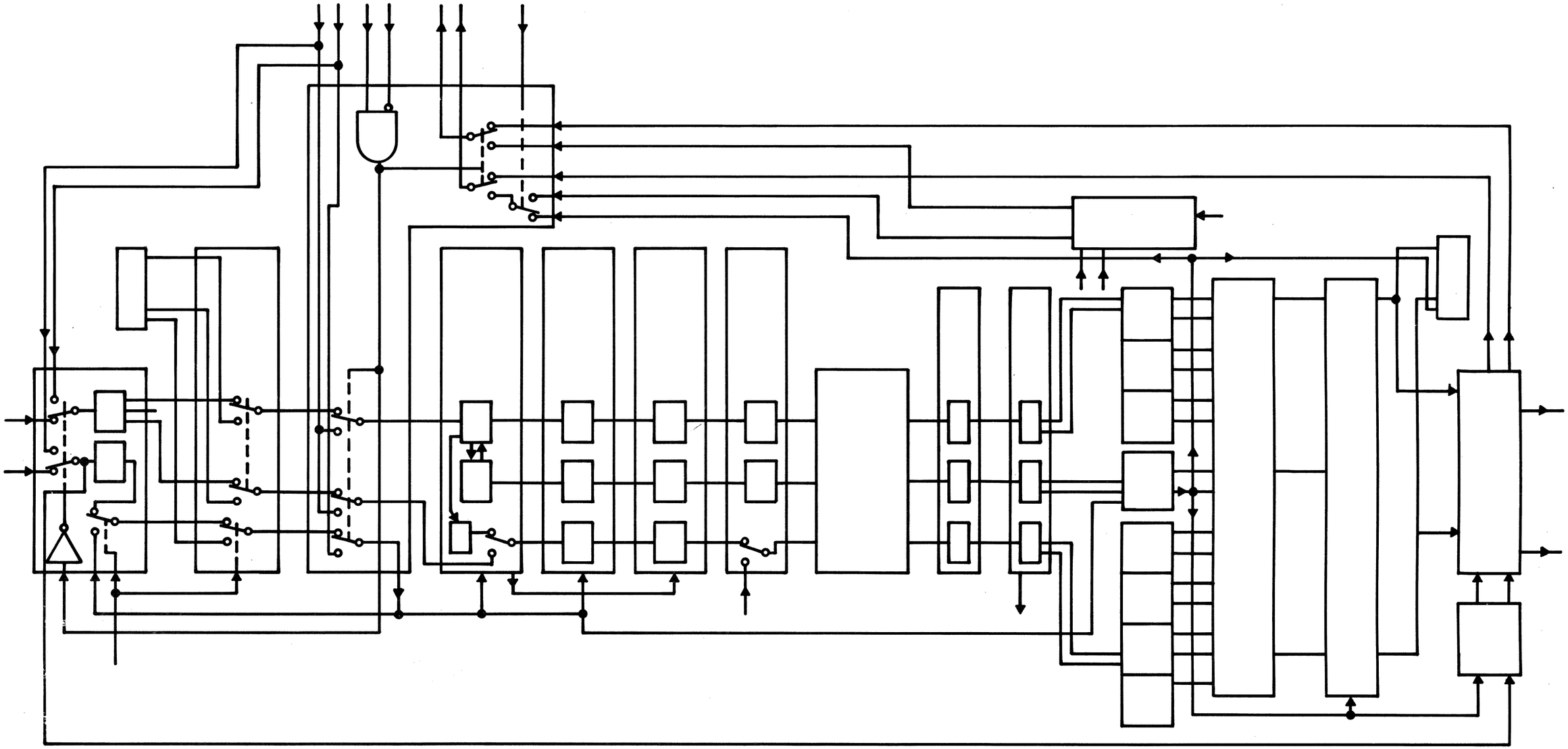
Fig. 3.2

28 CHANNEL INTERCONNECT



DPB MOTHERBOARD

Fig. 3.3



BLOCK DIAGRAM

Fig. 4.1

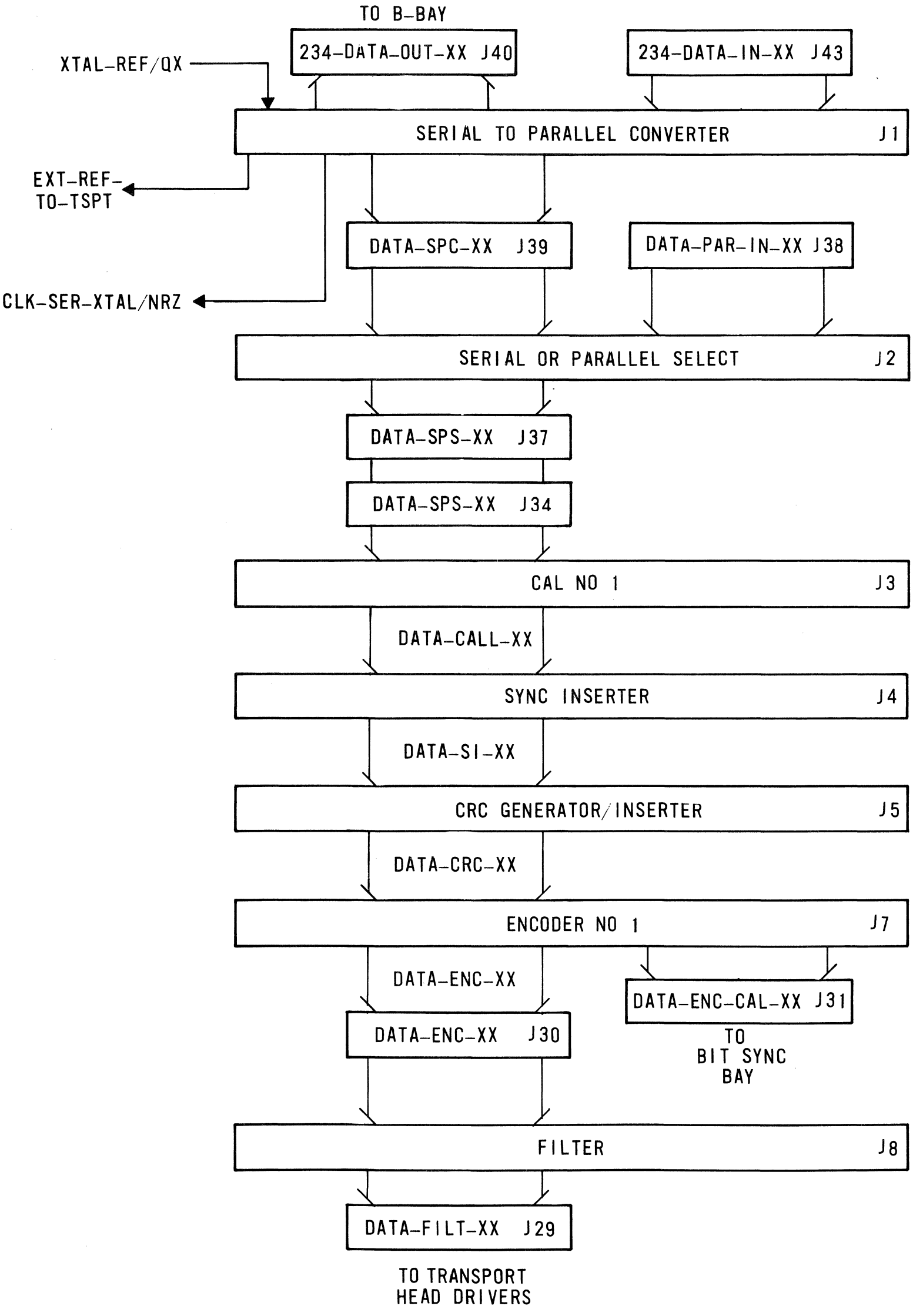
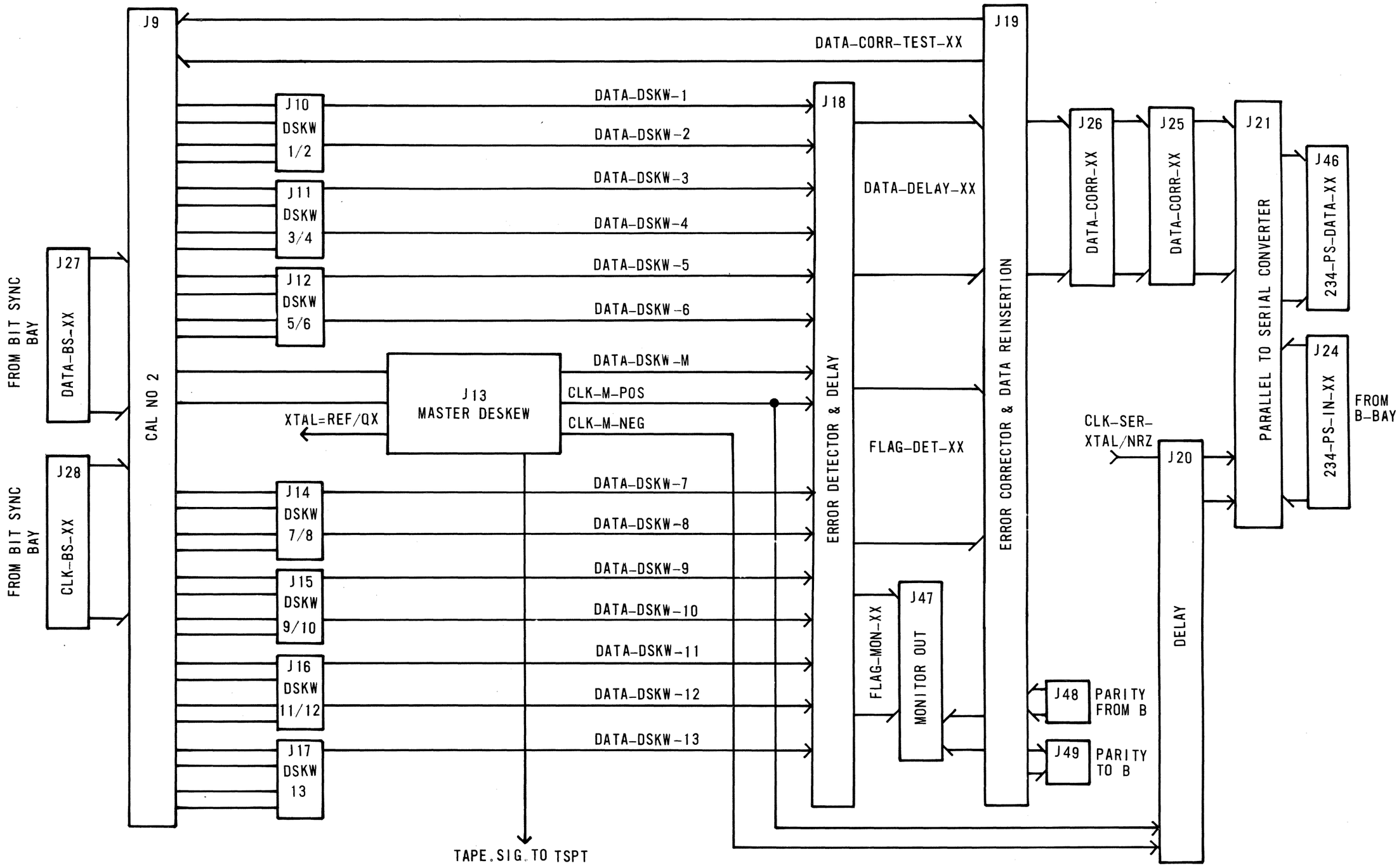


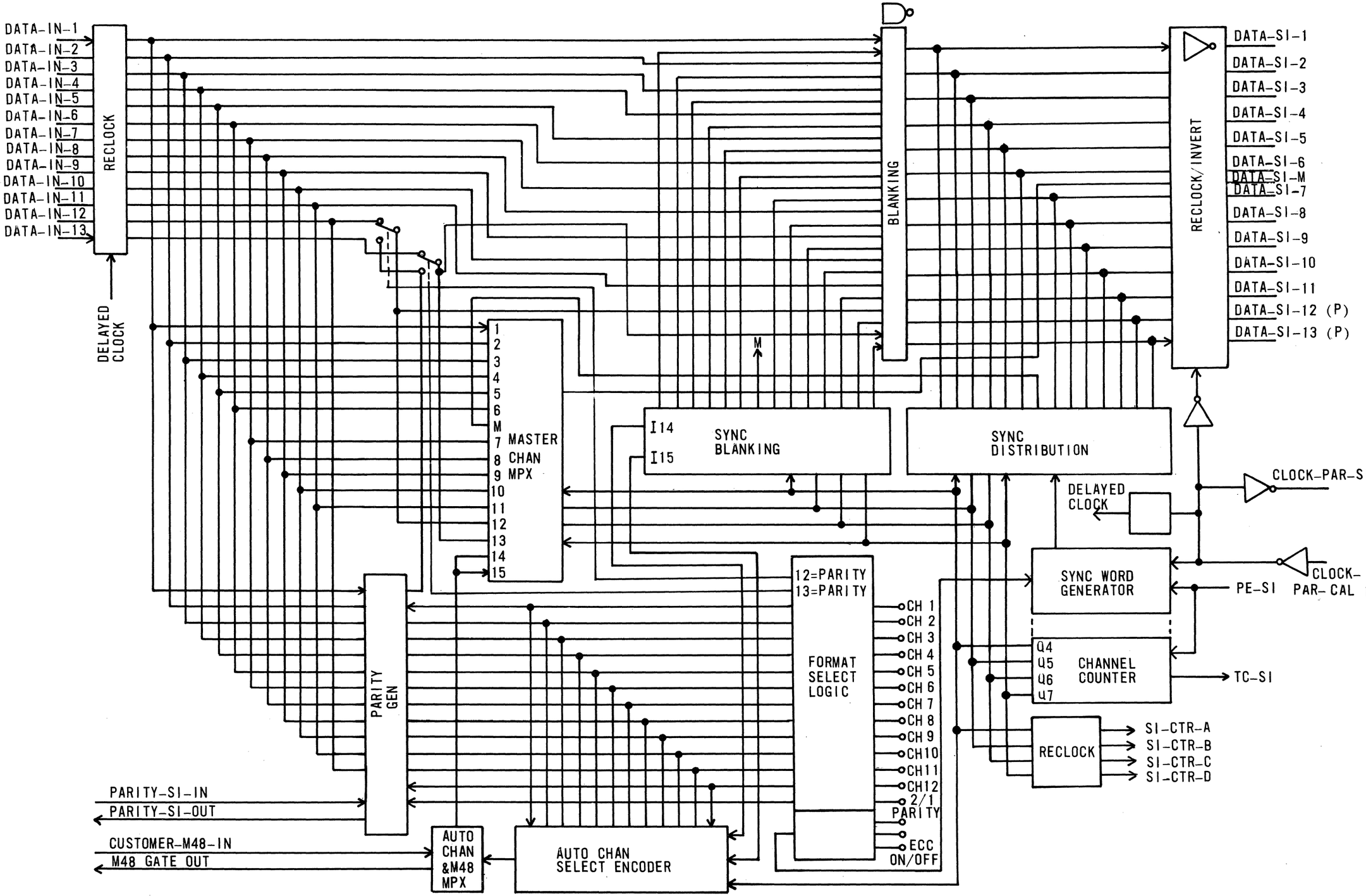
Fig. 4.2

DPB RECORD



DPB REPRODUCE

Fig. 4.3



SYNC INSERTER BLOCK

Fig. 5.1

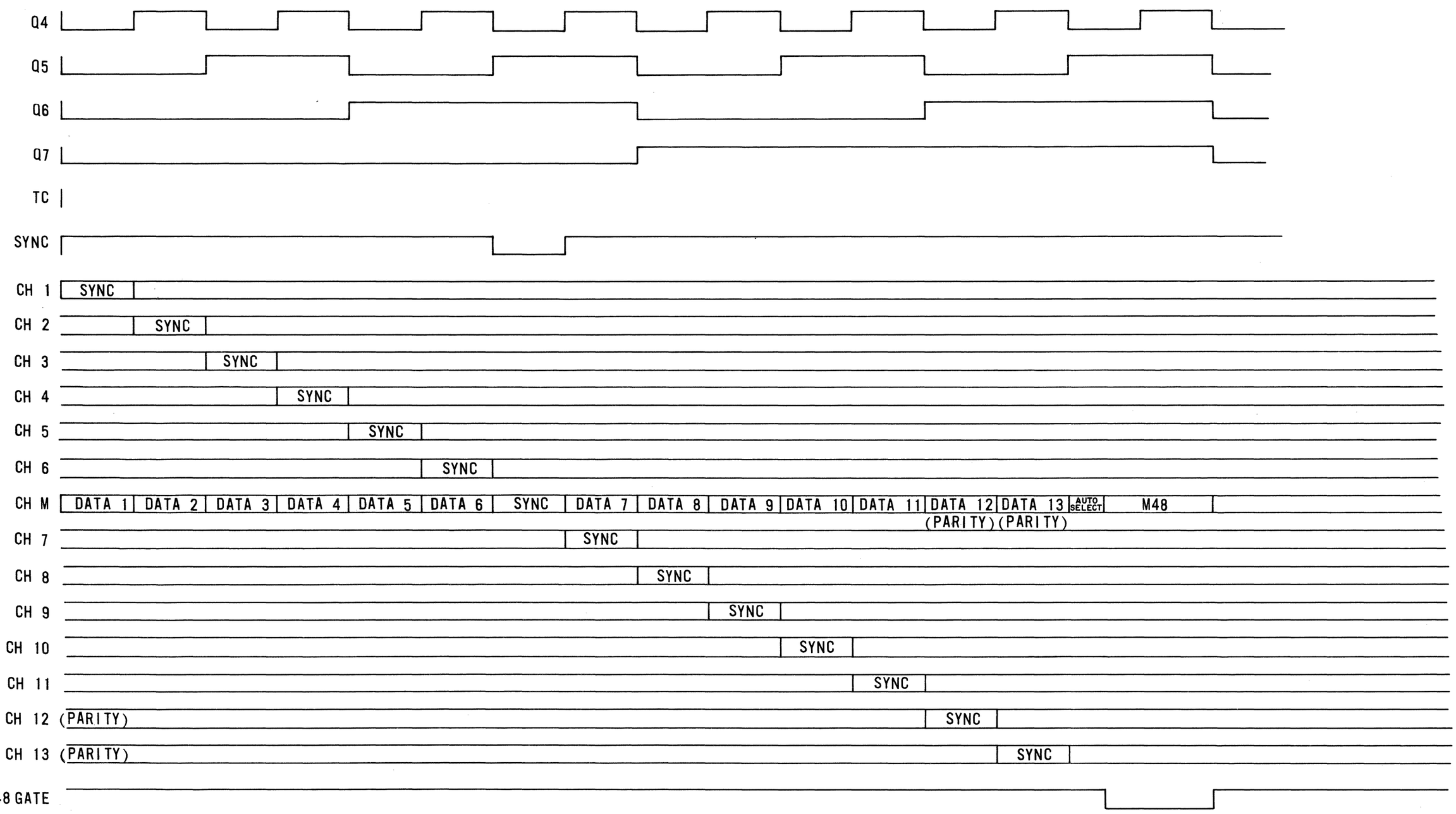


FIG. 5.2 **SYNC INSERTER TIMING**

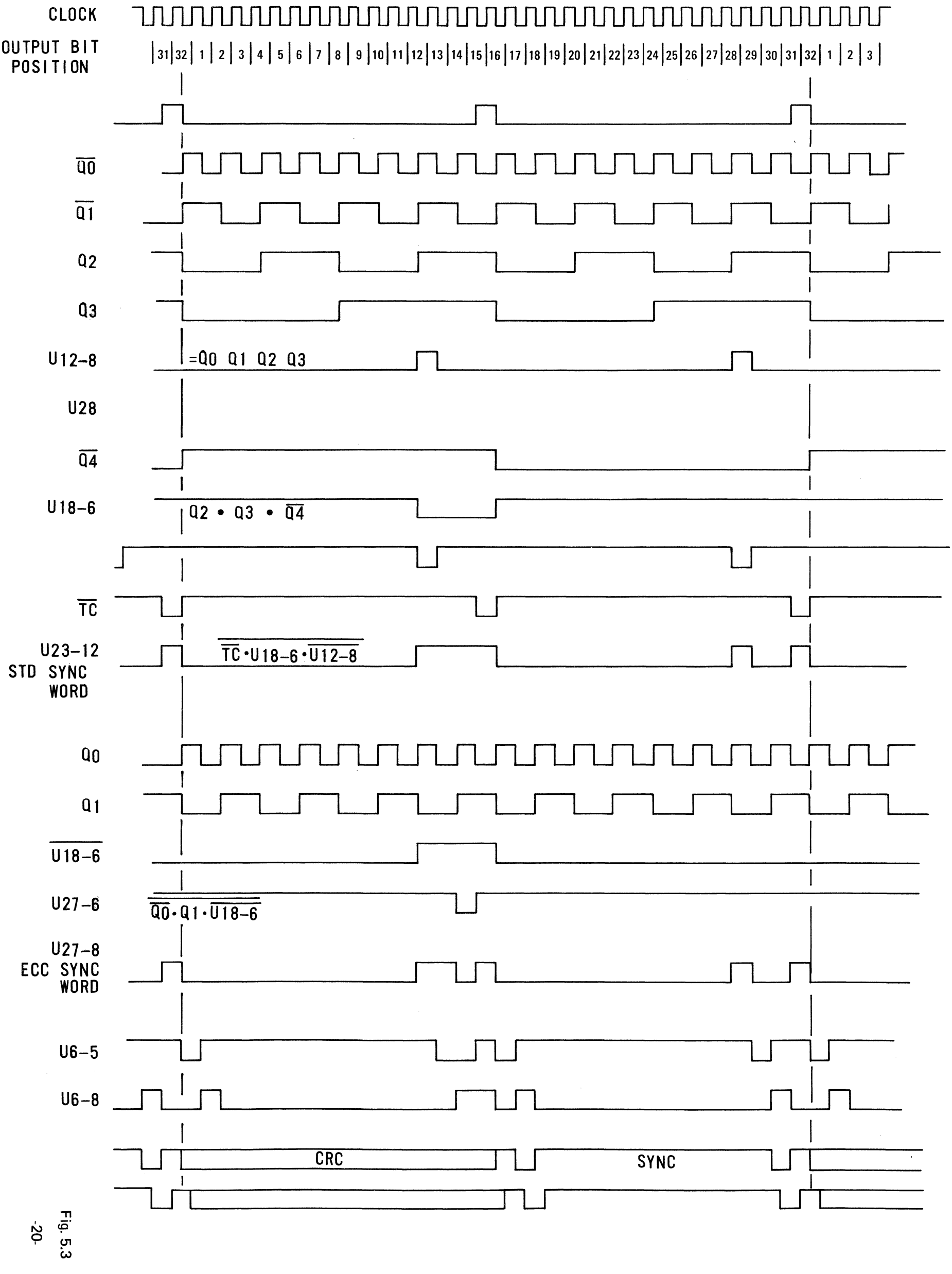


Fig. 5.3

SYNC GENERATION

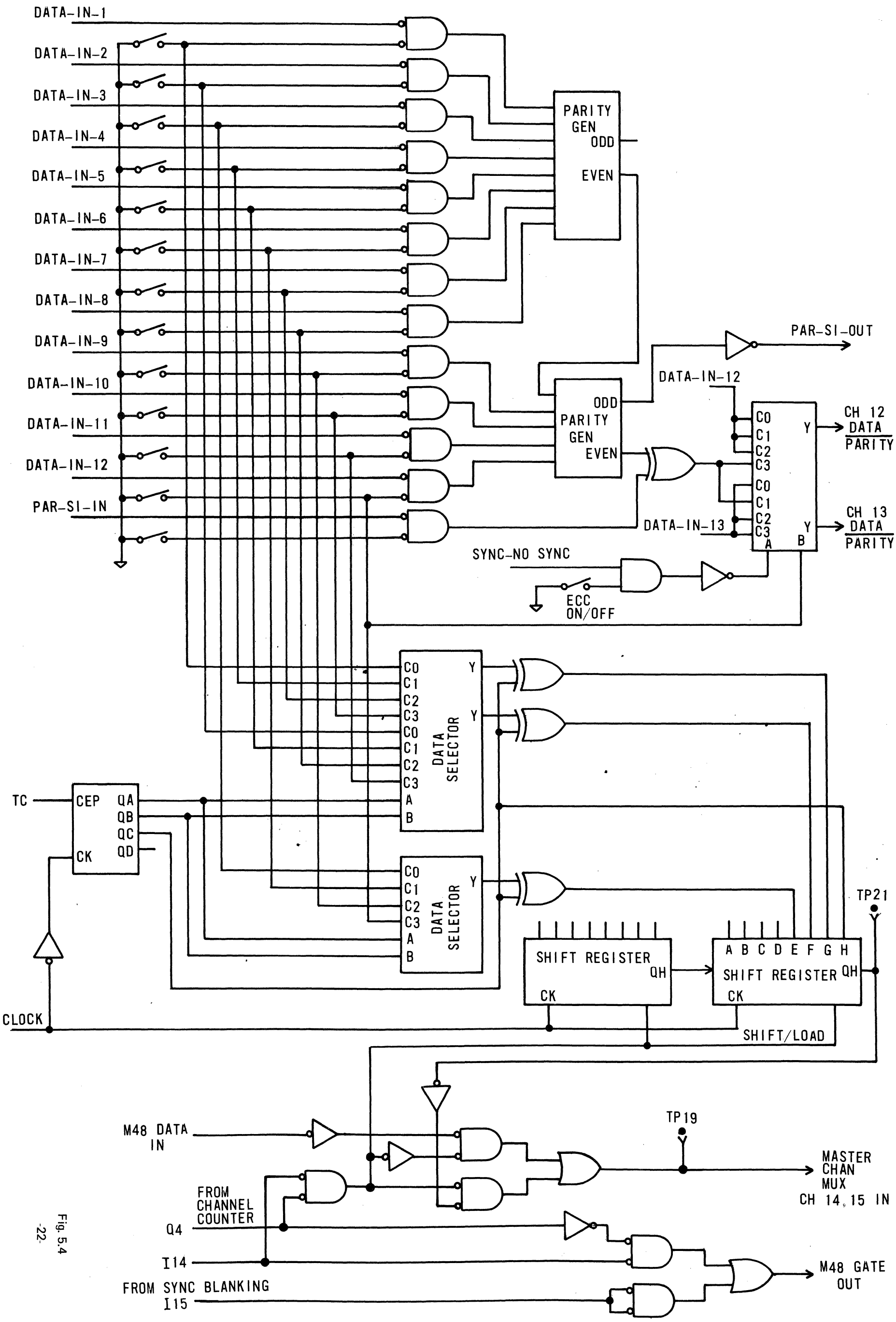
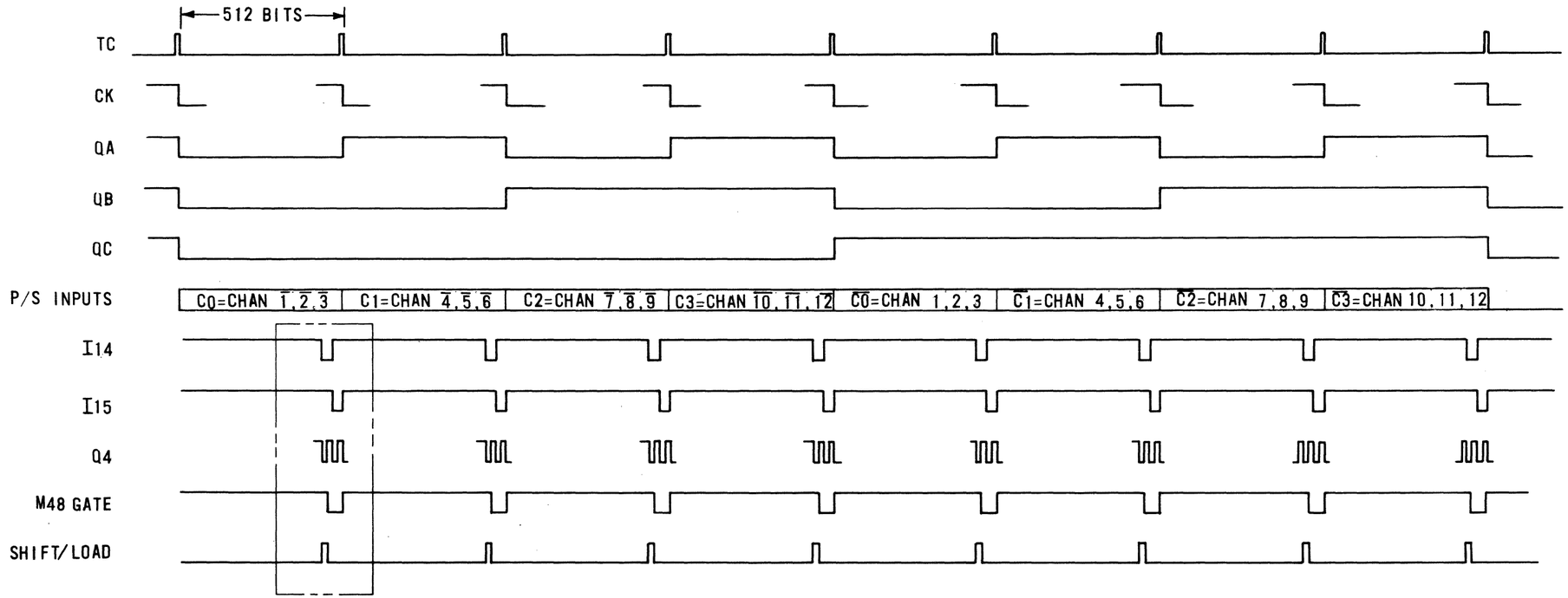
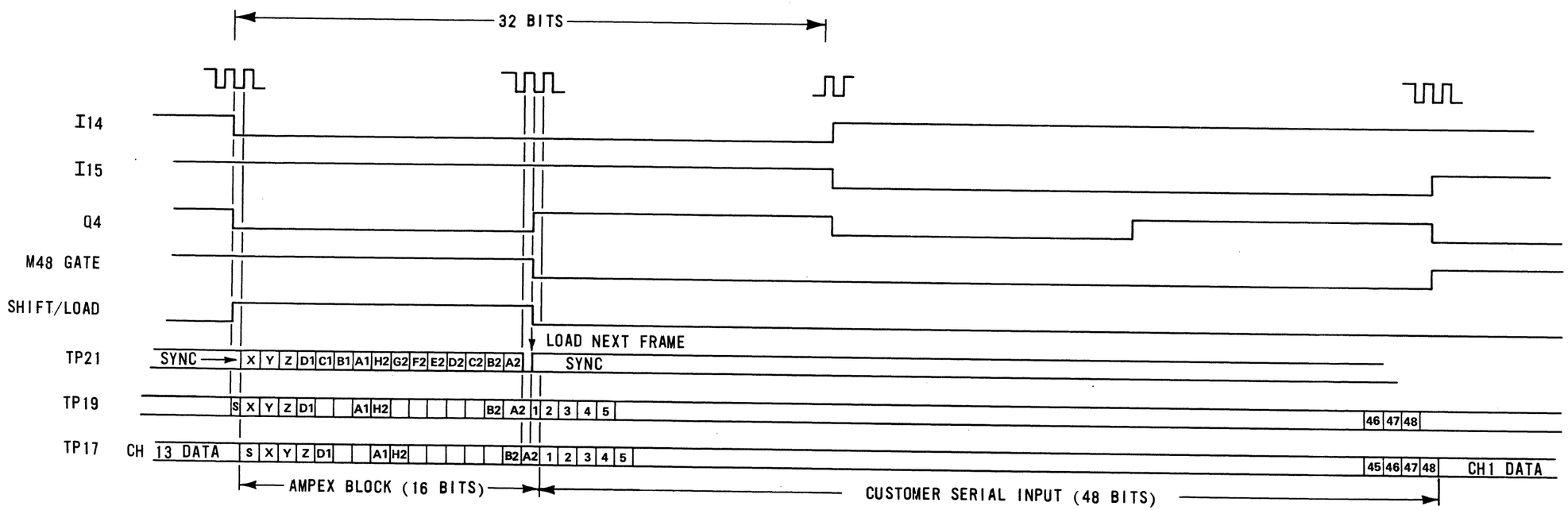


Fig. 5.4

PARITY GENERATION CHAN SELECT



SEE ENLARGED VIEW BELOW



AUTOMATIC CHANNEL SELECT - M48

Fig. 5.5

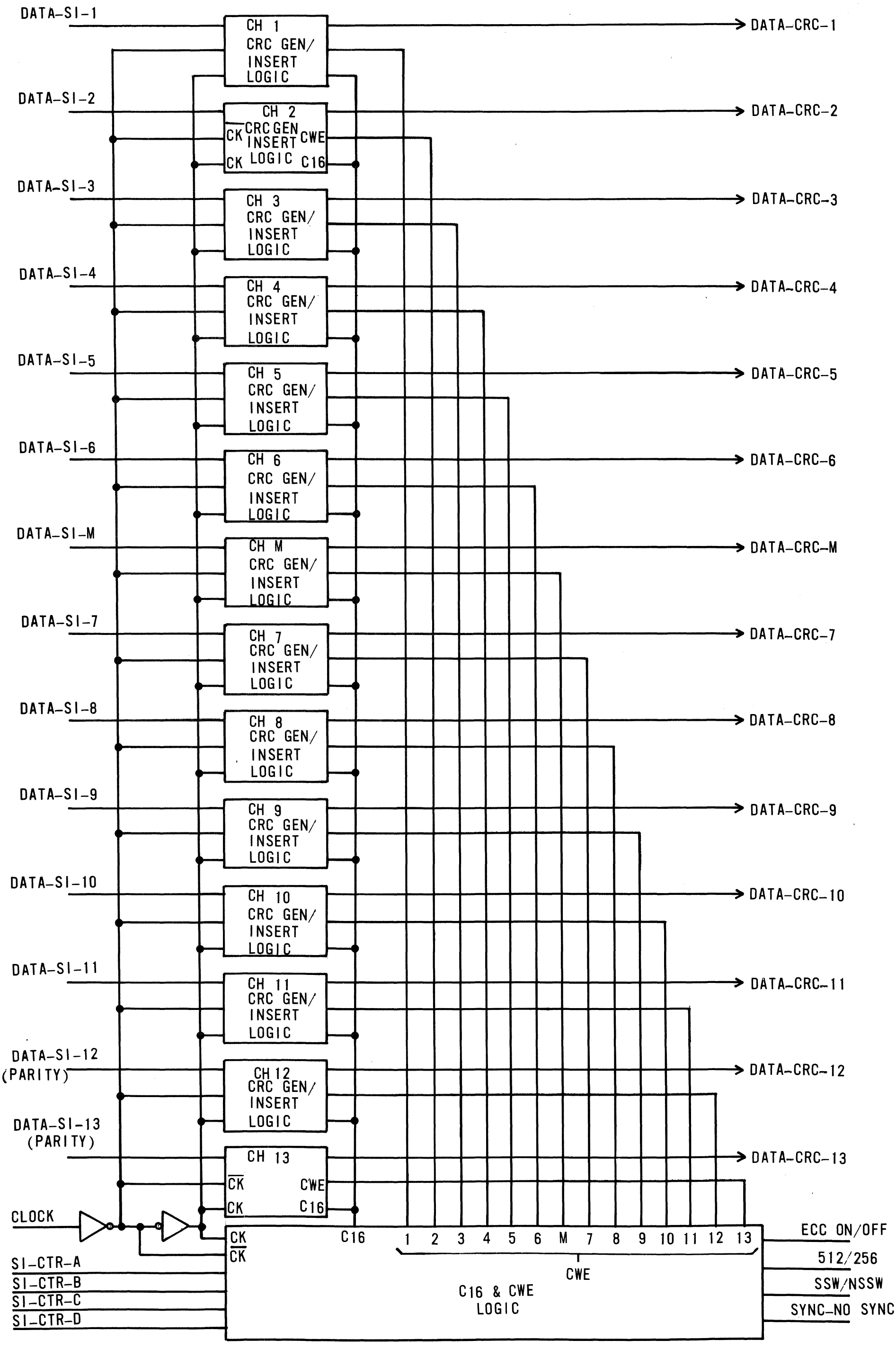
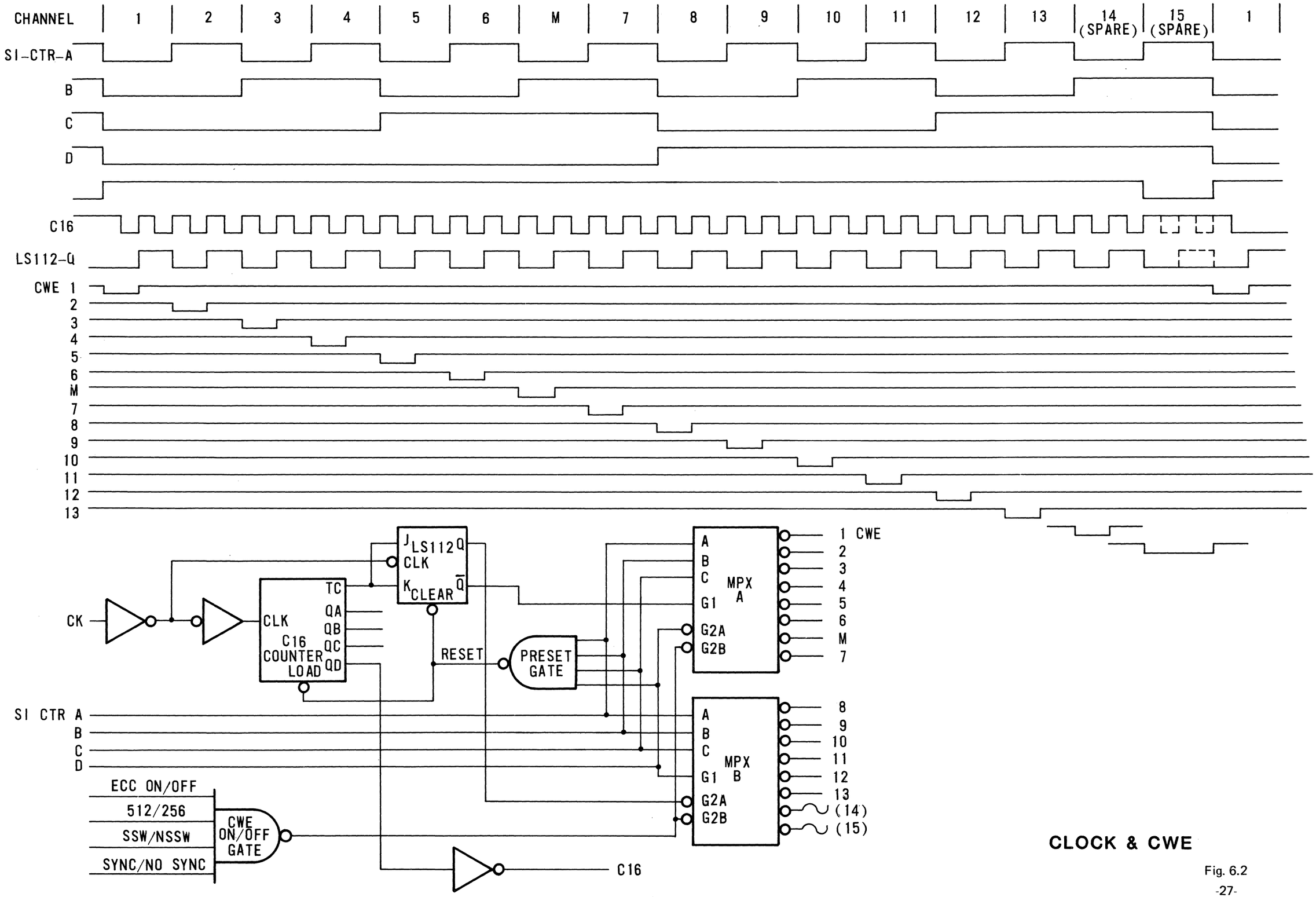


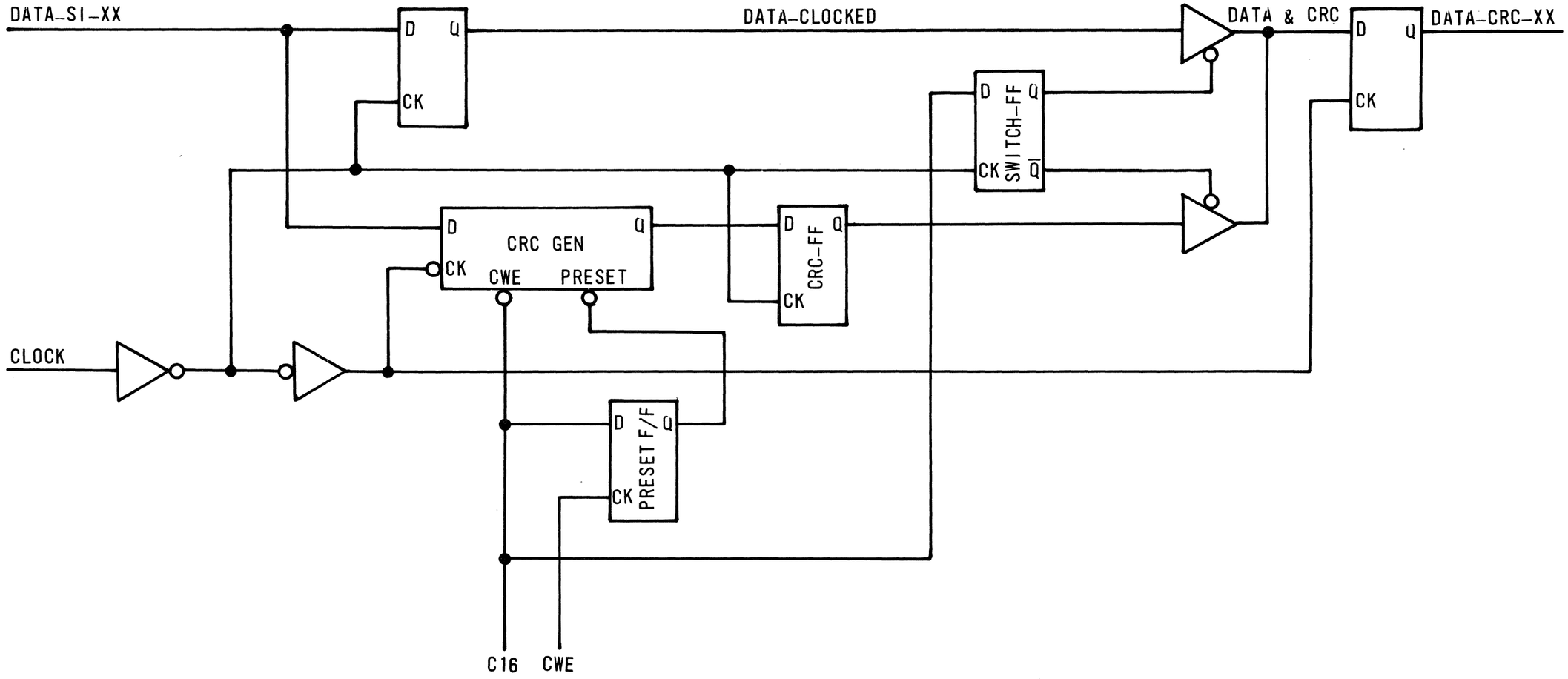
Fig. 6.1

CRC GENERATOR/INSERTER



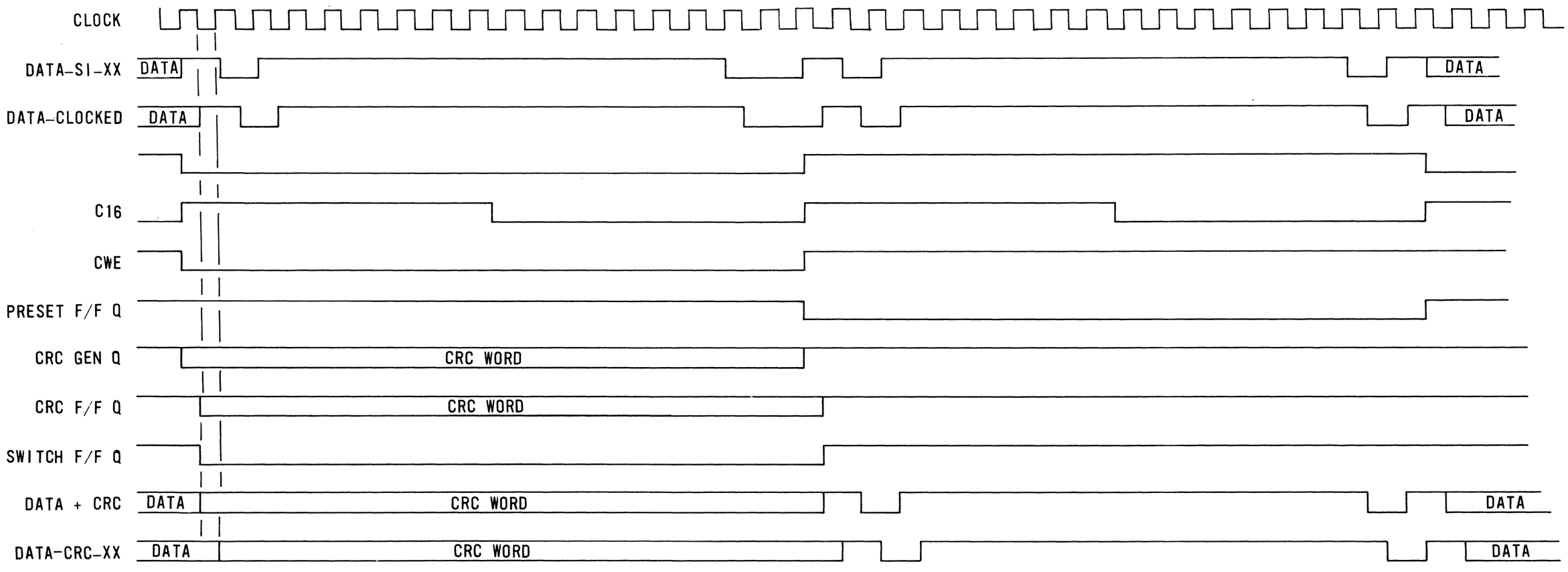
CLOCK & CWE

Fig. 6.2



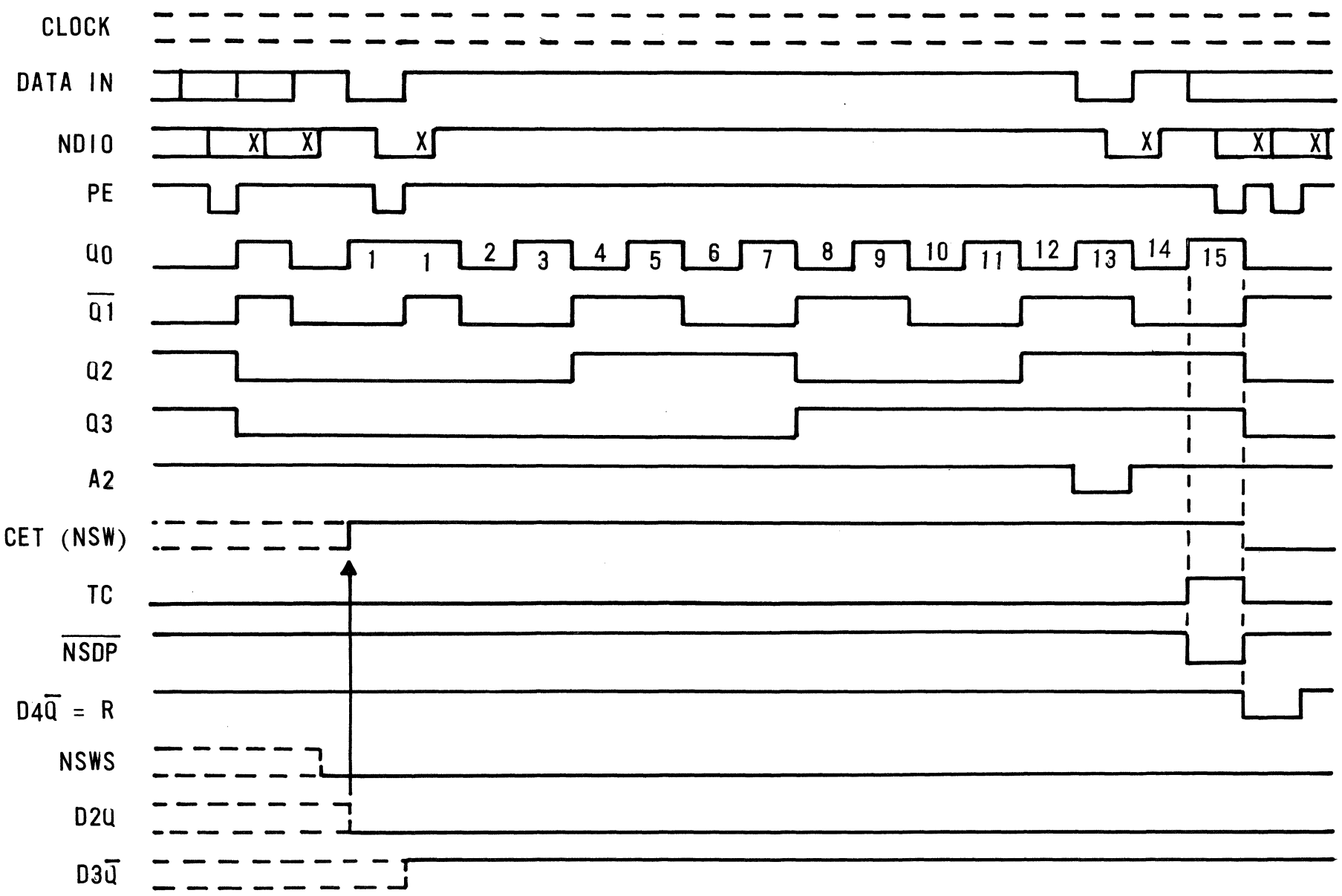
CRC GENERATION AND INSERTION

Fig. 6.3



CRC TIMING

Fig. 6.3A



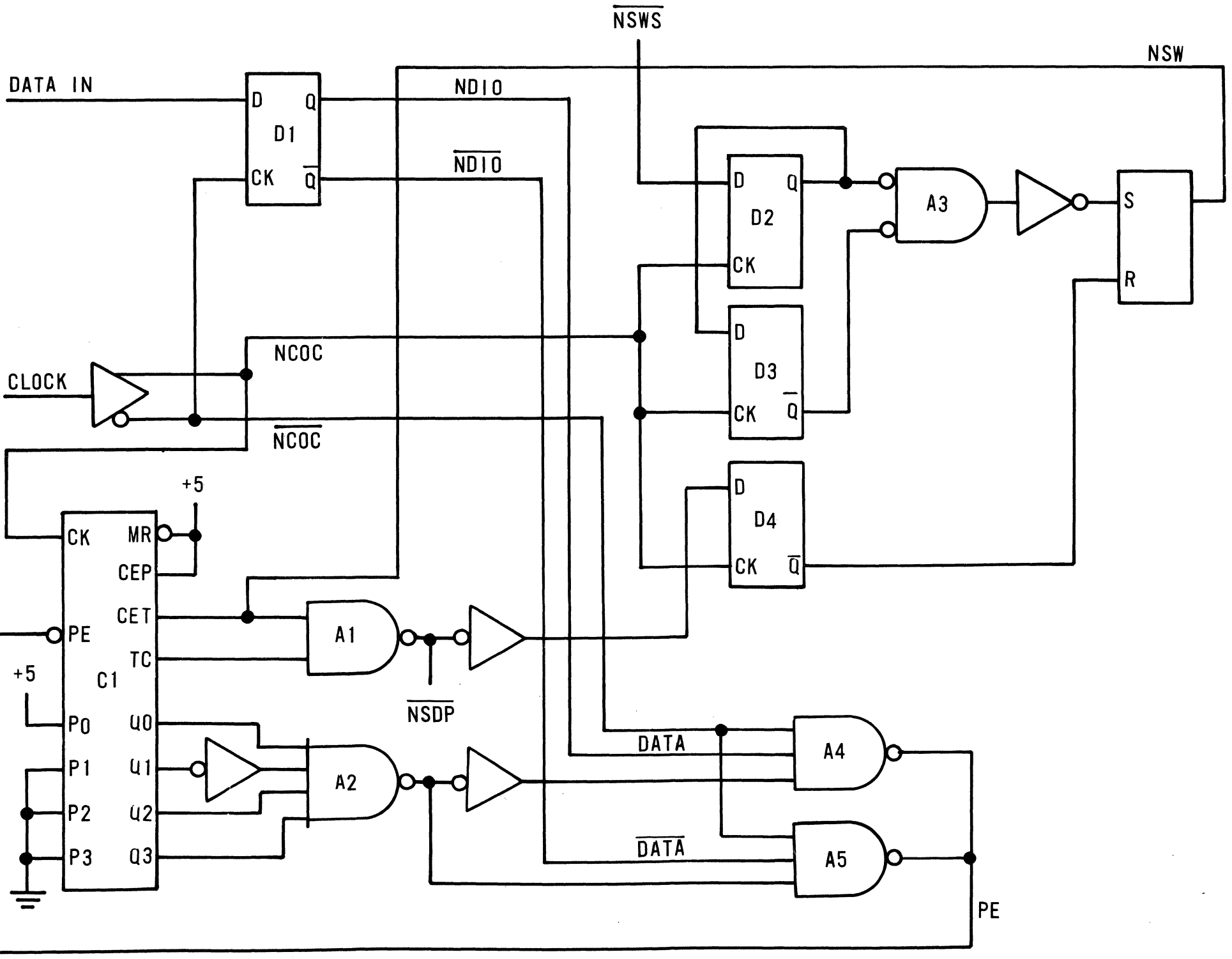
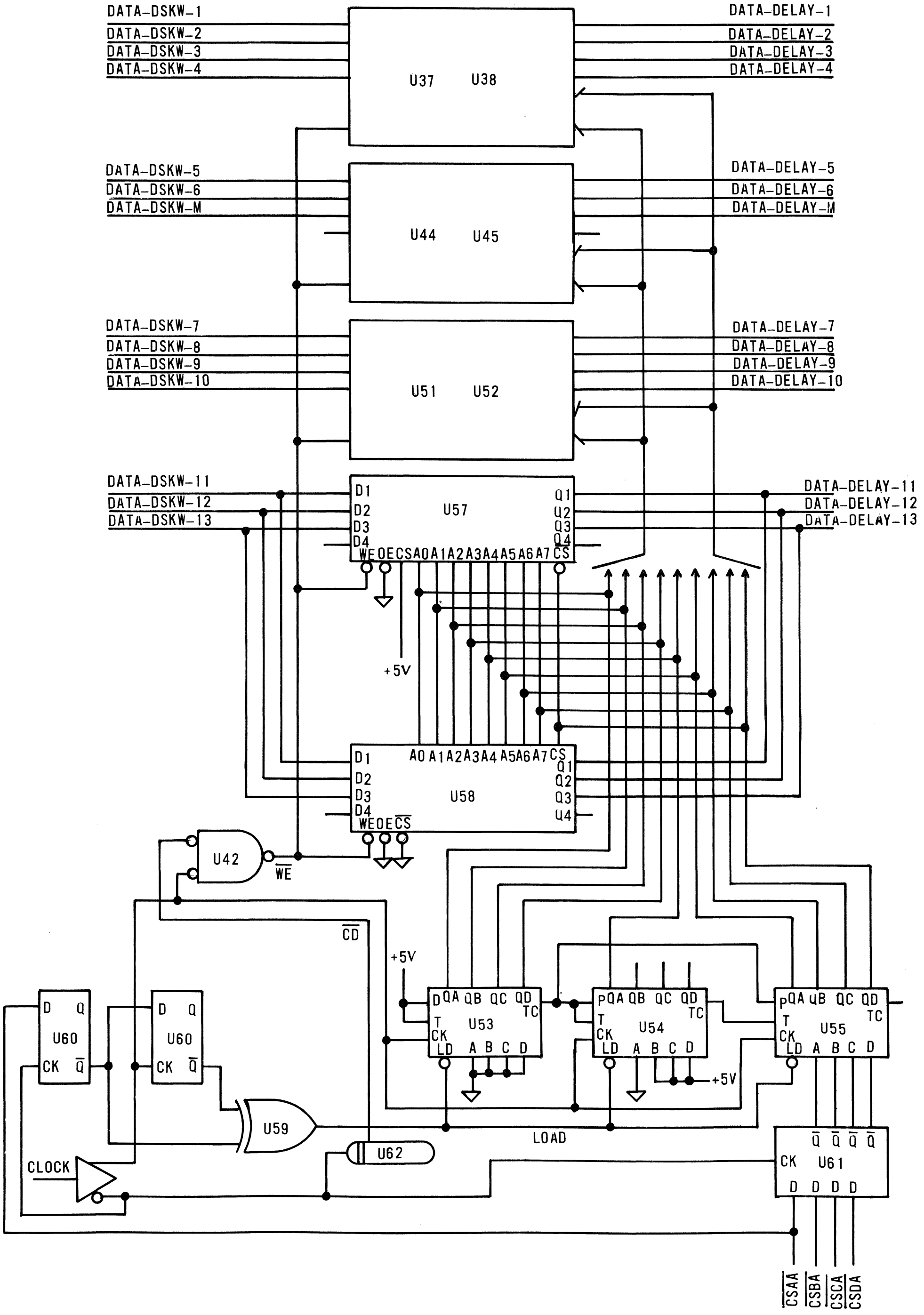


Fig. 7.2

SYNC DETECTION



DATA DELAY

Fig. 10.1

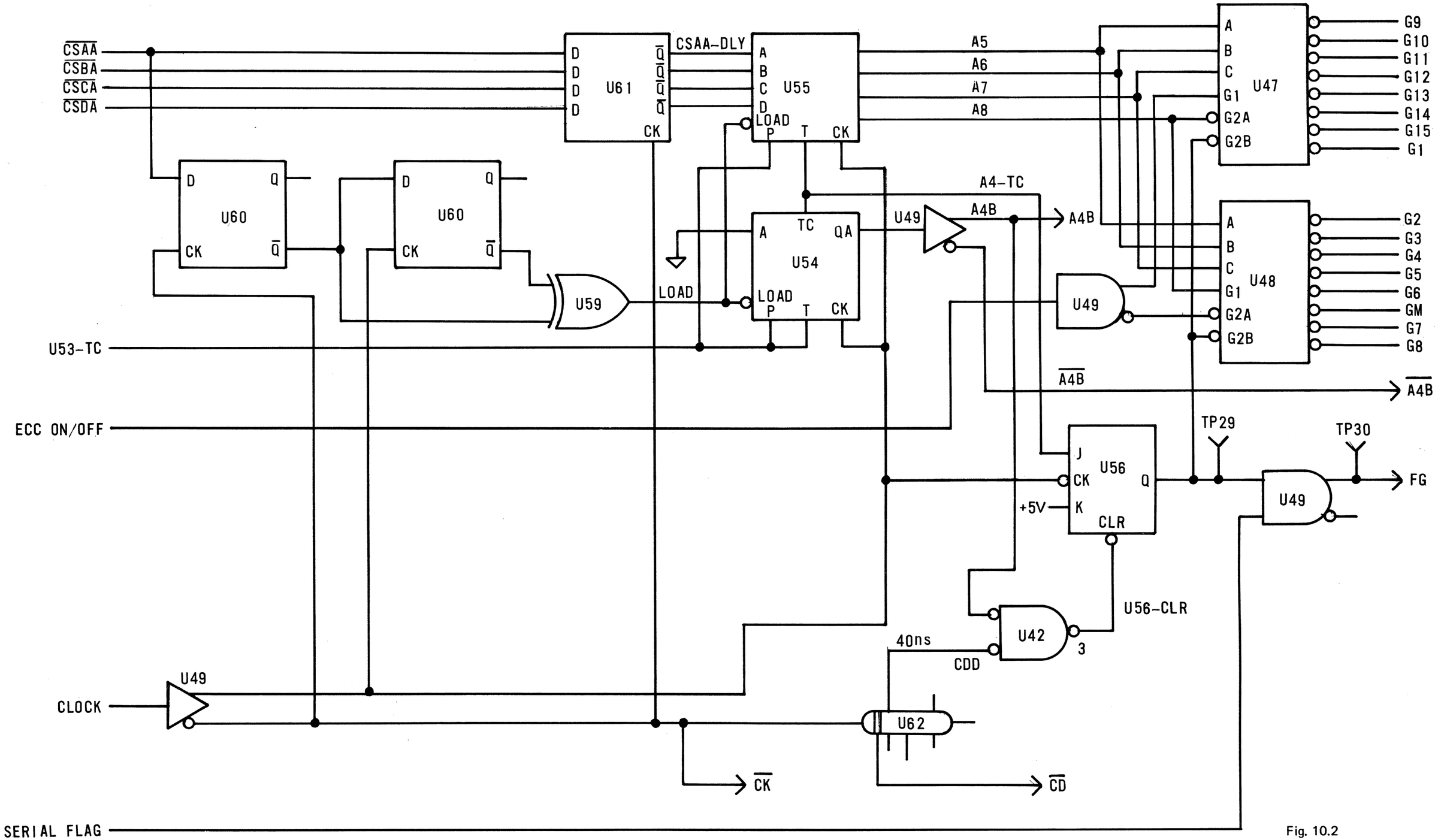


Fig. 10.2

GATE & COUNTER LOGIC

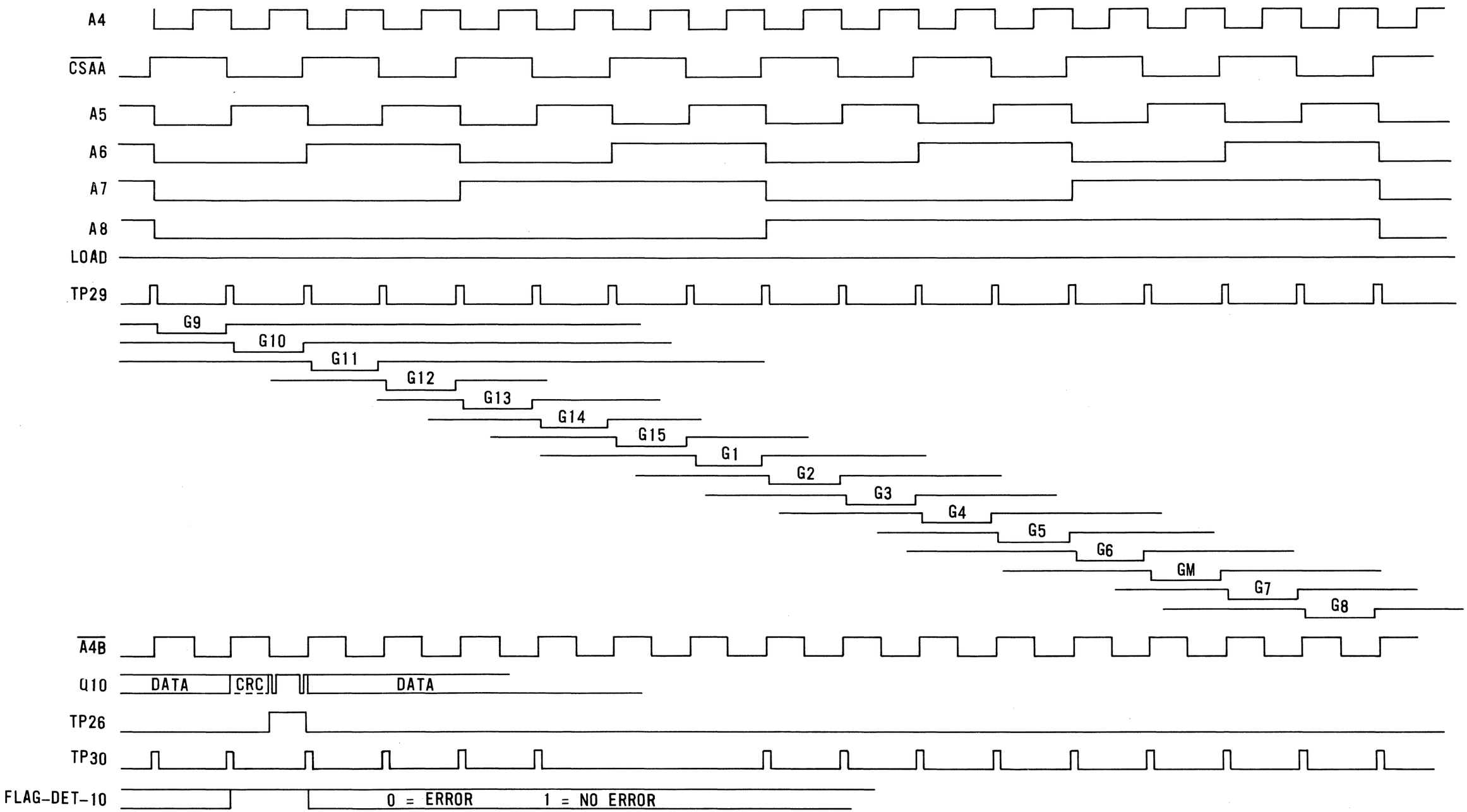


Fig. 10.3

GATE & COUNTER TIMING

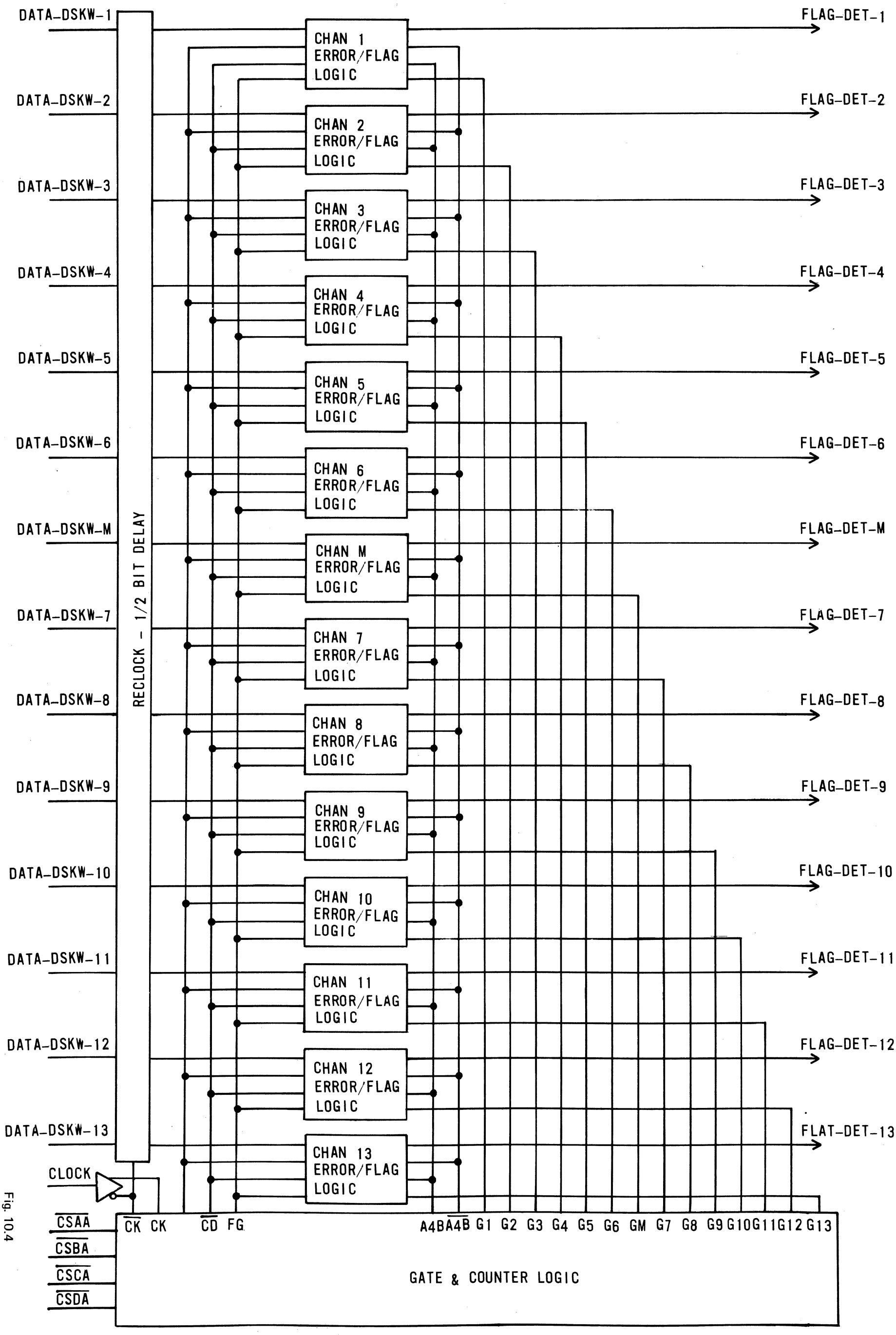
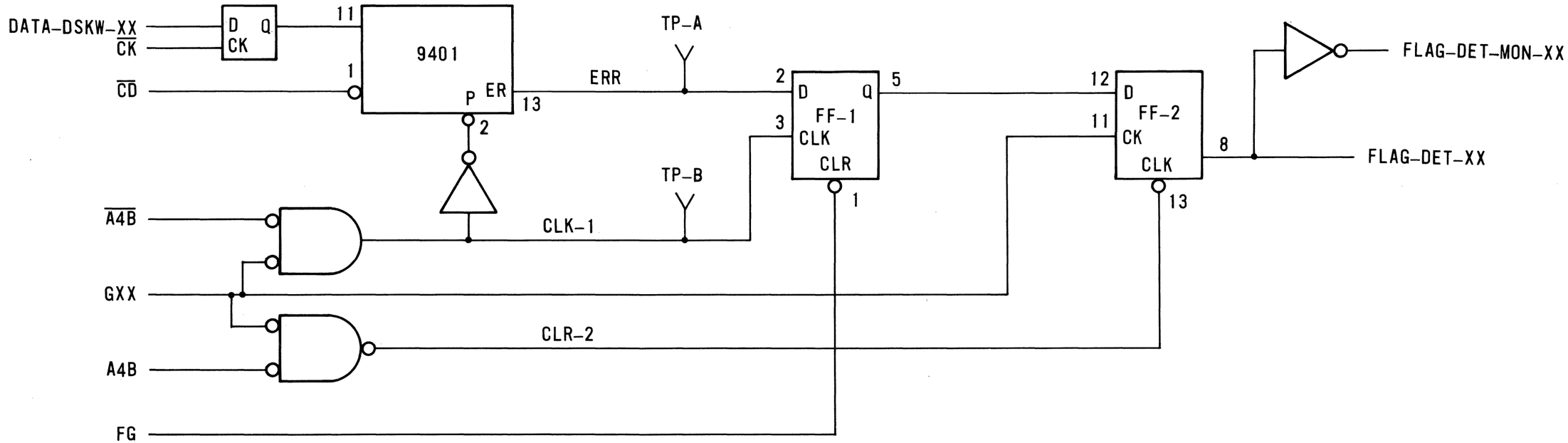


Fig. 10.4

FLAG DETECTION



ERROR FLAG LOGIC

Fig. 10.5

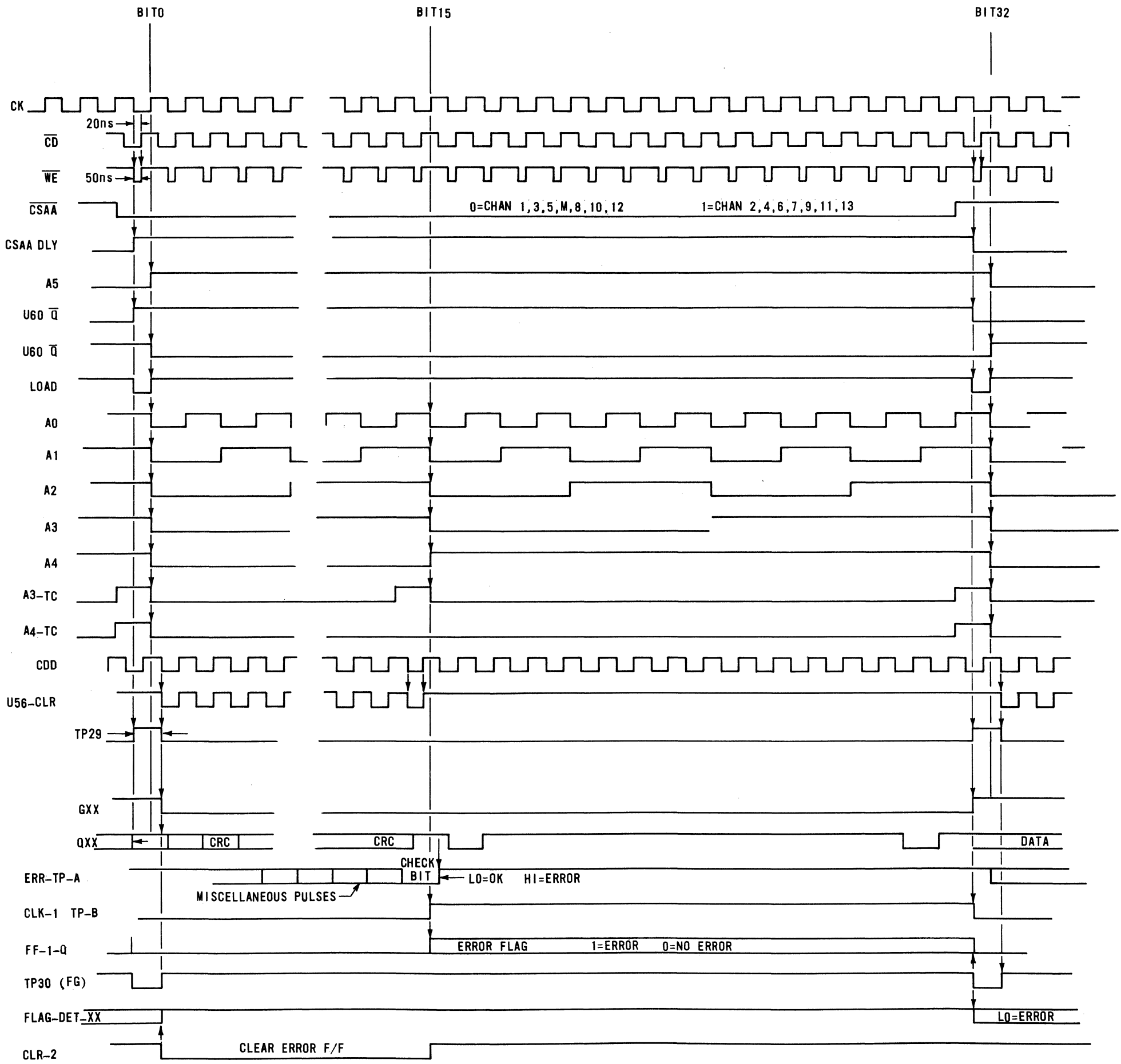


Fig. 10.6

ERROR FLAG TIMING

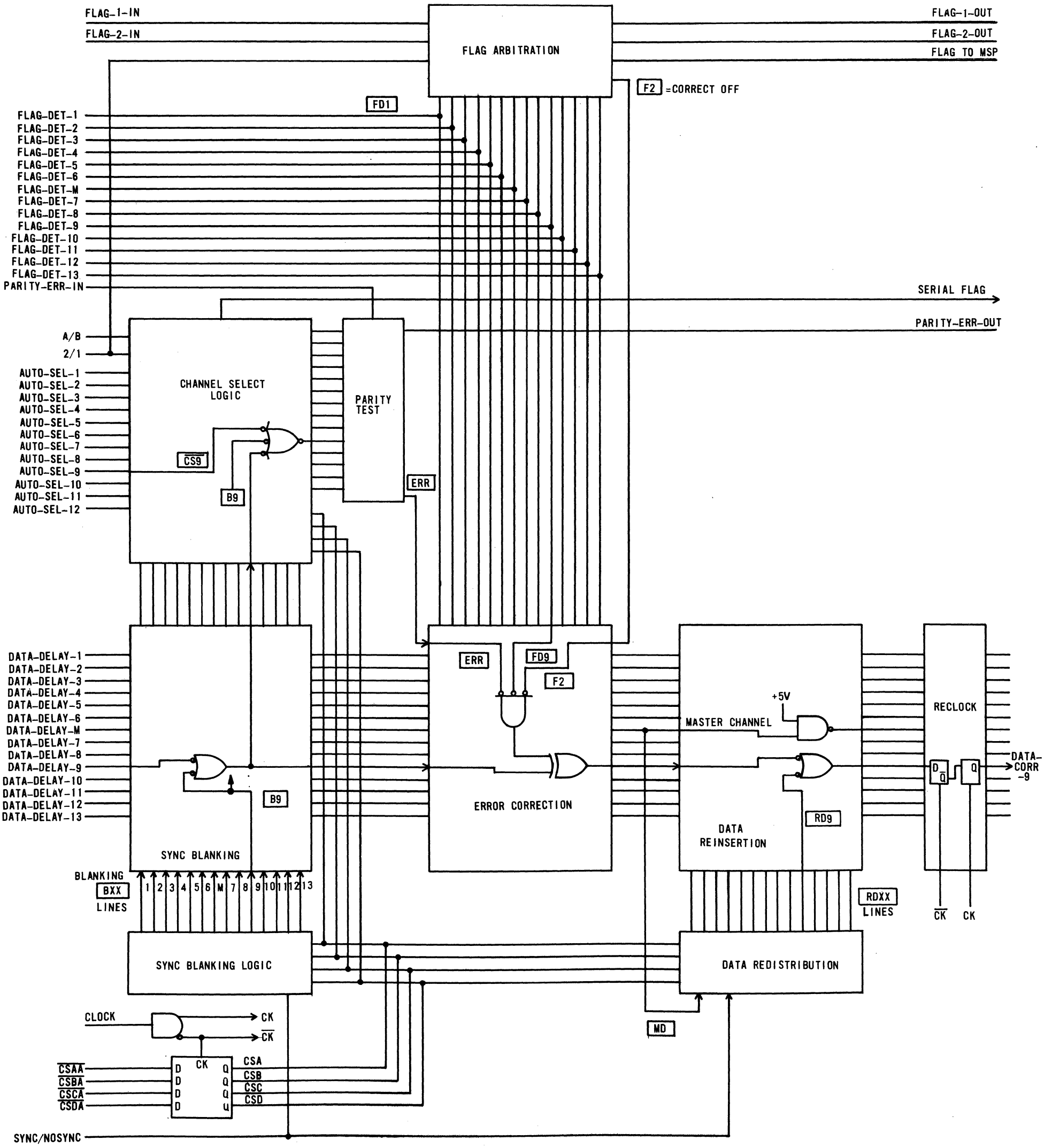
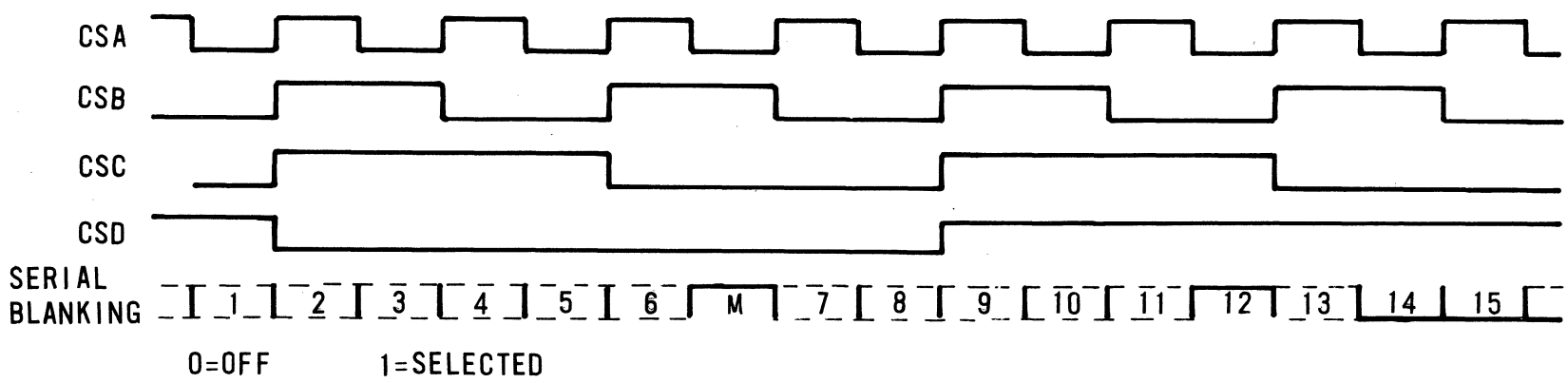


Fig. 11.1

ERROR CORRECTOR



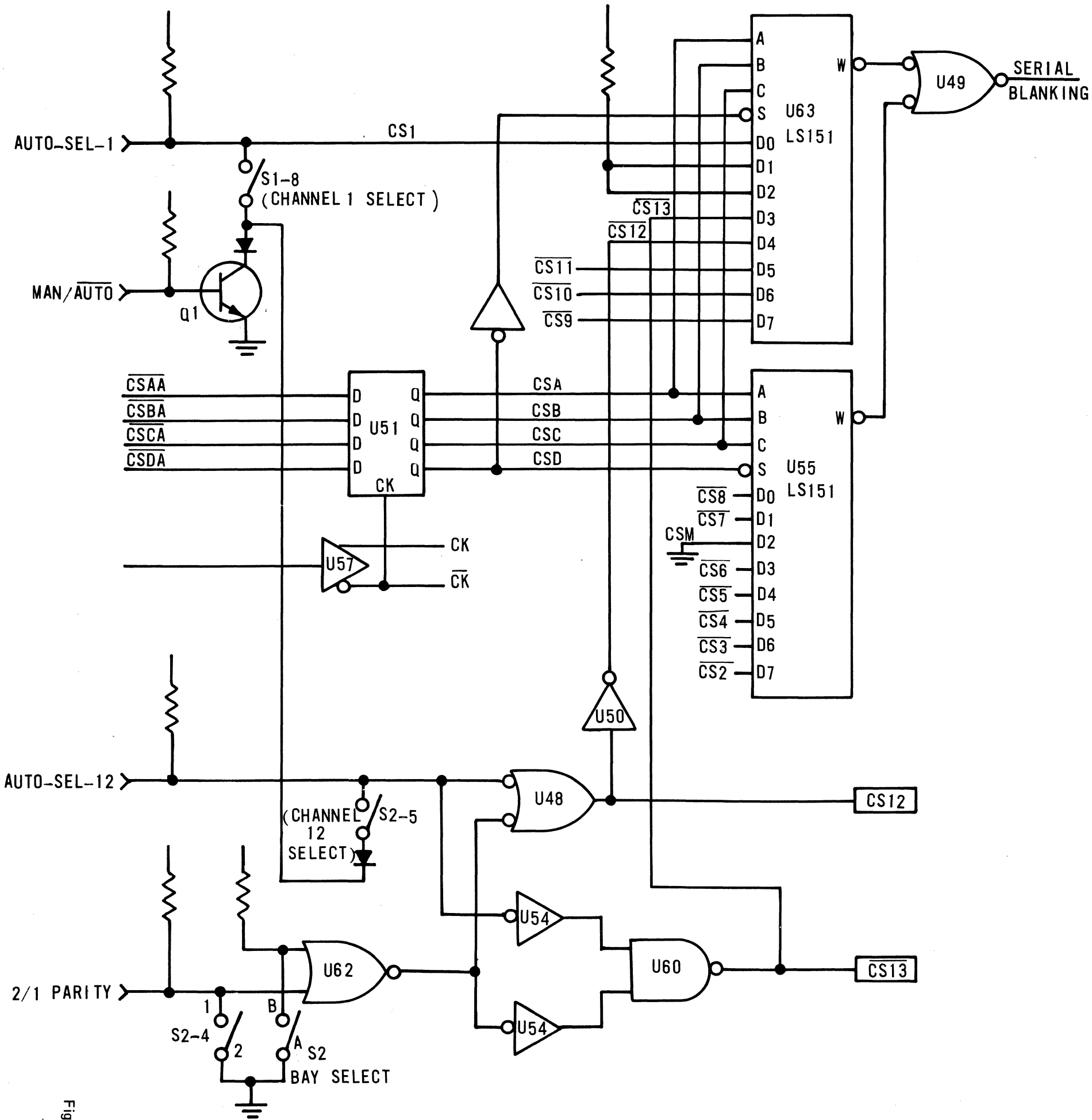


Fig. 11.2

CHANNEL SELECT LOGIC

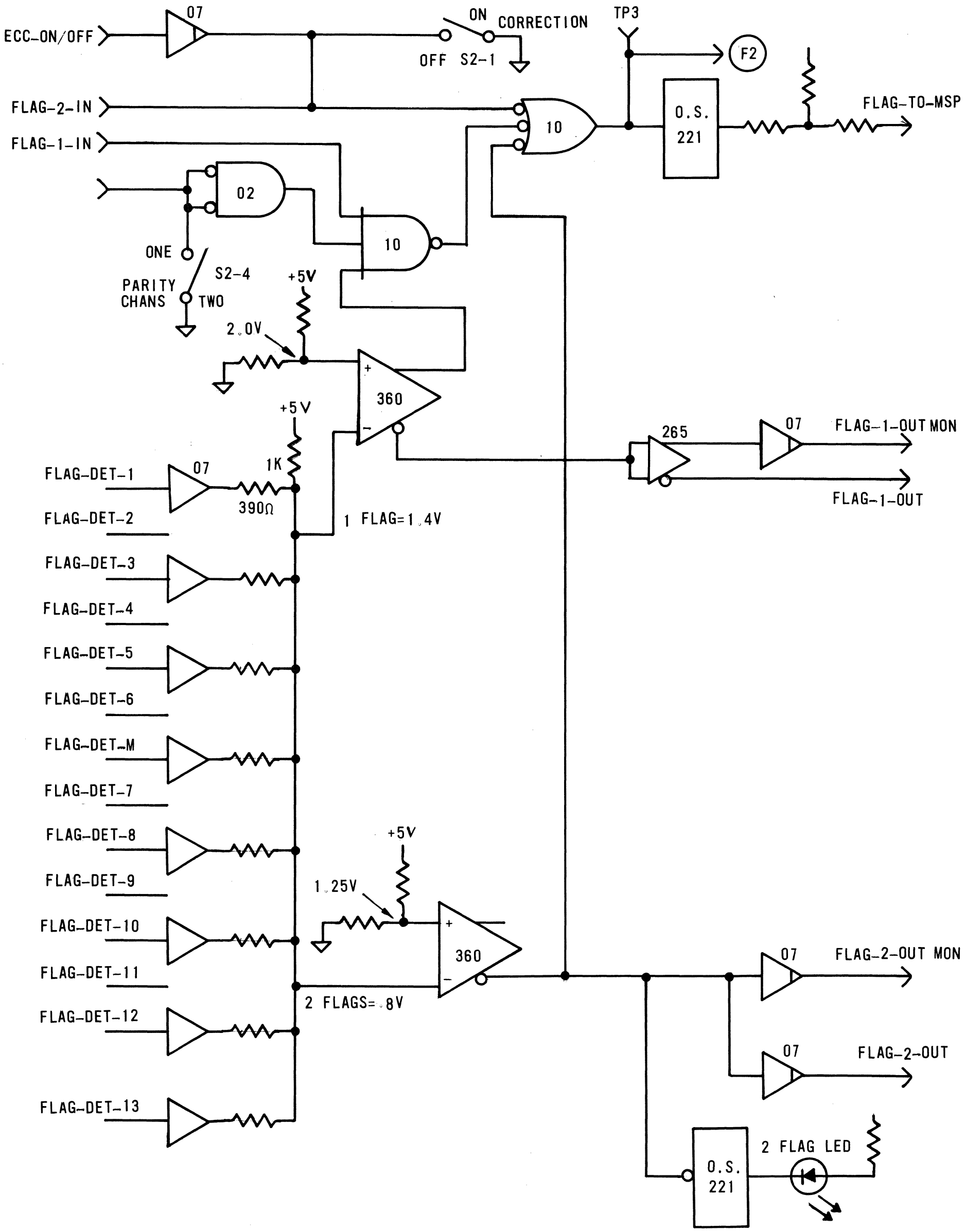
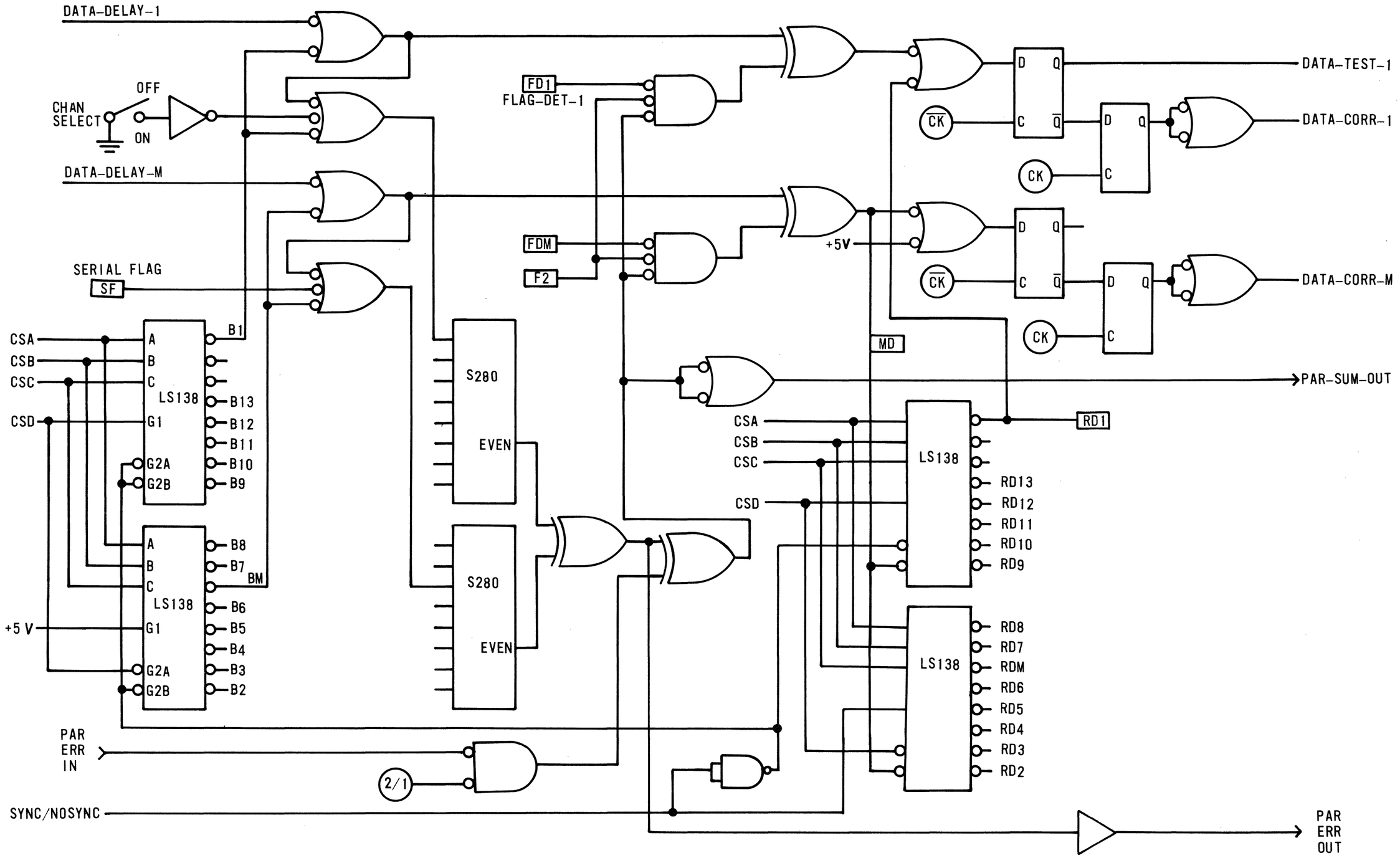


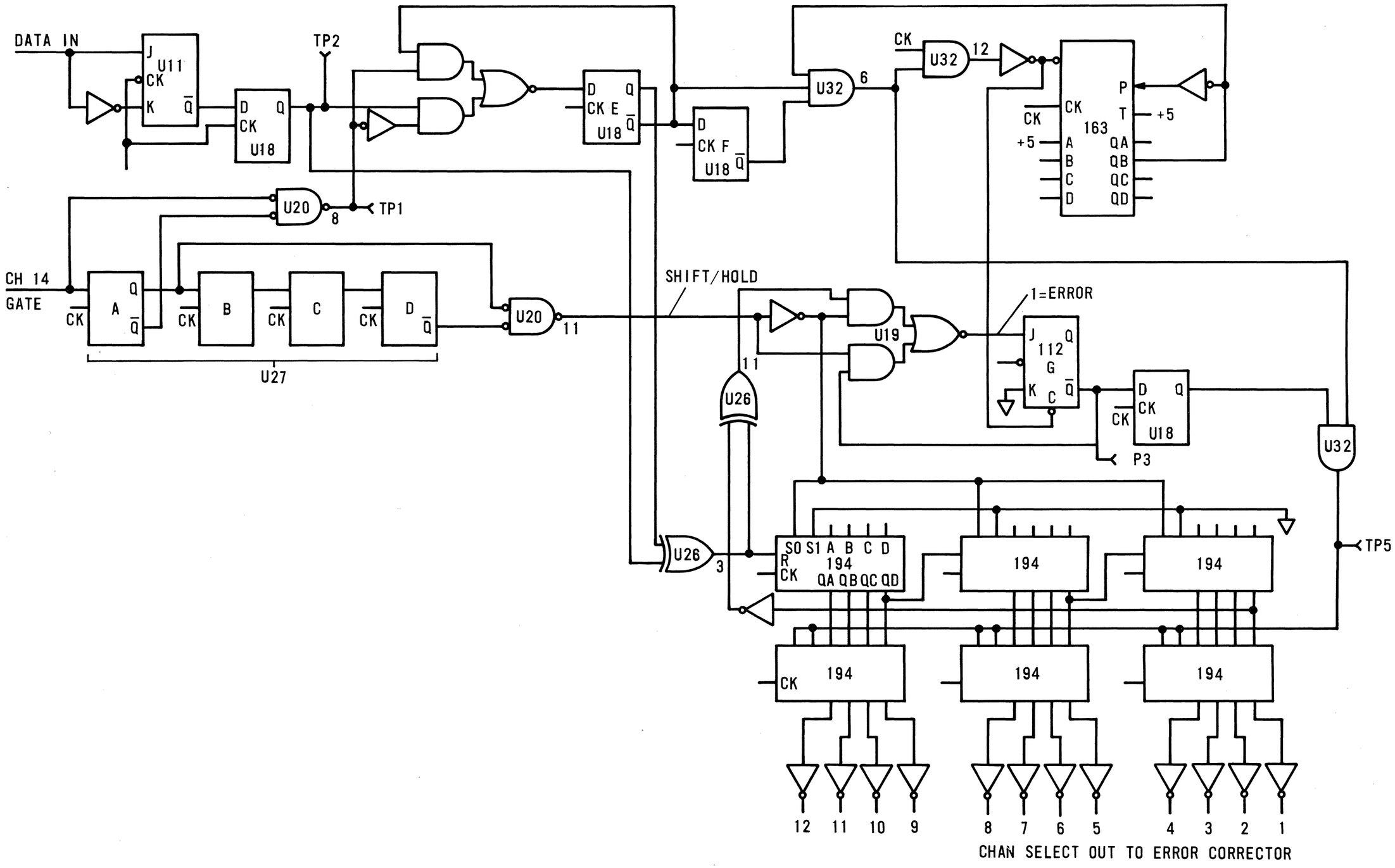
Fig. 11.3

FLAG ARBITRATION



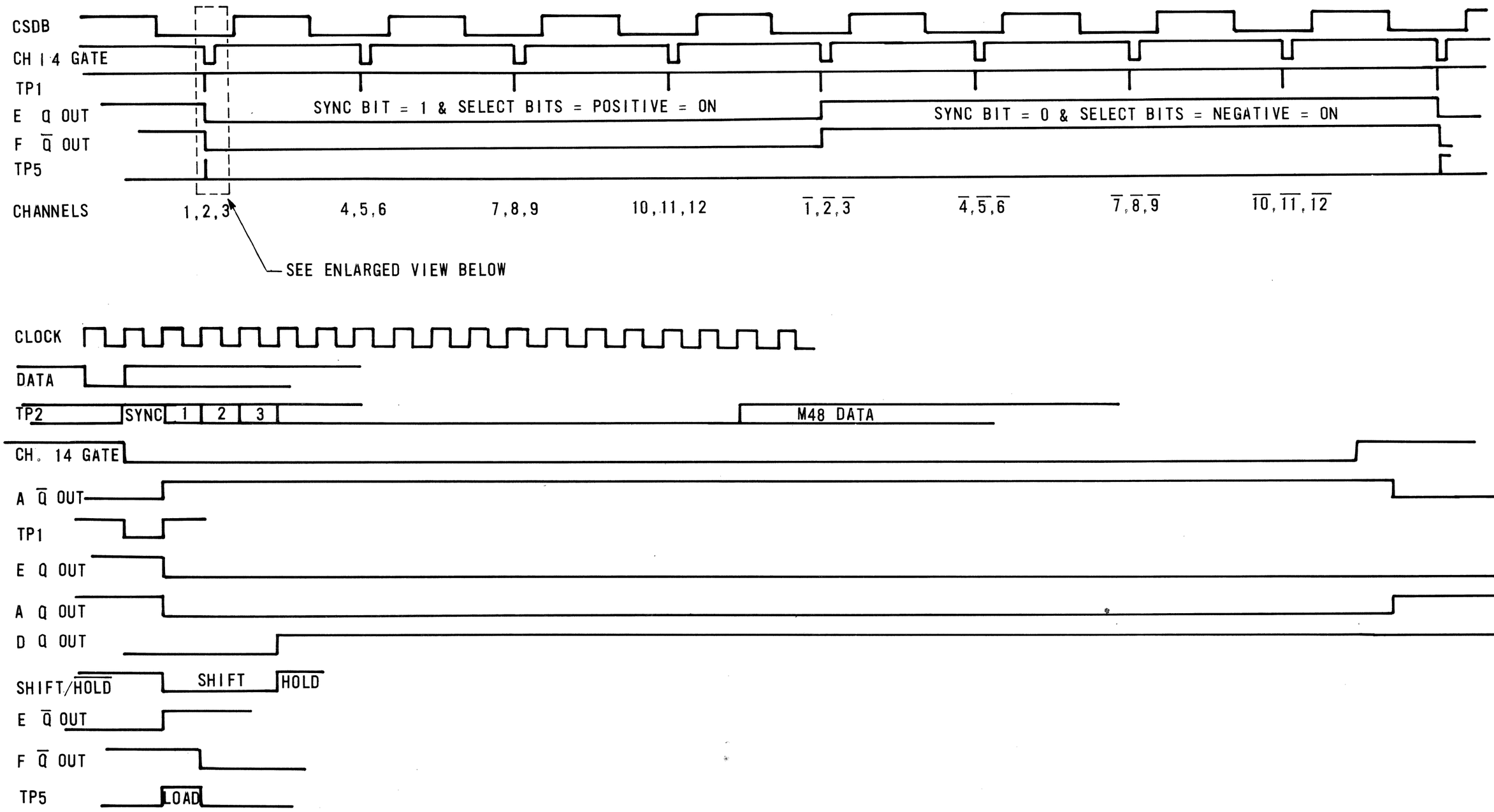
SIGNAL FLOW - CHAN 1 & M

Fig. 11.4



AUTO CHANNEL SELECT LOGIC

Fig. 12.1

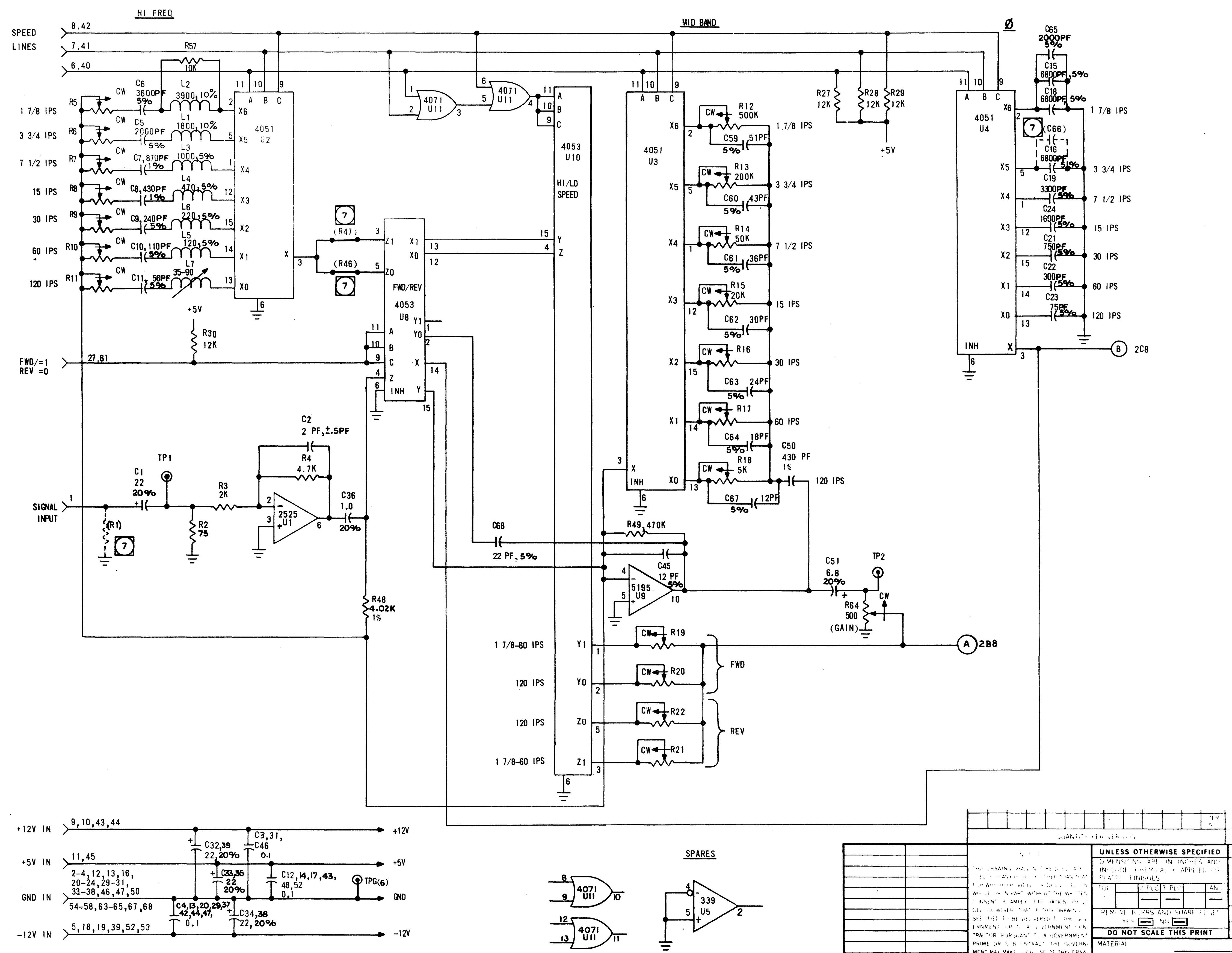


AUTO CHANNEL SELECT TIMING

Fig. 12.2

1257470-01 DISTR CODE: AJ

LTR	ZONE	DESCRIPTION	DFT	CHK	ENGRG
A	—	PROD RLSE	4-17-80	18 Nov 80	3-3-81



REFERENCE DESIGNATIONS	
LAST USED	NOT USED
C70	C66
CR5	
DS4	
L7	
Q6	
R65	R1,46,47
S1	
TP5,TPG	
U11	
E2	

7. C66, R1, 46 & 47 ARE NOT USED ON THIS VERSION.

6. IC POWER PINS ARE: GND=7,8, +5VDC=14,16 EXCEPT FOR:

IC TYPE	GND	+5VDC	+12VDC	-12VDC
2525	–	–	7	4
4051	6,8	16	–	7
339	–	–	3	12
0026	4	6	–	–
72510	1	–	8	4
5195	–	–	11	6

5. VARIABLE RESISTORS ARE 10K, 10%, 3/4W.

4. RESISTORS ARE ±5%, 1/4 WATT.

3. CAPACITORS ARE ±10%, 15 VDC OR GREATER.

2. ELECTRICAL VALUES ARE IN OHMS, MICROFARADS AND MICROHENRIES.

1. REFERENCE ASSEMBLY 1257473.

NOTES: UNLESS OTHERWISE SPECIFIED.

NEXT ASSY	USED ON
1257473	HBR 3000

APPLICATION

UNLESS OTHERWISE SPECIFIED

DO NOT SCALE THIS PRINT

AMPEX HEADQUARTERS Redwood City, California 94063

SCHEMATIC DIAGRAM, 7 SPEED DIRECT REPRODUCE AMPL

SIZE D CODE IDENT NO 92739 1257470-01

SHEET 1 OF 2

REVISIONS					
LTR	ZONE	DESCRIPTION	SIGNATURE AND DATE DFT	CHK	ENGRG
A	—	SEE SHEET ONE	—	—	—

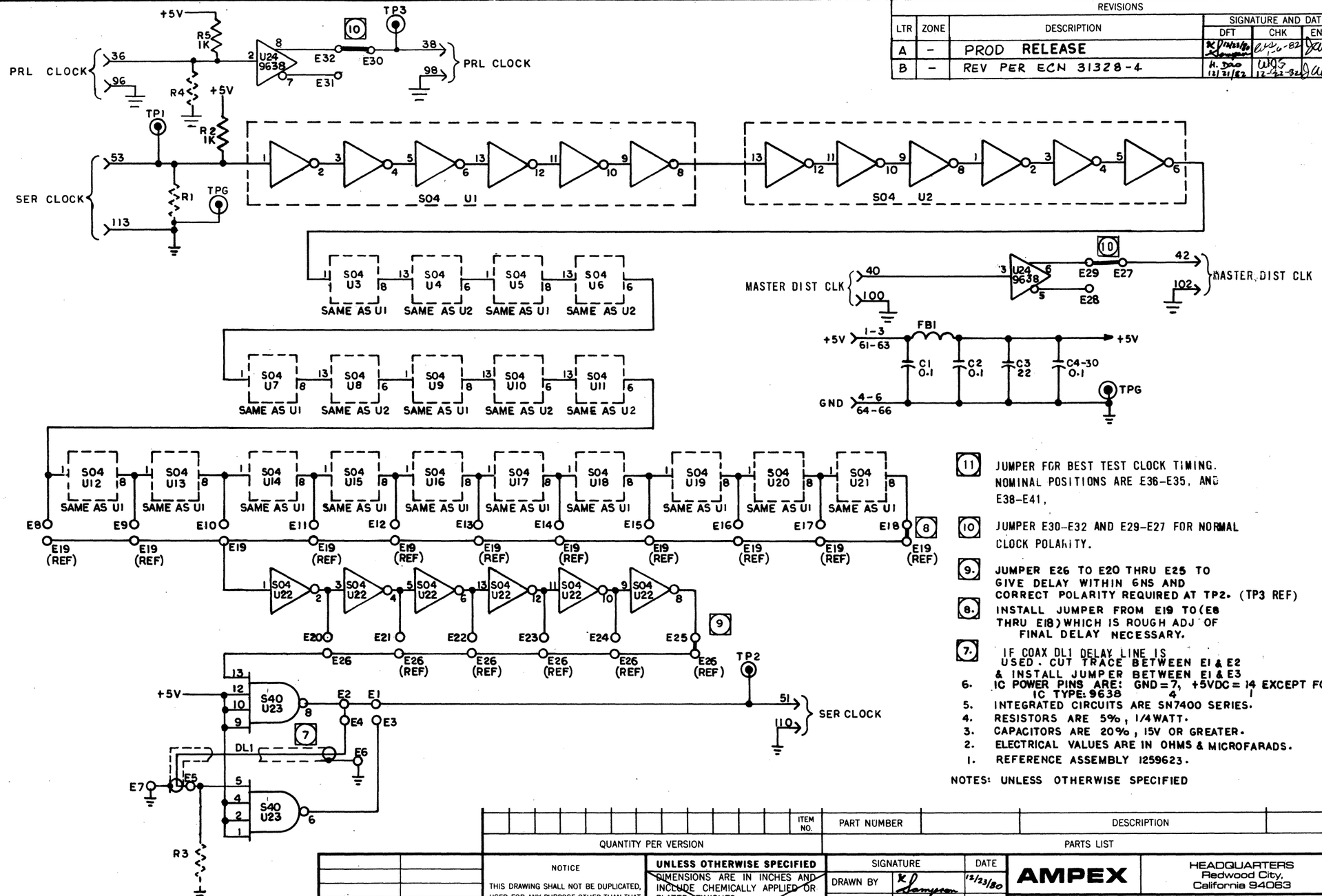
+12V
C57 0.1
R31 2K
R33 240
R32 2K
R34 150
Q1 014-505
Q4 014-505
C26 22 20%
C53 2.2 20%
C25 2 PF ±.5PF
Q2 014-506
Q3 014-506
Q6 014-506
IC3 (B)
R50 91
R51 75
R52 75
CR1 013-599
CR4 013-599
R58 5.1
R59 5.1
R60 3.6K
Q5 014-505
R62 2.4K
R63 150
C54 22 20%
R54 1.82K 1%
C58 0.1
-12V
IB4 (A)
R53 1.91K 1%
R61 75
C55 22 20%
PULSE RESTORER OPTIONAL FOR -02 VERSION
TP5
-01 VERSION
E2 E1
TP4
34 SIGNAL OUTPUT
S1
R56 1.91K 1%
R55 100 1%
C70 82 20%
C41 2.2 20%
+12V
R40 75
R65 620
YEL DS4 132-400
TP3
R43 2K
R42 1K
510 U7
0026 U6
R44 2K
R41 2K
C56 68 20%
C40 .015 20%
R45 1K
C69 2.2 20%
R35 2.4K
CR2 013-599
013-599 CR5
R36 10K
C27 22 20%
R25 5.6K
+R DS1 132-393
HI
R26 2K
339 U5
R24 820
C30 0.1
-R DS3 132-393
LO
CR3 013-599
NORM GRN CTR DS2 132-397
C28 0.1
R23 160
R39 2K
R38 2K
25 NORM LEVEL IND
R37 1.3K
C49 2.2 20%

SIZE	CODE IDENT NO	1257470-01
D	92739	
SCALE —		SHEET 2 OF 2

1257470-01

UC 3504A (Rev. Aug 67) Printed in U.S.A.

REVISIONS					
LTR	ZONE	DESCRIPTION	SIGNATURE AND DATE DFT	CHK	ENGRG
A	-	PROD RELEASE	K Simpson	1-6-82	1-7-82
B	-	REV PER ECN 31328-4	H. Dao 12/21/82	WJS 12-23-82	1-7-83



11. JUMPER FOR BEST TEST CLOCK TIMING. NOMINAL POSITIONS ARE E36-E35, AND E38-E41.

10. JUMPER E30-E32 AND E29-E27 FOR NORMAL CLOCK POLARITY.

9. JUMPER E26 TO E20 THRU E25 TO GIVE DELAY WITHIN 6NS AND CORRECT POLARITY REQUIRED AT TP2. (TP3 REF)

8. INSTALL JUMPER FROM E19 TO(E8 THRU E18)WHICH IS ROUGH ADJ OF FINAL DELAY NECESSARY.

7. IF COAX DL1 DELAY LINE IS USED. CUT TRACE BETWEEN E1 & E2 & INSTALL JUMPER BETWEEN E1 & E3

6. IC POWER PINS ARE: GND=7, +5VDC=14 EXCEPT FOR: IC TYPE: 9638 4 1

5. INTEGRATED CIRCUITS ARE SN7400 SERIES.

4. RESISTORS ARE 5%, 1/4WATT.

3. CAPACITORS ARE 20%, 15V OR GREATER.

2. ELECTRICAL VALUES ARE IN OHMS & MICROFARADS.

1. REFERENCE ASSEMBLY 1259623.

NOTES: UNLESS OTHERWISE SPECIFIED

ITEM NO.	PART NUMBER	DESCRIPTION
QUANTITY PER VERSION	PARTS LIST	

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES.
TOL ± | 2 PLC | 3 PLC | ANG
REMOVE BURRS AND SHARP EDGES YES ☐ NO ☐
DO NOT SCALE THIS PRINT

	SIGNATURE	DATE
DRAWN BY	K Simpson	12/23/80
CHK BY	D Ulmer	1-6-82
DFT APPD		
ENGRG APPD	J Aiken	1.7.82
AUTH BY	W. A. V...	7 Jan 82

MATERIAL:
FINISH:

1259623	HBR3000
NEXT ASSY	USED ON
APPLICATION	

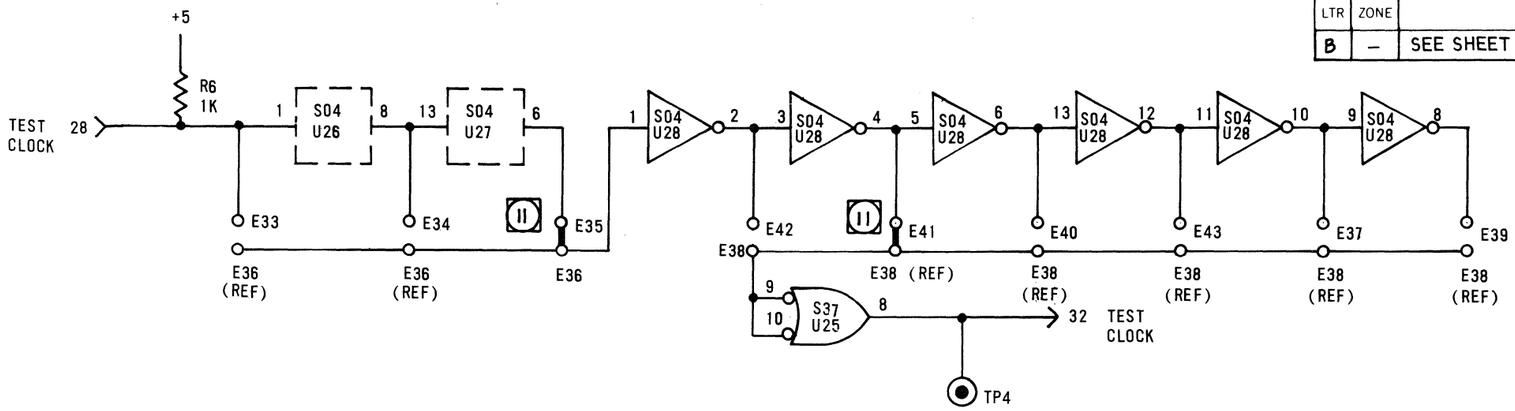
AMPEX
HEADQUARTERS
Redwood City,
California 94063

SCHEMATIC DIAGRAM
DELAY LINE

SIZE	CODE IDENT NO.	
C	92739	1259620-01
SCALE —		SHEET / OF 2

1259620-01

REVISIONS					
LTR	ZONE	DESCRIPTION	SIGNATURE AND DATE		
			DFT	CHK	ENGRG
B	–	SEE SHEET ONE	–	–	–



1259620-01

SIZE	CODE IDENT NO.	
C	92739	1259620-01
SCALE —		SHEET 2 OF 2

UC-3503A (Rev Aug 67) Printed in U.S.A.

			SIGNATURE AND DATE		
			ORIG	CHKD	ENGRG
A	-	REV PER ECR 29781-4 PRODUCTION RELEASE	CFH 7-31-81	MD 7-31-81	H Dodd 7-31-81
B	-	REV PER ECN 30095-2	H. Sano 10-2-81	[illegible] 10-13-81	H Dodd 10-23-81

CH 6 DATA IN 17
CH 5 DATA IN 16
CH 4 DATA IN 15
CH 3 DATA IN 14
CH 2 DATA IN 13
CH 1 DATA IN 12

CH 1 U6 1255975-01
CH 2 U5 1255975-01
CH 3 U4 1255975-01
CH 4 U3 1255975-01
CH 5 U11 1255975-01
CH 6 U10 1255975-01

E-E CMD 11 — 13 Q4 U1 — 12
9
10

R10 1K
R7 1K
R9 1K
R11 1K
+5V

S1 (1 2 3 4)

L IC1 — M IC1 — U7 330 — TP1
J IC1 — K IC1 — U7 330 — TP2
G IC1 — H IC1 — U7 330 — TP3
E IC1 — F IC1 — U7 330 — TP4
C IC1 — D IC1 — U12 330 — TP5
A IC1 — B IC1 — U12 330 — TP6
U13 1K, +5V

2 2C1, 3C8
GND 2C1, 3C8
3 2C1, 3C8
4 2C1, 3C8
6 2C1, 3C8
1 2C1, 3C8

50 DATA OUT
34 CAL OUT
} CH 6
49 DATA OUT
33 CAL OUT
} CH 5
48 DATA OUT
32 CAL OUT
} CH 4
47 DATA OUT
30 CAL OUT
} CH 3
46 DATA OUT
29 CAL OUT
} CH 2
45 DATA OUT
28 CAL OUT
} CH 1

5 2C2, 3C8
8 2C2
9 GLITCH 2A8, 3B7
10 REC 2A8, 3B7

S174 U20: IC2 (A 3) IC3 (C 4) IC4 (E 6) IC5 (G 11) IC6 (J 13) IC7 (L 14); CK 9, CLR 1; Q 2, 5, 7, 10, 12, 15 → B IC2, D IC3, F IC4, H IC5, K IC6, M IC7

CLK IN 8 — C8 2.2 20% — R3 1K — R1 100K — R2 1K — 760 U2 — TPCLK
C10 51 PF 5%, R6 1K, C9 .01, R5 1K, R4 1.5K, C12 .01, R8 1.5K, R12 CW 1K
+5V, U13 1K
04 U1: 5→6, 11→10, 9→8

R13 1K — S86 U24 ×4

-5 VDC 31
-5 VDC 91
+5V — R14 1K
REC COMMAND 59 — 04 U1: 1→2, 3→4

FB1
+5V — 1-3,61-63 — C2 .01 — C1 33 — C3,4,6,11,13-32 .01 — TP 15
GND 4-6,64-66, 68-90,92-120

5. INTEGRATED CIRCUITS ARE SN 5400 SERIES, EXCEPT FOR:
HYBRID 1255975-01
760
4. RESISTORS ARE ±5%, 1/4 WATT.
3. CAPACITOR VALUES ARE ±10%, 10 VDC OR GREATER.
2. ELECTRICAL VALUES ARE IN OHMS & MICROFARADS.
1. REFERENCE ASSEMBLY 1259673-01.
NOTES: UNLESS OTHERWISE SPECIFIED

6. IC POWER PINS ARE: GND=7, +5VDC=14, EXCEPT FOR

	GND	+5VDC
760	5	8
1255975-01	12	24
S174	16	8

REF DESIGNATIONS	
LAST USED	NOT USED
C32	C5,7
FB1	
R13	
S1	
TP15, TPCLK	
U23	

CAT. ITEM	NEXT ASSY	USED ON	IN	MF	PR
	1259673	HBR3000			
APPLICATION			CODE		

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES
TOL ± | 2 PLC | 3 PLC | ANG
REMOVE BURRS AND SHARP EDGES YES ☐ NO ☐
DO NOT SCALE THIS PRINT

SIGNATURE	DATE
DRAWN BY	12/29/80
CHK BY	
DFT APPD	
ENGRG APPD	
AUTH BY	

MATERIAL
FINISH

AMPEX HEADQUARTERS Redwood City, California 94063

SCHEMATIC DIAGRAM
ENCODER NO. 1

SIZE D | CODE IDENT NO 92739 | 1259670-01
SCALE — | SHEET 1 OF 3

UC-3504.03 (3.74) PRINTED IN U.S.A.

LTR	ZONE	REVISIONS	SIGNATURE AND DATE		
			CHK	APPV	ENGRG
B	—	SEE SH 1	—	—	—

CH 11 DATA IN 23
CH 10 DATA IN 22
CH 9 DATA IN 21
CH 8 DATA IN 20
CH 7 DATA IN 19
CH M DATA IN 18

CH M U9 1255975-01
CH 7 U8 1255975-01
CH 8 U17 1255975-01
CH 9 U16 1255975-01
CH 10 U15 1255975-01
CH 11 U14 1255975-01

(5) 1B2, 3C8
(8) 1B2
(1) 1D2, 3C8
(6) 1C2, 3C8
(4) 1C2, 3C8
(3) 1C2, 3C8
GND 1C2, 3C8
(2) 1C2, 3C8

(Z) 2B8
(X) 2B8
(V) 2B8
(T) 2B8
(R) 2B8
(N) 2C8

2B8 (AA) U12 330 TP7
2B8 (Y) U12 330 TP8
2B8 (W) U18 330 TP9
2B8 (U) U18 330 TP10
2B8 (S) U18 330 TP11
2C8 (P) U18 330 TP12

+5V U13 1K

2C2 (N) 6 D Q 7 (P) 2B2
2C3 (R) 4 D Q 5 (S) 2B3
2C4 (T) 3 D Q 2 (U) 2B4
2C5 (V) 11 D Q 10 (W) 2B5
2C5 (X) 13 D Q 12 (Y) 2B5
2C6 (Z) 14 D Q 15 (AA) 2B6
5174 U19
CK 9 CLR 1

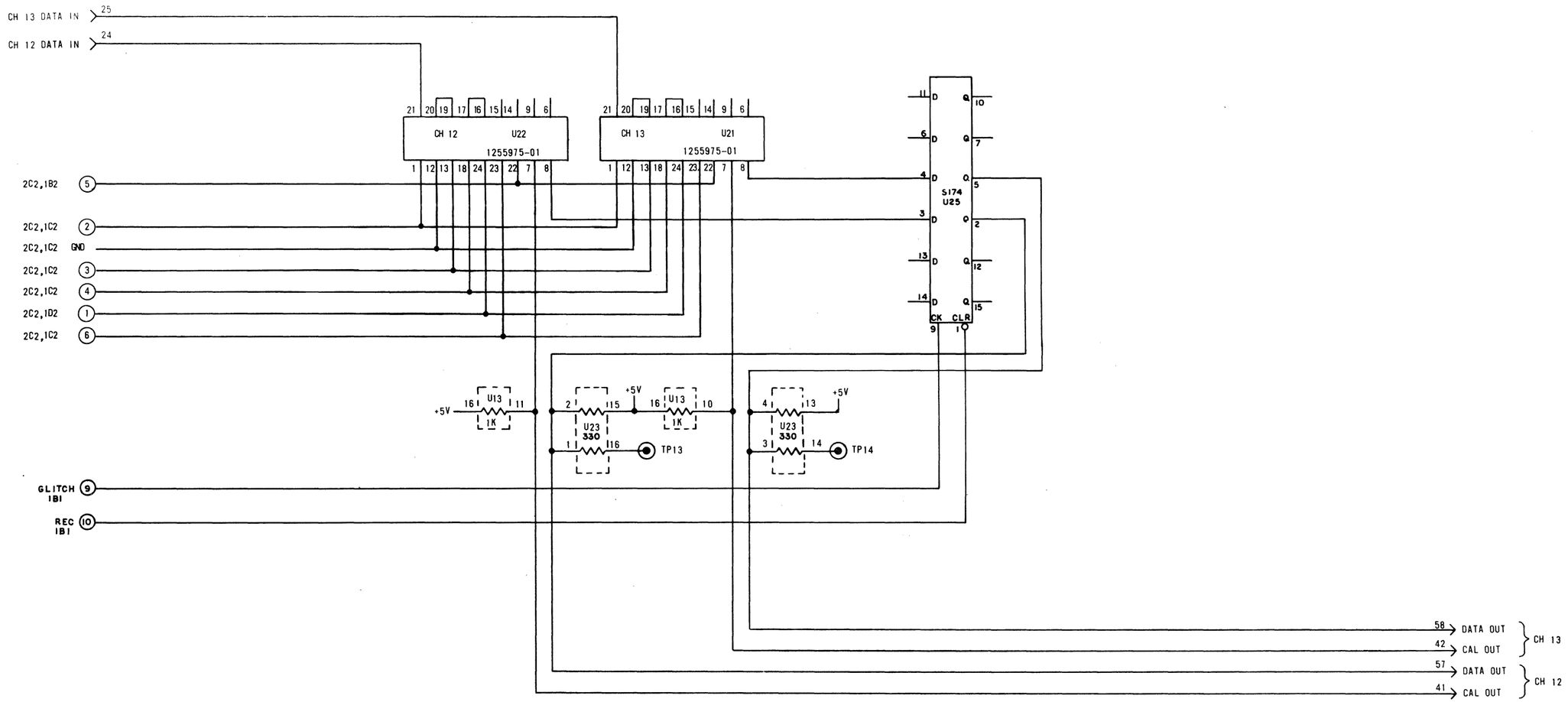
GLITCH (9) 1B1
REC (10) 1B1

56 DATA OUT
40 CAL OUT
CH 11
55 DATA OUT
39 CAL OUT
CH 10
54 DATA OUT
38 CAL OUT
CH 9
53 DATA OUT
37 CAL OUT
CH 8
52 DATA OUT
36 CAL OUT
CH 7
51 DATA OUT
35 CAL OUT
CH M

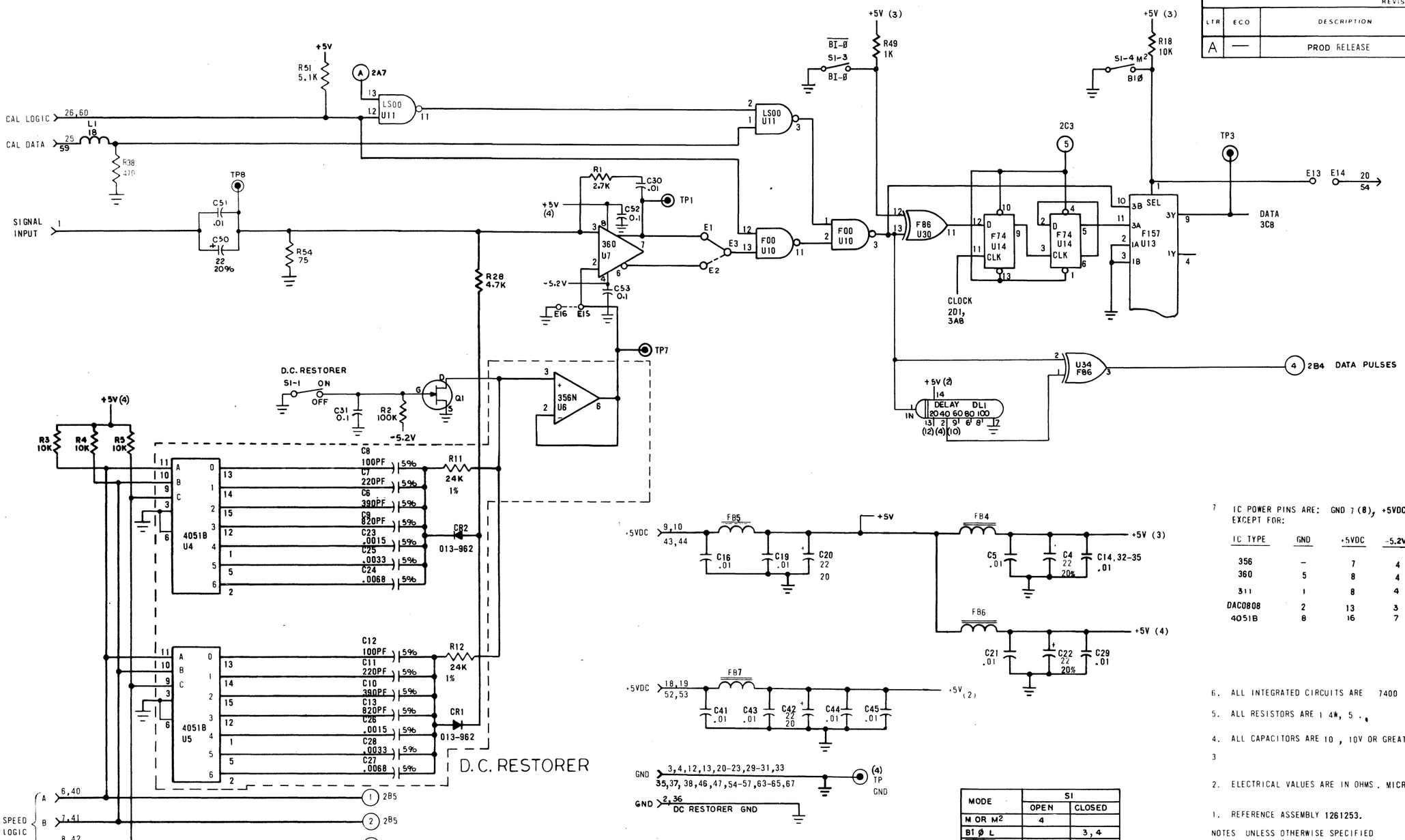
1259670-01

D	92739	1259670 -01	
	—		SHEET 2 OF 3

LTR	ZONE	DESCRIPTION	SIGNATURE AND DATE		
			DRN	CHK	ENGRG
B	—	SEE SH 1	—	—	—



REVISIONS					
LTR	ECO	DESCRIPTION	SIGNATURE AND DATE		
			DRAWN BY	CHK BY	ENGRG APPD
A	—	PROD RELEASE	[illegible] 8/26/81	[illegible] 5-4-82	[illegible] 5-6-82



MODE	S1	
	OPEN	CLOSED
M OR M2	4	
BIØL		3,4
BIØL	3	4
DCR OUT		1
DCR IN	1	

7 IC POWER PINS ARE: GND 7 (8), +5VDC = 14 (16) EXCEPT FOR:

IC TYPE	GND	+5VDC	-5.2VDC
356	—	7	4
360	5	8	4
311	1	8	4
DAC0808	2	13	3
4051B	8	16	7

6. ALL INTEGRATED CIRCUITS ARE 7400 SERIES EXCEPT CD4051,356,360,393 DAC0808
5. ALL RESISTORS ARE 1 4W, 5 .
4. ALL CAPACITORS ARE 10 , 10V OR GREATER.
3
2. ELECTRICAL VALUES ARE IN OHMS , MICROFARADS AND MICROHENRIES.
1. REFERENCE ASSEMBLY 1261253.

NOTES UNLESS OTHERWISE SPECIFIED

REFERENCE DESIGNATIONS		
FIRST	LAST	NOT USED
A1	A2	
C1	C56	
CR1	CR4	
DS1	DS1	
FB1	FB7	
R1	R54	R16,17,28
TP1	TP7,TPG	
U1	U33	

—	HBR3000
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES
TOL ± | 2 PLC | 3 PLC | ANG
REMOVE BURRS AND SHARP EDGES
DO NOT SCALE THIS PRINT

	SIGNATURE	DATE
DRAWN BY	[illegible]	8/26/81
CHK BY	[illegible]	5-4-82
DFT APPD		
ENGRG APPD		
AUTH BY	[illegible]	5/6/82

MATERIAL
FINISH

AMPEX DATA PRODUCTS DIVISION

SCHEMATIC DIAGRAM, BIT SYNC/DECODER

SIZE	CODE IDENT NO	
D	92739	1261250-01
SCALE —		SHEET 1 OF 3

1261250-01

REVISIONS					
LTR	ZONE	DESCRIPTION	SIGNATURE AND DATE		
			DFT	CHK	ENGRG
A	-	SEE SHEET 1	—	—	—

VCO'S

BIT SYNC

REVISIONS					
LTR	ZONE	DESCRIPTION	SIGNATURE AND DATE DFT	CHK	ENGRG
A	–	SEE SHEET 1	—	—	—

NRZ CLK
2A1

4X CLK
2A1

DATA SENSE
(NORMAL =1)
(INVERTED=0)
32,66

DATA
1C2

CLOCK
2D1

FWD/REV LOGIC
(FWD=1)
(REV=0)
27,61

+5V(2)

R42 1K
R40 1K
R41 22K
R48 1K
R47 1K
R39 1K
R45 1K
R46 1K
R43 1K
R44 1K

S74 U24
S74 U22
S74 U29
S74 U25
S174 U33
S175 U28
S37 U21
S04 U20
S04 U32
S86 U23
S260 U31
F86 U30
S20 U27
S10 U26

E6 E4 E7 E9 NRZ E5 E8
E10 E11 E12

C49 100 PF 5
C47 100 PF 5
C48 100 PF 5
C46 100 PF 5

TP6
TP5

28 CLOCK OUT
62 $\overline{\text{CLOCK OUT}}$
68 $\overline{\text{DATA OUT}}$
34 DATA OUT

MILLER DECODER

101 DETECTOR

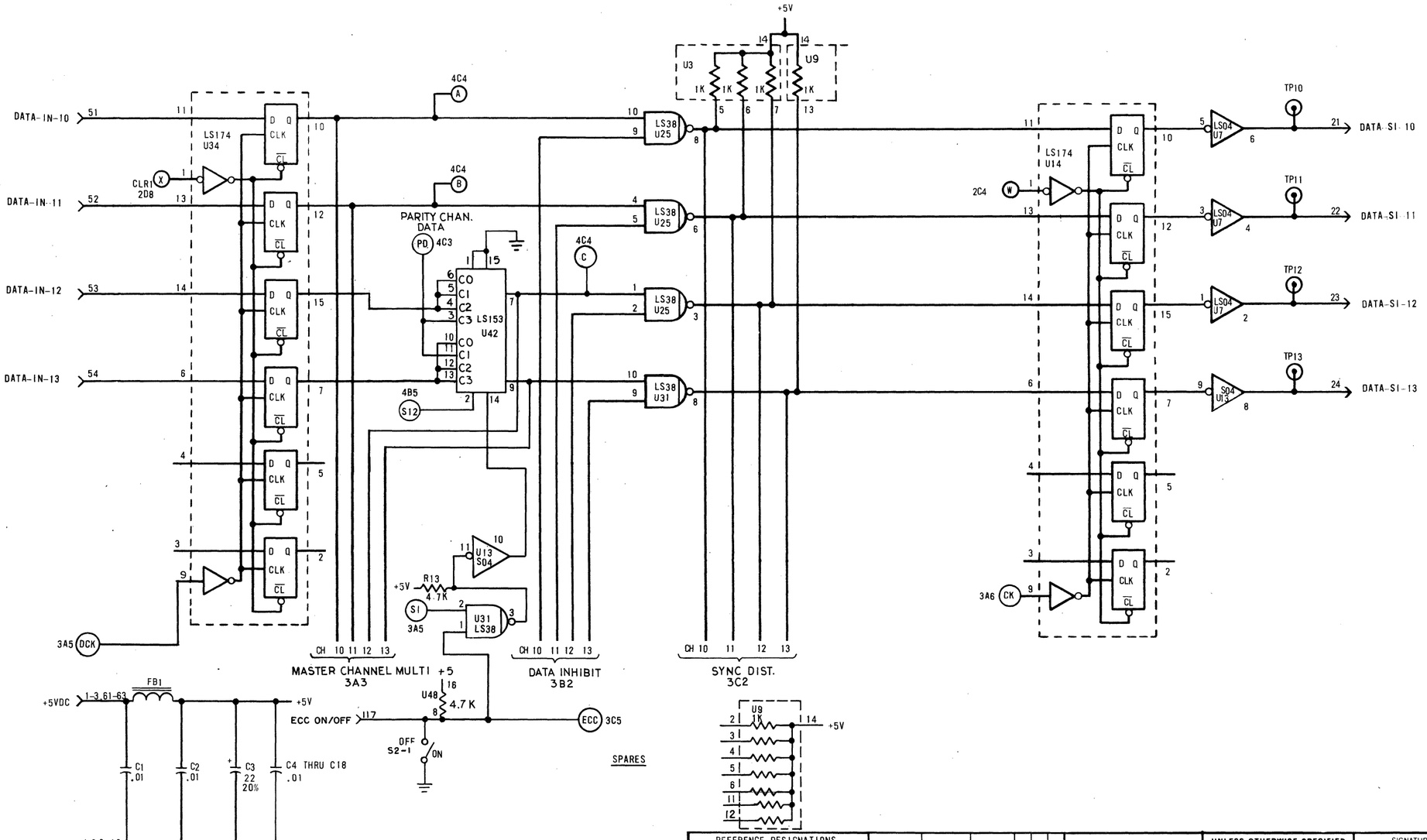
M^2 DECODER

1261250-01

SIZE	CODE IDENT NO	1261250-01
D	92739	
SCALE —		SHEET 3 OF 3

UC 3504A (Rev Aug 67) Printed in U.S.A.

LTR	ZONE	DESCRIPTION	SIGNATURE AND DATE DFT	CHK	ENGRG
1		PRE PRODUCTION RELEASE	C.F. 11-19-82	W.J.S. 11-19-82	



8 JUMPERS FOR NON STANDARD FUNCTIONS
E3-E4 = NONSYMMETRICAL SYNC WORD
E1-E2 = 256 BIT SYNC TO SYNC.

7. IC POWER PINS ARE GND=7, +5VDC=14 EXCEPT FOR:

IC TYPE	GND	+5VDC
LS112	8	16
150	12	24
154	12	24
LS157	8	16
159	12	24
LS163	8	16
LS174	8	16
LS175	8	16
LS273	10	20
LS395	8	16

6. SELECT VALUE AND INSTALL AT TEST IF REQUIRED.
5. ALL INTEGRATED CIRCUITS ARE: SN5400/SN7400 SERIES.
4. ALL RESISTORS ARE ±5%, 1/4W.
3. ALL CAPACITORS ARE ±10%, 10 VDC OR GREATER.
2. ELECTRICAL VALUES ARE IN OHMS AND MICROFARADS.
1. REFERENCE ASSEMBLY 1257353-02.

NOTES: UNLESS OTHERWISE SPECIFIED.

REFERENCE DESIGNATIONS		
FIRST	LAST	NOT USED
C1	C18	
DL1	DL1	
E1	E7	
R1	R27	R9,10,16-26
TP1, TPG(3)	TP18, TPG(3	TP14,15
U1	U49	
FB1	FB1	
S1	S2	

CAT. ITEM	NEXT ASSY	USED ON	IN	MF	PR CODE
	1261623	HBR ECC			

APPLICATION

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES.
TOL ± 2 PLC 3 PLC ANG
REMOVE BURRS AND SHARP EDGES YES NO
DO NOT SCALE THIS PRINT

SIGNATURE		DATE
DRAWN BY	K Sampson	9/24/82
CHK BY	W J Shanks	11-19-82
DFT APPD		
ENGRG APPD	J D Rinear	12-13-82
AUTH BY	J A Vice	12-16-82

MATERIAL:
FINISH:

AMPEX HEADQUARTERS Redwood City, California 94063

SCHEMATIC DIAGRAM, SYNC INSERTER (ECC)

SIZE	CODE IDENT NO.	
D	92739	1261620-02

SCALE — SHEET 1 OF 4

1261620-02

REVISIONS					
LTR	ZONE	DESCRIPTION	SIGNATURE AND DATE		
			DFT	CHK	ENGRG
1	-	SEE SHEET 1	—	—	—

+5V
R3
1K
CLR 1
1C8
DATA-IN-1
DATA-IN-2
DATA-IN-3
DATA-IN-4
DATA-IN-5
DATA-IN-6
DATA-IN-7
DATA-IN-8
DATA-IN-9
3A5 DCK
LS175 U24
LS174 U30
4D4 SH 4
4D4
4C4
LS38 U20
LS38 U15
LS38 U25
U3 1K
3B2
LS175 J2
LS174 U8
1C4
3A6 CK
LS04 U1
LS04 U7
TP1
TP2
TP3
TP4
TP5
TP6
TP7
TP8
TP9
DATA SI 1
DATA-SI-2
DATA-SI-3
DATA SI 4
DATA SI 5
DATA SI 6
DATA SI 7
DATA SI 8
DATA-SI-9
CH 1 2 3 4 5 6 7 8 9
MASTER CHANNEL MULTIPLEXER 3A3
DATA INHIBIT 3C2
SYNC DISTR. 3C2

SIZE	CODE IDENT NO	1261620-02
D	92739	
SCALE —		SHEET 2 OF 4

REVISIONS					
LTR	ZONE	DESCRIPTION	SIGNATURE AND DATE DFT	CHK	ENGRG
1	-	SEE SHEET 1	—	—	—

SSW/NSSW 59
PE-SI 32
MASTER/SLAVE-SI 33
RESET-SI 30
CLOCK PARALLEL 41
512/256 36
SYNC/NO SYNC 34
+5V
R6 1K
R1 1K
R2 1K
R4
R7 1K
U9 1K
E1 E2 E3 E4
LS00 U19
LS04 U12
LS04 U13
LS10 U23
LS20 U18
LS20 U27
S04 U22
S00 U49
U31 LS38
U49 S00
U27 LS20
LS74 U5
LS74 U6
LS00 U5
LS163 U11
LS163 U16
LS163 U17
LS157 U10
R5 1K
R8 1K
R15 1K
R27 1K
C18 200PF
TP16
TP17
TP18
TC-SI
CLK-PAR-SI
SYNC SI
DATA-SI-MASTER
DATA INHIBIT 2A5
1B6 DATA INHIBIT
SYNC DISTR 2A5
SYNC DISTR 1B5
MASTER CHANNEL MULTI 2A6
MASTER CHANNEL MULTI 1B6
159 U4
154 U21
150 U26
Q4 4B4
ECC 1B6
TC 4A8
CK 1B4 2A4 4A8 4B2
SI 1B6
DCK 1B8 2A8
I14 4A4
I15 4A4
FF 4D3
GG 4D3
HH 4C3
JJ 4C3
R 2D3
S 2D3
T 2D3
D 4B2

UC-3504A (Rev Aug 67) Printed in U.S.A.

SIZE	CODE IDENT NO	1261620-02
D	92739	
SCALE —		SHEET 3 OF 4

REVISIONS					
LTR	ZONE	DESCRIPTION	SIGNATURE AND DATE DFT	CHK	ENGRG
1		SEE SHT 1			

ECC-SEL-1 102 E1 A
ECC-SEL-2 103 E2 B
ECC-SEL-3 104 E3 C
ECC-SEL-4 105 E4 D
ECC-SEL-5 106 E5 E
ECC-SEL-6 107 E6 F
ECC-SEL-7 108 E7 H
ECC-SEL-8 109 E8 J
ECC-SEL-9 110 E9 K
ECC-SEL-10 111 E10 L
ECC-SEL-11 112 E11 M
ECC-SEL-12 113 E12 N
TWO/ONE-PARITY 114 E13 P
SPARE 115 E14

+5V 16
U48 4.7K 7 6 5 4 3 2 9 10 11 12 13 14 15

S1-8 S1-7 S1-6 S1-5 S1-4 S1-3 S1-2 S1-1 S2-8 S2-7 S2-6 S2-5 S2-4 TWO ONE PARITY

2D6 G LS02 U36 5 6 4
2D6 H LS02 U36 3 2 1
2C6 J LS02 U36 11 12 13
2C6 K LS02 U36 8 9 10
2C6 L LS02 U33 11 12 13
2B6 M LS02 U33 8 9 10
2B6 N LS02 U33 6 5 4
2B6 P LS02 U33 3 2 1
2B6 Q LS02 U29 11 12 13
1D6 A LS02 U32 12 11 13
1C6 B LS02 U32 3 2 1
1C6 C LS02 U29 8 9 10
LS02 U32 8 9 10

S280 U35 EVEN 5
S280 U28 EVEN 5

U38 LS04 6 9 8 → 116 PAR-SI-OUT
U47 S86 9 10 8 → PD 1C6

3A2 FF 6 D Q 7 → 40 SI-CTR-D
3A2 GG 4 D Q 5 → 39 SI-CTR-C
3A2 HH 13 D Q 12 → 38 SI-CTR-B
3A2 JJ 11 D Q 10 → 37 SI-CTR-A
CK P
+5V R11 1K 1
CK 9 3A7
U37 LS174

S12 1C6
+5V R14 1K
PAR-SI-IN 119

TWO/ONE-PARITY
SPARE
S153 U41 CO C1 C2 C3 A B STR Y
S153 U40 CO C1 C2 C3 A B STR Y
S86 U47 1 2 3 / 13 12 11 / 5 4 6
165 U46 QH SHFT/LD SER IN
165 U45 H G F E D C B A QH SHFT/LD SER IN
LS04 U38 13 12
+5V R12 4.7K
3B5 TC
3A7 CK
LS163 U39 CEP CET PE MR CP P0 P1 P2 P3 TC QA QB QC

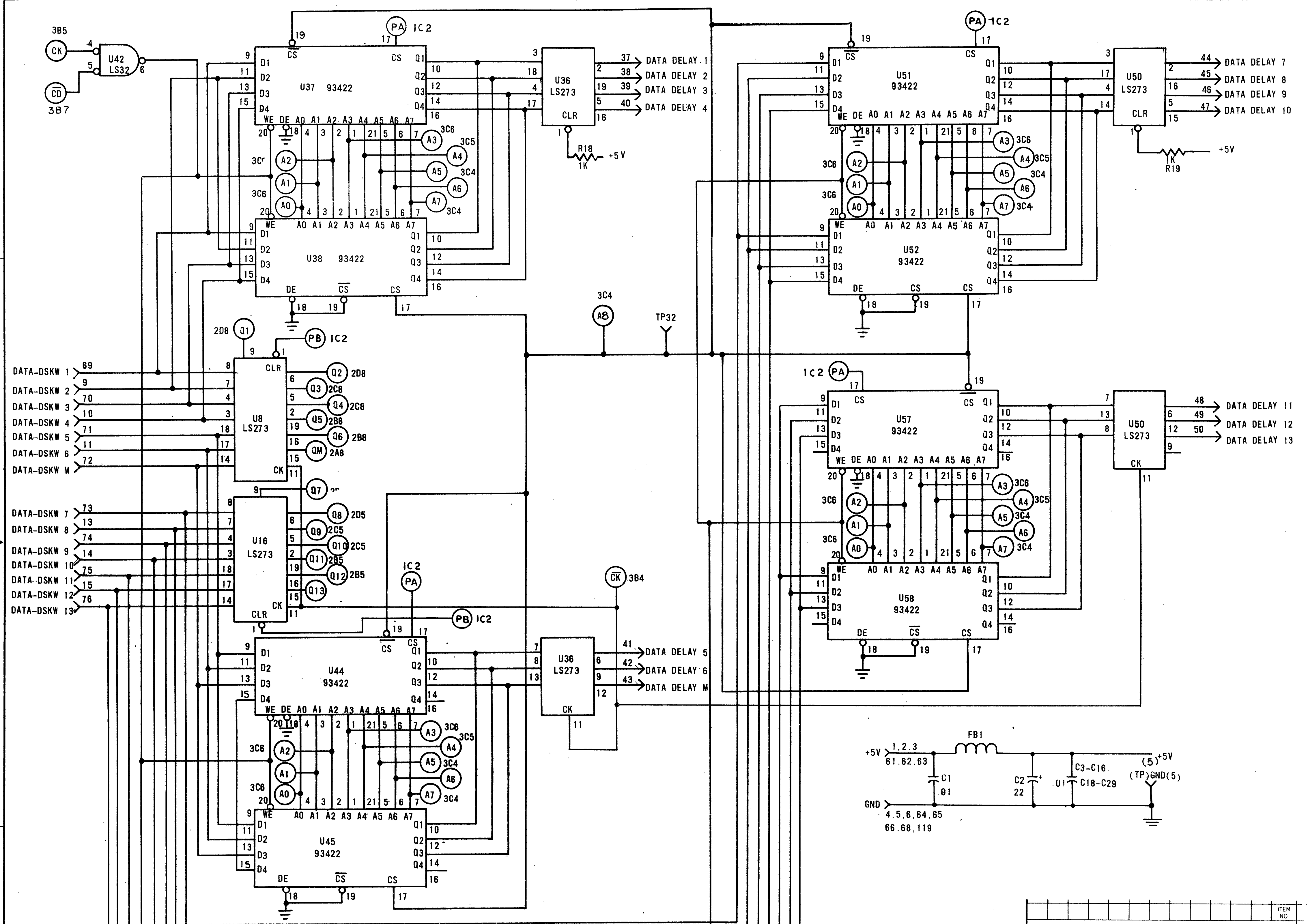
TP21
M48-DATA-IN 118
LS04 U38 5 6
LS00 U43 9 10 8 / 5 4 6 / 13 12 11
TP19
D 3A3
3C6 Q4
3B2 I14
3B2 I15
LS02 U44 2 3 1 / 11 10 / 8 9 10 / 6 5 4 / 12 11 13
58 M48-GATE-OUT

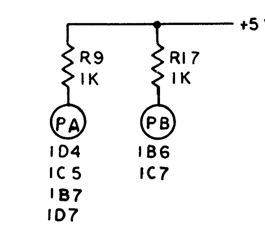
SIZE	CODE IDENT NO.	1261620-02
D	92739	
SCALE —		SHEET 4 OF 4

DISTR CODE:

REVISIONS

LTR	ZONE	DESCRIPTION	DFT	CHK	ENGRG
2	–	PRE-PROD RELEASE	[illegible]	[illegible]	[illegible]
3	–	REV PER ECR 31499-4 (A3)	[illegible]	[illegible]	[illegible]





4. I C POWER PINS ARE; GND = 7, +5VDC 14 EXCEPT FOR:

LOCATION	GND	+5VDC
U8,16,36,50	10	20
U37,38,44,45, 51,52,57,58	8	22
U47,48,53,54 55,56,61,63	8	16

3. RESISTORS ARE 1/4 WATT.

2. ELECTRICAL VALUES ARE IN OHMS, MICROFARADS, AND MICROHENRIES.

1. REFERENCE ASSEMBLY 1261633-02.

NOTES: UNLESS OTHERWISE SPECIFIED.

QUANTITY PER VERSION | ITEM NO | PART NUMBER | DESCRIPTION

PARTS LIST

1261633	HBR/ECC
NEXT ASSY	USED ON

APPLICATION

UNLESS OTHERWISE SPECIFIED

DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES

TOL ± | 2 PLC | 3 PLC | ANG

REMOVE BURRS AND SHARP EDGES YES ☐ NO ☐

DO NOT SCALE THIS PRINT

MATERIAL

FINISH

	SIGNATURE	DATE
DRAWN BY	[illegible]	5-25-82
CHK BY	[illegible]	11-12-82
DFT APPD		
ENGRG APPD	[illegible]	11-12-82
AUTH BY	[illegible]	[illegible]

AMPEX

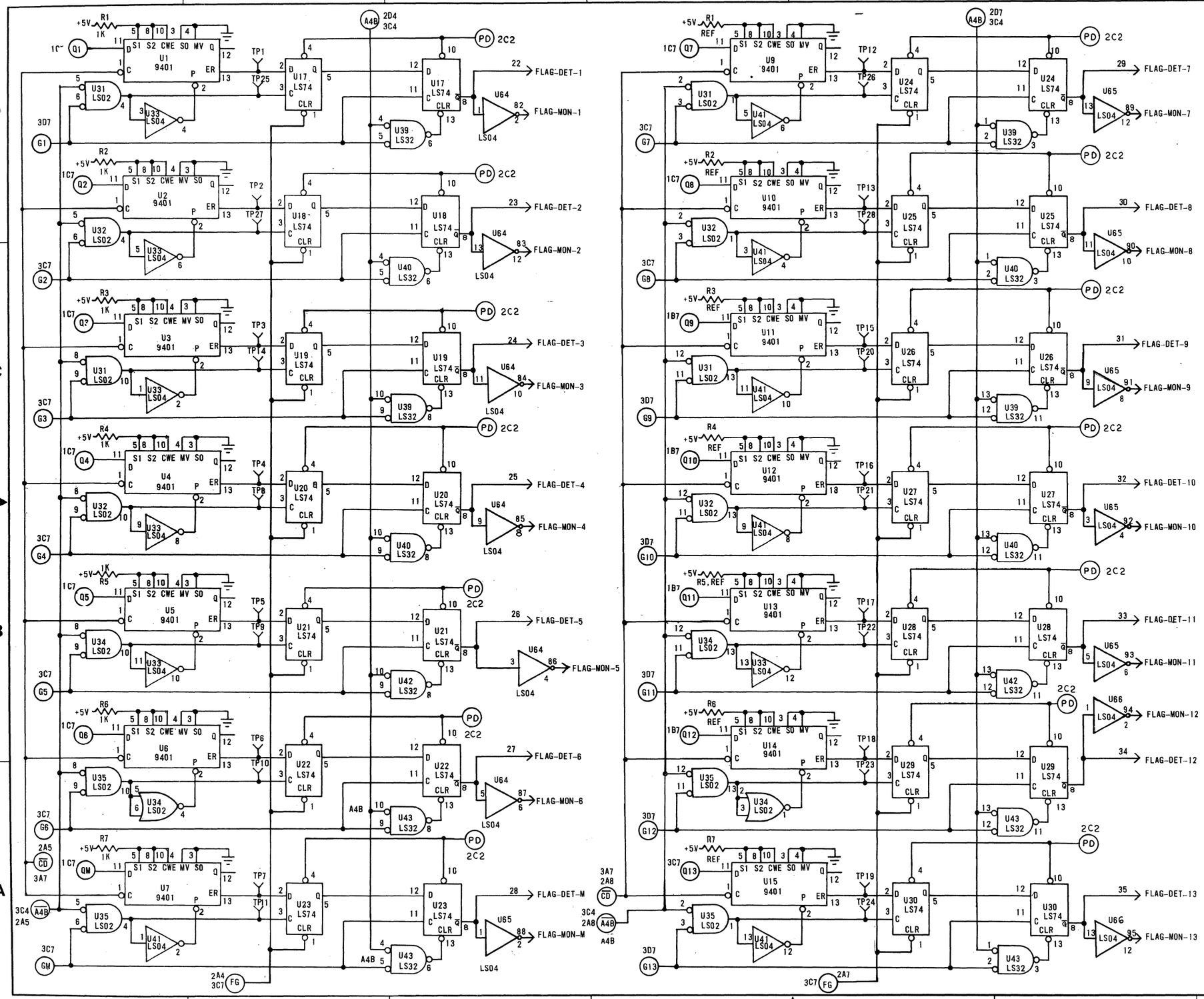
HEADQUARTERS
Redwood City,
California 94063

SCHEMATIC DIAGRAM CRC-ECC ERROR DETECTOR AND DELAY

SIZE D | CODE IDENT NO 92739 | 1261630-02

SCALE – | SHEET 1 OF 3

REVISIONS					
LTR	ZONE	DESCRIPTION	SIGNATURE AND DATE		
			DFT	CHK	ENGRG
3	–	SEE SHEET ONE	–	–	–



REFERENCE DESIGNATION	
LAST USED	NOT USED
C29	C17
FB1	
R21	R12-14
TP32	
U66	

SIZE	CODE IDENT NO.	
D	92739	1261630-02
SCALE –		SHEET 2 OF 3

REVISIONS					
LTR	ZONE	DESCRIPTION	SIGNATURE AND DATE DFT	CHK	ENGRG
3	–	SEE SHEET ONE	–	–	–

80 CH 14

U47 LS138 — Y5 Y6 Y7 — G1 2D8, G9 2C5, G10 2B5, G11 2B5, G12 2A5, G13 2A5, N/L

U48 LS138 — G2 2C8, G3 2C8, G4 2B8, G5 2B8, G6 2A8, GM 2A8, G8 2C5, G7 2D5

U46 LS04 — 58 CSDB, 57 CSCB, 56 CSBB, 55 CSAB

U63 S151 — +5V R10, 1K; R11 1K; 111 M48-GATE

U49 265 — SERIAL FLAG 53; TP30; FG 2A4 2A7

U56 LS112 — TP29; DECODE OFF; 5V R16 1K

U60 LS74 — U59 LS86; R15 REF +5

U62 — U42 LS32

U49 265 — A4B 2A5 2A8; A4B 2D7 2D4

2C7 1C6; A8 A7 A6 A5 — 1B6, 1D6, 1C4, 1D4

1B7, 1D7, 1C4, 1D4; +5V R15 1K; A0 A1 A2 A3

1B6, 1D6, 1C4, 1D4 — A4

U53 LS163; U54 LS163; U55 LS163 — R21 1K +5V

+5V R15 REF; U61 LS175 — 115 CSAA, 116 CSBA, 117 CSCA, 118 CSDA

+5V R8 1K; ECC ON/OFF; U49 265; R16 REF +5V

U49 74265 — CLOCK PARALLEL M (POS) 120 60; TP31

CK 1D8

$\overline{CK}$ 1B6

$\overline{CD}$ 2A8 2A5

UC 3504A (Rev Aug 67) Printed in U.S.A.

SIZE	CODE IDENT NO	1261630-02
D	92739	
SCALE –		SHEET 3 OF 3

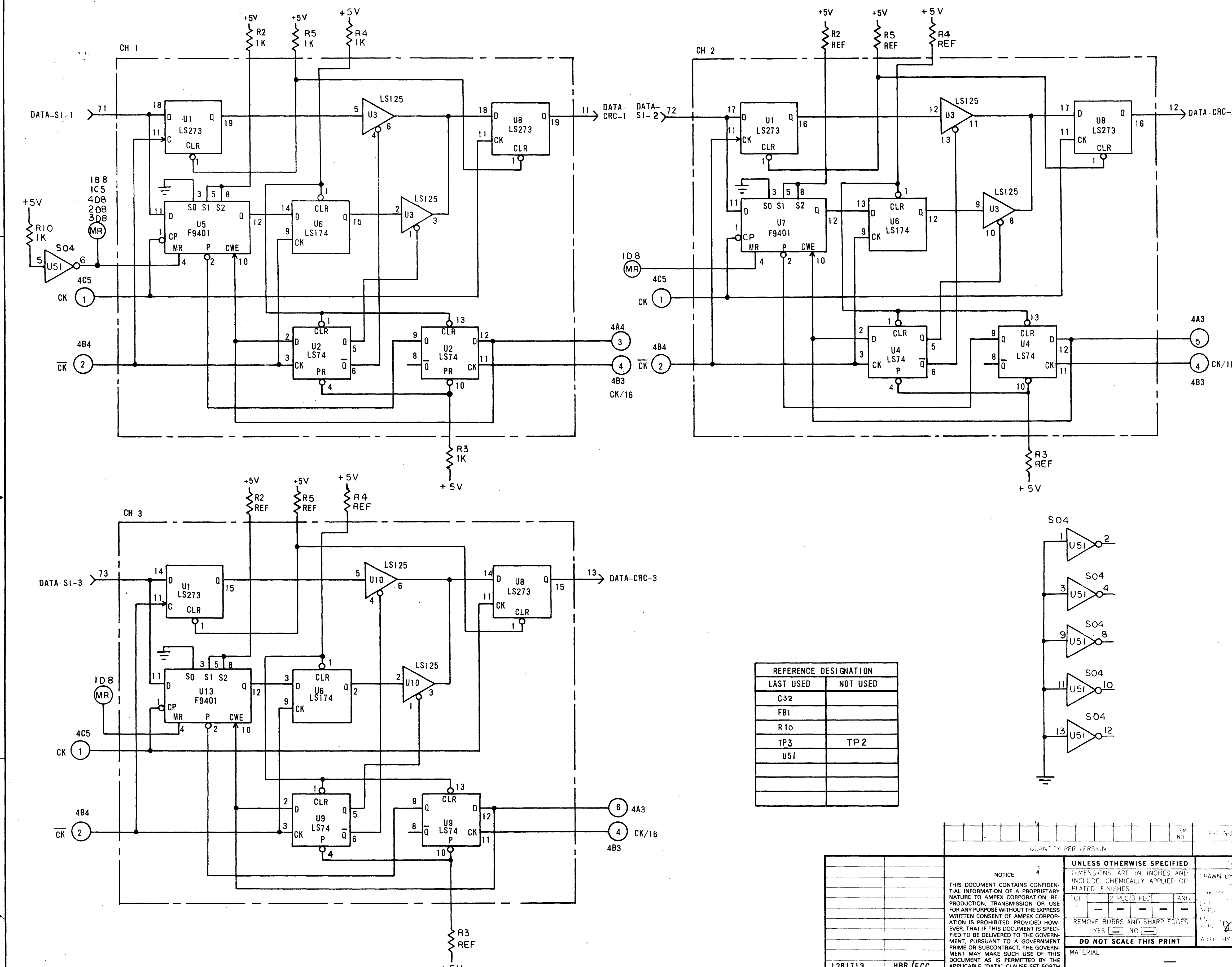
1261630-02

1261710-02

DISTR CODE: 1

REVISIONS

LTR	ZONE	DESCRIPTION	DFT	CHK	ENGRG
1	–	PRE-PROD RLSE			11-12-82
2	-	REV PER ECR 31311-4 (A.3)	13DEC82 C. FU		12-21-82



REFERENCE DESIGNATION	
LAST USED	NOT USED
C32	
FB1	
R10	
TP3	TP2
U51	

4. I.C. POWER PINS ARE

IC#	+5V	GND
U1,8,41,46	PIN 20	PIN 10
U2-5,7,9-11 13,15,17-29, 31,33,35-38, 40,42-45,47-50	PIN 14	PIN 7
U6,12,14,16,30, 32,34,39	PIN 16	PIN 8

3. RESISTORS ARE 1/4 WATT.

2. ELECTRICAL VALUES ARE IN OHMS, MICROFARADS, AND MICROHENRIES.

1. REF. ASSEMBLY 1261713-02.

NOTE: UNLESS OTHERWISE SPECIFIED.

ITEM NO.	PART NUMBER	DESCRIPTION
QUANTITY PER VERSION		PARTS LIST

NEXT ASSY	USED ON
1261713	HBR/ECC
APPLICATION	

NOTICE

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES

TOL: 2 PLC – 3 PLC – ANG –

REMOVE BURRS AND SHARP EDGES YES ☐ NO ☐

DO NOT SCALE THIS PRINT

MATERIAL: —

FINISH: —

	SIGNATURE	DATE
DRAWN BY	Charles Fry	4-6-82
	M. Slamb	11-11-82
	J. Zinner	11/12/82
AUTH BY	H.A. Vidal	12 Nov 82

AMPEX — HEADQUARTERS, Redwood City, California 94063

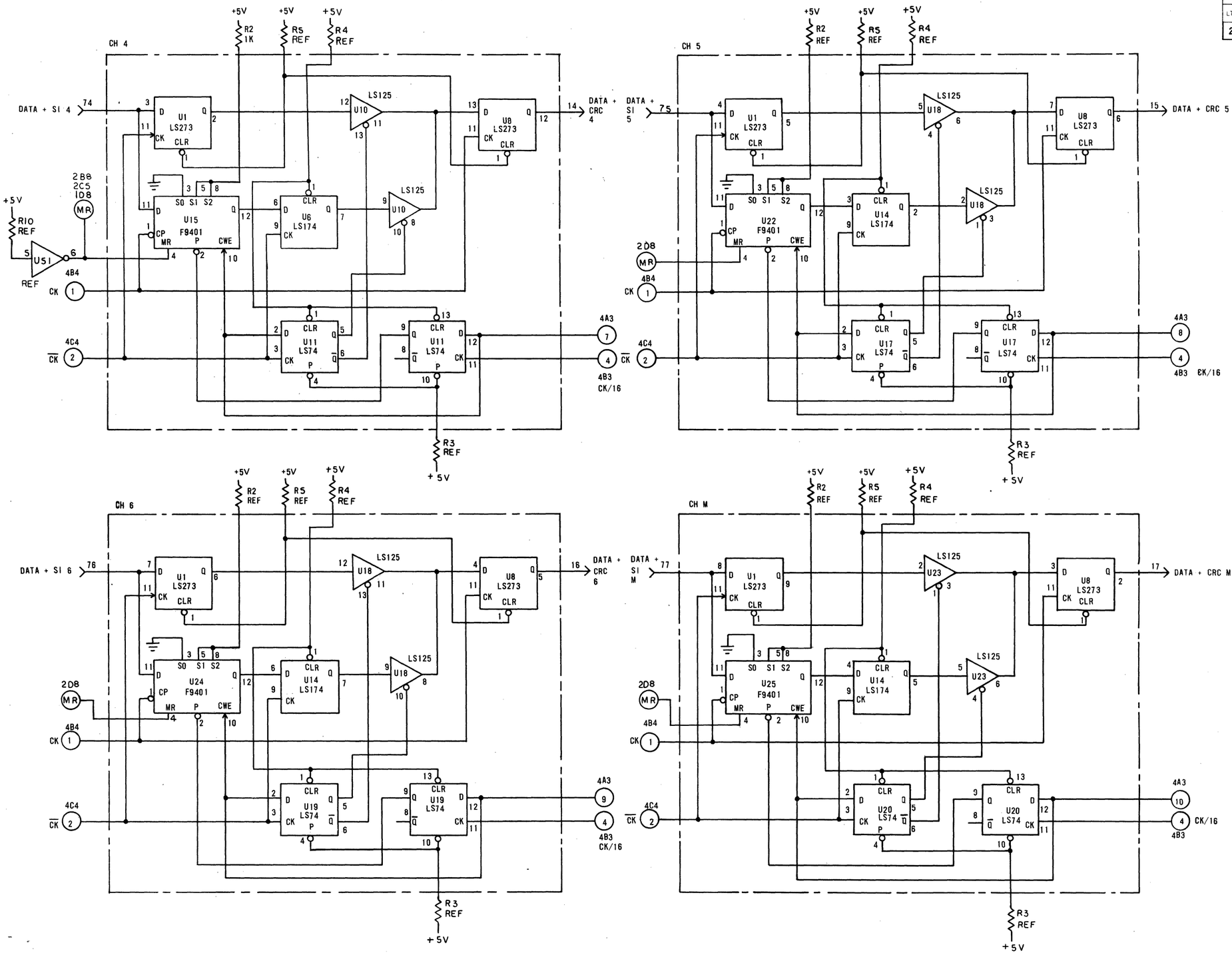
SCHEMATIC DIAGRAM CRC GENERATOR / INSERTER

SIZE D | CODE IDENT NO 92739 | 1261710-02

SCALE — | SHEET 1 OF 4

UC3504 (Rev Jan 82) Printed in U.S.A.

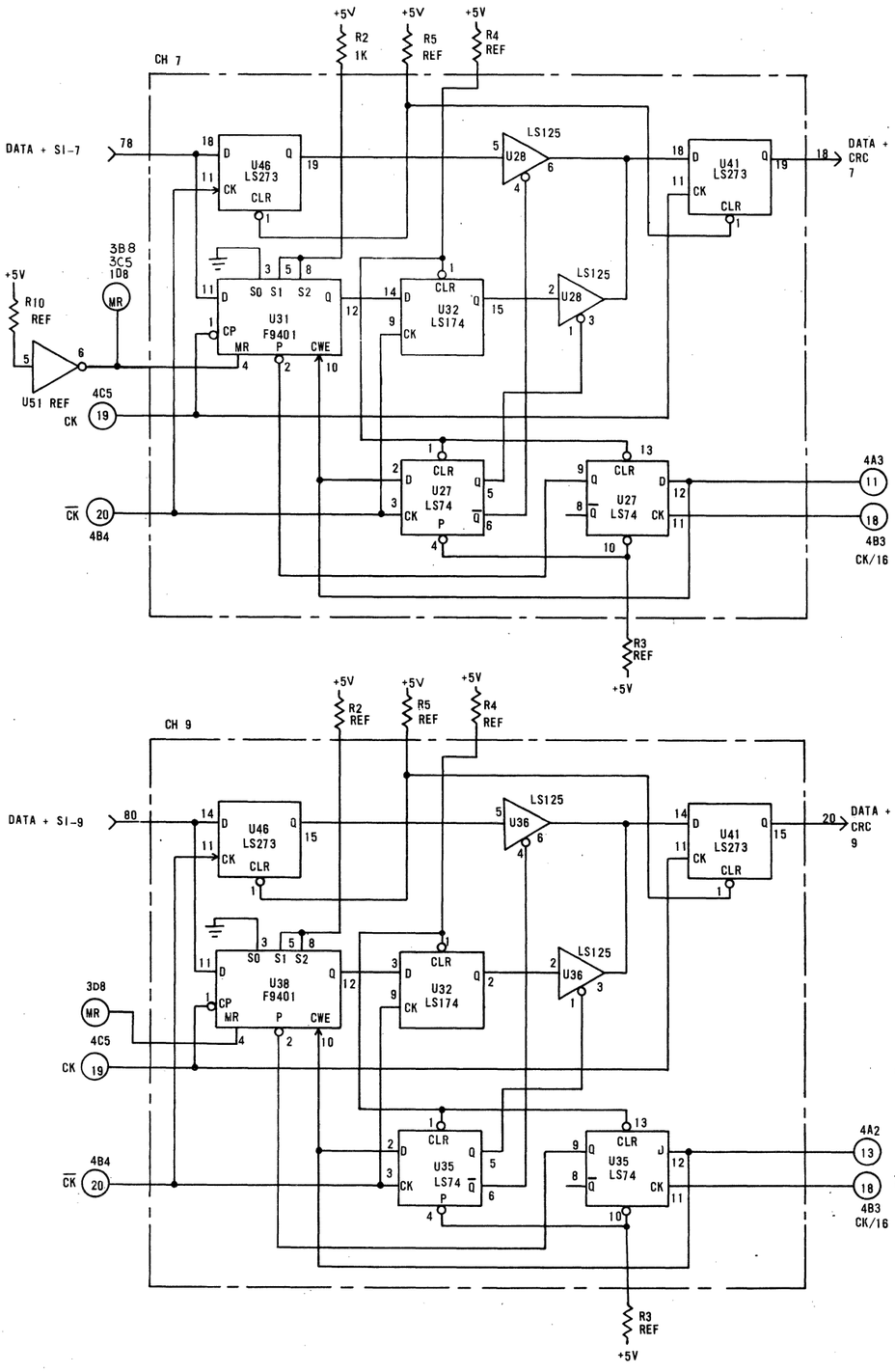
REVISIONS					
LTR	ZONE	DESCRIPTION	SIGNATURE AND DATE DFT	CHK	ENGRG
2	-	SEE SHEET 1	-	-	-

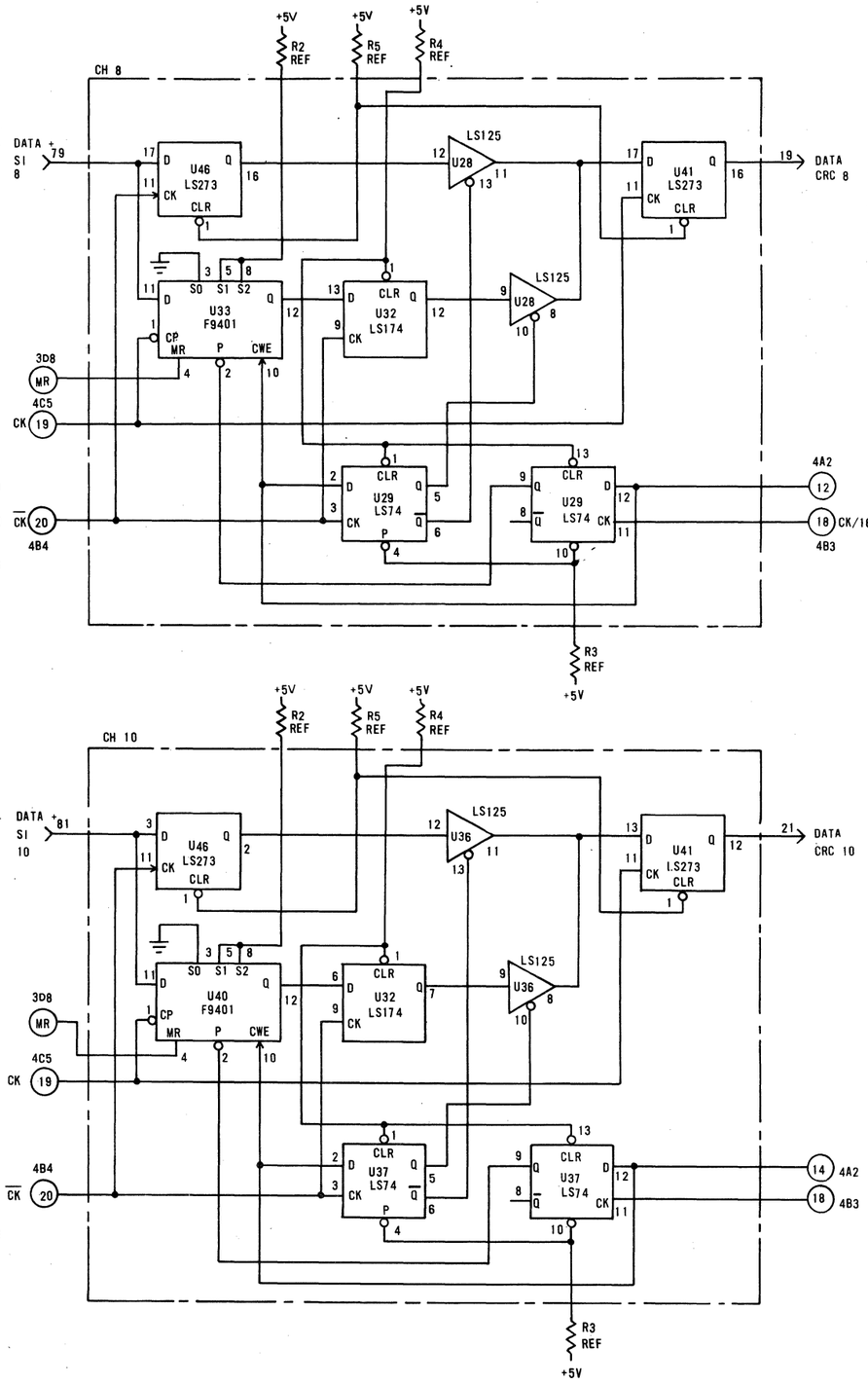


1261710-02

DISTR CODE:

LTR	ZONE	DESCRIPTION	SIGNATURE AND DATE: DFT	CHK	ENGRG
2	-	SEE SHEET 1	-	-	-





UC3504 (Rev Jan 82) Printed in U.S.A.

SIZE	CODE IDENT NO	1261710-02
D	92739	
SCALE —		SHEET 3 OF 4

1261710-02

ITEM	CHANGE	SIGNATURE AND DATE DFT	CHK	ENGRG
2	-	SEE SHEET 1	-	-	-

CH 11

DATA + SI 11 82

U46 LS273 CLR

U47 F9401 SO S1 S2 CP MR P CWE

U39 LS174 CLR CK

LS125 U43

U41 LS273 CLR

22 DATA + CRC 11

DATA + SI 12 83

+5V R10 REF

U51 REF

4B8 4C5 1D8 MR

4B4 CK 19

4B4 CK 20

U42 LS74 CLR CK P

4A2 15

4B3 CK/16 18

R2 1K

R5 REF

R4 REF

R3 REF

CH 12

U46 LS273 CLR

U49 F9401 SO S1 S2 CP MR P CWE

U39 LS174 CLR CK

LS125 U43

U41 LS273 CLR

23 DATA + CRC 12

4D8 MR

4B4 CK 19

4B4 CK 20

U44 LS74 CLR CK P

16 4A2

18 4B3 CK/16

R2 REF

R5 REF

R4 REF

R3 REF

CH 13

DATA + SI 13 84

U46 LS273 CLR

U50 F9401 SO S1 S2 CP MR P CWE

U39 LS174 CLR CK

LS125 U48

U41 LS273 CLR

24 DATA + CRC 13

4D8 MR

4B4 CK 19

4B4 CK 20

U45 LS74 CLR CK P

17 4A2

18 4B3 CK/16

R2 REF

R5 REF

R4 REF

R3 REF

TP3

CLOCK IN 41

S04 U21

2A5 CK, CH1-6&M 2

1 2A5 CK, CH1-6&M

+5V R5 REF

R1 1K

U12 LS163 P T CLR CK A B C GND LOAD OUT QA QB QC QD

U16 LS112 PR CLR J K Q

1C2 4 CK/16, CH1-6&M

4C5 20 CK, CH7-13

4C5 19 CK, CH7-13

18 4A5 CK/16, CH7-13

TP1

SI-COUNTER-A 37

SI-COUNTER-B 38

SI-COUNTER-C 39

SI-COUNTER-D 40

U26 LS20

U30 LS138 G1 A B C G2A G2B Y0 Y1 Y2 Y3 Y4 Y5 Y6 Y7

1C5 CH 1

1A5 2C2 2A5 2A2 3C5

U34 LS138 G1 A B C G2A G2B Y0 Y1 Y2 Y3 Y4 Y5 Y6 Y7

3C2 CH 8 3A5 3A2 4C2 4C5 4A5

CH 1 CH 2 CH 3 CH 4 CH 5 CH 6 CH M CH 7

CH 8 CH 10 CH 11 CH 12 CH 13

+5V R8 1K R6 1K R9 1K R7 1K

ECC ON/OFF 119

512/256 36

SSW/NSSW 59

SYNC/NO SYNC 34

U26 LS20

C31 0.1 C29 0.1 C32 0.1 C30 0.1

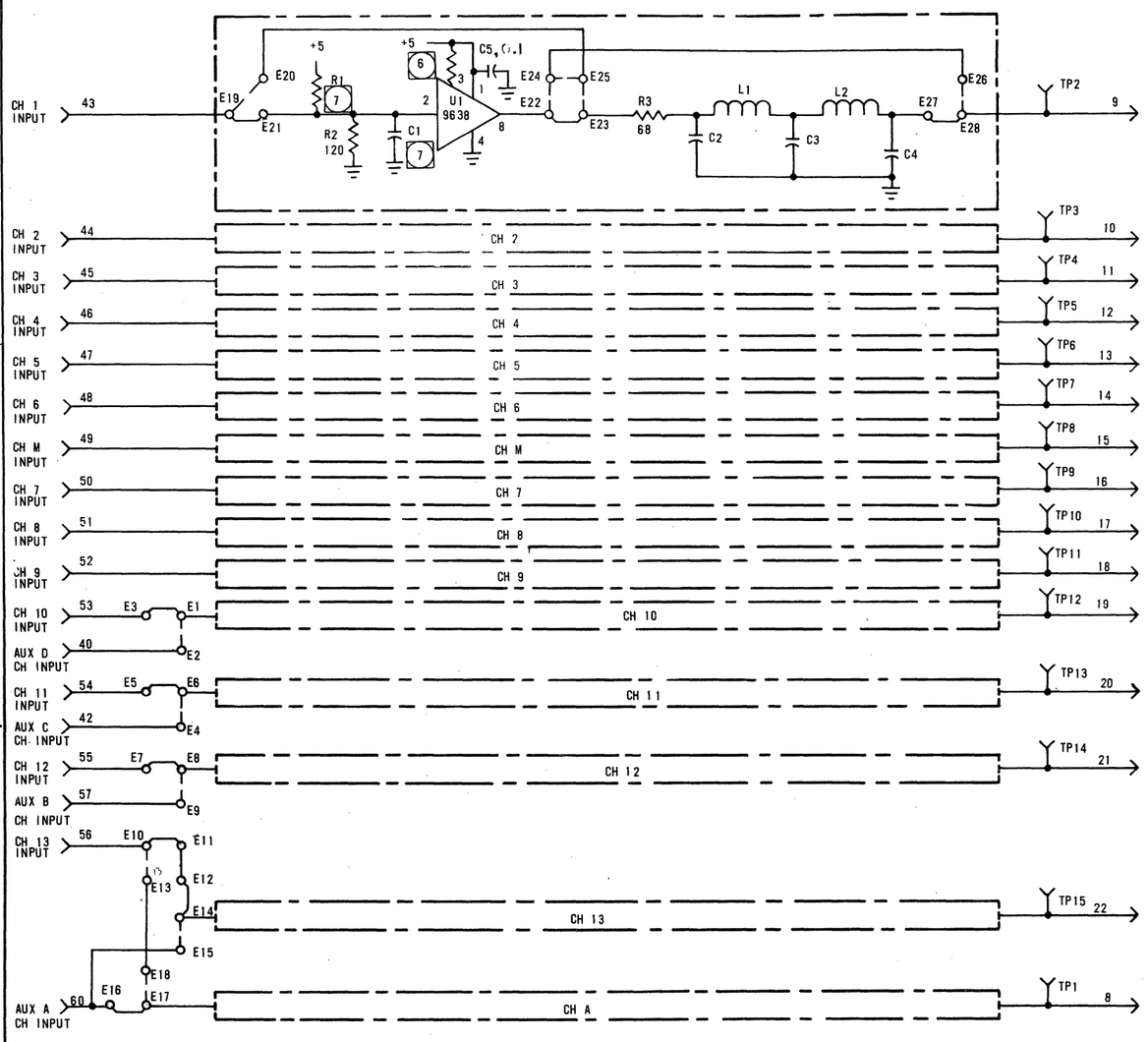
1,2,3 61,62,63 +5V

4,5,6 64,65,66 GND

C1 .01 C2 22UF C3-28 .01 FB1

+5V GND (3)

REVISIONS					
LTR	ZONE	DESCRIPTION	SIGNATURE AND DATE DFT	CHK	ENGRG
A	–	PROD REL			



VERSION	C2	C3	C4	L1	L2	REMARKS
-01	180	560	1500	2.2	3.9	FILTER ON CHAN A & 13 ONLY
-02	180	560	1500	2.2	3.9	3.3 MHz LP
-03	130	430	1200	2.2	3.3	4.0 MHz LP

JUMPER LIST			
LINE DRIVER/FILTER CONFIGURATION		JUMPER FROM	TO
DIGITAL	BIAS	E19 E22 E27	E21 E23 E28
DIGITAL	NON-BIAS	E19 E22 E26	E21 E24 E28
ANALOG	BIAS	E19 E23 E27	E20 E25 E28
TYPICAL INPUT CHAN. SELECTION		JUMPER FROM	TO
ANALOG AUX (AUX A)	AUX 1 ON TK1	E16	E17
ANALOG AUX (AUX A)	AUX 2 ON TK28	E14	E15
DIGITAL AUX (CH 13)	CH 13 ON TK1	E10 E17	E13 E18
DIGITAL AUX (CH 13)	CH 26 ON TK28	E10 E12	E11 E14
REQUIRED FOR NORMAL DIGITAL OPERATION	(CH 10)	E1	E3
	(CH 11)	E5	E6
	(CH 12)	E7	E8

REFERENCE DESIGNATIONS	
LAST USED	NOT USED
C8	
L2	
R10	
U1	
E28	
TP15, TPG	
FB1	

7 NOT INSTALLED (FOR FUTURE USE)

6 PULL UP RESISTORS 1K, FOR ALL CHAN U1 PIN 3, R4 FOR CHAN 1,2,3, R5 FOR CHAN 4,6, R6 FOR CHAN 5,M, R7 FOR CHAN 7,9, R3 FOR CHAN 9,10, R9 FOR CHAN 11,13 R10 FOR CHAN 12,A.

5. IC 9638 +5V ON PIN 1, GND ON PIN 4.
4. RESISTORS ARE +2%, 1/4W.
3. ALL CAPACITORS ARE ±5%, 500 VDC OR GREATER.
2. REFERENCE ASSEMBLY 1261763-XX.
1. ELECTRICAL VALUES ARE IN OHMS, PICOFARADS & MICROHENRIES.

NOTES: UNLESS OTHERWISE SPECIFIED.

ITEM NO.	PART NUMBER	DESCRIPTION	QUANTITY PER VERSION

PARTS LIST

1261763	AHBR1700
1261763	HBR3000
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES.
TOL ± | 2 PLC – | 3 PLC – | ANG –
REMOVE BURRS AND SHARP EDGES
YES ☐ NO ☐
DO NOT SCALE THIS PRINT
MATERIAL:
FINISH:

	SIGNATURE	DATE
DRAWN BY		7-7-82
CHK BY	W J Sanders	11-18-82
DFT APPD		
ENGRG APPD	B. Camus	11-19-82
AUTH BY	H. A Wells	22 Nov 82

AMPEX
HEADQUARTERS
Redwood City,
California 94063

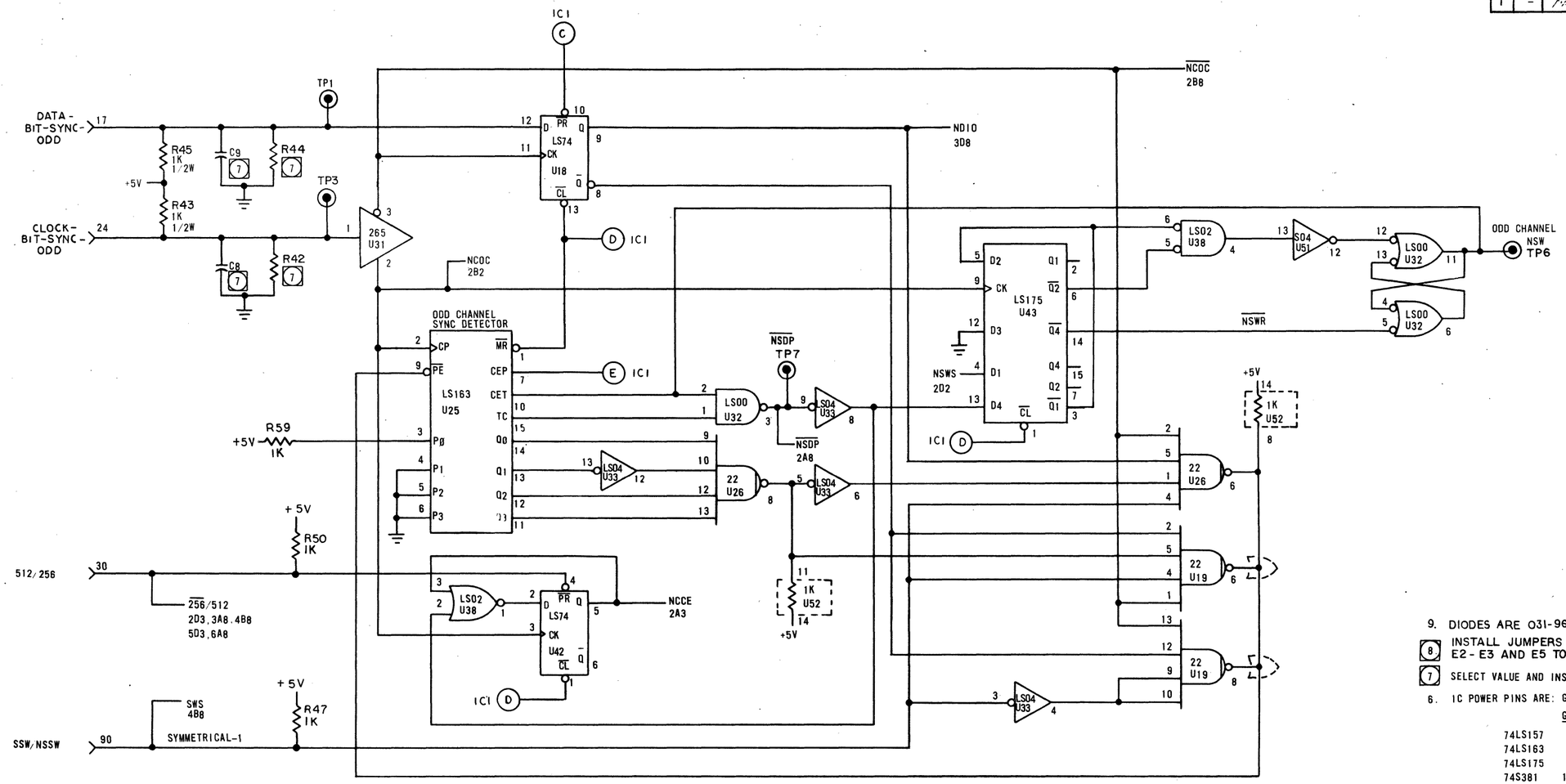
SCHEMATIC DIAGRAM,
LINE DRIVER/ FILTER,
75 OHMS

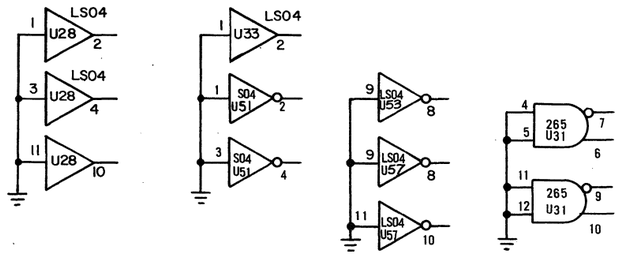
SIZE	CODE IDENT NO.	
D	92739	1261760-XX

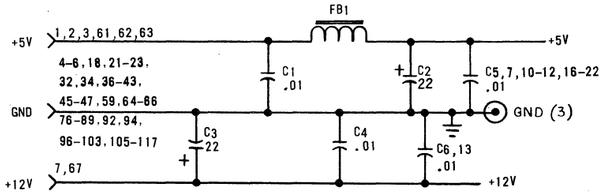
SCALE — SHEET 1 OF 1

1261760-XX

REVISIONS			
LTR	ZONE	DESCRIPTION	SIGNATURE AND DATE DFT CHK ENGRG
1	–	[illegible]	[illegible]







9. DIODES ARE 031-962.
8. INSTALL JUMPERS E1-E2 AND E4-E5 FOR STANDARD HBR APPLICATION, E2-E3 AND E5 TO E6 ARE FOR ECC APPLICATION ONLY.
7. SELECT VALUE AND INSTALL AT TEST IF REQUIRED.
6. IC POWER PINS ARE: GND=7, +5VDC=14 EXCEPT FOR

	GND	+5VDC	+12VDC
74LS157	8	16	
74LS163	8	16	
74LS175	8	16	
74S381	10	20	
14517	8	–	16
74LS85	8	16	

5. INTEGRATED CIRCUITS ARE SN7400N SERIES EXCEPT FOR 14517.
4. RESISTORS ARE 5%, 1/4 WATT.
3. CAPACITORS ARE 10%, 10VDC OR GREATER.
2. ELECTRICAL VALUES ARE IN OHMS & MICROFARADS.
1. REFERENCE ASSEMBLY 1261783-02.

NOTES: UNLESS OTHERWISE SPECIFIED

SLAVE ODD CHANNEL

PARTS LIST

.05	.04	.03	.02	.01	ITEM NO.	PART NUMBER	EQUIVALENT VENDOR OR MIL PART NUMBER (REF ONLY)	DESCRIPTION	FMC	LONG LEAD ITEM
QUANTITY PER UNIT										
ASSY CONTROL NO.										

REFERENCE DESIGNATIONS	
LAST USED	NOT USED
C22	
FB1	
R60	
TP15,(TP)GND(3)	TP13
U57	U30

CAT. ITEM	NEXT ASSY	USED ON	IN	MF	PR CODE
	1261783	HBR/ECC			

APPLICATION

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES
TOL ± 2 PLC 3 PLC ANG
REMOVE BURRS AND SHARP EDGES YES ☐ NO ☐
DO NOT SCALE THIS PRINT

	SIGNATURE	DATE
DRAWN BY	[illegible]	3/4/82
CHK BY	[illegible]	11-17-82
DFT APPD		
ENGRG APPD	[illegible]	11 19 82
AUTH BY	[illegible]	11 Nov 82

MATERIAL:
FINISH:

AMPEX
HEADQUARTERS Redwood City, California 94063

SCHEMATIC DIAGRAM, 2 CHANNEL SLAVE DESKEW

SIZE	CODE IDENT NO.	
D	92739	1261780 -02

SCALE NONE | SHEET 1 OF 6

UC-3504.03 (3-74) PRINTED IN U.S.A.

1261780-02

REVISIONS					
LTR	ZONE	DESCRIPTION	SIGNATURE AND DATE DFT	CHK	ENGRG
1	—	SEE SH 1	—	—	—

ODD CHANNEL NUMBER PROGRAM INPUTS
PGM P0
PGM P1
PGM P2
PGM P3
FWD/REV
+5V
1K U21
1K U52
S04 U51
LS86 U20
S381 U27
B0 B1 B2 B3 CIN
Σ0 Σ1 Σ2 Σ3
A0 A1 A2 A3
S2 S1 S0
LS04 U28
LS86 U22
LS08 U56
R48 1K
U29 LS85
A=B
LS08 U56
105 NSWS
256/512
LS00 U55
FWD 5C8
NCOC 1D3
NSDP 1C5
SNQ4
LS163 U34
CTR Ø CTR 1 CTR 2 CTR 3
P4 P5 P6 P7
Q4 Q5 Q6 Q7
SNQ5 SNQ6 SNQ7
CP PE MR CEP CET TC
ODD CHANNEL NRZ COUNTER
TP11
LS163 U35
P0 P1 P2 P3
Q0 Q1 Q2 Q3
IC2 IC1
SNQ3
ODD CHANNEL NCCE 1B6
LS10 U12
LS20 U14
SNQ6 SNQ7
WCB 3C8
NCOC 1C6
WCD 3A8
WCC 3B8
WCA 3C8

SLAVE ODD CHANNEL

SIZE	CODE IDENT NO.	
D	92739	1261780-02
SCALE —		SHEET 2 OF 6

1261780-02

REVISIONS					
LTR	ZONE	DESCRIPTION	SIGNATURE AND DATE DFT	CHK	ENGRG
1	—	SEE SH 1	—	—	—

+12V
R5 620 1/2W
NDIO 1D4
06 U36
14517 U9
R19 560
R12 680
R21 820
R17 560
R14 680
WCA 2A2 READ CLK A
10, 70
26 U7
RCA 6C8
14517 U3
R33 820
R16 560
R20 680
WCB 2B2 READ CLK B
11, 71
RCB 6C8
R18 560
R13 680
NRZ DATA IN. ODD CHANNEL
14517 U1
R31 680
WCC 2A2 READ CLK C
8, 68
RCC 6B8
R1 560
R11 560
R46 680
R30 680
14517 U2
R2 820
R3 560
WCD 2B2 READ CLK D
9, 69
RCD 6A8
R15 560
R4 820
R32 680
256/512 1B8
LS157 U8
1A 1B 2A 2B 3A 3B 4A 4B G S 1Y 2Y 3Y 4Y
READ GATE B 15 75 RGB 6C5
READ GATE A 14, 74 RGA 6C5
READ GATE C 12, 72 RGC 6B5
READ GATE D 13, 73 RGD 6B5
LS54 U13
REINSERTED DATA 20
SYNC INHIBIT 16
LS00 U23
TP2 DATA PLUS SYNC
IC1
LS74 U37 PR CK CL D
S37 U24
DATA DSKW ODD 19
CLK-PAR-DLY 60
DMCI 9
S04 U51
DMCI 6C2
DATA-CAL-DSKW-ODD 25
TP8 DATA
E1 E2 E3

1261780-02

SLAVE ODD CHANNEL

SIZE	CODE IDENT NO.	
D	92739	1261780-02
SCALE —		SHEET 3 OF 6

REVISIONS					
LTR	ZONE	DESCRIPTION	SIGNATURE AND DATE DFT	SYS T	ENGRG
1	—	SEE SH 1	—	—	—

DATA-BIT SYNC-EVEN 51
CLOCK-BIT SYNC-EVEN 52
+5V
R49 1K 1/2W
R56 1K 1/2W
C14 (7)
C15 (7)
R54 (7)
R55 (7)
TP4
TP12
265 U31
NCEC 5B2
IC1 (C)
LS74 U18
D PR Q CK CL
(D) IC1
NCEC 5B8
NDIE 6D8
EVEN CHANNEL SYNC DETECTOR
LS163 U49
CP PE MR CEP CET TC P0 P1 P2 P3 Q0 Q1 Q2 Q3
(B) IC2
(A) IC2
LS00 U55
LS04 U57
NSDP TP14
NSDP 5A8
LS175 U48
D1 D2 D3 D4 CK CL Q1 Q2 Q3 Q4
NSWS 5D1
NC
LS02 U38
LS00 U55
NSWR
EVEN CHANNEL NSW TP15
+5V
R53 1K
22 U50
22 U44
R60 1K
+5V
256/512 1B8
LS02 U38
LS74 U42
NCCE 5A3
(D) IC1
SWS 1B8

SLAVE EVEN CHANNEL

SIZE	CODE IDENT NO.	1261780-02
D	92739	
SCALE NONE		SHEET 4 OF 6

1261780-02

REVISIONS					
LTR	ZONE	DESCRIPTION	SIGNATURE AND DATE DFT	CHK	ENGRG
1	—	SEE SH 1	—	—	—

EVEN CHANNEL NUMBER PROGRAM INPUTS

PGM P0 53
PGM P1 54
PGM P2 55
PGM P3 56
FWD (F) 2B7

+5V
1K U52
3 6 1 4

S381 U46
BØ B1 B2 B3 CIN
ΣØ ΣI Σ2 Σ3
S2 S1 SØ
1K U52 +5V

LS86 U45
LS04 U51
LS04 U53
LS86 U47
LS08 U54
LS85 U41
A0 A1 A2 A3 B0 B1 B2 B3 A=B
R51 1K +5
LS08 U54 NSWS 4C4

NCEC 4D3
NSDP 4C5 (EVEN CHANNEL)

LS163 U40
CP PE MR CEP CET TC P0 P1 P2 P3 Q0 Q1 Q2 Q3
CTR 0 CTR 1 CTR 2 CTR 3
SNQ5 SNQ6 SNQ7
EVEN CHANNEL NRZ COUNTER

LS163 U39
EVEN CHANNEL NRZ COUNTER
SNQ3
EVEN CHANNEL NCCE 4B5

TP10

2B7 FWD (F)
256/512
LS10 U15
LS20 U14
+5V 1K U21

WCB 6C8
NCEC 4C6
WCD 6A8
WCC 6B8
WCA 6C8

SLAVE EVEN CHANNEL

SIZE	CODE IDENT NO.	
D	92739	1261780-02

SCALE — SHEET 5 OF 6

UC-3504A (Rev Aug 67) Printed in U.S.A.

REVISIONS					
LTR	ZONE	DESCRIPTION	SIGNATURE AND DATE DFT	CHK	ENGRG
1	—	SEE SHEET 1	—	—	—

+12V
R8 620 1/2 W
NDIE 4D3
U36
14517 U17
R38 560
R40 680
+12V R27 820
R39 560
R37 680
WCA 5A2
RCA 3C8
U10
R9 680
14517 U6
+12V R41 820
R28 560
WCB 5B2
RCB 3C8
R29 560
R10 680
NRZ DATA IN EVEN CHANNEL
R36 680
WCC 5A2
RCC 3B8
14517 U5
R26 560
R25 560
R34 680
R35 680
+12V R7 820
14517 U4
R24 560
WCD 5B2
RCD 3A8
R23 560
R6 820
+12V
R22 680
256/512 1B8
LS157 U11
1A 1B 2A 2B 3A 3B 4A 4B G
1Y 2Y 3Y 4Y S
RGB 3C4
RGA 3C4
RGC 3B4
RGD 3B4
LS54 U16
44 REINSERTED DATA
48 SYNC INHIBIT
LS00 U23
TP5
DATA PLUS SYNC
DMCI 3B2
IC1
LS74 U37
S37 U24
49 DATA DSKW EVEN
50 DATA-CAL DSKW EVEN
TP9 DATA
E4
E5
E6

UC-3504A (Rev Aug 67) Printed in U.S.A.

SLAVE EVEN CHANNEL

SIZE	CODE IDENT NO.	
D	92739	1261780-02
SCALE —		SHEET 6 OF 6

1261780-02

			SIGNATURE AND DATE		
	NO.	REVISION	ENGR	CHK	ENGRG
1		PRE-PRO REL			
2	-	REV PER ECR 31326-4 (B)			

VERSION TABLE

SCHEM NO.	USED WITH ASSY
1261790-01	1261793-01 (INACTIVE)
1261790-02	1261793-02 SHOWN
1261790-03	1261793-03 (11)

TRANSPORT REF SELECT

SWITCH		FUNCTION
S1-B	S1-A	DIVISION (E20-21 & E23-24)
CLOSED	CLOSED	÷4
CLOSED	CLOSED	÷8
OPEN	CLOSED	÷16
OPEN	OPEN	÷32

OPEN = OFF CLOSED = ON

JUMPER TABLE

FROM	TO	FUNCTION
E20	E21	÷ 4 OR ÷ 8 OR ÷16 OR ÷32 XTAL REF FREQ
E20	E22	÷ 2 XTAL REF FREQ
E24	E23	÷ 4 OR ÷ 8 OR ÷16 OR ÷32
E24	E25	÷ 2 TAPE FREQ
E12	E13	READ CLOCK SELECT
E12	E14	READ CLOCK SELECT

(11) -02 VERSION SHOWN. ON -03 VERSION, U8 IS REMOVED.

(10) REMOVE JUMPER E29-E30 TO PREVENT TBC OPERATION (AHBR1700 AND HBR-ES).

(9) SELECTED FOR POSITIVE CLOCK AT PIN 59 RELATIVE TO DATA AT PIN 30 (TP7).

8. DIODES ARE 013-962.

(7) SELECT VALUE & INSTALL AT TEST IF REQUIRED.

6. REFERENCE ASSEMBLY 1261793.

5. ALL RESISTORS ARE ±5%, 1/4 WATT & TERMINATE AT +5VDC.

4. ALL CAPACITORS ARE ±10%, 10VDC OR GREATER.

3. IC POWER PINS ARE GND = 7, +5VDC = 14 EXCEPT FOR

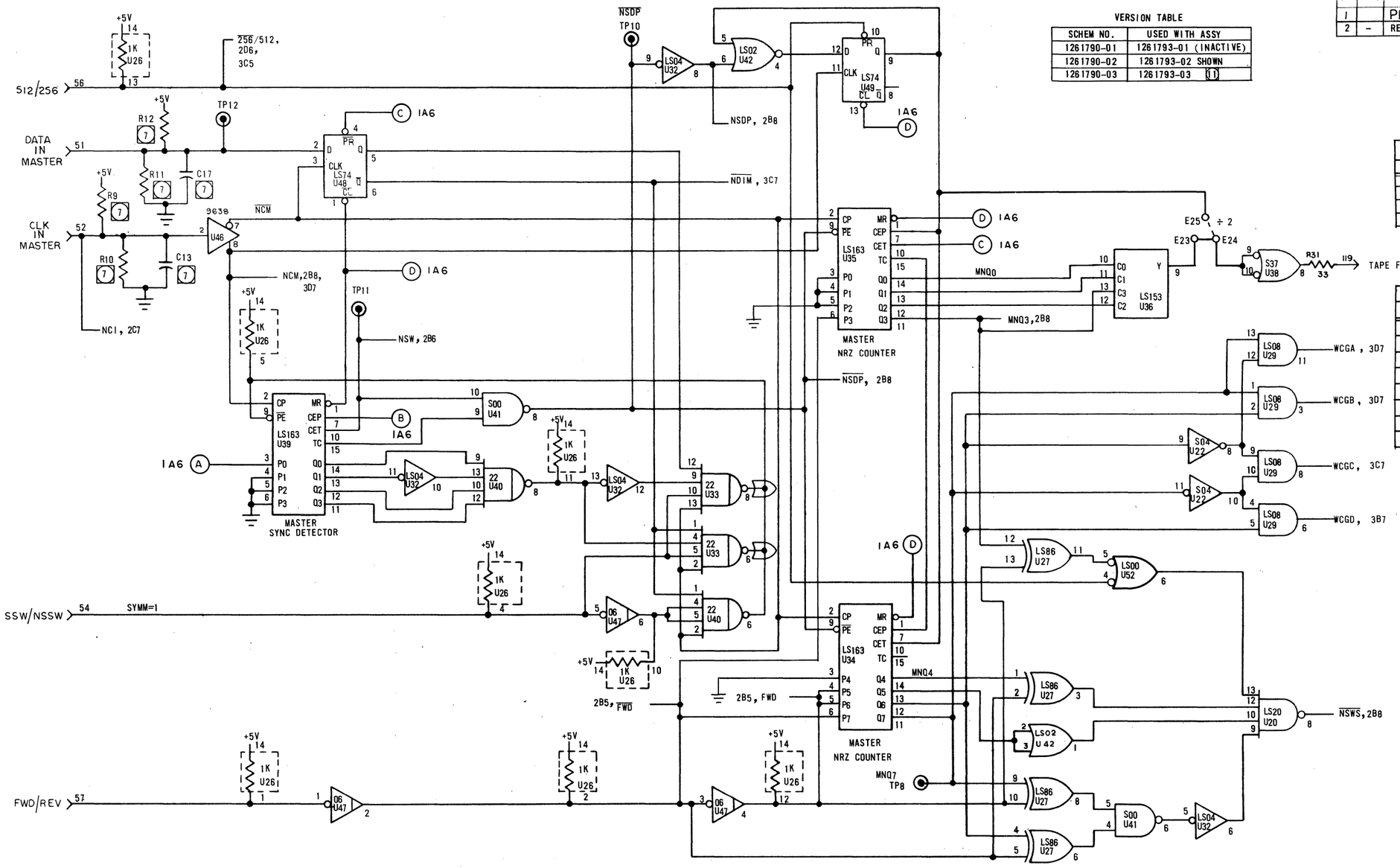
	GND	+5VDC	+12VDC
74LS153	8	16	-
74154	12	24	-
74LS157	8	16	-
74LS163	8	16	-
74LS174	8	16	-
74S175	8	16	-
9638	4	1	-
14517	8	-	16

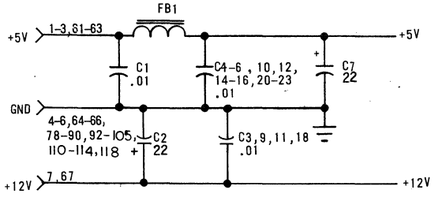
2. ALL INTEGRATED CIRCUITS ARE SN7400N SERIES EXCEPT 14517 AND 9612E.

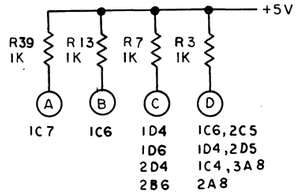
1. ELECTRICAL VALUES ARE IN OHMS AND MICROFARADS.

NOTES: UNLESS OTHERWISE SPECIFIED

1261790-XX







REFERENCE DESIGNATIONS		
FIRST	LAST	NOT USED
C1	C23	C8
E1	E30	
FB1	FB1	
R1	R39	
TP1	TP13	TP9
U1	U52	U45
S1	S1	
DLI	DLI	

CAT. ITEM	NEXT ASSY	USED ON	IN	MF	PR CODE
	1261793 HBR/ECC				

APPLICATION

NOTICE

THIS DRAWING SHALL NOT BE DUPLICATED, USED FOR ANY PURPOSE OTHER THAN THAT FOR WHICH PROVIDED OR DISCLOSED, IN WHOLE OR IN PART, WITHOUT THE WRITTEN CONSENT OF AMPEX CORPORATION. PROVIDED, HOWEVER, THAT IF THIS DRAWING IS SPECIFIED TO BE DELIVERED TO THE GOVERNMENT, OR TO A GOVERNMENT CONTRACTOR, PURSUANT TO A GOVERNMENT PRIME OR SUBCONTRACT, THE GOVERNMENT MAY MAKE SUCH USE OF THIS DRAWING AS IS PERMITTED BY THE APPLICABLE "DATA" CLAUSE SET FORTH IN SUCH CONTRACT OR SUBCONTRACT

.05	.04	.03	.02	.01	ITEM NO.	PART NUMBER	EQUIVALENT VENDOR OR MIL PART NUMBER (REF ONLY)	DESCRIPTION	FMC	LONG LEAD ITEM
QUANTITY PER UNIT										
ASSY CONTROL NO.										

PARTS LIST

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES
TOL ± | 2 PLC | 3 PLC | ANG
REMOVE BURRS AND SHARP EDGES YES ☐ NO ☐
DO NOT SCALE THIS PRINT

MATERIAL:
FINISH:

SIGNATURE		DATE
DRAWN BY	A. Dao	11-4-82
CHK BY	W. Stanke	11-18-82
DES APPD		
ENGRG APPD		11/19/82
AUTH BY		21NOV82

AMPEX
HEADQUARTERS
Redwood City,
California 94063

SCHEMATIC DIAGRAM
MASTER DESKEW, TIME BASE

SIZE	CODE IDENT NO.	
D	92739	1261790-XX

SCALE — | SHEET 1 OF 3

UC-3504.03 (3-74) PRINTED IN U.S.A.

REVISIONS					
LTR	ZONE	DESCRIPTION	SIGNATURE AND DATE		
			DFT	CHK	ENGRG
2	-	SEE SHEET 1	—	—	—

1D7, 256/512

3B7, XPEL

LS02 U42

LS74 U49

TP13

1A6

CLK
XCPE
MXQ0
XQ0L
3B8
3B7

S00 U41

LS20 U50

XSDP

R38 1K

CLOCK-PARALLEL 55

R17 7

R16 7

C19 7

1C8, NCI

LS51 U44

S00 U41

S37 U38

58 CLK-PAR-OUT-(POS)

LS163 U43

MASTER XTL COUNTER

LS74 U48

MXQ2

MXQ1

MXQ0

S1

LS153 U36

R37 1K

+5V

E22 ÷ 2

E20

E21

S37 U38

120 XTAL-REF/QX

MANUAL/AUTO-DESKEW 115

U3 1K

LS04 U32

LS20 U50

LS51 U44

LS04 U2

R2 33

17 SYNC DESKEW MASTER

R5 1K

R4 1K

E8 E7 E6 E5

LS20 U20

DTLC=1 116

TBC/NOTBC 1

E29 50

E30 10

U26 1K

LS51 U51

LS00 U52

TP2

E4 E3 E2 E1

R15 33

60 CLOCK-PARALLEL-M (NEG)

9638 U46

REC/REP 117

1C4, NSDP

06 U47

XCPE

DLI

E16 E17 E18 E19 9

E14 R CLOCK SELECT

E13 E12

RCS, 3C7

S04 U22

S37 U38

76 TC DESKEW-M

R30 33

59 MASTER CLK OUTPUT CLOCK-PARALLEL-M

1K U26

+5V

1C4, MNQ3

1B2, NSWS

LS175 U12

LS00 U52

LS04 U2

1D5, NSDP

1C7, NCM

NSWR

NSW, 1C6

LS74 U18

TP4

TP3

TP5

1A6

FLAG TP1

S37 U1

53 FLAG

R1 33

16 PE DESKEW-M

MXQ4

MXQ7 TP6

U14 PROM

1B5, FWD

1B5, FWD

MASTER XTL COUNTER

FLAG TEST

LS174 U13

CSAA, 3B3

CSBA, 3B3

CSCA, 3B3

CSDA, 3B3

XQ6L, 3B5

XQ7L, 3A5

MXQ6, 3A8

MXQ7, 3B8

REVISIONS					
LTR	ZONE	DESCRIPTION	SIGNATURE AND DATE DFT	CHK	ENGRG
2	-	SEE SHEET 1			

1C2,WCGA
1C7,NCM
1C2,WCGB
2C4,RCS
1D5,$\overline{NDTM}$
1C2,WCGC
RCGC
1C2,WCGD
2D3,$\overline{XCPE}$
2D3,MXQ0
2D3,CLK
2B2,MXQ7
2B2,MXQ6
S175 U28
XPEL, 2D6
XQ0L, 2D3
+12V
U23 1K
LS00 U37
S00 U30
26 U31
S08 U9
S37 U4
LS04 U2
37 U6
LS00 U7
4517 U24
4517 U17
4517 U11
4517 U5
R18 620 1/2W
06 U47
NRZ DATA IN, MASTER
R24 560
R23 560
R26 560
R25 560
R44 680
R43 680
R46 680
R45 680
R20 560
R19 560
R21 560
R22 560
R40 680
R39 680
R41 680
R42 680
1D7,256/512
LS157 U16
+5V
1K U3
LS54 U15
RGA
RGB
RGC
RGD
DATA OUTPUT
GND
TP7
U8 LS04
DATA DESKEW MASTER
RE-INSERT DATA
R6 1K
E28
E27
E26
ECC
STD
154 U25
MASTER
CHAN 9
10
11
12
13
14
15
6
7
8
SYNC INHIBIT
154 U19
2B2,CSAA
2B2,CSBA
2B2,CSCA
2B2,CSDA
R33 33 8,68 READ CLK C
R35 33 9,69 READ CLK D
R34 33 10,70 READ CLK A
R36 33 11,71 READ CLK B
2B2, XQ6L
2B2, XQ7L
R27 33 12,72 READ GATE C
R32 33 13,73 READ GATE D
R28 33 14,74 READ GATE A
R29 33 15,75 READ GATE B
106 CSAA
107 CSBA
108 CSCA
109 CSDA

SIZE	CODE IDENT NO.	1261790-XX
D	92739	
SCALE —		SHEET 3 OF 3

UC-3504A (Rev Aug 67) Printed in U.S.A.

2	-	PRE PRODUCTION RELEASE	4-Dao 5-23-84 WJS 11-5-84 WJS 11-14-84
3	-	REV PER ECR 31327-4 (B)	4-Dao 11-28-84 WJS 11-29-84 WJS 11-29-84

512/256 56
DATA BITSYNC MASTER 51
CLOCK BITSYNC MASTER 52
N CLK
SSW/NSSW 54
FWD/REV 57 FWD
256/512 3C8, 2A8 2D8
+5V R11 R10 R12 R13 R14 1F R15 1K R16 1K R38 1K R41 1K R6 1K R8 1K
TP8 TP11 NSDP TP12 TP10 NSW TP9
IC1 IC2
C13 C14
9638 U36
LS74 CLK U30 U37 U38
LS163 U31
SYNC DETECTOR
LS00 U41
LS04 U27
22 U26
22 U28
28 U21
SLAVE MASTER NRZ COUNTER
LS163 U32 U39
LS86 U40
LS20 U42
LS04 U33
FWD 3C8
SLAVE FLAG
NSWR
FLAG SENSE 3C4
2B8
+5V R7 1K R21 1K R39 1K
1B6 1D7 3B5 3C7 3D5
1B6 1D7
IC7
FB1
C1 .01
C2 22
C3-5,7-9,16-21 .01
C6 .01
C10 .01
1-3,61-63
4-6,64-66, 78-90,92-105, 110-114,118
7,67
GND
+12V

REFERENCE DESIGNATIONS	
LAST REF. DES.	NOT USED
FB1	
C21	
E14	
R41	
TP12	
U42	U23

CAT. ITEM	NEXT ASSY	USED ON	IN	MF	PR CODE
	1261863	HBRECC			

APPLICATION

05	04	03	02	01	ITEM NO	PART NUMBER	EQUIVALENT VENDOR OR MIL PART NUMBER (REF ONLY)	DESCRIPTION	FMC	LONG LEAD ITEM
QUANTITY PER UNIT										
ASSY CONTROL NO.										

PARTS LIST

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES
TOL ± | 2 PLC | 3 PLC | ANG
REMOVE BURRS AND SHARP EDGES YES ☐ NO ☐
DO NOT SCALE THIS PRINT

SIGNATURE		DATE
DRAWN BY	J. Dao	3-23-84
CHK BY		
DFT APPD		
ENGRG APPD		
AUTH BY		

MATERIAL
FINISH

AMPEX HEADQUARTERS Redwood City, California 94063

SCHEMATIC DIAGRAM, SLAVE MASTER DESKEW

SIZE	CODE IDENT NO	
D	92739	1261860-XX

SCALE — SHEET 1 OF 3

1261860-XX

REVISIONS					
LTR	ZONE	DESCRIPTION	SIGNATURE AND DATE DFT	CHK	ENGRG
3	–	SEE SHEET 1	—	—	—

VERSION TABLE

SCHEM NO.	USED WITH ASSY
1261860-01	1261863-01 (INACTIVE)
1261860-02	1261863-02 SHOWN
1261860-03	1261863-03 (11)

(11) -02 VERSION SHOWN, ON -03 VERSION U20 IS REMOVED.

(10) JUMPERS: E9 -E10 HBR WITH ECC
E10-E11 HBR W/O ECC
E12-E13 IN PHASE CLOCK
E13-E14 INVERTED CLOCK

(9) JUMPERS E1-E3, E1-E4, E5-E8 AND E6-E8 ARE NOT USED ON STANDARD HBR APPLICATION.

(8) USED FOR SPECIAL APPLICATION ONLY.

7. IC POWER PINS ARE: GND=7, +5VDC=14, EXCEPT FOR

IC TYPE	GND	+5VDC	+12VDC
74154	12	24	
74LS157	8	16	
74LS163	8	16	
74S175	8	16	
74188A	8	16	
14517	8	—	16
9638	4	1	
74LS174	8	16	
1257149	8	16	

6. INTEGRATED CIRCUITS ARE SN7400N SERIES EXCEPT FOR 14517, 9612E & 1257149.
5. RESISTORS ARE ±5%, 1/4 WATT.
4. CAPACITORS ARE ±10%, 10VDC OR GREATER.
3.
2. ELECTRICAL VALUES ARE IN OHMS & MICROFARADS.
1. REFERENCE ASSEMBLY 1261863-XX.

NOTES UNLESS OTHERWISE SPECIFIED

SIZE	DRAWING IDENT NO	
D	92739	1261860-XX
SCALE —		SHEET 2 OF 3

REVISIONS					
LTR	ZONE	DESCRIPTION	SIGNATURE AND DATE		
			DFT	CHK	ENGRG
3	–	SEE SHEET 1	–	–	–

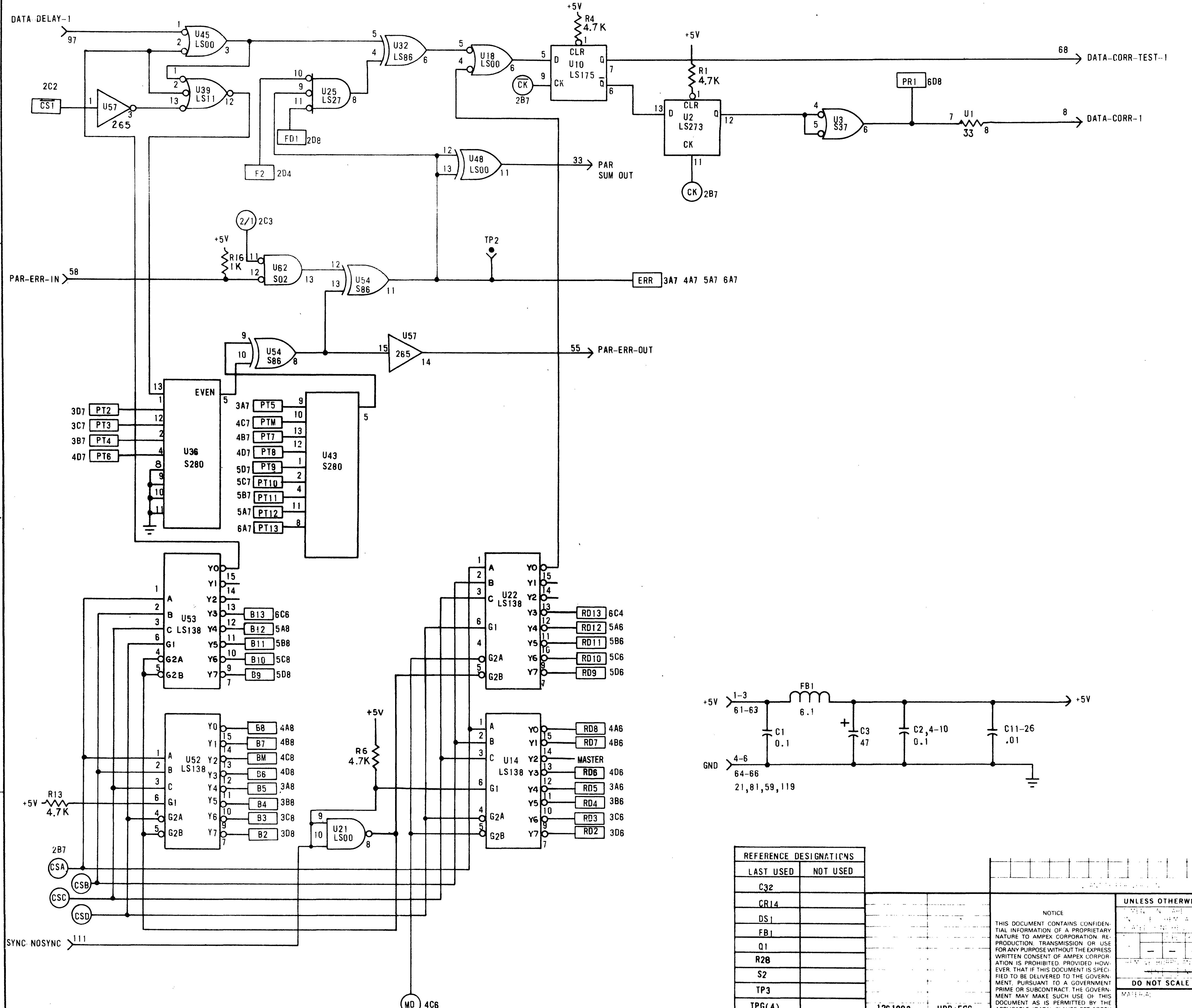
CLOCK-PARALLEL 58
TC-DSKW-M 76
PE-DSKW-M 16
512/256 1D4
FWD 1B4
FWD 1B4
RCLK 2A8
TP1
TP2
TP4
TP5
TP6
TP7
FLAG SENSE 1A8
IC2
R1 220 1/2W C11
R2 1K
R3 220 1/2W C12
R4 1K
R5 1K
R17 R18 C15
R40 1K
DL1 120 40 160 80 200
LS163 U17
LS174 U15
LS174 U22
1257149 U16
S175 U3
S04 U10
S08 U2
S37 U1
S00 U8
Q6 U14
9638 U36
U9 1K
U21 28
LS04 U20
CLOCK-PARALLEL-MASTER (POS) 59
CLOCK-PARALLEL-MASTER (NEG) 60
X CLK (200) DIST, SLAVE MASTER CLK OUT
R20 33
DATA 2C1
CSAA 106
CSBA 107
CSCA 108
ZCSDA 109
RCGC 2B8
RCGD 2A8
RCGA 2D8
RCGB 2C8
ECC E9 E10 E11
R19 1K
+5V (10)
REINSERT DATA
RE-INSERT DATA
SYNC INHIBIT
SYNC INHIBIT
154 U25
154 U13
CHANNEL 1 34
CHANNEL 2 37
CHANNEL 3 35
CHANNEL 4 36
CHANNEL 5 27
CHANNEL 6 41
MASTER NC
CHANNEL 7 26
CHANNEL 8 42
CHANNEL 9 20
CHANNEL 10 47
CHANNEL 11 21
CHANNEL 12 46
CHANNEL 13 22
CHANNEL 14 45
CHANNEL 15 23
CHANNEL 1 24
CHANNEL 2 44
CHANNEL 3 25
CHANNEL 4 43
CHANNEL 5 19
CHANNEL 6 48
MASTER NC
CHANNEL 7 18
CHANNEL 8 49
READ GATE C 12 RGC
RGC 2C3
READ GATE D 13 RGD
RGD 2C3
READ GATE A 14 RGA
RGA 2C3
READ GATE B 15 RGB
RGB 2C3
READ CLK C 8
READ CLK D 9
READ CLK A 10
READ CLK B 11

SIZE	SUBSTITUTE NO.	1261860-XX
D	92739	
SCALE —		SHEET 3 OF 3

1261860-XX

1261900-02 DISTR CODE:

2	PRE-PROD RELEASE	C.F. 12-1-82	WJS 12-12-82



SWITCH	FUNCTION (OFF/ON)
S1-8	CH 1 SELECT (ON = ECC)
S1-7	CH 2 SELECT (ON = ECC)
S1-6	CH 3 SELECT (ON = ECC)
S1-5	CH 4 SELECT (ON = ECC)
S1-4	CH 5 SELECT (ON = ECC)
S1-3	CH 6 SELECT (ON = ECC)
S1-2	CH 7 SELECT (ON = ECC)
S1-1	CH 8 SELECT (ON = ECC)
S2-8	CH 9 SELECT (ON = ECC)
S2-7	CH 10 SELECT (ON = ECC)
S2-6	CH 11 SELECT (ON = ECC)
S2-5	CH 12 SELECT (ON = ECC)
S2-4	TWO/ONE PARITY CH'S
S2-3	
S2-2	A/B BAY
S2-1	ECC ON/OFF

5. IC POWER PINS ARE: GND = 7, +5VDC = 14 EXCEPT FOR:

	GND	+5VDC
LM360	5	8
LS138	8	16
LS175	8	16
LS265	8	16
LS221	8	16
LS151	8	16

4. RESISTORS ARE 5%, 1/4 WATT

3. CAPACITORS ARE 10%, 10VDC OR GREATER

2. ELECTRICAL VALUES ARE IN OHMS AND MICROFARADS

1. REFERENCE ASSEMBLY 1261903-01

NOTES: UNLESS OTHERWISE SPECIFIED:

REFERENCE DESIGNATIONS	
LAST USED	NOT USED
C32	
CR14	
DS1	
FB1	
Q1	
R28	
S2	
TP3	
TPG(4)	
U63	

1261903	HBR/ECC
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED

DO NOT SCALE THIS PRINT

10-2-82
12-2-82
1-13-83

AMPEX
HEADQUARTERS
Redwood City, California 94063

SCHEMATIC DIAGRAM
ERROR CORRECTOR/
DATA REINSERTION

D 92739 1261900-02

1 OF 6

TR	ZONE	REVISIONS DESCRIPTION	SIGNATURE AND DATE DAT	CHK	ENGRG
2	-	SEE SHEET ONE	—	—	—

1D7

FLAG-DET-1 82 FD1 13 → 14 → 12 → 16 R7 1K TP1 FLAG 1 IN 56

FLAG. DET-2 83 FD2 3D7 11 → 12 → 10

FLAG-DET-3 84 FD3 3C7 9 → 10 → 8

FLAG-DET-4 85 FD4 3B7 1 → 15 → 2 U17 O7

FLAG-DET-5 86 FD5 3A7 3 → 13 → 6

FLAG-DET-6 87 FD6 4D7 5 → 11 → 12

FLAG-DET-M 88 FDM 4C7 13 → 3 → 12 U31 O7

FLAG-DET-7 89 FD7 4B7 11 → 5 → 10

FLAG-DET-8 90 FD8 4A7 9 → 8 → 8

FLAG-DET-9 91 FD9 5D7 1 → 1 → 2

FLAG-DET-10 92 FD10 5C7 3 → 4 → 4

FLAG-DET-11 93 FD11 5B7 5 → 6 → 6

FLAG-DET-12 94 FD12 5A7 13 → U38 O7 12 → 2 → U24 390X14

FLAG-DET-13 95 FD13 6C5 11 → U38 O7 10 → 7 → 1D5

+5V R12 1K → U60 10 (9, 11 → 8)

ECC ON/OFF 114 → U38 O7 (1 → 2) +5V R22 1K → S2-1 ON / OFF CORRECTION → U60 10 (3, 4, 5 → 6)

TP3 FLAG-2 → 1D7,3A7,4D7,5D7,6A7 F2

+5V R9 4.7K → FLAG 1-OUT-MON 34

U59 LM360 (2, 3, 4, 7, 6)

+5V R21 68.1 1% R20 45.3 1% C25 .01

-5V 35

U57 265 (12, 11 → 10) → 53 FLAG-1-OUT → U38 O7 (5 → 6)

FLAG-2-IN 57

U38 O7 (9 → 8) +5V R29 4.7K → FLAG-2-OUT-MON 32

U58 LM360 (2, 3, 4, 7, 6)

+5V R19 110 1% R18 36.5 1%

U38 O7 (3 → 4) +5V R10 4.7K → 54 FLAG-2-OUT

U61 221 (10 B, 9 A, 11 CLR, 5 Q, 6 C30 47, 7 CR14)

+5V R14 330 → R24 130 → R23 20 → 52 FLAG-TO-MSP

+5V R13 REF → R25 47K → R15 47K

C29 47UF (14) CR13 (15) → U61 221 (2 B, 1 A, 3 CLR, 4 Q̄) → DS1 → +5V R27 390 → (2 1) 1D7

51 PAR RETEST IN

+5V U56 4.7K (16, 2) U23 O2 (12, 11, 13) S2-4 TWO / ONE PARITY → PR 6B8

P 13 → 49 TWO ONE PARITY

CS1 1D8 6D8 → CR6 S1-8 6 → 4.7K → A 1 → 36 AUTO-SEL-1

CS11 5B8 6C8 → CR2 S2-5 1 → 4.7K → N 12 → 47 AUTO-SEL-12

CS10 5C8 6C8 → CR1 S2-6 3 → 4.7K → M 11 → 46 AUTO-SEL-11

CS9 5D8 6C8 → CR12 103 S2-7 4 → 4.7K U56 → L 10 → 45 AUTO-SEL-10

CS8 4A8 6C8 → CR8 92-8 5 → 4.7K → K 9 → 44 AUTO-SEL-9

CS7 4B8 6C8 → CR7 S1-1 9 → 4.7K → J 8 → 43 AUTO-SEL-8

CS6 4D8 6D8 → CR9 S1-2 10 → 4.7K → H 7 → 42 AUTO-SEL-7

CS5 3A8 6D8 → CR10 S1-3 15 → 4.7K → F 6 → 41 AUTO-SEL-6

CS4 3B8 6D8 → CR11 S1-4 14 → 4.7K → E 5 → 40 AUTO-SEL-5

CS3 3C8 6D8 → CR3 S1-5 13 → 4.7K → D 4 → 39 AUTO-SEL-4

CS2 3D8 6D8 → CR4 S1-6 12 → 4.7K → C 3 → 38 AUTO-SEL-3

CR5 S1-7 11 → 4.7K → B 2 → 37 AUTO SEL-2

8 4.7K U56

C28 .01 Q1 → 112 MAN AUTO SELECT

C27 .01

"A" S2-2 "B" BAY SELECT +5V R26 1K → U62 SO2 (8, 9, 2, 3 → 1)

CS12 5A8 → U48 LS00 (9, 10 → 8) → U50 LS04 (5 → 6) → CS12 6C8 CH 12 SELECT

+5V R28 4.7K → U54 LS86 (5, 4 → 6) → U60 10 (1, 2 → 12) → CS13 6D8 CH 13 SELECT

U54 LS86 (2, 1 → 3) → SF 4C8

U49 LS11 (11, 10, 9 → 8) → 113 SERIAL FLAG

+5V U56 4.7K (16 → 7)

CSD CSC CSB CSA 1A8

CSAA 115, CSBA 116, CSCA 117, CSDA 118 → U51 LS175 (5, 4, 12, 13 → 7, 2, 10, 15; CLK 9)

U63 151 (D0 4, D1 3, D2 2, D3 1, D4 15, D5 14, D6 13, D7 12; Y 5, W 6, S 7, A 11, B 10, C 9)

U55 151 (D0 4, D1 3, D2 2, D3 1, D4 15, D5 14, D6 13, D7 12; Y 5, W 6, S 7, A 11, B 10, C 9)

U62 SO2 (5, 6 → 4)

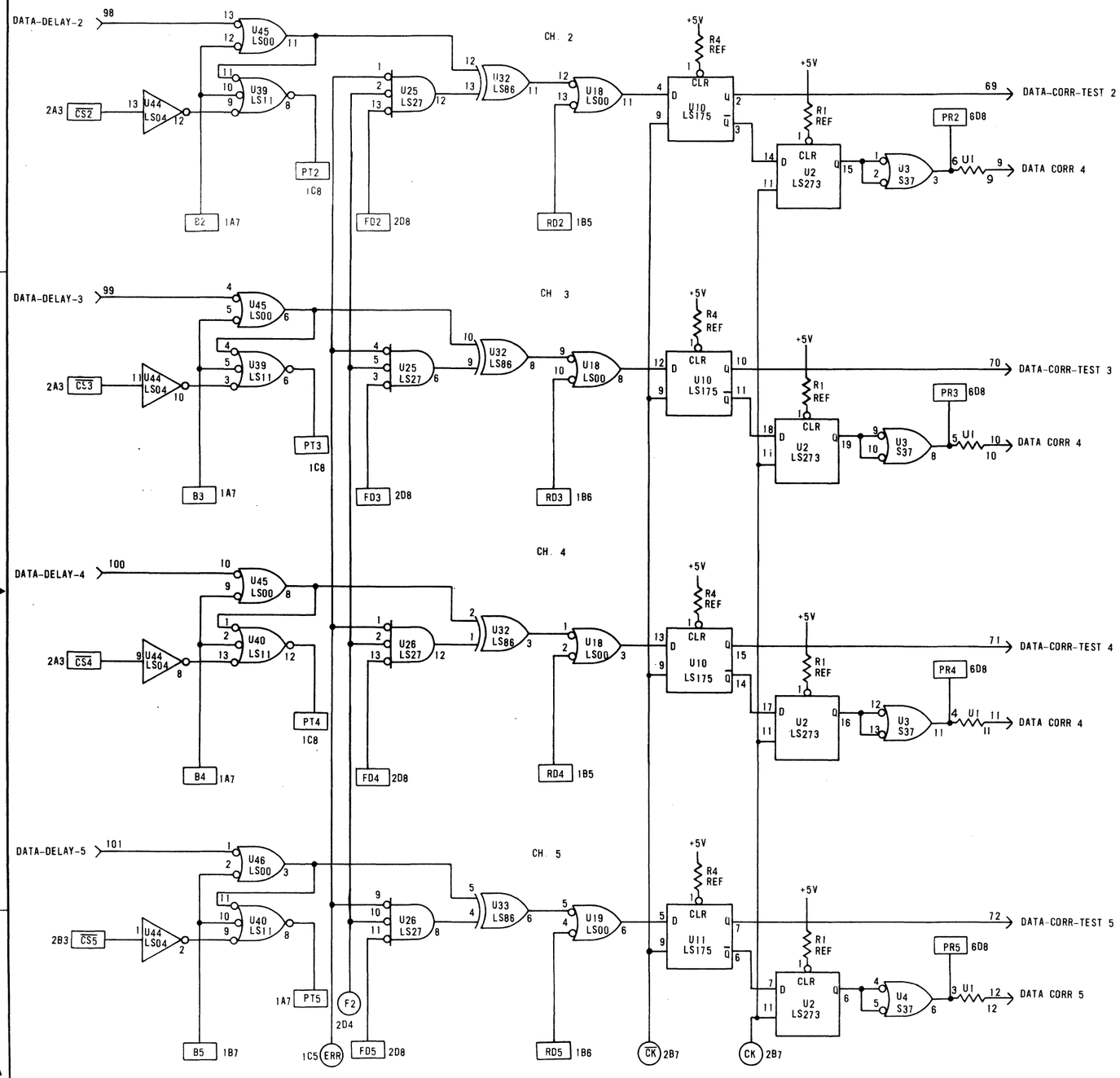
CLK-PAR-MASTER (POS) 60, 120 → U57 265 (4, 5 → 6, 7) +5V R17 4.7K

CK 1D5, 3A5, 4A5, 5A5, 6A5

C̄K 1D6, 3A6, 4A6, 5A6, 6A6

SIZE	CODE IDENT NO	
D	92739	1261900-02
SCALE —		SHEET 2 OF 6

REVISIONS					
LTR	ZONE	DESCRIPTION	SIGNATURE AND DATE DFT	CHK	ENGR
2	..	SEE SHEET ONE	–	–	–



REVISIONS					
LTR	ZONE	DESCRIPTION	SIGNATURE AND DATE		
			DFT	CHK	ENGR
2		SEE SHEET ONE	—	—	—

DATA DELAY 6 102
U46 LS00
U40 LS11
2B3 CS6
U44 LS04
B6 1B7
1C8 PT6
CHAN 6
U26 LS27
FD6 2C8
U33 LS86
RD6 1B5
U19 LS00
+5V
R4 REF
U11 LS175
CLR
R1 REF
U2 S273
PR6 6C8
U4 S37
U1 13
73 DATA CORR TEST 6
DATA CORR 6

DATA DELAY M 103
U46 LS00
U41 LS11
2B5 SF
BM 1B7
1A7 PTM
CHAN M
U27 LS27
FDM 2C8
U33 LS86
1A6 MD
U19 LS00
R8 4.7K
U11 LS175
U4 S37
U16 33Ω
31 DATA-CORR-M

DATA DELAY 7 104
U46 LS00
U41 LS11
2B3 CS7
U44 LS04
G7 1B7
1A7 PT7
CHAN 7
U27 LS27
FD7 2C8
U33 LS86
RD7 1B6
U19 LS00
U11 LS175
U2 LS273
PR7 6C8
U4 S37
U1 14
74 DATA CORR TEST 7
DATA CORR 7

DATA DELAY 8 105
U47 LS00
U41 LS11
2B3 CS8
U50 LS04
B8 1B7
1A7 PT8
1C5 ERR
F2 2D4
CHAN 8
U27 LS27
FD8 2C8
U34 LS86
RD8 1B5
U20 LS00
CK 2B7
U12 LS175
U7 LS273
PR8 6C8
U5 S37
U16 2
75 DATA CORR TEST 8
DATA CORR 8

1261900-02

SIZE	DRAWING NO.	REV
D	92739	1261900-02
SCALE —		SHEET 4 OF 6

REVISIONS					
LTR	ZONE	DESCRIPTION	SIGNATURE AND DATE DFT	CHK	ENGR
2		SEE SHEET ONE	—	—	—

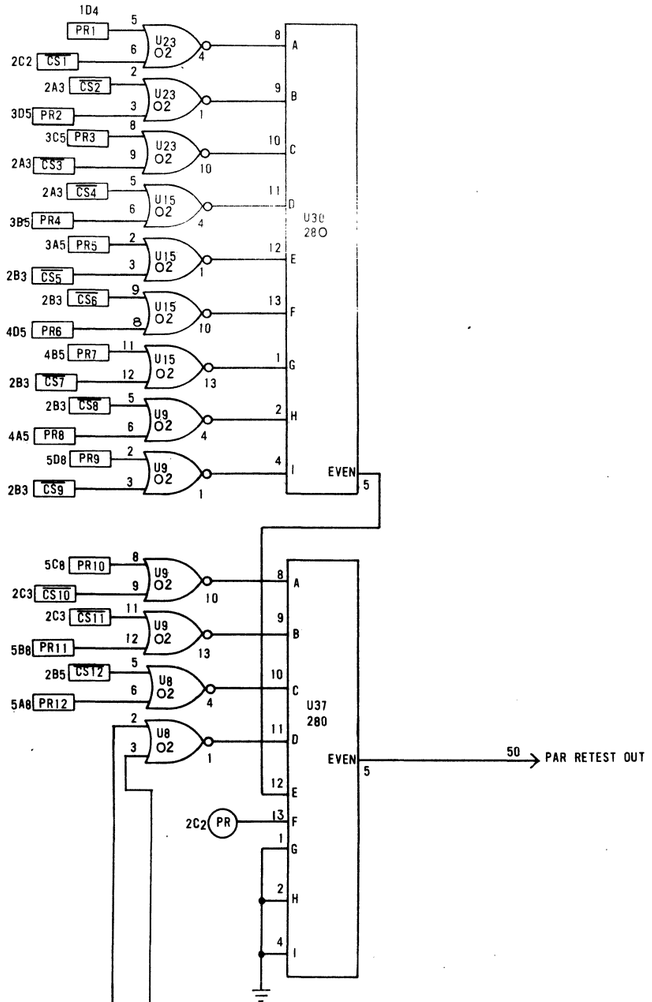
DATA DELAY 9 106
U47 LS00
U42 LS11
U50 LS04
2B3 CS9
B9 1B7
U28 LS27
FD9 2C8
U34 LS86
U20 LS00
RD9 1A5
1A7 PT9
CHAN 9
+5V
R4 REF
U12 LS175
R2 4.7K
U7 LS273
U5 S37
PR9 6C8
U16
76 DATA CORR TEST 9
DATA CORR 9

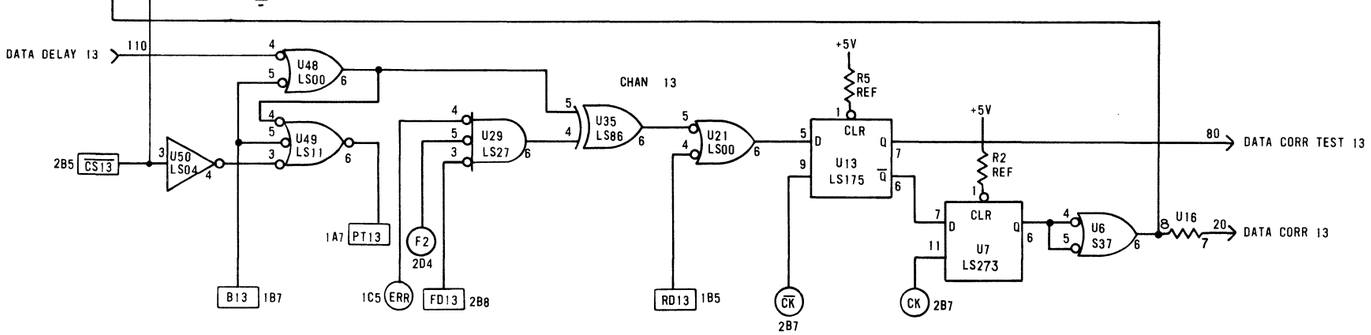
DATA DELAY 10 107
U47 LS00
U42 LS11
U50 LS04
2C3 CS10
B10 1B7
U28 LS27
FD10 2B8
U34 LS86
U20 LS00
RD10 1A6
1A7 PT10
CHAN 10
+5V
R4 REF
U12 LS175
R2 REF
U7 LS273
U5 S37
PR10 6C8
U16
77 DATA CORR TEST 10
DATA CORR 10

DATA DELAY 11 108
U47 LS00
U42 LS11
U50 LS04
2C3 CS11
B11 1B7
U28 LS27
FD11 2B8
U34 LS86
U20 LS00
RD11 1A5
1A7 PT11
CHAN 11
+5V
R4 REF
U12 LS175
R2 REF
U7 LS273
U5 S37
PR11 6C8
U16
78 DATA CORR TEST 11
DATA CORR 11

DATA DELAY 12 109
U48 LS00
U49 LS11
2C6 CS12
B12 1B7
U29 LS27
FD12 2B8
U35 LS86
U21 LS00
RD12 1B6
1A7 PT12
F2 2D4
1A5 ERR
CHAN 12
+5V
R5 4.7K
R2 REF
U13 LS175
U7 LS273
U6 S37
PR12 6B8
U16
CK 2B7
CK 2B7
79 DATA CORR TEST 12
DATA CORR 12

			SIGNATURE AND DATE		
			DFT	PD	ENGRG
2		SEE SHEET ONE	—	—	—

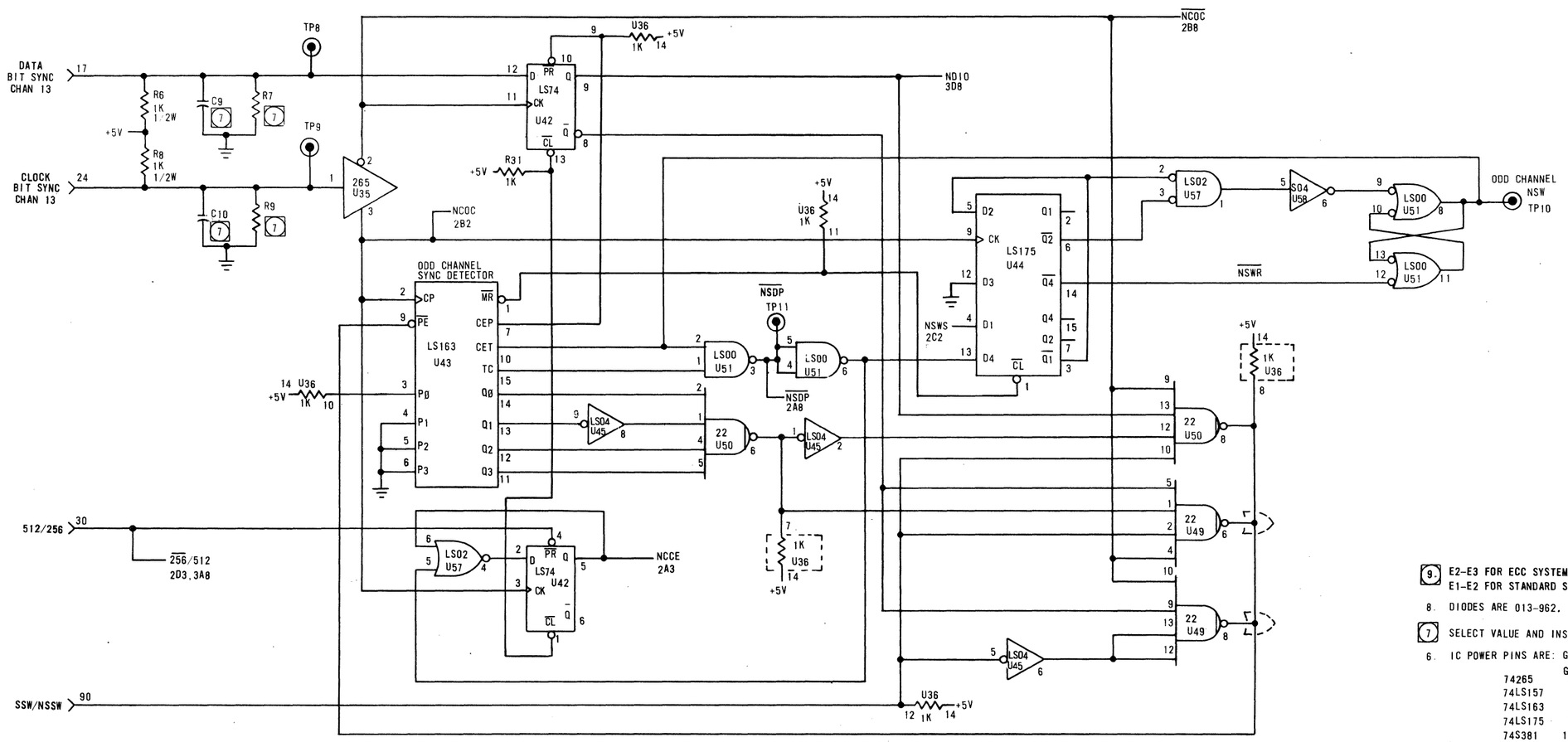




D	92739	1261900-02	
	—		SHEET 6 OF 6

1261900-02

ZONE		SIGNATURE AND DATE
4	– PRE-PRODUCTION RELEASE	ENGRG: CF 10-23-82



9. E2-E3 FOR ECC SYSTEM.
E1-E2 FOR STANDARD SYSTEM.

8. DIODES ARE 013-962.

7. SELECT VALUE AND INSTALL AT TEST IF REQUIRED.

6. IC POWER PINS ARE: GND=7, +5VDC=14 EXCEPT FOR

	GND	+5VDC	+12VDC
74265	8	16	–
74LS157	8	16	–
74LS163	8	16	–
74LS175	8	16	–
74S381	10	20	–
4517	8	–	16
74LS194	8	16	–

5. INTEGRATED CIRCUITS ARE SN7400N SERIES EXCEPT FOR 14517.

4. RESISTORS ARE 5%, 1/4 WATT.

3. CAPACITORS ARE 10%, 10VDC OR GREATER.

2. ELECTRICAL VALUES ARE IN OHMS & MICROFARADS.

1. REFERENCE ASSEMBLY 1262013-02.

NOTES: UNLESS OTHERWISE SPECIFIED

1262010-02

REFERENCE DESIGNATIONS	
LAST USED	NOT USED
C10	
R31	
S1	
TP12	
U62	

CAT. ITEM	NEXT ASSY	USED ON	IN	MF	PR CODE
APPLICATION	1262013	HBR/ECC			

05	04	03	02	01	ITEM NO.	PART NUMBER	EQUIVALENT VENDOR OR MIL PART NUMBER (REF ONLY)	DESCRIPTION	FMC	LONG LEAD ITEM
QUANTITY PER UNIT										
ASSY CONTROL NO.										

PARTS LIST

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES
TOL ± | 2 PLC | 3 PLC | ANG
REMOVE BURRS AND SHARP EDGES YES ☐ NO ☐
DO NOT SCALE THIS PRINT

MATERIAL
FINISH:

SIGNATURE		DATE
DRAWN BY	C. Fu	2/20/82
CHK BY	W.J. Shuttleworth	11/22/82
INT APPD		
ENGRG APPD	J. Ruiz	11-24-82
AUTH BY	J.A. Villar	Mar 82

AMPEX HEADQUARTERS Redwood City, California 94063

SCHEMATIC DIAGRAM,
AUTO CHANNEL SELECT

SIZE	CODE IDENT NO	
D	92739	1262010-02

SCALE NONE | SHEET 1 OF 4

UC 3504.03 (3-74) PRINTED IN U.S.A.

REVISIONS					
LTR	ZONE	DESCRIPTION	SIGNATURE AND DATE DFT	CHK	ENGRG
4	—	SEE SH 1	—	—	—

ODD CHANNEL NUMBER PROGRAM INPUTS

PRG 0 (26)
PRG 1 (27)
PRG 2 (28)
PRG 3 (29)
FWD/REV (57)

+5V
1K U36 (6 3 4 1)
R10 1K
+5V
FWD 2B3

U58 S04

LS86 U29 (x4)

S381 U37
B0 B1 B2 B3 C IN
A0 A1 A2 A3
Σ0 Σ1 Σ2 Σ3
S2 S1 S0
U39 1K +5V
1K U36 +5V

U45 LS04 (x6)
U30 LS86 (x4)
U31 LS08 (x3)

SNQ4

U38 LS85
A0 A1 A2 A3 B0 B1 B2 B3
A=B

U36 1K +5V
512/256 1B8
U23 LS00
FWD 2B8
U30 LS86
U31 LS08
NSWS 1C5

NCOC 1D3
NSDP 1C5

ODD CHANNEL NRZ COUNTER
LS163 U53
CP PE MR CEP CET TC P0 P1 P2 P3 Q0 Q1 Q2 Q3
SNQ3

LS163 U46
CP PE MR CEP CET TC P4 P5 P6 P7 Q4 Q5 Q6 Q7
CTR 0 CTR 1 CTR 2 CTR 3
SNQ5 SNQ6 SNQ7
ODD CHANNEL NRZ COUNTER

U36 1K +5V
ODD CHANNEL NCCE 1B6

TP12

SNQ6 SNQ7
LS10 U60
WCB 3C8
NCOC 1C6
WCD 3A8
SNQ7

SNQ6
LS10 U59
WCC 3B8
WCA 3C8

SIZE	CODE IDENT NO	
D	92739	1262010 - 02
SCALE —		SHEET 2 OF 4

REVISIONS					
LTR	ZONE	DESCRIPTION	SIGNATURE AND DATE		
			DFT	CHK	ENGRG
4	—	SEE SH 1	—	—	—

+12V
R5
620
1/2W

NDI0
1D4

U17
06

4517
U4

R26
560
R25
560
R17
680
R18
680
R3
510

WCA
2A2
READ CLK A
10, 70

26
U7

4517
U3

R22
560
R21
560
R15
680
R16
680
R4
510

WCB
2B2
READ CLK B
11, 71

NRZ DATA IN,
ODD CHANNEL

4517
U1

R24
560
R19
560
R11
680
R13
680

WCC
2A2
READ CLK C
8, 68

4517
U2

R20
560
R23
560
R12
680
R14
680
R1
510

WCD
2B2
READ CLK D
9, 69

R2
510

512/256
1B8

LS157
U8

READ GATE B
15
75

READ GATE A
14, 74

READ GATE C
12, 72

READ GATE D
13, 73

LS54
U16

TP6
DATA PLUS SYNC

+5V
U39 REF
1K

HIVB
4D5

REINSERTED
DATA
20

SYNC INHIBIT
16

LS00
U23

LS74
U24

R29
1K

S37
U22

19 DATA-DSKW-ODD

25 DATA-PAR-DSKW-ODD

CLK-PAR-DLY
60

DMCI

S04
U58

E1
E2
E3

TP7
DATA

CLK
4C8

1262010-02

SIZE	CODE IDENT NO	
D	92739	1262010-02
SCALE —		SHEET 3 OF 4

REVISIONS					
LTR	ZONE	DESCRIPTION	SIGNATURE AND DATE DFT	CHK	ENGRG
4	-	SEE SHT 1	-	-	-

M.C. DATA IN 33
CH 14 SYNC TIME 35
CLK 3B1
A8 CSDB 56
ECC ON/OFF 51
HIVB 3C2
MANUAL
AUTO
+5V
U27 LS175
U11 LS112
U18 LS175
U19 LS51
U20 LS32
U26 LS86
U35 265
U39 1K
U12 04
U32 LS11
U25 LS163
U33 LS194
U40 LS194
U47 LS194
U34 LS194
U41 LS194
U48 LS194
U13 LS08
R27 1K
R28 1K
R30 1K
TP1
TP2
TP3
TP4
TP5
7405
DS1
DS2
DS3
36 CHAN 1
37 CHAN 2
38 CHAN 3
39 CHAN 4
40 CHAN 5
41 CHAN 6
42 CHAN 7
43 CHAN 8
44 CHAN 9
45 CHAN 10
46 CHAN 11
47 CHAN 12
58 MANAUL/AUTO CHAN SELECT

SIZE	CODE IDENT NO	
D	92739	1262010-02
SCALE —		SHEET 4 OF 4