SERVICE MANUAL

1611A LOGIC STATE ANALYZER

HEWLETT PACKARD

HP 1611A

SAFETY

This product has been designed and tested according to International Safety Requirements. To ensure safe operation and to keep the product safe, the information, cautions, and warnings in this manual must be heeded. Refer to Section I and the Safety Summary for general safety considerations applicable to this product.

CERTIFICATION

Hewlett-Packard Company certifies that this product met its published specifications at the time of shipment from the factory. Hewlett-Packard further certifies that its calibration measurements are traceable to the United States National Bureau of Standards, to the extent allowed by the Bureau's calibration facility, and to the calibration facilities of other International Standards Organization members.

WARRANTY

This Hewlett-Packard product is warranted against defects in material and workmanship for a period of one year from date of shipment. During the warranty period, Hewlett-Packard Company will, at its option, either repair or replace products which prove to be defective.

The cathode-ray tube (CRT) in the instrument and any replacement CRT purchased from HP are also warranted against electrical failure for a period of one year from the date of shipment from Colorado Springs. BROKEN TUBES AND TUBES WITH PHOSPHOR OR MESH BURNS, HOWEVER, ARE NOT INCLUDED UNDER THIS WARRANTY.

For warranty service or repair, this product must be returned to a service facility designated by HP. However, warranty service for products installed by HP and certain other products designated by HP will be performed at Buyer's facility at no charge within the HP service travel area. Outside HP service travel areas, warranty service will be performed at Buyer's facility only upon HP's prior agreement and Buyer shall pay HP's round trip travel expenses.

For products returned to HP for warranty service, Buyer shall prepay shipping charges to HP and HP shall pay shipping charges to return the product to Buyer. However, Buyer shall pay all shipping charges, duties, and taxes for products returned to HP from another country.

LIMITATION OF WARRANTY

The foregoing warranty shall not apply to defects resulting from improper or inadequate maintenance by Buyer, Buyer-supplied software or interfacing, unauthorized modification or misuse, operation outside of the environmental specifications for the product, or improper site preparation or maintenance.

NO OTHER WARRANTY IS EXPRESSED OR IMPLIED. HP SPECIFICALLY DISCLAIMS THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.

EXCLUSIVE REMEDIES

THE REMEDIES PROVIDED HEREIN ARE BUYER'S SOLE AND EXCLUSIVE REMEDIES. HP SHALL NOT BE LIABLE FOR ANY DIRECT, INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES, WHETHER BASED ON CONTRACT, TORT, OR ANY OTHER LEGAL THEORY.

ASSISTANCE

Product maintenance agreements and other customer assistance agreements are available for Hewlett-Packard products.

For any assistance, contact your nearest Hewlett-Packard Sales and Service Office. Addresses are provided at the back of this manual.

S C W & A 9/78 (CRT)

SERVICE MANUAL

MODEL 1611A
LOGIC STATE ANALYZER

SERIAL NUMBERS

This manual applies directly to instruments with serial numbers prefixed **2017A.**

With changes described in Section VII, this manual also applies to instruments with serial numbers prefixed **2007A** thru **1635A.**

For additional information about serial numbers, see INSTRUMENTS COVERED by MANUAL in Section I.

Manual Part Number 01611-90909
Microfiche Part Number 01611-90809

PRINTED: JULY 1980

SAFETY SUMMARY

The following general safety precautions must be observed during all phases of operation, service, and repair of this instrument. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of the instrument. Hewlett-Packard Company assumes no liability for the customer's failure to comply with these requirements.

GROUND THE INSTRUMENT.

To minimize shock hazard, the instrument chassis and cabinet must be connected to an electrical ground. The instrument is equipped with a three-conductor ac power cable. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet. The power jack and mating plug of the power cable meet International Electrotechnical Commission (IEC) safety standards.

DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE.

Do not operate the instrument in the presence of flammable gases or fumes. Operation of any electrical instrument in such an environment constitutes a definite safety hazard.

KEEP AWAY FROM LIVE CIRCUITS.

Operating personnel must not remove instrument covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

DO NOT SERVICE OR ADJUST ALONE.

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

USE CAUTION WHEN EXPOSING OR HANDLING THE CRT.

Breakage of the Cathode-ray Tube (CRT) causes a high-velocity scattering of glass fragments (implosion). To prevent CRT implosion, avoid rough handling or jarring of the instrument. Handling of the CRT shall be done only by qualified maintenance personnel using approved safety mask and gloves.

DO NOT SUBSTITUTE PARTS OR MODIFY INSTRUMENT.

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the instrument. Return the instrument to a Hewlett-Packard Sales and Service Office for service and repair to ensure that safety features are maintained.

DANGEROUS PROCEDURE WARNINGS.

Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

WARNING

Dangerous voltages, capable of causing death, are present in this instrument. Use extreme caution when handling, testing, and adjusting.

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LIST OF ILLUSTRATIONS

LIST OF TABLES

SECTION I

GENERAL INFORMATION

1-1. INTRODUCTION.

1-2. This Operating and Service Manual contains information required to install, operate, test, adjust, and service the Hewlett-Packard Model 1611A Logic State Analyzer.

1-3. In addition to this manual, an Operating and Service Supplement for each microprocessor personality module option or accessory ordered with the instrument is also provided.

1-4. Listed on the title page of this manual is a microfiche part number. This number can be used to order 4- x 6-inch microfilm transparencies of the manual. Each microfiche contains up to 96 photo-duplicates of the manual pages. The microfiche package also includes the latest Manual Changes supplement.

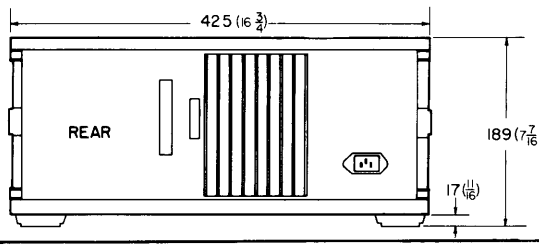
1-5. SPECIFICATIONS. Complete instrument performance specifications are listed in the personality module Operating and Service Supplement for each microprocessor option and accessory ordered with the instrument. These specifications are the performance standards or limits against which the instrument is tested. Detailed performance tests are also included in the personality module Operating and Service Supplement.

1-6. Table 1-1 lists supplemental characteristics of the 1611A which are not performance specifications but are typical characteristics included as additional information to the user.

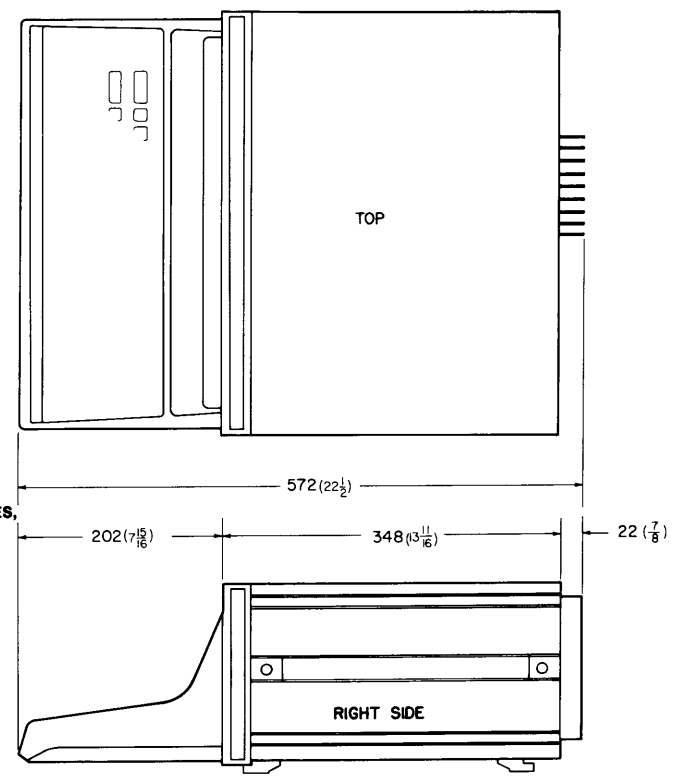
Table 1-1. Supplemental Characteristics

CONNECTION BETWEEN μP and 1611A INPUT BUFFERS: one 40 pin dual in-line package connector with 30.5 cm (12 in.) cable, one 40 pin male socket with 30.5 cm (12 in.) cable, or one 40 pin male socket with 7.6 cm (3 in.) cable.
MEMORY DEPTH: 64 memory transactions; 16 lines are displayed at one time, roll keys permit viewing all 64 transactions.
TIME INTERVAL: accuracy, 0.1% ±1 μs. Maximum time, 2^{24}—1 μs (16.7 seconds).
EVENTS COUNT: 2^{24}—1 events (16.7 million) max.
LOGIC PROBE OUTPUT POWER: 5 V dc at 0.1 A max.
POWER: 100, 120, 220, 240 V ac; —10% +5%; 48 to 440 Hz; 120 VA max.
DIMENSIONS: see outline drawings.
OPERATING ENVIRONMENT
Temperature: 0°C to 55°C.
Humidity: up to 95% relative humidity at 40°C.
Altitude: to 4600 m (15 000 ft).

NOTES: 1. DIMENSIONS ARE FOR GENERAL INFORMATION ONLY. IF DIMENSIONS ARE REQUIRED FOR BUILDING SPECIAL ENCLOSURES, CONTACT YOUR HP FIELD ENGINEER.
2. DIMENSIONS ARE IN MILLMETRES AND (INCHES).



Vibration: vibrated in three planes for 15 min. each with 0.38 mm (0.015 in.) excursions, 10 to 55 Hz.
WEIGHT: net, 15 kg (33 lb); shipping, 19.5 kg (43 lb).



1-7. INSTRUMENTS COVERED BY MANUAL.

1-8. Attached to the instrument is a serial number plate. The serial number is in the form: 0000A00000. It is in two parts; the first four digits and the letter are the serial prefix and the last five digits are the suffix. The prefix is the same for all identical instruments; it changes only when a change is made to the instrument. The suffix however, is assigned sequentially and is different for each instrument. The contents of this manual apply to instruments with the serial number prefix(es) listed under SERIAL NUMBERS on the title page.

1-9. An instrument manufactured after the printing of this manual may have a serial number prefix that is not listed on the title page. This unlisted serial number prefix indicates the instrument is different from those described in this manual. The manual for this newer instrument is accompanied by a yellow Manual Changes supplement. This supplement contains "change information" that explains how to adapt the manual to the newer instrument.

1-10. In addition to change information, the changes supplement may contain information for correcting errors in the manual. To keep this manual as current and accurate as possible, Hewlett-Packard recommends that you periodically request the latest Manual Changes supplement. The supplement for this manual is identified with the manual print date and part number, both of which appear on the manual title page. Complimentary copies of the supplement are available from Hewlett-Packard.

1-11. For information concerning a serial number prefix that is not listed on the title page or in the Manual Changes supplement, contact your nearest Hewlett-Packard office.

1-12. DESCRIPTION.

1-13. The HP 1611A Logic State Analyzer is dedicated to the design and troubleshooting of microprocessor based systems. For ease-of-use, a special probe offers two methods of connection to microprocessors —a dual in-line clip and a connector plug for interfacing with microprocessors in sockets. Measurements of system activity are displayed on the analyzer's CRT screen in selectable mnemonic or absolute codes of the microprocessor's own instruction set. The display is divided into three distinct fields—address, data, and external. Events and activity displayed in the address and op code/data fields are collected directly from the system microprocessor's address and data buses. An additional eight bits of binary information gathered by auxiliary probes is displayed in the external field.

1-14. With relational triggering capabilities, the 1611A permits framing of a real-time data window around virtually any event or set of related events—any desired sequence of system operations. The 1611A will also measure execution time or count selected events between two keyboard selected events. At a desired point, defined from a keyboard entry, the 1611A can be commanded to halt microprocessor operation; then, if desired, it can control the following transactions in single or multiple keyed steps. Keyboard entry of address or data bus trigger words may be entered in either octal or hexadecimal notation and the external trigger information is entered in binary format.

1-15. For increased confidence of instrument operation, it performs a self-test during the turn-on period and indicates test results on the CRT. The microprocessor probe data-gathering circuits may also be checked by connecting the probe to the front panel probe test socket with the test results displayed on the CRT.

1-16. OPTIONS.

1-17. The following options for the 1611A are available to configure the instrument for specific microprocessors and are covered by separate Manual Supplements.

Option A68: Model 1611A with Model 10257B Personality Module for use with any microprocessor that meets specifications of the Motorola 6800.

Option A80: Model 1611A with Model 10258B Personality Module for use with any microprocessor that meets specifications of the Intel 8080A.

Option 0F8: Model 1611A with Model 10259A Personality Module for use with any microprocessor that meets specifications of the Fairchild F8.

Option Z80: Model 1611A with Model 10260A Personality Module for use with any microprocessor that meets specifications of the Zilog Z80.

Option A65: Model 1611A with Model 10261A Personality Module for use with any microprocessor that meets specifications of the Rockwell R6502A.

Option A18: Model 1611A with Model 10262A Personality Module for use with any microprocessor that meets specifications of the RCA 1802.

Option A85: Model 1611A with Model 10263A Personality Module for use with any microprocessor that meets specifications of the Intel 8085.

1-18. ACCESSORIES SUPPLIED.

1-19. The following accessories are supplied with the 1611A:

External 8-bit Probe, HP Part No. 01611-62101

One Extender Board, HP Part No. 01611-66515
One 2.3 m (7.5 ft) Power Cord (refer to Section II)
One Accessory Bag, HP Part No. 1540-0325
One Keyboard Cover, HP Part No. 5040-0588

1-20. ACCESSORIES AVAILABLE.

1-21. The following accessories are available for the 1611A:

Model 10257B Personality Module (6800)
Model 10258B Personality Module (8080)
Model 10259A Personality Module (F8)
Model 10260A Personality Module (Z80)
Model 10261A Personality Module (6502)
Model 10262A Personality Module (1802)
Model 10263A Personality Module (8085)

1-22. RECOMMENDED TEST EQUIPMENT.

1-23. Equipment required to maintain the Model 1611A is listed in table 1-2. Other equipment may be substituted if it meets or exceeds the critical specifications listed in the table.

Table 1-2. Recommended Test Equipment

Instrument	Critical Specification	Recommended Model	Use*
Pulse Generators (2)	10 V output into 50 ohms, External trigger, 0 to +2.5 V DC offset, 0 to 1.4μs adjustable delay	HP 8013B	P
Digital Voltmeter	±1000 Vdc range, 0.1% accuracy	HP 3465A	P, A, T
Dual Channel Oscilloscope	50 MHz BW min	HP 1740A	P, T
Logic State Analyzer	Pattern recognition and state display	HP 1600A	T
Logic Pulser	Pulse logic circuits	HP 10526T	T
Logic Probe	Monitor digital IC's	HP 10525T	T
50Ω Feedthroughs (2)	50Ω feedthrough termination	HP 10100C	P
BNC-to-alligator Clip Adapters (3)		HP Part No. 8120-1292	P
BNC Tee Connectors (2)		HP Part No. 1250-0781	P
Current Tracer		HP 547A	T
Signature Analyzer	No Substitute	HP 5004A	T

*P=Performance Test; A=Adjustment, T=Troubleshooting

SECTION II

INSTALLATION

2-1. INTRODUCTION.

2-2. This section contains information and instructions for installing the Model 1611A. Included are initial inspection procedures, power and grounding requirements, and instructions for repacking for shipment.

2-3. INITIAL INSPECTION.

2-4. Inspect the shipping container for damage. If the shipping container or cushioning material is damaged, it should be kept until contents of the shipment have been checked for completeness and the instrument has been checked mechanically and electrically. Procedures for checking electrical performance are given in Section IV. If the contents are incomplete, if there is mechanical damage or defect, or if the instrument does not pass the Performance Tests, notify the nearest Hewlett-Packard office. If the shipping container is damaged, or the cushioning material shows signs of stress, notify the carrier as well as the Hewlett-Packard office. Keep the shipping materials for carrier's inspection. The HP office will arrange for repair or replacement at HP option without waiting for claim settlement.

2-5. PREPARATION FOR USE.

2-6. POWER REQUIREMENTS. The 1611A requires a power source of 100, 120, 220, or 240 Vac, —10%, +5%; single-phase; 48 to 440 Hz; 120 VA maximum.

CAUTION

The instrument may be damaged if the LINE SELECTOR switch setting does not match the input power source.

2-7. LINE VOLTAGE SELECTION. The LINE SELECTOR switches on the rear panel select either 100-, 120-, 220-, or 240-volt operation. To check or change positions of the LINE SELECTOR switches, proceed as follows:

a. Remove input power cord (if connected).

b. For 100- or 120-volt operation, set LINE SELECTOR switches to 100 V or 120 V respectively.

c. For 220- or 240-volt operation, set LINE SELECTOR switches to 220 V or 240 V respectively.

d. Reconnect power cord.

2-8. POWER CABLE. This instrument is equipped with a three-wire power cable. When connected to an appropriate ac power receptacle, this cable grounds the instrument cabinet. The type of power cable plug shipped with each instrument depends on the country of destination. Refer to figure 2-1 for the part numbers of the power cable and plug configurations available.

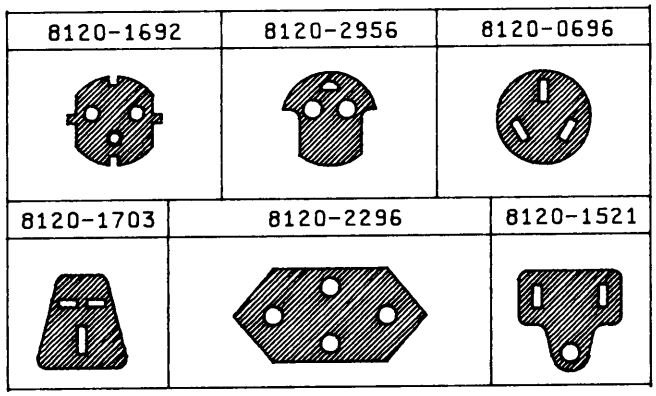


Figure 2-1. Power Cables Available

2-9. PROBE INSTALLATION. To install the Microprocessor Probe and External Probe, proceed as follows:

a. Ensure that LINE switch is in OFF position.

b. Connect Microprocessor Probe ribbon cable to Microprocessor Probe connector on 1611A rear panel (see figure 2-2). Ensure that cable socket is fully seated on board edge connector. Red stripe on cable indicates top edge.

c. Connect External Probe to External Probe connector on rear panel in same manner as for Microprocessor Probe.

d. Secure probe connectors to rear panel with screws provided.

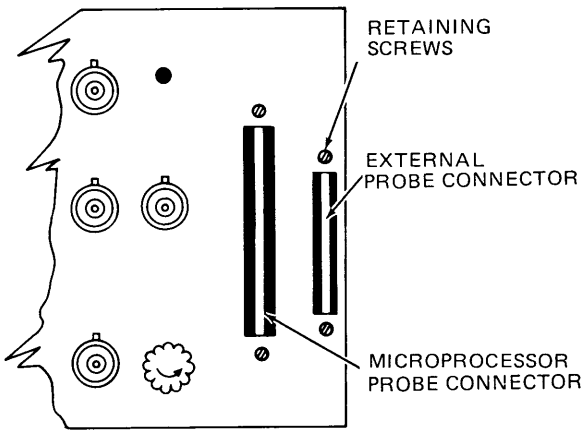


Figure 2-2. Rear-panel Probe Connectors

2-10. PERSONALITY MODULE INSTALLATION. To install a Personality Module in the instrument, refer to installation procedures in the manual supplement supplied with the Personality Module.

2-11. REPACKING FOR SHIPMENT.

2-12. If the instrument is to be shipped to a Hewlett-Packard Sales/Service Office for service or repair, attach a tag showing owner (with address), complete instrument serial number, and a description of the service required.

2-13. Use the original shipping carton and packing material. If the original packing material is not available, the Hewlett-Packard Sales/Service Office will provide information and recommendations on materials to be used.

SECTION III

OPERATION

Detailed operating information is provided in the Operating and Service Manual Supplement that is supplied with each Personality Module.

SECTION IV

PERFORMANCE TESTS

Detailed performance tests for the 1611A are dependent upon the personality module installed in the instrument. Therefore, complete performance tests for the 1611A are provided in the appropriate Personality Module Supplement provided with each 1611A Option and accessory. 1611A Options and Personality Module accessories are listed in Section I of this manual.

SECTION V

ADJUSTMENTS

5-1. INTRODUCTION.

5-2. This section contains a complete adjustment procedure for the 1611A. Power supply and display adjustments may be made separately following repairs or in sequence during periodic calibration.

WARNING

Read the Safety Summary at the front of this manual before performing adjustment procedures.

5-3. EQUIPMENT REQUIRED.

5-4. A list of Recommended Test Equipment is listed in Section I of this manual.

5-5. ADJUSTMENT LOCATIONS.

5-6. Adjustments and test point locations are shown in figures 5-1 and 5-3.

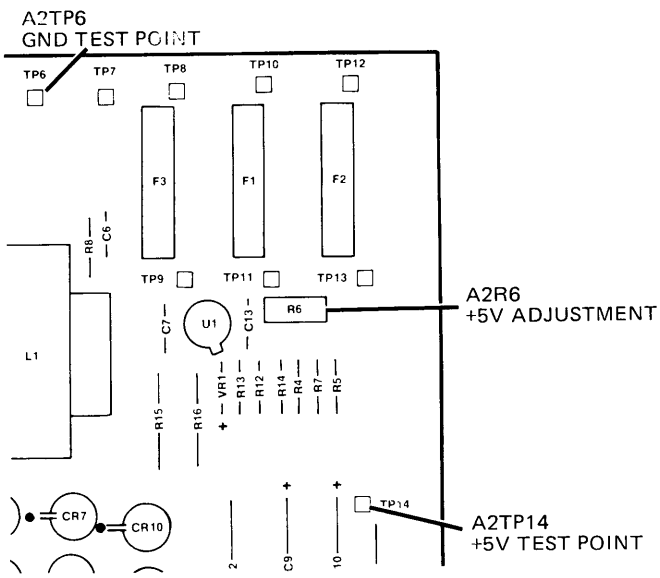


Figure 5-1. Power Supply Assy A2, Adjustment Location

5-7. +5 VOLT POWER SUPPLY ADJUSTMENT. (See figure 5-1 and service sheet 2.)

a. Disconnect 1611A power cord.

b. Remove 1611A top cover.

c. Reconnect power cord and place LINE switch in on position. LINE indicator lamp should light.

d. Connect (+) input of DVM to A2TP14 and connect (—) input of DVM to A2TP6.

e. Adjust A2R6 until DVM indicates +5.0 Vdc ±0.025 Vdc.

5-8. COMPARATOR ADJUSTMENT. (See figure 8-13, sheet 1 of 4, for part locations.)

a. Place LINE switch to off position and remove power cord.

b. Remove 1611A top cover.

c. Connect microprocessor probe to front-panel probe-test socket.

d. Connect dual-channel oscilloscope to test points TP1 and TP2 on A7.

e. Adjust delay clock A7R10 for 200-ns delay (±10 ns) between falling edges of signals at A7TP1 and A7TP2 (figure 5-2).

NOTE

The signals at A7TP1 and A7TP2 will be present for approximately 1 second in each 3 seconds.

f. Adjust clock width A7R12 (A7C4 on instruments with Serial Prefix 1723A) for 95 ±5 ns between falling edge and rising edge of signal at A7TP2 (figure 5-2).

NOTE

Some 1611A Options require additional adjustment of the Personality Board. Refer to the Operating and Service Manual Supplement to determine if additional adjustment is required.

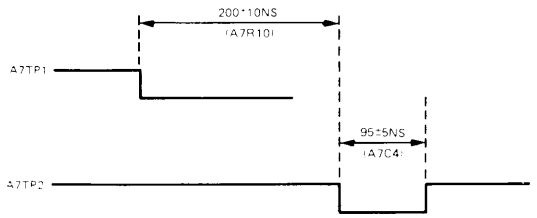


Figure 5-2. Delay and Clock Width Adjustments

5-9. DISPLAY ALIGNMENT. (See figure 6-1 for parts locations.)

NOTE

Normally, it is not necessary to perform this procedure unless the CRT has been replaced.

a. Place LINE switch to off position and remove power cord.

b. Remove 1611A top cover.

c. Remove screw that secures CRT post-accelerator lead holder (H39) to CRT shield (MP13).

d. Loosen four screws that hold CRT shield (MP13).

e. Remove CRT shield MP13.

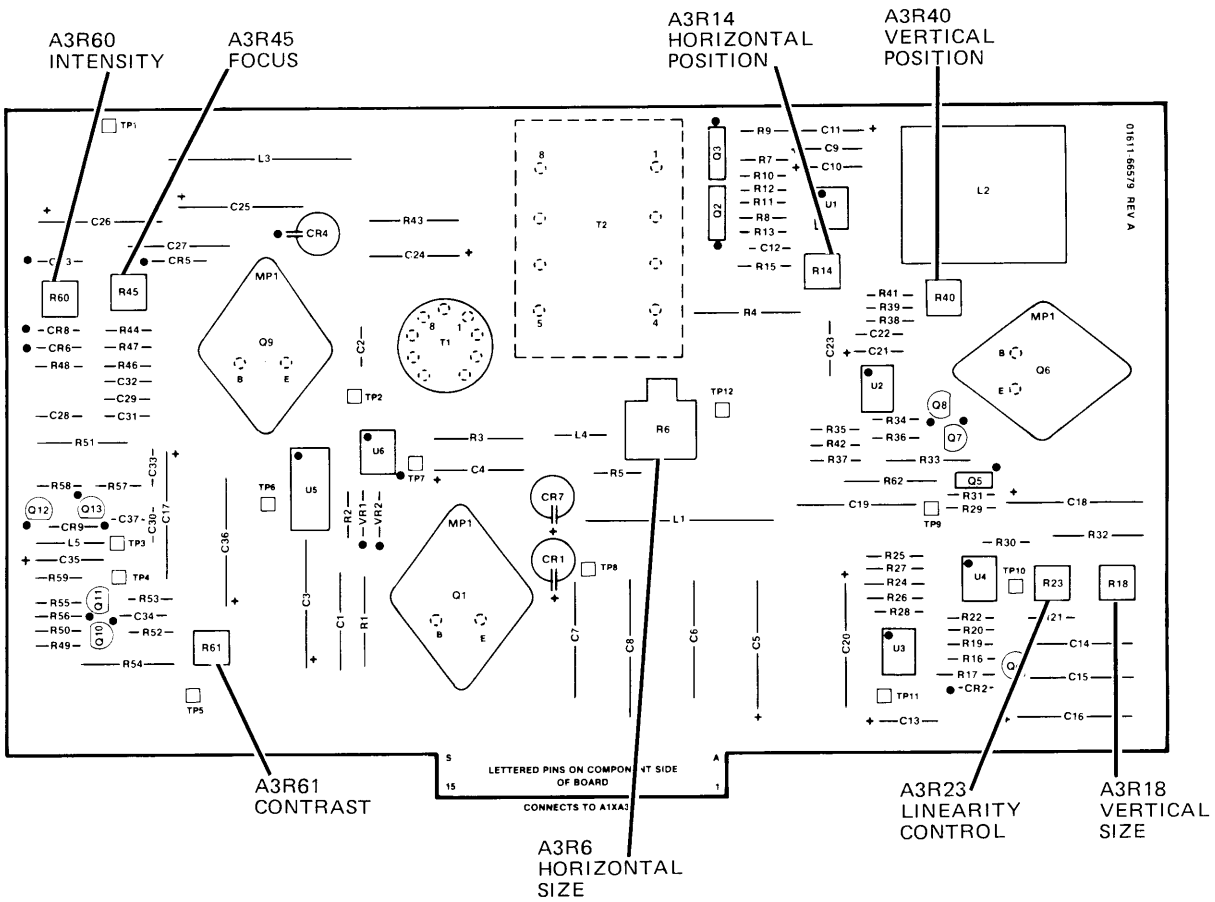


Figure 5-3. Display Assembly A3, Adjustment Locations

f. Loosen clamp on yoke L1.

g. Reconnect power cord and place LINE switch in on position.

h. Rotate yoke L1 so that horizontal lines on display are parallel with top and bottom of display window.

i. Set LINE switch to off position and remove power cord.

j. Tighten clamp on yoke L1.

CAUTION

Hand-tighten only. Over tightening will damage the CRT.

k. Install CRT shield MP13 and PA lead holder H39.

5-10. DISPLAY ADJUSTMENT. (See figure 5-3 and service sheet 3.)

a. Remove 1611A top cover and left side cover.

b. Connect external probe and microprocessor probe to their respective connectors on rear panel of 1611A.

c. Set front panel switches as follows:

FORMAT	HEXADECIMAL
TEST MODE	NORMAL
TRIGGER QUALIFIER (Option 068 only)	NORMAL

d. Connect microprocessor probe cable to PROBE TEST socket on front panel.

e. Press TRACE; a list should be displayed on CRT. If list is not displayed, set LINE switch to off, then on, and press TRACE again.

f. Turn contrast control A3R61 fully clockwise.

NOTE

This control is a service aid only. For normal operation, it should always be set fully clockwise.

g. Adjust intensity control A3R60 cw until retrace lines can be seen, then reduce intensity control until desired brightness is obtained.

CAUTION

Excessive intensity will cause permanent burning of CRT phosphor; however, this will not degrade display performance.

h. Adjust focus control A3R45 for best overall focus of display.

i. Adjust horizontal size A3R6 and vertical size A3R18 fully ccw.

j. Adjust horizontal position A3R14 and vertical position A3R40 to center display.

k. Adjust linearity control A3R23 so that characters in top and bottom lines of display are same height.

l. Adjust horizontal size A3R6 and horizontal position A3R14 for 20 mm (0.8 in.) margin on each side of display.

m. Adjust vertical size A3R18 and vertical position A3R40 for 5 mm (0.2 in.) margins at top and bottom.

n. Repeat step k.

SECTION VI

REPLACEABLE PARTS LIST

6-1. INTRODUCTION.

6-2. This section contains information for ordering parts. Table 6-1 lists abbreviations used in the parts list and throughout the manual. Table 6-2 lists all replaceable parts in reference designator order. Table 6-3 contains the names and addresses that correspond to the manufacturer's code number.

6-3. ABBREVIATIONS.

6-4. Table 6-1 lists abbreviations used in the parts list, the schematics and throughout the manual. In some cases, two forms of the abbreviation are used, one all in capital letters, and one partial or no capitals. This occurs because the abbreviations in the parts list are always all capitals. However, in the schematics and other parts of the manual, other abbreviation forms are used with both lower case and upper case letters.

6-5. REPLACEABLE PARTS LIST.

6-6. Table 6-2 is the list of replaceable parts and is organized as follows:

a. Electrical assemblies and their components in alphanumerical order by reference designation.

b. Chassis-mounted parts in alphanumerical order by reference designation.

c. Miscellaneous parts.

The information given for each part consists of the following:

a. The Hewlett-Packard part number.

b. The total quantity (Qty) in the instrument.

c. The description of the part.

d. A typical manufacturer of the part in a five-digit code.

e. The manufacturers' number for the part.

The total quantity for each part is given only once—at the first appearance of the part number in the list.

6-7. ORDERING INFORMATION.

6-8. To order a part listed in the replaceable parts table, quote the Hewlett-Packard part number, indicate the quantity required, and address the order to the nearest Hewlett-Packard office.

6-9. To order a part that is not listed in the replaceable parts table, include the instrument model number, instrument serial number, the description and function of the part, and the number of parts required. Address the order to the nearest Hewlett-Packard office.

6-10. DIRECT MAIL ORDER SYSTEM.

6-11. Within the USA, Hewlett-Packard can supply parts through a direct mail order system. Advantages of using the system are as follows:

a. Direct ordering and shipment from the HP Parts Center in Mountain View, California.

b. No maximum or minimum on any mail order (there is a minimum order amount for parts ordered through a local HP office when the orders require billing and invoicing).

c. Prepaid transportation (there is a small handling charge for each order).

d. No invoices—to provide these advantages, a check or money order must accompany each order.

6-12. Mail-order forms and specific ordering information are available through your local HP office. Addresses and phone numbers are located at the back of the 1611A Service Manual.

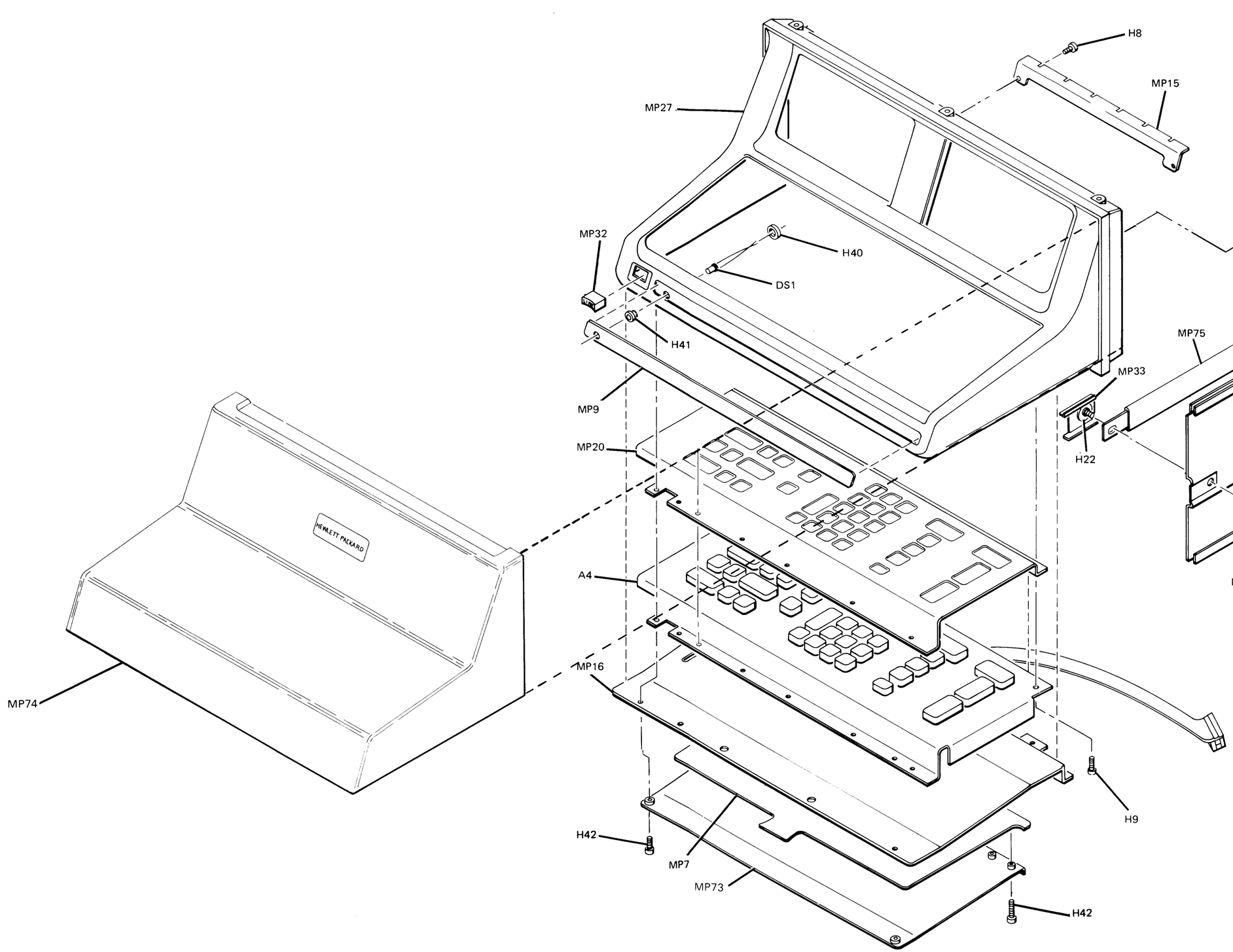
Table 6-1. Reference Designators and Abbreviations

REFERENCE DESIGNATORS

A	= assembly	**F**	= fuse	**MP**	= mechanical part	**U**	= integrated circuit
B	= motor	**FL**	= filter	**P**	= plug	**V**	= vacuum, tube, neon bulb, photocell, etc.
BT	= battery	**IC**	= integrated circuit	**Q**	= transistor		
C	= capacitor	**J**	= jack	**R**	= resistor	**VR**	= voltage regulator
CP	= coupler	**K**	= relay	**RT**	= thermistor	**W**	= cable
CR	= diode	**L**	= inductor	**S**	= switch	**X**	= socket
DL	= delay line	**LS**	= loud speaker	**T**	= transformer	**Y**	= crystal
DS	= device signaling (lamp)	**M**	= meter	**TB**	= terminal board	**Z**	= tuned cavity, network
E	= misc electronic part	**MK**	= microphone	**TP**	= test point		

ABBREVIATIONS

A	= amperes	**H**	= henries	**N/O**	= normally open	**RMO**	= rack mount only
AFC	= automatic frequency control	**HDW**	= hardware	**NOM**	= nominal	**RMS**	= root-mean square
AMPL	= amplifier	**HEX**	= hexagonal	**NPO**	= negative positive zero (zero temperature coefficient)	**RWV**	= reverse working voltage
		HG	= mercury				
BFO	= beat frequency oscillator	**HR**	= hour(s)				
BE CU	= beryllium copper	**HZ**	= hertz	**NPN**	= negative-positive-negative	**S-B**	= slow-blow
BH	= binder head					**SCR**	= screw
BP	= bandpass			**NRFR**	= not recommended for field replacement	**SE**	= selenium
BRS	= brass	**IF**	= intermediate freq			**SECT**	= section(s)
BWO	= backward wave oscillator	**IMPG**	= impregnated	**NSR**	= not separately replaceable	**SEMICON**	= semiconductor
		INCD	= incandescent			**SI**	= silicon
CCW	= counter-clockwise	**INCL**	= include(s)			**SIL**	= silver
CER	= ceramic	**INS**	= insulation(ed)	**OBD**	= order by description	**SL**	= slide
CMO	= cabinet mount only	**INT**	= internal	**OH**	= oval head	**SPG**	= spring
COEF	= coefficient			**OX**	= oxide	**SPL**	= special
COM	= common	**K**	= kilo = 1000			**SST**	= stainless steel
COMP	= composition					**SR**	= split ring
COMPL	= complete	**LH**	= left hand	**P**	= peak	**STL**	= steel
CONN	= connector	**LIN**	= linear taper	**PC**	= printed circuit		
CP	= cadmium plate	**LK WASH**	= lock washer	**PF**	= picofarads = 10^{-12} farads	**TA**	= tantalum
CRT	= cathode-ray tube	**LOG**	= logarithmic taper			**TD**	= time delay
CW	= clockwise	**LPF**	= low pass filter	**PH BRZ**	= phosphor bronze	**TGI**	= toggle
				PHL	= Phillips	**THD**	= thread
DEPC	= deposited carbon	**M**	= milli = 10^{-3}	**PIV**	= peak inverse voltage	**TI**	= titanium
DR	= drive	**MEG**	= meg = 10^{6}	**PNP**	= positive-negative-positive	**TOL**	= tolerance
		MET FLM	= metal film			**TRIM**	= trimmer
ELECT	= electrolytic	**MET OX**	= metallic oxide	**P/O**	= part of	**TWT**	= traveling wave tube
ENCAP	= encapsulated	**MFR**	= manufacturer	**POLY**	= polystyrene		
EXT	= external	**MHZ**	= mega hertz	**PORC**	= porcelain	**U**	= micro = 10^{-6}
		MINAT	= miniature	**POS**	= position(s)		
F	= farads	**MOM**	= momentary	**POT**	= potentiometer	**VAR**	= variable
FH	= flat head	**MOS**	= metal oxide substrate	**PP**	= peak-to-peak	**VDCW**	= dc working volts
FIL H	= fillister head	**MTG**	= mounting	**PT**	= point		
FXD	= fixed	**MY**	= "mylar"	**PWV**	= peak working voltage	**W/**	= with
						W	= watts
G	= giga (10^{9})	**N**	= nano (10^{-9})	**RECT**	= rectifier	**WIV**	= working inverse voltage
GE	= germanium	**N/C**	= normally closed	**RF**	= radio frequency		
GL	= glass	**NE**	= neon	**RH**	= round head or right hand	**WW**	= wirewound
GRD	= ground(ed)	**NI PL**	= nickel plate			**W/O**	= without


H8
MP15
MP27
MP32
H40
DS1
H41
MP75
MP33
MP9
MP20
H22
MP5
MP26
A4
MP16
MP74
H9
H42
MP7
MP73
H42
MP1

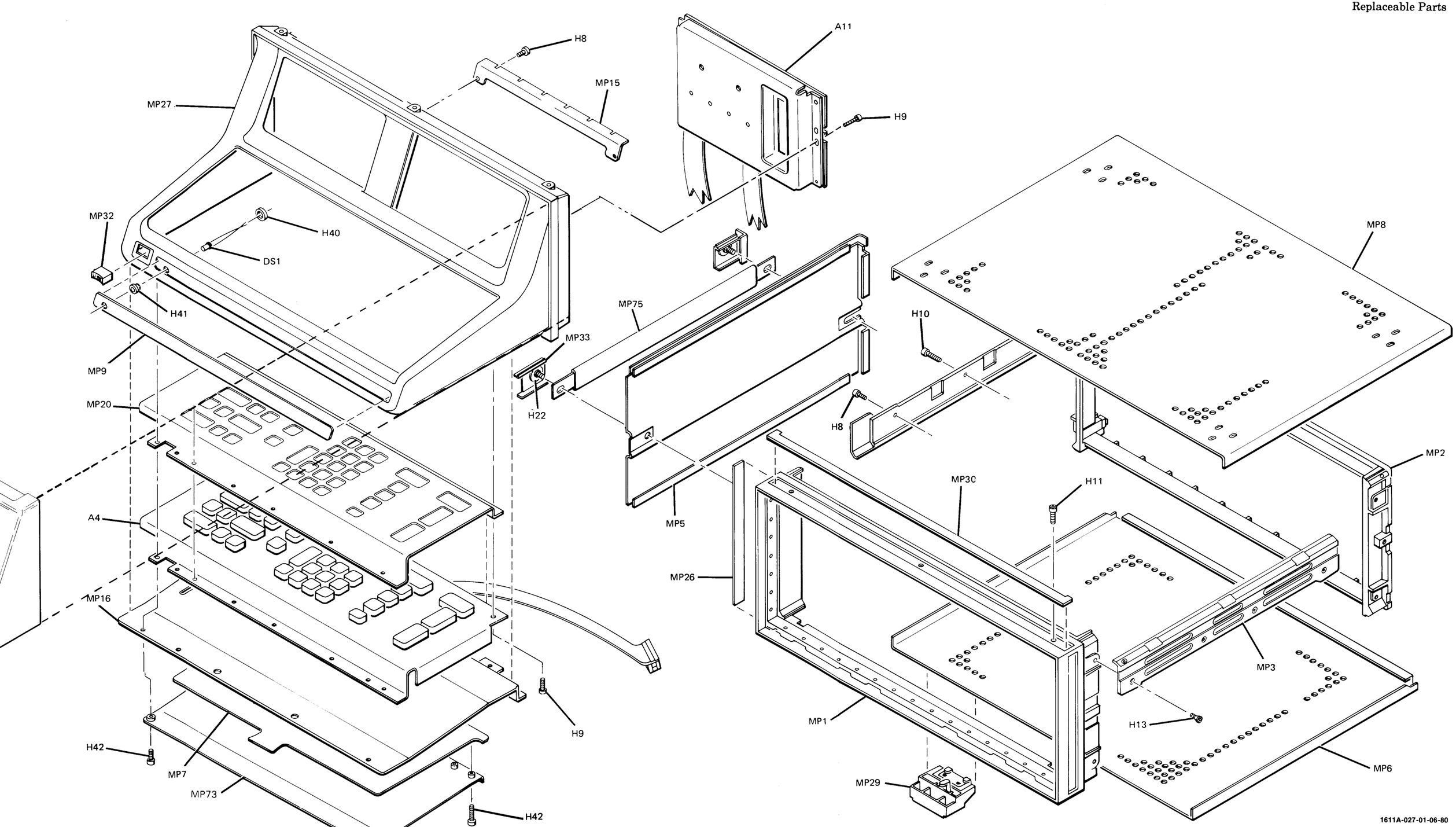
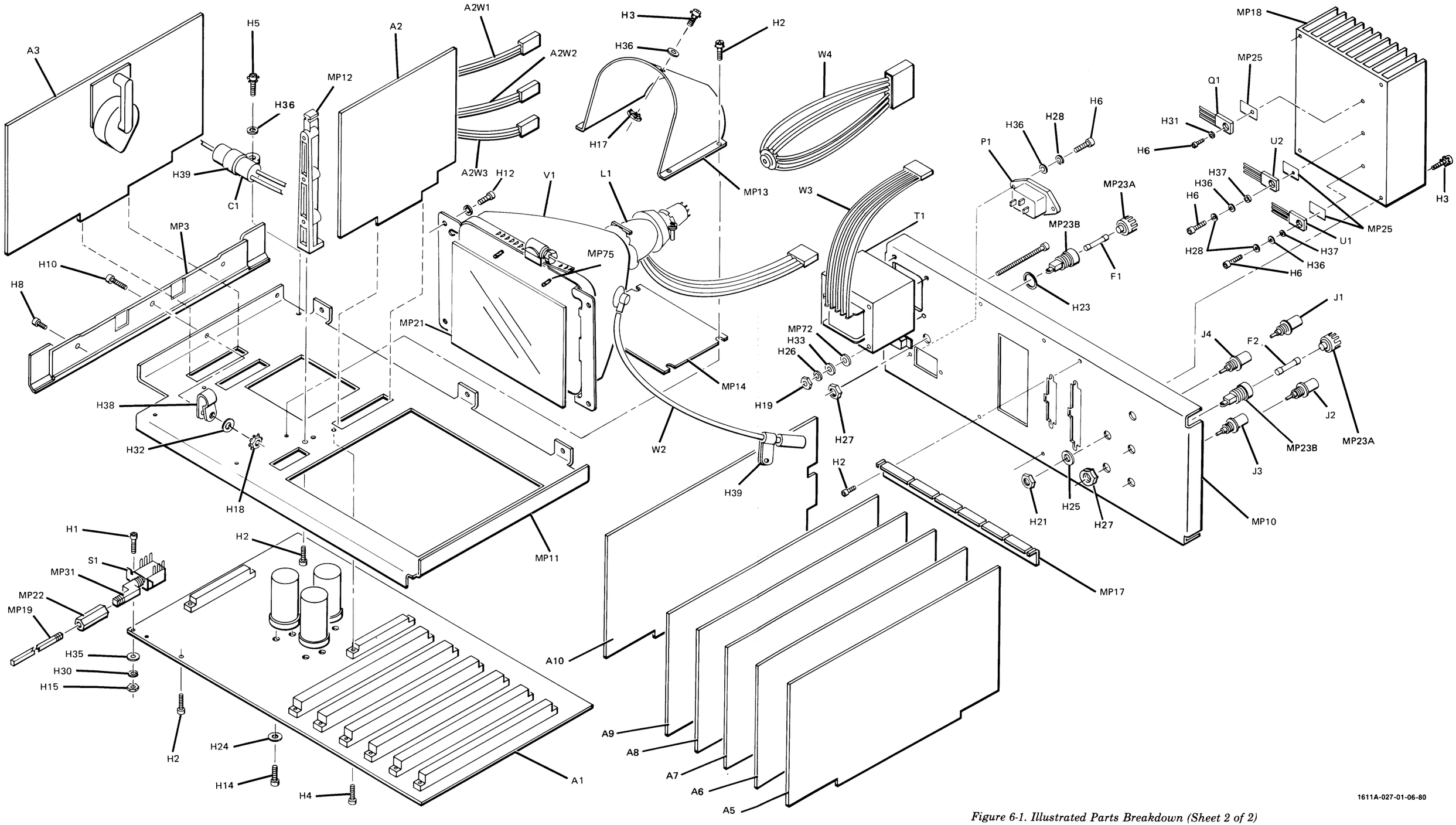


Figure 6-1.
Illustrated Parts Breakdown (Sheet 1 of 2)



1611A-027-01-06-80

Figure 6-1. Illustrated Parts Breakdown (Sheet 2 of 2)

Table 6-2. Replaceable Parts

Reference Designation	HP Part Number	CD	Qty	Description	Mfr Code	Mfr Part Number
A1	01611-66501	1		BOARD ASSEMBLY, MAIN	28480	01611-66501
A2	01611-66502	2		BOARD ASSEMBLY,LOW VOLTAGE POWER SUPPLY	28480	01611-66502
A3	01611-66579	3		BOARD ASSEMBLY, DISPLAY DRIVER	28480	01611-66579
A4	01611-66504	4		ASSEMBLY, KEYBOARD	28480	01611-66504
A5	01611-66505	5		BOARD ASSEMBLY, MICROPROCESSOR AND KEYBOARD SCAN	28480	01611-66505
A6	01611-66506	6		BOARD ASSEMBLY, RAM & DISPLAY GENERATOR	28480	01611-66506
A7	01611-66577	1		BOARD ASSEMBLY, COMPARATOR	28480	01611-66577
A8	01611-66535	1		BOARD ASSEMBLY, DATA STORE & COUNTERS	28480	01611-66535
A9				BOARD ASSEMBLY, PERSONALITY (SEE MANUAL SUPPLEMENT FOR OPTION INSTALLED IN YOUR INSTRUMENT)		
A10				BOARD ASSEMBLY, ROM (SEE MANUAL SUPPLEMENT FOR OPTION INSTALLED IN YOUR INSTRUMENT)		
A11				ASSEMBLY, PERSONALITY PANEL (SEE MANUAL SUPPLEMENT FOR OPTION INSTALLED IN YOUR INSTRUMENT)		
A12	01611-62101	9		ASSEMBLY, EXTERNAL PROBE	28480	01611-62101
A14	01611-66515	7		BOARD, EXTENDER	28480	01611-66515
C1	0160-4026	8	1	CAPACITOR-FXD .2UF +-20% 250VDC PPR	28480	0160-4026
CR1	1901-0768	0	1	DIODE-HV RECT 20KV 600UA 300NS	27777	H617
DS1	1990-0524	3	1	LED-VISIBLE LUM-INT=1MCD IF=20MA-MAX	28480	1990-0524
F1	2110-0007	4	1	FUSE 1A 250V TD 1.25X.25 UL	28480	2110-0007
F2	2110-0012	1	1	FUSE .5A 250V NTD 1.25X.25 UL	28480	2110-0012
H1	0520-0129	8	2	SCREW-MACH 2-56 .312-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H2	2200-0103	2	19	SCREW-MACH 4-40 .25-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H3	2200-0105	4	5	SCREW-MACH 4-40 .312-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H4	2200-0111	2	4	SCREW-MACH 4-40 .5-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H5	2200-0101	0	1	SCREW-MACH 4-40 .188-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H6	2200-0143	0	5	SCREW-MACH 4-40 .375-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H7				NOT ASSIGNED		
H8	2360-0113	2	21	SCREW-MACH 6-32 .25-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H9	2360-0115	4	11	SCREW-MACH 6-32 .312-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H10	2360-0121	2	1	SCREW-MACH 6-32 .5-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H11	2360-0194	9	9	SCREW-MACH 6-32 .312-IN-LG 100 DEG	00000	ORDER BY DESCRIPTION
H12	2510-0043	6	4	SCREW-MACH 8-32 .312-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H13	2510-0192	6	16	SCREW-MACH 8-32 .25-IN-LG 100 DEG	28480	2510-0192
H14	2680-0099	1	6	SCREW-MACH 10-32 .375-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H15	0610-0001	6	2	NUT-HEX-DBL-CHAM 2-56-THD .062-IN-THK	00000	ORDER BY DESCRIPTION
H16	2260-0001	5		NUT-HEX-DBL-CHAM 4-40-THD .094-IN-THK	28480	2260-0001
H17	2260-0009	3	1	NUT-HEX-W/LKWR 4-40-THD .094-IN-THK	00000	ORDER BY DESCRIPTION
H18	2420-0001	5	1	NUT-HEX-W/LKWR 6-32-THD .109-IN-THK	00000	ORDER BY DESCRIPTION
H19	2580-0004	6	4	NUT-HEX-DBL-CHAM 8-32-THD .125-IN-THK	00000	ORDER BY DESCRIPTION
H20	2950-0038	1	2	NUT-SPCLY 1/2-24-THD .125-IN-THK	28480	2950-0038
H21	2950-0043	8	4	NUT-HEX-DBL-CHAM 3/8-32-THD .094-IN-THK	00000	ORDER BY DESCRIPTION
H22	2680-0172	1	4	SCREW-MACH 10-32 .375-IN-LG 100 DEG	28480	2680-0172
H23	1400-0090	9	2	FUSEHOLDER COMPONENT FOR USE ON	28480	1400-0090
H24	2190-0011	8	6	WASHER-LK INTL T NO. 10 .195-IN-ID	28480	2190-0011
H25	2190-0016	3	4	WASHER-LK INTL T 3/8 IN .377-IN-ID	28480	2190-0016
H26	2190-0017	4	4	WASHER-LK HLCL NO. 8 .168-IN-ID	28480	2190-0017
H27	2110-0467	0	1	FUSEHOLDER COMPONENT HEX NUT: 1/2-28	28480	2110-0467
H28	2190-0019	6	6	WASHER-LK HLCL NO. 4 .115-IN-ID	28480	2190-0019
H29	2190-0037	8	2	WASHER-LK INTL T 1/2 IN .512-IN-ID	28480	2190-0037
H30	2190-0112	0	2	WASHER-LK HLCL NO. 2 .088-IN-ID	28480	2190-0112
H31	2190-0910	6	1	WASHER-LK INTL T NO. 4 .12-IN-ID	28480	2190-0910
H32	3050-0066	8		WASHER-FL MTLC NO. 6 .147-IN-ID	28480	3050-0066
H33	3050-0071	5	4	WASHER-FL MTLC NO. 8 .169-IN-ID	28480	3050-0071
H34	3050-0425	3	2	WASHER-FL MTLC .125-IN-ID .312-IN-OD SST	28480	3050-0425
H35	3050-0194	3	2	WASHER-FL MTLC NO. 1 .088-IN-ID	28480	3050-0194
H36	3050-0235	3	2	WASHER-FL MTLC NO. 4 .117-IN-ID	28480	3050-0235
H37	3050-0791	6	2	INSULATOR-XSTR NYLON	28480	3050-0791
H38	1400-0017	0	1	CLAMP-CABLE .312-DIA .375-WD NYL	28480	1400-0017
H39	1400-0335	5	2	CABLE TIE 1.75-DIA .188-WD NYL	28480	1400-0335
H40	1400-0540	4	1	RETAINER RING-LED CLIP 0.270-IN SERRATED	28480	1400-0540
H41	1400-0547	1	1	CL-LED-MTG	28480	1400-0547
H42	2360-0123	4	1	SCREW-MACH 6-32 .625-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
J1	1250-0083	1	4	CONNECTOR-RF BNC FEM SGL-HOLE-FR 50-OHM	28480	1250-0083
J2	1250-0083	1		CONNECTOR-RF BNC FEM SGL-HOLE-FR 50-OHM	28480	1250-0083
J3	1250-0083	1		CONNECTOR-RF BNC FEM SGL-HOLE-FR 50-OHM	28480	1250-0083
J4	1250-0083	1		CONNECTOR-RF BNC FEM SGL-HOLE-FR 50-OHM	28480	1250-0083

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-2. Replaceable Parts (Con't)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
L1	01611-61603	4	1	YOKE, WITH CABLE	28480	01611-61603
MP1	5020-8805	8	1	FRAME, FRONT	28480	5020-8805
MP2	5020-8806	9	1	FRAME, REAR	28480	5020-8806
MP3	5020-8835	4	4	STRUT, CORNER	28480	5020-8835
MP4				NOT ASSIGNED		
MP5	5060-9940	8	2	COVER, SIDE HANDLE	28480	5060-9940
MP6	5060-9991	9	1	COVER, BOTTOM	28480	5060-9991
MP7	9320-3699	8	1	CARD-INSTRUCTION	28480	9320-3699
MP8	5061-1933	5	1	COVER, TOP	28480	5061-1933
MP9	7120-5696	3	1	NAMEPLATE, 1611A	28480	7120-5696
MP10	01611-00215	6	1	PANEL, REAR	28480	01611-00215
MP11	01611-00101	9	1	DECK, MAIN	28480	01611-00101
MP12	01610-43101	8	1	GUIDE, CIRCUIT BOARD	28480	01610-43101
MP13	01611-00601	4	1	SHIELD, CRT	28480	01611-00601
MP14	01611-00602	5	1	SHIELD, CRT FLAT	28480	01611-00602
MP15	01611-01202	3	1	BRACKET, PC BOARD FLAT	28480	01611-01202
MP16	01611-04101	7	1	COVER, KEYBOARD	28480	01611-04101
MP17	01611-01204	5	1	BRACKET, PC BOARD, REAR	28480	01611-01204
MP18	01611-20501	5	1	HEAT SINK, MA	28480	01611-20501
MP19	01611-23701	3	1	SHAFT, SWITCH EXTENSION	28480	01611-23701
MP20	01611-00201	0	1	PANEL, KEYBOARD	28480	01611-00201
MP21	01611-24103	1	1	FACEPLATE, SAFETY	28480	01611-24103
MP22	01830-23201	3	1	COUPLER, SWITCH EXTENSION	28480	01830-23201
MP23A	2110-0465	8	2	FUSEHOLDER CAP EXTR PST; BAYONET; 20A	28480	2110-0465
MP23B	2110-0470	5	1	FUSEHOLDER BODY EXTR PST; BAYONET; TND	75915	345003-010
MP24	1540-0325	9	1	CASE, CRVG HANDLE	28480	1540-0325
MP25	0340-0511	0	3	INSULATOR-XSTR KAPTON	28480	0340-0511
MP26	5001-0440	1	2	TRIM, SIDE	28480	5001-0440
MP27	5040-0564	2	1	SUPPORT, KEYBOARD	28480	5040-0564
MP28	5060-9802	1	1	STRAP, HANDLE	28480	5060-9802
MP29	5040-7201	8	4	FEET	28480	5040-7201
MP30	5040-7202	9	1	TRIM STRIP, TOP	28480	5040-7202
MP31	5040-7675	0	1	PUSHROD, SWITCH	28480	5040-7675
MP32	0370-2989	3	1	KEY CAP, OFF/LINE	28480	0370-2989
MP33	5040-7219	8	2	CAP, STRAP HANDLE, FRONT	28480	5040-7219
MP34	5040-7220	1	2	CAP, STRAP HANDLE REAR	28480	5040-7220
MP35	5041-0676	9	1	KEYCAP, 1	28480	5041-0676
MP36	5041-0677	0	1	KEYCAP, 2	28480	5041-0677
MP37	5041-0678	1	1	KEYCAP, 3	28480	5041-0678
MP38	5041-0679	2	1	KEYCAP, 4	28480	5041-0679
MP39	5041-0680	5	1	KEYCAP, 5	28480	5041-0680
MP40	5041-0681	6	1	KEYCAP, 6	28480	5041-0681
MP41	5041-0682	7	1	KEYCAP, 7	28480	5041-0682
MP42	5041-0683	8	1	KEYCAP, 8	28480	5041-0683
MP43	5041-0684	9	1	KEYCAP, 9	28480	5041-0684
MP44	5041-0685	0	1	KEYCAP, 10	28480	5041-0685
MP45	5041-0040	1	1	KEYCAP, A	28480	5041-0040
MP46	5041-0041	2	1	KEYCAP, B	28480	5041-0041
MP47	5041-0042	3	1	KEYCAP, C	28480	5041-0042
MP48	5041-0043	4	1	KEYCAP, D	28480	5041-0043
MP49	5041-0044	5	1	KEYCAP, E	28480	5041-0044
MP50	5041-0045	6	1	KEYCAP, F	28480	5041-0045
MP51	5041-0046	7	1	KEYCAP, TIME INTRVL	28480	5041-0046
MP52	5041-0047	8	1	KEYCAP, COUNT TRIGS	28480	5041-0047
MP53	5041-0048	9	1	KEYCAP, BEFORE TRIG	28480	5041-0048
MP54	5041-0049	0	1	KEYCAP, AFTER TRIG	28480	5041-0049
MP55	5041-0050	3	1	KEYCAP, STOP	28480	5041-0050
MP56	5041-0051	4	1	KEYCAP, DON'T CARE	28480	5041-0051
MP57	5041-0052	5	1	KEYCAP, TRIGGER OCCURRENCE	28480	5041-0052
MP58	5041-0053	6	2	KEYCAP, ARROW	28480	5041-0053
MP59	5041-0060	5	2	KEYCAP, DATA BUS=, LIGHT	28480	5041-0060
MP60	5041-0065	0	1	KEYCAP, TRACE TRIGS	28480	5041-0065
MP61	5041-0073	0	1	KEYCAP, MNEMONIC=ABSOLUTE	28480	5041-0073
MP62	5041-0074	1	1	KEYCAP, ADRS BUS =	28480	5041-0074
MP63	5041-0075	2	1	KEYCAP, ADRS BUS =	28480	5041-0075
MP64	5041-0076	3	2	KEYCAP, EXT =, LIGHT	28480	5041-0076
MP65	5041-0088	7	1	KEYCAP, DATA BUS =, DARK	28480	5041-0088
MP66	5041-0089	8	1	KEYCAP, EXT =, DARK	28480	5041-0089
MP67	5041-0630	5	2	KEYCAP, ADDRESS BUS =, LIGHT	28480	5041-0630
MP68	5041-0631	6	1	KEYCAP, TRACE	28480	5041-0631
MP69	5041-0636	1	1	KEYCAP, ADDRESS BUS =, DARK	28480	5041-0636
MP70	0360-0016	2	2	TERMINAL-SLDR LUG LK-MTG FOR-#4-SCR	28480	0360-0016
MP71	0360-0053	7	1	TERMINAL-SLDR LUG LK-MTG FOR-#10-SCR	28480	0360-0053
MP72	0390-0006	3	4	INSULATOR-FLG-SSHG NYLON	28480	0390-0006
MP73	5061-1230	5	1	COVER, INSTRUCTION CARD	28480	5061-1230
MP74	5040-0588	0	1	COVER-KEYBOARD	28480	5040-0588

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-2. Replaceable Parts (Con't)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
MP75	01640-24701	0	4	SPACER-CRT SHIELD	28480	01640-24701
P_1	1251-2357	8	1	CONNECTOR-AC PWR HP-9 MALE FLG-MTG	28480	1251-2357
Q_1	1854-0433	5	1	TRANSISTOR NPN SI PD=90W FT=2MHZ	28480	1854-0433
R_1	0687-4751	2	1	RESISTOR 4.7M 10% .5W CC TC=0+1000	01121	EB4751
S_1	3101-1720	2	1	SWITCH-PB DPDT 4A 250VAC	28480	3101-1720
T_1	9100-3878	9	1	TRANSFORMER-LINE	28480	9100-3878
U_1	1826-0369	7	1	IC-LINEAR REG +12V	28480	1826-0369
U_2	1826-0368	6	1	IC-LINEAR REG-12V	28480	1826-0368
V1	5061-1250	9	1	ASSEMBLY, CRT	28480	5061-1250
W1	8120-1521	6	1	CABLE ASSY 18AWG 3-CNDCT JGK-JKT NOTE: FOR OTHER POWER CORDS AVAILABLE SEE SECTION II OF THIS MANUAL.	28480	8120-1521
W2	8120-2309	0	1	CABLE ASSEMBLY-H.V.	28480	8120-2309
W3	01611-61601	2	1	CABLE ASSEMBLY, TRANSFORMER	28480	01611-61601
W4	01611-61602	3	1	CABLE ASSEMBLY, CRT	28480	01611-61602

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-2. Replaceable Parts (Con't)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1	01611-66501	1	1	BOARD ASSEMBLY, MAIN	28480	01611-66501
A1C1	0180-0484	6	3	CAPACITOR-FXD 4500UF+75-10% 25VDC AL (NOT SUPPLIED W/A1,ORDER SEPARATELY)	28480	0180-0484
A1C2	0180-0484	6		CAPACITOR-FXD 4500UF+75-10% 25VDC AL (NOT SUPPLIED W/A1,ORDER SEPARATELY)	28480	0180-0484
A1C3	0180-0484	6		CAPACITOR-FXD 4500UF+75-10% 25VDC AL (NOT SUPPLIED W/A1,ORDER SEPARATELY)	28480	0180-0484
A1C4	0180-0228	6	6	CAPACITOR-FXD 22UF+-10% 15VDC TA	56289	150D226X9015B2
A1E1	0360-1653	5	5	CONNECTOR-SGL CONT PIN .045-IN-BSC-SZ SQ	28480	0360-1653
A1E2	0360-1653	5		CONNECTOR-SGL CONT PIN .045-IN-BSC-SZ SQ	28480	0360-1653
A1E3	0360-1653	5		CONNECTOR-SGL CONT PIN .045-IN-BSC-SZ SQ	28480	0360-1653
A1E4	0360-1653	5		CONNECTOR-SGL CONT PIN .045-IN-BSC-SZ SQ	28480	0360-1653
A1E5	0360-1653	5		CONNECTOR-SGL CONT PIN .045-IN-BSC-SZ SQ	28480	0360-1653
A1H1	0380-0059	5	1	SPACER-RVT-ON .25-IN-LG .152-IN-ID	00000	ORDER BY DESCRIPTION
A1P1	1251-4546	1	2	CONNECTOR 8-PIN M POST TYPE	28480	1251-4546
A1P2	1251-4549	4	2	CONNECTOR 7-PIN M POST TYPE	28480	1251-4549
A1P3	1251-3195	4	1	CONNECTOR 4-PIN M POST TYPE	28480	1251-3195
A1P4	1251-3279	5	1	CONNECTOR 12-PIN F POST TYPE	28480	1251-3279
A1P5	1251-0513	4	1	CONNECTOR 5-PIN M POST TYPE	28480	1251-0513
A1R1	0698-3180	2	1	RESISTOR 68 2% 2W MO TC=0+-200	28480	0698-3180
A1U1	1820-1450	7	1	IC BFR TTL S NAND QUAD 2-INP	01295	SN74837N
A1XA2	1251-1886	6	2	CONNECTOR-PC EDGE 15-CONT/ROW 2-ROWS	28480	1251-1886
A1XA3	1251-1886	6		CONNECTOR-PC EDGE 15-CONT/ROW 2-ROWS	28480	1251-1886
A1XA5	1251-4587	0	6	CONNECTOR-PC EDGE 50-CONT/ROW 2-ROWS	28480	1251-4587
A1XA6	1251-4587	0		CONNECTOR-PC EDGE 50-CONT/ROW 2-ROWS	28480	1251-4587
A1XA7	1251-4587	0		CONNECTOR-PC EDGE 50-CONT/ROW 2-ROWS	28480	1251-4587
A1XA8	1251-4587	0		CONNECTOR-PC EDGE 50-CONT/ROW 2-ROWS	28480	1251-4587
A1XA10P1	1251-4587	0		CONNECTOR-PC EDGE 50-CONT/ROW 2-ROWS	28480	1251-4587
A1XA9P1	1251-4587	0		CONNECTOR-PC EDGE 50-CONT/ROW 2-ROWS	28480	1251-4587
A1XU1	1200-0638	7	1	SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0638
A2	01611-66502	2	1	BOARD ASSEMBLY,LOW VOLTAGE POWER SUPPLY	28480	01611-66502
A2C1	0160-3508	9	9	CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3508
A2C2	0160-3508	9		CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3508
A2C3	0160-3508	9		CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3508
A2C4	0160-3508	9		CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3508
A2C5	0180-0091	1	1	CAPACITOR-FXD 10UF+50-10% 100VDC AL	56289	30D106F100DC2
A2C6	0160-3508	9		CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3508
A2C7	0160-2055	9	28	CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A2C8	0160-3508	9		CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3508
A2C9	0180-1714	7	1	CAPACITOR-FXD 330UF+-10% 6VDC TA	56289	150D337X9006B2
A2C10	0180-0137	6	1	CAPACITOR-FXD 100UF+-20% 10VDC TA	56289	150D107X0010R2
A2C11	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A2C12	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A2C13	0160-2204	0	2	CAPACITOR-FXD 100PF +-5% 300VDC MICA	28480	0160-2204
A2CR1	1901-0662	3	8	DIODE-PWR RECT 100V 6A	04713	MR751
A2CR2	1901-0662	3		DIODE-PWR RECT 100V 6A	04713	MR751
A2CR3	1901-0662	3		DIODE-PWR RECT 100V 6A	04713	MR751
A2CR4	1901-0662	3		DIODE-PWR RECT 100V 6A	04713	MR751
A2CR5	1901-0028	5	3	DIODE-PWR RECT 400V 750MA DO-29	28480	1901-0028
A2CR6	1901-0028	5		DIODE-PWR RECT 400V 750MA DO-29	28480	1901-0028
A2CR7	1901-0662	3		DIODE-PWR RECT 100V 6A	04713	MR751
A2CR8	1901-0662	3		DIODE-PWR RECT 100V 6A	04713	MR751
A2CR9	1901-0662	3		DIODE-PWR RECT 100V 6A	04713	MR751
A2CR10	1901-0662	3		DIODE-PWR RECT 100V 6A	04713	MR751
A2CR11	1901-0511	1	1	DIODE-PWR RECT 1N3889R 50V 12A 200NS	04713	1N3889R
A2CR12	1901-0028	5		DIODE-PWR RECT 400V 750MA DO-29	28480	1901-0028
A2F1	2110-0003	0	2	FUSE 3A 250V NTD 1.25X.25 UL	75915	312003
A2F2	2110-0003	0		FUSE 3A 250V NTD 1.25X.25 UL	75915	312003
A2F3	2110-0014	3	1	FUSE 4A 250V TD 1.25X.25 UL	75915	313004
A2H1	2360-0117	6	7	SCREW-MACH 6-32 .375-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
A2H2	2420-0002	6	2	NUT-HEX-DBL-CHAM 6-32-THD .109-IN-THK	28480	2420-0002
A2H3	2820-0002	4	1	NUT-HEX-DBL-CHAM 10-32-THD .094-IN-THK	00000	ORDER BY DESCRIPTION
A2H4	2190-0018	5	8	WASHER-LK HLCL NO. 6 .141-IN-ID	28480	2190-0018
A2H5	2190-0034	5	1	WASHER-LK HLCL NO. 10 .194-IN-ID	28480	2190-0034
A2H6	3050-0066	8	3	WASHER-FL MTLC NO. 6 .147-IN-ID	28480	3050-0066
A2H7	3050-0027	1	1	WASHER-FL MTLC NO. 10 .203-IN-ID	28480	3050-0027

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-2. Replaceable Parts (Con't)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A2L1	9100-3465	0	1	CHOKE-FILTER 580UH +-25% @ 20KHZ	28480	9100-3465
A2L2	9100-3829	0	1	INDUCTOR 10UH 10% .688DX1.188LG	28480	9100-3829
A2MP1	2110-0269	0	6	FUSEHOLDER-CLIP TYPE 5A .25D-FUSE	28480	2110-0269
A2MP2	1205-0310	2	2	HEAT SINK SGL TO-3-CS	28480	1205-0310
A2Q1	1853-0062	4	1	TRANSISTOR PNP SI PD=300MW FT=200MHZ	28480	1853-0062
A2Q2	1884-0082	3	1	THYRISTOR-SCR 2N4441 VRRM=50	04713	2N4441
A2R1	0698-4313	5	3	RESISTOR 2K 1% .5W F TC=0+-50	28480	0698-4313
A2R2	0698-4313	5		RESISTOR 2K 1% .5W F TC=0+-50	28480	0698-4313
A2R3	0698-4313	5		RESISTOR 2K 1% .5W F TC=0+-50	28480	0698-4313
A2R4	0757-0488	3	4	RESISTOR 909K 1% .125W F TC=0+-100	28480	0757-0488
A2R5	0757-0428	1	1	RESISTOR 1.62K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1621-F
A2R6	2100-3352	7	1	RESISTOR-TRMR 1K 10% C SIDE-ADJ 1-TRN	28480	2100-3352
A2R7	0757-0280	3	10	RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A2R8	0757-0438	3	6	RESISTOR 5.11K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5111-F
A2R9	0757-0419	0	1	RESISTOR 681 1% .125W F TC=0+-100	24546	C4-1/8-T0-681R-F
A2R10	0757-0809	2	1	RESISTOR 332 1% .5W F TC=0+-100	28480	0757-0809
A2R11	0698-3430	5	1	RESISTOR 21.5 1% .125W F TC=0+-100	03888	PME55-1/8-T0-21R5-F
A2R12	0757-0346	2	2	RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
A2R13	0757-0200	7	1	RESISTOR 5.62K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5621-F
A2R14	0757-0395	1	2	RESISTOR 56.2 1% .125W F TC=0+-100	24546	C4-1/8-T0-56R2-F
A2R15	0811-2771	7	2	RESISTOR .18 3% 3W PW TC=0+-90	28480	0811-2771
A2R16	0811-1758	8	1	RESISTOR .24 5% 2W PW TC=0+-800	75042	BWH2-24/100-J
A2R17	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
A2R18	0757-0395	1		RESISTOR 56.2 1% .125W F TC=0+-100	24546	C4-1/8-T0-56R2-F
A2R19	0811-2771	7		RESISTOR .18 3% 3W PW TC=0+-90	28480	0811-2771
A2U1	1820-0196	6	1	IC 723 V RGLTR TO-100	28480	1820-0196
A2VR1	1902-3104	6	1	DIODE-ZNR 5.62V 5% DO-35 PD=.4W	28480	1902-3104
A2W1	01611-61613	6	1	CABLE, VOLTAGE REGULATOR (NOT SUPPLIED W/A2, ORDER SEPARATELY)	28480	01611-61613
A2W2	01607-61613	0	1	CABLE, VOLTAGE REGULATOR (NOT SUPPLIED W/A2, ORDER SEPARATELY)	28480	01607-61613
A2W3	01611-61614	7	1	CABLE, VOLTAGE REGULATOR (NOT SUPPLIED W/A2, ORDER SEPARATELY)	28480	01611-61614
A3	01611-66579	3	1	BOARD ASSEMBLY, DISPLAY DRIVER	28480	01611-66579
A3C1	0160-0161	4	1	CAPACITOR-FXD .01UF +-10% 200VDC POLYE	28480	0160-0161
A3C2	0140-0199	6	1	CAPACITOR-FXD 240PF +-5% 300VDC MICA	72136	DM15F241J0300WV1CR
A3C3	0180-0097	7	6	CAPACITOR-FXD 47UF+-10% 35VDC TA	56289	150D476X903582
A3C4	0180-0106	9	3	CAPACITOR-FXD 60UF+-20% 6VDC TA	56289	150D606X000682
A3C5	0180-0097	7		CAPACITOR-FXD 47UF+-10% 35VDC TA	56289	150D476X903582
A3C6	0160-4455	7	1	CAPACITOR-FXD 10UF +-10% 50VDC MET-POLYC	28480	0160-4455
A3C7	0160-3127	8	2	CAPACITOR-FXD .022UF +-5% 400VDC POLYE	84411	663UW22354M2
A3C8	0160-3830	0	1	CAPACITOR-FXD 5UF +-10% 50VDC MET-POLYC	28480	0160-3830
A3C9	0180-0230	0	4	CAPACITOR-FXD 1UF+-20% 50VDC TA	56289	150D105X0050A2
A3C10	0180-0230	0		CAPACITOR-FXD 1UF+-20% 50VDC TA	56289	150D105X0050A2
A3C11	0180-0230	0		CAPACITOR-FXD 1UF+-20% 50VDC TA	56289	150D105X0050A2
A3C12	0160-3508	9		CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3508
A3C13	0180-1701	2	1	CAPACITOR-FXD 6.8UF+-20% 6VDC TA	56289	150D685X0006A2
A3C14	0160-3762	7	2	CAPACITOR-FXD .68UF +-5% 50VDC MET-POLYC	28480	0160-3762
A3C15	0160-3762	7		CAPACITOR-FXD .68UF +-5% 50VDC MET-POLYC	28480	0160-3762
A3C16	0180-0097	7		CAPACITOR-FXD 47UF+-10% 35VDC TA	56289	150D476X903582
A3C17	0180-1819	3	1	CAPACITOR-FXD 100UF+75-10% 50VDC AL	56289	30D107G050DM2
A3C18	0180-0097	7		CAPACITOR-FXD 47UF+-10% 35VDC TA	56289	150D476X903582
A3C19	0160-3127	8		CAPACITOR-FXD .022UF +-5% 400VDC POLYE	84411	663UW22354M2
A3C20	0180-2667	1	1	CAPACITOR-FXD 150UF+-10% 20VDC TA	56289	150D157X902082
A3C21	0180-0230	0		CAPACITOR-FXD 1UF+-20% 50VDC TA	56289	150D105X0050A2
A3C22	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A3C23	0160-3508	9		CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3508
A3C24	0180-0106	9		CAPACITOR-FXD 60UF+-20% 6VDC TA	56289	150D606X000682
A3C25	0180-0097	7		CAPACITOR-FXD 47UF+-10% 35VDC TA	56289	150D476X903582
A3C26	0180-0097	7		CAPACITOR-FXD 47UF+-10% 35VDC TA	56289	150D476X903582
A3C27	0160-4449	9	1	CAPACITOR-FXD 8200PF +-10% 400VDC POLYE	28480	0160-4449
A3C28	0180-0426	6	1	CAPACITOR-FXD 22UF+100-10% 250VDC AL	28480	0180-0426
A3C29	0160-3665	9	5	CAPACITOR-FXD .01UF +80-20% 500VDC CER	28480	0160-3665
A3C30	0160-3665	9		CAPACITOR-FXD .01UF +80-20% 500VDC CER	28480	0160-3665
A3C31	0160-3665	9		CAPACITOR-FXD .01UF +80-20% 500VDC CER	28480	0160-3665
A3C32	0160-3665	9		CAPACITOR-FXD .01UF +80-20% 500VDC CER	28480	0160-3665
A3C33	0160-3665	9		CAPACITOR-FXD .01UF +80-20% 500VDC CER	28480	0160-3665
A3C34	0160-2204	0		CAPACITOR-FXD 100PF +-5% 300VDC MICA	28480	0160-2204
A3C35	0180-0106	9		CAPACITOR-FXD 60UF+-20% 6VDC TA	56289	150D606X000682
A3C36	0180-0098	8	1	CAPACITOR-FXD 100UF+-20% 20VDC TA	56289	150D107X002082
A3C37	0160-3508	9		CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3508

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-2. Replaceable Parts (Con't)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A3CR1	1901-0767	9	3	DIODE-PWR RECT 400V 6A	04713	MR754
A3CR2	1901-0040	1	2	DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A3CR3	1901-0029	6	5	DIODE-PWR RECT 600V 750MA DO-29	28480	1901-0029
A3CR4	1901-0767	9		DIODE-PWR RECT 400V 6A	04713	MR754
A3CR5	1901-0029	6		DIODE-PWR RECT 600V 750MA DO-29	28480	1901-0029
A3CR6	1901-0029	6		DIODE-PWR RECT 600V 750MA DO-29	28480	1901-0029
A3CR7	1901-0767	9		DIODE-PWR RECT 400V 6A	04713	MR754
A3CR8	1901-0029	6		DIODE-PWR RECT 600V 750MA DO-29	28480	1901-0029
A3CR9	1901-0029	6		DIODE-PWR RECT 600V 750MA DO-29	28480	1901-0029
A3H1	2360-0201	9	6	SCREW-MACH 6-32 .5-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
A3H2	2420-0003	7	6	NUT-HEX-DBL-CHAM 6-32-THD .094-IN-THK	00000	ORDER BY DESCRIPTION
A3H3	2260-0001	5	3	NUT-HEX-DBL-CHAM 4-40-THD .094-IN-THK	28480	2260-0001
A3H4	2190-0018	5		WASHER-LK HLCL NO. 6 .141-IN-ID	28480	2190-0018
A3H5	2190-0019	6	10	WASHER-LK HLCL NO. 4 .115-IN-ID	28480	2190-0019
A3H6	3050-0016	8	6	WASHER-FL MTLC NO. 6 .147-IN-ID	28480	3050-0016
A3H7	3050-0235	3	10	WASHER-FL MTLC NO. 4 .117-IN-ID	28480	3050-0235
A3L1	9100-3930	4	1	INDUCTOR 2.5MH 10% .625DX1.437LG	28480	9100-3930
A3L2	9100-3877	8	1	INDUCTORRF-CH-MLD 290MH	28480	9100-3877
A3L3	9100-3931	5	1	INDUCTOR 700UH 10% .6DX1.437LG	28480	9100-3931
A3L4	01611-86001	8	1	COIL, FXD	28480	01611-86001
A3L5	9140-0111	1	1	INDUCTORRF-CH-MLD 3.3UH 10%	28480	9140-0111
A3MP1	1205-0310	2		HEAT SINK SGL TO-3-C8	28480	1205-0310
A3Q1	1854-0751	0	3	TRANSISTOR NPN 2N5840 SI TO-3 PD=100W	07263	2N5840
A3Q2	1854-0558	5	1	TRANSISTOR NPN SI DARL PD=70W FT=1MHZ	28480	1854-0558
A3Q3	1853-0334	3	1	TRANSISTOR PNP SI DARL PD=70W FT=1MHZ	04713	MJE1090
A3Q4	1854-0215	1	5	TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A3Q5	1854-0330	1	1	TRANSISTOR NPN SI PD=21W FT=10MHZ	28480	1854-0330
A3Q6	1854-0751	0		TRANSISTOR NPN 2N5840 SI TO-3 PD=100W	07263	2N5840
A3Q7	1854-0215	1		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A3Q8	1853-0036	2	2	TRANSISTOR PNP SI PD=310MW FT=250MHZ	28480	1853-0036
A3Q9	1854-0751	0		TRANSISTOR NPN 2N5840 SI TO-3 PD=100W	07263	2N5840
A3Q10	1854-0215	1		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A3Q11	1854-0215	1		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A3Q12	1854-0215	1		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A3Q13	1853-0036	2		TRANSISTOR PNP SI PD=310MW FT=250MHZ	28480	1853-0036
A3R1	0757-0812	7	1	RESISTOR 432 1% .5W F TC=0+-100	28480	0757-0812
A3R2	0757-0442	9	1	RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A3R3	0811-1878	3	1	RESISTOR 7.5 5% 25W PW TC=0+-260	28480	0811-1878
A3R4	0698-3605	6	1	RESISTOR 15 5% 2W MO TC=0+-200	27167	FP42-2-T00-15R0-J
A3R5	0757-0401	0	6	RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A3R6	2100-3576	7	1	RESISTOR-VAR CONTROL CC 50 10% LIN	01121	73M4G0248500U
A3R7	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A3R8	0757-0457	6	9	RESISTOR 47.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4752-F
A3R9	0757-0457	6		RESISTOR 47.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4752-F
A3R10	0757-0457	6		RESISTOR 47.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4752-F
A3R11	0757-0457	6		RESISTOR 47.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4752-F
A3R12	0757-0283	6	4	RESISTOR 2K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2001-F
A3R13	0757-0283	6		RESISTOR 2K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2001-F
A3R14	2100-3252	6	4	RESISTOR-TRMR 5K 10% C TOP-ADJ 1-TRN	28480	2100-3252
A3R15	0757-0283	6		RESISTOR 2K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2001-F
A3R16	0757-0437	2	3	RESISTOR 4.75K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4751-F
A3R17	0757-0488	3		RESISTOR 909K 1% .125W F TC=0+-100	28480	0757-0488
A3R18	2100-3213	7	1	RESISTOR-TRMR 200K 10% C TOP-ADJ 1-TURN	28480	2100-3213
A3R19	0757-0470	3	2	RESISTOR 162K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1623-F
A3R20	0757-0394	0	3	RESISTOR 51.1 1% .125W F TC=0+-100	24546	C4-1/8-T0-51R1-F
A3R21	0757-0437	2		RESISTOR 4.75K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4751-F
A3R22	0757-0470	3		RESISTOR 162K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1623-F
A3R23	2100-3252	6		RESISTOR-TRMR 5K 10% C TOP-ADJ 1-TRN	28480	2100-3252
A3R24	0698-5437	6	2	RESISTOR 12K .1% .125W F TC=0+-50	28480	0698-5437
A3R25	0698-5437	6		RESISTOR 12K .1% .125W F TC=0+-50	28480	0698-5437
A3R26	0698-5420	7	2	RESISTOR 3.874K .1% .125W F TC=0+-50	28480	0698-5420
A3R27	0698-5420	7		RESISTOR 3.874K .1% .125W F TC=0+-50	28480	0698-5420
A3R28	0757-0407	6	1	RESISTOR 200 1% .125W F TC=0+-100	24546	C4-1/8-T0-201-F
A3R29	0757-0437	2		RESISTOR 4.75K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4751-F
A3R30	0757-0283	6		RESISTOR 2K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2001-F
A3R31	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A3R32	0811-1671	4	1	RESISTOR 2.7 5% 2W PW TC=0+-400	75042	BWH2-2R7-J
A3R33	0757-0804	7	1	RESISTOR 200 1% .5W F TC=0+-100	28480	0757-0804
A3R34	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A3R35	0757-0457	6		RESISTOR 47.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4752-F
A3R36	0757-0457	6		RESISTOR 47.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4752-F
A3R37	0757-0457	6		RESISTOR 47.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4752-F
A3R38	0757-0457	6		RESISTOR 47.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4752-F
A3R39	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A3R40	2100-3252	6		RESISTOR-TRMR 5K 10% C TOP-ADJ 1-TRN	28480	2100-3252

See introduction to this section for ordering information
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Table 6-2. Replaceable Parts (Con't)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A3R41	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A3R42	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A3R43	0811-1678	1	1	RESISTOR 10 5% 2W PW TC=0+-400	75042	BWH2-10R-J
A3R44	0684-1041	1	2	RESISTOR 100K 10% .25W FC TC=-400/+800	01121	CB1041
A3R45	2100-0569	2	2	RESISTOR-TRMR 1M 20% C TOP-ADJ 1-TRN	28480	2100-0569
A3R46	0684-1041	1		RESISTOR 100K 10% .25W FC TC=-400/+800	01121	CB1041
A3R47	0757-0488	3		RESISTOR 909K 1% .125W F TC=0+-100	28480	0757-0488
A3R48	0757-0488	3		RESISTOR 909K 1% .125W F TC=0+-100	28480	0757-0488
A3R49	0757-0457	6		RESISTOR 47.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4752-F
A3R50	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A3R51	0757-0159	5	2	RESISTOR 1K 1% .5W F TC=0+-100	28480	0757-0159
A3R52	0757-0394	0		RESISTOR 51.1 1% .125W F TC=0+-100	24546	C4-1/8-T0-51R1-F
A3R53	0757-0394	0		RESISTOR 51.1 1% .125W F TC=0+-100	24546	C4-1/8-T0-51R1-F
A3R54	0698-0090	7	1	RESISTOR 464 1% .5W F TC=0+-100	28480	0698-0090
A3R55	0757-0412	3	1	RESISTOR 365 1% .125W F TC=0+-100	24546	C4-1/8-T0-365R-F
A3R56	0757-0284	7	1	RESISTOR 150 1% .125W F TC=0+-100	24546	C4-1/8-T0-151-F
A3R57	0757-0469	0	1	RESISTOR 150K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1503-F
A3R58	0757-0453	2	1	RESISTOR 30.1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3012-F
A3R59	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A3R60	2100-0569	2		RESISTOR-TRMR 1M 20% C TOP-ADJ 1-TRN	28480	2100-0569
A3R61	2100-3252	6		RESISTOR-TRMR 5K 10% C TOP-ADJ 1-TRN	28480	2100-3252
A3R62	0757-0159	5		RESISTOR 1K 1% .5W F TC=0+-100	28480	0757-0159
A3T1	5061-1228	1	1	TRANSFORMER	28480	5061-1228
A3T2	9100-3927	9	1	TRANSFORMER-POWER	28480	9100-3927
A3TP1	0360-0535	0	45	TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A3TP2	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A3TP3	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A3TP4	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A3TP5	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A3TP6	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A3TP7	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A3TP8	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A3TP9	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A3TP10	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A3TP11	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A3TP12	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A3U1	1826-0254	9	4	IC OP AMP GP 8-DIP-P	04713	MC17418CP1
A3U2	1826-0254	9		IC OP AMP GP 8-DIP-P	04713	MC17418CP1
A3U3	1826-0254	9		IC OP AMP GP 8-DIP-P	04713	MC17418CP1
A3U4	1826-0254	9		IC OP AMP GP 8-DIP-P	04713	MC17418CP1
A3U5	1820-1422	3	2	IC MV TTL LS MONOSTBL RETRIG	01295	SN74LS122N
A3U6	1820-1796	4	1	IC DRVR TTL DUAL 2-INP	27014	DS3611N
A3VR1	1902-0041	4	2	DIODE-ZNR 5.11V 5% DO-35 PD=.4W	28480	1902-0041
A3VR2	1902-0593	1	1	DIODE-ZNR 43.2V 10% DO-15 PD=1W TC=+.08%	28480	1902-0593
A4	01611-66504	4	1	ASSEMBLY, KEYBOARD	28480	01611-66504
A4C1	0180-0228	6		CAPACITOR-FXD 22UF+-10% 15VDC TA	56289	150D226X9015B2
A4C2	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A4C3	0160-0158	9	1	CAPACITOR-FXD 5600PF +-10% 200VDC POLYE	28480	0160-0158
A4H1	2360-0113	2	22	SCREW-MACH 6-32 .25-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
A4MP1	01611-04701	3	1	SUPPORT, KEYBOARD	28480	01611-04701
A4R1	0757-0416	7	1	RESISTOR 511 1% .125W F TC=0+-100	24546	C4-1/8-T0-511R-F
A4R2	0684-2711	4	1	RESISTOR 270 10% .25W FC TC=-400/+600	01121	CB2711
A4S1-A4S48	3101-2137	7	2 48	SWITCH-PB SPST-NO MOM	28480	3101-2137
A4U1	1820-1418	7	4	IC DCDR TTL LS BCD-TO-DEC 4-TO-10-LINE	01295	SN74LS42N
A4U2	1820-0535	7	4	IC DRVR TTL AND DUAL 2-INP	01295	SN75451BP
A4U3	1820-0535	7		IC DRVR TTL AND DUAL 2-INP	01295	SN75451BP
A4U4	1820-0535	7		IC DRVR TTL AND DUAL 2-INP	01295	SN75451BP
A4U5	1820-0535	7		IC DRVR TTL AND DUAL 2-INP	01295	SN75451BP
A4W1	01611-61604	5	1	CABLE ASSEMBLY, KEYBOARD	28480	01611-61604
A5	01611-66505	5	1	BOARD ASSEMBLY, MICROPROCESSOR AND KEYBOARD SCAN	28480	01611-66505
A5C1	0140-0198	5	1	CAPACITOR-FXD 200PF +-5% 300VDC MICA	72136	DM15F201J0300WV1CR
A5C2	0160-2150	5	1	CAPACITOR-FXD 33PF +-5% 300VDC MICA	28480	0160-2150
A5C3	0180-0229	7	2	CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
A5C4	0180-0155	8	1	CAPACITOR-FXD 2.2UF+-20% 20VDC TA	56289	150D225X0020A2
A5C5	0180-1746	1	13	CAPACITOR-FXD 15UF +80-20% 100VDC CER	28480	0180-1746

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-2. Replaceable Parts (Con't)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A5C6	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A5C7	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A5C8	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A5C9	0180-0229	7		CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
A5C10	0160-3451	1		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-3451
A5R1	0757-0427	0	2	RESISTOR 1.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1501-F
A5R2	0761-0054	8	2	RESISTOR 330 5% 1W MO TC=0+-200	28480	0761-0054
A5R3	0761-0054	8		RESISTOR 330 5% 1W MO TC=0+-200	28480	0761-0054
A5R4	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A5R5	0684-3311	2	1	RESISTOR 330 10% .25W FC TC=-400/+600	01121	CB3311
A5R6	0757-0279	0	1	RESISTOR 3.16K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3161-F
A5R7	0698-3154	0	1	RESISTOR 4.22K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4221-F
A5R8	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A5R9	0757-0429	2	4	RESISTOR 1.82K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1821-F
A5R10	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A5R11	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A5R12	0757-0429	2		RESISTOR 1.82K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1821-F
A5R13	0698-0084	9	1	RESISTOR 2.15K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2151-F
A5R14	0757-0427	0		RESISTOR 1.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1501-F
A5R15	0757-0420	3	1	RESISTOR 750 1% .125W F TC=0+-100	24546	C4-1/8-T0-751-F
A5TP1	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A5TP2	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A5TP3	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A5TP4	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A5TP5	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A5TP6	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A5TP7	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A5TP8	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A5TP9	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A5U1	1820-1112	8	4	IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
A5U2	1820-1201	6	4	IC GATE TTL LS AND QUAD 2-INP	01295	SN74LS08N
A5U3	1820-1199	1	2	IC INV TTL LS HEX 1-INP	01295	SN74LS04N
A5U4	1820-0471	0	1	IC INV TTL HEX 1-INP	01295	SN7406N
A5U5	1820-1217	4	1	IC MUXR/DATA-SEL TTL LS 8-TO-1-LINE	01295	SN74LS151N
A5U6	1820-1422	3		IC MV TTL LS MONOSTBL RETRIG	01295	SN74LS122N
A5U7	1820-1464	3	2	IC CNTR TTL BIN ASYNCHRO NEG-EDGE-TRIG	01295	SN74393N
A5U8	1820-1198	0	2	IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS03N
A5U9	1820-1198	0		IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS03N
A5U10	1820-1201	6		IC GATE TTL LS AND QUAD 2-INP	01295	SN74LS08N
A5U11	1820-1783	9	1	IC MICPROC NMOS 8-BIT	01295	TMS8080AN
A5U12	1820-1491	6	2	IC BFR TTL LS NON-INV HEX 1-INP	01295	SN74LS367AN
A5U13	1820-1207	2	1	IC GATE TTL LS NAND 8-INP	01295	SN74LS30N
A5U14	1820-1425	6	2	IC SCHMITT-TRIG TTL LS NAND QUAD 2-INP	01295	SN74LS132N
A5U15	1821-0001	4	2	TRANSISTOR ARRAY 14-PIN PLSTC DIP	01928	CA3046
A5U16	1821-0001	4		TRANSISTOR ARRAY 14-PIN PLSTC DIP	01928	CA3046
A5U17	1820-1282	3	1	IC FF TTL LS J-K BAR POS-EDGE-TRIG	01295	SN74LS109AN
A5U18	1820-1439	2	9	IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE	01295	SN74LS258AN
A5U19	1820-1439	2		IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE	01295	SN74LS258AN
A5U20	1820-1201	6		IC GATE TTL LS AND QUAD 2-INP	01295	SN74LS08N
A5U21	1820-1491	6		IC BFR TTL LS NON-INV HEX 1-INP	01295	SN74LS367AN
A5U22	1820-1196	8	5	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS174N
A5U23	1820-1429	0	2	IC CNTR TTL LS DECD SYNCHRO	01295	SN74LS160AN
A5U24	1810-0283	1	1	NETWORK-RES 16-DIP270.0 OHM X 8	28480	1810-0283
A5U25	1810-0049	7	2	NETWORK-RES 12-SIP6.8K OHM X 10	28480	1810-0049
A5U26	1810-0049	7		NETWORK-RES 12-SIP6.8K OHM X 10	28480	1810-0049
A5U27	1810-0163	6	1	NETWORK-RES 9-SIP200.0 OHM X 8	91637	CSP09C07-201J
A5U28	1810-0121	6	1	NETWORK-RES 9-SIP1.0K OHM X 8	91637	CSP09C07-102J
A5VR1	1902-3092	1	1	DIODE-ZNR 4.99V 2% DO-35 PD=.4W	28480	1902-3092
A5XU11	1200-0654	7	1	SOCKET-IC 40-CONT DIP DIP-SLDR	28480	1200-0654
A5XY1	1200-0761	7	1	SOCKET-XTAL 2-CONT HC-6/U DIP-SLDR	28480	1200-0761
A5Y1	0410-1003	6	1	CRYSTAL-QUARTZ 10.000 MHZ	28480	0410-1003
A6	01611-66506	6	1	BOARD ASSEMBLY,RAM & DISPLAY FORMAT GENERATOR	28480	01611-66506
A6C1	0160-2306	3	2	CAPACITOR-FXD 27PF +-5% 300VDC MICA	28480	0160-2306
A6C2	0160-2306	3		CAPACITOR-FXD 27PF +-5% 300VDC MICA	28480	0160-2306
A6C3	0140-0197	4	1	CAPACITOR-FXD 180PF +-5% 300VDC MICA	72136	DM15F181J0300WV1CR
A6C4	0180-0228	6		CAPACITOR-FXD 22UF+-10% 15VDC TA	56289	150D226X9015B2
A6C5	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A6C6	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A6C7	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A6C8	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A6C9	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A6C10	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-2. Replaceable Parts (Con't)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A6C11	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A6C12	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A6C13	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A6C14	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A6C15	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A6C16	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A6R1	0757-0430	5	3	RESISTOR 2.21K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2211-F
A6R2	0757-0430	5		RESISTOR 2.21K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2211-F
A6R3	0757-0391	7	1	RESISTOR 39.2 1% .125W F TC=0+-100	24546	C4-1/8-T0-39R2-F
A6R4	0757-0430	5		RESISTOR 2.21K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2211-F
A6R5	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A6R6	0757-0409	8	1	RESISTOR 274 1% .125W F TC=0+-100	24546	C4-1/8-T0-274R-F
A6R7	0757-1090	5	1	RESISTOR 261 1% .5W F TC=0+-100	28480	0757-1090
A6TP1	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A6TP2	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A6TP3	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A6TP4	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A6TP5	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A6TP6	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A6TP7	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A6TP8	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A6TP9	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A6TP10	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A6U1	1820-1196	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS174N
A6U2	1820-0683	6	1	IC INV TTL S HEX 1-INP	01295	SN74S04N
A6U3	1820-1285	6	3	IC GATE TTL LS AND-OR-INV 4-INP	01295	SN74LS54N
A6U4	1820-1196	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS174N
A6U5	1820-1430	3	11	IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS161AN
A6U6	1820-1429	0		IC CNTR TTL LS DECD SYNCHRO	01295	SN74LS160AN
A6U7	1820-1430	3		IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS161AN
A6U8	1820-1430	3		IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS161AN
A6U9	1820-1202	7	5	IC GATE TTL LS NAND TPL 3-INP	01295	SN74LS10N
A6U10	1820-1202	7		IC GATE TTL LS NAND TPL 3-INP	01295	SN74LS10N
A6U11	1820-1430	3		IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS161AN
A6U12	1820-1430	3		IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS161AN
A6U13	1818-0237	1	1	IC PMOS 2.5K ROM CHAR GEN 450-NS 3-S	14936	R0-3-2513
A6U14	1820-1042	3	1	IC SHF-RGTR TTL R-S PRL-IN SERIAL-OUT	01295	SN74165N
A6U15	1818-0348	5	8	IC NMOS 1K RAM STAT 3-S	07263	2102LHPC
A6U16	1818-0348	5		IC NMOS 1K RAM STAT 3-S	07263	2102LHPC
A6U17	1818-0348	5		IC NMOS 1K RAM STAT 3-S	07263	2102LHPC
A6U18	1818-0348	5		IC NMOS 1K RAM STAT 3-S	07263	2102LHPC
A6U19	1818-0348	5		IC NMOS 1K RAM STAT 3-S	07263	2102LHPC
A6U20	1818-0348	5		IC NMOS 1K RAM STAT 3-S	07263	2102LHPC
A6U21	1818-0348	5		IC NMOS 1K RAM STAT 3-S	07263	2102LHPC
A6U22	1818-0348	5		IC NMOS 1K RAM STAT 3-S	07263	2102LHPC
A6U23	1820-1202	7		IC GATE TTL LS NAND TPL 3-INP	01295	SN74LS10N
A6U24	1820-1196	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS174N
A6U25	1820-1196	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS174N
A6U26	1820-1200	5	2	IC INV TTL LS HEX	01295	SN74LS05N
A6U27	1820-1158	2	1	IC GATE TTL S AND-OR-INV DUAL 2-INP	01295	SN74S51N
A6U28	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
A6U29	1820-1200	5		IC INV TTL LS HEX	01295	SN74LS05N
A6U30	1820-1415	4	1	IC SCHMITT-TRIG TTL LS NAND DUAL 4-INP	01295	SN74LS13N
A6U31	1820-1470	1	11	IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS157N
A6U32	1820-1470	1		IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS157N
A6U33	1820-1470	1		IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS157N
A6U34	1820-1197	9	1	IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
A6VR1	1902-0041	4		DIODE-ZNR 5.11V 5% DO-35 PD=.4W	28480	1902-0041
A7	01611-66577	1	1	BOARD ASSEMBLY, COMPARATOR	28480	01611-66577
A7C1	0140-0196	3	2	CAPACITOR-FXD 150PF +-5% 300VDC MICA	72136	DM15F151J0300WV1CR
A7C2	0160-2308	5	1	CAPACITOR-FXD 36PF +-5% 300VDC MICA	28480	0160-2308
A7C3	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A7C4	0121-0201	1	1	CAPACITOR-FXD 12PF 500WVDC MICA	28480	0121-0201
A7C5	0180-0228	6		CAPACITOR-FXD 22UF+-10% 15VDC TA	56289	150D226X9015B2
A7C6	0140-0149	6	1	CAPACITOR-FXD 470PF +-5% 300VDC MICA	72136	DM15F471J0300WV1CR
A7C7	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A7C8	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A7C9	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A7C10	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A7C11	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A7C12	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A7C13	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A7C14	0140-0196	3		CAPACITOR-FXD 150PF +-5% 300VDC MICA	72136	DM15F151J0300WV1CR
A7C15	0160-3443	1	3	CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-2. Replaceable Parts (Con't)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A7C16	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A7C17	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A7R1	0757-0413	4	3	RESISTOR 392 1% .125W F TC=0+-100	24546	C4-1/8-T0-392R-F
A7R2	0757-0429	2		RESISTOR 1.82K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1821-F
A7R3	0757-0424	7	2	RESISTOR 1.1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1101-F
A7R4	0757-0424	7		RESISTOR 1.1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1101-F
A7R5	0757-0429	2		RESISTOR 1.82K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1821-F
A7R6	0757-0438	3		RESISTOR 5.11K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5111-F
A7R7	0757-0438	3		RESISTOR 5.11K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5111-F
A7R8	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A7R9	0757-0415	6	1	RESISTOR 475 1% .125W F TC=0+-100	24546	C4-1/8-T0-475R-F
A7R10	2100-2489	9	2	RESISTOR-TRMR 5K 10% C SIDE-ADJ 1-TRN	30983	ET50X502
A7R11	0757-0413	4		RESISTOR 392 1% .125W F TC=0+-100	24546	C4-1/8-T0-392R-F
A7R12	2100-2489	9		RESISTOR-TRMR 5K 10% C SIDE-ADJ 1-TRN	30983	ET50X502
A7TP1	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A7TP2	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A7TP3	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A7TP4	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A7TP5	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A7TP6	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A7U1	1820-1782	8	1	IC MV TTL S MONOSTBL RETRIG/RESET DUAL	34335	AM26S02PC
A7U2	1816-0913	6	11	IC TTL S 64-BIT RAM STAT 110-NS O-C	34335	AM31L01PC
A7U3	1816-0913	6		IC TTL S 64-BIT RAM STAT 110-NS O-C	34335	AM31L01PC
A7U4	1816-0913	6		IC TTL S 64-BIT RAM STAT 110-NS O-C	34335	AM31L01PC
A7U5	1820-1285	6		IC GATE TTL LS AND-OR-INV 4-INP	01295	SN74LS54N
A7U6	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
A7U7	1820-1285	6		IC GATE TTL LS AND-OR-INV 4-INP	01295	SN74LS54N
A7U8	1820-0691	6	2	IC GATE TTL S AND-OR-INV	01295	SN74S64N
A7U9	1820-1202	7		IC GATE TTL LS NAND TPL 3-INP	01295	SN74LS10N
A7U10	1816-0913	6		IC TTL S 64-BIT RAM STAT 110-NS O-C	34335	AM31L01PC
A7U11	1816-0913	6		IC TTL S 64-BIT RAM STAT 110-NS O-C	34335	AM31L01PC
A7U12	1816-0913	6		IC TTL S 64-BIT RAM STAT 110-NS O-C	34335	AM31L01PC
A7U13	1816-0913	6		IC TTL S 64-BIT RAM STAT 110-NS O-C	34335	AM31L01PC
A7U14	1816-0913	6		IC TTL S 64-BIT RAM STAT 110-NS O-C	34335	AM31L01PC
A7U15	1816-0913	6		IC TTL S 64-BIT RAM STAT 110-NS O-C	34335	AM31L01PC
A7U16	1816-0913	6		IC TTL S 64-BIT RAM STAT 110-NS O-C	34335	AM31L01PC
A7U17	1816-0913	6		IC TTL S 64-BIT RAM STAT 110-NS O-C	34335	AM31L01PC
A7U18	1820-1195	7	1	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS175N
A7U19	1820-1203	8	1	IC GATE TTL LS AND TPL 3-INP	01295	SN74LS11N
A7U20	1820-1212	9	3	IC FF TTL LS J-K NEG-EDGE-TRIG	01295	SN74LS112AN
A7U21	1820-0681	4	1	IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
A7U22	1820-1470	1		IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS157N
A7U23	1820-1470	1		IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS157N
A7U24	1820-1470	1		IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS157N
A7U25	1820-1470	1		IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS157N
A7U26	1820-1470	1		IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS157N
A7U27	1820-1470	1		IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS157N
A7U28	1820-1470	1		IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS157N
A7U29	1820-1470	1		IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS157N
A7U30	1820-1418	7		IC DCDR TTL LS BCD-TO-DEC 4-TO-10-LINE	01295	SN74LS42N
A7U31	1820-1202	7		IC GATE TTL LS NAND TPL 3-INP	01295	SN74LS10N
A7U32	1820-0691	6		IC GATE TTL S AND-OR-INV	01295	SN74S64N
A7U33	1820-0686	9	1	IC GATE TTL S AND TPL 3-INP	01295	SN74S11N
A7U34	1820-1212	9		IC FF TTL LS J-K NEG-EDGE-TRIG	01295	SN74LS112AN
A7U35	1810-0041	9	2	NETWORK-RES 9-SIP2.7K OHM X 8	28480	1810-0041
A7U36	1810-0041	9		NETWORK-RES 9-SIP2.7K OHM X 8	28480	1810-0041
A8	01611-66535	1	1	BOARD ASSEMBLY, DATA STORE AND COUNTERS	28480	01611-66535
A8C1	0140-0203	3	2	CAPACITOR-FXD 30PF +-5% 500VDC MICA	72136	DM15E300J0500MV1CR
A8C2	0140-0203	3		CAPACITOR-FXD 30PF +-5% 500VDC MICA	72136	DM15E300J0500MV1CR
A8C3	0160-0196	5	1	CAPACITOR-FXD 24PF +-5% 300VDC MICA	28480	0160-0196
A8C4	0180-0228	6		CAPACITOR-FXD 22UF+-10% 15VDC TA	56289	150D226X9015B2
A8C5	0160-3451	1		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-3451
A8C6	0160-3451	1		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-3451
A8C7	0160-3451	1		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-3451
A8C8	0160-3451	1		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-3451
A8C9	0160-3451	1		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-3451
A8C10	0160-3451	1		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-3451
A8C11	0160-3451	1		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-3451
A8C12	0160-3451	1		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-3451
A8C13	0160-3451	1		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-3451
A8C14	0160-3451	1		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-3451
A8C15	0150-0051	0	1	CAPACITOR-FXD 100PF +80-20% 1KVDC CER	28480	0150-0051

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-2. Replaceable Parts (Con't)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A8C16	0160-3447	5	1	CAPACITOR-FXD 470PF +-10% 1KVDC CER	28480	0160-3447
A8CR1	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A8L1	9140-0210	1	1	INDUCTORRF-CH-MLD 100UH 5% .166DX.385LG	28480	9140-0210
A8R1	0757-0438	3		RESISTOR 5.11K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5111-F
A8R2	0757-0438	3		RESISTOR 5.11K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5111-F
A8R3	0757-0413	4		RESISTOR 392 1% .125W F TC=0+-100	24546	C4-1/8-T0-392R-F
A8R4	0757-0438	3		RESISTOR 5.11K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5111-F
A8R5	0698-5068	9	1	RESISTOR 50 1% .125W F TC=0+-25	28480	0698-5068
A8R6	0698-3113	1	1	RESISTOR 100 5% .125W CC TC=-270/+540	01121	BB1015
A8TP1	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A8TP2	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A8TP3	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A8TP4	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A8TP5	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A8TP6	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A8TP7	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A8TP8	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A8U1	1820-1464	3		IC CNTR TTL BIN ASYNCHRO NEG-EDGE-TRIG	01295	SN74393N
A8U2	1820-1425	6		IC SCHMITT-TRIG TTL LS NAND QUAD 2-INP	01295	SN74LS132N
A8U3	1820-1144	6	1	IC GATE TTL LS NOR QUAD 2-INP	01295	SN74LS02N
A8U4	1820-1423	4	1	IC MV TTL LS MONOSTBL RETRIG DUAL	01295	SN74LS123N
A8U5	1820-1212	9		IC FF TTL LS J-K NEG-EDGE-TRIG	01295	SN74LS112AN
A8U6	1820-1430	3		IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS161AN
A8U7	1820-1199	1		IC INV TTL LS HEX 1-INP	01295	SN74LS04N
A8U8	1820-1210	7	1	IC GATE TTL LS AND-OR-INV DUAL 2-INP	01295	SN74LS51N
A8U9	1820-1430	3		IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS161AN
A8U10	1820-1430	3		IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS161AN
A8U11	1820-1430	3		IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS161AN
A8U12	1820-1130	0	1	IC GATE TTL S NAND 13-INP	01295	SN74S133N
A8U13	1820-1430	3		IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS161AN
A8U14	1820-1430	3		IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS161AN
A8U15	1820-1116	2	1	IC FF TTL J-K BAR POS-EDGE-TRIG	01295	SN74109N
A8U16	1820-1418	7		IC DCDR TTL LS BCD-TO-DEC 4-TO-10-LINE	01295	SN74LS42N
A8U17	1820-1439	2		IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE	01295	SN74LS258AN
A8U18	1820-1439	2		IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE	01295	SN74LS258AN
A8U19	1820-1439	2		IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE	01295	SN74LS258AN
A8U20	1820-1439	2		IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE	01295	SN74LS258AN
A8U21	1820-1439	2		IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE	01295	SN74LS258AN
A8U22	1820-1439	2		IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE	01295	SN74LS258AN
A8U23	1820-1201	6		IC GATE TTL LS AND QUAD 2-INP	01295	SN74LS08N
A8U24	1820-1418	7		IC DCDR TTL LS BCD-TO-DEC 4-TO-10-LINE	01295	SN74LS42N
A8U25	1816-0728	1	4	IC TTL S RAM STAT 50-NS 0-C	18324	N82S09I
A8U26	1816-0728	1		IC TTL S RAM STAT 50-NS 0-C	18324	N82S09I
A8U27	1816-0728	1		IC TTL S RAM STAT 50-NS 0-C	18324	N82S09I
A8U28	1816-0728	1		IC TTL S RAM STAT 50-NS 0-C	18324	N82S09I
A8U29	1820-1205	0	1	IC GATE TTL LS AND DUAL 4-INP	01295	SN74LS21N
A8U30	1810-0055	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
A8U31	1810-0055	2		IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE	01295	SN74LS258AN
A8U32	1810-0055	2		NETWORK-RES 9-SIP 10.0K OHM ×8	28480	1810-0055
A8U33	1810-0055	5		NETWORK-RES 9-SIP 10.0K OHM ×8	28480	1810-0055
A8XU25	1200-0567	1	4	SOCKET-IC 28-CONT DIP DIP-SLDR	28480	1200-0567
A8XU26	1200-0567	1		SOCKET-IC 28-CONT DIP DIP-SLDR	28480	1200-0567
A8XU27	1200-0567	1		SOCKET-IC 28-CONT DIP DIP-SLDR	28480	1200-0567
A8XU28	1200-0567	1		SOCKET-IC 28-CONT DIP DIP-SLDR	28480	1200-0567
A9				BOARD ASSEMBLY, PERSONALITY		
A9				BOARD ASSEMBLY-PERSONALITY (SEE MANUAL SUPPLEMENT FOR OPTION INSTALLED IN YOUR INSTRUMENT)		
A10				BOARD ASSEMBLY-ROM (SEE MANUAL SUPPLEMENT FOR OPTION INSTALLED IN YOUR INSTRUMENT)		
A11				ASSEMBLY-PERSONALITY PANEL (SEE MANUAL SUPPLEMENT FOR OPTION INSTALLED IN YOUR INSTRUMENT)		
A12	01611-62101	9	1	ASSEMBLY, EXTERNAL PROBE	28480	01611-62101

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-2. Replaceable Parts (Con't)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A12A1	01611-66516	8		BOARD ASSEMBLY-PROBE	28480	01611-66516
A12CP1	10230-62101	7	9	PROBE ASSEMBLY, HOOK-TYPE	28480	10230-62101
A12MP1	0624-0306	3	4	SCREW-TPG 2-28 .5-IN-LG PAN-HD-POZI STL	28480	0624-0306
A12MP2	2200-0111	2	6	SCREW-MACH 4-40 .5-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
A12MP1	5040-8261	2	1	BOTTOM POD	28480	5040-8261
A12MP2	5040-8260	1	1	COVER, POD	28480	5040-8260
A12MP3	7120-5707	7	1	LABEL, EXTERNAL PROBE	28480	7120-5707
A12MP4	5040-0563	1	1	CONNECTOR CLIP	28480	5040-0563
A12MP5	1540-0320	4	1	CASE, VINYL	28480	1540-0320
A12W1	01611-61622	7		CABLE, EXTERNAL PROBE	28480	01611-61622
A12W2	5061-1215	6	1	CABLE, BLACK, PIN ADAPTER	28480	5061-1215
A12W3	5061-1217	8	1	CABLE, WHITE/BLACK PIN ADAPTER	28480	5061-1217
A12W4	5061-1218	9	1	CABLE, WHITE/BROWN PIN ADAPTER	28480	5061-1218
A12W5	5061-1219	0	1	CABLE, WHITE/RED PIN ADAPTER	28480	5061-1219
A12W6	5061-1220	3	1	CABLE, WHITE/ORANGE PIN ADAPTER	28480	5061-1220
A12W7	5061-1221	4	1	CABLE, WHITE/YELLOW PIN ADAPTER	28480	5061-1221
A12W8	5061-1222	5	1	CABLE, WHITE/GREEN PIN ADAPTER	28480	5061-1222
A12W9	5061-1223	6	1	CABLE, WHITE/BLUE PIN ADAPTER	28480	5061-1223
A12W10	5061-1224	7	1	CABLE, WHITE/VIOLET PIN ADAPTER	28480	5061-1224
A12W1MP1	2200-0091	7	2	SCREW-MACH 4-40 .562-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
A12W1MP2	3050-0235	3		WASHER-FL MTLC NO. 4 .117-IN-ID	28480	3050-0235
A12W1MP3	2190-0019	6		WASHER-LK HLCL NO. 4 .115-IN-ID	28480	2190-0019
A12W1MP4	2260-0002	6	2	NUT-HEX-DBL-CHAM 4-40-THD .062-IN-THK	00000	ORDER BY DESCRIPTION
A12W1MP1	01611-61203	0	1	CABLE CLAMP	28480	01611-61203
A12A1C1	0160-3451	1		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-3451
A12A1C2	0180-022R	6		CAPACITOR-FXD 22UF+-10% 15VDC TA	56289	150D226X9015B2
A12A1CR1	1901-0025	2	1	DIODE-GEN PRP 100V 200MA DO-7	28480	1901-0025
A12A1E1	1460-1473	0	9	SPRING-CONT BE CU NI	28480	1460-1473
A12A1E2	1460-1473	0		SPRING-CONT BE CU NI	28480	1460-1473
A12A1E3	1460-1473	0		SPRING-CONT BE CU NI	28480	1460-1473
A12A1E4	1460-1473	0		SPRING-CONT BE CU NI	28480	1460-1473
A12A1E5	1460-1473	0		SPRING-CONT BE CU NI	28480	1460-1473
A12A1E6	1460-1473	0		SPRING-CONT BE CU NI	28480	1460-1473
A12A1E7	1460-1473	0		SPRING-CONT BE CU NI	28480	1460-1473
A12A1E8	1460-1473	0		SPRING-CONT BE CU NI	28480	1460-1473
A12A1E9	1460-1473	0		SPRING-CONT BE CU NI	28480	1460-1473
A12A1U1	1820-1829	4	2	IC	28480	1820-1829
A12A1U2	1820-1829	4		IC	28480	1820-1829
A12A1U3	1810-0293	3	2	NETWORK-RC 11 PIN SIP; 0.1 IN SPACING	28480	1810-0293
A12A1U4	1810-0293	3		NETWORK-RC 11 PIN SIP; 0.1 IN SPACING	28480	1810-0293

Table 6-3. List of Manufacture's Codes

Mfr No.	Manufacturer Name	Address		Zip Code
00000	ANY SATISFACTORY SUPPLIER			
01121	ALLEN-BRADLEY CO	MILWAUKEE	WI	53204
01295	TEXAS INSTR INC SEMICOND CMPNT DIV	DALLAS	TX	75222
01928	RCA CORP SOLID STATE DIV	SOMERVILLE	NJ	08876
03888	KDI PYROFILM CORP	WHIPPANY	NJ	07981
04713	MOTOROLA SEMICONDUCTOR PRODUCTS	PHOENIX	AZ	85062
07263	FAIRCHILD SEMICONDUCTOR DIV	MOUNTAIN VIEW	CA	94042
14936	GENERAL INSTR CORP SEMIDON PROD GP	HICKSVILLE	NY	11802
18324	SIGNETICS CORP	SUNNYVALE	CA	94086
24546	CORNING GLASS WORKS (BRADFORD)	BRADFORD	PA	16701
27014	NATIONAL SEMICONDUCTOR CORP	SANTA CLARA	CA	95051
27167	CORNING GLASS WORKS (WILMINGTON)	WILMINGTON	NC	28401
27777	VARO SEMICONDUCTOR INC	GARLAND	TX	75040
28480	HEWLETT-PACKARD CO CORPORATE HQ	PALO ALTO	CA	94304
30983	MEPCO/ELECTRA CORP	SAN DIEGO	CA	92121
34335	ADVANCED MICRO DEVICES INC	SUNNYVALE	CA	94086
56289	SPRAGUE ELECTRIC CO	NORTH ADAMS	MA	01247
72136	ELECTRO MOTIVE CORP SUB IEC	WILLIMANTIC	CT	06226
75042	TRW INC PHILADELPHIA DIV	PHILADELPHIA	PA	19108
75915	LITTELFUSE INC	DES PLAINES	IL	60016
84411	TRW CAPACITOR DIV	OGALLALA	NE	69163
91637	DALE ELECTRONICS INC	COLUMBUS	NE	68601

See introduction to this section for ordering information
*Indicates factory selected value

SECTION VII

MANUAL CHANGES

7-1. INTRODUCTION.

7-2. This section contains information for adapting this manual to instruments for which the content does not apply directly.

7-3. MANUAL CHANGES.

7-4. To adapt this manual to your instrument, refer to table 7-1 and make all of the manual changes listed opposite your instrument serial number. Perform these changes in the sequence listed.

7-5. If your instrument serial number is not listed on the title page of this manual or in table 7-1 below, it may be documented in a yellow MANUAL CHANGES supplement. For additional information about serial number coverage, refer to INSTRUMENTS COVERED BY MANUAL in Section I.

Table 7-1. Manual Changes

Serial Prefix	Make Changes
1635A	5 thru 1
Instruments with Options 068 or 080 installed	5 thru 2
1723A	5 thru 3
2007A	5 and 4
2017A	5

7-6. MANUAL CHANGE INSTRUCTIONS.

CHANGE 1

Paragraph 5-8,
Delete: 5-8. COMPARATOR ADJUSTMENT.

Table 6-2,
A7: Change HP Part No. and Mfr Part No. to 01611-66507.
A7C2: Change to HP Part No. 0160-2204, CAPACITOR-FXD 100PF +—5% 300WVDC MICA, Mfr Code 28480, Mfr Part No. 0160-2204.
A7C4: Change to HP Part No. 0121-0202, CAPACITOR-FXD 15PF +—5% 500WVDC CER, Mfr Code 72136, Mfr Part No. DM15C150J0500WV1CR.
A7C6: Change to HP Part No. 0140-0199, CAPACITOR-FXD 240PF ±5% 300WVDC MICA, Mfr Code 72136, Mfr Part No. DM15F241J0300WV1CR.
Delete: A7R9.
Delete: A7R10.
Delete: A7U34.
A7U36: Change Reference Designation to A7U34.
A8: Change HP Part No. and Mfr Part No. to 01611-66508.
Delete: A8U30.
Delete: A8U31.
Figure 8-13, Service Sheet 7 (Sheet 4 of 4):
Replace with figure 7-1.
Figure 8-14, Service Sheet 8 (Sheet 1 of 6):
Replace with figure 7-2.
Figure 8-14, Service Sheet 8 (Sheet 2 of 6):
Replace with figure 7-3.
Figure 8-14, Service Sheet 8 (Sheet 4 of 6):
Replace with figure 7-4.

CHANGE 2

Figure 8-4 (8 Sheets):
Replace with figure 7-5 (5 Sheets).

CHANGE 3

Table 6-2,
A7: Change HP Part No. and Mr. Part No. to 01611-66507, Rev B.
A7C4: Change to HP Part No. 0121-0434, CAPACITOR-VAR TRMR-AIR 2-19, 3 PF 350V, Mfr Code 74970, Mfr Part No. 189-0507-125.
Delete: A7R12.
Figure 8-13, Service Sheet 7 (sheet 4 of 4): Replace with figure 7-6.

CHANGE 4

Table 6-2,
MP10: Change HP Part No. and Mfr. Part No. to 01611-00202, CD 1.

CHANGE 5

Table 6-2,

A3: Change HP Part No. and Mfr Part No. to 01611-66503, CD 3.

A7: Change HP Part No. and Mfr Part No. to 01611-66507, CD 7.

H14: Change HP Part No. and Mfr Part No. to 2680-0128, CD 7.

Add: MP4, HP Part No 1520-0063, CD 0, Qty 1, Description MOUNT, VIBRATION, Mfr Code 70485, Mfr Part No. OBD.

MP10: Change HP Part No. and Mfr Part No. to 01611-00202, CD 1.

Delete: MP27.

Delete: MP75.

A1XU1: Change HP Part No. and Mfr Part No. to 1200-0474, CD 9.

A3C28: Change to HP Part No. 0160-3665, CD 9, Qty 6, Description CAPACITOR-FXD .01UF + 80–20% 500 WVDC CER, Mfr Code 28480, Mfr Part No. 0160-3665.

A3C29: Delete Qty.

A3R45: Change Qty to 1.

A3R60: Change to HP Part No. 2100-3214, CD 0, Qty 1, Description RESISTOR-TRMR 100K 10% C TOP-ADJ 1-TRN, Mfr Code 73138, Mfr Part No. 72-112-0.

Delete: A7C15.

A7C16: Change to HP Part No. 0160-2055, CD 9, Description CAPACITOR-FXD .01UF +80-20% 100 WVDC CER, Mfr Code 28480, Mfr Part No. 0160-2055.

Delete: A7C17.

A7U35: Change HP Part No. and Mfr Part No. to 1820-0041, CD 0.

A7U36: Change HP Part No. and Mfr Part No. to 1820-0041, CD 0.

A8C6: Delete Qty.

Delete: A8C13.

Delete: A8C14.

Delete: A8C15.

Delete: A8C16.

Delete: A8R5.

Delete: A8R6.

A8U25: Change to HP Part No. 1816-0728, CD 1, Qty 4, Description IC 82S09I RAM TTL, Mfr Code 18324, Mfr Part No. 82S09I.

A8U26: Change to HP Part No. 1816-0728, CD 1, Description IC 82S09I RAM TTL, Mfr Code 18324, Mfr Part No. 82S09I.

A8U27: Change to HP Part No. 1816-0728, CD 1, Description IC 82S09I RAM TTL, Mfr Code 18324, Mfr Part No. 82S09I.

A8U28: Change to HP Part No. 1816-0728, CD 1, Description IC 82S09I RAM TTL, Mfr Code 18324, Mfr Part No.82S09I.

A12W1H1: Change to HP Part No. 2200-0111, CD 2, Description SCREW-MACH 4-40 .5-IN-LG PAN-HD-POZI, Mfr Code 28480, Mfr Part No. 2200-0111.

A12W1MP1: Change HP Part No. and Mfr No. to 01611-61201,CD 8.

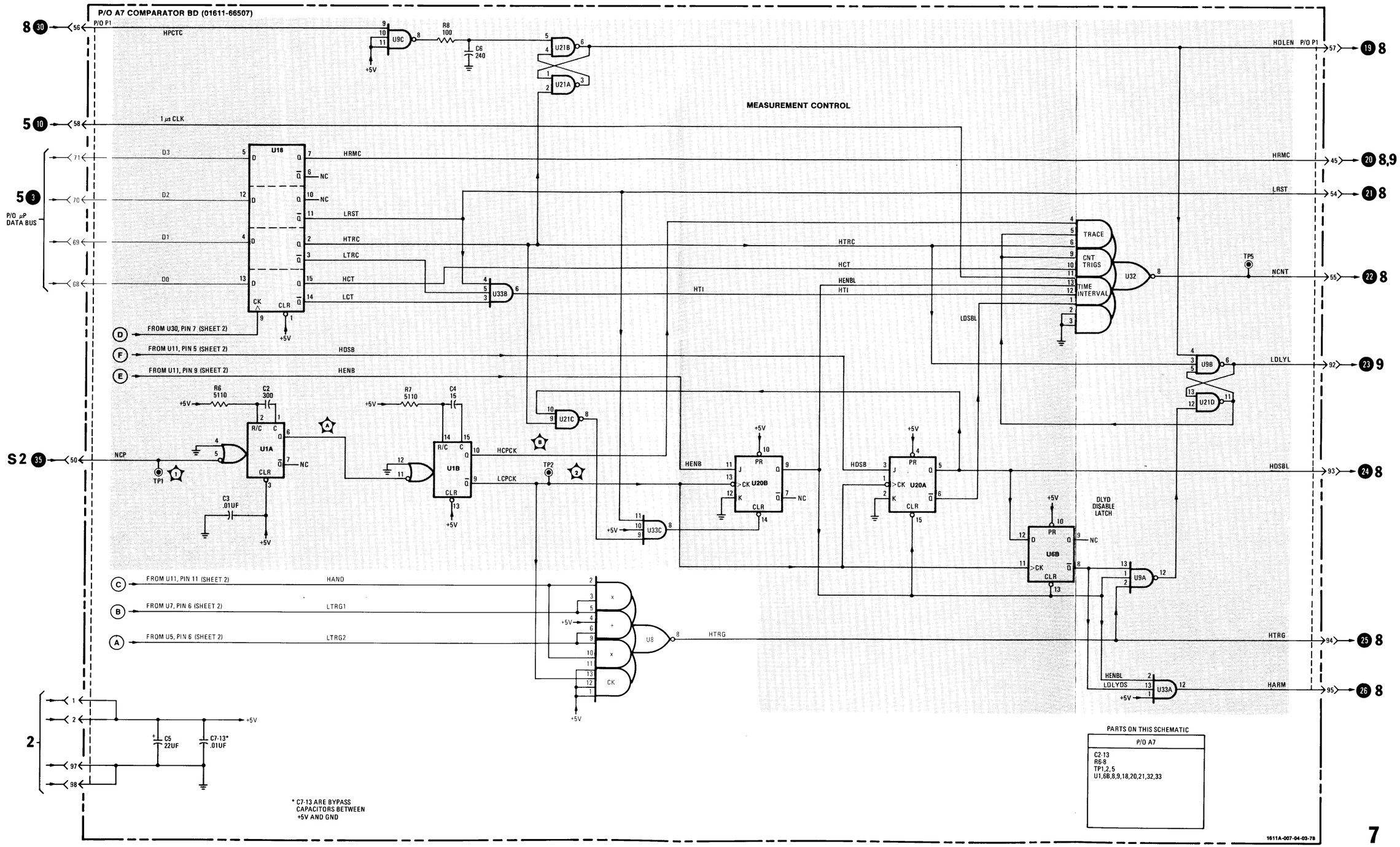
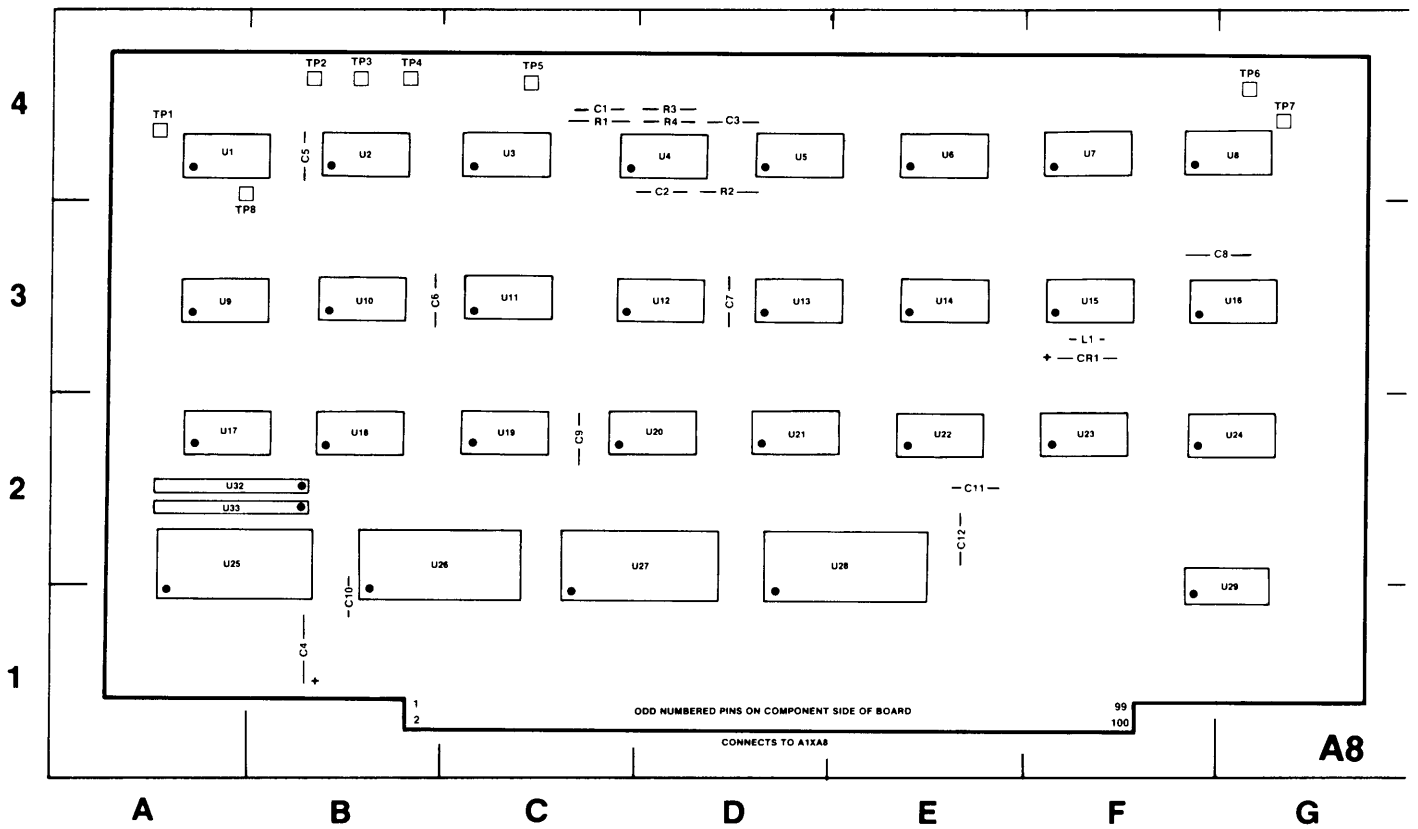


Figure 7-1. Replacement for figure 8-13, Service Sheet 7, (Sheet 4 of 4)



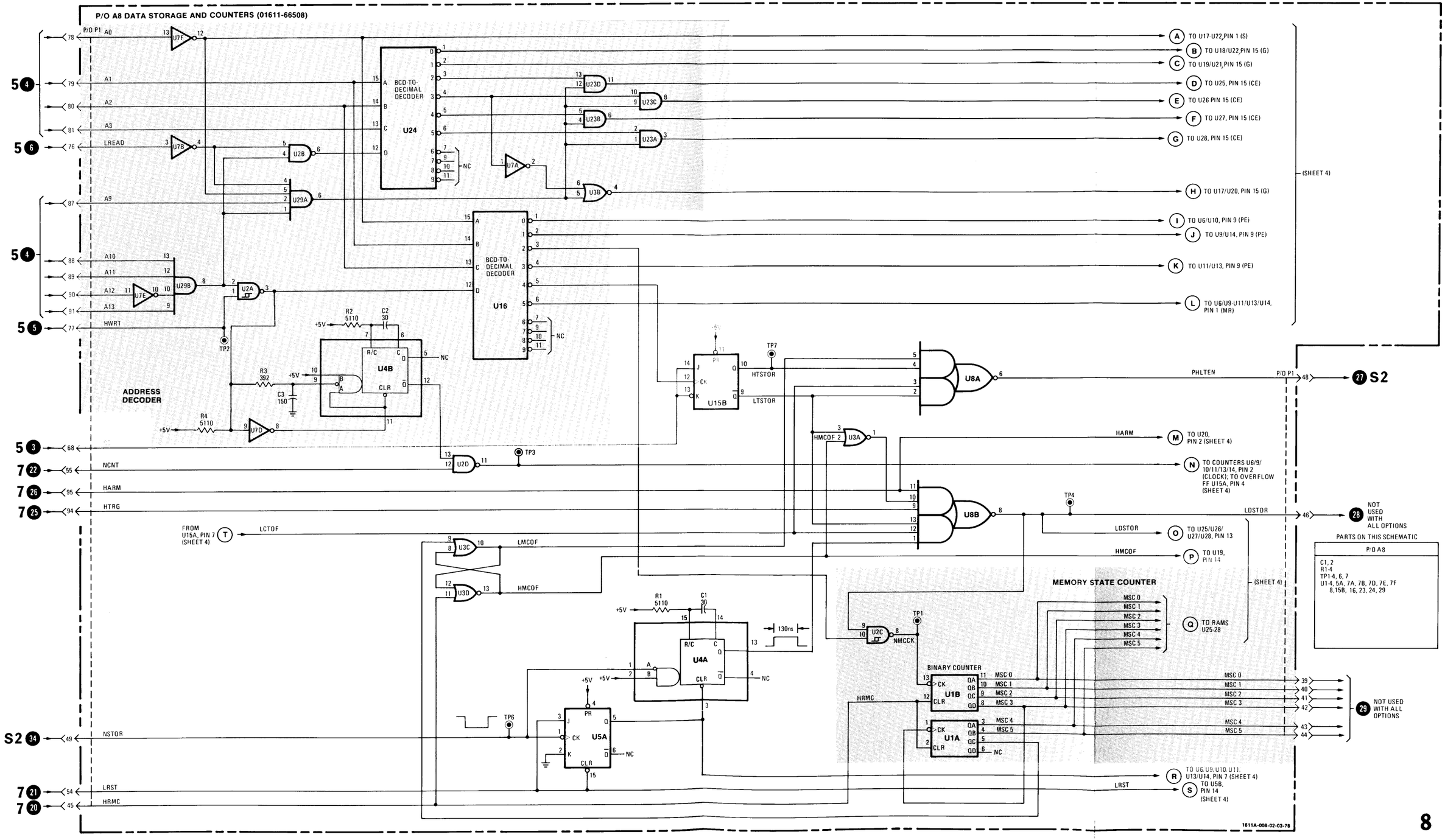
Data Store and Counters Board A8 Component Locator
(01611-66508)

REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC
C1	C-4	TP3	B-4	U15	F-3
C2	D-4	TP4	B-4	U16	G-3
C3	D-4	TP5	C-4	U17	A-2
C4	B-1	TP6	C-4	U18	B-2
C5	B-4	TP7	G-4	U19	C-2
C6	B-3	TP8	A-3	U20	D-2
C7	D-3	U1	A-4	U21	D-2
C8	G-3	U2	B-4	U22	E-2
C9	C-2	U3	C-4	U23	F-2
C10	B-1	U4	D-4	U24	G-2
C11	E-2	U5	D-4	U25	A-2
C12	E-2	U6	E-4	U26	B-2
CR1	F-3	U7	F-4	U27	D-2
L1	F-3	U8	G-4	U28	E-2
R1	C-4	U9	A-3	U29	G-2
R2	D-4	U10	B-3	U32	A-2
R3	D-4	U11	C-3	U33	A-2
R4	D-4	U12	D-3		
TP1	A-4	U13	D-3		
TP2	B-4	U14	E-3		

ICs ON THIS SCHEMATIC

IC REF DES	HP PART NO.	MFR PART NO.
U1	1820-1464	SN74393N
U2	1820-1425	SN74LS132N
U3	1820-1144	SN74LS02N
U4	1820-1423	SN74LS123N
U5	1820-1212	SN74LS112N
U6, 9-11, 13, 14	1820-1430	SN74LS161N
U7	1820-1199	SN74LS04N
U8	1820-1210	SN74LS51N
U12	1820-1130	SN74S13N
U15	1820-1116	SN74109N
U16, 24	1820-1418	SN74LS42N
U17-22	1820-1439	SN74LS258N
U23	1820-1201	SN74LS08N
U25-28	1816-0728	82S09I
U29	1820-1205	SN74LS21N
U32, 33	1810-0055	1810-0055

Figure 7-2. Replacement for Figure 8-14. Service Sheet 8, Assembly A8 Component Locator (Sheet 1 of 6)



8

Figure 7-3.
***Replacement** for figure 8-14,*
***Service** Sheet 8 (Sheet 2 of 6)*
7-7/(7-8 blank)

P/O A8 DATA STORAGE AND COUNTERS (01611-66508)

HIGH SPEED MEMORY

MEMORY STATE COUNT (SHEET 2) Q

MSC0 MSC1 MSC1 MSC3 MSC4 MSC5

P/O P1 EXT0 EXT1 EXT2 EXT3 EXT4 EXT5 EXT6 EXT7

48 S4

FROM U8B PIN 8 (SHEET 1) O

LDSTOR

FROM U23D PIN 11 (SHEET 2) D

U25 9-BY-64 RAM

INP D0 INP D1 INP D2 INP D3 INP D4 INP D5 INP D6 INP D7

33 S2

FLAG 0 FLAG 1 FLAG 2 FLAG 3

39 S2

FROM U23C PIN 8 (SHEET 2) E

U26 9-BY-64 RAM

INP A0 INP A1 INP A2 INP A3 INP A4 INP A5 INP A6 INP A7

FROM U23B PIN 6 (SHEET 2) F

32 S2

U27 9-BY-64 RAM

INP A8 INP A9 INP A10 INP A11 INP A12 INP A13 INP A14 INP A15

FROM U23A PIN 3 (SHEET 2) G

U28 9-BY-64 RAM

FROM P1, PIN 95 (SHEET 2) M HARM

FROM U5A, PIN 5 R FROM U2D, PIN 11 N L FROM U16, PIN 6

TO U7C, PIN 5 A

P/O U33 R=10K

P/O U32 R=10K

P/O U33 R=10K

P/O U32 R=10K

HCTOF

U20 2-TO-1 DATA SELECTOR

U17 2-TO-1 DATA SELECTOR

U22 2-TO-1 DATA SELECTOR

U18 2-TO-1 DATA SELECTOR

DATA SELECTOR

FROM U3B, PIN 4 H

FROM U7F, PIN 12 A

FROM U24, PIN 1 B

FROM U24, PIN 2 C

5 3 µP DATA BUS

7 23 24 7

P/O P1

LDLYL HDSBL

7 30 19 7

HPCTC HOLEN

FROM U16 PIN 2 (SHEET 2) J

FROM U16 PIN 1 (SHEET 2) I

PASS COUNTER

U14 BINARY COUNTER

U9 BINARY COUNTER

U6 BINARY COUNTER

U10 BINARY COUNTER

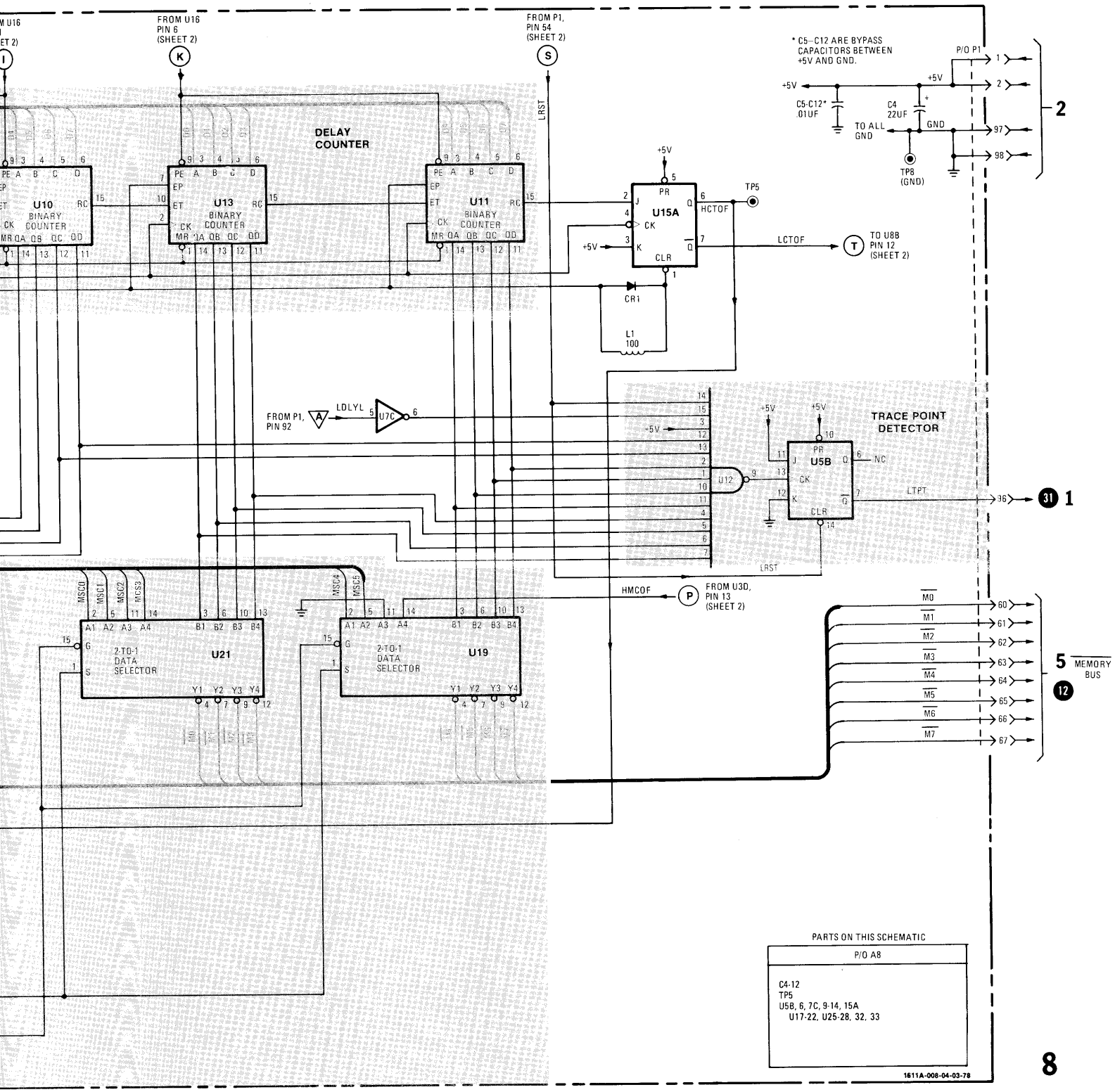


Figure 7-4.
Replacement for figure 8-14,
Service Sheet 8 (Sheet 4 of 6)

NOTE

Procedures in this figure apply only to instruments with Option 068 or 080 installed.

SIGNATURE ANALYSIS PROCEDURE NO. 1.

a. Set 1611A LINE switch to off position.

b. Remove A6, A7, A8, and A10 assemblies from 1611A.

NOTE

The boards installed in the 1611A for the following measurements depend upon the Troubleshooting Tree. Follow the procedure given in the Troubleshooting Tree.

c. Ground A5U3, pin 6.

d. Set signature analyzer controls as follows:

START ....
STOP ....
CLOCK ....
HOLD .... Released

e. Connect signature analyzer probe to the following circuit points:

START .... A5U11, Pin 36
STOP .... A5U11, Pin 36
CLOCK .... A5U11, Pin 18
GND .... A5TP9 (GND)

f. Set 1611A LINE switch to on position.

g. Verify that signature measurements called out in troubleshooting tree match following table.

MEASUREMENT NUMBER	TEST POINT	SIGNATURE
101	V_H	755U
102	$\overline{\text{MEMORY}}$ BUS	
	A5U9, PIN 13	V_H
	A5U9, PIN 9	V_H
	A5U9, PIN 1	V_H
	A5U9, PIN 5	V_H
	A5U8, PIN 13	V_H
	A5U8, PIN 9	V_H
	A5U8, PIN 1	V_H
	A5U8, PIN 5	V_H
103	DATA BUS	
	A5U20, PIN 8	H335
	A5U20, PIN 11	V_{LP}
	A5U20, PIN 6	V_{LP}
	A5U20, PIN 3	H335
	A5U10, PIN 8	H335
	A5U10, PIN 11	H335
	A5U10, PIN 6	V_{LP}
	A5U10, PIN 3	V_{LP}
104	μP OUTPUTS	
	A5U11, PIN 10	H335
104 (Cont'd)	A5U11, PIN 9	V_{LP}
	A5U11, PIN 8	V_{LP}
	A5U11, PIN 7	H335
	A5U11, PIN 3	H335
	A5U11, PIN 4	H335
	A5U11, PIN 5	V_{LP}
	A5U11, PIN 6	V_{LP}
105	ADDRESS BUS	
	A5U2, PIN 13	64 HU
	A5U2, PINS 9, 8	9P9F
	A5U12, PINS 2, 3	HPF6
	A5U2, PINS 1, 3	UF9P
	A5U2, PINS 4, 6	A8H9
	A5U12, PINS 4, 5	2225
	A5U12, PINS 6, 7	0258
	A5U12, PINS 14, 13	H6PP
	A5U12, PINS 12, 11	074P
	A5U12, PINS 10, 9	HU57
	A5U21, PINS 12, 11	F1PF
	A5U21, PINS 10, 9	722H
	A5U21, PINS 2, 3	050U
	A5U21, PINS 4, 5	F44F
	A5U21, PINS 6, 7	A66A
106	A6U30, PIN 5	9P9F
	A6U30, PIN 4	HPF 6
	A6U30, PIN 1	A8H9
	A6U29, PIN 11	UF9P
107	A6U29, PIN 10	89F1
	A6U30, PIN 6	HA34
	A6U29, PIN 8	AU6C
108	A5U11, PIN 17	V_{LP}
	A5U3, PIN 4	V_{HP}
109	A8U17, PIN 15	V_H
	A8U18, PIN 15	V_H
	A8U19, PIN 15	V_H
	A8U20, PIN 15	V_H
	A8U21, PIN 15	V_H
	A8U22, PIN 15	V_H
110	A8U24, PIN 2	V_H
	A8U24, PIN 1	V_H
	A8U24, PIN 12	V_H
	A8U24, PIN 13	722H
	A8U24, PIN 14	050U
	A8U24, PIN 15	F44F
	A8U29, PIN 6	V_L
	A8U29, PIN 8	A41U
	A8U29, PIN 5	H335
	A8U29, PIN 4	V_{LP}
	A8U29, PIN 10	AC99
111	A6U26, PIN 12	1079
	A6U26, PIN 10	V_H
	A6U26, PIN 8	V_H
	A6U26, PIN 6	1079
	A6U26, PIN 4	1079
	A6U26, PIN 2	1079
	A6U29, PIN 2	V_H
	A6U29, PIN 6	V_H
112	A6U25, PIN 2	6526
	A6U25, PIN 5	V_L
	A6U25, PIN 7	V_L
	A6U25, PIN 10	6526
	A6U25, PIN 12	6526
	A6U25, PIN 15	6526
	A6U28, PIN 9	V_L
	A6U28, PIN 5	V_L

V_H = 755U, V_{HP} = 755U, V_L = 0000, V_{LP} = 0000

SIGNATURE ANALYSIS PROCEDURE NO. 2

a. Set 1611A LINE switch to off position.

b. Remove A6, A7, A8, and A10 assemblies from 1611A.

c. Reinstall A6 on extender board A14.

d. Ground A5U3, pin 6.

e. Set signature analyzer controls as follows:

START ....
STOP ....
CLOCK ....
HOLD .... Released

f. Connect signature analyzer probe to the following circuit points:

START .... A5U11, Pin 36
STOP .... A5U11, Pin 36
CLOCK A6TP3
GND .... A5TP9 (GND)

g. Set 1611A LINE switch to on postion.

h. Verify that signature measurements called out in troubleshooting tree match following table.

MEASUREMENT NUMBER	TEST POINT	SIGNATURE
201	V_H	7A70
202	A6U33, PIN 12	6H44
	A6U33, PIN 9	PF45
	A6U33, PIN 7	7H02
	A6U33, PIN 4	355A
	A6U32, PIN 12	3P32
	A6U32, PIN 9	9A40
202 (Cont'd)	A6U32, PIN 7	AAHA
	A6U32, PIN 4	A077
	A6U31, PIN 12	F86A
	A6U31, PIN 9	AF5U
	A6U31, PIN 7	V_{LP}

V_H = 7A70, V_{LP} = 0000

SIGNATURE ANALYSIS PROCEDURE NO. 3

a. Set 1611A LINE switch to off position.

b. Remove A6, A7, A8, A9, and A10 assemblies from 1611A.

c. Reinstall A6 on extender board A14.

d. Ground A5U3, pin 6.

e. Set signature analyzer controls as follows:

START ....
STOP ....
CLOCK ....
HOLD .... Released

f. Connect signature analyzer probe to the following circuit points:

START A6TP4
STOP A6TP4
CLOCK A6TP2
GND .... A6TP10 (GND)

g. Set 1611A LINE switch to on position.

h. Verify that signature measurements called out in troubleshooting tree match following table.

MEASUREMENT NUMBER	TEST POINT	SIGNATURE
301	V_H	7092
302	A6U15, PIN 12	5U1F
	A6U16, PIN 12	V_L or V_{LP}
	A6U17, PIN 12	V_L or V_{LP}
	A6U18, PIN 12	5U1F
	A6U19, PIN 12	5U1F
	A6U20, PIN 12	5U1F
	A6U21, PIN 12	V_L or V_{LP}
	A6U22, PIN 12	V_L or V_{LP}
303	A6U33, PIN 12	H93A
	A6U33, PIN 9	5UA3
	A6U33, PIN 7	U869
	A6U33, PIN 4	57PC
	A6U32, PIN 12	PPPP
	A6U32, PIN 9	U6P0

Figure 7-5 (Sheet 1 of 5).
Replacement for figure 8-4. 1611A Troubleshooting

MEASUREMENT NUMBER	TEST POINT	SIGNATURE
303 (Cont'd)	A6U32, PIN 7	05F9
	A6U32, PIN 4	065F
	A6U31, PIN 12	1U2U
	A6U31, PIN 9	2U8P
	A6U31, PIN 7	V_{HP}
304	A6U33, PIN 14	H93A
	A6U33, PIN 11	5UA3
	A6U33, PIN 5	U869
	A6U33, PIN 2	57PC
	A6U32, PIN 14	PPPP
	A6U32, PIN 11	U6P0
	A6U32, PIN 5	05F9
	A6U32, PIN 2	065F
	A6U31, PIN 14	1U2U
	A6U31, PIN 11	2U8P
V_H = 7092, V_{HP} = 7092, V_L = 0000, V_{LP} = 0000		

SIGNATURE ANALYSIS PROCEDURE NO. 4.

a. Set 1611A LINE switch to off position.

b. Remove A6, A7, A8, A9, and A10 assemblies from 1611A.

c. Reinstall A6 on extender board A14A.

d. Ground A5U3, pin 6.

e. Set signature analyzer controls as follows:

START .....]
STOP .....]=
CLOCK .....]
HOLD ..... Released

f. Connect signature analyzer probe to the following circuit points:

START A6TP4
STOP A6TP4
CLOCK A6TP7
GND ..... A6TP10 (GND)

g. Set1611A LINE switch to on position.

h. Verify that signature measurements called out in troubleshooting tree match following table.

MEASUREMENT NUMBER	TEST POINT	SIGNATURE
401	V_H	31PA
402	A6U24, PIN 2	8791
	A6U24, PIN 5	V_L or V_{LP}
	A6U24, PIN 7	V_L or V_{LP}
	A6U24, PIN 10	8791
	A6U24, PIN 12	8791
402 (Cont'd)	A6U24, PIN 15	8791
	A6U1, PIN 13	V_L or V_{LP}
	A6U27, PIN 9	V_L or V_{LP}
403	A6TP5	4UF5
404	A6U10, PIN 4	81UF
	A6U10, PIN 5	9PP0
405	A6U27, PIN 13	2F02
	A6U27, PIN 10	31PA and 0000 Alternating
406	A6U1, PIN 3	5H5A
	A6U1, PIN 4	HF38
	A6U1, PIN 6	7F9C
	A6U1, PIN 14	8AH9
407	A6U1, PIN 2	7A8U
	A6U1, PIN 5	3P84
	A6U1, PIN 7	5CP4
	A6U1, PIN 10	408A
	A6U1, PIN 12	V_L
	A6U1, PIN 15	8F56
408	A6U14, PIN 5	F33H
	A6U14, PIN 4	047F
	A6U14, PIN 3	29C3
	A6U14, PIN 14	288A
	A6U14, PIN 13	186A
409	A6U14, PIN 2	V_{HP}
	A6U14, PIN 9	PU0H
	A6U14, PIN 7	HPP7
410	A6U3, PIN 6	HA0H
	A6U2, PIN 2	PCP7
V_H = 31PA, V_{HP} = 31PA, V_L = 0000, V_{LP} = 0000		

SIGNATURE ANALYSIS PROCEDURE NO. 5.

SETUP PROCEDURE

a. Set 1611A LINE switch to off position.

b. Remove A6, A7, and A8 assemblies from from 1611A.

c. Reinstall A6 on extender board A14.

d. Set signature analyzer controls as follows:

START .....]
STOP .....]=
CLOCK .....]
HOLD ..... Depressed

e. Connect signature analyzer probe to the following circuit points:

START ..... A6U33, Pin 13
STOP ..... A6U33, Pin 13
CLOCK ..... A5U11, Pin 18
GND ..... A5TP9 (GND)

NOTE

Connect CLOCK probe to A6TP3 for measurements 503, 504, and 505.

f. Set 1611A LINE switch to on position.

MEASUREMENT PROCEDURE

a. Ground (+) side of A5C3.

b. Place signature analyzer probe on pin to be measured.

c. Press and release RESET on probe.

d. Release ground on A5C3 and take reading. Verify that reading matches value in following table.

e. Repeat steps a thru d for each measurement.

MEASUREMENT NUMBER	TEST POINT	SIGNATURE
	V_H	4596
501	A6U26, PIN 12	496A
	A6U26, PIN 10	3917
	A6U26, PIN 8	687P
	A6U26, PIN 6	902A
	A6U26, PIN 4	A5C4
	A6U26, PIN 2	AH58
	A6U29, PIN 2	8P3U
	A6U29, PIN 6	A0A6
502	A6U25, PIN 2	0FUF
	A6U25, PIN 5	7F81
	A6U25, PIN 7	2HP8
	A6U25, PIN 10	H5CF
	A6U25, PIN 12	P022
	A6U25, PIN 15	P8FP
	A6U28, PIN 9	FCA9
	A6U28, PIN 5	P530
503	A6U15, PINS 12, 11	0FUF
504	A6U16, PINS 12, 11	7F81
	A6U17, PINS 12, 11	2HP8
	A6U18, PINS 12, 11	H5CF
	A6U19, PINS 12, 11	P022
	A6U20, PINS 12, 11	P8FP
503 * 504 * (Cont'd)	A6U21, PINS 12, 11	FCA9
	A6U22, PINS 12, 11	P530
505	A5U11, PIN 10	0FUF
	A5U11, PIN 9	7F81
	A5U11, PIN 8	2HP8
	A5U11, PIN 7	H5CF
	A5U11, PIN 3	P022
	A5U11, PIN 4	P8FP
	A5U11, PIN 5	FCA9
	A5U11, PIN 6	P530

SIGNATURE ANALYSIS PROCEDURE NO. 6

SETUP PROCEDURE

a. Set 1611A LINE switch to off position.

b. Remove A6, A7, and A8 assemblies from 1611A.

c. Reinstall A6 on extender board A14.

d. Set signature analyzer controls as follows:

START .....]
STOP .....]=
CLOCK .....]
HOLD ..... Depressed

e. Connect signature analyzer probe to the following circuit points:

START ..... A6U33, Pin 13
STOP ..... A6U33, Pin 13
CLOCK A6TP3
GND ..... A5TP9 (GND)

f. Set 1611A LINE switch to on position.

MEASUREMENT PROCEDURE

a. Ground (+) side of A5C3.

b. Place signature analyzer probe on pin to be measured.

c. Press and release RESET on probe.

d. Release ground on A5C3 and take reading. Verify that reading matches value in following table.

e. Repeat steps a thru d for each measurement.

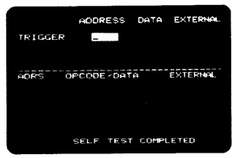
MEASUREMENT NUMBER	TEST POINT	SIGNATURE
601	A6U15, PINS 11, 12	*
	A6U16, PINS 11, 12	*
	A6U17, PINS 11, 12	*
	A6U18, PINS 11, 12	*
	A6U19, PINS 11, 12	*
	A6U20, PINS 11, 12	*
	A6U21, PINS 11, 12	*
	A6U22, PINS 11, 12	*
*Pins 11 and 12 of each IC should have the same reading.		

Figure 7-5 (Sheet 2 of 5). Replacement for figure 8-4. 1611A Troubleshooting

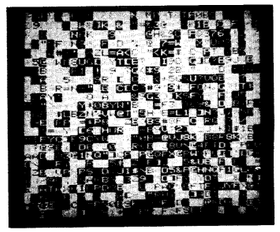
1611A INITIAL SETUP:

1. DISCONNECT EXTERNAL AND MICROPROCESSOR PROBES.
2. SET OCTAL/HEXADECIMAL SWITCH TO HEXADECIMAL POSITION.
3. ENSURE THAT ALL BOARDS ARE PROPERLY INSTALLED.

NOTE: CURSOR IN TRIGGER FIELD SHOULD BE BLINKING



POWER ON DISPLAY



EXAMPLE OF BAD POWER ON DISPLAY WITH CORRECT CHARACTER AND RASTER SIZE (A31NT. ADJUSTMENT FULL CW)

CHECK +5V AND ±12V SUPPLIES

IS POWER ON DISPLAY CORRECT? — YES → A

NO

ARE CHARACTERS CORRECT SIZE? — NO → SEE SERVICE SHEET 3 TROUBLESHOOTING

YES

IS "ERROR IN RAM" MESSAGE DISPLAYED? — YES → H

NO

IS "ERROR IN ROM" MESSAGE DISPLAYED? — YES → PERFORM ROM TEST. SEE SERVICE SHEET S4 IN OPTION SUPPLEMENT.

NO

IS POWER ON DSPL CORRECT EXCEPT FOR INVERSE VIDEO OR BLINKING CURSOR? — YES → SEE SERVICE SHEET 6 TROUBLESHOOTING.

NO

ARE FIELDS IN TRACE SPEC AREA OPENING AND CLOSING? — YES → CHECK KEYSCAN OPERATION. SEE SERVICE SHEET 5.

NO

REMOVE A7 & A8 ASSEMBLIES.

F

F

REPEAT POWER ON DISPLAY CHECK.

IS POWER ON DISPLAY CORRECT? — YES → G

NO

IS TIME INTERVAL AT A5TP3 ≈160 μs? — YES → GROUND A5U3, PIN 6

NO

PERFORM ROM CHECK. SEE SERVICE SHEET S4 IN OPTION SUPPLEMENT.

H ROM GOOD

GROUND A5U3, PIN 6 WITH A5,A6 ASSEMBLIES INSTALLED

IS DISPLAY AS SHOWN IN PHOTOGRAPH — NO → J

YES

SET UP TEST NO. 1 WITH A6 INSTALLED

111 CHECK A6U26 & A6U29 OUTPUTS — BAD → 112 CHECK A6U25 & A6U28 OUTPUTS — GOOD → A6U26 OR U29 BAD

GOOD → Q

BAD → A6U25,U26, U28, OR U29 BAD

NOTE: ALL PROCEDURES IN THESE TROUBLESHOOTING TREES (PAGE 7-13, 7-14, and 7-15) APPLY ONLY TO OPTIONS 068 AND 080. IF OTHER OPTIONS ARE INSTALLED IN YOUR 1611A, REFER TO SECTION VIII FOR SIGNATURE ANALYSIS PROCEDURES.

GROUND A5U3, PIN 6

IS DISPLAY AS SHOWN IN PHOTOGRAPH? — YES → REMOVE A5U11 FROM SOCKET

NO

J

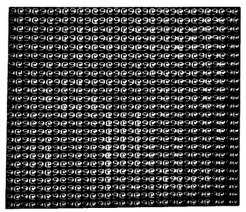
CYCLE POWER SWITCH OFF THEN ON

CHECK FOR ACTIVITY AT INPUTS AND OUTPUTS OF A6U24

ARE LEVELS CHANGING? — NO → A6U24 OR U13 BAD

YES

Q



DISPLAY WITH A5U3, PIN 6 GROUNDED

A

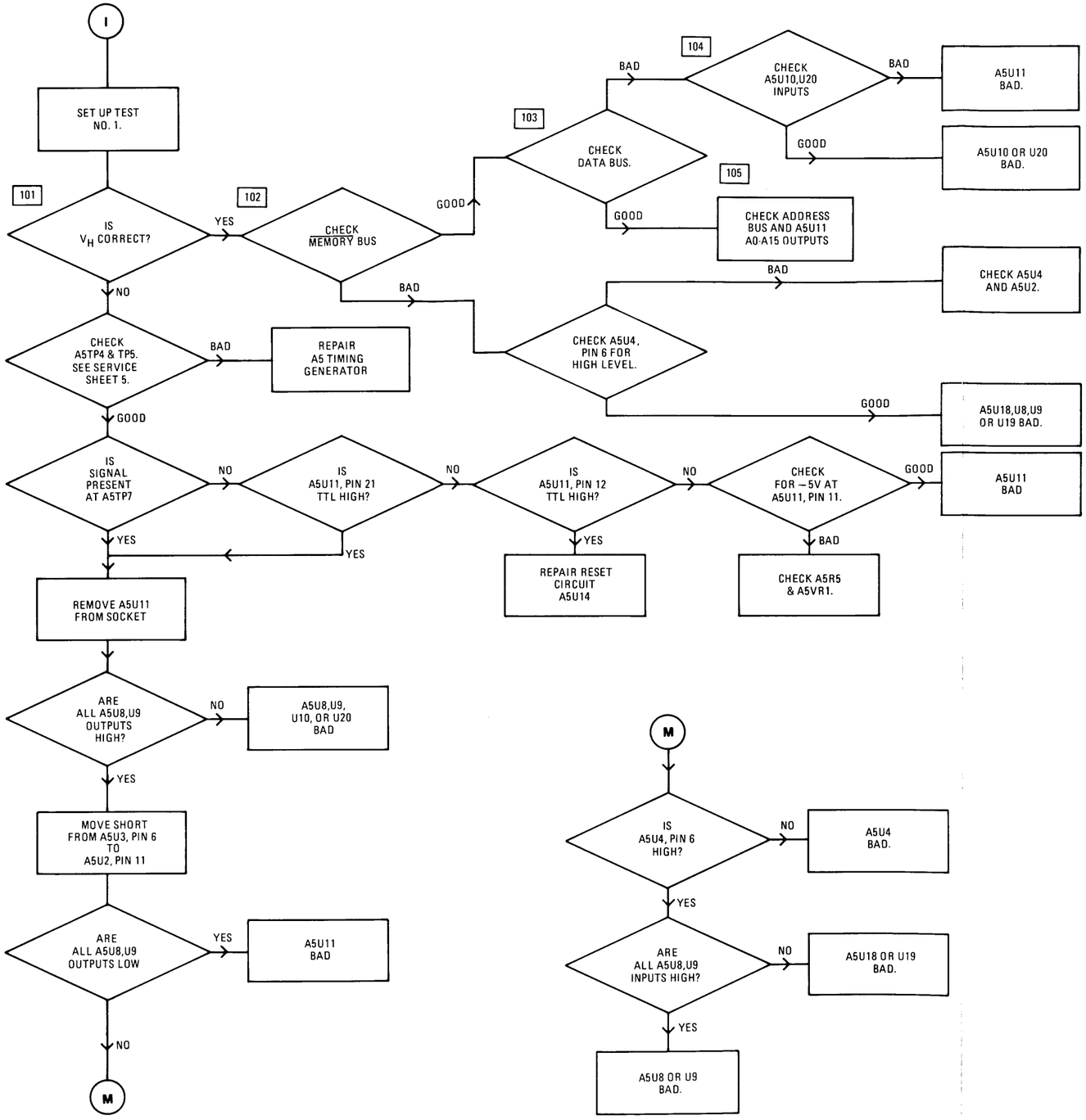
IS THE 1611A RESPONDING TO KEY INPUTS CORRECTLY? — YES → SEE SERVICE SHEET 7 FOR MEASUREMENT PROBLEMS

NO

CHECK KEYSCAN OPERATION ON A5. SEE SERVICE SHEET 5.

1611A-029-01-11-78

Figure 7-5 (Sheet 3 of 5).
Replacement for figure 8-4. 1611A Troubleshooting



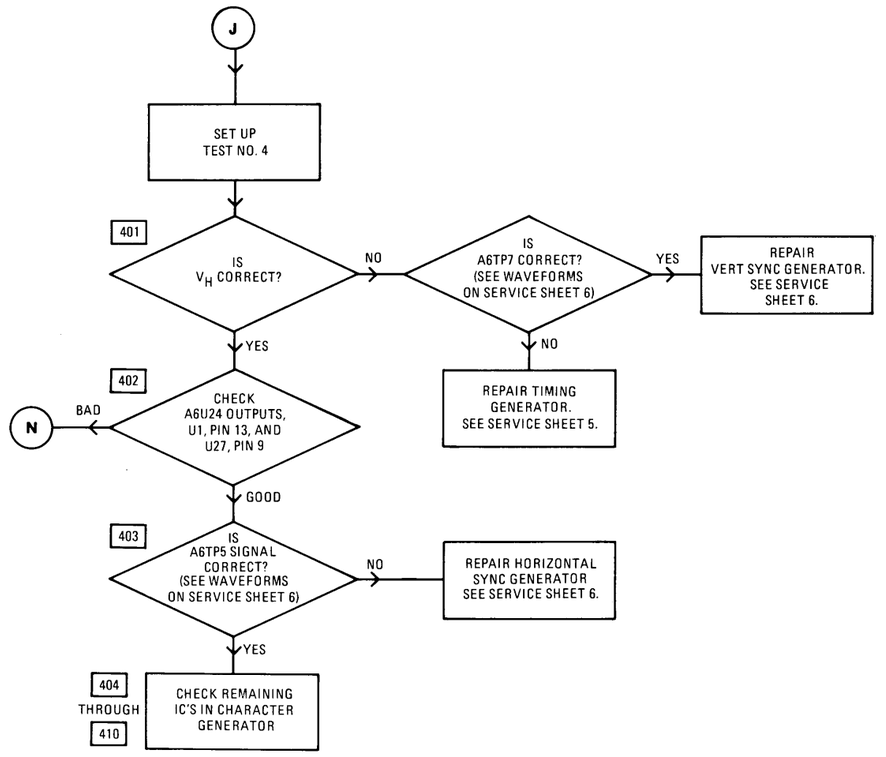


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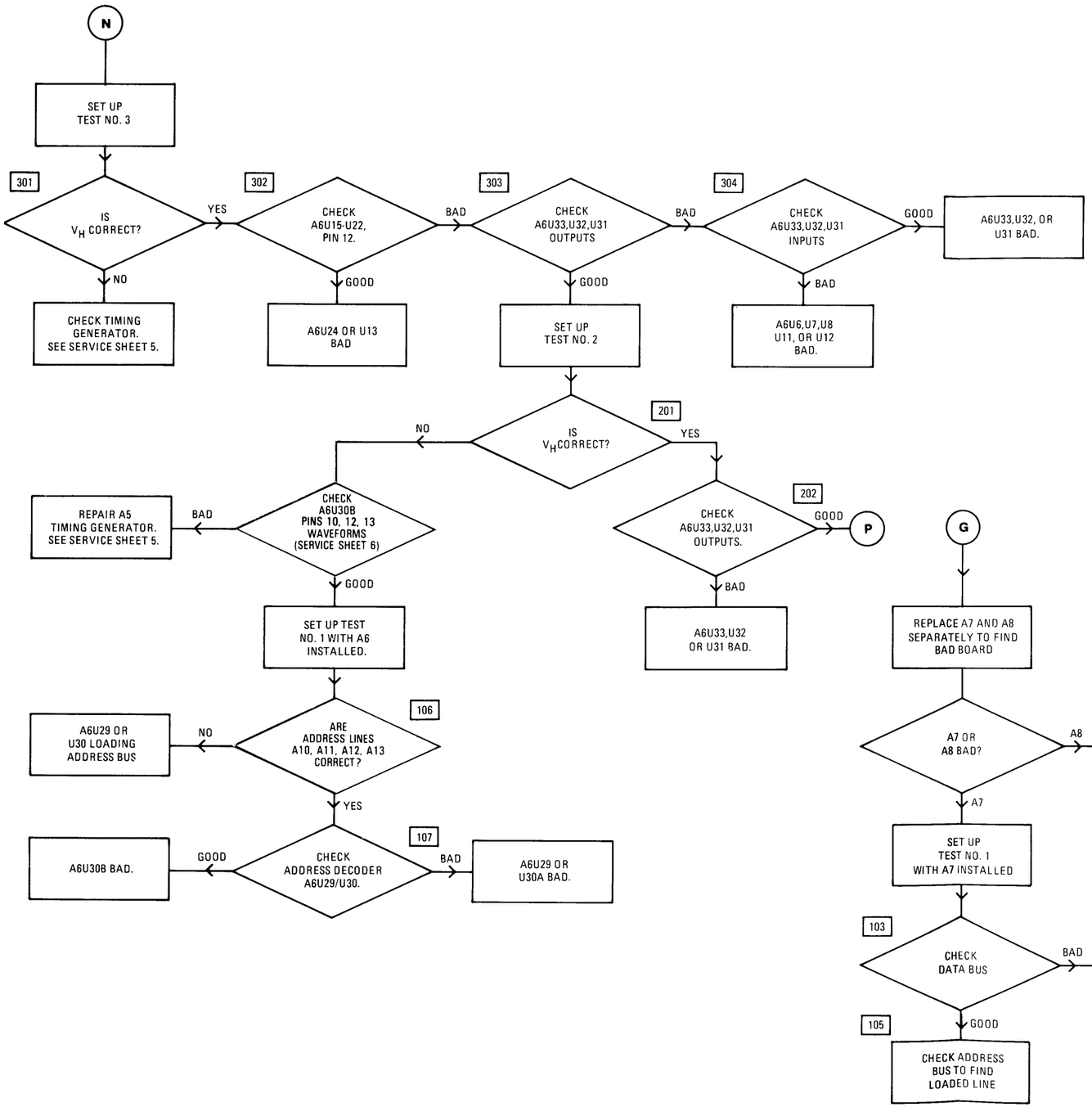
Figure 7-5 (Sheet 4 of 5). Replacement for figure 8-4. 1611A Troubleshooting



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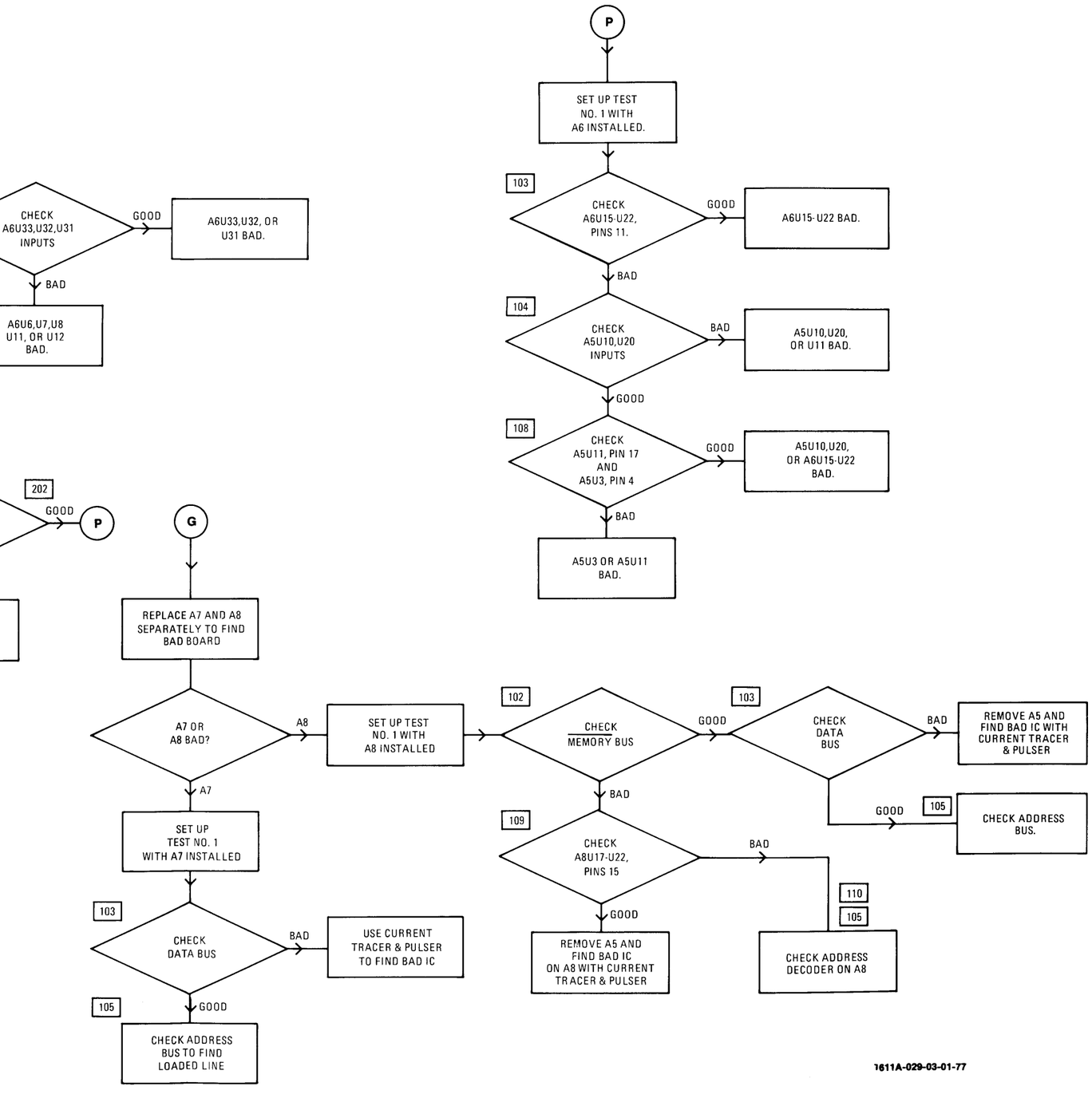

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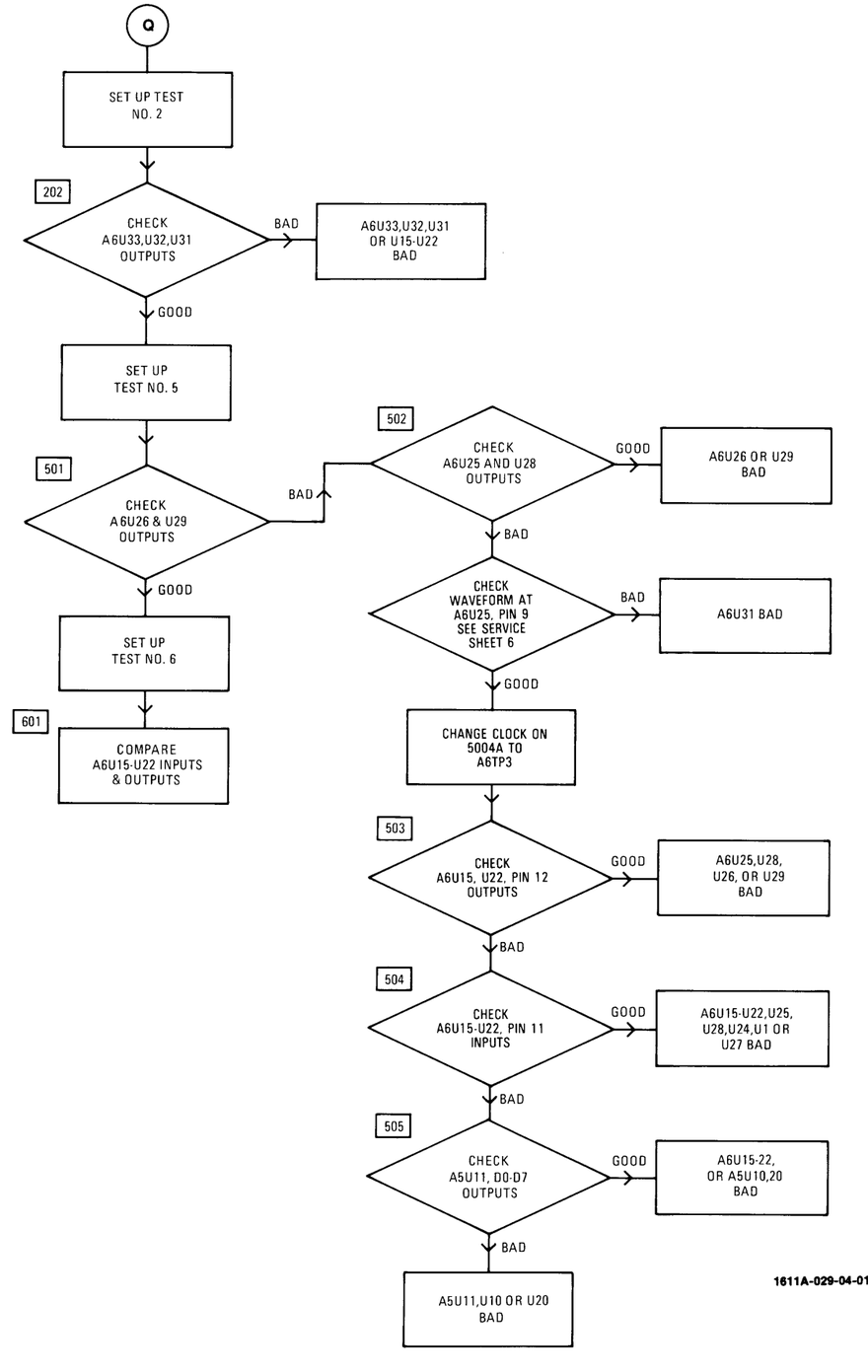

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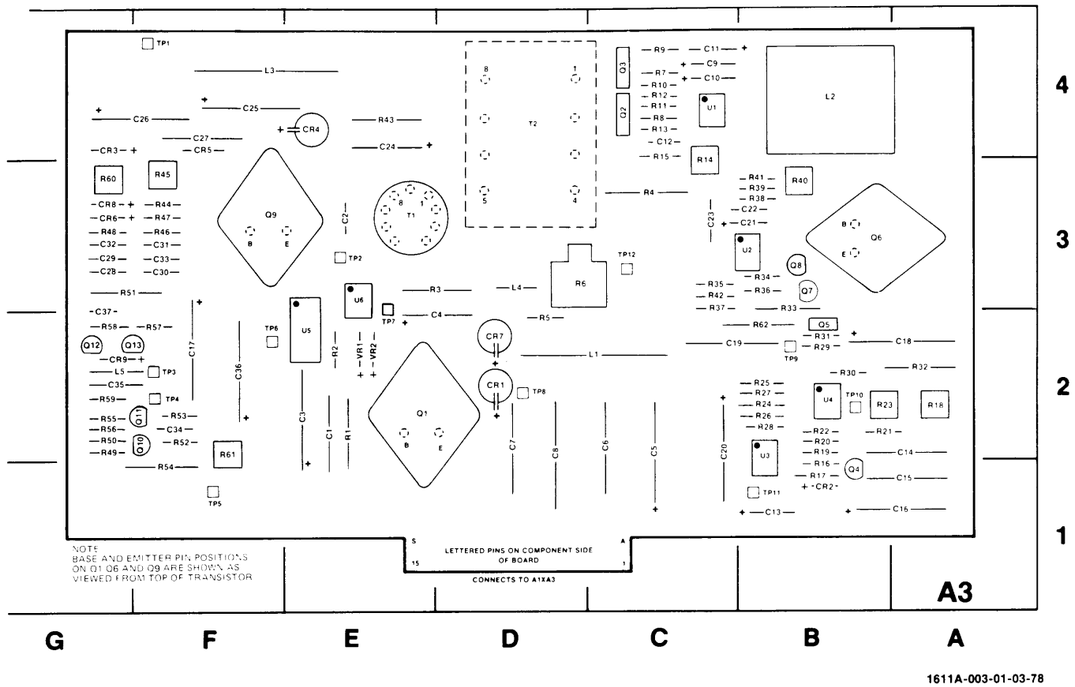
Figure 7-5 (Sheet 5 of 5).
Replacement for figure 8-4. 1611A Troubleshooting



1611A-003-01-03-78

REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC
C1	E-2	C20	C-2	CR2	B-1	Q7	B-3	R12	C-4	R30	B-2	R48	G-3	TP2	E-3
C2	E-3	C21	B-3	CR3	G-4	Q8	B-3	R13	C-4	R31	B-2	R49	G-2	TP3	F-2
C3	E-2	C22	B-3	CR4	E-4	Q9	F-3	R14	C-3	R32	A-2	R50	G-2	TP4	F-2
C4	D-2	C23	C-3	CR5	F-4	Q10	F-2	R15	C-4	R33	B-3	R51	G-3	TP5	F-1
C5	C-2	C24	E-4	CR6	G-3	Q11	F-2	R16	B-1	R34	B-3	R52	F-2	TP6	F-2
C6	C-2	C25	F-4	CR7	D-2	Q12	G-2	R17	B-1	R35	C-3	R53	F-2	TP7	E-2
C7	D-2	C26	F-4	CR8	G-3	Q13	G-2	R18	A-2	R36	B-3	R54	F-1	TP8	D-2
C8	D-2	C27	F-4	CR9	G-2	R1	E-2	R19	B-2	R37	C-3	R55	G-2	TP9	B-2
C9	C-4	C28	G-3	L1	C-2	R2	E-2	R20	B-2	R38	B-3	R56	G-2	TP10	B-2
C10	C-4	C29	G-3	L2	B-4	R3	D-3	R21	B-2	R39	B-3	R57	F-2	TP11	B-1
C11	C-4	C30	F-3	L3	F-4	R4	C-3	R22	B-2	R40	B-3	R58	G-2	TP12	C-3
C12	C-4	C31	F-3	L4	D-3	R5	D-2	R23	B-2	R41	B-3	R59	G-2	U1	C-4
C13	B-1	C32	G-3	L5	G-2	R6	D-3	R24	B-2	R42	C-3	R60	G-3	U2	B-3
C14	A-1	C33	F-3	Q1	E-2	R7	C-4	R25	B-2	R43	E-4	R61	F-1	U3	B-1
C15	A-1	C34	F-2	Q2	C-4	R8	C-4	R26	B-2	R44	F-3	R62	B-2	U4	B-2
C16	A-1	C35	G-2	Q3	C-4	R9	C-4	R27	B-2	R45	F-3	T1	E-3	U5	E-2
C17	F-2	C36	F-2	Q4	B-1	R10	C-4	R28	B-2	R46	F-3	T2	D-4	U6	E-3
C18	A-2	C37	G-2	Q5	B-2	R11	C-4	R29	B-2	R47	F-3	TP1	F-4	VR1	E-2
C19	B-2	CR1	D-2	Q6	B-3									VR2	E-2

ICs ON THIS SCHEMATIC

IC REF DES	HP PART NO.	MFR PART NO.
U1-4	1826-0254	MC1741SCP1
U5	1820-1422	SN74LS122N
U6	1820-1796	DS3611N

Figure 7-6. Replacement for figure 8-9. Service Sheet 3, Display Driver Assembly A3

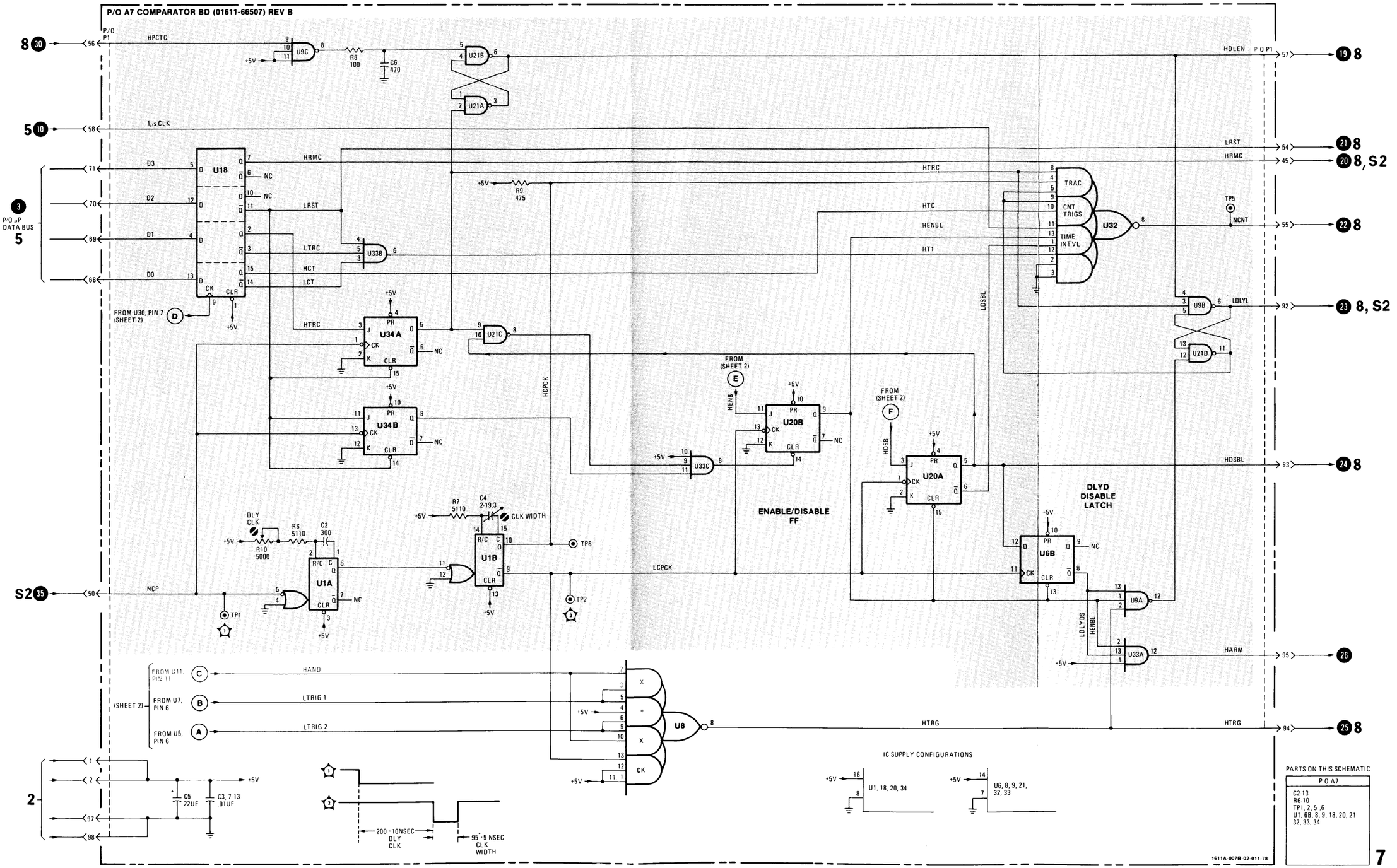
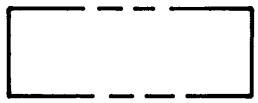
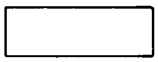


Figure 7-7. Replacement for Figure 8-13, Service Sheet 7, RAM Comparator Assembly A7 (Sheet 4 of 4)



ETCHED CIRCUIT BOARD



FRONT PANEL MARKING

REAR-PANEL MARKING

MANUAL CONTROL

SCREWDRIVER ADJUSTMENT

ELECTRICAL TEST POINT
TP (WITH NUMBER)

NUMBERED WAVEFORM
NUMBER CORRESPONDS TO
ELECTRICAL TEST POINT NO.

LETTERED TEST POINT
NO MEASUREMENT AID
PROVIDED

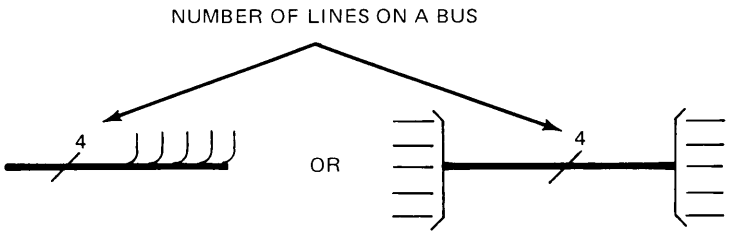
COMMON CONNECTIONS. ALL LIKE-DESIGNATED POINTS ARE CONNECTED.

NUMBER ON BLACK BACKGROUND = OFF-PAGE CONNECTION.
LARGE NUMBER ADJACENT = SERVICE SHEET NUMBER FOR OFF-PAGE CONNECTION.

CIRCLED LETTER = OFF-PAGE CONNECTION BETWEEN PAGES OF SAME SERVICE SHEET.

S PREFIX TO SERVICE SHEET NUMBER INDICATES SERVICE SHEET IS IN MANUAL SUPPLEMENT

INDICATES SINGLE SIGNAL LINE



INDICATES GROUPING OF LINES (BUSES)

μP BUSES AND CONTROL LINES ARE SHOWN IN RED ON SHEMATICS

(925) WIRE COLORS ARE GIVEN BY NUMBERS IN PARENTHESIS USING THE RESISTOR COLOR CODE

[(925) IS WHT-RED-GRN]

0 - BLACK	5 - GREEN
1 - BROWN	6 - BLUE
2 - RED	7 - VIOLET
3 - ORANGE	8 - GRAY
4 - YELLOW	9 - WHITE

* OPTIMUM VALUE SELECTED AT FACTORY, TYPICAL VALUE SHOWN; PART MAY HAVE BEEN OMITTED.

UNLESS OTHERWISE INDICATED:
RESISTANCE IN OHMS
CAPACITANCE IN PICOFARADS
INDUCTANCE IN MICROHENRIES

μP	=	MICROPROCESSOR
P/O	=	PART OF
NC	=	NO CONNECTION
CW	=	CLOCKWISE END OF VARIABLE RESISTOR

STD-20-01-77

Figure 8-1. Schematic Diagram Notes

SECTION VIII

SERVICE

8-1. INTRODUCTION.

8-2. This section contains instructions for troubleshooting and repairing the Hewlett-Packard Model 1611A Logic State Analyzer.

8-3. Principles of operation and troubleshooting information are located opposite the schematics on foldout Service Sheets. The rest of this section has general service information that should help you to quickly service and repair the 1611A.

8-4. PRINCIPLES OF OPERATION.

8-5. Principles of operation appear on pages opposite the block diagram and schematics on the Service Sheets. Figure 8-1 explains symbols that appear on the schematics. Figure 8-5 is an overall block diagram that briefly describes overall instrument operation. It is keyed, by Service Sheet numbers in the blocks, to schematics on the Service Sheets. These Service Sheets provide a stage-by-stage description of circuits on the schematics. The stages are keyed to the descriptions by stage names that appear on the schematics. An overall view of instrument program operation is presented in the macro flowchart shown in figure 8-6.

8-6. LOGIC CONVENTIONS. Positive logic convention is used in describing logic variables and circuits within the 1611A. Positive logic convention defines a logic "1" as the more positive voltage (high) and a logic "0" as the more negative voltage (low). The integrated circuits in the 1611A are almost entirely transistor-transistor-logic (TTL). Major exceptions are the 8080A microprocessor, ROMs, and some RAMs. All these devices have TTL drive capability.

8-7. MNEMONICS. Signals in the 1611A have been assigned mnemonics that describe the active state and function of the signal line. A prefix letter (H, L, P, or N) indicates the active state of the signal, and the remaining letters indicate its function. An H prefix indicates the function is active in the high state; an L prefix indicates the function is active in the low state. For edge-controlled devices, the prefix P indicates the function is active on the positive-going transition; prefix N indicates the function is active on the negative-going transition. Mnemonic functional definitions and points of origin are listed alphabetically in table 8-1.

8-8. TROUBLESHOOTING.

WARNING

Read the Safety Summary at the front of this manual before troubleshooting the instrument.

8-9. The most important prerequisites for successful troubleshooting are an understanding of instrument functional operation and the correct use of front panel controls. Suspected malfunctions may be caused by improper control settings. Before performing the test and/or troubleshooting procedures, refer to the Operating and Service Manual Supplement (provided with each μP personality module. For an explanation of controls, connectors, and general operating considerations, and to the service sheets in this section for an explanation of circuit functional operation.

8-10. If trouble is suspected, visually inspect the instrument. Look for loose or burned components that might suggest a source of trouble. Check to see that all circuit board connections are making good contact and are not shorting to an adjacent circuit. If no obvious trouble is found, check the instrument power-supply voltages, and external power sources.

8-11. FAULT ISOLATION. Figure 8-4 is a 1611A troubleshooting tree which can be used to isolate problems that cause an incorrect turn-on display. Refer to Service Sheets 7 and 8 for measurement problems such as improper triggering or incorrect measurement results. Some paths in the troubleshooting tree reference ROM test procedures. These procedures are provided in the personality module supplement for this manual.

8-12. Many measurements in the troubleshooting tree are made with an HP Signature Analyzer. Each signature is measured under specific conditions described in the test procedures accompanying the troubleshooting tree. Each signature measurement in the tree is assigned a three-digit number. This refers to a measurement step in the test procedures. If the measured signature matches the signature given in the test procedure, the circuit is functioning correctly at the node being measured. An incorrect signature indicates a malfunction somewhere in the circuit leading up to the measured node. An oscilloscope can be used in place of the signature analyzer, but problems other than nodes stuck at one level will be difficult to find.

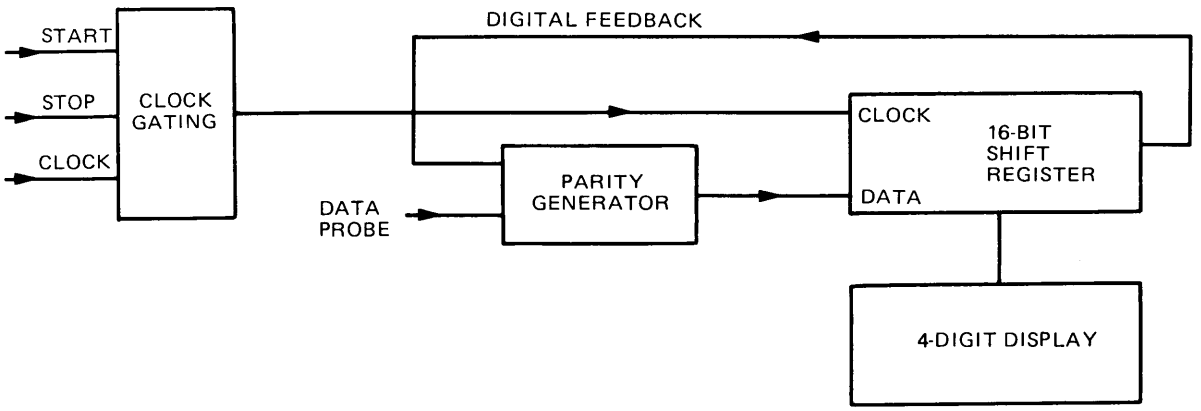


Figure 8-2. 5004A Block Diagram

8-13. Troubleshooting with the HP Signature Analyzer (SA). The SA is a service tool designed to analyze complex digital signals. The instrument provides a unique four-digit alphanumeric signature for each monitored data pattern. Figure 8-2 is a simple block diagram of the SA. The SA collects data between the occurrence of START and STOP signals. The data probe input is read on the selected clock edge. Data is routed to a 16-bit shift register through a parity generator. Parallel outputs of the shift register drive the four-digit display. START, STOP, and CLOCK signals are selected so that normally they are not dependent on the circuitry being analyzed.

8-14. Signatures of some nodes are designated with special symbols. These nodes are at one state (high or low) everytime the clock edge occurs. These symbols are:

V_H-Corresponds to signature displayed when the SA data probe is at a node that is always high. This signature should be checked at the +5 V supply on the board before test measurements are made. A correct signature verifies that clock and time intervals are correct. The probe-tip indicator is on continuously at V_H.

V_{HP}-Indicates node is high whenever clock edge occurs. The signature is the same as V_H, but the probe-tip indicator flashes on and off, rather than staying on continuously.

V_L-Indicates node being measured is always low; signature for V_L is 0000. The probe-tip indicator always remains off when probing a V_L node.

V_{LP}-Indicates node is low whenever a clock edge occurs. The V_{LP} signature is 0000 as for V_L, but the probe-tip indicator flashes.

A reading other than V_H, V_{HP}, V_L, or V_{LP} indicates that the state of the node varies on the clock edge during the measurement interval.

8-15. TROUBLESHOOTING MICROPROCESSOR PROBLEMS. The troubleshooting tree can be used to isolate some microprocessor (A5U11) problems. However, it is sometimes difficult to isolate μP failures due to complexity of the device. It is possible for the 1611A to pass all tests in the troubleshooting tree and still have a faulty μP. Therefore, it is recommended that a good μP be substituted for the one in the instrument before attempting to isolate a problem that could be caused by a faulty μP. A5U11 is mounted in a 40-pin socket for easy removal.

8-16. TROUBLESHOOTING WITH LOGIC TEST EQUIPMENT. Dedicated logic test equipment is required to efficiently and effectively troubleshoot most faults in the 1611A. The following equipment is recommended:

HP 547A Current Tracer—used for precise localization of low-impedance faults. The hand-held probe senses the magnetic field generated by a pulsing current internal to the circuit or by current pulses supplied by an external stimulus such as the HP 10526A Logic Pulser.

HP 1600A Logic State Analyzer—used to monitor counters, address decoders, and data selectors within the 1611A.

HP 10525T Logic Probe—used to check operation of gates and flip-flops.

HP 10526T Logic Pulser—used with the HP 547A to provide a high-current pulse.

8-17. RECOMMENDED TEST EQUIPMENT.

8-18. Equipment required for troubleshooting is listed in the Recommended Test Equipment Table in Section I. Any equipment that satisfies the critical specifications given in the table may be substituted for the recommended model(s).

8-19. SERVICE AIDS.

8-20. TEST POINTS. Test points shown on schematics correspond to pins protruding from circuit boards and do not necessarily correspond to waveform measurement points.

8-21. EXTENDER BOARD. An extender board (HP Part No. 01611-66515) is supplied with the 1611A to provide access to circuits on plug-in boards while the instrument is operating.

8-22. PART LOCATION AIDS. The locations of assemblies, chassis-mounted parts, and hardware are shown in the Illustrated Parts Breakdown in Section VI. The locations of individual components mounted on printed circuit boards or other assemblies are shown on the page opposite the appropriate schematic diagram page. The part reference designator is the assembly designator plus the part designator (for example, A6R9 is R9 on the A6 assembly). For specific component description and ordering information, refer to the parts list in Section VI.

8-23. REPAIR.

8-24. CRT REPLACEMENT PROCEDURE. (See figure 6-1.)

a. Set LINE power switch to off position and disconnect power cord.

b. Remove top, bottom, and side covers.

c. Disconnect diode CR1 from PA (post-accelerator) cable W2.

d. Remove 3 screws that hold A3 board to corner strut MP3 and remove A3 board from instrument.

e. Remove PA cable clamp H39 from CRT shield MP13.

f. Loosen, but do not remove, 4 screws securing CRT shield MP13.

g. Remove MP13 from instrument.

h. Disconnect yoke cable (P/O L1) and CRT cable W4 from connectors P3 and P4 on main board A1.

i. Remove 2 lower screws H12 that hold CRT to Keyboard Support MP27 through bottom of instrument.

j. Remove 2 upper screws H12 that hold CRT to MP27 through top of instrument.

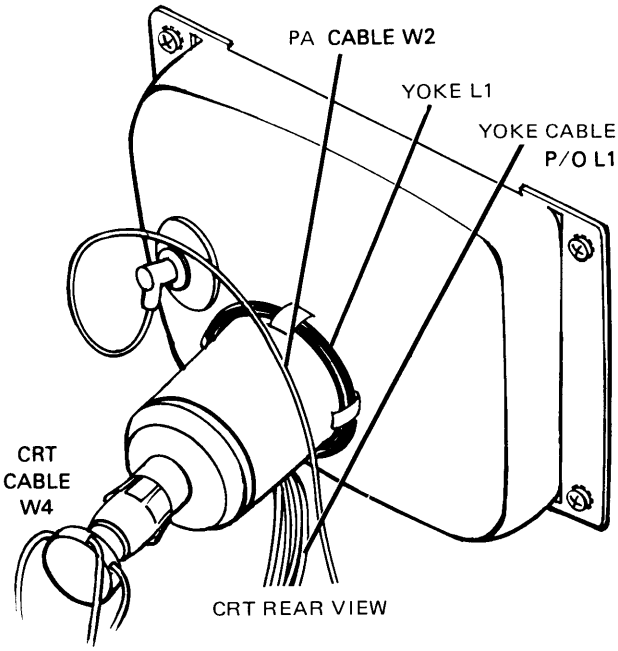


Figure 8-3. CRT Yoke Installation

k. Slide CRT back from MP27 and remove contrast filter.

l. Remove CRT from instrument with CRT cable W4 and yoke assembly L1 attached.

m. Remove CRT cable and L1 from CRT.

n. Install L1 on new CRT with yoke cable on bottom of CRT (see figure 8-3).

o. Install CRT cable W4 on new CRT.

p. Install CRT in instrument by reversing steps a through l.

q. Perform Trace Alignment Procedure (Section V).

Table 8-1. 1611A Mnemonics

MNEMONIC	DESCRIPTION	ORIGIN
A0-A13	Microprocessor Address Bus. Address lines from 8080A μP on A5 board. Bus is shown in red on schematics.	Schematic 5, A5P1, PINS 78-91
A0*-A9*	Display RAM address lines. Lines originate from μP ADDRESS BUS or display format generator, depending on the state of HμPCY.	Schematic 6, A6U31-A6U33
D0-D7	Microprocessor Data Bus. Data that 8080A μP A5U11 is outputting. Bus is shown in red on schematics.	Schematic 5, A5P1, PINS 68-75
EXT 0-EXT 7	External Inputs 0-7. Inputs from External Probe.	Schematic S4, A10P1, PINS 3-10
FLAG 0-FLAG 3	Flags 0-3. Status bits indicating the type of machine cycle being executed by the μP under test. A 4-bit flag byte is stored for each of the 64 words stored in High-Speed Memory.	Schematic S2, A9P1, PINS 19-22

Table 8-1. 1611A Mnemonics (Cont'd)

MNEMONIC	DESCRIPTION	ORIGIN
HAND	High, AND. Determines whether the two outputs LTRG1 and LTRG2 from RAM Comparator A7 will be logic ANDed or logic ORed.	Schematic 7, A7U11, PIN 11
HARM	High, Armed. Signal is true when μP under test is between the Enable and Disable trace specifications.	Schematic 7, A7U33A, PIN 12
HBLINK	High, Blink. Signal is true when character being read from RAM is to be displayed in a blinking mode.	Schematic 6, A6U22, PIN 12
HCT	High, Count Triggers. Signal is true when 1611A is executing a a COUNT TRIGS measurement.	Schematic 7, A7U18, PIN 15
HCTOF	High, Counter Overflow. Signal is true when delay counter overflows during Trace, Time Interval, or Count Trigs measurement.	Schematc 8, A8U15A, PIN 7
HDLEN	High, Delay Enable. Signal Enables Delay Counter on A8. True when Pass Counter = Terminal Count.	Schematic 7, A7U21B, PIN 6
HDSB	High, Disable. Signal assumes true state when Disable trace specification is met.	Schematic 7, A7P1, PIN 53
HDSBL	High, Disable Latched. Signal is latched in true state when Disable trace specification is met.	Schematic 7, A7U20A, PIN 5
HDSPC	High, Display Cycle. Signal is true when Display Format Generator is accessing RAM on A6. Rising edge of HDSPC is used to latch data onto $\overline{\text{MEMORY}}$ bus.	Schematic 6, A6U31, PIN 7
HENB	High, Enable. Signal assumes true state when Enable trace specification is met.	Schematic 7, A7P1, PIN 51
HENBL	High, Enable Latched. Signal is latched in true state when Enable trace specification is met.	Schematic 7, A7U20B, PIN 9
HHBLK	High, Horizontal Blank. Signal is true when display is blanked during horizontal retrace.	Schematic 6, A6U4, PIN 15
HHSY	High, Horizontal Sync. Positive edge of signal starts horizontal retrace.	Schematic 6, A6U34C, PIN 8
HINVS	High, Inverse. Signal is true when character being generated is displayed in inverse video (black character on white background).	Schematic 6, A6U4, PIN 7
HMCOF	High, Memory counter Overflow. Signal is true when memory state counter reaches count of 64 or greater.	Schematic 8, A8U3D, PIN 13
HNORM	High, Normal. Signal is true when character being generated is displayed normally (white character on dark background). Signal is false when character is displayed in inverse video.	Schematic 6, A6U4, PIN 5
HPCTC	High, Pass Counter Terminal Count. Signal is true when pass counter MSD (A8U11, pin 15) reaches terminal count.	Schematic 8, A8U9, PIN 15
HRADR	High, RAM Address. Signal is true when μP ADDRESS Bus (A0-A13) is equal to RAM address (320008-337778).	Schematic 6, A6U29D, PIN 8

Table 8-1. 1611A Mnemonics (Cont'd)

MNEMONIC	DESCRIPTION	ORIGIN
HRMC	High, Reset Memory Counter. Signal resets memory state counter and clears memory counter overflow flip-flop A8U3.	Schematic 7, A7U18, PIN 7
HTI	High, Time Interval. Signal is true when 1611A is executing Time Interval measurement.	Schematic 7, A7U33B, PIN 6
HTRC	High, Trace. Signal is true when 1611A is executing Trace or Trace Trigs measurement.	Schematic 7, A7U18, PIN 2
HTRG	High, Trigger. Signal is true when trigger specification is met and LCPCK is low.	Schematic 7, A7U8, PIN 8
HTSTOR	High, Trigger Store. Signal is true when 1611A is executing Trace Trigs measurement.	Schematic 8, A8U15B, PIN 10
HVBLK	High, Vertical Blank. Signal is true when display is blanked for vertical retrace.	Schematic 6, A6U4, PIN 10
HWRT	High, Write. Signal is true when microprocessor A5U11 is outputting data on the data bus.	Schematic 5, A5U3A, PIN 2
HμPCY	High, Microprocessor Cycle. Signal is high when 8080 μP A5U11 is addressing RAM on A6. Signal is low when character generator is addressing RAM.	Schematic 5, A5U14A, PIN 3
INP A0-A15	Input Address Bus. Address Lines from μP under test.	Schematic S2, A9P1, PINS 23-38
INP D0-D7	Input Data Bus. Data lines from μP under test.	Schematic S2, A9P1, PINS 11-18
KS0-KS4, KS7	Key Sense Lines. Lines are tied to keyboard matrix columns. Depressed key in a column will generate a 1 to 2 volt pulse output on appropriate sense line.	Schematic 4, A4W1J1
LCPCK	Low, Compare Clock. When true, signal enables outputs of RAM Comparator (LTRG1 and LTRG2) to be gated through A7U8.	Schematic 7, A7U1B, PIN 9
LCTOF	Low, Counter Overflow. When True, signal indicates Delay Counter has reached terminal count.	Schematic 8, A8U15B, PIN 7
LDLYDS	Low, Delayed Disable. Delayed HDSBL. Signal allows trigger to be recognized if HDSB and HTRG are true on same cycle.	Schematic 7, A7U6B, PIN 8
LDLYL	Low, Delaying Latched. Signal is true after pass counter reaches terminal count when executing Trace measurement.	Schematic 7, A7U9B, PIN 6
LDSBL	Low, Disable Latched. Signal is true when Disable trace specification is met.	Schematic 7, A7U20A, PIN 5
LDSTOR	Low, Data Store. Signal enables write mode of high-speed RAM (A8U25-28) and clocks memory counter during measurements.	Schematic 8, A8U8B, PIN 8
LLSRE	Low, Load Shift Register Enable. Signal enables character shift register A6U14 to parallel load when 200 ns CLK is low.	Schematic 5, A5U22, PIN 15
LMCOF	Low, Memory Counter Overflow. Signal is true when memory counter counts pass 63.	Schematic 8, A8U3C, PIN 10

Table 8-1. 1611A Mnemonics (Cont'd)

MNEMONIC	DESCRIPTION	ORIGIN
LREAD	Low, Read. Signal is true when μP A5U11 is reading from MEMORY Bus.	Schematic 5, A5U3B, PIN 4
LRST	Low, Reset. Signal Clears Enable and Disable flip-flops on A7 board, inhibits pass and delay counters on A8 board, and inhibits Trace Point Output.	Schematic 7, A7U18, PIN 11
LTRG1	Low, Trigger 1. Signal is true when = and < trigger conditions are met.	Schematic 7, A7U7, PIN 6
LTRG2	Low, Trigger 2. Signal is true when > trigger conditions are met.	Schematic 7, A7U5, PIN 6
LTSTOR	Low, Trigger Store. Signal is true when 1611A is executing Trace Trigs measurement.	Schematic 8, A8U15B, PIN 9
$\overline{M0}$-$\overline{M7}$	MEMORY Bus. Data that is read by μP A5U11. BUS lines are shown in red on schematics.	Schematics 6, 8, and 10
MSC0-5	Memory State Count. Signal indicates address of high-speed RAM (A8U25-28) that is being written into or read from.	Schematic 8, A8U1A/B
NCNT	Negative, Count. Negative edge of signal clocks pass and delay counters when enabled.	Schematic 7, A7U32, PIN 8
NCP	Negative Compare. Negative edge of signal indicates that personality board A9 has valid data ready for comparator.	Schematic S2, A9P1, PIN 50
NMCCK	Negative, Memory Counter Clock. Negative edge of signal clocks memory counter.	Schematic 8, A8U2C, PIN 8
NSTOR	Negative, Store. Negative edge of signal enables LDSTOR when executing Trace measurement.	Schematic S2, A9P1, PIN 49
PEXCK	Positive, External Clock. Positive edge of signal latches data from external probe.	Schematic S2, A9P1, PIN 47
PRWCK	Positive, RAM Write Clock, Signal enables RAM on A6 to be written into.	Schematic 5, A5U3E, PIN 10
PHLTEN	Positive, Halt Enable. Positive edge of signal enables personality board A9 to halt μP under test in Trace Then Wait or Trace Then Halt Test modes.	Schematic 8, A8U8A, PIN 6
SCAN A-D	Four signals scan keyboard.	Schematic 5, A5U7/A5U17
SW0-7	Switch lines 0-7. Signals indicate personality panel switch positions. SW0=HEXADECIMAL/OCTAL switch, SW7=TEST MODE. Some lines are not used by all options.	Schematic S3, A11W1
VIDEO	Z-axis blanking signal from character generator.	Schematic 6, A6U2A, PIN 2
1μS CK	Signal provides timing clock for Time Interval measurements and is master clock for porbe test generator.	Schematic 5, A5U23, PIN 11
2 Hz CLK	Signal provides blanking signal for A6 assembly. It is also used by probe test generator.	Schematic 6, A6U5, PIN 13

NOTE

The following procedures do not apply to Options 068 and 080. If either of these Personality Panel Modules are installed in your 1611A, refer to Section VII for Signature Analysis Procedures.

SIGNATURE ANALYSIS PROCEDURE NO. 1.

See Service Sheet S4 in the manual supplement supplied with your option for ROM Test signatures and flow chart procedure.

SIGNATURE ANALYSIS PROCEDURE NO. 2.

a. Set 1611A LINE switch to off position.

b. Remove A7 and A8 boards from 1611A.

c. Install A6 board on extender board A14.

d. Jumper A6U31 pin 7 to pin 8.

e. Connect signature analyzer probes to the following circuit points:

START ..... A6U33, Pin 13
STOP ..... A6U33, Pin 13
CLOCK A6TP3
GND ..... A6TP (GND)

f. Set signature analyzer controls as follows:

START .....
STOP .....
CLOCK .....

g. Set 1611A LINE switch to on position.

h. Verify that signature measurements called out in troubleshooting tree match following table.

Figure 8-4.
1611A Troubleshooting (Sheet 1 of 8)

MEASUREMENT NUMBER	TEST POINT	SIGNATURE
201	VH	2A42 or 5216
202 press ABSOLUTE/ MNEMONIC key while reading signatures.	A6U15, PIN 12 A6U16, PIN 12 A6U17, PIN 12 A6U18, PIN 12 A6U19, PIN 12 A6U20, PIN 12 A6U21, PIN 12 A6U22, PIN 12	44AC or CC27 007A or 7U7H 2P47 or U140 05P3 or 9405 6FP5 or AF05 2P78 or H6CC 8235 or C811 A8CU or F81A
203	A6U31, PIN 9 A6U31, PIN 12 A6U32, PIN 4 A6U32, PIN 7 A6U32, PIN 9 A6U32, PIN 12 A6U33, PIN 4 A6U33, PIN 7 A6U33, PIN 9 A6U33, PIN 12	C51U or A8C3 4405 or 6405 U21A or 636C C0P6 or U40F A70H or 4P5F H597 or 461F 2HP1 or H24C 1892 or 2U1P PP62 or C6A7 7A70 or 72A0
204	A6U31, PIN 13 A6U31, PIN 10 A6U32, PIN 13 A6U32, PIN 10 A6U32, PIN 6 A6U32, PIN 3 A6U33, PIN 13 A6U33, PIN 10 A6U33, PIN 6 A6U33, PIN 3	4405 or 6405 C51U or A8C3 H597 or 461F A70H or 4P5F C0P6 or U40F U21A or 636C 7A70 or 72A0 PP62 or C6A7 1892 or 2U1P 2HP1 or H24C
205	A5U11, PIN 25 A5U11, PIN 26 A5U11, PIN 27 A5U11, PIN 29 A5U11, PIN 30 A5U11, PIN 31 A5U11, PIN 32 A5U11, PIN 33 A5U11, PIN 34 A5U11, PIN 35 A5U11, PIN 1 A5U11, PIN 40 A5U11, PIN 37 A5U11, PIN 38	C51U or A8C3 4405 or 6405 U21A or 636C C0P6 or U40F A70H or 4P5F H597 or 461F 2HP1 or H24C 1892 or 2U1P PP62 or C6A7 7A70 or 72A0 VHP or VHP VLP or VLP VHP or VHP VHP or VHP
206 press ABSOLUTE/ MNEMONIC key while reading signatures	A6U15, PIN 11 A6U16, PIN 11 A6U17, PIN 11 A6U18, PIN 11 A6U19, PIN 11 A6U20, PIN 11 A6U21, PIN 11 A6U22, PIN 11	44AC or CC27 007A or 7U7H 2P47 or U140 05P3 or 9405 6FP5 or AF05 2P78 or H6CC 8235 or C811 A8CU or F81A

MEASUREMENT NUMBER	TEST POINT	SIGNATURE
207 press ABSOLUTE/ MNEMONIC key while reading signatures.	A5U11, PIN 10 A5U11, PIN 9 A5U11, PIN 8 A5U11, PIN 7 A5U11, PIN 3 A5U11, PIN 4 A5U11, PIN 5 A5U11, PIN 6	44AC or CC27 007A or 7U7H 2P47 or U140 05P3 or 9405 6FP5 or AF05 2P78 or H6CC 8235 or C811 A8CU or F81A

SIGNATURE ANALYSIS PROCEDURE NO. 3.

a. Set 1611A LINE switch to off position.

b. Remove A6, A7, A8, A9, and A10 assemblies from 1611A.

c. Reinstall A6 on extender board A14.

d. Ground A5U3, pin 6.

e. Connect signature analyzer probe to the following circuit points:

START A6TP4
STOP A6TP4
CLOCK A6TP7
GND ..... A6TP (GND)

f. Set signature analyzer controls as follows:

START ..... ┐
STOP ..... ├ =
CLOCK ..... ┐
HOLD ..... Released

g. Set 1611A LINE switch to on position.

h. Verify that signature measurements called out in troubleshooting tree match following table.

MEASUREMENT NUMBER	TEST POINT	SIGNATURE
301	VH	31PA
302	A6U24, PIN 2 A6U24, PIN 5 A6U24, PIN 7 A6U24, PIN 10 A6U24, PIN 12 A6U24, PIN 15 A6U1, PIN 13 A6U27, PIN 9	8791 VL or VLP VL orVLP 8791 8791 8791 VL or VLP VL or VLP
303	A6TP5	4UF5

MEASUREMENT NUMBER	TEST POINT	SIGNATURE
304	A6U10, PIN 4 A6U10, PIN 5	81UF 9PP0
305	A6U27, PIN 13 A6U27, PIN 10	2F02 31PA and 0000 Alternating
306	A6U1, PIN 3 A6U1, PIN 4 A6U1, PIN 6 A6U1, PIN 14	5H5A HF38 7F9C 8AH9
307	A6U1, PIN 2 A6U1, PIN 5 A6U1, PIN 7 A6U1, PIN 10 A6U1, PIN 12 A6U1, PIN 15	7A8U 3P84 5CP4 408A VL 8F56
308	A6U14, PIN 5 A6U14, PIN 4 A6U14, PIN 3 A6U14, PIN 14 A6U14, PIN 13	F33H 047F 29C3 288A 186A
309	A6U14, PIN 2 A6U14, PIN 9 A6U14, PIN 7	VHP PU0H HPP7
310	A6U3, PIN 6 A6U2, PIN 2	HA0H PCP7
VH=31PA, VHP=31PA, VL=0000, VLP=0000		

SIGNATURE ANALYSIS PROCEDURE NO. 4

a. Set 1611A LINE switch to off position.

b. Remove A6, A7, A8, A9, and A10 assemblies from 1611A.

c. Reinstall A6 on extender board A14.

d. Ground A5U3, pin 6.

e. Connect signature analyzer probe to the following circuit points:

START A6TP4
STOP A6TP4
CLOCK A6TP2
GND ..... A6TP (GND)

f. Set signature analyzer controls as follows:

START ..... ┐
STOP ..... ├ =

CLOCK ..... ┐
HOLD ..... Released

g. Set 1611A LINE switch to on position.

h. Verify that signature measurements called out in troubleshooting tree match following table.

MEASUREMENT NUMBER	TEST POINT	SIGNATURE
401	VH	7092
402	A6U15, PIN 12 A6U16, PIN 12 A6U17, PIN 12 A6U18, PIN 12 A6U19, PIN 12 A6U20, PIN 12 A6U21, PIN 12 A6U22, PIN 12	5U1F VL or VLP VL or VLP 5U1F 5U1F 5U1F VL or VLP VL or VLP
403	A6U33, PIN 12 A6U33, PIN 9 A6U33, PIN 7 A6U33, PIN 4 A6U32, PIN 12 A6U32, PIN 9 A6U32, PIN 7 A6U32, PIN 4 A6U31, PIN 12 A6U31, PIN 9 A6U31, PIN 7	H93A 5UA3 U869 57PC PPPP U6P0 05F9 065F 1U2U 2U8P VHP
404	A6U33, PIN 14 A6U33, PIN 11 A6U33, PIN 5 A6U33, PIN 2 A6U32, PIN 14 A6U32, PIN 11 A6U32, PIN 5 A6U32, PIN 2 A6U31, PIN 14 A6U31, PIN 11	H93A 5UA3 U869 57PC PPPP U6P0 05F9 065F 1U2U 2U8P
VH=7092, VHP=7092, VL=0000, VLP=0000		

SIGNATURE ANALYSIS PROCEDURE NO. 5

a. Set 1611A LINE switch to off position.

b. Remove A6, A7, A8, and A10 assemblies from 1611A.

c. Reinstall A6 on extender board A14.

d. Ground A5U3, pin 6.

Figure 8-4. 1611A Troubleshooting (Sheet 2 of 8)

e. Connect signature analyzer probe to the following circuit points:

START ..... A5U11, Pin 36
STOP ..... A5U11, Pin 36
CLOCK A6TP3
GND ..... A5TP (GND)

f. Set signature analyzer controls as follows:

START ..... ┐
STOP ..... ┤
CLOCK ..... ┘
HOLD ..... Released

g. Set 1611A LINE switch to on position.

h. Verify that signature measurements called out in troubleshooting tree match following table.

MEASUREMENT NUMBER	TEST POINT	SIGNATURE
501	VH	7A70
502	A6U33, PIN 12	6H44
	A6U33, PIN 9	PF45
	A6U33, PIN 7	7H02
	A6U33, PIN 4	355A
	A6U32, PIN 12	3P32
	A6U32, PIN 9	9A40
	A6U32, PIN 7	AAHA
	A6U32, PIN 4	A077
	A6U31, PIN 12	F86A
	A6U31, PIN 9	AF5U
	A6U31, PIN 7	VLP
VH=7A70, VLP=0000		

SIGNATURE ANALYSIS PROCEDURE NO. 6

a. Set 1611A LINE switch to off position.

b. Remove A6, A7, A8, and A10 assemblies from 1611A.

NOTE

The boards installed in the 1611A for the following measurements depend upon the Troubleshooting Tree. Follow the procedure given in the Troubleshooting Tree.

c. Ground A5U3, pin 6.

d. Connect signature analyzer probe to the following circuit points:

START ..... A5U11, Pin 36
STOP ..... A5U11, Pin 36
CLOCK ..... A5U11, Pin 18
GND ..... A5TP (GND)

e. Set signature analyzer controls as follows:

START ..... ┐
STOP ..... ┤
CLOCK ..... ┘
HOLD ..... Released

f. Set 1611A LINE switch to on position.

g. Verify that signature measurements called out in troubleshooting tree match following table.

MEASUREMENT NUMBER	TEST POINT	SIGNATURE
601	VH	755U
602	MEMORY BUS	
	A5U9, PIN 13	VH
	A5U9, PIN 9	VH
	A5U9, PIN 1	VH
	A5U9, PIN 5	VH
	A5U8, PIN 13	VH
	A5U8, PIN 9	VH
	A5U8, PIN 1	VH
	A5U8, PIN 5	VH
603	DATA BUS	
	A5U20, PIN 8	H335
	A5U20, PIN 11	VLP
	A5U20, PIN 6	VLP
	A5U20, PIN 3	H335
	A5U10, PIN 8	H335
	A5U10, PIN 11	H335
	A5U10, PIN 6	VLP
	A5U10, PIN 3	VLP
604	μP OUTPUTS	
	A5U11, PIN 10	H335
	A5U11, PIN 9	VLP
	A5U11, PIN 8	VLP
	A5U11, PIN 7	H335
	A5U11, PIN 3	H335
	A5U11, PIN 4	H335
	A5U11, PIN 5	VLP
	A5U11, PIN 6	VLP
605	ADDRESS BUS	
	A5U2, PIN 13	64HU
	A5U2, PINS 9, 8	9P9F
	A5U12, PINS 2, 3	HPF6
	A5U2, PINS 1, 3	UF9P
	A5U2, PINS 4, 6	A8H9
	A5U12, PINS 4, 5	2225
	A5U12, PINS 6, 7	0258
	A5U12, PINS 13, 14	H6PP
	A5U12, PINS 11, 12	074P
	A5U12, PINS 9, 10	HU57
	A5U21, PINS 11, 12	F1PF
	A5U21, PINS 9, 10	722H
	A5U21, PINS 2, 3	050U
	A5U21, PINS 4, 5	F44F
	A5U21, PINS 6, 7	A66A
606	A6U30, PIN 5	9P9F
	A6U30, PIN 4	HPF6
	A6U30, PIN 1	A8H9
	A6U29, PIN 11	UF9P
607	A6U29, PIN 10	89F1
	A6U30, PIN 6	HA34
	A6U29, PIN 8	AU6C
608	A5U11, PIN 17	VLP
	A5U3, PIN 4	VHP
609	A8U17, PIN 15	VH
	A8U18, PIN 15	VH
	A8U19, PIN 15	VH
	A8U20, PIN 15	VH
	A8U21, PIN 15	VH
	A8U22, PIN 15	VH
610	A8U24, PIN 2	VH
	A8U24, PIN 1	VH
	A8U24, PIN 12	VH
	A8U24, PIN 13	722H
	A8U24, PIN 14	050U
	A8U24, PIN 15	F44F
	A8U29, PIN 6	VL
	A8U29, PIN 8	A41U
	A8U29, PIN 5	H335
	A8U29, PIN 4	VLP
	A8U29, PIN 10	AC99
611	A6U26, PIN 12	1079
	A6U26, PIN 10	VH
	A6U26, PIN 8	VH
	A6U26, PIN 6	1079
	A6U26, PIN 4	1079
	A6U26, PIN 2	1079
	A6U29, PIN 2	VH
	A6U29, PIN 6	VH
612	A6U25, PIN 2	6526
	A6U25, PIN 5	VL
	A6U25, PIN 7	VL
	A6U25, PIN 10	6526
	A6U25, PIN 12	6526
612 (Cont'd)	A6U25, PIN 15	6526
	A6U28, PIN 9	VL
	A6U28, PIN 5	VL
VH=755U, VHP755U, VL=0000, VLP=0000		

SIGNATURE ANALYSIS PROCEDURE NO. 7.

a. Set 1611A LINE switch to off position.

b. Remove A8 board from 1611A and reinstall on Extender Board A14.

c. Connect signature analyzer probes to the following circuit points:

START ..... A8U15, Pin 10 (TP7)
STOP ..... A8U15, Pin 10 (TP7)
CLOCK ..... A5U11, Pin 17 (DBIN)
GND ..... A8TP (GND)

d. Set signature analyzer controls as follows:

START ..... ┐
STOP ..... ┤
CLOCK ..... ┘
HOLD ..... Released

e. Hold DON'T CARE key down and set LINE switch to on position. Keep DON'T CARE key held down for several seconds to force 1611A into loop to check error in hardware.

NOTE

"ERROR IN HARDWARE"message must be displayed during test no. 7 in order for correct signatures to occur. If a wrong key is pressed or circuit pins are shorted together, repeat the power up sequence.

f. Verify that signature measurements called out in troubleshooting tree match the following table.

MEASUREMENT NUMBER	TEST POINT	SIGNATURE
701	VH	7C3U
702	A8U18, PIN 4	FAH7
	A8U18, PIN 7	3608
	A8U18, PIN 9	21FU
	A8U18, PIN 12	A6C8
	A8U19, PIN 4	FAH7
	A8U19, PIN 7	3608
	A8U19, PIN 9	21FU
	A8U19, PIN 12	A6C8
	A8U21, PIN 4	7081

Figure 8-4.
1611A Troubleshooting (Sheet 3 of 8)

MEASUREMENT TNUMBER	TEST POINT	SIGNATURE
702 (Cont'd)	A8U21, PIN 7	4H2C
	A8U21, PIN 9	68H2
	A8U21, PIN 12	C799
	A8U22, PIN 4	7081
	A8U22, PIN 7	4H2C
	A8U22, PIN 9	68H2
	A8U22, PIN 12	C799
703	A8U18, PIN 15	51F1
	A8U18, PIN 1	693U
	A8U19, PIN 15	C83P
704	A8U7, PIN 13	1200
	A8U7, PIN 3	VLP
	A8U7, PIN 4	VH
	A8U7, PIN 11	VLP
	A8U7, PIN 10	VHP
	A8U29, PIN 13	P9UU
	A8U29, PIN 12	P9UU
	A8U29, PIN 9	P9UU
	A8U29, PIN 8	P9UU
	A8U2, PIN 5	VHP
	A8U2, PIN 4	P9UU
	A8U2, PIN 6	92F0
	A8U24, PIN 15	38H3
	A8U24, PIN 14	756A
	A8U24, PIN 13	8AU8
705	A8U18, PIN 3	A575
	A8U18, PIN 6	897A
	A8U18, PIN 10	4648
	A8U18, PIN 13	F534
	A8U18, PIN 2	F4CP
	A8U18, PIN 5	749F
	A8U18, PIN 11	FF87
	A8U18, PIN 14	F34F
	A8U19, PIN 3	3555
	A8U19, PIN 6	P463
	A8U19, PIN 10	A27P
	A8U19, PIN 13	6U1A
	A8U21, PIN 3	1A2U
	A8U21, PIN 6	58UF
	A8U21, PIN 10	73C9
	A8U21, PIN 13	5607
	A8U22, PIN 3	8F4A
	A8U22, PIN 6	6HF8
	A8U22, PIN 10	C936
	A8U22, PIN 13	5A3C
	A8U22, PIN 2	3420
	A8U22, PIN 5	4247
	A8U22, PIN 11	5864
	A8U22, PIN 14	PAH5
706	A8U14, PIN 3	AUUC
	A8U14, PIN 4	34U8
	A8U14, PIN 5	7P27
	A8U14, PIN 6	CU13
	A8U9, PIN 3	HU89

MEASUREMENT NUMBER	TEST POINT	SIGNATURE
706 (Cont'd)	A8U9, PIN 4	6UF4
	A8U9, PIN 5	37P2
	A8U9, PIN 6	9CU1
	A8U6, PIN 3	AUUC
	A8U6, PIN 4	34U8
	A8U6, PIN 5	7P27
	A8U6, PIN 6	CU13
	A8U10, PIN 3	HU89
	A8U10, PIN 4	6UF4
	A8U10, PIN 5	37P2
	A8U10, PIN 6	9CU1
	A8U13, PIN 3	AUUC
	A8U13, PIN 4	34U8
	A8U13, PIN 5	7P27
	A8U13, PIN 6	CU13
	A8U11, PIN 3	HU89
	A8U11, PIN 4	6UF4
	A8U11, PIN 5	37P2
	A8U11, PIN 6	9CU1
707	A8U6, U9, U10, U11, U13, U14 PIN 1	VH
	A8U6, U9, U10, U11, U13, U14, PIN 2	VLP
	A8U6, U9, U10, U11, U13, U14, PIN 7	VL
	A8U14, U19, PIN 9	A69P
	A8U6, U10, PIN 9	50PA
	A8U11, U13, PIN 9	C86H
708	A8U7, PIN 13	F4A8
	A8U7, PIN 12	1PU3
	A8U16, PIN 15	1PU3
	A8U16, PIN 14	2F2P
	A8U16, PIN 13	0001
	A8U16, PIN 12	VLP
	A8U7, PIN 11	VLP
	A8U7, PIN 10	VHP
	A8U29, PIN 13	VHP
	A8U29, PIN 12	VHP
	A8U29, PIN 9	VHP
	A8U29, PIN 8	VHP
	A8U2, PIN 1	VHP
	A8U2, PIN 3	VLP
709	A8U5, PIN 15	VLP
	A8U5, PIN 5	VL
710	A8U2, PIN 13	VHP
	A8U2, PIN 12	VH
	A8U2, PIN 11	VLP

MEASUREMENT NUMBER	TEST POINT	SIGNATURE
711	A8U21, PIN 2	H576
	A8U21, PIN 5	846A
	A8U21, PIN 11	965P
	A8U21, PIN 14	HA14
	A8U19, PIN 2	45HC
	A8U19, PIN 5	47HH
712	A8U1, PIN 12	VLP
	A8U1, PIN 13	4P18
713	A7U18, PIN 7	VLP
	A7U18, PIN 5	CU13
714	A7U18, PIN 9	VHP
715	A7U30, PIN 15	VLP
	A7U30, PIN 14	VLP
	A7U30, PIN 13	VLP
	A7U30, PIN 12	VHP
	A7U31, PIN 8	VHP
	A7U31, PIN 11	VHP
	A7U31, PIN 10	VLP
	A7U31, PIN 9	VHP
	A7U19, PIN 11	VHP
	A7U19, PIN 10	VLP
	A7U19, PIN 9	VHP
716	A8U2, PIN 9	VH
	A8U2, PIN 10	9443
717	A8U8, PIN 1	VL
	A8U8, PIN 11	VL
718	A8U4, PIN 13	VL
	A8U4, PIN 3	VL
719	A8U5, PIN 15	VLP
720	A7U18, PIN 11	VL
	A7U18, PIN 12	7P27
721	A7U18, PIN 7	VLP
	A7U18, PIN 5	CU13
722	A7U20, PIN 14	VL
723	A7U33, PIN 11	VL
724	A7U18, PIN 12	7P27
725	A7U32, PIN 6	VL
	A7U32, PIN 10	VL
	A7U32, PIN 12	VL

MEASUREMENT NUMBER	TEST POINT	SIGNATURE
726	A7U33, PIN 3	VH
	A7U33, PIN 4	VL
	A7U33, PIN 5	VH
727	A7U18, PIN 13	AUUC
	A7U18, PIN 4	34U8
	A7U18, PIN 12	7P27
	A7U18, PIN 5	CU13

SIGNATURE ANALYSIS PROCEDURE NO. 8

a. Set 1611A LINE switch to off position.

b. Remove A8 board from 1611A and reinstall on Extender Board A14.

c. Connect signature analyzer probes to the following circuit test points.

START ..... A5U11, Pin 36
STOP ..... A5U11, Pin 36
CLOCK ..... A5U11, PIN 18
GND ..... A5TP (GND)

d. Set signature analyzer controls as follwos:

START ..... ⌜
STOP ..... ⌞
CLOCK ..... ⌜
HOLD ..... Released

e. Ground A5U3, pin 6.

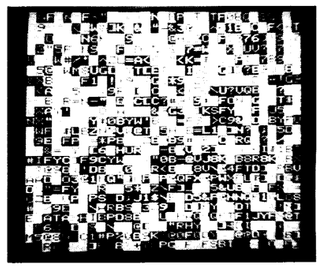
f. Set 1611A LINE switch to on position.

MESUREMENT NUMBER	TEST POINT	SIGNATURE
801	A8U15, PIN 10	VL
	A8U15, PIN 14	H335
	A8U15, PIN 12	C719
	A8U16, PIN 15	H335
	A8U16, PIN 14	F44F
	A8U16, PIN 13	050U
	A8U16, PIN 12	H140
	A8U7, PIN 12	H335
	A8U7, PIN 13	A66A
	A8U7, PIN 11	HPF6
	A8U7, PIN 10	AC99
	A8U29, PIN 13	A8H9
	A8U29, PIN 12	UF9P
	A8U29, PIN 9	9P9F
	A8U29, PIN 8	A41U
	A8U2, PIN 1	VHP
VH=755U, VHP=755U, VL=0000, VLP=0000		

Figure 8-4. 1611A Troubleshooting (Sheet 4 of 8)

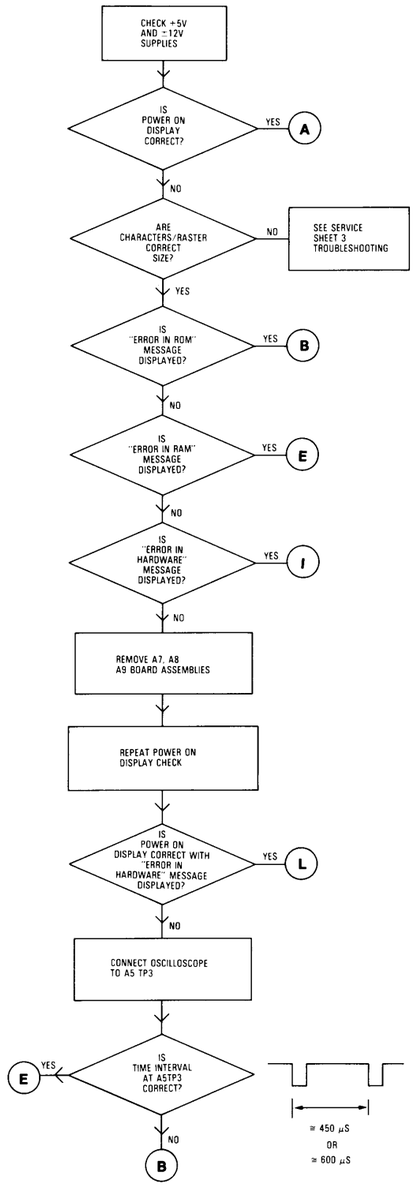
NOTE: CURSOR IN TRIGGER FIELD SHOULD BE BLINKING

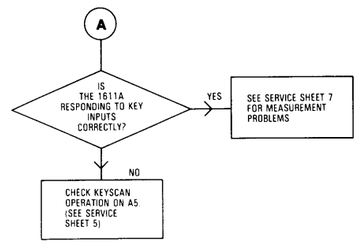
EXAMPLE OF CORRECT POWER-ON DISPLAY

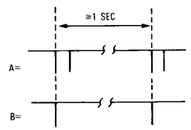


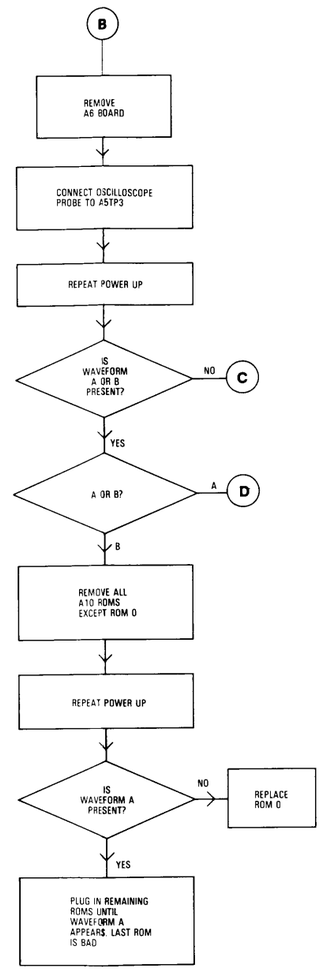
EXAMPLE OF BAD POWER-ON DISPLAY WITH CORRECT CHARACTER AND RASTER SIZE (A3 INT. ADJUSTMENT FULL CW)

NOTE THE FOLLOWING PROCEDURES DO NOT APPLY TO OPTIONS 068 AND 080. IF EITHER OF THESE PERSONALITY PANEL MODULES ARE INSTALLED IN YOUR 1611A, REFER TO SECTION VII FOR SIGNATURE ANALYSIS PROCEDURES.









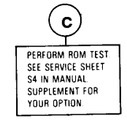


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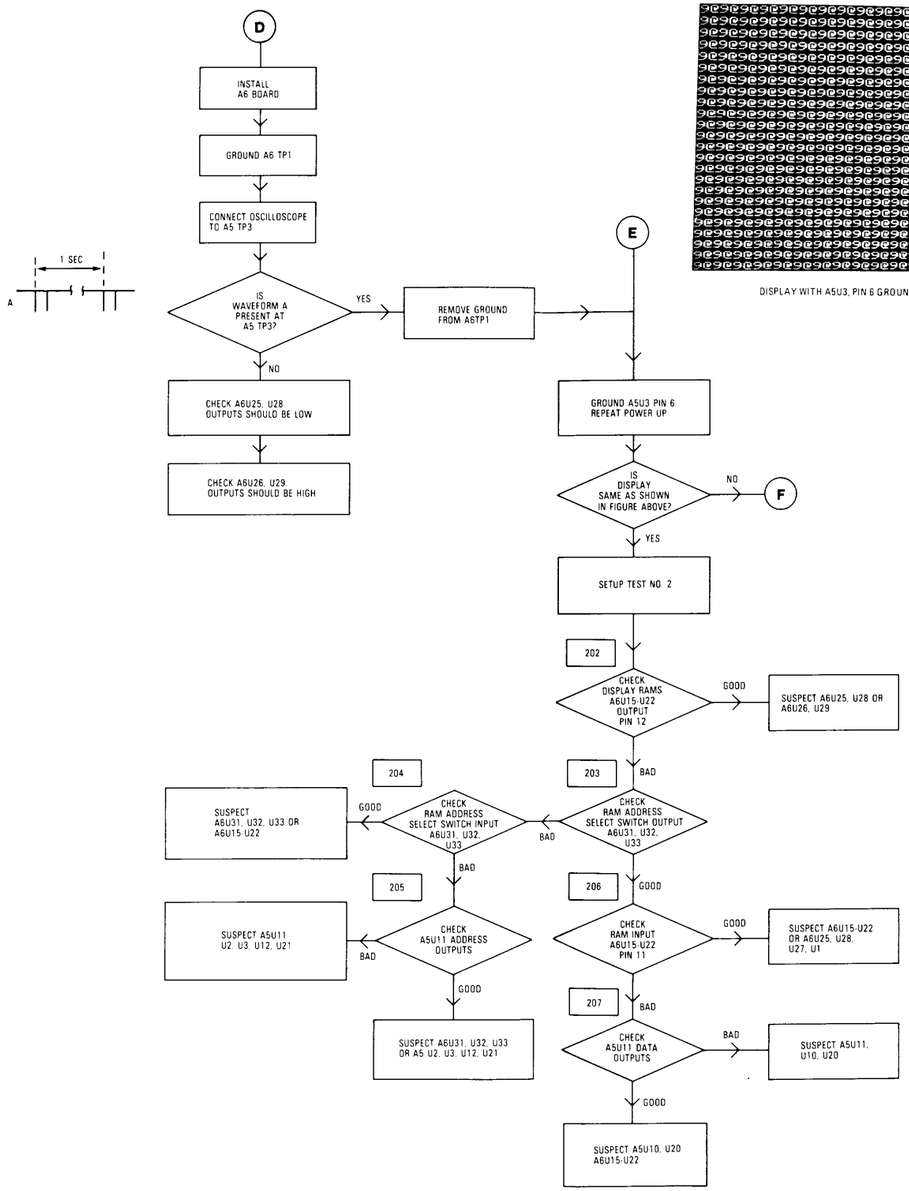
Figure 8-4.
1611A Troubleshooting (Sheet 5 of 8)



DISPLAY WITH A5U3, PIN 6 GROUNDED

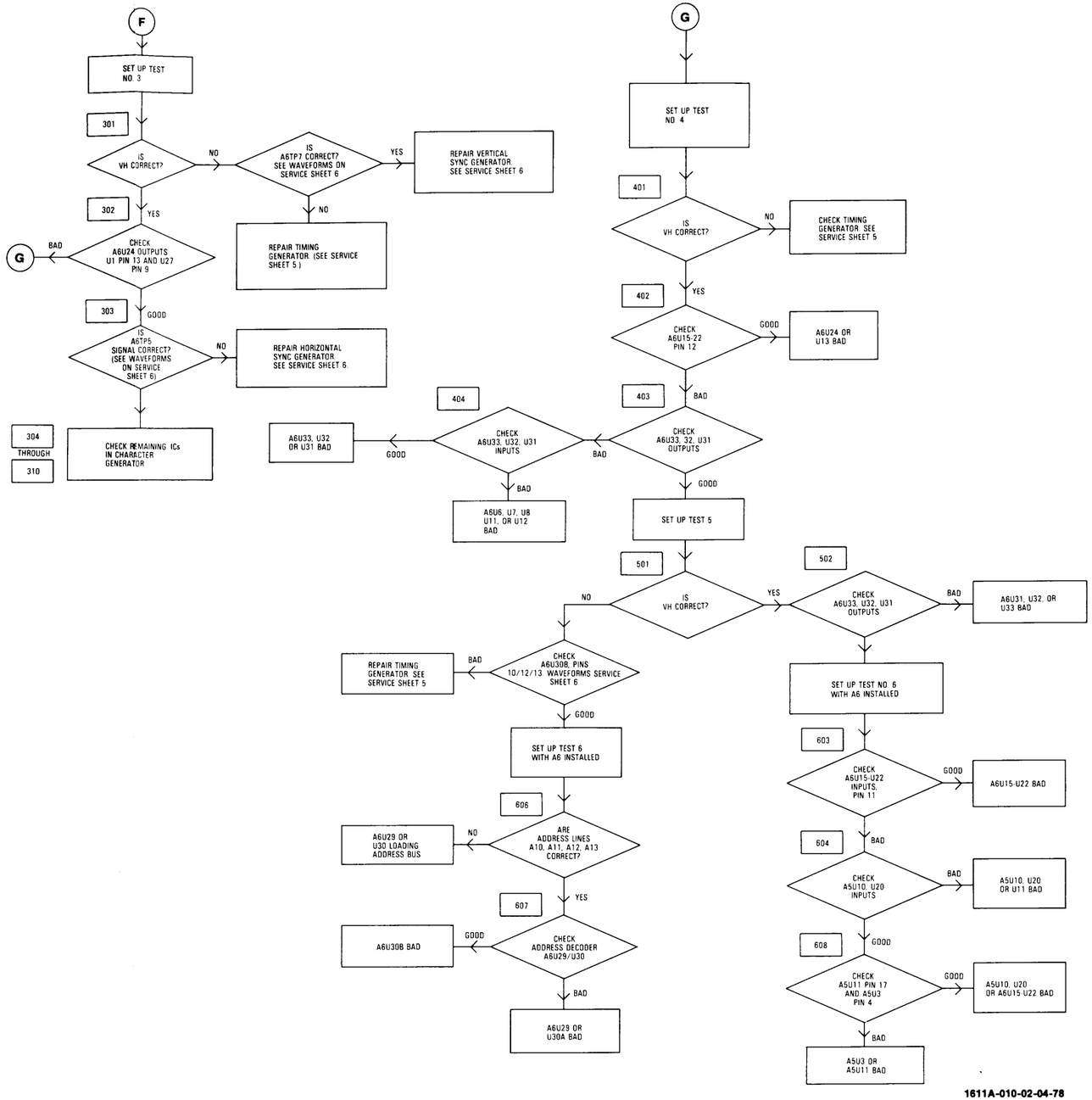
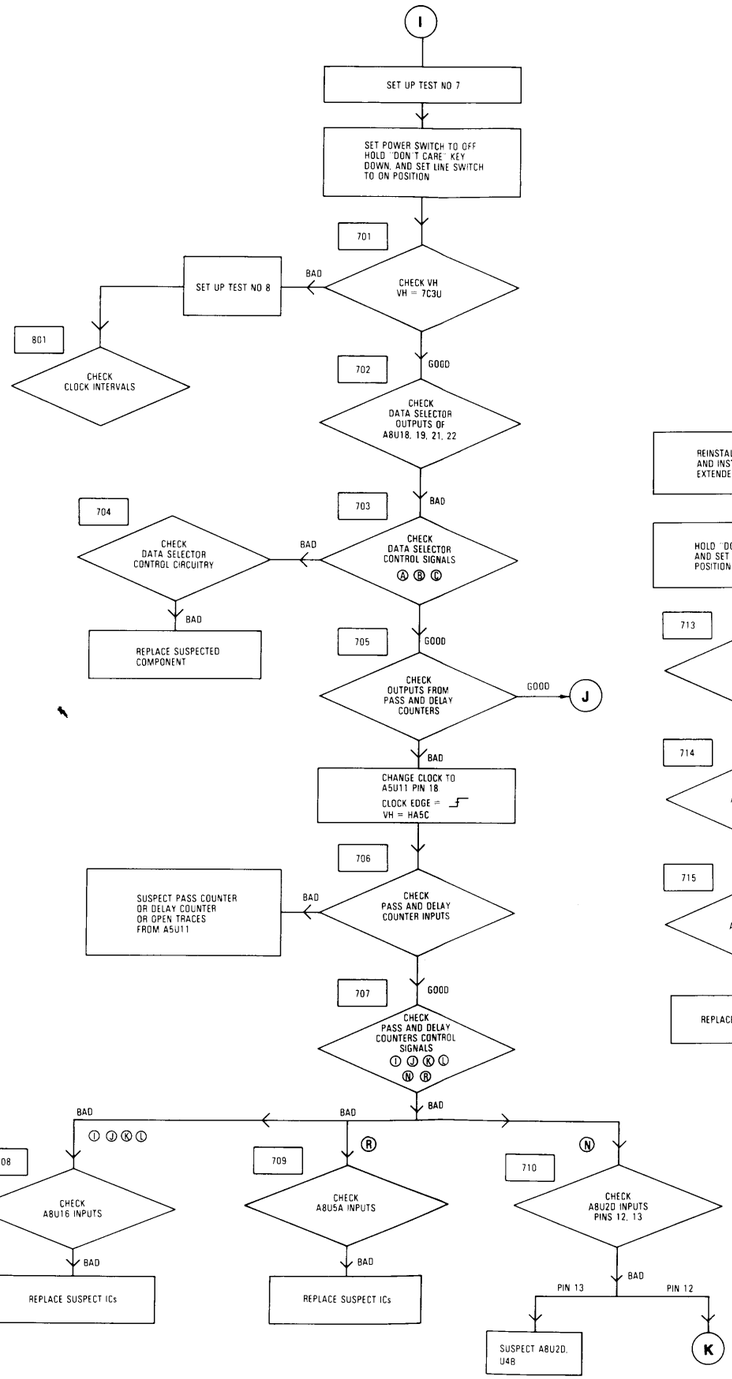


Figure 8-4. 1611A Troubleshooting (Sheet 6 of 8)


I
SET UP TEST NO 7
SET POWER SWITCH TO OFF HOLD "DON'T CARE" KEY DOWN, AND SET LINE SWITCH TO ON POSITION
701
CHECK VH VH = 7C3U
BAD
SET UP TEST NO 8
801
CHECK CLOCK INTERVALS
GOOD
702
CHECK DATA SELECTOR OUTPUTS OF A8U18, 19, 21, 22
703
BAD
CHECK DATA SELECTOR CONTROL SIGNALS (A) (B) (C)
704
CHECK DATA SELECTOR CONTROL CIRCUITRY
BAD
REPLACE SUSPECTED COMPONENT
GOOD
705
CHECK OUTPUTS FROM PASS AND DELAY COUNTERS
GOOD
J
BAD
CHANGE CLOCK TO A5U11 PIN 18 CLOCK EDGE = VH = HA5C
706
CHECK PASS AND DELAY COUNTER INPUTS
BAD
SUSPECT PASS COUNTER OR DELAY COUNTER OR OPEN TRACES FROM A5U11
GOOD
707
CHECK PASS AND DELAY COUNTERS CONTROL SIGNALS (I) (J) (K) (L) (N) (R)
BAD
BAD
BAD
(I) (J) (K) (L)
708
CHECK A8U16 INPUTS
BAD
REPLACE SUSPECT ICs
(R)
709
CHECK A8U5A INPUTS
BAD
REPLACE SUSPECT ICs
(N)
710
CHECK A8U20 INPUTS PINS 12, 13
BAD
PIN 13
SUSPECT A8U20, U48
PIN 12
K
J
711
CHECK DATA SELECTOR INPUTS FROM MEMORY STATE COUNTER
BAD
CHANGE CLOCK TO A5U11 PIN 18 CLOCK SLOPE = VH = HA5C
712
CHECK MEMORY COUNTER INPUTS A8U1
BAD
PIN 12
REINSTALL A8 BOARD IN 1611A, AND INSTALL A7 BOARD ON EXTENDER BOARD A14
HOLD "DON'T CARE" KEY DOWN AND SET LINE SWITCH TO ON POSITION
713
CHECK A7U18 PINS 7 AND 5
GOOD
714
CHECK A7U18 CLOCK PIN 9
BAD
715
CHECK A7U30 INPUTS
REPLACE SUSPECT COMPONENT
PIN 13
716
CHECK A8U2C INPUTS
PIN 9
BAD
PIN 10
BAD
708
CHECK A8U16 INPUTS
BAD
REPLACE SUSPECTED IC
717
CHECK A8U8B INPUTS PIN 1, PIN 11
PIN 11
BAD
PIN 1
BAD
718
CHECK A8U4A
GOOD
SUSPECT U4A OR U8B
BAD
719
CHECK A8U5A INPUT PIN 15
GOOD
SUSPECT U5A OR U4A
BAD
REINSTALL A8 BOARD IN 1611A, AND INSTALL A7 BOARD ON EXTENDER BOARD A14
HOLD "DON'T CARE" KEY DOWN AND SET POWER SWITCH TO ON
720
CHECK A7U18 PIN 12
BAD
SUSPECT A7U18 OR OPEN TRACE BETWEEN A5U11 AND A7U18
GOOD
714
CHECK CLOCK AT A7U18 PIN 9
BAD
715
CHECK A7U30 INPUTS
REPLACE SUSPECT IC
SUSPECT A7U3
OR A8U8B
SUSPECT A7U20
U9, U32, U33
SUSPECT A7U
SUSPECT A7U18
OR U33C
SUSPECT A7U30
OR A7U18

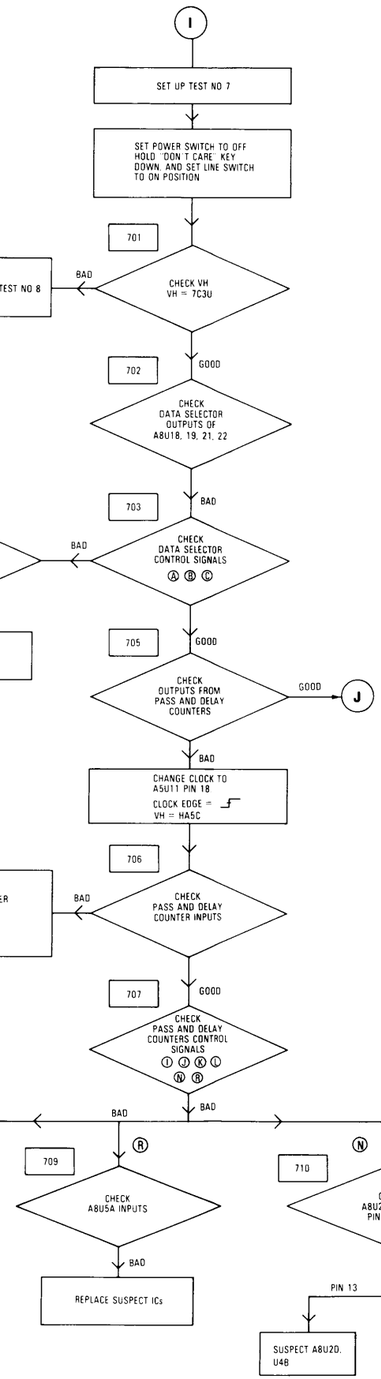


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Figure 8-4.
1611A Troubleshooting (Sheet 7 of 8)

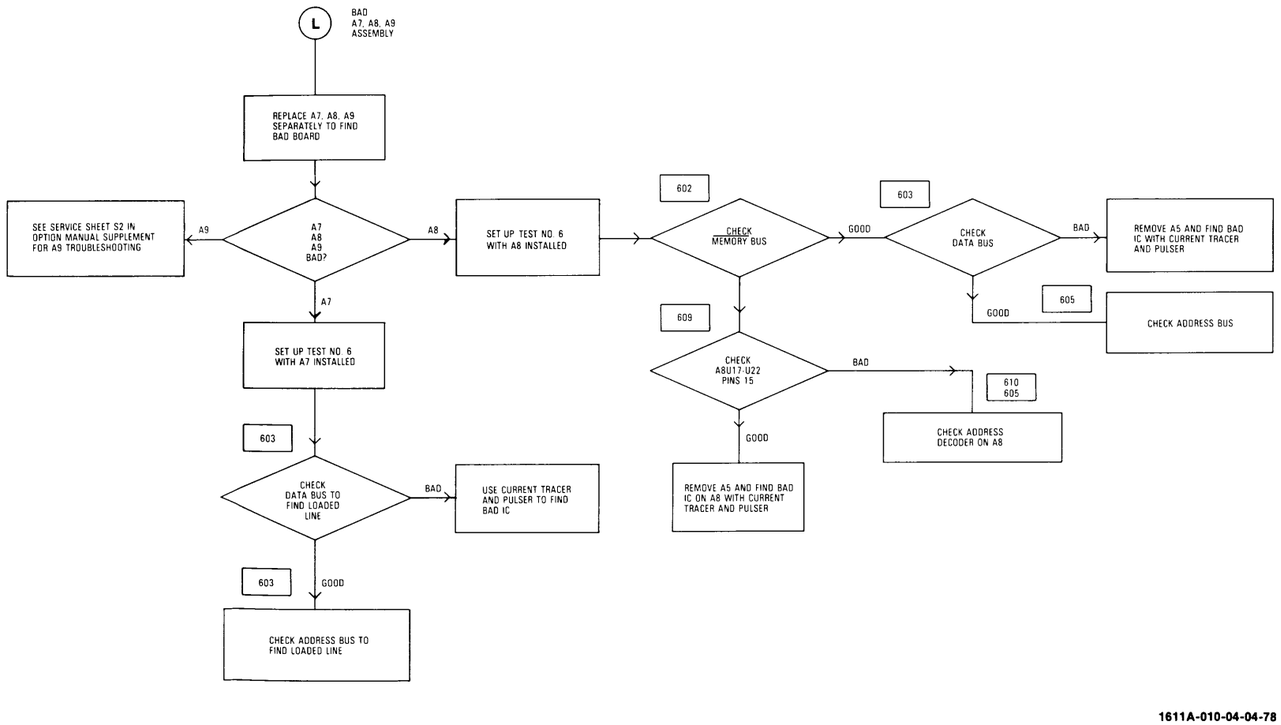

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Figure 8-4. 1611A Troubleshooting (Sheet 8 of 8)

BLOCK DIA

Each block
assembly in
areas are desc
rear of this m
the personalit
ment for a pa
are described
each personali

POWER SUPP
—12, and +5 v

DISPLAY DRIV
three digital s
deflection, ver
that drive the
also developed

KEYBOARD. K
of keys for ent
1611A. The ke
through a keyb

MICROPROCE
BOARD SCAN
contains an 8
1611A, a timi
signals used i
ning circuit
read the keyb
its instruction
processor read
the personality
A6, A7, and A
red).

RAM AND FC
contains the
display infor
resulting from
board. RAM is
and the displ
continuously

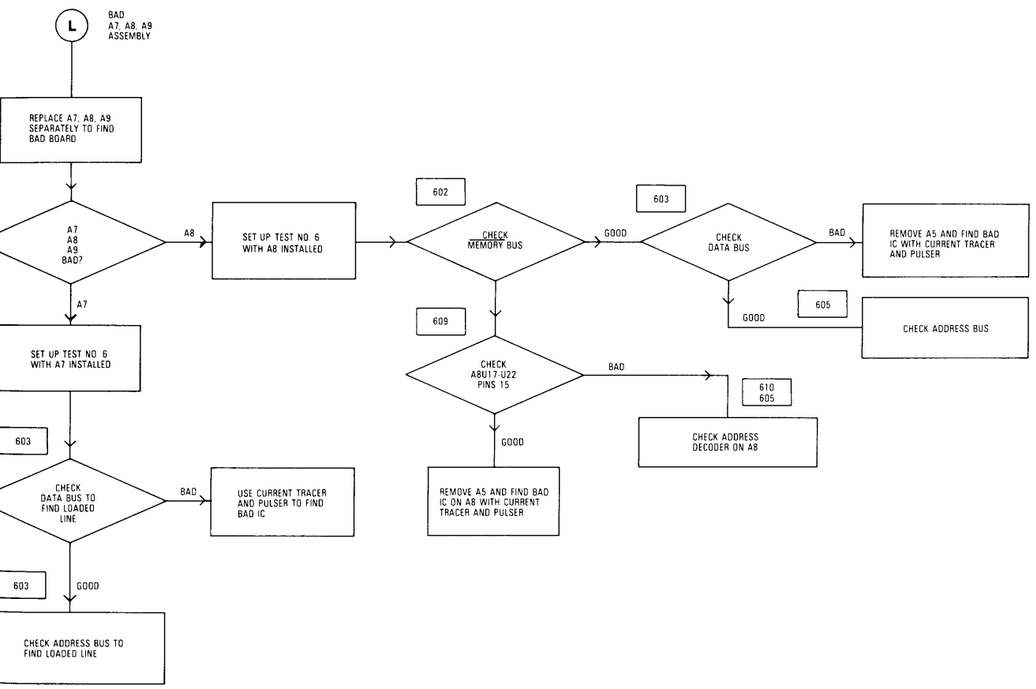

Figure 8-4. 1611A Troubleshooting (Sheet 8 of 8)

BLOCK DIAGRAM DESCRIPTION

Each block in the diagram represents a board assembly in the 1611A. Blocks in the gray-shaded areas are described in detail on service sheets at the rear of this manual. The remaining blocks make up the personality module which configures the instrument for a particular microprocessor. These blocks are described in detail in a manual supplement for each personality module.

POWER SUPPLY. Power supply A2 provides the +2, —12, and +5 volts required for operation of the 1611A.

DISPLAY DRIVER AND CRT. Display Driver A3 uses three digital signals from A6 to generate horizontal deflection, vertical deflection, and blanking signals that drive the CRT. Dc high voltages for the CRT are also developed on this board.

KEYBOARD. Keyboard Assembly A4 contains a matrix of keys for entering measurement parameters into the 1611A. The keyboard is read by the microprocessor through a keyboard scanning circuit on A5.

MICROPROCESSOR, SYSTEM TIMING, AND KEYBOARD SCANNER ASSEMBLY. This assembly (A5) contains an 8080A microprocessor that controls the 1611A, a timing generator that provides basic clock signals used in the instrument, and a keyboard scanning circuit which enables the microprocessor to read the keyboard. The 8080 microprocessor gets its instructions from ROM Board A10. The microprocessor reads the keyboard, monitors switches on the personality panel, and controls and monitors the A6, A7, and A8 assemblies via the buses (shown in red).

RAM AND FORMAT GENERATOR. Assembly A6 contains the random-access memory that stores display information and temporary information resulting from trace specifications entered on the keyboard. RAM is time shared between the microprocessor and the display character generator. The RAM is continuously scanned by the character generator which converts display information stored in RAM into a video signal that drives the display. Horizontal and vertical sync signals that control Display Driver A3 are also generated on this board.

COMPARATOR. Comparator A7 consists of the trigger comparator and measurement control circuits. This board compares the information from the system under test with the trace specification and supplies the appropriate measurement signals to the A8 board.

DATA STORE AND COUNTERS. A8 contains the high-speed memory where data from the microprocessor under test is stored and counters that count time, delay, and trigger occurrences.

PERSONALITY BOARD. Personality Board A9 interfaces the 1611A to the microprocessor under test. It collects address, data, and status information during each machine or instruction cycle of the microprocessor under test and provides a clock that tells the A7 and A8 boards when to process the information. The Personality Board also contains circuitry which allows the 1611A to halt the microprocessor under test and a circuit which generates the test signals available at the PROBE TEST socket on A11.

ROM BOARD. ROM Board A10 provides a read-only memory which contains instructions for the microprocessor on A5 and data latches which store information from External Probe A12.

PERSONALITY PANEL. Personality Panel A11 contains switches that control measurement mode and display format. Panel indicators show status of the microprocessor under test. A probe test socket on the personality panel allows the operator to make a quick operational check of the instrument.

EXTERNAL PROBE. Probe A12 is used to monitor up to eight lines of information in the system under test.

MICROPROCESSOR PROBE. A13 is a dedicated probe that connects the 1611A to the microprocessor under test. It monitors the address, clock, data, and status lines of the microprocessor.

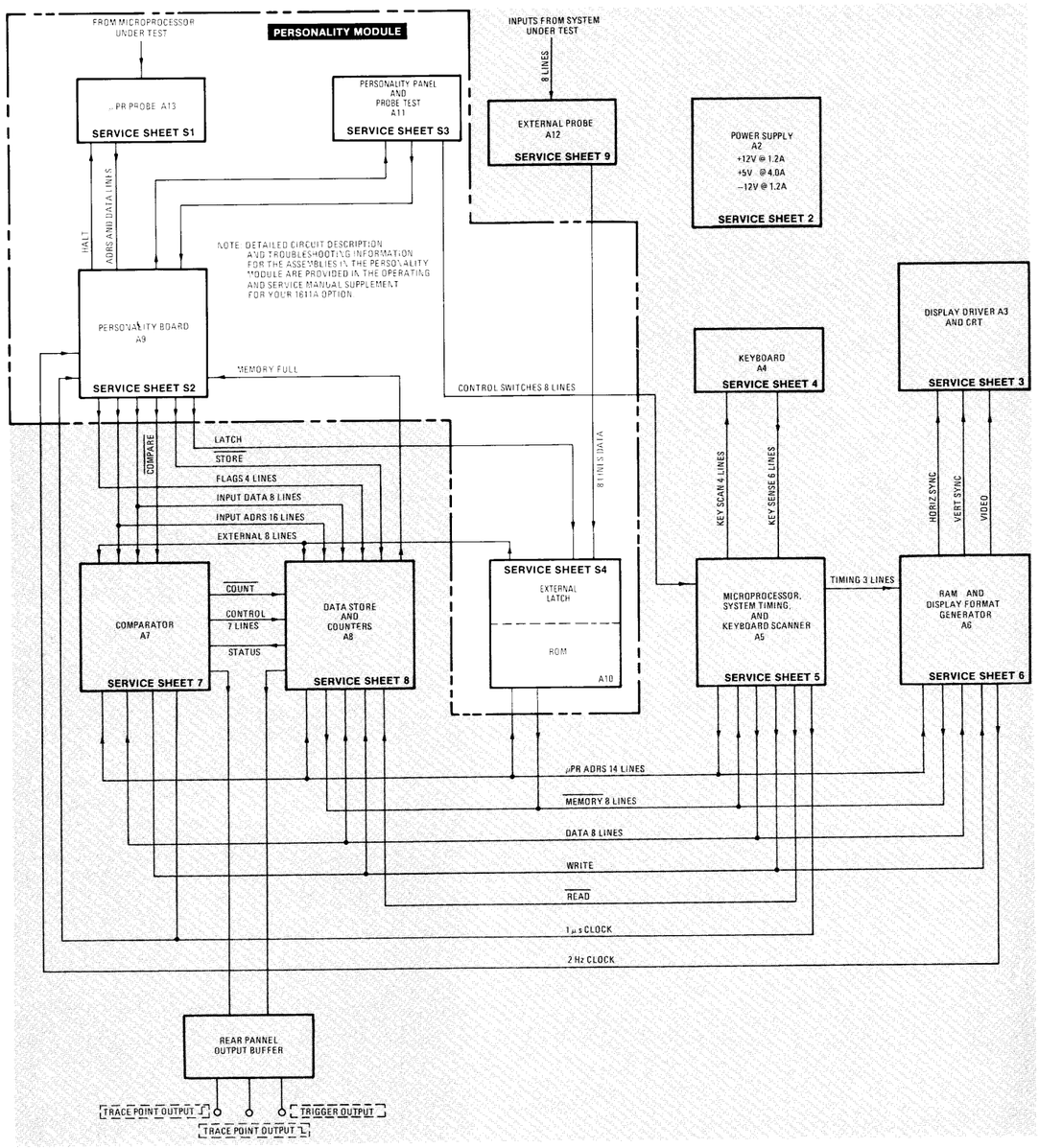

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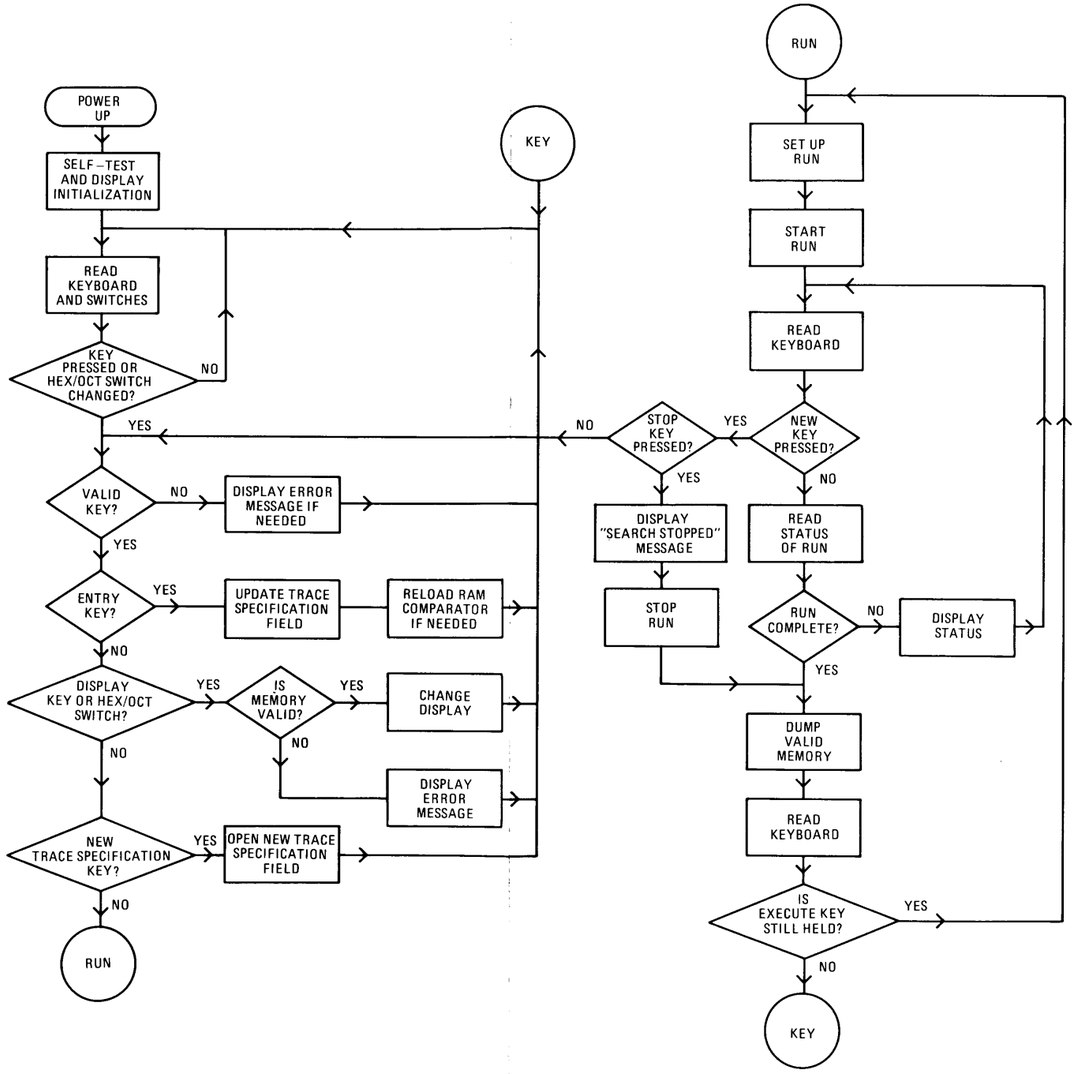
Figure 8-5. 1611A Block Diagram



1611A-030-01-77

Figure 8-6. 1611A Macro Flowchart

A1XA2 INTERCONNECTION LIST

PIN	SIGNAL	ORIGIN	CONNECTS TO
A	COM	A2P1-A	A1C3
1	NC		
B	COM	A2P1-B	A1C3
2	COM	A2P1-2	ALL BOARDS
C	+5V	A2P1-C	A1C3
3	COM	A2P1-3	ALL BOARDS
D	+5V	A2P1-D	A1C3
4	COM	A2P1-4	ALL BOARDS
E	-12V	A2P1-E	AlC2
5	+5V	A2P1-5	ALL BOARDS
F	COM	A1P5-1	A2P1-F, A3P1, CRT GND
6	+5V	A2P1-6	ALL BOARDS
H	COM	A1P5-1	A2P1-H, A3P1, CRT GND
7	+5V	A2P1-7	ALL BOARDS
J	+12V	A2P1-J	A1C1
8	COM	A2P1-8	ALL BOARDS
K	+12V	A2P1-K	A3P1-2, A5P1-100 THROUGH A10P1-100
9	-12V	A2P1-9	A5P1-99 THROUGH A10P1-99
L	-12V	A2P1-L	A1P4-1, A3P1-C
10	XFMR SEC	A1P5-4	A2P1-10
M	COM	A2P1-M	A3P1-3
11	XFMR SEC	A1P5-4	A2P1-11
N	COM	A2P1-N	A3P1-3
12	XFMR SEC	A1P5-5	A2P1-12
P	+12V	A2P1-P	A3P1-K, R
13	XFMR SEC	A1P5-5	A2P1-13
R	COM	A1P5-1	A2P1-R, A3P1, CRT GND
14	XFMR SEC	A1P5-3	A2P1-14
S	COM	A1P5-1	A2P1-S, A3P1, CRT GND
15	XFMR SEC	A1P5-2	A2P1-15

A1XA3 INTERCONNECTION LIST

PIN	SIGNAL	ORIGIN	CONNECTS TO
A	HVSY	A6P1-94	A3P1-A
1	VERT GND	A2P1	A3P1-1
B	NC		
2	+12V	A2P1-K	A3P1-2
C	-12V	A2P1-L	A3P1-C
3	COM	A2P1	
D	V YOKE	A3P1-D	A1P3-2
4	V YOKE	A3P1-4	A1P3-1
E	H YOKE	A3P1-E	A1P3-3
5	H YOKE	A3P1-5	A1P3-3
F	H YOKE	A3P1-F	A1P3-3
6	H YOKE	A3P1-6	A1P3-3
H	H YOKE	A3P1-H	A1P3-4
7	H YOKE	A3P1-7	A1P3-4
J	H YOKE	A3P1-J	A1P3-4
8	H YOKE	A3P1-8	A1P3-4
K	+12V	A2P1-P	A3P1-K
9	COM	A1P5-1	A3P1-9

XA1A3 INTERCONNECTION LIST (CONT'D)

PIN	SIGNAL	ORIGIN	CONNECTES TO
L	HHSY	A6P1-95	A3P1-L
10	HORIZ GND	A2P1	A3P1-10
M	GRID 1	A3P1-M	A1P4-4
11	FOCUS	A3P1-11	A1P4-3
N	CATHODE	A3P1-N	A1P4-6
12	GRID 2	A3P1-12	A1P4-5
P	+5V	A2P1	A3P1-P
13	COM	A1P5-1	A3P1-13
R	+12V	A2P1-P	A3P1-R
14	-12V	A2P1-L	A3P1-14
S	VIDEO	A6P1-96	A3P1-S
15	VIDEO GND	A2P1	A3P1-15

A1 INTERCONNECTION LIST (XA5, XA6)

PIN NO.	SIGNAL	ORIGIN	CONNECTS TO
1	+5V	A2P1	A5P1-1, A6P1-1
2	+5V	A2P1	A5P1-2, A6P1-2
3	KS0	A4W1-15	A5P1-3
4	KS1	A4W1-2	A5P1-4
5	KS2	A4W1-14	A5P1-5
6	KS3	A4W1-3	A5P1-6
7	KS4	A4W1-13	A5P1-7
8	KS7	A4W1-4	A5P1-8
9	KS GND	A4W1-1, 5, 12, 16	A5P1-9
10	KS GND	A4W1-1, 5, 12, 16	A5P1-10
11	GND on XA5, +5V on XA6	A2P1	A5P1-11, A6P1-11
12	GND on XA5,+5V on XA6	A2P1	A5P1-12, A6P1-12
13	SCAN D	A5P1-13	A4W1-10
14	SCAN A	A5P1-14	A4W1-7
15	SCAN B	A5P1-15	A4W1-8
16	SCAN C	A5P1-16	A4W1-9
17	SW0	A11W1-14	A5P1-17
18	SW1	A11W1-1	A5P1-18
19	SW2	A11W1-13	A5P1-19
20	SW3	A11W1-2	A5P1-20
21	SW4	A11W1-12	A5P1-21
22	SW5	A11W1-3	A5P1-22
23	SW6	A11W1-11	A5P1-23
24	SW7	A11W1-4	A5P1-24
25	NC		
26	NC		
27	GND on XA5, +5V on XA6	A2P1	A5P1-27, A6P1-27
28	GND on XA5,+5V on XA6	A2P1	A5P1-28, A6P1-28
29	GND	A2P1	A5P1-29, A6P1-29
30	GND	A2P1	A5P1-30, A6P1-30

Figure 8-7. Service Sheet 1, Main Board Assembly A1, Interconnections (Sheet 1 of 4)

A1 INTERCONNECTION LIST (XA5, XA6) (CONT'D)

PIN NO.	SIGNAL	ORIGIN	CONNECTS TO
31	GND	A2P1	A5P1-31, A6P1-31
32	GND	A2P1	A5P1-32, A6P1-32
33	GND	A2P1	A5P1-33, A6P1-33
34	GND	A2P1	A5P1-34, A6P1-34
35	GND	A2P1	A5P1-35, A6P1-35
36	GND	A2P1	A5P1-36, A6P1-36
37	GND	A2P1	A5P1-37, A6P1-37
38	GND	A2P1	A5P1-38, A6P1-38
39	PRWCK	A5P1-39	A6P1-39
40	GND	A2P1	A5P1-40, A6P1-40
41	GND	A2P1	A5P1-41, A6P1-41
42	HμPCY	A5P1-42	A6P1-42
43	GND	A2P1	A5P1-43, A6P1-43
44	GND	A2P1	A5P1-44, A6P1-44
45	NC		
46	LDSTOR	A8P1-46	A9P1-46
47	PEXCK	A9P1-47	A10P1-47
48	NC		
49	NC		
50	LLSRE	A5P1-50	A6P1-50
51	NC		
52	NC		
53	NC		
54	NC		
55	NC		
56	200 ns CK	A5P1-56	A6P1-56
57	NC		
58	1 μs CK	A5P1-58	A7P1-58, A9P1-58
59	2 Hz CK	A6P1-59	A9P1-59
60	$\overline{M0}$	A6P1, A8P1, A10P1-60	A5P1-60
61	$\overline{M1}$	A6P1, A8P1, A10P1-61	A5P1-61
62	$\overline{M2}$	A6P1, A8P1, A10P1-62	A5P1-62
63	$\overline{M3}$	A6P1, A8P1, A10P1-63	A5P1-63
64	$\overline{M4}$	A6P1, A8P1, A10P1-64	A5P1-64
65	$\overline{M5}$	A6P1, A8P1, A10P1-65	A5P1-65
66	$\overline{M6}$	A6P1, A8P1, A10P1-66	A5P1-66
67	$\overline{M7}$	A6P1, A8P1, A10P1-67	A5P1-67
68	D0	A5P1-68	A6P1-68, A7P1-68, A8P1-68
69	D1	A5P1-69	A6P1-69, A7P1-69, A8P1-69
70	D2	A5P1-70	A6P1-70, A7P1-70, A8P1-70
71	D3	A5P1-71	A6P1-71, A7P1-71, A8P1-71
72	D4	A5P1-72	A6P1-72, A7P1-72, A8P1-72
73	D5	A5P1-73	A6P1-73, A7P1-73, A8P1-73
74	D6	A5P1-74	A6P1-74, A7P1-74, A8P1-74
75	D7	A5P1-75	A6P1-75, A7P1-75, A8P1-75

A1 INTERCONNECTION LIST (XA5, XA6) (CONT'D)

PIN NO.	SIGNAL	ORIGIN	CONNECTS TO
76	LREAD	A5P1-76	A7P1-76, A8P1-76
77	HWRT	A5P1-77	A6P1-77, A7P1-77, A8P1-77
78	A0	A5P1-78	A6P1-78, A7P1-78, A8P1-78, A10P1-78
79	A1	A5P1-79	A6P1-79, A7P1-79, A8P1-79, A10P1-79
80	A2	A5P1-80	A6P1-80, A7P1-80, A8P1-80, A10P1-80
81	A3	A5P1-81	A6P1-81, A7P1-81, A8P1-81, A10P1-81
82	A4	A5P1-82	A6P1-82, A7P1-82, A10P1-82
83	A5	A5P1-83	A6P1-83, A7P1-83, A10P1-83
84	A6	A5P1-84	A6P1-84, A7P1-84, A10P1-84
85	A7	A5P1-85	A6P1-85, A10P1-85
86	A8	A5P1-86	A6P1-86, A10P1-86
87	A9	A5P1-87	A6P1-87, A7P1-87, A8P1-87, A10P1-87
88	A10	A5P1-88	A6P1-88, A7P1-88. A8P1-88, A10P1-88
89	A11	A5P1-89	A6P1-89, A7P1-89, A8P1-89, A10P1-89
90	A12	A5P1-90	A6P1-90, A7P1-90, A8P1-90, A10P1-90
91	A13	A5P1-91	A6P1-91, A7P1-91, A8P1-91, A10P1-91
92	LDLYL	A7P1-92	A8P1-92, A9P1-92
93	HDSBL	A7P1-93	A8P1-93
94	HTRG	A7P1-94	A8P1-94
95	HARM	A7P1-95	A8P1-95
96	LTPT	A8P1-96	A1U1-5
97	GND	A2P1	
98	GND	A2P1	
99	-12V	A2P1	
100	+12V	A2P1	

A1 INTERCONNECTION LIST (XA7, XA8, XA9P1, XA10P1)

PIN NO.	SIGNAL	ORIGIN	CONNECTS TO
1	+5 V	A2P1	
2	+5 V	A2P1	
3	EXT 0	A10P1-3	A7P1-3, A8P1-3
4	EXT 1	A10P1-4	A7P1-4, A8P1-4
5	EXT 2	A10P1-5	A7P1-5, A8P1-5
6	EXT 3	A10P1-6	A7P1-6, A8P1-6
7	EXT 4	A10P1-7	A7P1-7, A8P1-7
8	EXT 5	A10P1-8	A7P1-8, A8P1-8
9	EXT 6	A10P1-9	A7P1-9, A8P1-9
10	EXT 7	A10P1-10	A7P1-10, A8P1-10
11	INP D0	A9P1-11	A7P1-11, A8P1-11
12	INP D1	A9P1-12	A7P1-12, A8P1-12
13	INP D2	A9P1-13	A7P1-13, A8P1-13
14	INP D3	A9P1-14	A7P1-14, A8P1-14
15	INP D4	A9P1-15	A7P1-15, A8P1-15

A1 INTERCONNECTION LIST (XA5, XA6) (CONT'D)

PIN NO.	SIGNAL	ORIGIN	CONNECTS TO
76	LREAD	A5P1-76	A7P1-76, A8P1-76
77	HWRT	A5P1-77	A6P1-77, A7P1-77, A8P1-77
78	A0	A5P1-78	A6P1-78, A7P1-78, A8P1-78, A10P1-78
79	A1	A5P1-79	A6P1-79, A7P1-79, A8P1-79, A10P1-79
80	A2	A5P1-80	A6P1-80, A7P1-80, A8P1-80, A10P1-80
81	A3	A5P1-81	A6P1-81, A7P1-81, A8P1-81, A10P1-81
82	A4	A5P1-82	A6P1-82, A7P1-82, A10P1-82
83	A5	A5P1-83	A6P1-83, A7P1-83, A10P1-83
84	A6	A5P1-84	A6P1-84, A7P1-84, A10P1-84
85	A7	A5P1-85	A6P1-85, A10P1-85
86	A8	A5P1-86	A6P1-86, A10P1-86
87	A9	A5P1-87	A6P1-87, A7P1-87, A8P1-87, A10P1-87
88	A10	A5P1-88	A6P1-88, A7P1-88. A8P1-88, A10P1-88
89	A11	A5P1-89	A6P1-89, A7P1-89, A8P1-89, A10P1-89
90	A12	A5P1-90	A6P1-90, A7P1-90, A8P1-90, A10P1-90
91	A13	A5P1-91	A6P1-91, A7P1-91, A8P1-91, A10P1-91
92	LDLYL	A7P1-92	A8P1-92, A9P1-92
93	HDSBL	A7P1-93	A8P1-93
94	HTRG	A7P1-94	A8P1-94
95	HARM	A7P1-95	A8P1-95
96	LTPT	A8P1-96	A1U1-5
97	GND	A2P1	
98	GND	A2P1	
99	-12V	A2P1	
100	+12V	A2P1	

A1 INTERCONNECTION LIST (XA7, XA8, XA9P1, XA10P1)

PIN NO.	SIGNAL	ORIGIN	CONNECTS TO
1	+5 V	A2P1	
2	+5 V	A2P1	
3	EXT 0	A10P1-3	A7P1-3, A8P1-3
4	EXT 1	A10P1-4	A7P1-4, A8P1-4
5	EXT 2	A10P1-5	A7P1-5, A8P1-5
6	EXT 3	A10P1-6	A7P1-6, A8P1-6
7	EXT 4	A10P1-7	A7P1-7, A8P1-7
8	EXT 5	A10P1-8	A7P1-8, A8P1-8
9	EXT 6	A10P1-9	A7P1-9, A8P1-9
10	EXT 7	A10P1-10	A7P1-10, A8P1-10
11	INP D0	A9P1-11	A7P1-11, A8P1-11
12	INP D1	A9P1-12	A7P1-12, A8P1-12
13	INP D2	A9P1-13	A7P1-13, A8P1-13
14	INP D3	A9P1-14	A7P1-14, A8P1-14
15	INP D4	A9P1-15	A7P1-15, A8P1-15

A1 INTERCONNECTION LIST (XA7, XA8, XA9P1, XA10P1) (CONT'D)

PIN NO.	SIGNAL	ORIGIN	CONNECTS TO
16	INP D5	A9P1-16	A7P1-16, A8P1-16
17	INP D6	A9P1-17	A7P1-17, A8P1-17
18	INP D7	A9P1-18	A7P1-18, A8P1-18
19	FLAG 0	A9P1-19	A8P1-19
20	FLAG 1	A9P1-20	A8P1-20
21	FLAG 2	A9P1-21	A8P1-21
22	FLAG 3	A9P1-22	A8P1-22
23	INP A0	A9P1-23	A7P1-23, A8P1-23
24	INP A1	A9P1-24	A7P1-24, A8P1-24
25	INP A2	A9P1-25	A7P1-25, A8P1-25
26	INP A3	A9P1-26	A7P1-26, A8P1-26
27	INP A4	A9P1-27	A7P1-27, A8P1-27
28	INP A5	A9P1-28	A7P1-28, A8P1-28
29	INP A6	A9P1-29	A7P1-29, A8P1-29
30	INP A7	A9P1-30	A7P1-30, A8P1-30
31	INP A8	A9P1-31	A7P1-31, A8P1-31
32	INP A9	A9P1-32	A7P1-32, A8P1-32
33	INP A10	A9P1-33	A7P1-33, A8P1-33
34	INP A11	A9P1-34	A7P1-34, A8P1-34
35	INP A12	A9P1-35	A7P1-35, A8P1-35
36	INP A13	A9P1-36	A7P1-36, A8P1-36
37	INP A14	A9P1-37	A7P1-37, A8P1-37
38	INP A15	A9P1-38	A7P1-38, A8P1-38
39	MSC 0	A8P1-39	NOT USED WITH ALL OPTIONS
40	MSC 1	A8P1-40	
41	MSC 2	A8P1-41	NOT USED WITH ALL 1611A OPTIONS
42	MSC 3	A8P1-42	
43	MSC 4	A8P1-43	
44	MSC 5	A8P1-44	
45	HRMC	A7P1-45	A8P1-45, A9P1-45
46	LDSTOR	A8P1-46	A9P1-46
47	PEXCK	A9P1-47	A10P1-47
48	PHLTEN	A8P1-48	A9P1-48
49	NSTOR	A9P1-49	A8P1-49
50	NCP	A9P1-50	A7P1-50
51	HENB	A7P1-51	NOT USED WITH ALL 1611A OPTIONS
52		A7P1-52	
53	HDSB	A7P1-53	
54	LRST	A7P1-54	A8P1-54
55	NCNT	A7P1-55	A8P1-55
56	HPCTC	A8P1-56	A7P1-56
57	HDLEN	A7P1-57	A8P1-57
58	1 μs CK	A5P1-58	A7P1-58, A9P1-58
59	2 Hz CK	A6P1-59	A9P1-59
60	$\overline{M0}$	A6P1, A8P1, A10P1-60	A5P1-60

Figure 8-7. Service Sheet 1, Main Board Assembly A1 Interconnections (Sheet 2 of 4)

A1 INTERCONNECTION LIST (XA7, XA8, XA9P1, XA10P1) (CONT'D)

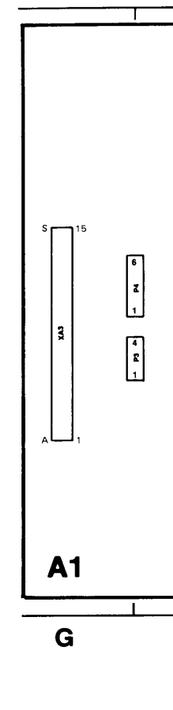
PIN NO.	SIGNAL	ORIGIN	CONNECTS TO
61	$\overline{M1}$	A6P1, A8P1, A10P1-61	A5P1-61
62	$\overline{M2}$	A6P1, A8P1, A10P1-62	A5P1-62
63	$\overline{M3}$	A6P1, A8P1, A10P1-63	A5P1-63
64	$\overline{M4}$	A6P1, A8P1, A10P1-64	A5P1-64
65	$\overline{M5}$	A6P1, A8P1, A10P1-65	A5P1-65
66	$\overline{M6}$	A6P1, A8P1, A10P1-66	A5P1-66
67	$\overline{M7}$	A6P1, A8P1, A10P1-67	A5P1-67
68	D0	A5P1-68	A6P1-68, A7P1-68, A8P1-68
69	D1	A5P1-69	A6P1-69, A7P1-69, A8P1-69
70	D2	A5P1-70	A6P1-70, A7P1-70, A8P1-70
71	D3	A5P1-71	A6P1-71, A7P1-71, A8P1-71
72	D4	A5P1-72	A6P1-72, A7P1-72, A8P1-72
73	D5	A5P1-73	A6P1-73, A7P1-73, A8P1-73
74	D6	A5P1-74	A6P1-74, A7P1-74, A8P1-74
75	D7	A5P1-75	A6P1-75, A7P1-75, A8P1-75
76	LREAD	A5P1-76	A7P1-76, A8P1-76
77	HWRT	A5P1-77	A6P1-77, A7P1-77, A8P1-77
78	A0	A5P1-78	A6P1-78, A7P1-78, A8P1-78, A10P1-78
79	A1	A5P1-79	A6P1-79, A7P1-79, A8P1-79, A10P1-79
80	A2	A5P1-80	A6P1-80, A7P1-80, A8P1-80, A10P1-80
81	A3	A5P1-81	A6P1-81, A7P1-81, A8P1-81, A10P1-81
82	A4	A5P1-82	A6P1-82, A7P1-82, A10P1-82
83	A5	A5P1-83	A6P1-83, A7P1-83, A10P1-83
84	A6	A5P1-84	A6P1-84, A7P1-84, A10P1-84
85	A7	A5P1-85	A6P1-85, A10P1-85
86	A8	A5P1-86	A6P1-86, A10P1-86
87	A9	A5P1-87	A6P1-87, A7P1-87, A8P1-87, A10P1-87
88	A10	A5P1-88	A6P1-88, A7P1-88, A8P1-88, A10P1-88
89	A11	A5P1-89	A6P1-89, A7P1-89, A8P1-89, A10P1-89
90	A12	A5P1-90	A6P1-90, A7P1-90, A8P1-90, A10P1-90
91	A13	A5P1-91	A6P1-91, A7P1-91, A8P1-91, A10P1-91
92	+5 V	A2P1	
93	+5 V	A2P1	
94	HVSY	A6P1-94	A3P1-A
95	HHSY	A6P1-95	A3P1-L
96	VIDEO	A6P1-96	A3P1-S
97	GND	A2P1	
98	GND	A2P1	
99	-12 V	A2P1	
100	+12 V	A2P1	

A1P1 INTERCONNECTION LIST

PIN NO.	SIGNAL	ORIGIN	CONNECTS TO
1	KS GND	A4W1-1	A5P1-9, 10
2	KS1	A4W1-2	A5P1-4
3	KS3	A4W1-3	A5P1-6
4	KS7	A4W1-4	A5P1-8
5	KS GND	A4W1-5	A5P1-9, 10
6	+5 V	A2P1	A4W1-6
7	SCAN A	A5P1-14	A4W1-7
8	SCAN B	A5P1-15	A4W1-8
9	SCAN C	A5P1-16	A4W1-9
10	SCAN D	A5P1-13	A4W1-10
11	GND	A2P1	A4W1-11
12	KS GND	A4W1-12	A5P1-9, 10
13	KS4	A4W1-13	A5P1-7
14	KS2	A4W1-14	A5P1-5
15	KS0	A4W1-15	A5P1-3
16	KS GND	A4W1-16	A5P1-9, 10

A1P2 INTERCONNECTION LIST

PIN NO.	SIGNAL	ORIGIN	CONNECTS TO
1	SW1	A11W1-1	A5P1-18
2	SW3	A11W1-2	A5P1-20
3	SW5	A11W1-3	A5P1-22
4	SW7	A11W1-4	A5P1-24
5	+5 V	A2P1	A11W1-5
6	+5 V	A2P1	A11W1-6
7	+5 V	A2P1	A11W1-7
8	GND	A2P1	A11W1-8
9	GND	A2P1	A11W1-9
10	GND	A2P1	A11W1-10
11	SW6	A11W1-11	A5P1-23
12	SW4	A11W1-12	A5P1-21
13	SW2	A11W1-13	A5P1-19
14	SW0	A11W1-14	A5P1-17

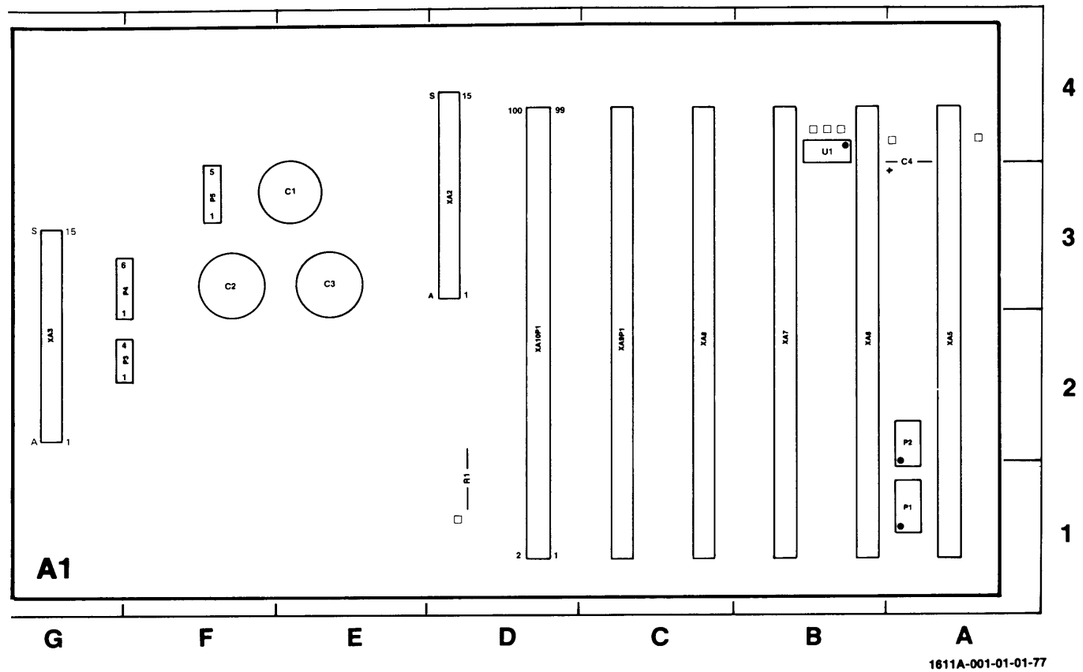


A1P1 INTERCONNECTION LIST

PIN NO.	SIGNAL	ORIGIN	CONNECTS TO
1	KS GND	A4W1-1	A5P1-9, 10
2	KS1	A4W1-2	A5P1-4
3	KS3	A4W1-3	A5P1-6
4	KS7	A4W1-4	A5P1-8
5	KS GND	A4W1-5	A5P1-9, 10
6	+5 V	A2P1	A4W1-6
7	SCAN A	A5P1-14	A4W1-7
8	SCAN B	A5P1-15	A4W1-8
9	SCAN C	A5P1-16	A4W1-9
10	SCAN D	A5P1-13	A4W1-10
11	GND	A2P1	A4W1-11
12	KS GND	A4W1-12	A5P1-9, 10
13	KS4	A4W1-13	A5P1-7
14	KS2	A4W1-14	A5P1-5
15	KS0	A4W1-15	A5P1-3
16	KS GND	A4W1-16	A5P1-9, 10

A1P2 INTERCONNECTION LIST

PIN NO.	SIGNAL	ORIGIN	CONNECTS TO
1	SW1	A11W1-1	A5P1-18
2	SW3	A11W1-2	A5P1-20
3	SW5	A11W1-3	A5P1-22
4	SW7	A11W1-4	A5P1-24
5	+5 V	A2P1	A11W1-5
6	+5 V	A2P1	A11W1-6
7	+5 V	A2P1	A11W1-7
8	GND	A2P1	A11W1-8
9	GND	A2P1	A11W1-9
10	GND	A2P1	A11W1-10
11	SW6	A11W1-11	A5P1-23
12	SW4	A11W1-12	A5P1-21
13	SW2	A11W1-13	A5P1-19
14	SW0	A11W1-14	A5P1-17



REF DESIG	GRID LOC	REF DESIG	GRID LOC
C1	E-3	U1	B-4
C2	F-3	XA2	D-3
C3	E-3	XA3	G-2
C4	A-3	XA5	A-2
P1	A-1	XA6	B-2
P2	A-2	XA7	B-2
P3	F-2	XA8	C-2
P4	F-3	XA9P1	C-2
P5	F-3	XA10P1	D-2
R1	D-1		

Main Board A1 Component Locator
(01611-66501)

Figure 8-7. Service Sheet 1, Main Board Assembly A1 Interconnections (Sheet 3 of 4)

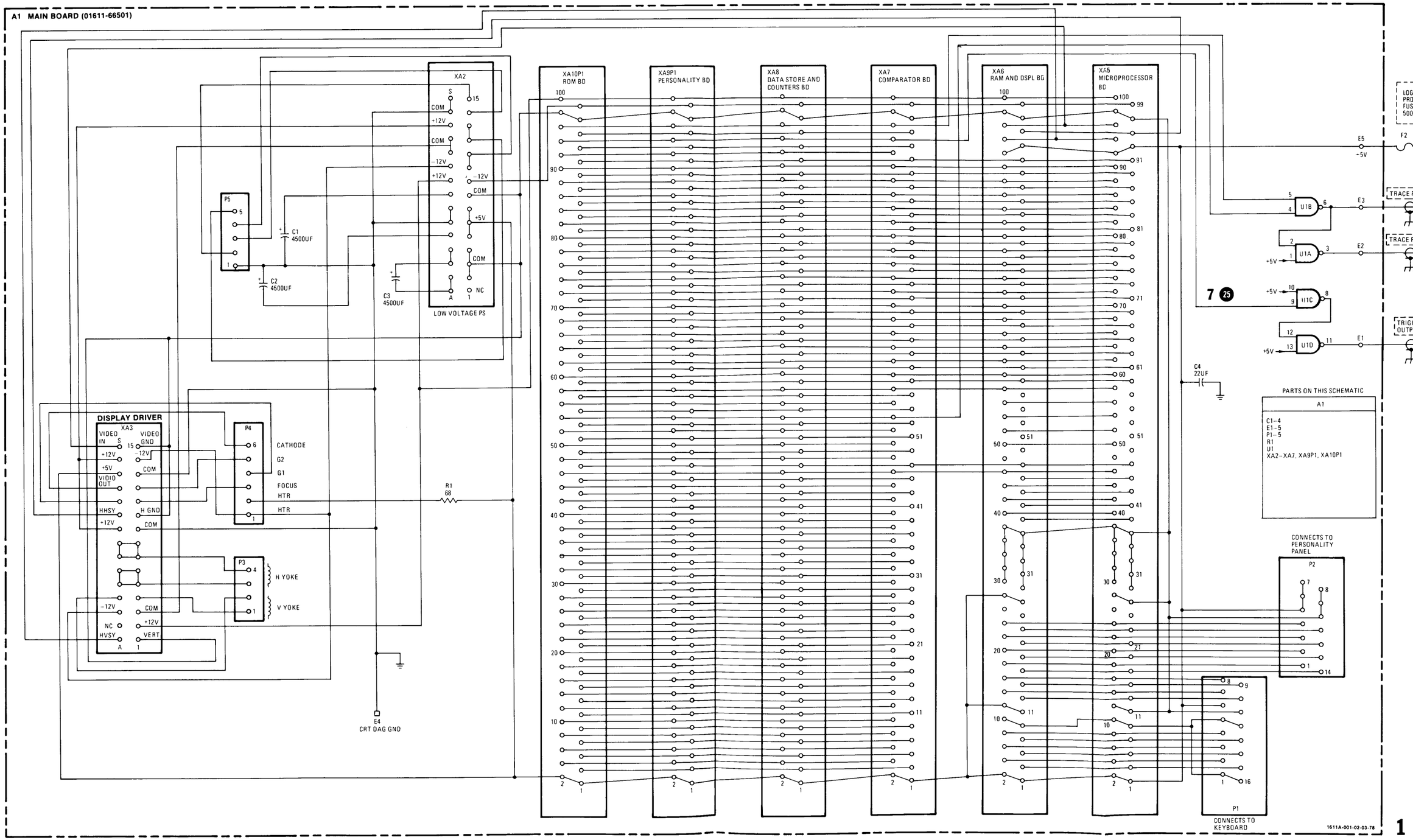


Figure 8-7. Service Sheet 1, Main Board Assembly A1 Interconnections (Sheet 4 of 4)

SERVICE SHEET 2

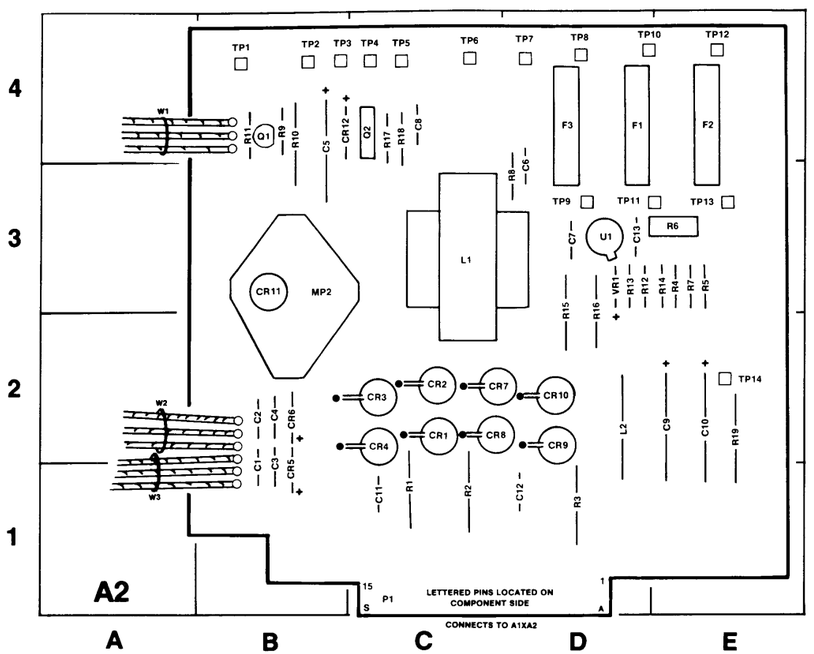
PRINCIPLES OF OPERATION

+5V POWER SUPPLY. The +5V supply is a switching regulator with current limiting and over-voltage protection. The series element Q1 in the switching regulator is either saturated or in the cut-off condition. Therefore, very little power is dissipated in Q1. This keeps power supply efficiency high.

The regulator operates as follows: A2U1 compares output voltage of the power supply and a reference voltage established by the V_{REF} output of A2U1 and divide network R4 through R8. When the output voltage drops below the reference voltage, A2U1 turns Q1 on through A2Q1. When Q1 is turned on, its emitter voltage is very close to the unregulated DC at the input. R4 then increases the voltage reference that is compared to the output voltage. As a result, the reference voltage is higher when Q1 is on than when it is off. This dual threshold determines peak-to-peak ripple of the supply. When Q1 is on, current is supplied to the load through L1. When the upper threshold is met, A2U1 turns Q1 off and the emitter voltage of Q1 goes to -0.6 volts. When Q1 is off, the energy stored in L1 supplies current to the load. This current flows through CR11. When the output voltage of the regulator drops below the lower voltage reference threshold, Q1 again turns on and the cycle repeats.

The +5 volt regulator is protected against short circuits and overloads. When Q1 is on and the peak current through L1 reaches 5 amperes, the voltage between current limit and current sense of A2U1 is sufficient to cause A2U1 to turn Q1 off. After Q1 is turned off the current through L1 must fall below 3.75 amperes and output of the supply must fall below the lower voltage reference before Q1 is turned on again. As the load increases, the on time of Q1 decreases. If there is a malfunction in the regulator and the output of the +5 volt supply goes above 5.6 volts, the voltage developed across R18 will turn on SCR Q2 and blow fuse F3.

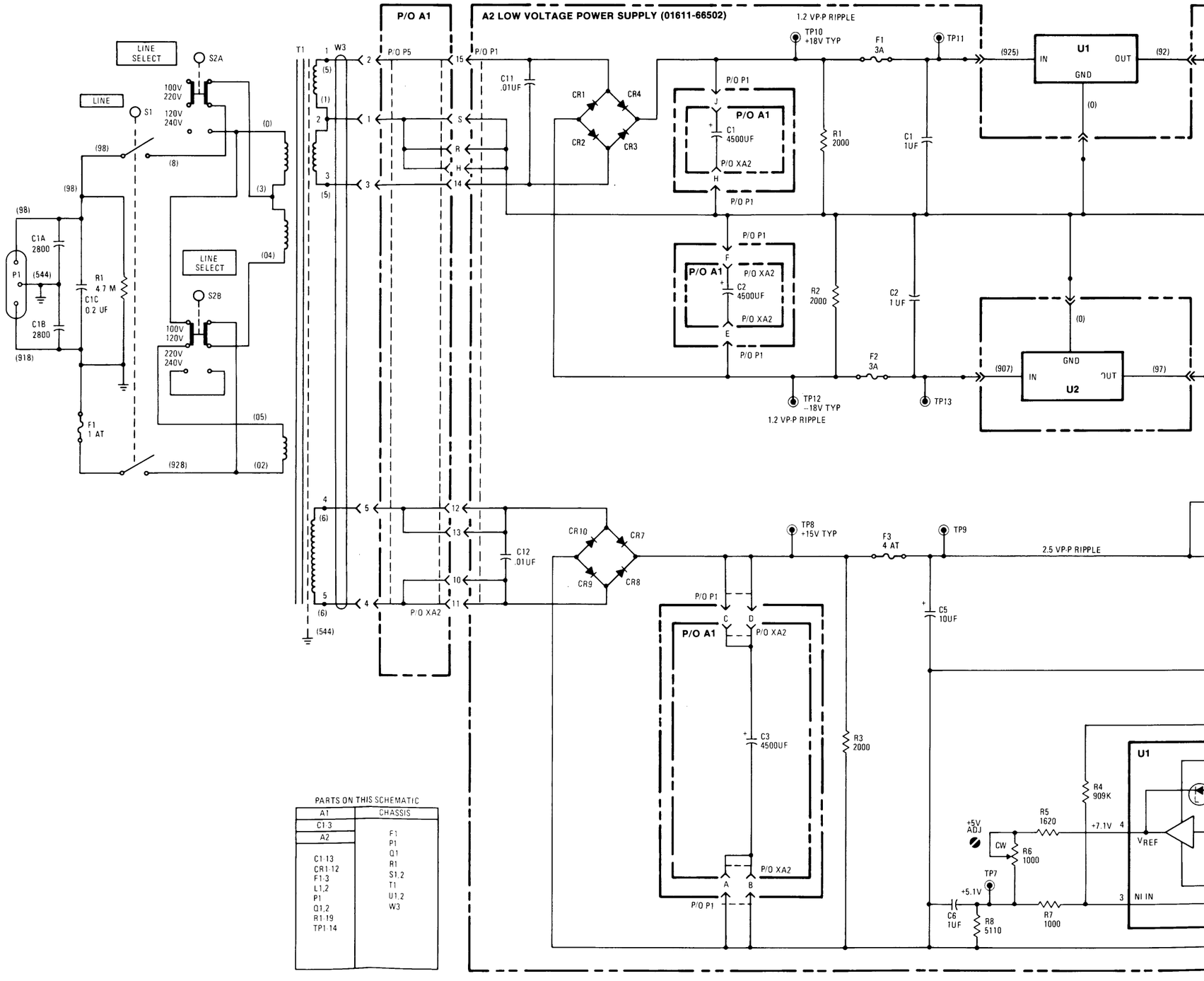
±12 V POWER SUPPLIES. The ±12 volt supplies are three-terminal voltage regulators. They are internally protected against thermal and current overloads.



REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC
C1	B-1	CR2	C-2	L1	C-3	R10	B-4	TP5	C-4
C2	B-2	CR3	C-2	L2	D-2	R11	B-4	TP6	C-4
C3	B-1	CR4	C-2	MP2	B-3	R12	D-3	TP7	D-4
C4	B-2	CR5	B-1	Q1	B-4	R13	D-3	TP8	D-4
C5	B-4	CR6	B-2	Q2	C-4	R14	E-3	TP9	D-3
C6	D-3	CR7	C-2	R1	C-1	R15	D-2	TP10	D-4
C7	D-3	CR8	C-2	R2	C-1	R16	D-2	TP11	D-3
C8	C-4	CR9	D-2	R3	D-1	R17	C-4	TP12	E-4
C9	E-2	CR10	D-2	R4	E-3	R18	C-4	TP13	E-3
C10	E-2	CR11	B-3	R5	E-3	R19	E-2	TP14	E-2
C11	C-1	CR12	B-4	R6	E-3	TP1	B-4	U1	D-3
C12	D-1	F1	D-4	R7	E-3	TP2	B-4	VR1	D-3
C13	D-3	F2	E-4	R8	D-3	TP3	B-4	W1	A-4
CR1	C-2	F3	D-4	R9	B-4	TP4	C-4	W2	A-2
								W3	A-1

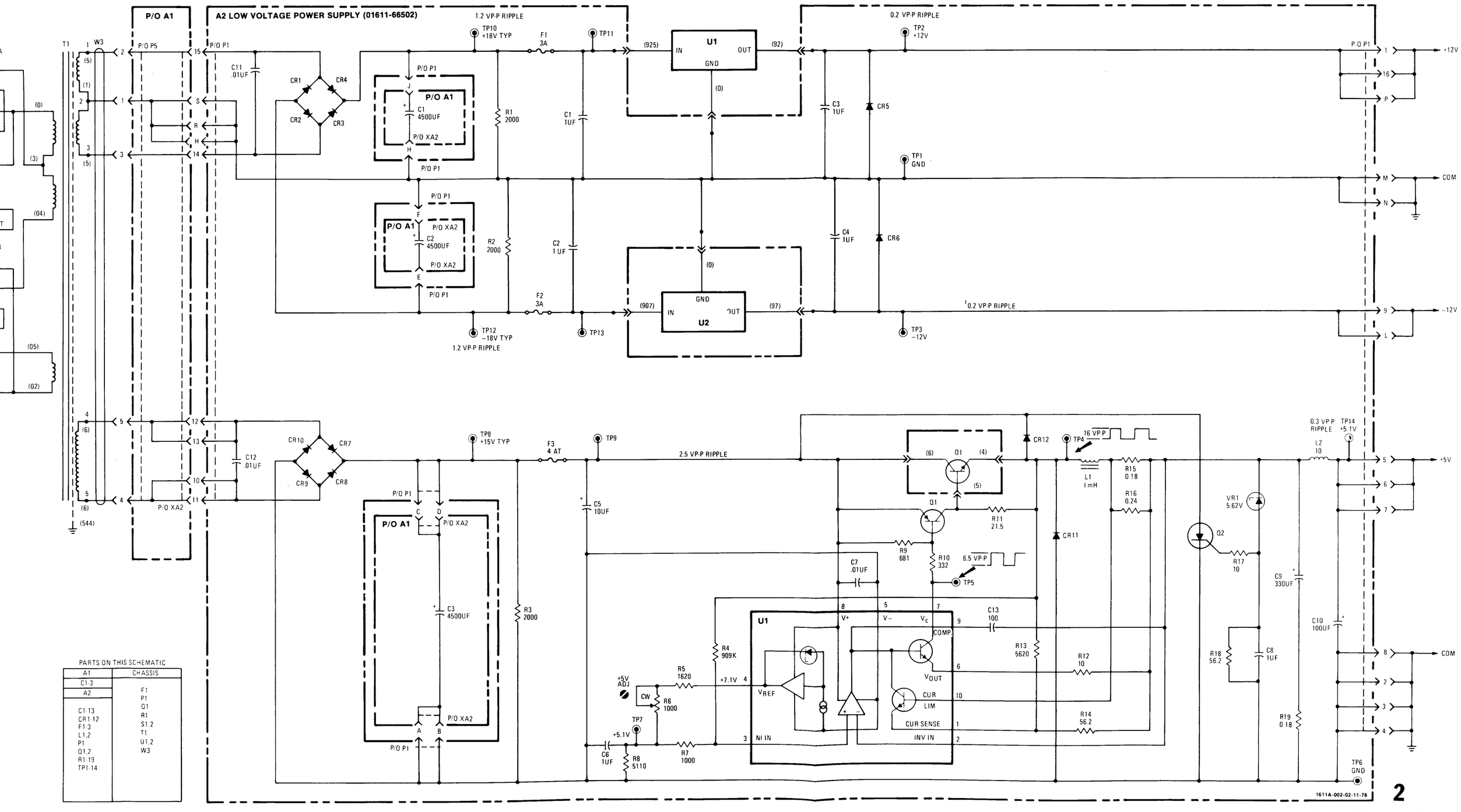
Power Supply A2 Component Locator
(01611-66502)

Figure 8-8. Service Sheet 2, Low Voltage Power Supply A2 (Sheet 1 of 2)



PARTS ON THIS SCHEMATIC

A1	CHASSIS
C1-3	
A2	
C1-13 CR1-12 F1-3 L1,2 P1 Q1,2 R1-19 TP1-14	F1 P1 Q1 R1 S1,2 T1 U1,2 W3



PARTS ON THIS SCHEMATIC

A1	CHASSIS
C1-13	
A2	
C1-13 CR1-12 F1-3 L1,2 P1 Q1,2 R1-19 TP1-14	F1 P1 Q1 R1 S1,2 T1 U1,2 W3

Figure 8-8. Service Sheet 2, Low Voltage Power Supply A2 (Sheet 2 of 2)

SERVICE SHEET 3

PRINCIPLES OF OPERATION

Display Driver A3 generates signals to drive the display. The display is a magnetically-deflected, raster-scanned CRT. Display format is 24 lines of 32 characters each; each line consists of 10 horizontal scans of the CRT. Three signals from the A6 assembly, HVSY, HHSY, and VIDEO control the horizontal deflection, vertical deflection, and video amplifier circuits.

HORIZONTAL SYNC. HHSY (horizontal sync) controls the horizontal deflection circuit and the high-voltage supply. The HHSY signal is applied to U5 where, under normal operation, it is inverted, and used to drive U6. If the HHSY signal has an incorrect repetition rate or pulse width, U5 prevents the outputs of U6 from being on continuously, which would result in damage to U6. U6 provides a current pulse to the primary of T1. The secondary of T1 drives the horizontal deflection and high voltage circuits.

HIGH-VOLTAGE SUPPLY. The HV supply provides dc voltages for the CRT, bias voltage for the horizontal deflection circuit, and +35 volts for the video amplifier.

When Q9 is on, the current through L3 and the primary of T2 increases. When Q9 is turned off, energy stored in L3 and the primary of T2 rapidly charges C27. The result of the rapid charging is a large positive voltage across L3. This voltage is rectified by CR5 to provide the CRT accelerator grid bias. The positive voltage is also coupled to the secondaries of T2 where it is rectified.

HORIZONTAL DEFLECTION CIRCUIT. The secondary of T1 also controls the horizontal deflection circuit. Just before Q1 is turned off, current is flowing in the deflection coil and the beam is at the right side of the CRT. When Q1 is turned off, the deflection coil current changes direction as C7 charges rapidly. After all the energy is transferred to C7, it then discharges through the coil, causing another change in direction of coil current. The rapid charge and discharge of C7 causes a rapid retrace of the beam. At the end of retrace, the voltage across the coil attempts to go negative and charge C7 again. When voltage across the coil reaches a few volts positive, CR1 turns on and becomes the current path for the coil. This voltage clamping by CR1 causes a constant rate of change in coil current. This accounts for the first half of horizontal scan. CR1 is turned on at a positive voltage, rather than zero, to compensate for resistive elements in the coil current path. This keeps the rate of current change from being greater at the beginning of the sweep than at the center or right side of the sweep.

When the beam reaches center screen, the deflection coil current is zero. At this time, Q1 is turned on and the current flow changes direction. This deflects the CRT beam toward the right side of the screen until Q1 turns off. When Q1 turns off, retrace begins.

Compensation for the deflection rate at the sides of the CRT is accomplished using C8. During the first half of the sweep the charge on C8 increases slightly. At center screen, when Q1 is turned on, C8 is slowly discharged, until the beam reaches the end of the sweep. This reduces voltage across the deflection coil at the beginning and end of the sweep, reducing the rate of current change in the coil.

Size of the horizontal scan is controlled by R6. R6 controls the voltage available to the deflection circuit by decreasing the coil current rate of change. Since the period of the sync signal does not vary, the scan will be shorter if the deflection rate is decreased.

Horizontal position is accomplished by injecting a constant current into the deflection coil. R14 determines the current. U1 compares voltage drops across C12 and R4, and drives Q2 and Q3 until the voltage drops are equal. This establishes a constant current through R4.

VERTICAL DEFLECTION CIRCUIT. This circuit generates the vertical sweep and controls height, linearity, and position of the sweep. One vertical sweep of the CRT occurs every 13.7 msec. Vertical sync (HVSY) from A6 controls a ramp generator, which in turn controls current through the deflection coil. When HVSY goes high, Q4 is turned on; this discharges C14 and C15 through R20. HVSY remains high for 0.5 milliseconds (until capacitor charge returns to a few millivolts). When HVSY goes low, Q4 is turned off and C14 and C15 charge at a rate determined by R18 and R19. R18 controls amplitude of the vertical sweep. Since the period of HVSY is constant (13.7 milliseconds), R18 can be used to control the distance the beam is deflected within that period.

The voltage ramp developed at the junction of R20 and C14 is applied to U4. Part of the output of U4 is fed back to C14 and C15 to correct the voltage input of U4 which compensates the ramp generator. R23 controls the amount of feedback, which in turn controls the shape of the sweep generated. The ramp at the output of U4 drives current amplifier U3/Q5/Q6 which maintains a current through the emitter of Q6 that is proportional to the ramp voltage. U3 compares the ramp voltage to voltage across R32. U3 drives Q5 until the inputs to U3 are equal.

At the beginning of the sweep a very small current is flowing through Q6 and a large current is flowing from the +5 volt supply through deflection coil L1. This corresponds with the beam being at the top of the display. As the Q6 current increases, more current from the +5 volt supply flows through Q6 and less through the deflection coil. Coil current decreases and Q6 current increases until the beam reaches center screen. At that time, coil current has reached zero and begins to flow in the opposite direction as Q6 current starts to draw current from the coil and the +5 volts supply. When the beam reaches the bottom of the screen, coil current is about the same as it was at the top of the screen but is flowing in the opposite direction.

At the end of the sweep, Q6 is turned off abruptly, and the current through R32 is reduced to zero. This sudden change in coil current results in a positive voltage pulse at the collector of Q6. This charges C19, using energy stored in the deflection coil. This causes the beam to return to center screen as C19 reaches its peak voltage. C19 then discharges through R62 and the deflection coil. Discharge current and the current through L2 change the coil current direction and return the beam to the top of the CRT. At this time, Q6 starts conducting again and the sweep starts over.

Compensation for deflection rate at the top and bottom of the CRT is accomplished by C20 in a manner similar to that used in the horizontal deflection circuit. Position control is maintained by injecting a constant current into the deflection circuit through R33.

VIDEO. This circuit amplifies the video signal to drive the CRT cathode. Gain control R61 is provided for contrast adjustment of the display.

TROUBLESHOOTING

Before attempting to repair the A3 assembly, verify that horizontal sync, vertical sync and video signals from A6 are present (see waveforms). If these signals are incorrect, see service sheet 6.

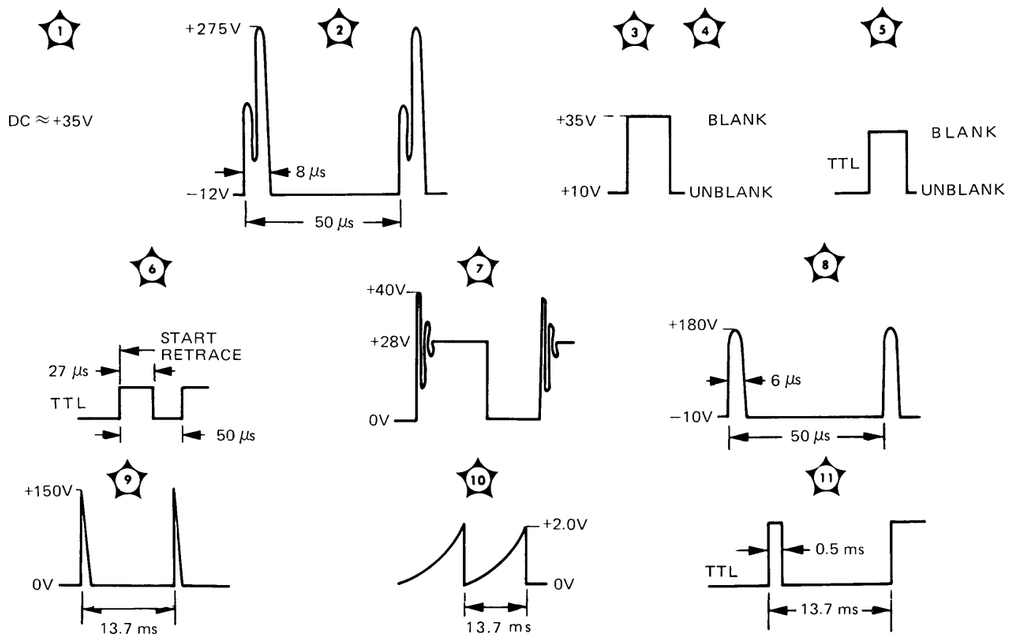
The presence of deflection currents can be checked at A3TP8 and TP9. Isolation of deflection circuits and positioning circuits can be accomplished by removing A3R4 or A3R33; this will cause only a slight shift in position of the display. The horizontal deflection circuit and the video amplifier require voltages from the high voltage supply. Always check the HV supply before troubleshooting deflection or video problems.

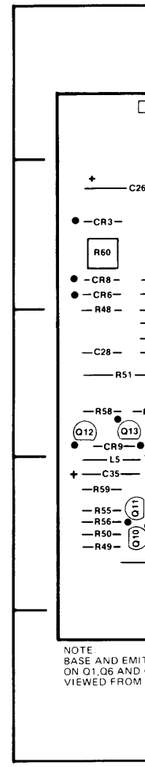
If A3U6, A3Q1 or A3Q9 should fail, check capacitors A3C2, A3C7 or A3C27. Open circuits or a decrease in capacitance can cause the peak voltage across U6 or Q9 to increase, causing breakdowns.

Deflection correction magnets on the coils are permanently attached and are not adjustable. However, they should be inspected for damage if display distortion is evident.

MONOSTABLE U5 TIMING EQUATION

T = 0.4 RC
Where
R=kΩ
C=pF
T=ns





REF DESIG	GRID LOC
C1	C2
C2	C4
C3	B2
C4	C3
C5	E2
C6	E2
C7	D2
C8	D2
C9	E5
C10	E5
C11	E5
C12	E4
C13	F1
C14	G2
C15	G2
C16	G1
C17	B3
C18	G3

responds with the beam being at the top of the display. As the Q6 current increases, more current from the +5 volt supply flows through Q6 and less through the deflection coil. Coil current decreases and Q6 current increases until the beam reaches center screen. At that time, coil current has reached zero and begins to flow in the opposite direction as Q6 current starts to draw current from the coil and the +5 volts supply. When the beam reaches the bottom of the screen, coil current is about the same as it was at the top of the screen but is flowing in the opposite direction.

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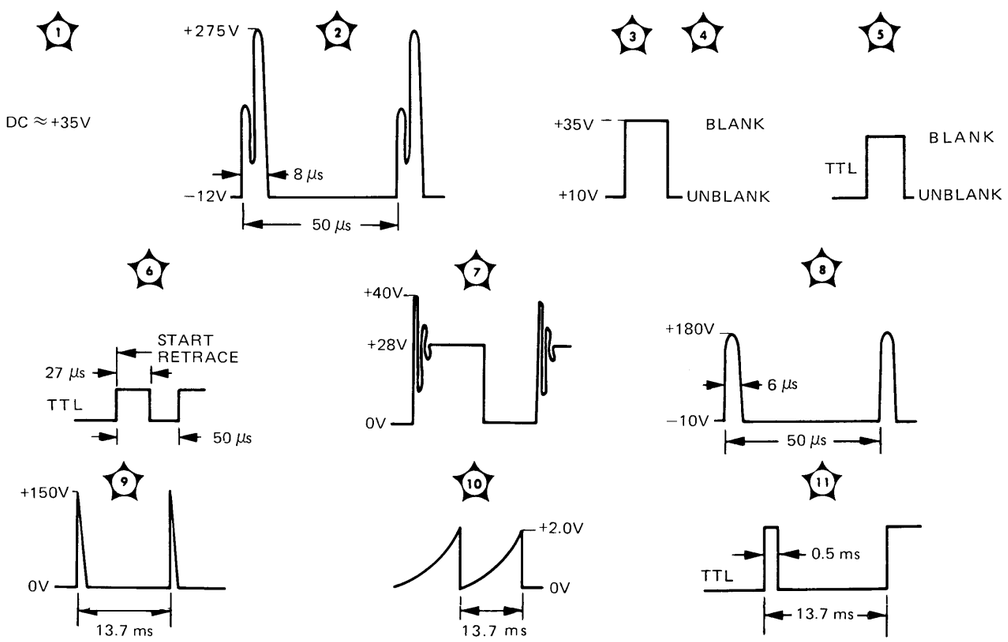
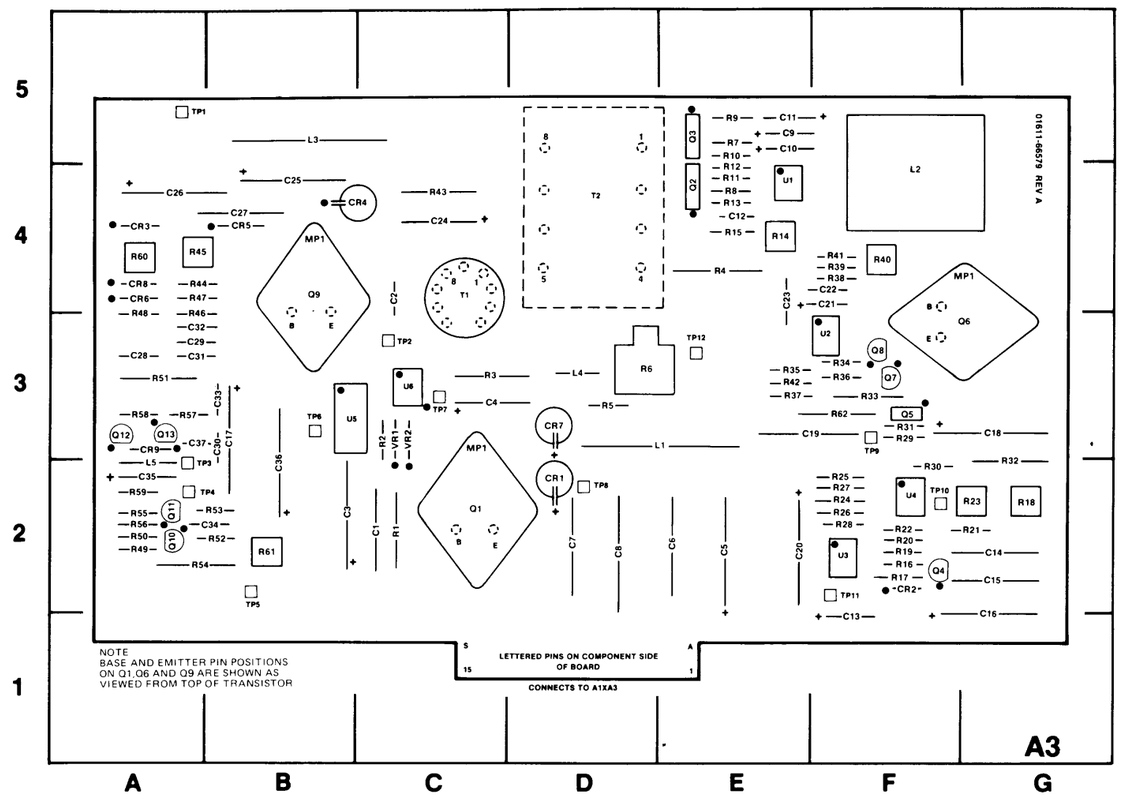
MONOSTABLE U5 TIMING EQUATION

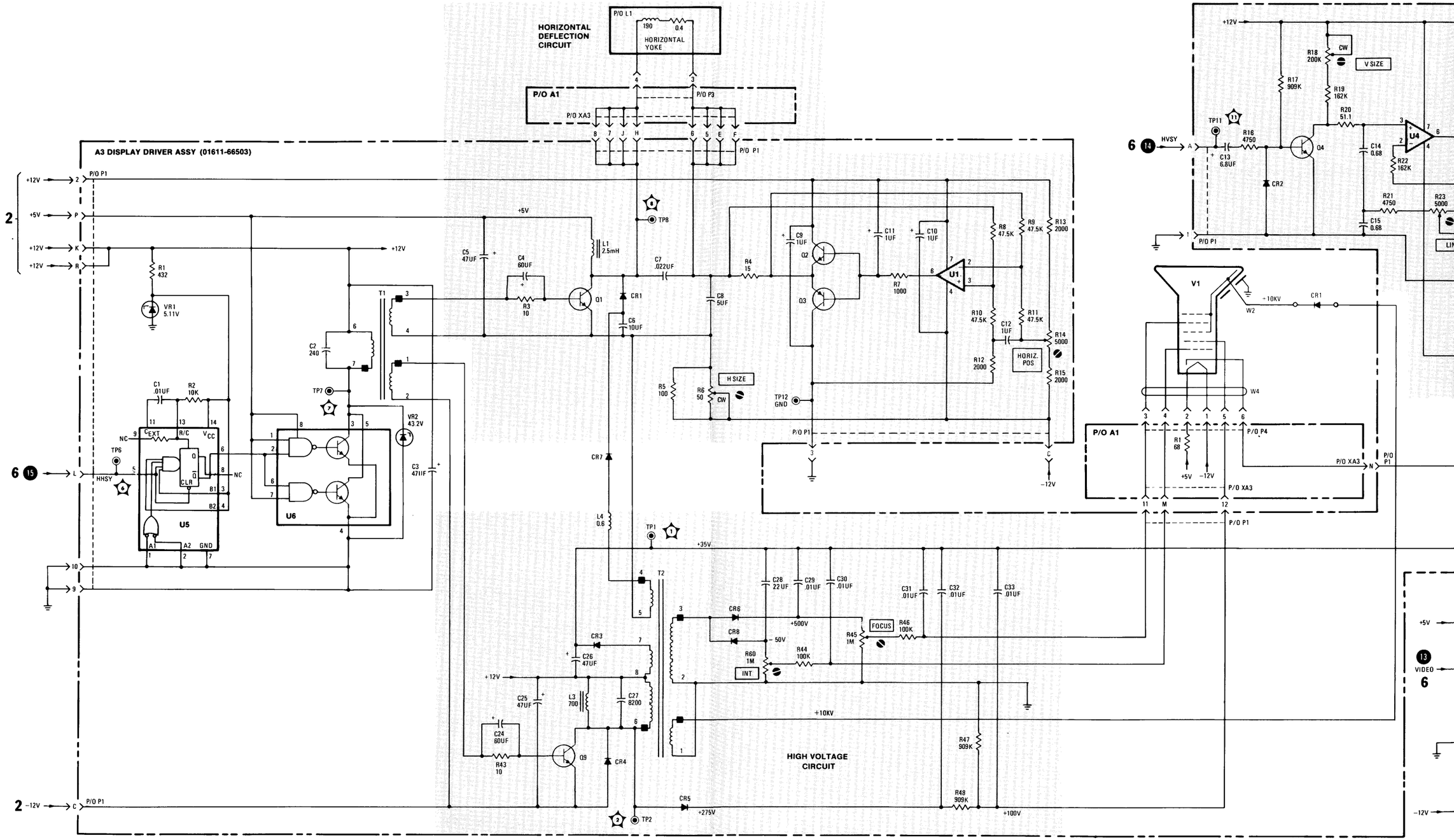
T = 0.4 RC
Where
R=kΩ
C=pF
T=ns

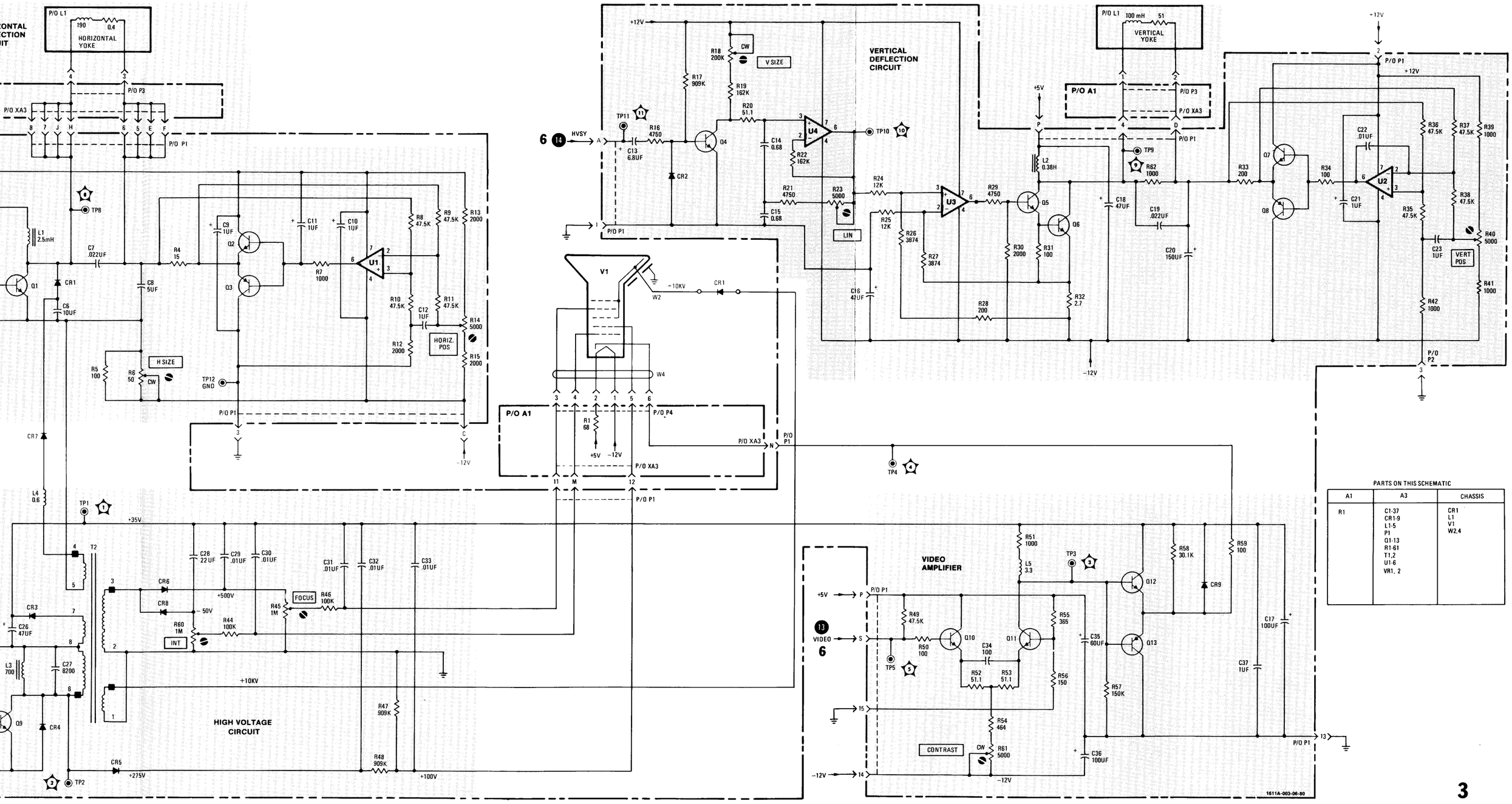




REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC
C1	C2	C19	E3	C37	A3	Q2	E4	R7	B5	R25	F2	R43	C4	T2	D4
C2	C4	C20	E2	CR1	D2	Q3	E5	R8	E4	R26	F2	R44	A4	TP1	A5
C3	B2	C21	F4	CR2	F2	Q4	F2	R9	E5	R27	F2	R45	A4	TP2	C3
C4	C3	C22	F4	CR3	A4	Q5	F3	R10	E5	R28	F2	R46	A3	TP3	A2
C5	E2	C23	E4	CR4	B4	Q6	G3	R11	E4	R29	F3	R47	A4	TP4	A2
C6	E2	C24	C4	CR5	B4	Q7	F3	R12	E4	R30	F2	R48	A3	TP5	B2
C7	D2	C25	B4	CR6	A4	Q8	F3	R13	E4	R31	F3	R49	A2	TP6	B3
C8	D2	C26	A4	CR7	D3	Q9	B4	R14	E4	R32	G2	R50	A2	TP7	C3
C9	E5	C27	B4	CR8	A4	Q10	A2	R15	E4	R33	F3	R51	A3	TP8	D2
C10	E5	C28	A3	CR9	A3	Q11	A2	R16	F2	R34	F3	R52	B2	TP9	F3
C11	E5	C29	A3	L1	E3	Q12	A3	R17	F2	R35	E3	R53	B2	TP10	F2
C12	E4	C30	B3	L2	F4	Q13	A3	R18	G2	R36	F3	R54	A2	TP11	F2
C13	F1	C31	A3	L3	B5	R1	C2	R19	F2	R37	E3	R55	A2	TP12	E3
C14	G2	C32	A3	L4	D3	R2	C3	R20	F2	R38	F4	R56	A2	U1	E4
C15	G2	C33	B3	L5	A2	R3	C3	R21	G2	R39	F4	R57	A3	U2	F3
C16	G1	C34	B2	MP1	B4	R4	B4	R22	F2	R40	F4	R58	A3	U3	F2
C17	B3	C35	A2	MP2	G4	R5	D3	R23	G2	R41	F4	R59	A2	U4	F2
C18	G3	C36	B2	Q1	C2	R6	D3	R24	F2	R42	E3	R60	A4	U5	B3
												R61	B2	U6	C3
												T1	C4	VR1	C3
														VR2	C3

Figure 8-9. Service Sheet 3, Display Driver Assembly A3 (Sheet 1 of 2)


HORIZONTAL DEFLECTION CIRCUIT
P/O L1
190
0.4
HORIZONTAL YOKE
P/O A1
P/O XA3
P/O P3
P/O P1
A3 DISPLAY DRIVER ASSY (01611-66503)
+12V
+5V
+12V
+12V
P/O P1
R1 432
VR1 5.11V
C1 .01UF
R2 10K
U5
U6
TP6
HHSV
TP7
C2 240
T1
VR2 43.2V
C3 471IF
TP8
C5 47UF
C4 60UF
R3 10
L1 2.5mH
Q1
CR1
C6 10UF
C7 .022UF
C8 5UF
R4 15
R5 100
R6 50
H SIZE
TP12 GND
C9 1UF
Q2
Q3
C11 1UF
C10 1UF
U1
R7 1000
R8 47.5K
R9 47.5K
R13 2000
R10 47.5K
R11 47.5K
C12 1UF
R14 5000
HORIZ. POS
R12 2000
R15 2000
CR7
L4 0.6
TP1
+35V
T2
C28 22UF
C29 .01UF
C30 .01UF
C31 .01UF
C32 .01UF
C33 .01UF
CR6
+500V
CR8
-50V
FOCUS
R46 100K
R45 1M
R60 1M
INT
R44 100K
C26 47UF
+12V
C25 47UF
L3 700
C27 8200
C24 60UF
R43 10
Q9
CR4
+10KV
R47 909K
HIGH VOLTAGE CIRCUIT
CR5
+275V
TP2
R48 909K
+100V
-12V
+12V
R18 200K
CW
V SIZE
R17 909K
R19 162K
R20 51.1
TP11
R16 4750
C13 6.8UF
Q4
U4
C14 0.68
R22 162K
CR2
R21 4750
C15 0.68
R23 5000
LIN
HVSY
V1
+10KV
CR1
W2
W4
P/O A1
P/O P4
R1 68
+5V
-12V
P/O XA3
P/O P1
+5V
VIDEO
-12V



PARTS ON THIS SCHEMATIC

A1	A3	CHASSIS
R1	C1-37 CR1-9 L1-5 P1 Q1-13 R1-61 T1,2 U1-6 VR1, 2	CR1 L1 V1 W2,4

Figure 8-9. Service Sheet 3, Display Driver Assembly A3 (Sheet 2 of 2)

SERVICE SHEET 4

PRINCIPLES OF OPERATION. (Also refer to keyboard scanner circuit description on Service Sheet 5.)

KEYBOARD. The 1611A keyboard contains 39 switches wired in a matrix of 8 rows by 6 columns. Each switch has two, one-turn coils wrapped around a core. When a key is not pressed, the magnet is held so that its field permeates the core, saturating it completely; thus, there is very little coupling between coils. If the key is pressed, the magnet is released and the core and windings act as a transformer.

The primary (scan) windings of the switches are wired together in eight rows. All windings in each row are connected in series between R1/C3 and the buffered outputs of BCD-To-Decimal decoder U1. The secondary (sense) windings are wired together in 6 columns. All windings in each column are connected in series between ground and key-sense lines KS0-KS4, and KS7. The key-sense lines go to the Keyboard Scanner circuit on A5 (Service Sheet 5). Three separate ground paths are provided to switch columns for isolation between column grounds.

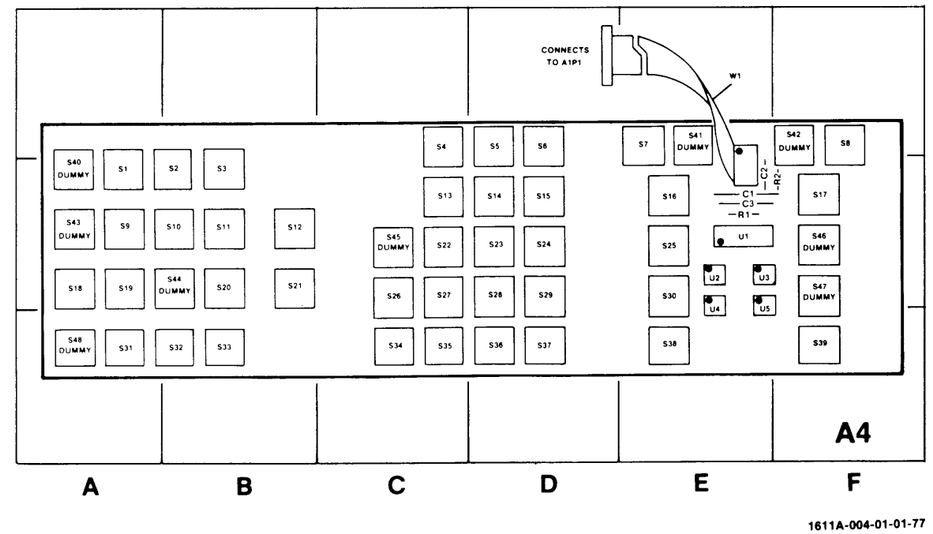
The rows of switches are scanned by U1. The outputs of U1 are buffered by U2-U5 to increase their current sink capability. The BCD inputs of U1 are driven by SCAN A-C from the three LSB outputs of the Keyscan Counter on A5. SCAN D functions as an enable for U1. Each time SCAN D goes low, SCAN A, B, and C are interpreted as a count, driving the selected output of U1 low.

When an output of U1 goes low, C3 is discharged through the row of switches connected to that output. This provides a sharp current pulse through the primary winding of each switch. Since the discharge rate of C3 is limited only by inductance of the switches, a pulse width of approx 100 ns is obtained. If a key in a row is pressed when that row is excited, a pulse is generated on the key-sense line for that column due to coupling between the primary and secondary windings in the switch. This pulse is routed to the Keyboard Scanner circuit on A5.

TROUBLESHOOTING

If the 1611A does not respond to a key or group of keys, check the junction of A4R1 and A4C1 for the proper waveform (shown on schematic). Adjust the oscilloscope to observe at least eight cycles. If a pulse is missing, a key may be open or one output of U2 through U5 may not be driving a row of switches. If no pulses are detected at the junction of R1/C3, and the inputs of U2 through U5 are being driven, one of the outputs of U2 through U5 is shorted. Disconnect A4W1 from Main Board A1 and use a current tracer and logic pulser to detect the shorted output.

If the waveform at R1/C3 is correct, check the output voltage of the keysense lines; It should be from 1 to 2 volts when a key is depressed. If there is no output voltage, a key switch in the monitored column is faulty.



1611A-004-01-01-77

REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC
C1	E-2	S8	F-3	S20	B-2	S32	B-1	S44	B-2
C2	E-2	S9	A-2	S21	B-2	S33	B-1	S45	C-2
C3	E-2	S10	B-2	S22	C-2	S34	C-1	S46	F-2
R1	E-2	S11	B-2	S23	D-2	S35	C-1	S47	F-2
R2	F-2	S12	B-2	S24	D-2	S36	D-1	S48	A-1
S1	A-2	S13	C-2	S25	E-2	S37	D-1	U1	E-2
S2	B-2	S14	D-2	S26	C-2	S38	E-1	U2	E-2
S3	B-2	S15	D-2	S27	C-2	S39	F-1	U3	E-2
S4	C-3	S16	E-2	S28	D-2	S40	A-2	U4	E-2
S5	D-3	S17	F-2	S29	D-2	S41	E-3	U5	E-2
S6	D-3	S18	A-2	S30	E-2	S42	F-3	W1	E-3
S7	E-3	S19	A-2	S31	A-1	S43	A-2		

Keyboard A4 Component Locator
(01611-66504)

Figure 8-10. Service Sheet 4, Keyboard Assembly A4 (Sheet 1 of 2)

A4 KEYBOARD (01611-66504)

COLUMN → 0 1 2

ROW

R2 270 +5V DS1 ON

FROM A5 5 — POW1 7 8 9 10 — SCAN A SCAN B SCAN C SCAN D

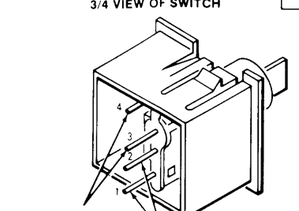
FROM A2 2 — 6 11 — +5V — C2 .01UF C1 22UF

U1 BCD TO DECIMAL DECODER — D C B A — NC NC

U2 U3 U4 U5 +5V

ROW	0	1	2
0	S34 0 X00*	S23 8 X10	S26 DON'T CARE X20
1	S35 1 X01	S24 9 X11	
2	S36 2 X02	S13 A X12	
3	S37 3 X03	S14 B X13	S8 ABSOL MNEM X23
4	S27 4 X04	S15 C X14	
5	S28 5 X05	S4 D X15	S17 ROLL ▲ X25
6	S29 6 X06	S5 E X16	S39 ROLL ▼ X26
7	S22 7 X07	S6 F X17	

3/4 VIEW OF SWITCH



SECONDARY (COLUMNS CONNECTED IN SERIES TO OUTPUT PINS)

PRIMARY (ROWS CONNECTED TO U1 IN SERIES)

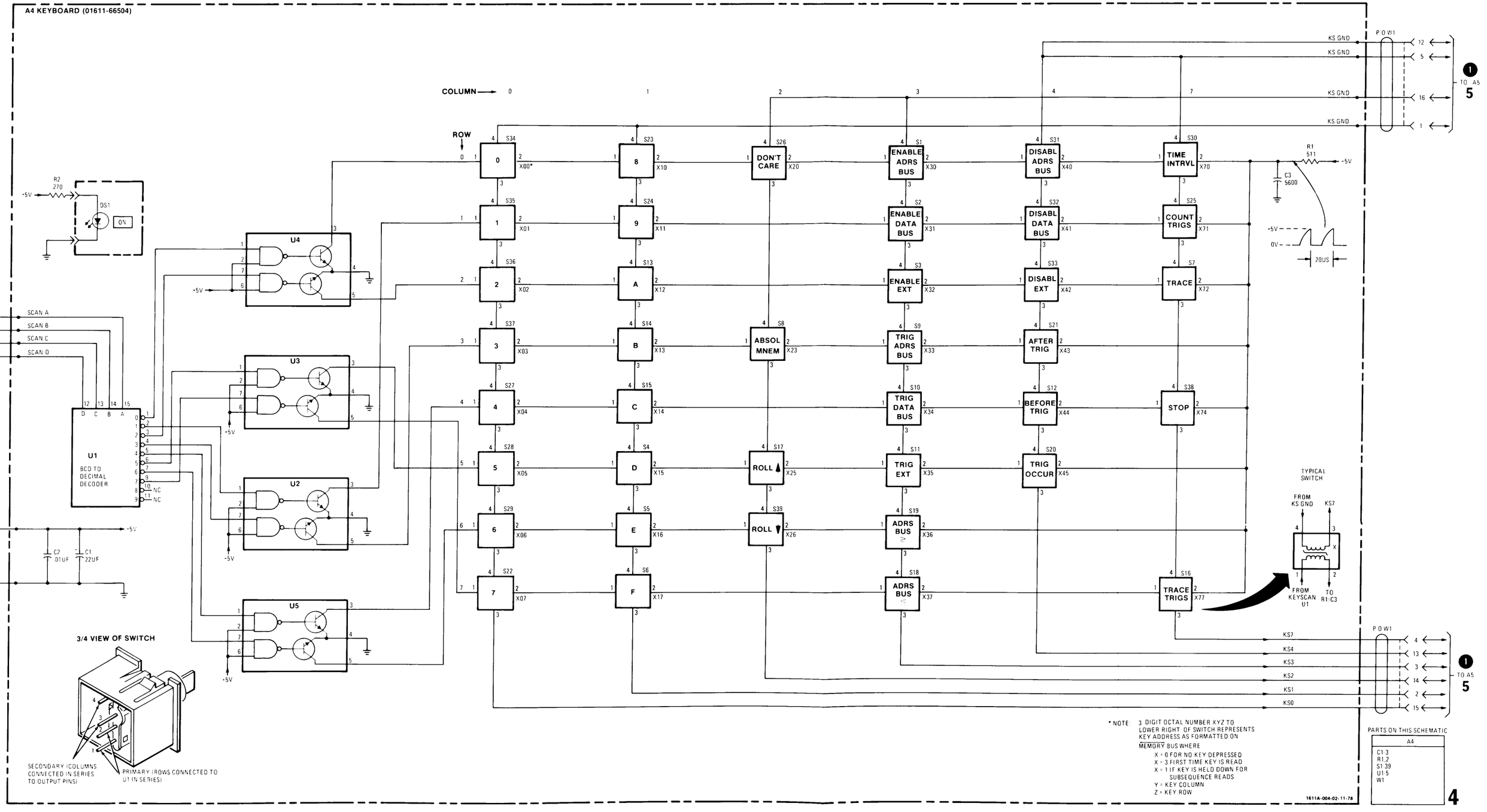


Figure 8-10. Service Sheet 4, Keyboard Assembly A4 (Sheet 2 of 2)

SERVICE SHEET 5

PRINCIPLES OF OPERATION

MICROPROCESSOR AND I/O. 8080 Microprocessor U11 is an N-channel MOS device with a separate 16-line address bus and an 8-line bidirectional data bus. The microprocessor monitors both keyboard and personality panel switches and configures the 1611A circuits for selected operating modes and measurements. The microprocessor controls all data acquisition and data manipulation in the 1611A. In addition, it provides diagnostic routines for self-test, and generates error and status messages.

The data bus on the microprocessor chip is the only bidirectional bus in the 1611A. During microprocessor read operations, DBIN (U11, pin 17) enables NAND gates U8/U9. This routes all data on the MEMORY bus through to pins D0-D7 of the microprocessor. During microprocessor write operations, DBIN enables AND gates U10/U20. U10/U20 transfer data on pins D0-D7 of the microprocessor to the μP DATA bus (P1, pins 68-75). NAND gates U8/U9 are open collector devices which present a high impedance to microprocessor data lines during write operations.

Buffers U12/U21 and AND gates U2A/B/C buffer the microprocessor address bus to increase the limited drive capability of the MOS microprocessor. The μP ADDRESS bus accesses ROM (ROM Board A10) and RAM (Service Sheet 6). It also controls most hardware in the instrument.

Microprocessor Power-up Circuit. C3, R6/R7, and NAND gate U14C form the power-up circuit that resets the microprocessor to its startup routine at instrument turn on. The output of U14C holds the RESET pin of the microprocessor high for a time interval determined by RC network C3/R6/R7. The microprocessor program counter is cleared during this time. When RESET goes low, the microprocessor starts at location 0 in memory.

TIMING GENERATOR. System timing signals for the 1611A are provided by the Timing Generator. The Timing Generator consists of 10-MHz crystal Y1, decade counter U23, hex "D" latch U22, and associated gating.

The 10-MHz cystal oscillator drives decade counter U23. U23 divides the 10-MHz signal to 1 MHz (1 μs CK) and 5 MHz (200 ns CK). The 1 μs CK is used as the time base for 1611A timing measurements and as the clock for the probe Test Generator on A9. 200 ns CK is routed to the display generator circuit on A6 and to Hex "D" latch U22.

U22 is wired as a six-bit shift register. Eight-input NAND gate U13 provides a low to the first stage of the shift register only when outputs of the first five stages are high. Therefore only one bit of the six-bit shift register can be low at any time. Thus, the shift register divides 200 ns CK by six and yields 833-kHz outputs. U22 and RS latch U14A/B provide the two-phase, non-overlapping clock for the microprocessor (ϕ1 and ϕ2), and other system timing signals required by the instrument. (see timing diagram on this service sheet.)

KEYBOARD SCANNER

Keyboard Scan. Keyboard scanning is accomplished by six-bit Keyscan Counter U17B/U17A/U7A, which is driven by 4-bit binary counter U7B. U7B divides the 833-kHz system clock down to 52 kHz. The three LSB's from the Keyscan Counter address the switch rows on the keyboard through BCD-to-decimal decoder A4U1 (Service Sheet 4). The three MSB's from the counter address the switch columns through 8-to-1 data selector U5. Thus the counter points to one column of switches and scans each switch in the column, then points to the next column of switches and scans each switch in that column. In this manner the Keyscan Counter repetitively scans the keyboard until a depressed key is sensed.

Key Sense. Operation of the keysense circuit is best explained by the following example: Assume the D key is pressed; keycode for D is 15 (octal). Thus, the switch is in row 5 of column 1 on the keyboard matrix (see Service Sheet 4). When the keyscan count reaches 001 101 (octal 15), data selector U5 is pointing to KS 1 (D1 input) and row 5 of the matrix is excited. Since D is held down, a pulse is generated on KS1 and applied to the base of U15Q2 (pin 6). Transistor arrays U15 and U16 form a differential amplifier The bases of Q4 in both arrays are connected in parallel. Base voltage of each transistor is determined by a voltage divider network consisting of a 200Ω resistor (P/O U27), three 6800Ω resistors (P/O U26), and R14. The voltage divider maintains the bases of the two transistors at +0.7 V. Therefore, the pulse (>+0.7 V) on KS1 turns U15Q2 on, forcing the D1 input of U5 low. Since the keyscan counter is pointing to the D1 input of U5, the W output goes high, triggering monostable U6. U6 clocks the Q output of D flip-flop U1A high and places the first stage of the keyscan counter in its hold state. This locks the counter at state 15 and clears D flip-flop U1B. The counter remains locked as long as D is depressed because the monostable is re-triggered each time SCAN D occurs and not allowed to time out.

The Keyscan Count (key code) is routed to the six LSB of the MEMORY bus (M0-M5) through quad 2-to-1 data selectors U18/U19. The two MSB's of MEMORY bus (M6, M7) come from monostable U6 and D flip-flop U1A. The first time the microprocessor reads the keyboard, both lines are high. The microprocessor sees 315_8 on its data bus, indicating that key D is being read for the first time. At the end of the first read, the positive-going edge on the select line of U18/U19 clears U1A by clocking U1B. Thus, on subsequent reads, the microprocessor sees 115_8 on its data bus. The 1 in the MSD indicates that the information has been read but the key is still depressed. This condition is held until the D key is released. The monostable then times out and unlocks the counter.

The counter then continues to scan the keyboard until another depressed key is sensed. When the counter is scanning, a 0 in the MSD of the keycode indicates to the microprocessor that no key is depressed.

Data selectors U18/U19 are enabled during a microprocessor read operation by A14 (U11, pin 39). The data selectors select either the keyboard or the switch lines (SW0-SW7) from personality panel A11 under control of A15 (U11, pin 36).

TROUBLESHOOTING

Most failures on the A5 assembly result in a faulty display at turn-on. The troubleshooting tree in figure 8-4 should be used to isolate problems affecting the display.

The keyboard and personality panel can cause problems that will not be seen until the power-up routine is completed. If the 1611A fails to respond to personality panel switches, check the switches as follows: Toggle the HEXADECIMAL/OCTAL format switch between both positions and verify that A5U18 pin 3 changes levels. Toggle the TEST MODE switch while monitoring A5U19 pin 10. Verify that the signal changes levels. Also check A5U19 pin 15 for a low pulse. If the pulse is not present, check A5U4 and A5U2. Check A5U19 pin 1 for presence of a toggling signal. This signal determines whether the microprocessor reads data from the personality panel or the keyboard. If inputs are correct and the gating signal (U18/19 pin 15) and select signal (U18/19 pin 1) are present, U18 or U19 is bad.

If the 1611A does not respond to the keyboard or responds incorrectly, check U19 pins 1 and 15 as done for the personality panel switches. Verify that U6 pin 8 is high only when a key is depressed. Verify that the outputs of U17 and U7 do not toggle while U6 pin 8 is high. If the instrument does not respond to a key, check TP1 for presence of a clocking signal to U6. Check for a pulse at one of the inputs of U5. If no pulse is present, check keysense lines KS0-4 and KS7. A pulse with amplitude of more than one volt indicates that a key is depressed.

Incorrect key codes can be checked by pressing a key while monitoring the outputs of keyscan counter U17/U7 with a logic analyzer. The codes of each key is shown on the keyboard schematic (see Service Sheet 4). Incorrect codes can result from U5 selecting the wrong keysense line or from a fault on the keyboard. If all signals from the Keyboard Scanner are correct, replace U18 or U19.

DATA SELECTOR U5 TRUTH TABLE

INPUTS				OUTPUTS	
SELECT			STROBE		
C	B	A	S	Y	W
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

BINARY COUNTER U7 TRUTH TABLE

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_Q
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

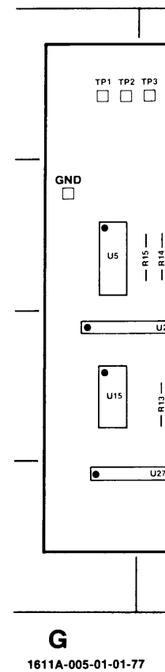
DATA SELECTORS U18/U19 TRUTH TABLE

INPUTS				OUTPUT Y
OUTPUT CONTROL	SELECT	A	B	
H	X	X	X	Z
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

Z=high impedance (off)

μP HARDWARE ADDRESSES

ADDRESS	FUNCTION
075300_8	Reads position of personality panel switches
175700_8	Reads keyboard



G
1611A-005-01-01-77

REF DESIG	GRID LOC
C1	B-4
C2	B-4
C3	A-2
C4	C-4
C5	F-3
C6	C-4
C7	E-3
C8	C-2
C9	B-2
C10	F-1
R1	E-3
R2	C-4
R3	C-4
R4	C-2
R5	C-3
R6	A-3
R7	B-3
R8	A-2
R9	B-4
R10	B-4
R11	B-4

MONOSTABL
T = 0.4 RC

DECADE COU
COUNT E
TC = CET
PRESET =
RESET = $\overline{1}$

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the select line of U18/U19 clears U1A by clocking U1B. Thus, on subsequent reads, the microprocessor sees 1158 on its data bus. The 1 in the MSD indicates that the information has been read but the key is still depressed. This condition is held until the D key is released. The monostable then times out and unlocks the counter.

The counter then continues to scan the keyboard until another depressed key is sensed. When the counter is scanning, a 0 in the MSD of the keycode indicates to the microprocessor that no key is depressed.

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L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

BINARY COUNTER U7 TRUTH TABLE

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_Q
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

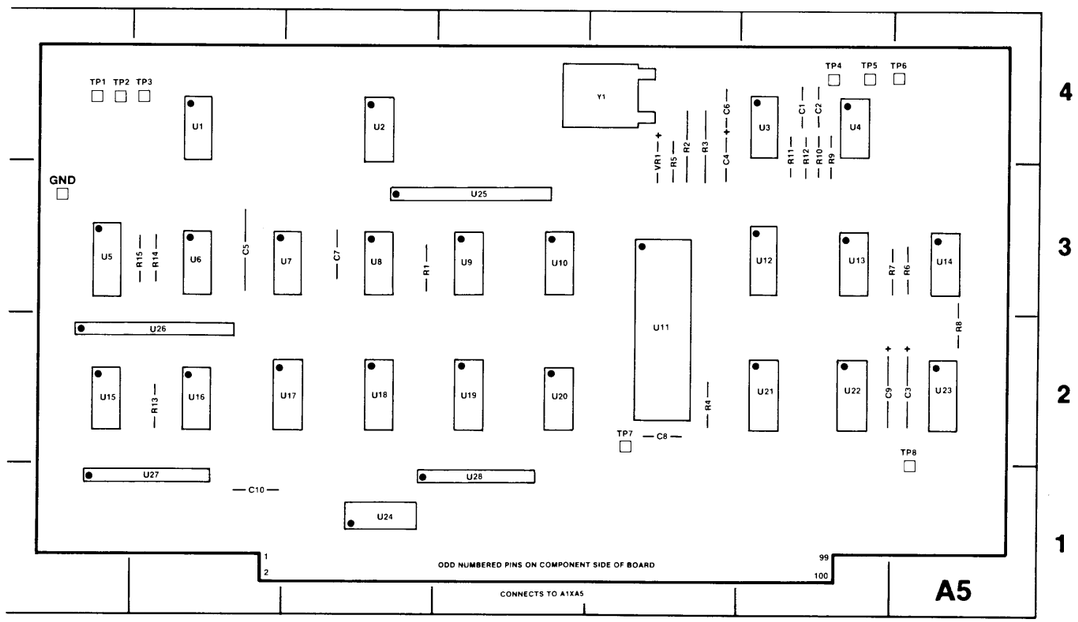
DATA SELECTORS U18/U19 TRUTH TABLE

INPUTS				OUTPUT Y
OUTPUT CONTROL	SELECT	A	B	
H	X	X	X	Z
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

Z=high impedance (off)

μP HARDWARE ADDRESSES

ADDRESS	FUNCTION
075300_8	Reads position of personality panel switches
175700_8	Reads keyboard



1611A-005-01-01-77

Microprocessor Board A5 Component Locator
(01611-66505)

1611A-005-01-03-78

REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC
C1	B-4	R12	B-4	U9	D-3
C2	B-4	R13	F-2	U10	D-3
C3	A-2	R14	F-3	U11	C-2
C4	C-4	R15	F-3	U12	B-3
C5	F-3	TP1	G-4	U13	B-3
C6	C-4	TP2	G-4	U14	A-3
C7	E-3	TP3	F-4	U15	G-2
C8	C-2	TP4	B-4	U16	F-2
C9	B-2	TP5	B-4	U17	E-2
C10	F-1	TP6	A-4	U18	E-2
R1	E-3	TP7	C-2	U19	D-2
R2	C-4	TP8	A-2	U20	D-2
R3	C-4	TP9	G-3	U21	B-2
R4	C-2	U1	F-4	U22	B-2
R5	C-3	U2	E-4	U23	A-2
R6	A-3	U3	B-4	U24	E-1
R7	B-3	U4	B-4	U25	D-3
R8	A-2	U5	G-3	U26	F-2
R9	B-4	U6	F-3	U27	F-1
R10	B-4	U7	E-3	U28	D-1
R11	B-4	U8	E-3	VR1	C-3
				Y1	C-4

MONOSTABLE U6 TIMING EQUATION

$T = 0.4\ RC$ where R is in kΩ
C is in pF
T is in ns

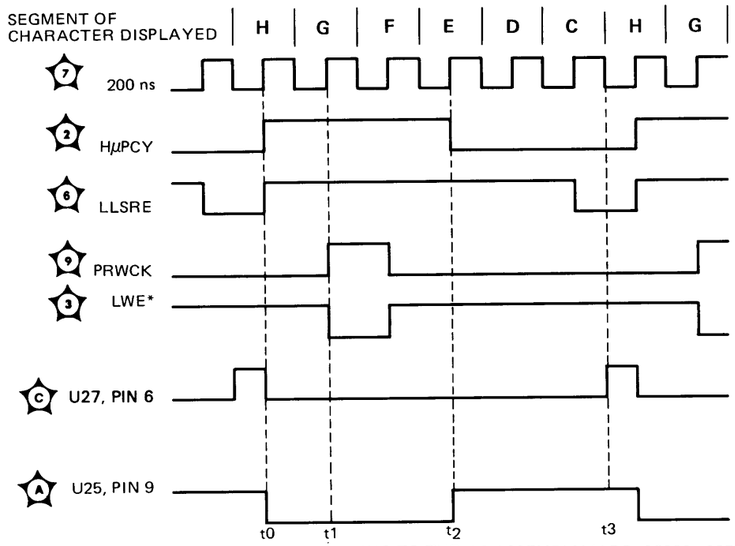
DECADE COUNTER U23 COUNT EQUATION

$\text{COUNT ENABLE} = \overline{CEP} \bullet CET \bullet \overline{PE}$
$TC = CET \bullet Q0 \bullet \overline{Q1} \bullet \overline{Q2} \bullet Q3$
$\text{PRESET} = \overline{PE} \bullet CP+$
$\text{RESET} = \overline{MR}$

ICs ON THIS SCHEMATIC

IC REF DES	HP PART NO.	MFR PART NO.
U1	1820-1112	SN74LS74N
U2, 10, 20	1820-1201	SN74LS08N
U3	1820-1199	SN74LS04N
U4	1820-0471	SN7406N
U5	1820-1217	SN74LS151N
U6	1820-1422	SN74LS122N
U7	1820-1464	SN7393N
U8, 9	1820-1198	SN74LS03N
U11	1820-1783	8080AP
U12, 21	1820-1491	SN74LS367N
U13	1820-1207	SN74LS30N
U14	1820-1425	SN74LS132N
U15, 16	1821-0001	CA3046
U17	1820-1282	SN74LS109N
U18, 19	1820-1439	SN74LS258N
U22	1820-1196	SN74LS174N
U23	1820-1429	SN74LS160N
U24	1810-0283	1810-0283
U25, 26	1810-0049	1810-0049
U27	1810-0163	1810-0163
U28	1810-0121	1810-0121

Figure 8-11. Service Sheet 5, Microprocessor and Key Board Scan Assembly A5 (Sheet 1 of 2)



*ONLY WHEN 8080A ON A5 IS WRITING TO THE A6 ASSEMBLY (ADD=32000$_8$-32777$_8$)

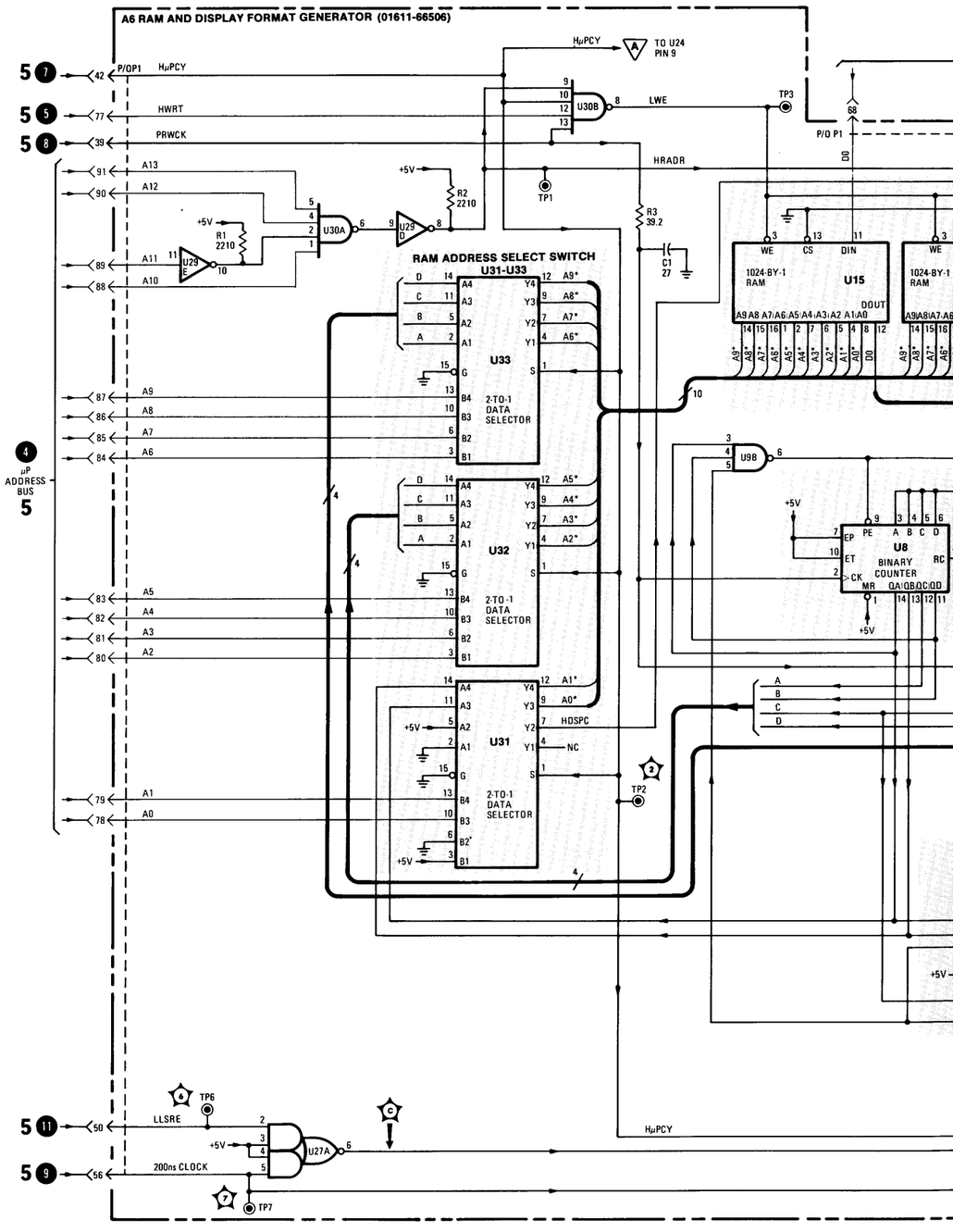
t_0 - CHARACTER ROW SELECT, BLANKING, BLINKING, INVERSE VIDEO AND CHARACTER ARE CLOCKED INTO U1 AND U24 FOR CHARACTER BEING DISPLAYED.

t_1 - COUNTERS FOR DISPLAY ADDRESS ARE CLOCKED.

t_2 - DATA FROM RAM IS LATCHED INTO U25 AND U28 IF INTERNAL μP IS ADDRESSING A6.

t_3 - BLANKING AND CLOCK INHIBIT (U14) SIGNALS ARE LATCHED INTO U4 FOR NEXT CHARACTER. DISPLAY DATA FROM CHARACTER ROM IS LOADED INTO SHIFT REGISTER U14.

A6 Timing Diagram



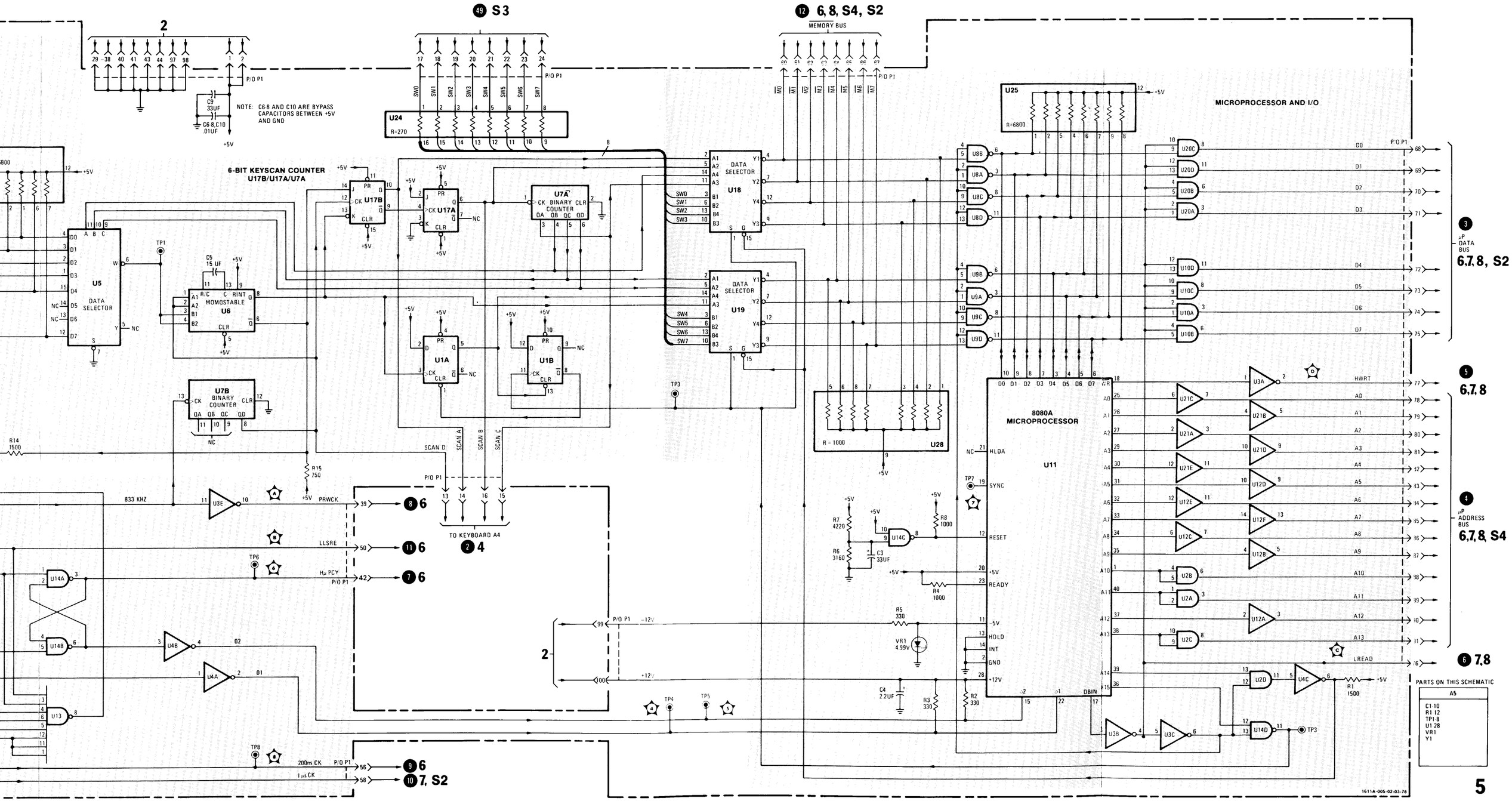
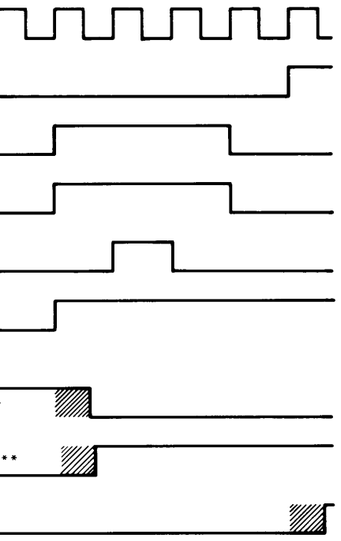
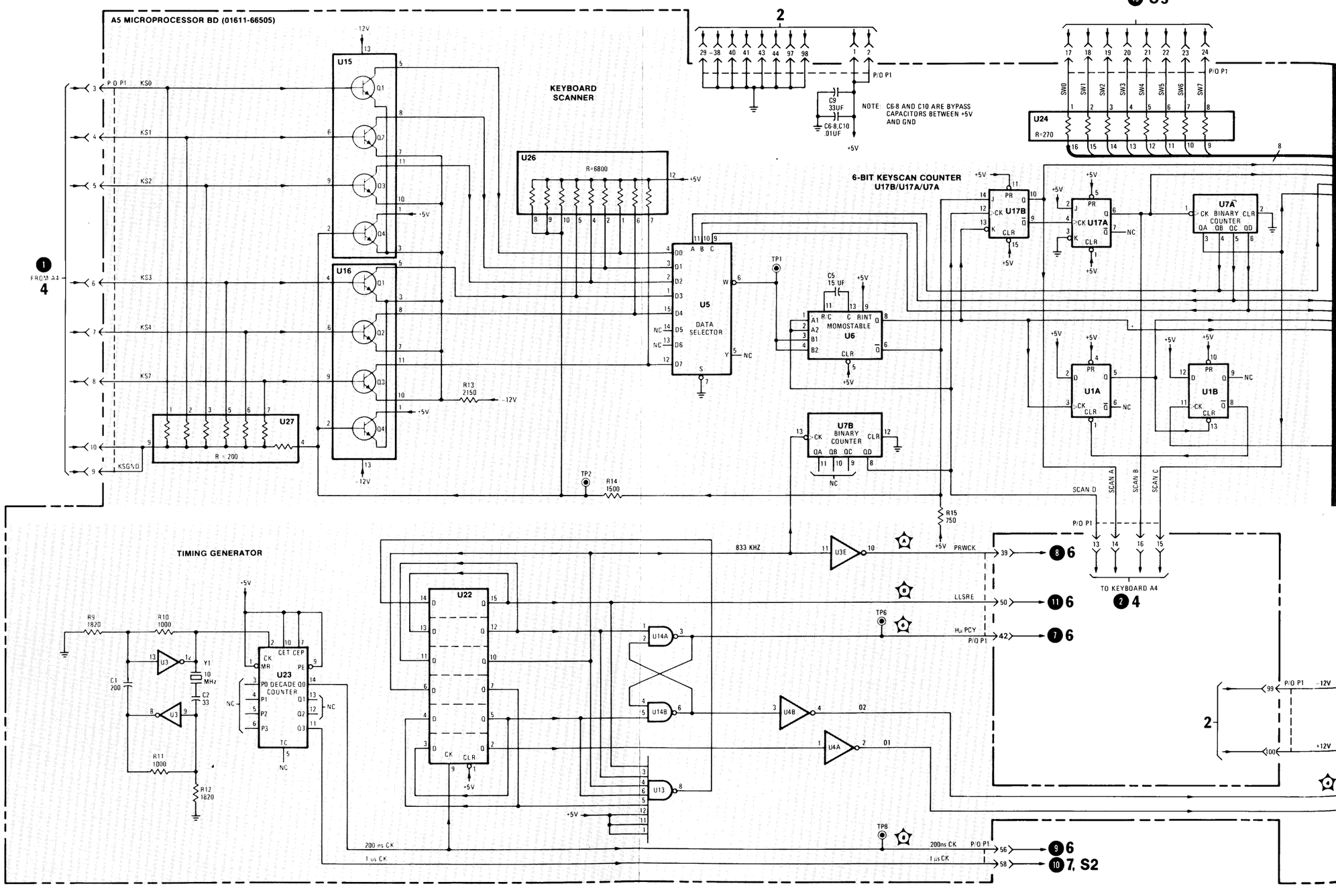


Figure 8-11. Service Sheet 5, Microprocessor and Keyboard Scan Assembly A5 (Sheet 2 of 2)



D BY A5U11 (8080A) AND ARE
RELATIONSHIP BETWEEN
ONLY WHEN SIGNAL IS TRUE.

A MICROPROCESSOR STATES.



SERVICE SHEET 6

PRINCIPLES OF OPERATION

RAM and Display Format Generator Assembly A6 consists of several circuits. 1k-by-1 RAMs U15 through U22 form a 1k-by-8 random access memory. This memory stores display information for the Character Generator and provides temporary data storage for μP A5U11. The RAM is time shared between the μP and the Character Generator. This is accomplished with RAM Address Select Switch U31-33. U31-33 are quad 2 line-to-1 line data selectors that form a 10-pole, two-position switch. The switch toggles between the μP ADDRESS Bus and the output of the counter chain. The counter chain is made up of Display Column Counter U8/U7, Character Line Counter U6, and Display Line Counter U11/U12. The switch is controlled by HμPCY.

The CRT displays 24 lines of 32 characters. Each character is displayed as a 10-by-6 dot matrix. The display has a horizontal raster scan with 240 scan lines (24 lines of characters X 10 lines per character). Each character displayed on the CRT corresponds to an address in RAM. The upper left character is stored in location 0. This character location corresponds with a display column count of 0 and a display line count of 0. The character next to the upper left character horizontally is stored in location 1 in RAM. The upper-right character is stored in location 31; the second line of characters correspond with addresses 32 through 63 in RAM, etc. The lower right character corresponds to address 767_{10} in RAM. Address 767_{10} is read when the display column count equals 31 and the display line count equals 23. Character Line Counter U6 determines which of the ten lines of a character is being written on the CRT screen by the Character Generator.

The Character Generator provides the video signal for Display Driver Assembly A3. The Character Generator consists of 64-by-8-by-5 character generator ROM U13, 8-bit shift register U14, AOI U3, and data Latches U1, U4, and U24. The Horizontal and Vertical Sync Generators synchronize the raster scan with the displayed data. The 2-Hz clock generator blinks the display and drives the probe test generator on personality board A9.

RAM. The 1024-by-8 RAM is controlled by the μP when HμPCY is high. When the μP is addressing RAM (HRADR=1), NAND gate U30B and data latches U25 and U28A/B are enabled. When the μP is writing to RAM (HWRT=1), U30B pulls the WE lines on the RAMs low, writing information on the μP DATA Bus into RAM. During μP read operations, the data outputs from RAM are latched into data latches U25 and U28A/B on the positive-going edge of HDSPC (complement of HμPCY). Outputs of the latches are applied to the $\overline{\text{MEMORY}}$ bus through open-collector buffers U26 and U29. If the μP is not addressing RAM (HRADR=0), write gate U30B is disabled and the data latches are held in the clear state. This prevents the open collector buffer outputs from driving the $\overline{\text{MEMORY}}$ bus.

During the time that HμPCY is low, RAM is addressed by the five LSBs of the Display Column Counter and the five LSBs of the Display Line Counter. The Character Generator reads from RAM the character code for the character to be displayed. The information is latched in data latches U1 and U24 on the positive-going edge of HμPCY. D0 through D5 from RAM provides the character code. D6 determines whether the character is displayed in inverse video (D6=1) or normal video (D6=0). D7 determines whether or not the character is blinked on the display.

DISPLAY COLUMN COUNTER AND HORIZONTAL SYNC GENERATOR. Six-bit Display Column Counter U8/U7 keeps track of which of the 32 characters on the displayed line is being addressed. In addition to supplying the five LSB's of RAM address, the counter also controls horizontal blanking and the Horizontal Sync Generator.

When Display Column Counter MSB (U7, pin 13) goes high on count 32, the condition is latched in U4. This pulls pin 1 of AOI U3 high (HHBLK=1). HHBLK forces the video signal to the Display Driver Assembly high, blanking the CRT. At count 35, the Horizontal Sync Generator is set. This generates HHSY which initiates horizontal retrace. The counter continues to count up to 41. The additional time is required by the CRT for retrace. At count 41, the counter is reset through U9B and the Character Line Counter is incremented. The Display Column Counter starts over and a new trace is initiated. At count 16, the Horizontal Sync Generator is reset. This forces HHSY low, completing the cycle.

CHARACTER LINE COUNTER. Character Line Counter U6 keeps track of which of the 10 lines in the 10-by-6 dot character is being written on the display. The three LSB's of the counter output address the three line select inputs (A1-A3) of character generator U13 through data latch U1. The MSB of the counter output blanks lines 8 and 9 of the character dot matrix to provide spacing between lines of characters on the display. The MSB output also increments the Display Line Counter when the tenth line of a character is written on the display.

DISPLAY LINE COUNTER AND VERTICAL SYNC GENERATOR. 5-bit Display Line Counter U11/U12 keeps track of which of the 24 rows of characters on the display is being addressed. It supplies the five MSB's of RAM address and controls vertical blanking and the Vertical Sync Generator.

When the display line count reaches 24, the condition is detected by NAND gate U10B and latched in U4 through U1 and U2F. This places HVBLK in the high state. HVBLK forces VIDEO high through AOI U3, blanking the CRT. At a count of 25, the Vertical Sync Generator is set by the QC output of U6, the LSB of the Display Line Counter, and HVBLK. This sets HVSY high for 0.5 milliseconds, initiating vertical retrace. During vertical retrace, the count of 25 is detected by NAND gate U10C. U10C then resets the Display Line Counter to 0.

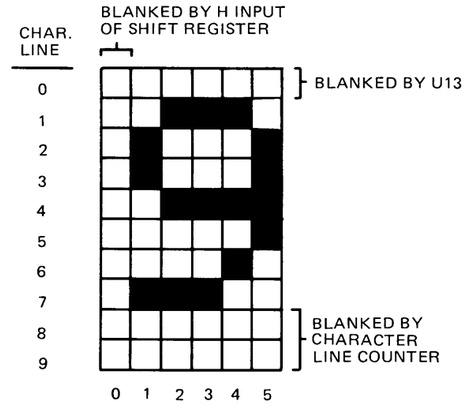
CHARACTER GENERATOR. The Character Generator consists of character generator ROM U13, 8-bit shift register U14, AOI U3, and data latches U1/U4/U24. The data latches store information needed by the character generator to display each character. U1 stores the three LSB's of character line count, vertical and character-line blanking information, and inverse video field information (D6 From RAM). U4 stores blanking and inverse video information from U1 and the horizontal blanking signal from the Display Column Counter. U24 stores the six-bit character code from RAM.

U13 is a 64-by-8-by-5 character generator ROM. It is capable of generating the 64 characters in the modified ASCII set. Each ROM character is an 8-by-5 dot matrix. The actual displayed character is a 10-by-6 matrix. The first line of each character is always blanked by U13. The last two lines of each character are blanked by Character Line Counter U6. The first column of each character is blanked by the H input of shift register U14 (see character dot-matrix on this Service Sheet).

Input A4 through A9 of U13 provide the 6-bit character code that tells U13 which character to output. Inputs A1 through A3 determine which line of the character is generated. A1 through A3 are addressed by the stored character line count from U1. The code for each line of a character is output to inputs G through C of shift register U14 in parallel format. The shift register outputs the character code in serial format in sequence H through C.

The output code for the number 9 shown in the matrix illustration is as follows:

CHARACTER LINE NO.	U13 CODE OUTPUT 05	04	03	02	01
0	0	0	0	0	0
1	0	1	1	1	0
2	1	0	0	0	1
3	1	0	0	0	1
4	0	1	1	1	1
5	0	0	0	0	1
6	0	0	0	1	0
7	1	1	1	0	0



Character Dot Matrix (9)

On the negative-going edge of the first 200 ns CLK after LLSRE goes low, the shift register is parallel loaded from the character generator. The H output of the shift register is immediately presented at the output. Since H is tied to ground, the first dot in each character line is blanked. This provides the horizontal spacing between characters of the display. On the next clock, the shift register starts outputting the code in serial format beginning with G. After inputs G through C are shifted out, LLSRE loads the shift register with the code for the same character line of the next character in the display line. The character Generator writes line 0 of all 32 characters in a display line, then horizontal retrace occurs. The Character Generator then writes line 1 of all 32 characters in the display line, and so forth until line 7 of all 32 characters has been written on the display. At this point, the Character Line Counter is incremented to eight, inhibiting the shift register for two scan lines. This generates two blank lines on the display. The two blank lines provide the vertical spacing between characters on the CRT screen.

AOI U3 controls normal and inverse video, vertical blanking, and horizontal blanking. When normal video is displayed, HNORM enables U3 to Gate the $\overline{\text{H}}$ output of U14 through to Display Driver Assembly A3. When inverse video is displayed, U3 gates the H output of U14 through to A3. In this manner, VIDEO is inverted when inverse video is selected. AOI U3 blanks the display any time HVBLK or HHBLK is true.

Blinking characters are generated by alternately displaying the character in normal video for 32 scans, then blanking the character for 32 scans. This is accomplished by gating the blinking signal (D7) with the 2 Hz clock through U27B and U4. When the 2 Hz clock signal is low, D7 inhibits U14 from shifting. This results in the character being blanked.

Relative timing between events on the A6 assembly is shown in the timing diagram on this service sheet.

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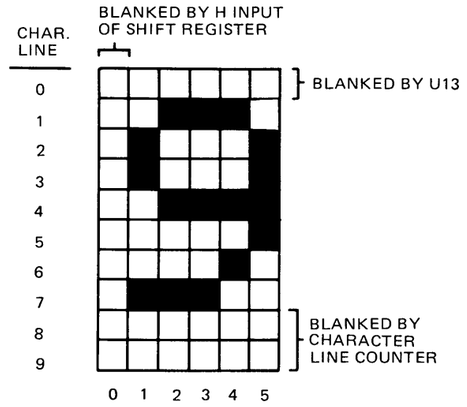
1	0	1	1	1	0
2	1	0	0	0	1
3	1	0	0	0	1
4	0	1	1	1	1
5	0	0	0	0	1
6	0	0	0	1	0
7	1	1	1	0	0



Character Dot Matrix (9)

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Blinking characters are generated by alternately displaying the character in normal video for 32 scans, then blanking the character for 32 scans. This is accomplished by gating the blinking signal (D7) with the 2 Hz clock through U27B and U4. When the 2 Hz clock signal is low, D7 inhibits U14 from shifting. This results in the character being blanked.

Relative timing between events on the A6 assembly is shown in the timing diagram on this service sheet.

TROUBLESHOOTING

Most problems on the A6 assembly can be isolated using the troubleshooting tree in figure 8-4. Horizontal and vertical sync problems can be found using a logic state analyzer.

VERTICAL SYNC PROBLEMS. Using A6U8 pin 2 as a clock, monitor Display Column Counter A6U7/U8 with a logic state analyzer. The counter should count from 0 to 41 and then start at zero again. If the count is correct, the vertical sync problem is caused by A6U9, U34, or U4.

HORIZONTAL SYNC PROBLEMS. Using A6U6 pin 7 as a clock, monitor Character Line Counter U6. The counter should count from 0 to 9 repetitively. Display Row Counter U11/U12 can be checked using A6U11 pin 2 as a clock. U11/12 should count from 0 to 25 repetitively. If the count is correct, the horizontal sync problem is in U23, U34, U10, U1, or U4.

INVERSE VIDEO PROBLEMS. Data line D6 from A6U21 controls the inverse video field. After the power-up sequence, D6 should be toggling. If inverse video problems occur, trace the signal through U1, U2, and U4.

BLINKING PROBLEMS. Data line D7 from A6U22 controls blinking characters. After the power-up sequence, D7 should be toggling. Check the 2-Hz signal from U5 pin 13. If the blanking between display lines is correct and a blinking problem exists, then U22, U5, or U27 is bad.

U14 TRUTH TABLE

INPUT					INTERNAL OUTPUTS		OUTPUT
SHIFT/ LOAD	CLOCK INHIBIT	CLOCK	SERIAL	PARALLEL A. . . H	Q_A	Q_B	Q_H
L	X	X	X	a. . . h	a	b	h
H	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	↑	H	X	H	Q_{A0}	Q_{Gn}
H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	H	↑	X	X	Q_{A0}	Q_{B0}	Q_{H0}

U31-33 TRUTH TABLE

INPUTS				OUTPUT Y
STROBE	SELECT	A	B	
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

μP HARDWARE ADDRESSES

ADDRESS	FUNCTION
320000_8 through 323778	Accesses Display RAM
334000_8 through 337778	Accesses Temporary Storage

U5/7/8/11/12 COUNT EQUATIONS

COUNT ENABLE = EP • ET • PE
TC = ET • $\overline{QA}$ • QB • QC • QD
PRESET = $\overline{PE}$ • CK+
RESET = $\overline{MR}$

U6 COUNT EQUATIONS

COUNT ENABLE = EP • ET • PE
RC = ET • $\overline{QA}$ • $\overline{QB}$ • $\overline{QC}$ • QD
PRESET = $\overline{PE}$ • CK+
RESET = $\overline{MR}$

TROUBLESHOOTING

Most problems on the A6 assembly can be isolated using the troubleshooting tree in figure 8-4. Horizontal and vertical sync problems can be found using a logic state analyzer.

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U14 TRUTH TABLE

INPUT					INTERNAL OUTPUTS		OUTPUT
SHIFT/ LOAD	CLOCK INHIBIT	CLOCK	SERIAL	PARALLEL A. . . H	Q_A	Q_B	Q_H
L	X	X	X	a. . . h	a	b	h
H	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	↑	H	X	H	Q_{A0}	Q_{Gn}
H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	H	↑	X	X	Q_{A0}	Q_{B0}	Q_{H0}

U31-33 TRUTH TABLE

INPUTS				OUTPUT Y
STROBE	SELECT	A	B	
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

μP HARDWARE ADDRESSES

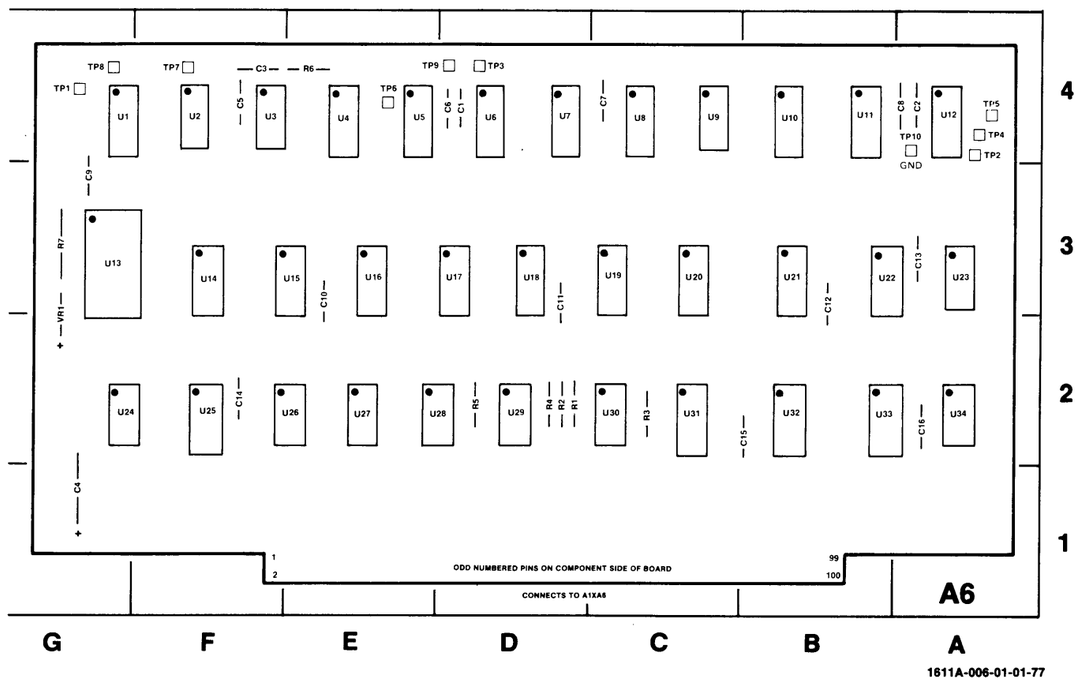
ADDRESS	FUNCTION
32000_8 through 32377_8	Accesses Display RAM
33400_8 through 33777_8	Accesses Temporary Storage

U5/7/8/11/12 COUNT EQUATIONS

COUNT ENABLE = EP • ET • PE
TC = ET • $\overline{QA}$ • QB • QC • QD
PRESET = $\overline{PE}$ • CK+
RESET = $\overline{MR}$

U6 COUNT EQUATIONS

COUNT ENABLE = EP • ET • PE
RC = ET • $\overline{QA}$ • $\overline{QB}$ • $\overline{QC}$ • QD
PRESET = $\overline{PE}$ • CK+
RESET = $\overline{MR}$

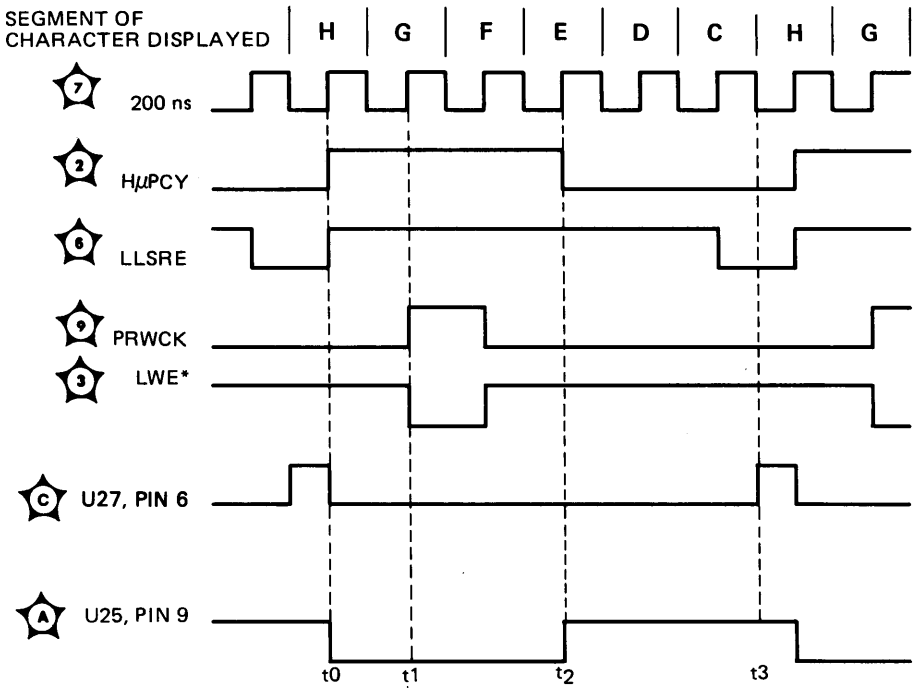


REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC
C1	D-4	R2	D-2	U2	F-4	U19	C-3
C2	A-4	R3	C-2	U3	F-4	U20	C-3
C3	F-4	R4	D-2	U4	E-4	U21	B-3
C4	G-1	R5	D-2	U5	E-4	U22	B-3
C5	F-4	R6	E-4	U6	D-4	U23	A-3
C6	D-4	R7	G-3	U7	D-4	U24	G-2
C7	C-4	TP1	G-4	U8	C-4	U25	F-2
C8	A-4	TP2	A-4	U9	C-4	U26	E-2
C9	G-3	TP3	D-4	U10	B-4	U27	E-2
C10	E-3	TP4	A-4	U11	B-4	U28	E-2
C11	D-3	TP5	A-4	U12	A-4	U29	D-2
C12	B-3	TP6	E-4	U13	G-3	U30	C-2
C13	A-3	TP7	F-4	U14	F-3	U31	C-2
C14	F-2	TP8	G-4	U15	E-3	U32	B-2
C15	B-2	TP9	E-4	U16	E-3	U33	B-2
C16	A-2	TP10	A-4	U17	D-3	U34	A-2
R1	D-2	U1	G-4	U18	D-3	VR1	G-3

IC REF DES	HP PART NO.	MFR PART NO.
U1,4,24,25	1820-1196	SN74LS174N
U2	1820-0683	SN74S04N
U3	1820-1285	SN74LS54N
U5,7,8,11,12	1820-1430	SN74LS161N
U6	1820-1429	SN74LS160N
U9,10,23	1820-1202	SN74LS10N
U13	1818-0237	2513
U14	1820-1042	SN74165N
U15-22	1818-0348	AM9102APC
U26,29	1820-1200	SN74LS05N
U27	1820-1158	SN74S51N
U28	1820-1112	SN74LS74N
U30	1820-1415	SN74LS13N
U31,32,33	1820-1470	SN74LS157N
U34	1820-1197	SN74LS00N

RAM and Display Format Generator Board A6 Component Locator
(01611-66506)

Figure 8-12. Service Sheet 6, and Display Format Generator Assembly A6 (Sheet 1 of 2)



*ONLY WHEN 8080A ON A5 IS WRITING TO THE A6 ASSEMBLY (ADD=32000_8-32777_8)

t_0 - CHARACTER ROW SELECT, BLANKING, BLINKING, INVERSE VIDEO AND CHARACTER ARE CLOCKED INTO U1 AND U24 FOR CHARACTER BEING DISPLAYED.

t_1 - COUNTERS FOR DISPLAY ADDRESS ARE CLOCKED.

t_2 - DATA FROM RAM IS LATCHED INTO U25 AND U28 IF INTERNAL μP IS ADDRESSING A6.

t_3 - BLANKING AND CLOCK INHIBIT (U14) SIGNALS ARE LATCHED INTO U4 FOR NEXT CHARACTER. DISPLAY DATA FROM CHARACTER ROM IS LOADED INTO SHIFT REGISTER U14.

A6 Timing Diagram

C H G

t3

SEMBLY (ADD=32000$_8$-32777$_8$)

VERSE VIDEO AND CHARACTER
EING DISPLAYED.

NTERNAL μP IS ADDRESSING A6.

LATCHED INTO U4 FOR NEXT
M IS LOADED INTO SHIFT REGISTER

A6 RAM AND DISPLAY FORMAT GENERATOR (01611-66506)

5 7 P/OP1 42
5 5 HWRT 77
5 8 PRWCK 39
A13 91
A12 90
A11 89
A10 88
A9 87
A8 86
A7 85
A6 84
4 μP ADDRESS BUS 5
A5 83
A4 82
A3 81
A2 80
A1 79
A0 78
5 11 50
5 9 56

HμPCY
TO U24 PIN 9
U30B
LWE
TP3
HRADR
TP1
+5V
R2 2210
R3 39.2
C1 27
U30A
U29D
R1 2210
U29E
RAM ADDRESS SELECT SWITCH U31-U33
U33
U32
U31
2-TO-1 DATA SELECTOR
HDSPC
NC
TP2
LLSRE
TP6
U27A
200ns CLOCK
TP7
HμPCY

3 5 μP DATA BUS
P/O P1
D0 D1 D2 D3 D4 D5 D6
68 69 70 71 72 73 74
1024-BY-1 RAM U15 U16 U17 U18 U19 U20 U21
WE CS DIN DOUT
A9 A8 A7 A6 A5 A4 A3 A2 A1 A0
1024-BY-8 RAM U15-U22

U9B
U10A
U10C
DISPLAY COLUMN COUNTER U7//U8
U8 BINARY COUNTER
U7 BINARY COUNTER
CHARACTER LINE COUNTER U6
U6 DECADE COUNTER
DISPLAY LINE COUNTER U11/U12
U11 BINARY COUNTER
U12 BINARY COUNTER
2-HZ CLOCK G U5
9.5HZ
76.3 Hz
TP9
R4 2210
U29F
R5 1000
U29B
C2 27
HORIZONTAL SYNC GENERATOR U9A/C, U34C/D
U9A U9C U34C U34D
TP5
VERTICAL SYNC GENERATOR U23A/B/C, U34C/B
U23A U23B U23C U34A U34B
HBK2L

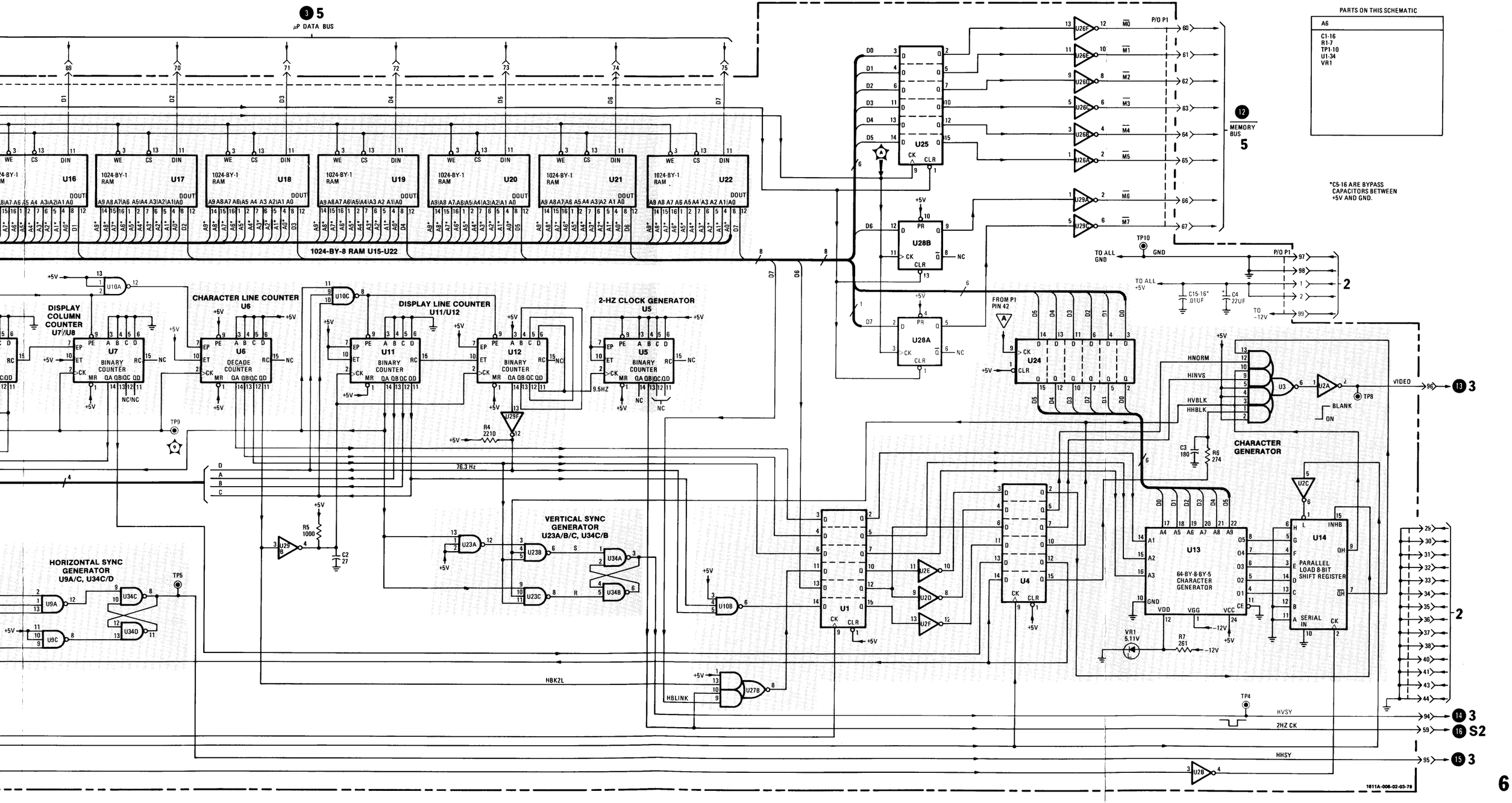


Figure 8-12. Service Sheet 6, RAM and Display Format Generator Assembly A6 (Sheet 2 of 2)

SERVICE SHEET 7

PRINCIPLES OF OPERATION

The A7 assembly compares data from the microprocessor (μP) under test to the trace specification and generates signals that control the counters and memory on the A8 assembly. A7 also outputs status signals that are used by the internal μP to determine the status of a measurement. A7 can be divided into these functions: an Address Decoder, a Trigger Gating circuit which controls various signal outputs dependent on measurement mode set-up, and a RAM Comparator circuit that generates triggers when trace specifications shown on the display are met.

The Address Decoder detects addresses of the RAM comparator (37000$_8$-37137$_8$) and of measurement mode control latch A7U18 (36140$_8$). When 37000$_8$ thru 37137$_8$ is detected on the μP ADDRESS bus, information on the μP DATA bus is loaded into the RAMs on A7. When address 36140 is detected, A7U18 is clocked by A7U30. The clock causes the four least significant bits of the μP DATA bus to be latched to the output of A7U18. A7U18 and A7U33B generate five signals (HRMC, LRST, HTRC, HTI, HCT) that initialize circuitry on A7 and A8 and control the type of measurement (COUNT TRIGGERS, COUNT TIME or TRACE) made by the 1611A.

The RAM comparator uses random access memory to generate triggers that meet trace specifications shown on the display. Figure 1 shows a basic 4-bit

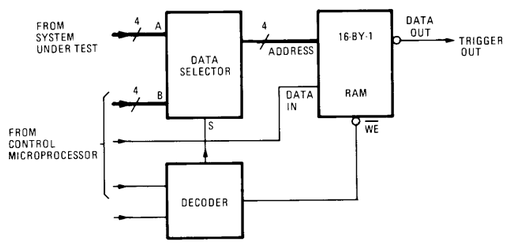


Figure 1. 4-Bit RAM Comparator

RAM comparator. Before the RAM comparator can generate triggers, it must first be loaded (written to) with a pattern that will provide a high output when the trigger condition is met and a low output when it is not. This is done in the 1611A by allowing μP A5U11 to control the data and address information to the RAM. To load the RAM, the μP first selects the B input to the data selector and drives the WE (write enable) input to the RAM low. This allows the μP to load RAM with a pattern that will detect the trigger selected. Table 1 shows how the RAM is loaded when the selected trigger is 5. Notice that the B input goes through all 16 possible combinations of a 4-bit input. This ensures that each cell in RAM is set to the correct state. The data loaded is the complement of the output desired because the RAM shown in figure 1 has an inverted output. After loading is completed, the control μP selects the A input to the data selector and puts the RAM in a READ MODE£ (WE=HIGH). When the input to A is equal to 5, output of the RAM will go high. All other inputs will produce a low output.

Table 1.

Data at B Input	Data Loaded For TRIG = 5
0	1
1	1
2	1
3	1
4	1
5	0
6	1
7	1
8	1
9	1
10	1
11	1
12	1
13	1
14	1
15	1

A RAM comparator can also be used to generate a trigger when the input is less than or greater than a specific trigger. This is accomplished by changing the pattern loaded into the RAM by the control μP. Table 2 shows some examples of the loaded patterns for different triggers.

Table 2.

Data at B	Data Loaded for Specified Trigger Condition				
	TRIG=5	TRIG>5	TRIG>5	TRIG<5	TRIG<5
0	1	1	1	0	0
1	1	1	1	0	0
2	1	1	1	0	0
3	1	1	1	0	0
4	1	1	1	0	0
5	0	1	0	1	0
6	1	0	0	1	1
7	1	0	0	1	1
8	1	0	0	1	1
9	1	0	0	1	1
10	1	0	0	1	1
11	1	0	0	1	1
12	1	0	0	1	1
13	1	0	0	1	1
14	1	0	0	1	1
15	1	0	0	1	1

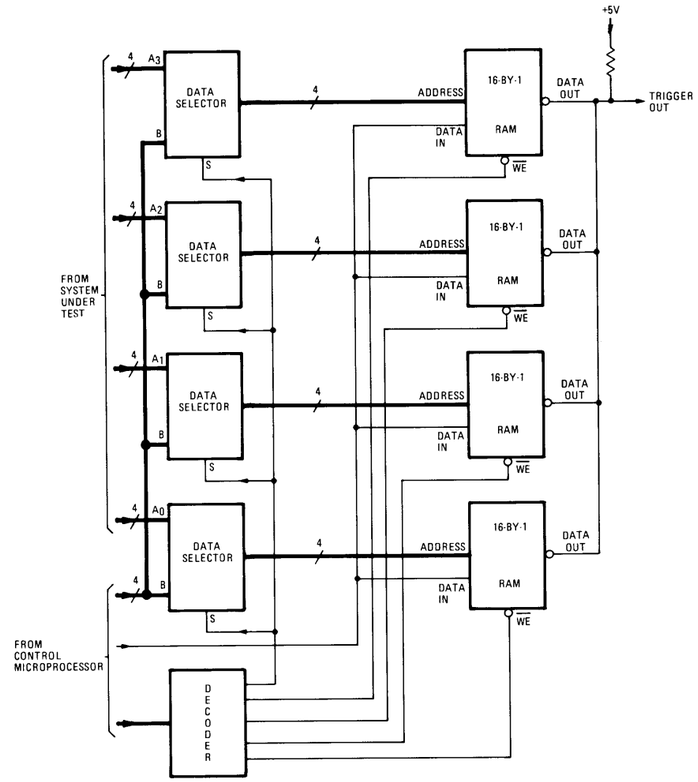


Figure 2. 16 Bit RAM Comparator (= ONLY)

A RAM comparator can easily be expanded to more than 4 bits by adding more DATA SELECTORS and RAM plus some additional decoding circuitry. Figure 2 shows a 16 bit RAM comparator.

This circuitry employs the wired AND capability of the open collector outputs of the RAMs. The decoder determines when the RAM comparator is to be loaded and which RAM will be loaded. Since the trigger specified may be different for each group of A inputs, the RAMs must be loaded separately. When the RAMs are loaded, the control μP selects the A inputs. When all four A inputs are equal to the selected trigger, the output will go high. Anytime the trigger condition is not met in one or more of the RAMs, the output will be pulled low.

The circuit shown in figure 2 works only when a trigger is needed for A inputs equal to the specified value. To permit ≥ or ≤ triggering, additional RAMs and gating are necessary. In the 1611A, 16-by-4 RAMs are used instead of 16-by-1 RAMs. This allows four different trigger patterns, for the same 4 input bits to be loaded in one RAM. Figure 3 shows a 16-bit comparator connected for triggering using two outputs of a 16-by-4 RAM. All RAMs except the one looking at the four least significant bits must provide two outputs, one for equal to and one for greater than triggering. These additional outputs are needed because conditions exist where less than 16 bits determine whether the trigger conditions are met. For example, if the A3 inputs are the most significant and they are greater than the specified trigger value for those bits, then the ≥ condition has been met regardless of the value of the remaining 12 bits. Gating on the RAM outputs allows the less significant bits to be compared if the most significant bits equal the specified trigger.

The RAM comparator on A7 has four outputs (HENB, HDSB, LTRG1, LTRG2). ENABLE (HENB) and DISABLE (HDSB) are derived from 32 inputs made up of the Input Address bus (INP A0-A15), Input Data bus (IND D0-D7) and external inputs (EXT0-7) from the μP under test. Both outputs produce a high level only when the inputs are equal to the trigger specified. LTRG1 is used for = or ≤ trigger conditions depending on the trace specification field selected. LTRG2 is used for

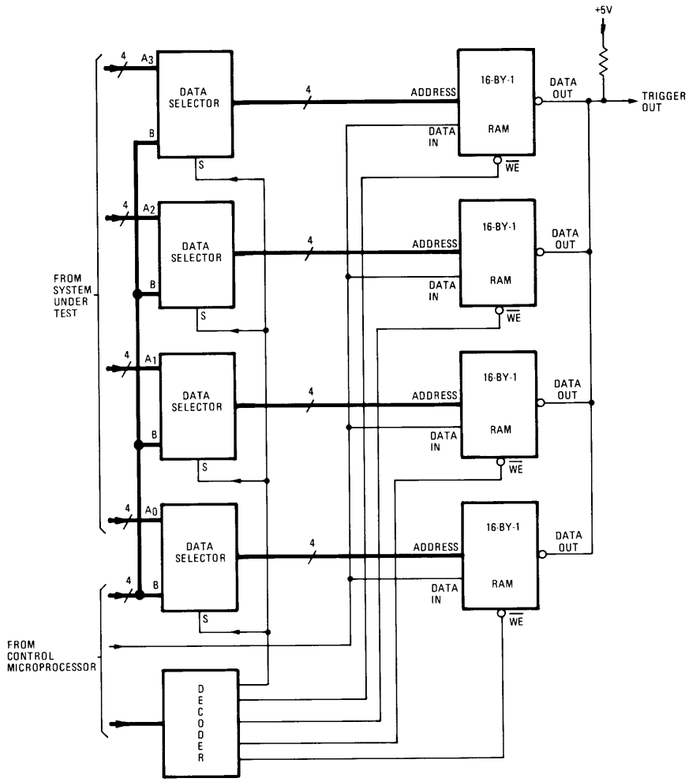


Figure 2. 16 Bit RAM Comparator (= ONLY)

ator can easily be expanded to more ding more DATA SELECTORS and dditional decoding circuitry. Figure 2 M comparator.

nploys the wired AND capability of outputs of the RAMs. The decoder the RAM comparator is to be loaded will be loaded. Since the trigger different for each group of A inputs, be loaded separately. When the the control μP selects the A inputs. nputs are equal to the selected trig- will go high. Anytime the trigger net in one or more of the RAMs, the ed low.

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tor connected for triggering using two outputs of a 16-by-4 RAM. All RAMs except the one looking at the four least significant bits must provide two outputs, one for equal to and one for greater than triggering. These additional outputs are needed because conditions exist where less than 16 bits determine whether the trigger conditions are met. For example, if the A3 inputs are the most significant and they are greater than the specified trigger value for those bits, then the ≥ condition has been met regardless of the value of the remaining 12 bits. Gating on the RAM outputs allows the less significant bits to be compared if the most significant bits equal the specified trigger.

The RAM comparator on A7 has four outputs (HENB, HDSB, LTRG1, LTRG2). ENABLE (HENB) and DISABLE (HDSB) are derived from 32 inputs made up of the Input Address bus (INP A0-A15), Input Data bus (IND D0-D7) and external inputs (EXT0-7) from the μP under test. Both outputs produce a high level only when the inputs are equal to the trigger specified. LTRG1 is used for = or ≤ trigger conditions depending on the trace specification field selected. LTRG2 is used for

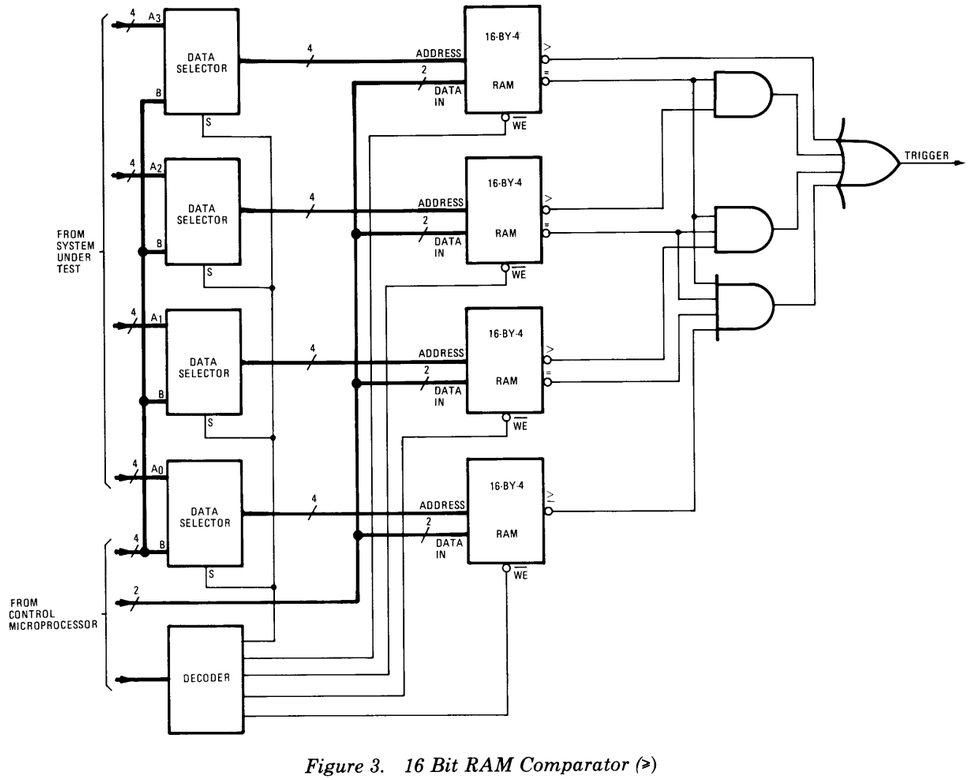


Figure 3. 16 Bit RAM Comparator (≥)

≥ only. LTRG1 and LTRG2 use address, data, and external information to detect a trigger. When the ADDRS BUS ≥ and ADDRS BUS ≤ are used with Data and External specifications, the ≥ or ≤ applies only to the address bus. Data and External trigger conditions are the same for LTRG1 and LTRG2. Table 3 shows the RAM outputs associated with each of the four outputs. All outputs in the HENB or HDSB columns must be true before HENB or HDSB goes high. LTRG1 or LTRG2 goes low when outputs of the RAM comparing the data and external inputs go high and a combination of outputs for the addresses go high that satisfy the LTRG1 (= or ≤) or LTRG2 (≥) conditions.

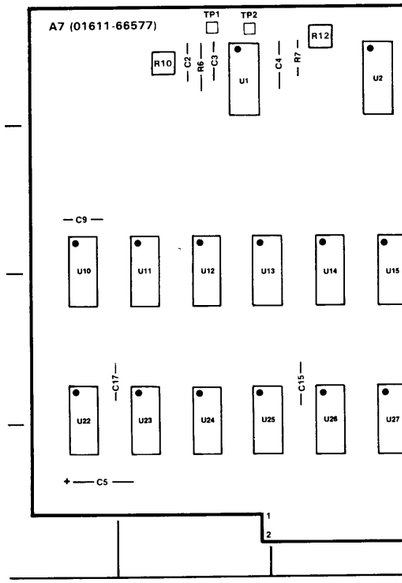
The RAM comparator has one output, A7U11 pin 11 (HAND), that is not data dependent. HAND determines whether the two triggers LTRG1, and LTRG2 are combined in a logical AND or a logical OR at A7U3 to produce HTRG. HAND is true only when the Address Bus ≤ specification is greater than the Address Bus ≥ specification.

The Trigger Gating circuit detects the presence of the four triggers and generates signals for the A8 assembly. Each time a 32-bit word is captured by the A9 assembly, it may produce a compare command (NCP). NCP is delayed 270 ns by A7U1A. It then clocks A7U1B which produces a low pulse (LCPCK) for 75 ns. The 270 ns delay allows time for the data from A9 to propagate through the data selectors and to access the RAMs. The negative edge of LCPCK clocks enable-disable latches U20A and U20B. If HENB or HDSB are true on this edge, they are latched by U20 (HENBL and HDSBL). On the positive edge of LCPCK, A7U6B is clocked. If the disable trigger HDSB was true on the negative edge of LCPCK, A7U6 pin 8 (B) (LDLYDS) will go low. In some measurement modes LDLYDS allows processing of an HTRG from A7U8 when HDSB occurs at the same time. During the time that LCPCK is low, A7U8 is enabled. If a trigger is produced by LTRG1 or LTRG2 during this time, A7U8 pin 8 (HTRG) goes high. If HAND is true, both LTRG1 and LTRG2 must be true before HTRG can go high. If HAND is low only one of the triggers is needed.

The remaining signals on A7 are discussed in the measurement mode description on Service Sheet 8.

	HENB	HDSE
A0-A3	U14 (11)	U14 (
A4-A7	U15 (9)	U2 (5
A8-A11	U16 (9)	U3 (
A12-A15	U17 (9)	U4 (
D0-D3	U12 (9)	U12 (
D4-D7	U13 (9)	U13 (
Ext 0-3	U10 (9)	U10 (
Ext 4-7	U11 (9)	U11 (

LTRG1: = or ≤
LTRG2: ≥ only



ICs ON THIS SCHEMATIC

IC REF DES	HP PART NO.	MFR P
U1	1820-1782	AM2
U2-4, 10-17	1816-0913	AM3
U5, 7	1820-1285	SN74
U6	1820-1112	SN74
U8, 32	1820-0691	SN74
U9, 31	1820-1202	SN74
U18	1820-1195	SN74
U19	1820-1203	SN74
U20, 34	1820-1212	SN74
U21	1820-0681	SN74
U22-29	1820-1470	SN74
U30	1820-1418	SN74
U33	1820-0686	SN74
U35, 36	1810-0041	1810

Figure 8-13. Service Sh

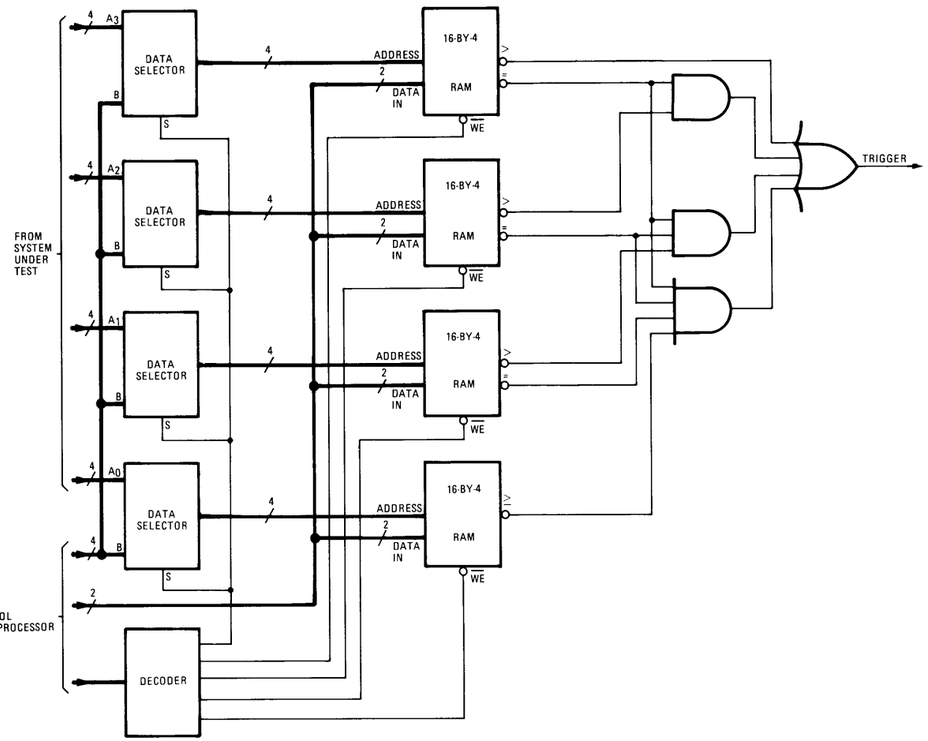


Figure 3. 16 Bit RAM Comparator (>)

. LTRG1 and LTRG2 use address, data, and ex- information to detect a trigger. When the S BUS > and ADDRS BUS < are used with Data xternal specifications, the > or < applies only to ddress bus. Data and External trigger conditions e same for LTRG1 and LTRG2. Table 3 shows the outputs associated with each of the four outputs. tputs in the HENB or HDSB columns must be efore HENB or HDSB goes high. LTRG1 or 2 goes low when outputs of the RAM comparing ta and external inputs go high and a combination puts for the addresses go high that satisfy the 1 (= or <) or LTRG2 (>) conditions.

RAM comparator has one output, A7U11 pin 11 D), that is not data dependent. HAND deter- whether the two triggers LTRG1, and LTRG2 mbined in a logical AND or a logical OR at to produce HTRG. HAND is true only when the ss Bus < specification is greater than the Address specification.

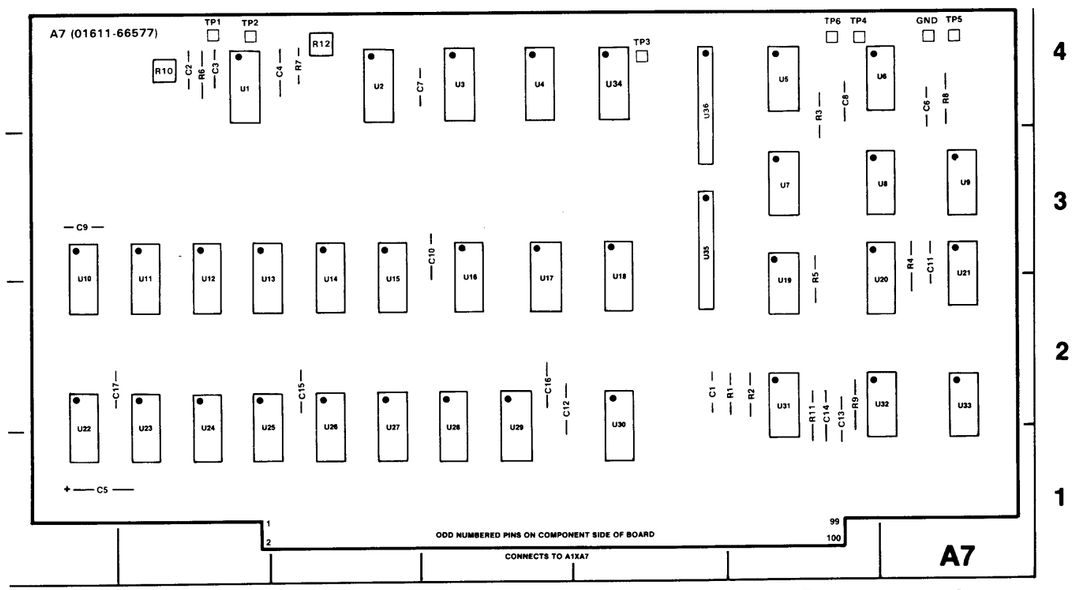
Trigger Gating circuit detects the presence of ur triggers and generates signals for the A8 assembly. Each time a 32-bit word is captured by the A9 assembly, it may produce a compare command (NCP). NCP is delayed 270 ns by A7U1A. It then clocks A7U1B which produces a low pulse (LCPCK) for 75 ns. The 270 ns delay allows time for the data from A9 to propagate through the data selectors and to access the RAMs. The negative edge of LCPCK clocks enable-disable latches U20A and U20B. If HENB or HDSB are true on this edge, they are latched by U20 (HENBL and HDSBL). On the positive edge of LCPCK, A7U6B is clocked. If the disable trigger HDSB was true on the negative edge of LCPCK, A7U6 pin 8 (B) (LDLYDS) will go low. In some measurement modes LDLYDS allows processing of an HTRG from A7U8 when HDSB occurs at the same time. During the time that LCPCK is low, A7U8 is enabled. If a trigger is produced by LTRG1 or LTRG2 during this time, A7U8 pin 8 (HTRG) goes high. If HAND is true, both LTRG1 and LTRG2 must be true before HTRG can go high. If HAND is low only one of the triggers is needed.

The remaining signals on A7 are discussed in the measurement mode description on Service Sheet 8.

Table 3.

	HENB	HDSB	LTRG1 =	LTRG1 <	LTRG2 =	LTRG2 >
A0-A3	U14 (11)	U14 (5)	U14 (9)	U14 (9)	U14 (7)	U14 (7)
A4-A7	U15 (9)	U2 (5)	U15 (5)	U15 (7)	U2 (9)	U2 (11)
A8-A11	U16 (9)	U3 (5)	U16 (5)	U16 (7)	U3 (9)	U3 (11)
A12-A15	U17 (9)	U4 (5)	U17 (5)	U17 (7)	U4 (9)	U4 (11)
D0-D3	U12 (9)	U12 (5)	U12 (7)	none	U12 (7)	none
D4-D7	U13 (9)	U13 (5)	U13 (7)	none	U13 (7)	none
Ext 0-3	U10 (9)	U10 (5)	U10 (7)	none	U10 (7)	none
Ext 4-7	U11 (9)	U11 (5)	U11 (7)	none	U11 (7)	none

LTRG1: = or ≤
LTRG2: > only



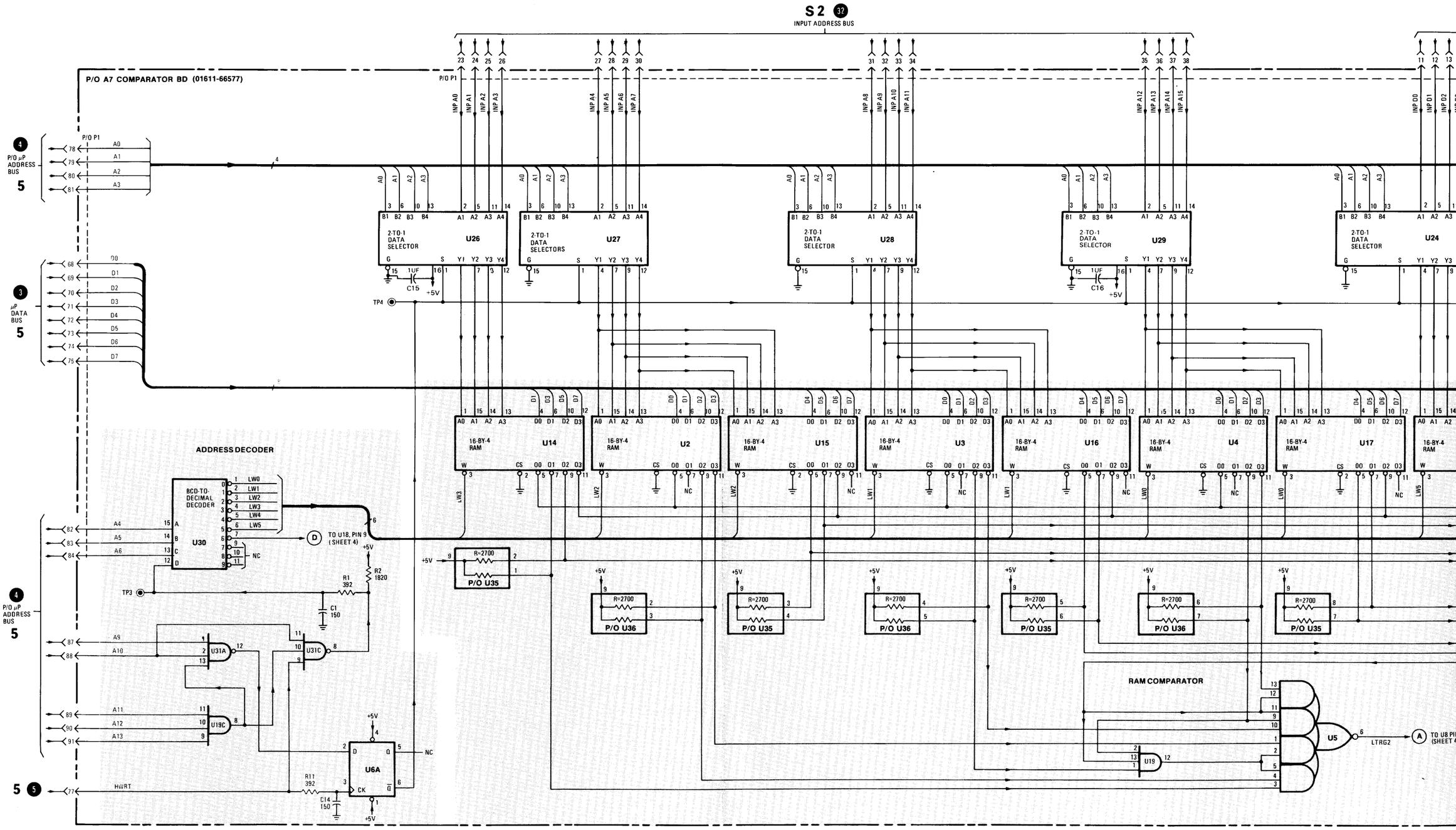
ICs ON THIS SCHEMATIC

IC REF DES	HP PART NO.	MFR PART NO.
U1	1820-1782	AM26S02PC
U2-4, 10-17	1816-0913	AM31L01PC
U5, 7	1820-1285	SN74LS54N
U6	1820-1112	SN74LS74N
U8, 32	1820-0691	SN74S64N
U9, 31	1820-1202	SN74LS10N
U18	1820-1195	SN74LS175N
U19	1820-1203	SN74LS11N
U20, 34	1820-1212	SN74LS112N
U21	1820-0681	SN74S00N
U22-29	1820-1470	SN74LS157N
U30	1820-1418	SN74LS42N
U33	1820-0686	SN74S11N
U35, 36	1810-0041	1810-0041

REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC
C1	C-2	R1	B-2	U1	F-4	U19	B-2
C2	F-4	R2	B-2	U2	E-4	U20	B-2
C3	F-4	R3	B-4	U3	D-4	U21	A-3
C4	E-4	R4	A-3	U4	D-4	U22	G-2
C5	G-1	R5	B-2	U5	B-4	U23	F-2
C6	A-4	R6	F-4	U6	B-4	U24	F-2
C7	E-4	R7	E-4	U7	B-3	U25	F-2
C8	B-4	R8	A-4	U8	B-3	U26	E-2
C9	G-3	R9	B-2	U9	A-3	U27	E-2
C10	D-3	R10	F-4	U10	G-3	U28	D-2
C11	A-3	R11	B-2	U11	F-3	U29	D-2
C12	D-2	R12	E-4	U12	F-3	U30	C-2
C13	B-2	TP1	F-4	U13	F-3	U31	B-2
C14	B-2	TP2	F-4	U14	E-3	U32	B-2
C15	E-2	TP3	C-4	U15	E-3	U33	A-2
C16	D-2	TP4	B-4	U16	D-3	U34	C-4
C17	G-2	TP5	A-4	U17	D-3	U35	C-3
				U18	C-4	U36	C-4

Comparator Board A7 Component Locator
(01611-66577)

Figure 8-13. Service Sheet 7, RAM Comparator Assembly A7 (Sheet 1 of 4)


S2 32
INPUT ADDRESS BUS
P/O A7 COMPARATOR BD (01611-66577)
P/O P1
P/O μP ADDRESS BUS
5
μP DATA BUS
5
A0
A1
A2
A3
D0
D1
D2
D3
D4
D5
D6
D7
INP A0
INP A1
INP A2
INP A3
INP A4
INP A5
INP A6
INP A7
INP A8
INP A9
INP A10
INP A11
INP A12
INP A13
INP A14
INP A15
INP D0
INP D1
INP D2
2-TO-1 DATA SELECTOR
2-TO-1 DATA SELECTORS
U26
U27
U28
U29
U24
C15
C16
1UF
+5V
TP4
16-BY-4 RAM
U14
U2
U15
U3
U16
U4
U17
W
CS
LW3
LW2
LW1
LW0
LW5
NC
ADDRESS DECODER
BCD-TO-DECIMAL DECODER
U30
LW0
LW1
LW2
LW3
LW4
LW5
TO U18, PIN 9 (SHEET 4)
R1
392
R2
1820
C1
150
TP3
U31A
U31C
U19C
U6A
R11
392
C14
150
HWRT
R=2700
P/O U35
P/O U36
RAM COMPARATOR
U5
U19
LTRG2
TO U8 PIN (SHEET 4)

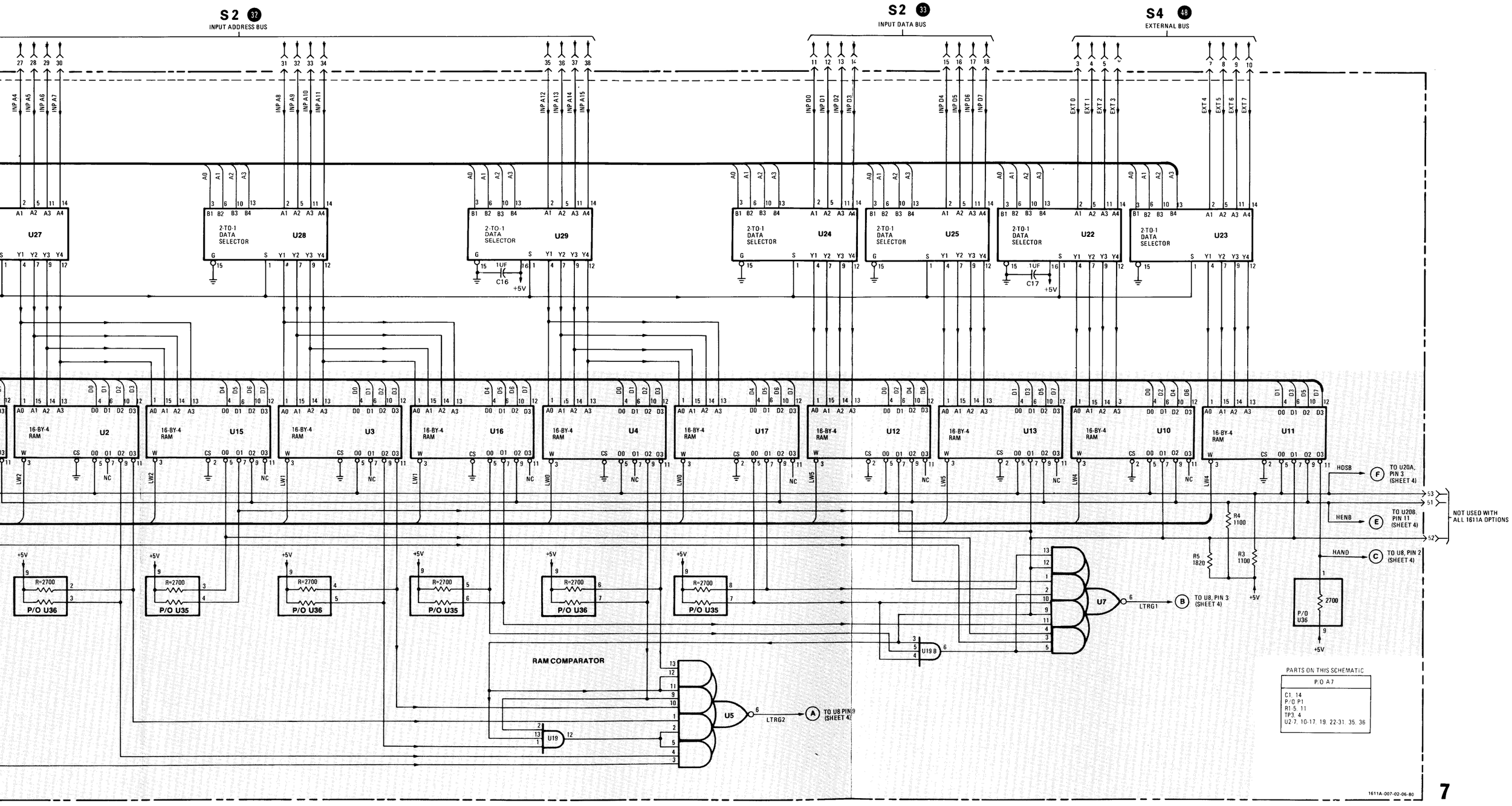


Figure 8-13. Service Sheet 7, RAM Comparator Assembly A7 (Sheet 2 of 4)

TROUBLESHOOTING

Problems on the A7 assembly can be isolated by exercising the 1611A with the front-panel PROBE TEST socket outputs. If the 1611A is not operating properly in a measurement mode (or modes), it can be checked by comparing 1611A operation to measurement mode theory and flowcharts on Service Sheet 8. The simpler Time Interval and Count Trigs modes should be verified for proper operation before troubleshooting Trace Trigs or Trace mode problems.

An improperly operating mode should be checked for proper initialization. This can be done by disconnecting the μP probe from the PROBE TEST socket and checking for an HRMC pulse and either HTRC, HTI, or HCT going high when an Execute key is pressed. "WAITING FOR ENABLE" should be displayed after the key is pressed, except in the Trace Single Step mode. Next, connect the μP probe to the PROBE TEST socket and check for proper execution. The status messages are useful in analyzing defective measurement modes (see Status Byte Table on Service Sheet 8). When triggering problems are apparent, set the FORMAT switch to HEXADECIMAL so that each digit in a trigger field corresponds to the four input bits of a specific RAM in the RAM Comparator. Before attempting to check the RAM outputs for problems, check the Address Decoder and Data Selector for proper operation when the μP is loading the comparator. This may be done using the signature analyzer test procedure on this service sheet. The timing of A7U1 should also be checked. Next, the outputs of the RAM Comparator (LTRG1, LTRG2, HENB, and HDSB) should be checked with DON'T CARE entered in the Trace specification. These signals should be checked only when A7U1 pin 10 is high. If the trigger output in question does not go to its true state with DON'T CARE entered, use a current tracer to isolate the bad RAM output. Refer to the RAM Output Table on this service sheet for the RAM outputs used to generate each trigger.

Trigger problems that are dependent on the entered trigger specification can be isolated to four bits by entering DON'T CARE for all but one digit and checking for a trigger. Once a defective trigger is found, check for presence of that trigger at the inputs of the data selectors. Inputs of the data selectors are connected directly to the High Speed Memory on the A8 assembly. Therefore, if the trigger is displayed in the list resulting from a Trace measurement, it is present at the Data Selector inputs. If the trigger is not displayed, the A9 assembly should be checked. If data at the inputs of the Data Selector is correct, check the outputs for the presence of the trigger with a logic state analyzer using the positive edge of A7U1 pin 10 as a clock. If the trigger is present, then the RAM for those bits is bad.

If no NCNT clocks are occurring, check A7U32, U9, U21, and U8. Also verify the outputs of enable/disable latches U6 and U20. The status message displayed can be used to determine why a measurement is not being completed. For incorrect counting and listing, see Service Sheet 8.

A7 SIGNATURE ANALYSIS PROCEDURE

a. Set 1611A LINE switch to off position.

b. Remove A6, A7, A8, A9 and A10 assemblies from 1611A.

c. Reinstall A7 on extender board A14.

d. Ground A5U3, pin 6.

e. Set Signature Analyzer (SA) controls as follows:

START ..... ┐
STOP ..... ┌
CLOCK ..... ┌
HOLD ..... Released

f. Connect SA probe to following circuit points.

START ..... A5U11, pin 36
STOP ..... A5U11, pin 36
CLOCK ..... A5U11, pin 18
GND ..... A5TP9 (GND)

g. Set 1611A LINE switch to on position.

h. Monitor test points listed in the following table and verify signatures.

TEST POINT	SIGNATURE
VH	755U
A7U30, Pin 1	AFA4
A7U30, Pin 2	382F
A7U30, Pin 3	C17A
A7U30, Pin 4	AA76
A7U30, Pin 5	9UF8
A7U30, Pin 6	5365
A7U30, Pin 7	5988
A7U31, Pin 12	C9C6
A7U31, Pin 10	4U68
A7U31, Pin 8	3PHP
A7U22-29, Pin 1	FFP9
A7U22-29, Pin 4	3107
A7U22-29, Pin 7	4968
A7U22-29, Pin 9	H3UC
A7U22-29, Pin 12	P600

U22-29 TRUTH TABLE

INPUTS				OUTPUT Y
STROBE	SELECT	A	B	
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

U30 TRUTH TABLE

NO.	BCD INPUT				DECIMAL OUTPUT									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
INVALID	H	L	H	L	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	H	H	H	H	H	H	H	H	H	H
	H	H	H	H	H	H	H	H	H	H	H	H	H	H

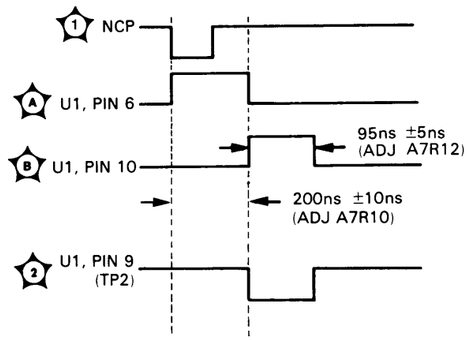
μP HARDWARE ADDRESSES

ADDRESS	FUNCTION
361408	Controls A7 measurement mode
370008 through 371378	Loads RAM Comparator

U1 TIMING EQUATION

$$T \approx 0.33\ RC\ (1 + \frac{3.0}{R})$$

Where R = kΩ
C = PF
T = ns



NOTE

Some 1611A Options may require different adjustment of ROM Comparator Board A7. Refer to the Operating and Service Manual Supplement to determine if different timing adjustments are used.

A7 Timing Diagram

Figure 8-13. Service Sheet 7, RAM Comparator Assembly A7 (Sheet 3 of 4)

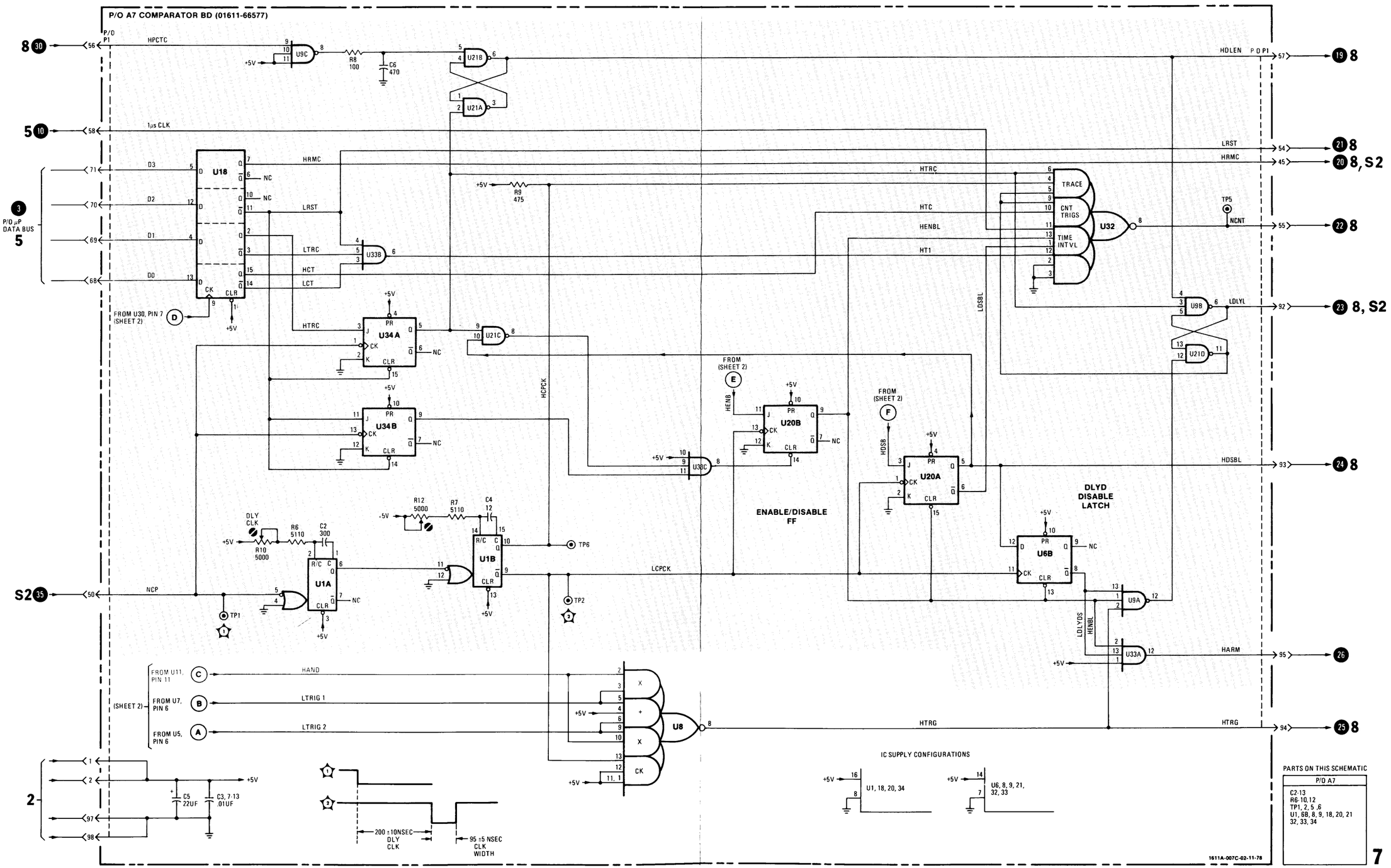


Figure 8-13. Service Sheet 7, RAM Comparator Assembly A7 (Sheet 4 of 4)

SERVICE SHEET 8

PRINCIPLES OF OPERATION

Assembly A8 contains the High-speed Memory that stores data acquired from the system under test and the Delay and Pass Counters that count time, triggers, and delay. A8 also contains the interface between the memory and counter circuits and the internal microprocessor (μP) DATA and $\overline{\text{MEMORY}}$ buses.

HIGH-SPEED MEMORY. 9-by-64 RAMS A8U25-28 make up the High-speed Memory. The memory stores 64 36-bit words. Each word consists of 16 bits of μP address, eight bits of μP data, eight bits of external information, and four flag bits. Each word corresponds to one memory transaction of the μP under test. The information stored in memory comes from Personality Board A9 and the External Latch on A10. The memory outputs to the μP on A5 through data selectors U17 and U20.

The High-speed Memory is controlled by Memory-state Counter U1 and LDSTOR. The counter addresses the location in memory that is being written to or read from. LDSTOR controls the write lines (W) of the memory. When LDSTOR goes low, data at the RAM inputs is stored at the location in memory addressed by the Memory-state Counter. When LDSTOR returns high, the memory counter is incremented through NAND gate U2C to the next address to be written to.

LDSTOR is derived through AOI U8B from NSTOR or HTRG, depending upon the measurement mode. Trigger store flip-flop U15B determines how LDSTOR is generated. In Trace Trigs mode, HTRG generates LDSTOR when HARM is true and the Memory-state Counter is not in an overflow condition. In Trace mode, LDSTOR is generated by NSTOR when binary counter U11 in the Delay Counter is not in an overflow condition. In Count Trigs and Time Interval measurement modes, the High-speed Memory and Memory-state Counter are not used.

During a Trace Trigs measurement, μP A5U11 monitors the Memory-state Counter through data selectors U19 and U21. This is accomplished when the μP reads from address 260038. A0 is inverted by U7F and applied to the S inputs of the data selectors. This low level selects the A inputs of the data selectors. The remaining address lines (shown in red) are decoded in the Address Decoder circuit to produce a low level at pin 2 of BCD-to-decimal decoder U24. This low enables U19 and U21. U19 and U21 drive the $\overline{\text{MEMORY}}$ bus with the complement of the memory state count. The $\overline{\text{MEMORY}}$ bus is complemented again on A5 so that the μP reads the true value of the memory state count.

After a Trace or Trace Trigs measurement is completed, μP A5U11 reads the data stored in the High Speed Memory. The μP reads the data by reading from address 274048, 274068, 274108, 274128, and 260078. Each of the first four addresses enables one of the four RAMS in High-speed Memory to be read through the B inputs of data selectors U17 and U20. When the μP reads from address 260078, all four RAMs are enabled (pin 15 of each RAM is pulled low). The μP then reads the four flag bits through the A inputs of data selector U17. The μP controls the address in High-speed Memory that it is reading from through the Memory-state Counter. The counter is clocked by NMCCK when the μP writes to address 260038. Pin 3 of BCD-to-decimal decoder U16 goes low when it detects a write operation to address 260038. U16, pin 3 returns to a high level when HWRT goes false. This clocks the Memory-state Counter through U2C.

DELAY AND PASS COUNTERS. The Pass and Delay Counters count time or triggers in TIME INTRVL and COUNT TRIGS measurements. They also provide digital delay when TRIGGER OCCURRENCES and BEFORE TRIG or AFTER TRIG specifications are selected.

When a counting measurement is selected, the six binary counters are cascaded to make a 24-bit binary counter. The counter counts the number of NCNT clocks generated by Assembly A7. During Count Trigs or Time Interval measurements, μP A5U11 reads the value of the counter outputs and converts the binary number to BCD. This number is written to the display memory for display on the CRT screen. The μP reads the count from addresses 260008, 260018, and 260028. These addresses are detected by the Address Decoder which enables one pair of data selectors (U19/U21 or U18/U22) by pulling pin 15 of the appropriate data selectors low. The Address Decoder also selects the correct input of the data selector (A or B). Data on the inputs is routed to the μP over the $\overline{\text{MEMORY}}$ bus.

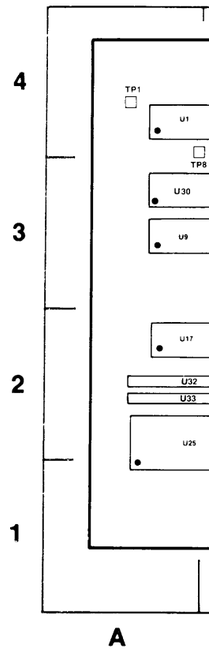
The ripple carry (RC) output of U11 is routed to JK flop-flop U15A. U15A detects a counter overflow condition. When an overflow occurs, (U11 RC output goes high), the Q output of U15A goes high (HCTOF). This status condition is read through data selector U20 when the microprocessor reads from address 260078. In the Trace mode, HCTOF indicates that the measurement is complete. In Count Trigs or Time Interval modes, HCTOF indicates that the maximum count capability has been exceeded.

A measurement can be delayed in the Trace mode, until up to 256 triggers have occurred (TRIGGER OCCURRENCE) and/or until up to 65 472 memory transactions have occurred (AFTER TRIG). The number of trigger occurrences specified must be met before the memory transaction delay starts. If no Trigger Occurrence specification ic selected, the 1611A defaults to 1. The default condition for memory transaction delay is 0.

The Pass Counter counts trigger occurrences in the Trace mode. The counter is preset by the μP such that when the specified number of trigger occurrences is reached, the RC output of U9 goes high. The μP presets the counter by subtracting 1 from the specified trigger occurrences and complementing the results. This value is written to address 260008 on the DATA bus. When the Address Decoder detects this address, it forces the parallel enable inputs (pin 7) of U9 and U14 low. This enables the two binary counters to be preset to the value on the DATA bus when a clock in received at pin 2 of both counters. The clock is produced by U4B when the Address Decoder detects HWRT and address 260008. U4B clocks U9 and U14 through U2D. R3 and C3 delay the clock so that the parallel enable inputs will go low before the clock arrives at the counters. U4B also provides the clock for the Delay Counter when it is preset.

The Delay Counter is preset in the same manner as the Pass Counter, except that 63 is added to the specified delay. This number is complemented by the μP and is loaded into the Delay Counter. This offsets the Delay Counter so that it overflows 64 counts after the point where the measurement starts. The overflow condition indicates to the μP that the measurement is complete. The Delay Counter must be loaded in two steps since it is a 16-bit counter and the μP DATA bus is only 8-bits wide. The 8 LSB's are preset when the μP writes to address 260018. The 8 MSB's are preset when it writes to address 260028.

A partial list may be displayed when using negative delay (BEFORE TRIG) due to the way the Delay Counter is loaded. A partial list is displayed when the 1611A does not acquire a sufficient number of memory transactions before the specified trigger. This causes the RC output of A8U11 to go high before the High-speed Memory has been written to 64 times.



REF DESIG	GRID LOC
C1	C-4
C2	D-4
C3	D-4
C4	B-1
C5	B-4
C6	B-3
C7	D-3
C8	G-3
C9	C-2
C10	B-1
C11	E-2
C12	E-2
C13	B-2
C14	E-4
C15	B-4
C16	E-4
CR1	F-3
L1	F-3
R1	C-4
R2	D-4
R3	D-4
R4	D-4

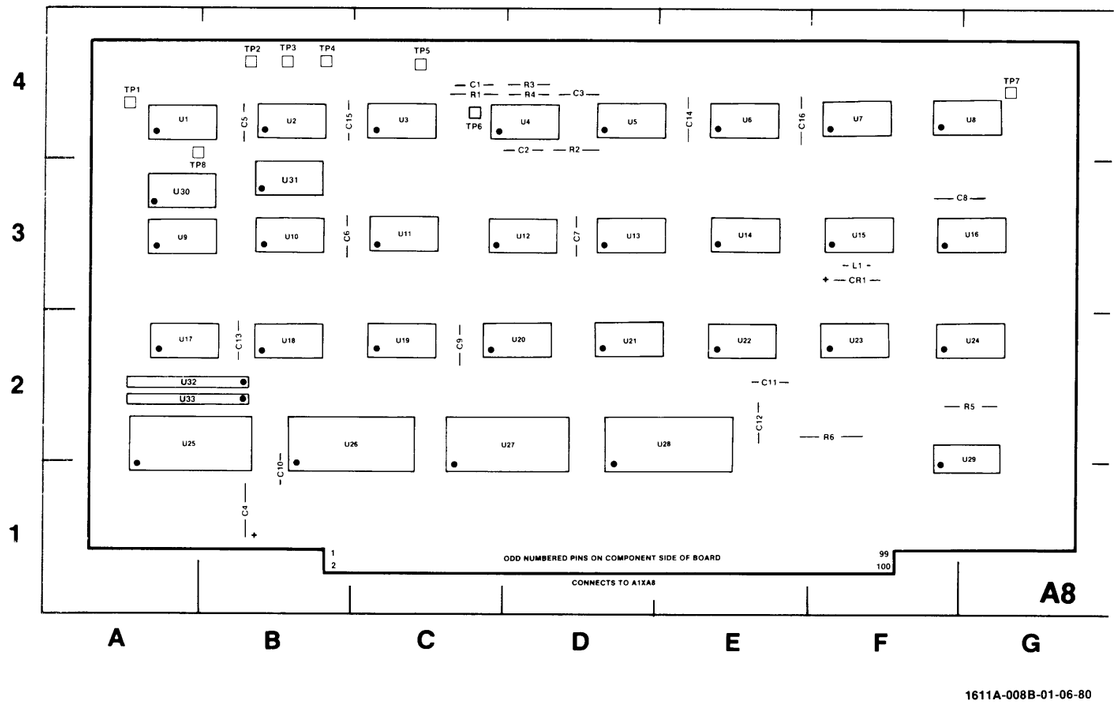
Figu

number of trigger occurrences specified must be met before the memory transaction delay starts. If no Trigger Occurrence specification is selected, the 1611A defaults to 1. The default condition for memory transaction delay is 0.

The Pass Counter counts trigger occurrences in the Trace mode. The counter is preset by the μP such that when the specified number of trigger occurrences is reached, the RC output of U9 goes high. The μP presets the counter by subtracting 1 from the specified trigger occurrences and complementing the results. This value is written to address 260008 on the DATA bus. When the Address Decoder detects this address, it forces the parallel enable inputs (pin 7) of U9 and U14 low. This enables the two binary counters to be preset to the value on the DATA bus when a clock in received at pin 2 of both counters. The clock is produced by U4B when the Address Decoder detects HWRT and address 260008. U4B clocks U9 and U14 through U2D. R3 and C3 delay the clock so that the parallel enable inputs will go low before the clock arrives at the counters. U4B also provides the clock for the Delay Counter when it is preset.

The Delay Counter is preset in the same manner as the Pass Counter, except that 63 is added to the specified delay. This number is complemented by the μP and is loaded into the Delay Counter. This offsets the Delay Counter so that it overflows 64 counts after the point where the measurement starts. The overflow condition indicates to the μP that the measurement is complete. The Delay Counter must be loaded in two steps since it is a 16-bit counter and the μP DATA bus is only 8-bits wide. The 8 LSB's are preset when the μP writes to address 260018. The 8 MSB's are preset when it writes to address 260028.

A partial list may be displayed when using negative delay (BEFORE TRIG) due to the way the Delay Counter is loaded. A partial list is displayed when the 1611A does not acquire a sufficient number of memory transactions before the specified trigger. This causes the RC output of A8U11 to go high before the High-speed Memory has been written to 64 times.



1611A-008B-01-06-80

Data Store and Counters Board A8 Component Locator
(01611-66535)

REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC
C1	C-4	R5	G-2	U13	D-3
C2	D-4	R6	F-2	U14	E-3
C3	D-4	TP1	A-4	U15	F-3
C4	B-1	TP2	B-4	U16	G-3
C5	B-4	TP3	B-4	U17	A-2
C6	B-3	TP4	B-4	U18	B-2
C7	D-3	TP5	C-4	U19	C-2
C8	G-3	TP6	C-4	U20	D-2
C9	C-2	TP7	G-4	U21	D-2
C10	B-1	TP8	A-3	U22	E-2
C11	E-2	U1	A-4	U23	F-2
C12	E-2	U2	B-4	U24	G-2
C13	B-2	U3	C-4	U25	A-2
C14	E-4	U4	D-4	U26	B-2
C15	B-4	U5	D-4	U27	D-2
C16	E-4	U6	E-4	U28	E-2
CR1	F-3	U7	F-4	U29	G-2
L1	F-3	U8	G-4	U30	A-3
R1	C-4	U9	A-3	U31	B-3
R2	D-4	U10	B-3	U32	A-2
R3	D-4	U11	C-3	U33	A-2
R4	D-4	U12	D-3		

ICs ON THIS SCHEMATIC

IC REF DES	HP PART NO.	MFR PART NO.
U1	1820-1464	SN74393N
U2	1820-1425	SN74LS132N
U3	1820-1144	SN74LS02N
U4	1820-1423	SN74LS123N
U5	1820-1212	SN74LS112N
U6, 9-11, 13, 14	1820-1430	SN74LS161N
U7	1820-1199	SN74LS04N
U8	1820-1210	SN74LS51N
U12	1820-1130	SN74LS133N
U15	1820-1116	SN74109N
U16, 24	1820-1418	SN74LS42N
U17-22	1820-1439	SN74LS258N
U23	1820-1201	SN74LS08N
U25-28	1816-0728	82S09I
U29	1820-1205	SN74LS21N
U30	1820-1112	SN74LS74N
U31	1820-1439	SN74LS258N
U32, 33	1810-0055	1810-0055

Figure 8-14. Service Sheet 8, Data Storage and Counter Assembly A8 (Sheet 1 of 6)

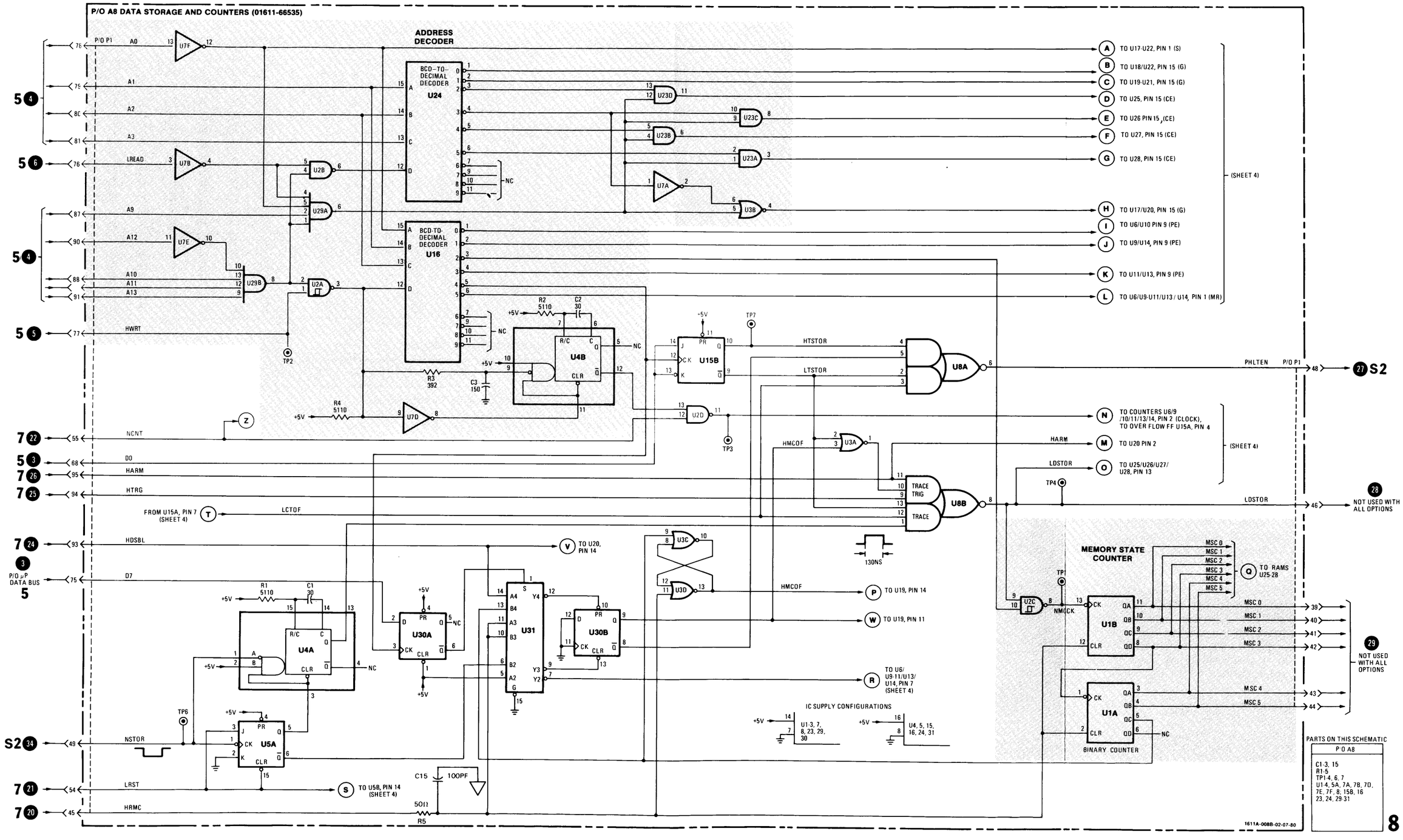
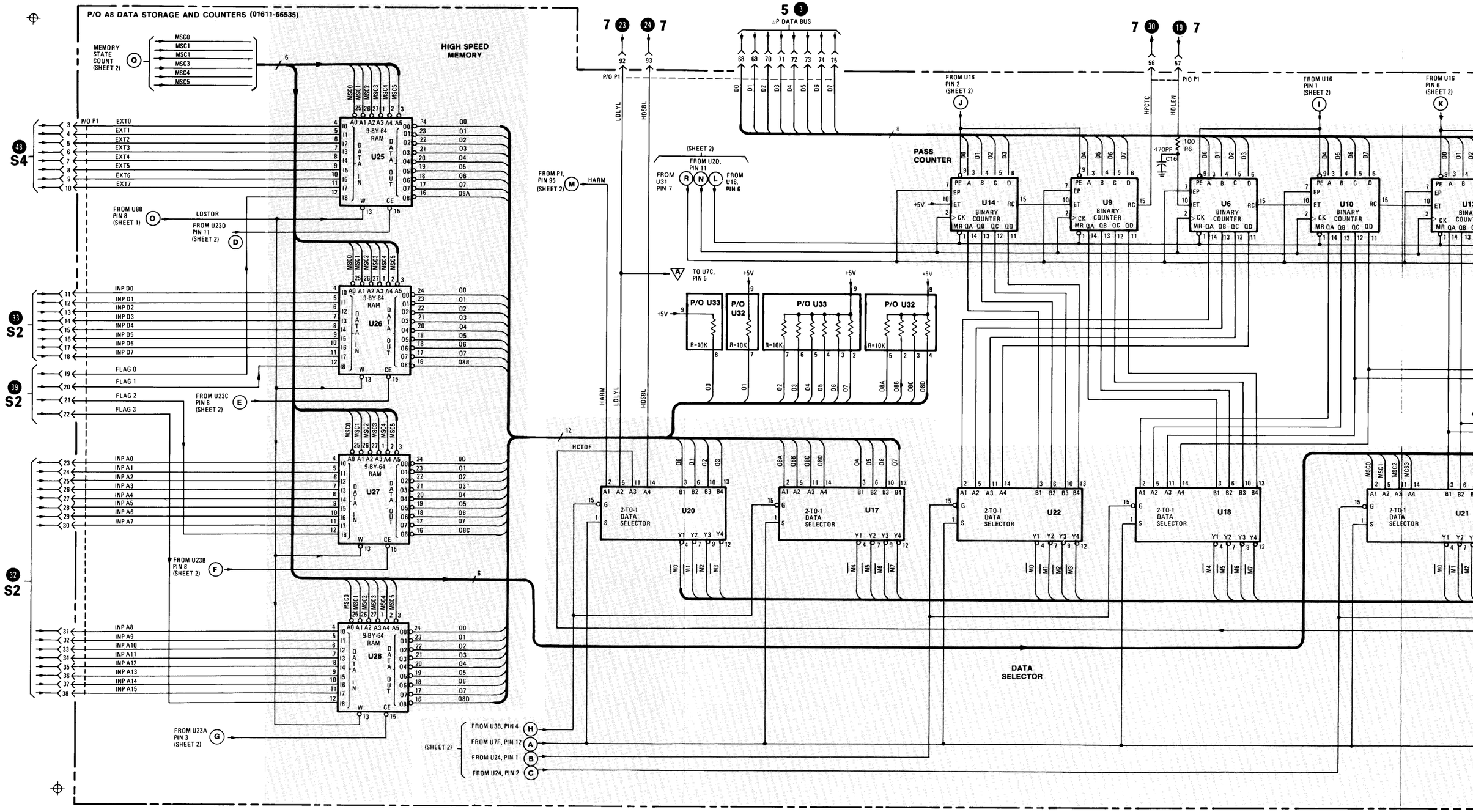


Figure 8-14. Service Sheet 8, Data Storage and Counter Assembly A8 (Sheet 2 of 6)


P/O A8 DATA STORAGE AND COUNTERS (01611-66535)
HIGH SPEED MEMORY
MEMORY STATE COUNT (SHEET 2)
MSC0
MSC1
MSC2
MSC3
MSC4
MSC5
P/O P1
EXT0
EXT1
EXT2
EXT3
EXT4
EXT5
EXT6
EXT7
S4
FROM U8B PIN 8 (SHEET 1)
LDSTOR
FROM U23D PIN 11 (SHEET 2)
INP D0
INP D1
INP D2
INP D3
INP D4
INP D5
INP D6
INP D7
S2
FLAG 0
FLAG 1
FLAG 2
FLAG 3
FROM U23C PIN 8 (SHEET 2)
INP A0
INP A1
INP A2
INP A3
INP A4
INP A5
INP A6
INP A7
FROM U23B PIN 6 (SHEET 2)
INP A8
INP A9
INP A10
INP A11
INP A12
INP A13
INP A14
INP A15
FROM U23A PIN 3 (SHEET 2)
9-BY-64 RAM
U25
U26
U27
U28
DATA IN
DATA OUT
W
CE
FROM P1, PIN 95 (SHEET 2)
HARM
LOLYL
HOSBL
HCTOF
μP DATA BUS
FROM U16 PIN 2 (SHEET 2)
FROM U16 PIN 1 (SHEET 2)
FROM U16 PIN 6 (SHEET 2)
HPCTC
HOLEN
PASS COUNTER
U14
U9
U6
U10
BINARY COUNTER
100 R6
470PF C16
(SHEET 2) FROM U2D, PIN 11
FROM U31 PIN 7
FROM U16, PIN 6
TO U7C, PIN 5
P/O U33
P/O U32
R=10K
U20
U17
U22
U18
U21
2-TO-1 DATA SELECTOR
DATA SELECTOR
FROM U3B, PIN 4
FROM U7F, PIN 12
FROM U24, PIN 1
FROM U24, PIN 2
(SHEET 2)

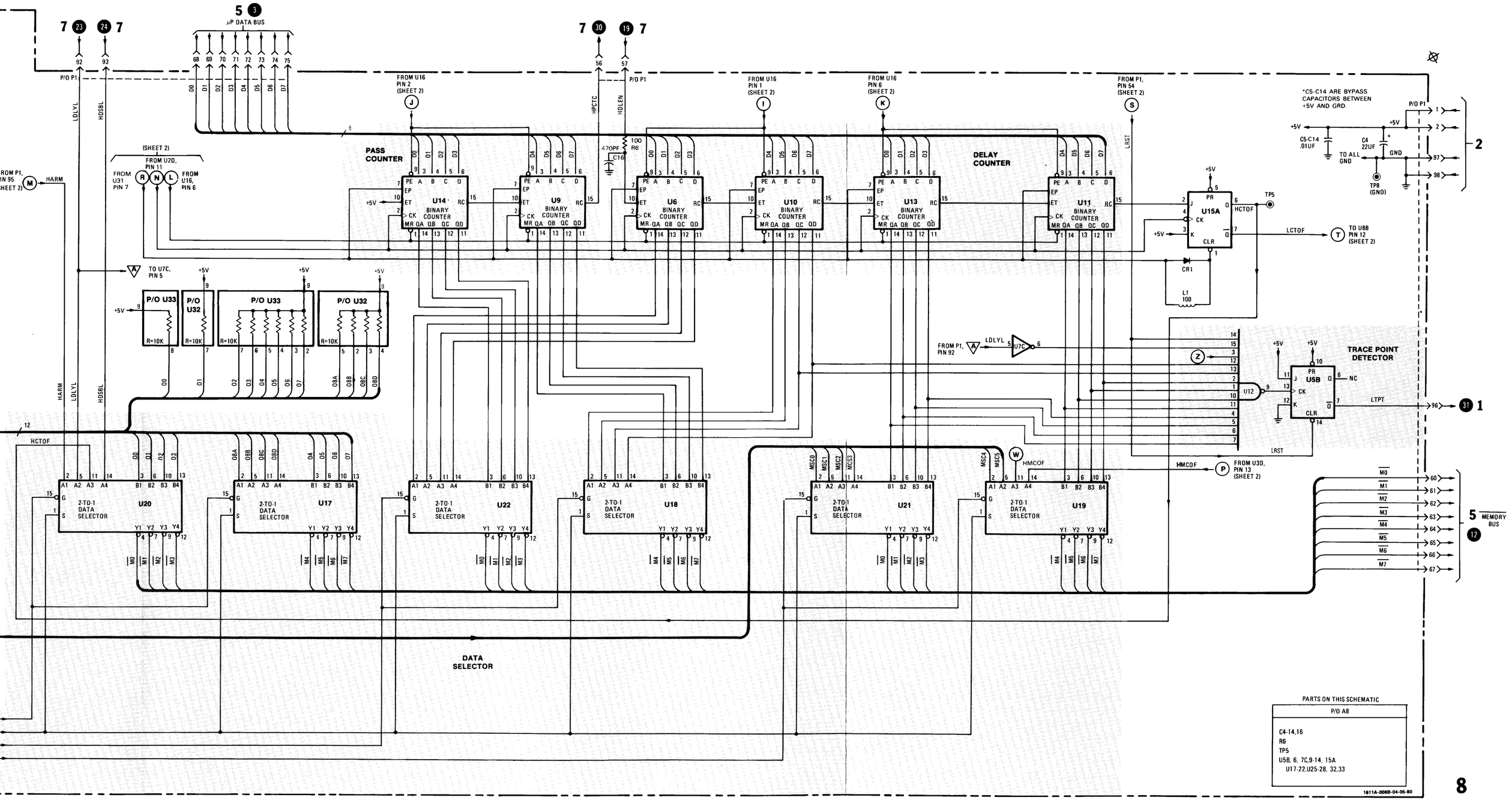


Figure 8-14. Service Sheet 8, Data Storage and Counter Assembly A8 (Sheet 4 of 6)

TROUBLESHOOTING

The PROBE TEST socket output should be used as a test signal for isolating problems on A8. The simpler Time Interval and Count Trigs measurements should be verified before Trace and Trace Trigs. When a measurement mode is operating incorrectly, remove the test signal and restart the measurement. Initial conditions described in the Measurement Mode theory on this service sheet should be checked.

The Memory State Counter, Pass Counter, and Delay Counter outputs can be checked for a reset condition or the correct preset value. If initial conditions are not correct, the output of the Address Decoder controlling the device should be checked. To continuously generate initialization signals, it is necessary to repeatedly press the STOP key and then the EXECUTE key being checked. If desired, the Address Decoder can be checked with a signature analyzer (see procedure on this service sheet).

After initialization is checked, connect the Probe Test Generator and check status bits and counters. Data being written on the MEMORY bus by a data selector can be checked when pin 15 of the data selector is low. Note that the data selector output is the complement of the input. The Delay and Pass Counter chain can be checked four bits at a time by monitoring the QA, QB, QC, and QD outputs with a logic state analyzer and clocking on pin 10 of the counter (use pin 2 for U14). The Time Interval measurement with no trigger specification provides a good clock for this check. The outputs should count from 0 to 15 on each counter. The Memory State Counter sequence can be checked in the Trace mode by viewing the entire 64-line display in absolute mode and verifying that the list progresses from 0000 through FFFF in sequence. Lines in the listing that are partially correct usually indicate a bad RAM in High-speed Memory or a bad data selector.

Inputs to the RAMs can be checked with a logic state analyzer using the negative edge of LDSTOR as a clock. Another easy check is to key in a trigger value equal to the data input being checked and verify that the 1611A triggers. This indicates presence of the data, since the inputs to the RAM Comparator are the same lines that are connected to the High-speed Memory.

A8 SIGNATURE ANALYSIS PROCEDURE.

a. Set 1611A LINE Switch to off position.

b. Remove A8 assembly and reinstall it on extender board A14.

c. Ground A5U3, pin 6.

d. Set Signature Analyzer (SA) controls as follows:

START .....]
STOP .....]
CLOCK .....]
HOLD ..... Released

e. Connect SA Probe to following circuit points:

START ..... A5U11, Pin 36
STOP ..... A5U11, Pin 36
CLOCK ..... A5U11, Pin 18
GND ..... A5TP9 (GND)

f. Set 1611A LINE switch to on position.

g. Monitor test points listed in the following table and verify signatures.

TEST POINT	SIGNATURE*
A8U2, Pin 1	V_{HP}
A8U2, Pin 2	A41U
A8U2, Pin 3	H140
A8U2, Pin 4	A41U
A8U2, Pin 5	V_{LP}
A8U2, Pin 6	V_H
A8U29, Pin 6	V_L
A8U7, Pin 3	V_{HP}
A8U7, Pin 4	V_{LP}
A8U7, Pin 10	AC99
A8U7, Pin 12	H335
A8U16, Pin 1	897C
A8U16, Pin 2	8C4H
A8U16, Pin 3	85FP
A8U16, Pin 4	8H17
A8U16, Pin 5	C719
A8U16, Pin 6	947F

*V_H = 755U, V_{HP} = 755U, V_L = 0000, V_{LP} = 0000

U17-22 TRUTH TABLE

INPUTS				OUTPUT Y
OUTPUT CONTROL	SELECT	A	B	
H	X	X	X	Z
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

Z = high impedance (off)

U16/24 TRUTH TABLE

NO.	'42A, 'L42, 'LS42 BCD INPUT				DECIMAL OUTPUT									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
INVALID	H	L	H	L	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	H	H	H	H	H	H	H	H	H	H
	H	H	H	H	H	H	H	H	H	H	H	H	H	H

μP HARDWARE ADDRESSES

ADDRESS	FUNCTION
260008	Reads or loads Pass Counter.
260018	Reads or loads 8 LSB of Delay Counter.
260028	Reads or loads 8 MSB of Delay Counter.
260038	Clocks Memory State Counter or reads its output.
260048	Resets Delay and Pass Counters to zero.
260058	Sets or clears trigger store mode. D0 = 0 → Clear, D0 = 1 → Set.
260078	Reads status of measurement and flags from High Speed Memory.
274048	Reads 8 bits of external data from High Speed Memory.
274068	Reads 8 bits of μP data from High Speed Memory.
274108	Reads 8 LSB of μP address from High Speed Memory.
274128	Reads 8 MSB of μP address from High Speed Memory.

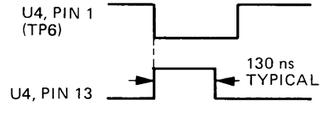
U4 TIMING EQUATION

$T \approx 0.4\ RC$

WHERE R = kΩ
C = pF
T = ns

U6/9/10/11/13/14 COUNT EQUATIONS

COUNT ENABLE = EP • ET • PE
RC = CET • QA • QB • QC • QD
PRESET = $\overline{PE}$ • CP+
RESET = $\overline{MR}$



A8 Timing Diagram

Figure 8-14. Service Sheet 8, Data Storage and Counter Assembly A8 (Sheet 3 of 6)

MEASUREMENT MODES

The following paragraphs describe how the internal microprocessor (μP) initiates, monitors and terminates each measurement made by the 1611A. The descriptions follow the measurement flow charts on this service sheet.

TIME INTERVAL. The Time Interval measurement counts 1-μs clocks between the Enable and Disable trace specifications. When TIME INTVL is pressed, internal μP A5U11 writes 14_8 to address 361408. This puts HTRC, HCT, and HTI in a low state, so that no NCNT clocks are generated by A7U32. LRST goes low and clears enable/disable latches A7U20A/B and U6B. LRST also inhibits the Pass and Delay Counters by applying a low through A8U5A to pin 7 on all the counters. HRMC goes high, resetting the Memory State Counter to 0, and resetting memory state count overflow flip-flop A8U3C/D. Next, a 0 is written to address 260048. This resets the Pass and Delay Counters to zero. Information on the data bus has no effect when the μP is writing to address 260048. This address is detected, and the master reset on all counters is pulled low by A8U16 pin 6. Next, a 0 is written to address 260058. This clears trigger store flip-flop A8U15B. A8U15B is not used in the Time Interval mode.

All counters and flip-flops are now initialized and the 1611A is ready to start a measurement. The internal μP starts a measurement by writing 37_8 to address 361408. HRMC then goes low, and LRST and HTI go high. HTI enables part of A7U32 to pass 1-μs clocks as long as HENBL is true and LDSBL is false (see figure 1). Before the Enable trigger specification is detected by the 1611A, HENBL is low and LDSBL is high. As soon as the Enable trace specification is detected by the RAM Comparator, HENBL goes high and the 1-μs clock is passed through A7U32. The count continues until the Disable trace specification is met. LDSBL then goes low and inhibits generation of NCNT.

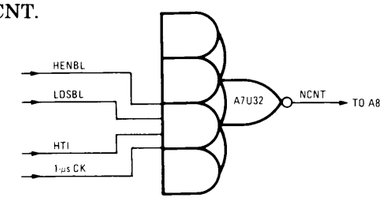


Figure 1.

During the measurement μP A5U11 monitors and displays the status of the measurement. The μP reads from address 260078 and checks the four least significant bits. The status signals are monitored through the A input of A8U20. In the Time Interval mode, μP A5U11 detects four conditions. Before the Enable trace specification is met, all status bits are low except LDLYL; thus, the status byte is 2. A WAITING FOR ENABLE message is displayed when the status byte equals 2. After the enable condition is met, the output of A7U33A (HARM) goes true, causing a COUNTING message to be displayed. If counter capacity is exceeded during the measurement, A8U15 pin 6 (HCTOF) goes high. This causes a COUNTER OVERFLOW message to be displayed (see status byte table on this service sheet).

Until the measurement is completed, μP A5U11 continues to check the status byte, update the count in the display, and monitor the keyboard for depressed keys. The count is updated by reading the binary count from the Pass and Delay Counters, converting it to BCD, and displaying the results. The keyboard monitoring function permits the operator to abort a measurement that is not complete. When the measurement is complete. A7U20 pin 5 (HDSBL) goes true. When this is detected, the μP reads the final count and displays it.

COUNTS TRIGS. The Count Trigs measurement counts the number of triggers between the Enable and Disable trace specifications. Initialization of circuits on A7 and A8 is accomplished in the same manner as in the Time Interval mode, except for generation of NCNT. To start the measurement, 37_8 is written to address 361408, This enables A7U32 to generate NCNT when a trigger is recognized between the Enable and Disable trace specifications (see figure 2). The status byte has the same meaning as in the Time Interval mode. Except for the generation of NCNT, μP A11U5 treats Count Trigs measurements the same as Time Interval measurements.

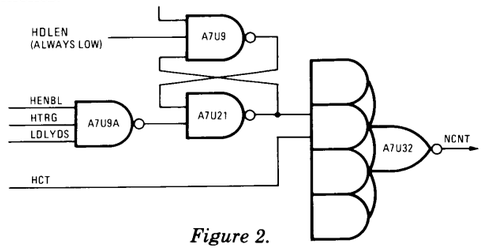


Figure 2.

TRACE TRIGS. The Trace Trigs measurement stores and displays 64 consecutive memory transactions that meet trigger specifications. No trigger occurrence or memory transaction delay is available in this mode. Before this measurement is started, the enable/disable latches and the Pass and Delay Counters are reset as in the Time Interval measurement. Next, a 1 is written to address 260058. The address is detected by the decoder on A8 and produces a clock for A8U15B. This allows the D0 line of the Data bus (high) to be latched. In Trace Trigs mode, A8U15 pin 10 (HTSTOR) is high and A815 pin 9 (LSTOR) is low. HSTOR AND LTSTOR cause LDSTOR to be generated by HTRG (see figure 3).

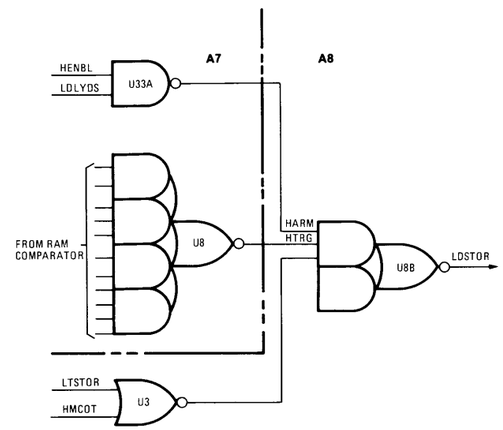


Figure 3.

The measurement begins when 2 is written to 361408 enabling A7U20A/B and A7U6 to latch the detected enable and disable triggers. Each time a trigger is recognized between the Enable and Disable trace specifications, LDSTOR causes the trigger to be stored and the Memory-state Counter to be clocked. In TRACE TRIGS mode, only two status messages are displayed. When HARM is false, a WAITING FOR ENABLE message is displayed; when HARM is true, a WAITING FOR TRIGGER message is displayed.

During the Trace Trigs measurement, data is read from address 260038. This data is the value of the memory state count. If the Memory-state Counter is not in an overflow condition, the number of memory transactions stored is displayed. When 64 words are stored, the memory counter will overflow. This inhibits A8U8 from generating more LDSTOR clocks (see figure 3). The overflow condition is detected by the internal μP, which then reads data from the High-speed Memory and displays it in absolute format.

TRACE (NORMAL). In the normal test mode, the Trace measurement allows 64 consecutive memory transactions to be stored and displayed. The starting point of the acquisition can be delayed up to 256 trigger occurrences and/or 64,742 memory transactions relative to the first recognized trigger. TRACE is initiated by writing to addresses 361408 and 260048 as in the Time Interval mode. Next, a 0 is written to 260058 to disable the trigger store mode. (HTSTOR and LTSTOR). This allows the NSTOR clock from A9 to generate LDSTOR through A8U4A and A8U8B. The Delay and Pass counters are now preset as explained in the A8 theory. Thus A8U15A, pin 6 goes high when the measurement is complete.

To start the measurement, a 2 is written to address 361408. This forces A7U32 pin 6 (HTRC) high, enabling part of U32. Until the pass counter reaches terminal count, an NCNT clock is generated only when a memory transaction meets trigger specifications and is between the Enable and Disable trace specifications. A7U9A controls this by gating HTRG through U9 when HENBL is true and LDLYDS is false. Since NCNT is equivalent to a trigger occurrence, it serves as a clock for the Pass Counter which counts the number of trigger occurrences. When the specified number of trigger occurrences has been reached, A8U9 pin 15 (HPCTC) and A7U21 pin 6 (HDLEN) go true.

HDLEN enables the delay counter to count delay and forces A7U21 pin 11 high. This allows NCNT to be generated each time a pulse from A7U1 pin 10 occurs. Since the pulse is a delayed NCP generated by the A9 assembly, it occurs on every memory transaction. NCNT now clocks the Delay Counter on every memory transaction. At this time, the HTRG, HENBL, HDSBL, and LDLYDS signals generated by A7 no longer affect NCNT generation. The measurement stops after A8U11 pin 15 goes high. This forces A8U15 pin 7 low on the next NCNT clock and prevents A8U8B from generating more LDSTOR clocks.

Up to this point, LDSTOR has been generated for each NSTOR from A9. Thus, the memory counter may have overflowed many times and the first memory transaction to be displayed may not be at location 0 in the High-speed Memory. The μP determines the first line to be displayed by first reading from address 260038, checking the Memory-state Counter for overflow, and determining the present value of the memory state count. If the counter has overflowed, the information to be displayed in the first line of the list is at the address equal to the present memory state count. If there is no overflow, the information for the first displayed line is at address 0 in the High-speed Memory.

During a measurement interval, the 1611A monitors and displays the status of the measurement. Until the first trigger is recognized, a WAITING FOR TRIGGER or WAITING FOR ENABLE message is displayed. If HARM is true when the status is read, the message is WAITING FOR TRIGGER. Otherwise WAITING FOR ENABLE is displayed. When a status byte equal to 2 or 3 is read, the pass counter value is also read (address 260008). If the value is not equal to the preset value, one or more triggers have occurred. When this condition is detected, the number of trigger occurrences is computed and displayed, rather than WAITING FOR ENABLE or WAITING FOR TRIGGER. When the pass counter reaches terminal count and LDLYL becomes true, the status byte is equal to 0 or 1, and a DELAYING message is displayed. When the measurement is complete, A8U15 pin 6 (HCTOF) goes true. This causes the status byte value to be greater than 3. A value greater than 3 indicates to the internal μP that the measurement is complete.

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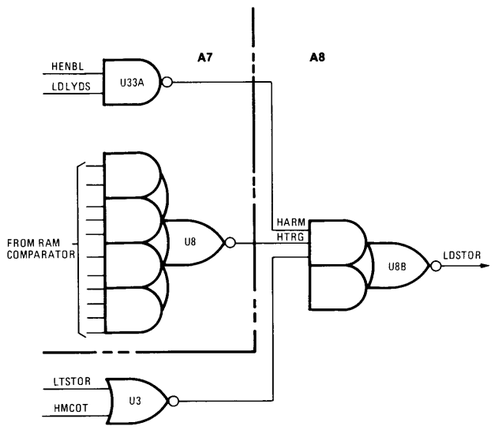

Figure 3.

The measurement begins when 2 is written to 361408 enabling A7U20A/B and A7U6 to latch the detected enable and disable triggers. Each time a trigger is recognized between the Enable and Disable trace specifications, LDSTOR causes the trigger to be stored and the Memory-state Counter to be clocked. In TRACE TRIGS mode, only two status messages are displayed. When HARM is false, a WAITING FOR ENABLE message is displayed; when HARM is true, a WAITING FOR TRIGGER message is displayed.

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During a measurement interval, the 1611A monitors and displays the status of the measurement. Until the first trigger is recognized, a WAITING FOR TRIGGER or WAITING FOR ENABLE message is displayed. If HARM is true when the status is read, the message is WAITING FOR TRIGGER. Otherwise WAITING FOR ENABLE is displayed. When a status byte equal to 2 or 3 is read, the pass counter value is also read (address 260008). If the value is not equal to the preset value, one or more triggers have occurred. When this condition is detected, the number of trigger occurrences is computed and displayed, rather than WAITING FOR ENABLE or WAITING FOR TRIGGER. When the pass counter reaches terminal count and LDLYL becomes true, the status byte is equal to 0 or 1, and a DELAYING message is displayed. When the measurement is complete, A8U15 pin 6 (HCTOF) goes true. This causes the status byte value to be greater than 3. A value greater than 3 indicates to the internal μP that the measurement is complete.

TRACE SINGLE STEP. In Single Step test mode, the TRACE key allows the 1611A to single step the μP under test and to display the memory transaction executed. To excute single step trace, no trigger specifications are required. The Trace Single Step mode is initiated like TRACE in the Norm Test mode except that the Pass and Delay counters are not preset. The only signal used from A7 in this mode is HRMC. HRMC goes high to reset the Memory-state Counter, and returns low when the measurement starts. When A9 generates an NSTOR, LDSTOR is produced by A8U8B and the memory state counter is clocked. The internal μP monitors the memory state count to determine when its value is not equal to zero. When a non-zero condition is detected, the μP starts reading from High-speed Memory and displays the result. No status messages are displayed in the Trace Single Step mode.

STATUS BYTE TABLE

STATUS BYTE VALUE*	MEASUREMENT STATUS
TRACE MODE	
2 (Trigger Occurrences = 0)	"WAITING FOR ENABLE" message is displayed if Enable specification has been entered. If no Enable specification is entered, "WAITING FOR TRIGGER" message is displayed.
3 (Trigger Occurrences = 0)	"WAITING FOR TRIGGER" Displayed
2 or 3 (Trigger Occurrences ≠ 0)	"TRIGGER OCCURRENCE =" Displayed
0 or 1	"DELAYING" Displayed
>3	End of Run
TRACE TRIGS MODE	
2 (Memory State Count = 0)	"WAITING FOR ENABLE" Displayed
≠ 2 (Memory State Count = 0)	"WAITING FOR TRIGGER" Displayed
≠ 2 (Memory State Count ≠ 0)	"TRIGGER OCCURRENCES =" Displayed
Don't Care (HMCOF = 1)	End of Run
COUNT TIME/COUNT TRIGS MODES	
2	"WAITING FOR ENABLE" Displayed
<7 and ≠ 2	"COUNTING" Displayed
7	"COUNTER OVERFLOW" Displayed
>7	End of Run
* STATUS BYTE ADDRESS = 260078 Bit 0 = HARM (A8U20, Pin 2) Bit 1 = LDLYL (A8U20, Pin 5) Bit 2 = HCTOF (A8U20, Pin 11) Bit 3 = HDSL (A8U20, Pin 14)	

Figure 8-14. Service Sheet 8, Data Storage and Counter Assembly A8 (Sheet 5 of 6)

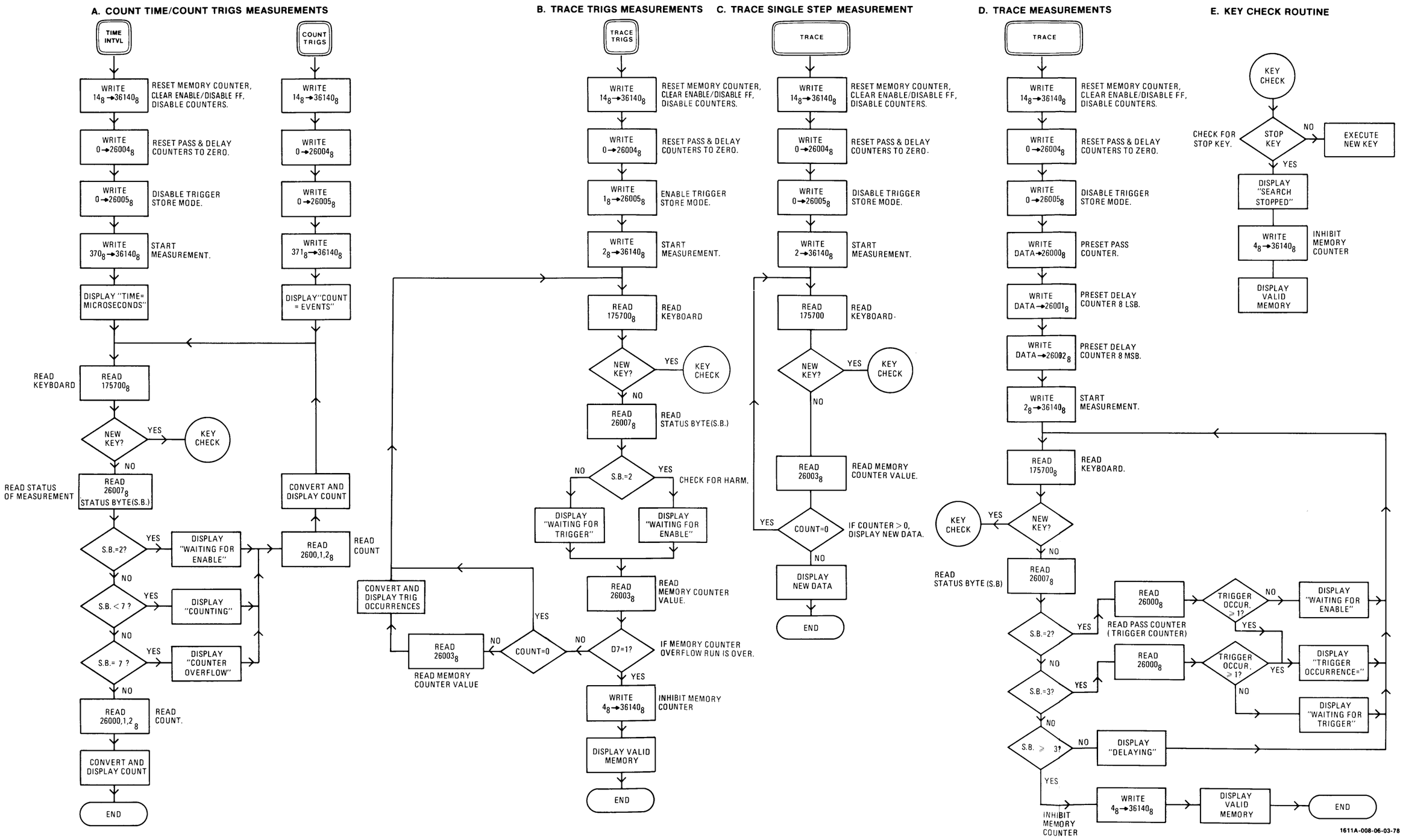


Figure 8-14. Service Sheet 8, Data Storage and Counter Assembly A8 (Sheet 6 of 6)

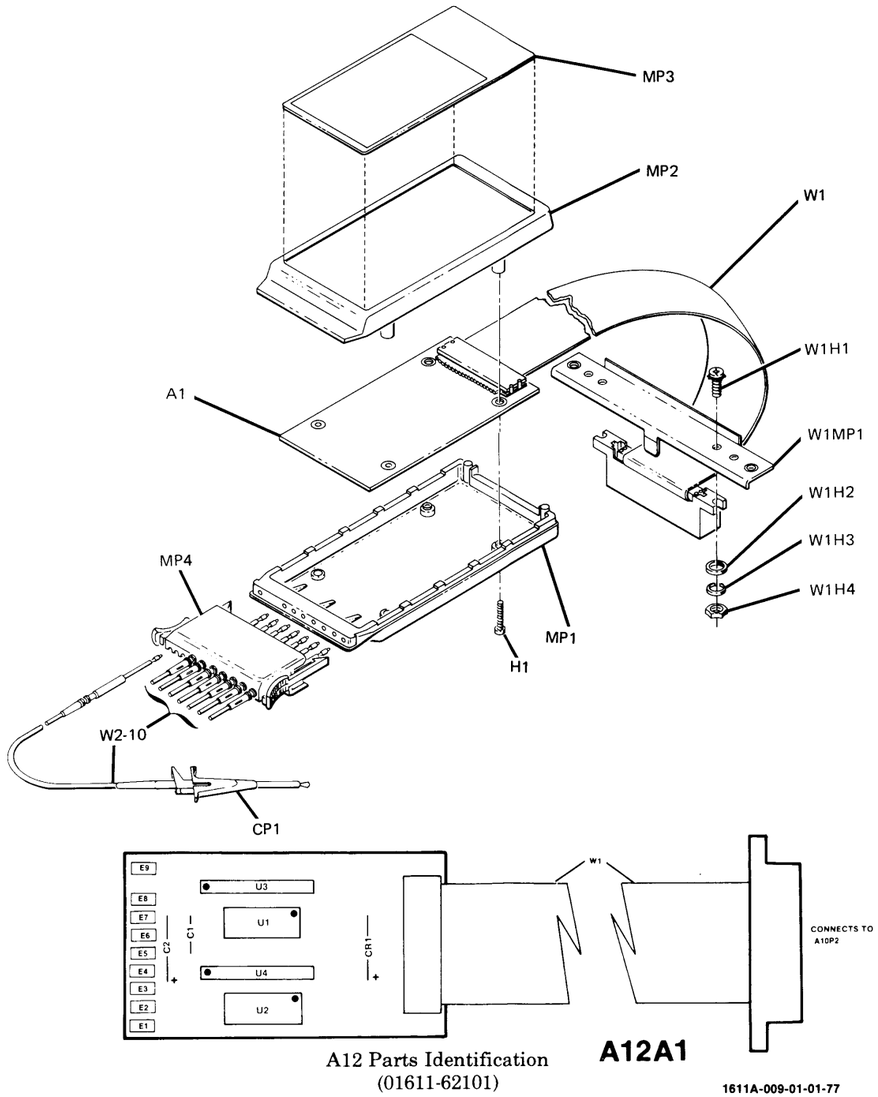
SERVICE SHEET 9

PRINCIPLES OF OPERATION

The External Probe allows the 1611A to monitor up to eight circuit nodes in the system under test. Bus drivers U1 and U2 buffer the monitored signals to reduce loading on the circuit being monitored. RC networks U3 and U4 adjust timing of signals so they arrive at the External Latch on A10 at the proper time. The External Latch is clocked by PEXCK from A9.

ICs ON THIS SCHEMATIC

IC REF DES	HP PART NO.	MFR PART NO.
U1, 2 U3, 4	1820-1829 1810-0293	1820-1829 1810-0293



A12 Parts Identification
(01611-62101)

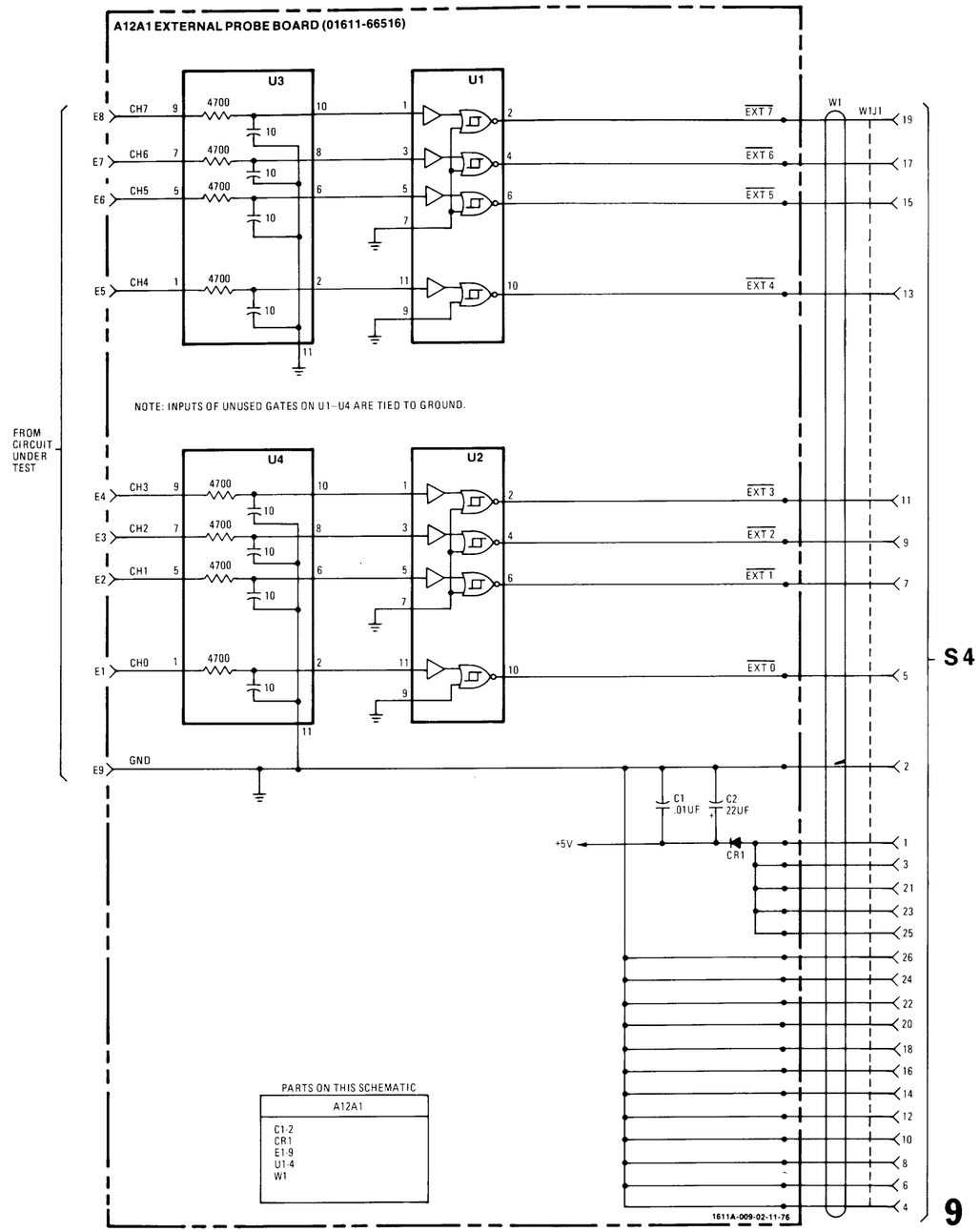


Figure 8-15. Service Sheet 9, External Probe Assembly A12

SERVICE NOTE

Supersedes:
None

HP MODEL 1611A LOGIC STATE ANALYZER

Serial Prefix 1635A and Below

+5 VOLT SUPPLY FUSE FAILURE

The +5 Volt fuse A2F3 (HP Part Number 2110-0029) may fail when the above instruments are operated in a high ambient temperature. The problem can be eliminated by changing the fuse to a 4 amp SLO-BLO (HP Part Number 2110-0014).

DH/rw/WO

7-77/08

Part Number
5955-2771

HEWLETT PACKARD

For more information, call your local HP Sales Office or nearest Regional Office: Eastern (301) 258-2000; Midwestern (312) 255-9800; Southern (404) 955-1500; Western (213) 877-1282; Canadian (416) 678-9430. Ask the operator for Instrument Sales. Or, Write: Hewlett-Packard, 1501 Page Mill Road, Palo Alto, CA 94304. In Europe: Hewlett-Packard S.A., 7, rue du Bois-du-Lan, P.O. Box CH-1217 Meyrin 2, Geneva, Switzerland. In Japan: Yokogawa-Hewlett-Packard Ltd., 29-21, Takaido-Higashi 3-chome, Suginami-ku, Tokyo, 168.

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S E R V I C E N O

Supersedes:
None

HP MODEL 1611A LOGIC STATE ANALYZER

Serial Numbers 1723A00590 and Below

POWER SUPPLY CURRENT LIMIT MODIFICATION

The current limiting circuit in the above instruments may not operate properly when used with any option other than 080 or 068. An annoying audible sound may result. The problem can be eliminated by changing A2R15 (HP Part Number 0811-1758) .24Ω to .18Ω (HP Part Number 0811-2771).

Materials required for this modification:

1 0811-2771 .18Ω 3 watt resistor

DH/rw/WO

7-77/08

Part Number
5955-2772

HEWLETT PACKARD

For more information, call your local HP Sales Office or nearest Regional Office: Eastern (301) 258-2000; Midwestern (312) 255-9800; Southern (404) 955-1500; Western (213) 877-1282; Canadian (416) 678-9430. Ask the operator for Instrument Sales. Or, Write: Hewlett-Packard, 1501 Page Mill Road, Palo Alto, CA 94304. In Europe: Hewlett-Packard S.A., 7, rue du Bois-du-Lan, P.O. Box CH-1217 Meyrin 2, Geneva, Switzerland. In Japan: Yokogawa-Hewlett-Packard Ltd., 29-21, Takaido-Higashi 3-chome, Suginami-ku, Tokyo, 168.

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SERVICE NOTE

Supersedes:

None

HP MODEL 1611A LOGIC STATE ANALYZER

Serial Numbers 1723A00696 and below

TRACE POINT OUTPUT CORRECTION

The trace point output on the rear panel of the 1611A has incorrect pulse width when some values of after-trigger delay are specified. This problem can be corrected by adding the signal NCNT (from A8U32) to the input of NAND gate A8U12.

Material required:

1 - 74S133 IC, HP Part No. 1820-1130

1 - 16 pin IC socket, HP Part No. 1200-0507

1 - Insulated jumper wire, approx 7cm (2 3/4 in.) long

INSTALLATION PROCEDURE

1. Remove the A8 assembly (01611-66508/66535) and locate A8U12.
2. Cut the trace between +5 volts and A8U12 pin 3 (See figure 1).
3. Remove A8U12 and install the IC socket.
4. Install the jumper wire as shown in figure 1.
5. Install the new A8U12 (1820-1130) in the socket.

Recalibration is not required. Update schematics in the 1611A manual as shown in figure 2.

DH/mc/WO

12/77-08

5955-4123

HEWLETT PACKARD

For more information, call your local HP Sales Office or nearest Regional Office: Eastern (301) 258-2000; Midwestern (312) 255-9800; Southern (404) 955-1500; Western (213) 877-1282; Canadian (416) 678-9430. Ask the operator for Instrument Sales. Or, Write: Hewlett-Packard, 1501 Page Mill Road, Palo Alto, CA 94304. In Europe: Hewlett-Packard S.A., 7, rue du Bois-du-Lan, P.O. Box CH-1217 Meyrin 2, Geneva, Switzerland. In Japan: Yokogawa-Hewlett-Packard Ltd., 29-21, Takaido-Higashi 3-chome, Suginami-ku, Tokyo, 168.

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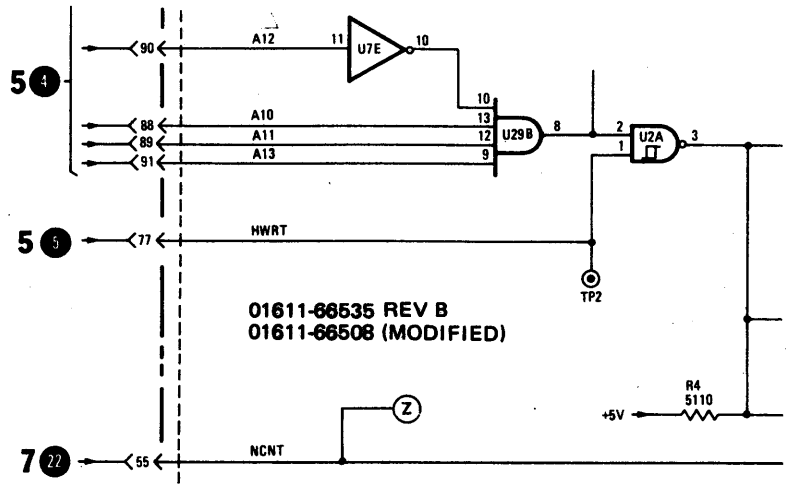
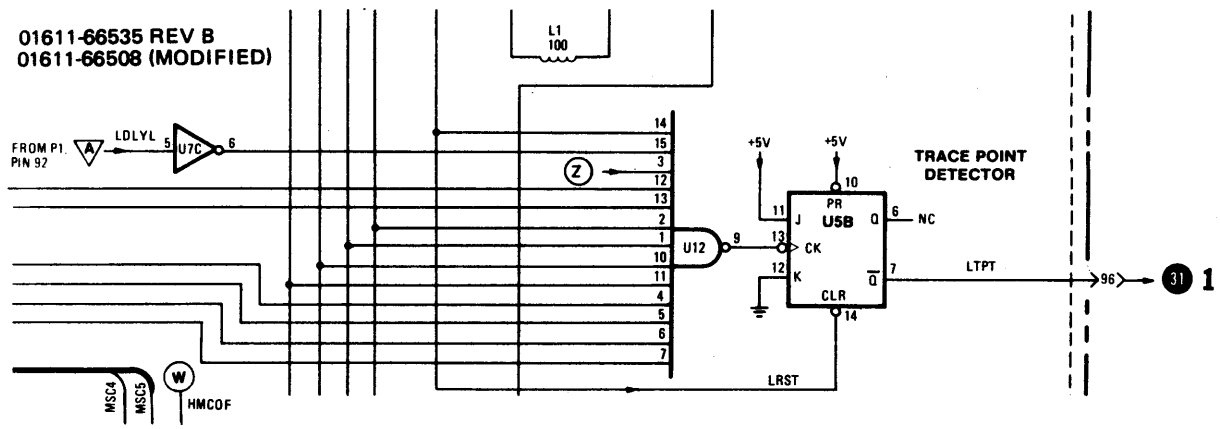


(SCHEMATIC 8, SHEET 2 OF 6)



(SCHEMATIC 8, SHEET 4 OF 6)

Figure 2. Updated Schematics.

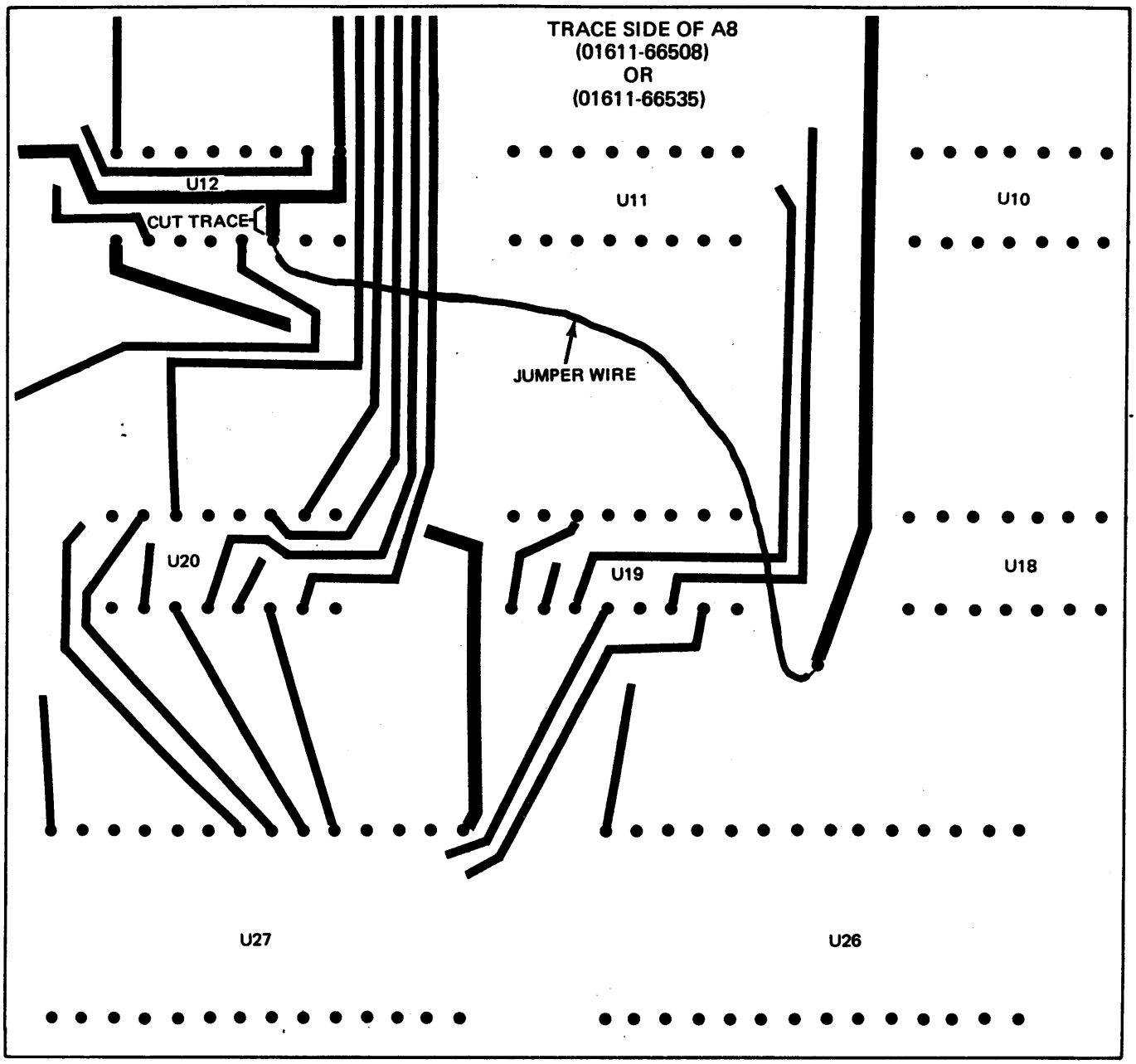

TRACE SIDE OF A8
(01611-66508)
OR
(01611-66535)
U12
CUT TRACE
U11
U10
JUMPER WIRE
U20
U19
U18
U27
U26

Figure 1.

01611-90909

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