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User's Guide

HP E2412A
Intel i860XP
Preprocessor Interface

HP E2412A Intel i860XP Preprocessor Interface User's Guide

for the HP 1660A, HP 16540/16541A,D, and HP 16550A Logic Analyzers

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Chapter 3: General Information

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Introduction

The HP E2412A Preprocessor Interface provides a complete interface for state analysis between any i860XP target system and an HP 1660A, HP 16540/16541A,D, or HP 16550A Logic Analyzer.

The i860XP configuration software on the flexible disk sets up the format specification menu of the logic analyzer for compatibility with the i860XP microprocessor. It also loads the inverse assembler for obtaining displays of i860XP data in i860XP assembly language mnemonics.

HP 16500A Software Compatibility

The HP E2412A Preprocessor Interface requires HP 16500A system and module software version V04.01 or higher. If your software version is older than V04.01, load new HP 16500A system software version number V04.01 or higher before loading the HP E2412A software.

Logic Analyzers Supported

The following logic analyzers are supported by the HP E2412A Preprocessor Interface:

HP 1660A

The HP 1660A Logic Analyzer provides 4 k of memory depth with 136 channels of 100 MHz state analysis or 250 MHz timing analysis. This logic analyzer also supports various combinations of mixed state/timing analysis.

HP 16540A,D with three HP 16541A,D Expansion Cards

This logic analyzer combination provides 4 k of memory depth (16 k with the D version) with 160 channels of 100 MHz state or timing analysis.

HP 16550A (two cards)

This logic analyzer provides 4 k of memory depth with 102 channels per card of 100 MHz state analysis or 250 MHz timing analysis. The logic analyzer will also support various combinations of mixed state/timing analysis.

How to Use This Manual

This manual is organized into three chapters and one appendix:

- Chapter 1 explains how to install and configure the HP E2412A Preprocessor Interface for state analysis with the supported logic analyzers.
- Chapter 2 provides reference information on the format specification and symbols configured by the HP E2412A software. It also provides information about the inverse assembler and status encoding.
- Chapter 3 contains additional reference information including the characteristics and signal mapping for the HP E2412A Preprocessor Interface. It also contains information on troubleshooting and servicing.
- Appendix A contains information on troubleshooting problems or difficulties which may occur with the preprocessor interface.

1 Setting Up the HP E2412A

Introduction

This chapter explains how to install and configure the HP E2412A Preprocessor Interface for state analysis with the HP 1660A, HP 16540/16541A,D, or HP 16550A Logic Analyzer.

Duplicating the Master Disk

Before you use the HP E2412A software, use the Duplicate Disk operation in the disk menu of your logic analyzer to make a duplicate copy of the HP E2412A master disk. Store the master disk and use the back-up copy to configure your logic analyzer. This will help prevent the possibility of losing or destroying the original files in the event the disk wears out, is damaged, or a file is accidentally deleted.

Accessories Supplied

The HP E2412A Preprocessor Interface consists of the following accessories:

- The preprocessor interface hardware, which includes the preprocessor circuit card and cables.
- The inverse assembly software on a 3.5-inch disk.
- Nine 100 kOhm Termination Modules (HP part number 01650-63204).
- Two jumpers (HP part number 1258-0261) for designating the Endian mode and State-Per-Clock mode.
- This user's guide.

Note

The preprocessor interface socket assembly pins are covered at the time of shipment with either a conductive foam wafer or a conductive plastic pin protector. This is done to protect the delicate gold plated pins of the assembly from damage due to impact.

When you're not using the preprocessor interface, protect the socket assembly pins from damage by covering them with the foam or plastic pin protector.

Minimum Equipment Required

The minimum hardware for state analysis of an i860XP target system consists of the following equipment:

- An HP 1660A, an HP 16540A,D with three HP 16541A,D Expansion Cards, or an HP 16550A (two cards).
- The HP E2412A Preprocessor Interface and Inverse Assembler.

Installation Quick Reference

The following procedure describes the major steps required to perform measurements with the HP E2412A Preprocessor Interface. The page numbers listed in the various steps refer you to sections in this manual that offer more detailed information.

Caution

To prevent equipment damage, be sure to remove power from both the logic analyzer and the target system whenever the preprocessor interface or microprocessor is being connected or disconnected.

1. Connect the 100 kOhm Termination Modules to the cables on the preprocessor interface (see page 1-4).
2. Install the preprocessor interface in the target system (page 1-5).
3. Connect the logic analyzer probes to the termination modules on the cable connectors of the preprocessor interface board as listed in table 1-1 (see page 1-7).
4. Load the logic analyzer configuration file (see page 1-9).
5. If you want to fully capture the execution trace, disable the cache memory. If possible, you may also want to disable address translation, so the physical addresses the preprocessor interface monitors are effectively the logical addresses (see page 1-6).

Note

If you leave the cache enabled, all data will still be captured and decoded but you may lose prefetch flagging for identifying the execution trace. An enabled cache will allow you to view all data coming across the bus, although some of the execution trace information will be lost.

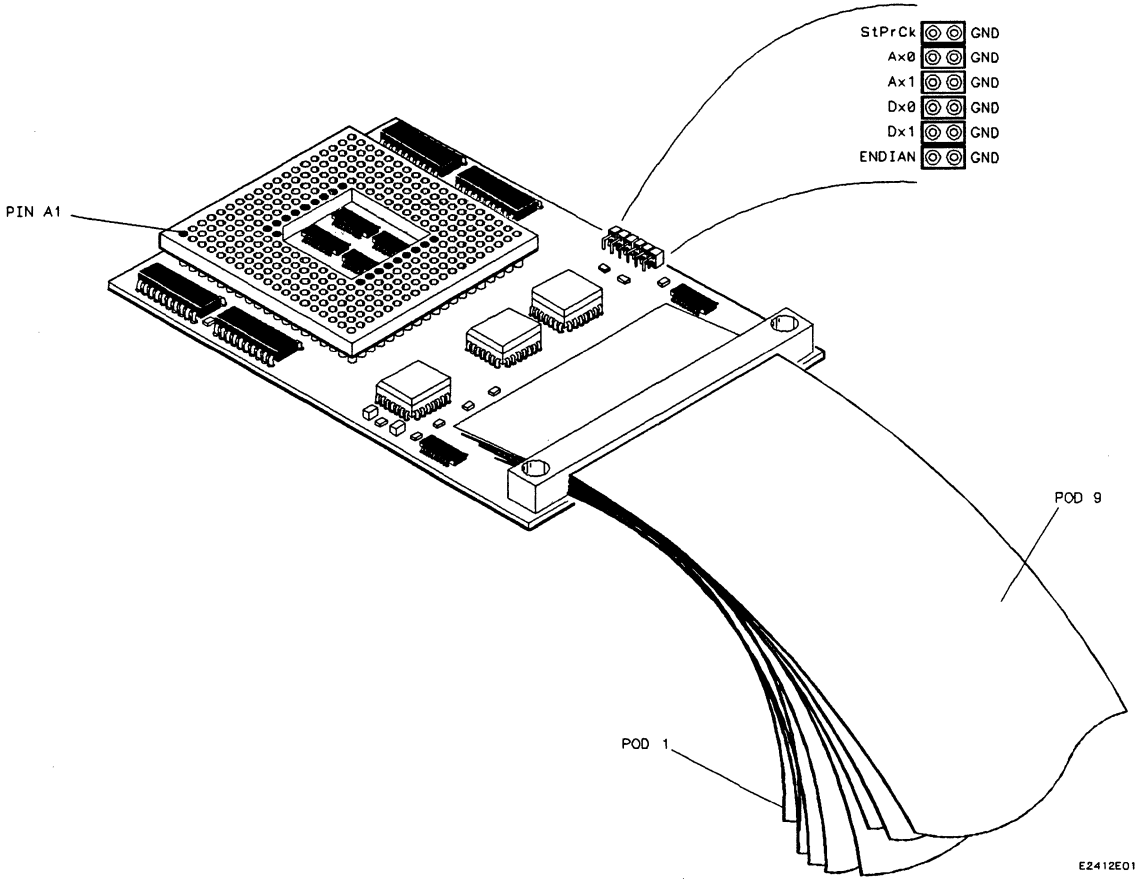

Figure 1-1. Preprocessor Interface Assembly

Connecting the Termination Module to the Preprocessor Interface

The 100 kOhm Termination Module (HP part number 01650-63204) properly terminates the logic analyzer probes. The following steps explain how to connect the termination module to the cables on the HP E2412A Preprocessor Interface:

1. Align the key on the end of the termination module with the slot on the connector of one of the preprocessor interface cables (see figure 1-2).
2. Push the termination module into the connector.
3. Repeat steps 1 and 2 for each termination module.

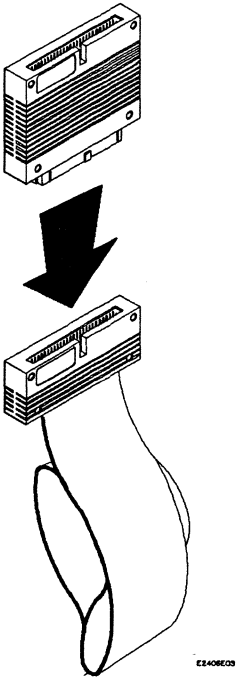

Figure 1-2. Connecting the Termination Module

Connecting to the Target System

The following steps explain how to connect the HP E2412A Preprocessor Interface to your target system:

Caution

To prevent equipment damage, be sure to remove power from both the logic analyzer and the target system whenever the preprocessor interface or microprocessor is being connected or disconnected.

1. Remove the i860XP microprocessor from its socket on the target system and store it in a protected environment.

Caution

Serious damage to the target system or preprocessor interface can result from incorrect connection. Note the position of pin A1 (figure 1-1) on the preprocessor interface connector and the target system socket prior to inserting the connector in the socket. Also, take care to align the preprocessor interface connector with the socket on the target system so that all microprocessor pins are making contact.

2. Plug the preprocessor interface connector into the microprocessor socket on the target system.

Note

If the preprocessor interface connector interferes with components of the target system or if a higher profile is required, additional plastic pin guards can be added. Plastic pin guards can be ordered from Hewlett-Packard using the part number 1200-1678. However, any 262-pin PGA IC socket with an i860XP foot print and gold-plated pins can be used.

3. Plug the i860XP microprocessor into the socket of the preprocessor interface board. The socket on the preprocessor interface board is designed with low insertion force pins to allow you to install or remove the microprocessor with a minimum amount of force.

Caution 

Care must be used when removing a microprocessor or socket from the preprocessor interface board to prevent damaging the traces on the board.

4. If you want to fully capture the execution trace, disable the cache memory. If you leave the cache enabled, all data will still be captured and decoded but you may lose prefetch flagging for identifying the execution trace. An enabled cache will allow you to view all data coming across the bus, although some of the execution trace information will be lost. The cache can be disabled by setting the CD bits in the page table entries to "1."
5. If possible, you may want to disable address translation so that the physical addresses the preprocessor interface monitors are effectively the logical addresses. Address translation can be disabled by setting the ATE bit (bit 0) of the directory base register to zero.

Power Up / Down Sequence

Once the logic analyzer and target system are connected to the preprocessor interface (see next page), the proper power up / down sequence must be observed. When powering up, the logic analyzer must be powered up first, and then the target system. The logic analyzer provides the power to the active circuits on the preprocessor interface; unpowered circuits may cause improper operation of the target system or preprocessor interface.

When powering down, the target system should be powered down first, and then the logic analyzer.

Connecting to the HP E2412A

Connect the logic analyzer probes to the termination modules on the cable connectors of the preprocessor interface board as listed in table 1-1. Figure 1-3 shows the relative locations for the HP 16540/16541A,D and HP 16550A Logic Analyzer cards.

Table 1-1. Logic Analyzer Connections and Configuration Files

HP 16540/16541A,D Logic Analyzer Pod *	HP 16550A Logic Analyzer Pod **	HP 1660A Logic Analyzer Pod	(into) HP E2412A Connector
Master Card, Pod 1	Master Card, Pod 1	Pod 1	P1 (STAT) clk ↑
Exp. Card 3, Pod 1	Master Card, Pod 3	Pod 3	P2 (DATA)
Exp. Card 3, Pod 2	Master Card, Pod 4	Pod 4	P3 (DATA)
Exp. Card 3, Pod 3	Master Card, Pod 5	no connection	P4 (DP)
Exp. Card 2, Pod 1	Expander Card, Pod 3	Pod 5	P5 (DATA_B)
Exp. Card 2, Pod 2	Expander Card, Pod 4	Pod 6	P6 (DATA_B)
Exp. Card 2, Pod 3	Master Card, Pod 2	Pod 2	P7 (STAT)
Exp. Card 1, Pod 1	Expander Card, Pod 5	Pod 7	P8 (ADDR)
Exp. Card 1, Pod 2	Expander Card, Pod 6	Pod 8	P9 (ADDR)
	Configuration Files		
E_i860XP	F_i860XP	F_i860XP	

* For the HP 16541A,D cards, expansion card 1 is the physically highest HP 16541A,D card, expansion card 2 is the second physically highest HP 16541A,D card, and expansion card 3 is the third highest HP 16541A,D card (see fig. 1-3).

** For the HP 16550A cards, the Master Card is the lower card, and the expansion card is the higher card. Note that the two HP 16550A cards must be configured as a single logic analyzer.

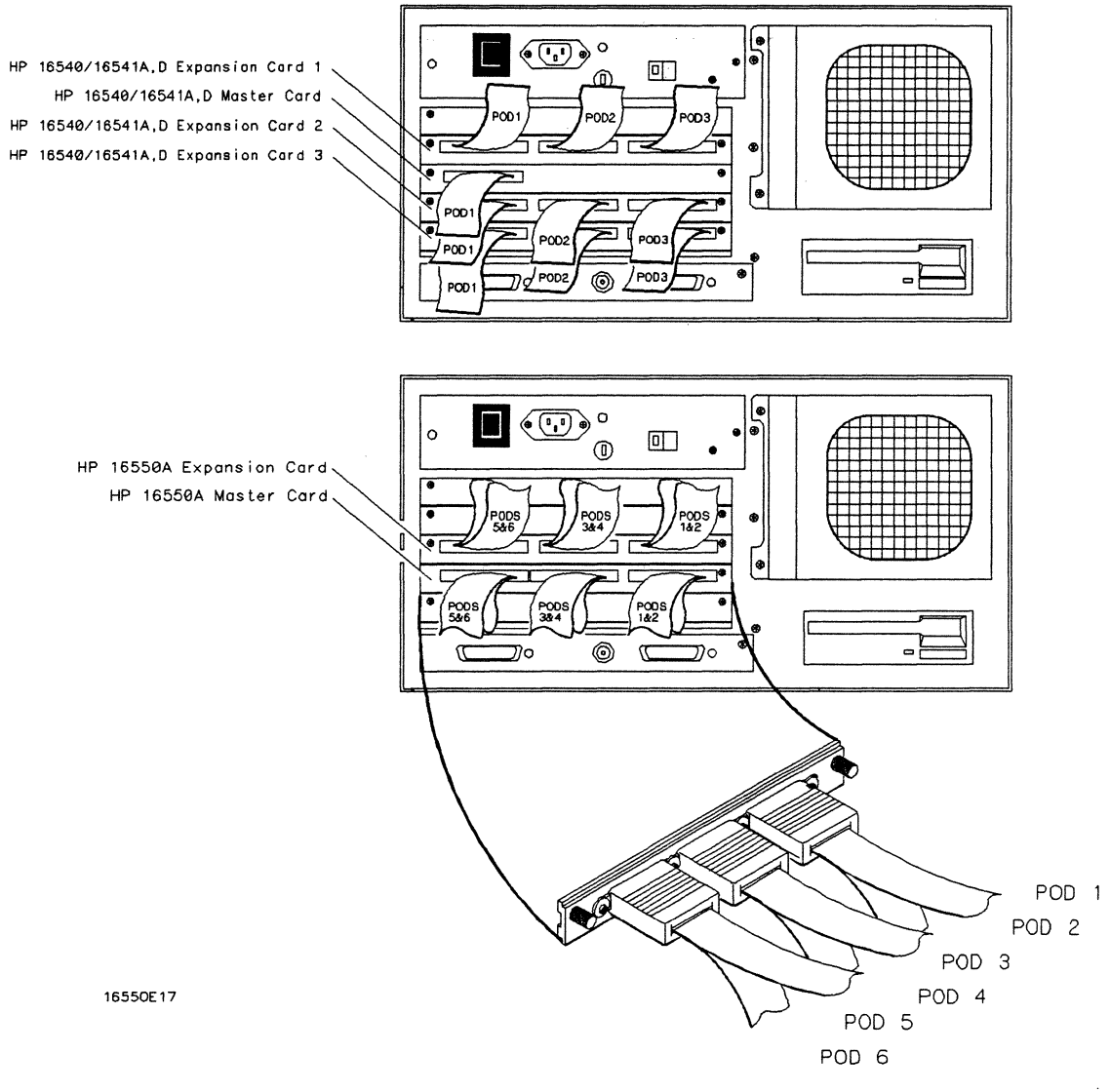

Figure 1-3. Logic Analyzer Card Locations
(relative locations, actual slots used can vary)

Setting Up the Analyzer from the Disk

The logic analyzer can be configured for i860XP analysis by loading the appropriate configuration file. Loading this file will also load the inverse assembler file. To load the configuration and inverse assembler:

1. Install the HP E2412A flexible disk in the front disk drive of the logic analyzer.
2. Select the System Front Disk menu.
3. Configure the menu to "Load" the analyzer configuration from disk.
4. Select the appropriate module (such as "100/500 MHz LA" or "Analyzer") for the load.
5. Use the knob to select the appropriate configuration file (see table 1-1).
6. Execute the load operation to load the file into the logic analyzer.

Connecting External Signals

The 12-pin connector on the preprocessor interface contains six ground pins and six connectors for external signals. Four of the connectors are for external signals to be monitored, one connector is for selecting the Endian mode, and one connector is for selecting State-Per-Clock mode (StPrCk). Figure 1-1 shows the connection points for these signals.

External Signals

You can monitor up to four additional signals from your target system with the preprocessor interface. These signals are called Ax0, Ax1, Dx0, and Dx1, and can be viewed in the Ax and Dx labels, respectively. Ax0 and Ax1 are latched with i860XP valid addresses, and Dx0 and Dx1 are latched with i860XP valid data; therefore, Ax and Dx signals must meet the same timing requirements as i860XP addresses and data.

Caution 

External signals must be TTL levels to avoid damage to the preprocessor interface.

Endian Mode Jumper

The Endian external signal selects whether the data will be interpreted as Big Endian or Little Endian mode. This signal is normally high to select Little Endian interpretation. If the signal is jumpered to ground it will be pulled low to select Big Endian mode. As an alternative, if an output such as from an address decoder dynamically changes state with the Endian mode, that signal can be connected to the Endian signal to indicate mode. The Endian signal is latched the same as i860XP valid data signals. See Chapter 2 for additional information on Endian mode.

State-Per-Clock (StPrCk) Mode

This signal is normally high, to clock the logic analyzer when data is valid. If the signal is jumpered to ground, it will be pulled low to select State-Per-Clock mode. In State-Per-Clock mode, the logic analyzer is clocked on every CLK rising edge, regardless of whether or not a valid data transfer occurs. Inverse assembly is not available when the preprocessor interface is in State-Per-Clock mode.

When the jumpers are not being used, they can be jumpered across two ground pins for safekeeping.

2

Analyzing the Intel i860XP

Introduction

This chapter provides reference information on the format specification and symbols configured by the HP E2412A software. It also provides information about the inverse assembler and status encoding.

Format Specification

When you use the HP E2412A Preprocessor Interface, the format specification set up by the software will look like that shown in figures 2-1, 2-2 and 2-3.

Table 3-1 in chapter 3 lists the i860XP signals for the HP E2412A Preprocessor Interface and their corresponding lines to the logic analyzer.

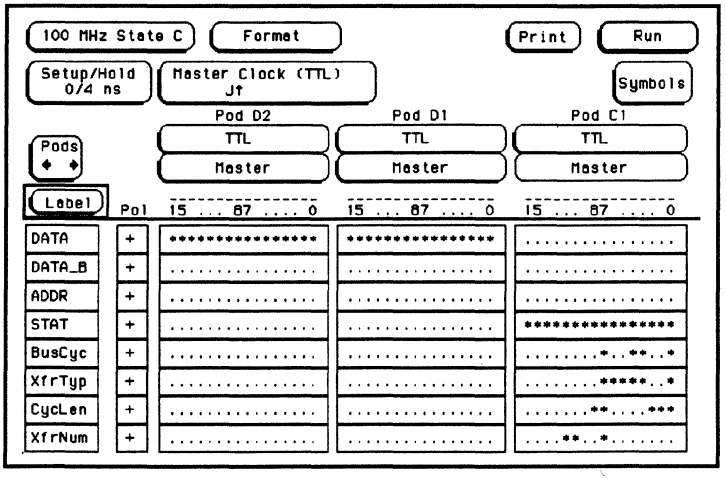

Figure 2-1. Format Specification (Pods 1 - 3)

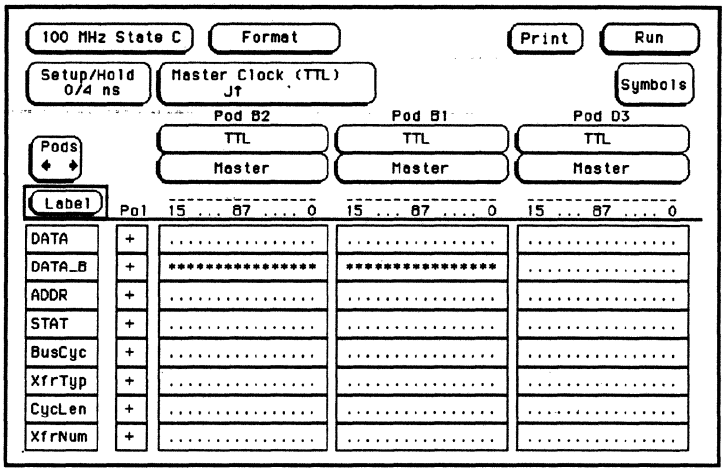

Figure 2-2. Format Specification (Pods 4 - 6)

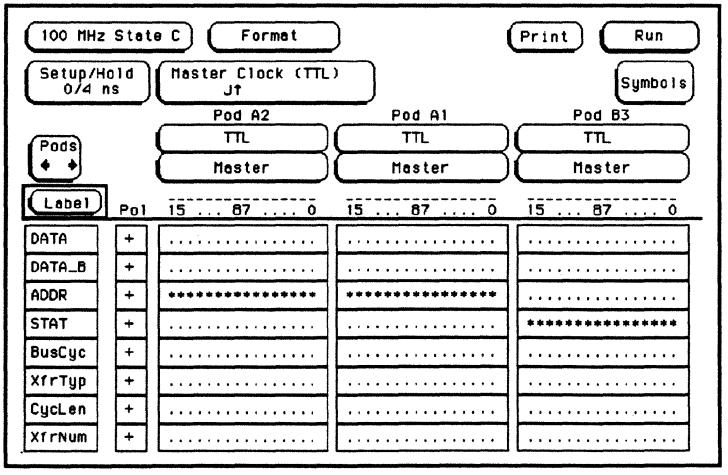

Figure 2-3. Format Specification (Pods 7 - 9)

Note

The Setup/Hold time must remain in the current setting (0 s setup/4 ns hold for the HP 16540/16541A,D, 0 s setup/3.5 ns hold for the HP 1660A and HP 16550A) for proper operation with the HP E2412A.

Symbols

The configuration files set up symbol tables on the logic analyzer. The tables contain alphanumeric values which identify data patterns or ranges.

Table 2-1 lists the bits assigned to the STAT label. Table 2-2 lists the symbols for all labels except BE#. Table 2-3 lists the symbols for BE#. The patterns for each symbol listed in the tables are shown in the binary base. In the actual software, these patterns may be listed in the hexadecimal base to conserve display space.

Table 2-1. STAT Label Bits

Bit	Status Signals	Description
0	W/R#	This signal is high for a Write bus cycle and low for a Read.
1	LEN	This signal specifies the number of burst transfers for each cycle.
2	CACHE#	This signal indicates whether a bus request is internally cacheable.
3	M/IO#	This signal is high for memory address space and low for IO address space.
4	D/C#	This signal is high for data requests and low for instruction requests
5	CTYP	This signal is one of the data transfer type signals.
6	PCYC	This signal is high for page table accesses and low for other type accesses
7	*InqCyc (EADS#)	This signal is generated by the preprocessor interface. A low indicates that the current transfer is an inquire cycle.
8	KEN#	This signal indicates whether a bus request is externally cacheable.

*When the preprocessor interface is in State-Per-Clock mode, this signal is replaced with EADS#.

Table 2-2. STAT Label Bits (Continued)

Bit	Status Signals	Description
9	WB/WT#	This signal indicates the cache policy for the line being accessed in the current bus cycle. A high indicates a write-back and a low indicates a write-through.
10 - 11	*BQ0 - BQ1 (BRDY#, BRDYC#)	These signals are generated by the preprocessor interface to indicate the transfer number of a burst cycle. See the XfrNum Symbol Table for patterns and definitions.
12	HIT#	This signal is low if the previous inquiry cycle hit a valid cache line.
13	HITM#	This signal is low if the previous inquiry cycle hit a modified cache line.
14	HLDA	This signal is high when the microprocessor has granted bus access to another bus master.
15	BERR	This signal is high when a bus error or other urgent circumstances require immediate attention.
16 - 23	BE0# - BE7#	These signals indicate which byte(s) of the 64-bit data word are valid.
24	PWT	This signal provides a write back/write through indication on a page-by-page basis.
25	PCD	This signal provides a cacheability indication on a page-by-page basis.
26	INV	This signal is high to invalidate the cache line status for an inquiry hit.
27 - 30	Ax0, Ax1, Dx0, Dx1 (external signals)	These are external signals which the user can connect. Refer to Chapter 1 for further information.
31	Endian	This is an external signal set by the user to indicate the Endian mode. It is high for Little Endian and low for Big Endian. Refer to Chapter 1 for further information.

*When the preprocessor interface is in State-Per-Clock mode, these signals are replaced with BRDY# and BRDYC#.

Label Description

The following descriptions apply to the labels listed in table 2-2. In some cases, the labels contain information which is generated by the preprocessor interface.

Those labels marked with an asterisk are not valid when the preprocessor interface is in State-Per-Clock mode. In State-Per-Clock mode, the AhInOc, InqCyc, BQ0, and BQ1 signals are replaced with ADS#, EADS#, BRDY#, and BRDYC#. The labels with an asterisk contain one or more of the signals which are replaced in State-Per-Clock mode.

***BusCyc** Describes the type of bus cycle.

***XfrTyp** Describes the data transfer type if the bus cycle is a data read or write.

***CycLen** Length (number of transfers) of a burst cycle. This number remains constant throughout the cycle.

***XfrNum** The number of the transfer within a burst cycle. This number will start at the same number as CycLen, and decrement to 1.

***AdrOut** The number of outstanding (pipelined) addresses at the time of the transfer.

***BofInq** Back Off Inquire. This label shows the results of a BOFF-initiated inquire cycle.

***AhdInq** AHOLD Inquire. Flags whether or not an AHOLD-initiated inquire cycle occurred sometime between the current state and the previous state.

***WB/WT#** Described in table 2-1.

***PWT** Described in table 2-1.

***PCD** Described in table 2-1.

Endian Described in table 2-1.

BE# Described in table 2-1.

Table 2-2. HP E2412A Symbols

Label	Symbol	Pattern
BusCyc	IntAck	1000
	SpcCyc	1001
	I/O Rd	1100
	I/O Wr	1101
	CodeRd	1010
	Resrvd	1011
	Mem Rd	1110
	Mem Wr	1111
	(blank)	0xxx
XfrTyp	Norm Rd	100110
	Pipe Ld	101110
	PgDirRd	110110
	PgTblRd	111110
	WrThru	100111
	WrBack	101111
	PgDirWr	110111
	PgTblWr	111111
	(blank)	(other patterns)
CycLen	1	x1100
	1	11x00
	1	x110x
	2	x1110
	2	11x10
	2	x1111
	4	010x0
	4	x10x1
	(blank)	x0xxx
XfrNum	4	011
	3	111
	2	101
	1	001
	(blank)	xx0

Table 2-2. HP E2412A Symbols (Continued)

Label	Symbol	Pattern
AdrOut	0 1 2 (blank)	1 1 1 1 0 1 0 1 1 (other patterns)
BofInq	Hit Inval Miss (blank)	0 0 0 1 0 0 x 1 0 x x 1
AhdInq	Occurred (blank)	1 0
WB/WT#	WrBack WrThru (blank)	1 1 0 1 x 0
PWT	WrThru WrBack (blank)	1 1 0 1 x 0
PCD	Disabled Enabled (blank)	1 1 0 1 x 0
Endian	Little Big	1 0

Table 2-3. BE# (Byte Enable) Symbols

Label	Symbol	Pattern
BE# (Little Endian)	b0 ltl	111111110
	b1 ltl	111111101
	b2 ltl	111111011
	b3 ltl	111110111
	b4 ltl	111101111
	b5 ltl	111011111
	b6 ltl	110111111
	b7 ltl	101111111
	s0 ltl	111111100
	s2 ltl	111110011
	s4 ltl	111001111
	s6 ltl	100111111
	l0 ltl	111110000
	l4 ltl	100001111
	dbl	x00000000
BE# (Big Endian)	b0 big	001111111
	b1 big	010111111
	b2 big	011011111
	b3 big	011101111
	b4 big	011110111
	b5 big	011111011
	b6 big	011111101
	b7 big	011111110
	s0 big	000111111
	s2 big	011001111
	s4 big	011110011
	s6 big	011111100
	l0 big	000001111
	l4 big	011110000
	(blank)	(other patterns)

Listing Menu

Captured data is displayed as shown in figures 2-4 and 2-5. Figure 2-4 shows CS8 mode cycles after disassembly. Figure 2-5 displays the state listing for 64-bit bus cycles after disassembly. The inverse assembler is constructed so the mnemonic output closely resembles the actual assembly source code.

The logic analyzers always probe the full 64-bit data bus of the i860XP. When fewer than the full 64 bits of the data bus are used by a memory cycle, the inverse assembler marks the bytes not used by the microprocessor with "--."

Since the data bus is 64 bits and the display is only 32 bits (hex) wide, the inverse assembler marks the data as <lsw> or <msw> for least or most significant word. However, this designation also depends on the Endian mode (see "Endian Mode" under Inverse Assembler).

When the i860XP is running in the dual instruction mode, concurrently executed instructions are marked with the prefix "d".

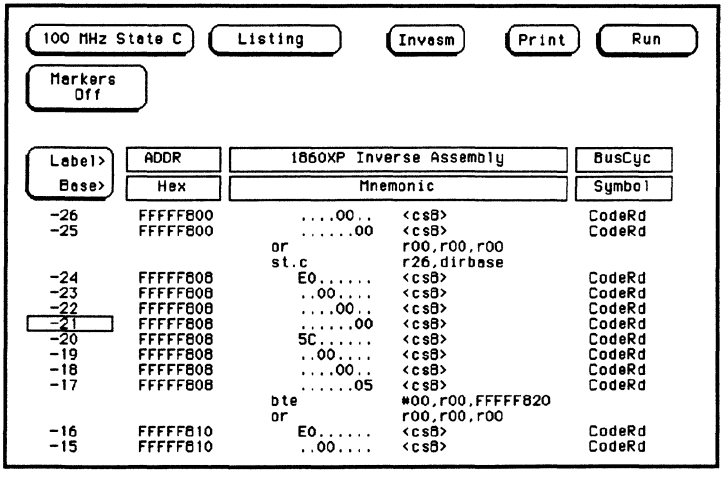

Figure 2-4. State Listing (CS8 Mode)

Burst Data

The logic analyzer can trace one-, two-, and four-cycle burst transfers. During burst transfers the microprocessor holds the address constant during the entire burst. The inverse assembler listing displays the two least significant hexadecimal digits of the actual address at the left side of the column.

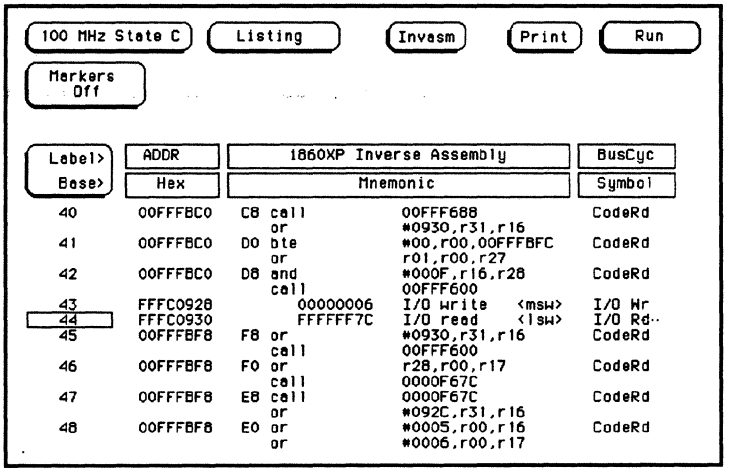

Figure 2-5. State Listing (Burst)

The i860XP Inverse Assembler

The i860XP Inverse Assembler analyzes the microprocessor code and disassembles it into i860XP mnemonics, which are displayed on the logic analyzer screen. Unexecuted prefetches are captured and flagged. Some assembler pseudo-operations are handled. In addition, the HP E2412A can be set for Little Endian or Big Endian mode, so that the inverse assembler displays the data in physical or logical order.

Inverse assembly is not available when the preprocessor interface is operating in State-Per-Clock mode.

Prefetched Instructions

The i860XP microprocessor is a prefetching microprocessor. That is, it may fetch up to the next eight instruction words (up to four 64-bit code fetches) while the last opcode is still being executed. When a program executes an instruction that causes a branch, the prefetched words are not used and will be discarded by the microprocessor. The inverse assembler marks unused prefetches with an asterisk "*".

The logic analyzer captures prefetches, even if they are not executed. Therefore, care must be taken when you are specifying a trigger condition or a storage qualification and the instruction of interest follows an instruction that may cause branching. An unused prefetch may generate an unwanted trigger.

Since the microprocessor may prefetch up to eight long words, one technique to avoid unwanted triggering from unused prefetches is to add "20 hex" (32 decimal) to the trigger address. This trigger condition will only be satisfied if the branch is not taken.

The i860XP has a pipeline depth of essentially eight long words. This means that by the time a branching instruction is fully decoded, up to eight other instruction words may have already been prefetched across the data bus, and stored in the logic analyzer. Both exceptions and instructions can cause the pipeline to be flushed and subsequently refilled. Branches, jumps, calls, and returns are the most common causes of pipeline flushes, but there are many others. Refer to your i860XP user's manual for more information.

When the i860XP is operating in a full 64-bit environment, two instructions (32 bits each) will be fetched on one bus cycle. When this happens, the instructions will be displayed on separate lines.

Synchronizing the Inverse Assembler

In some cases the prefetch flagging algorithm in the inverse assembler may lose synchronization, and prefetches or executed instructions may be incorrectly flagged. If you suspect that the inverse assembler has lost synchronization, re-syncronize the inverse assembler by pointing to an executed instruction. Once synchronized, the inverse assembler will disassemble from this state through the end of the screen. To point to an executed instruction:

1. Select a line on the display that you know contains an executed instruction, and that is also the least significant word (D31 - D0).
2. Roll this line to the top of the listing.

Note 

The cursor location is not the top of the listing. In figure 2-5, line 40 is the top of the listing.

---

3. Select the "Invasm" field at the top of the display. The listing will inverse assemble from the top line down. Any data before this screen is left unchanged.

Rolling the screen up will inverse assemble the lines as they appear on the bottom of the screen. If you jump to another area of the screen by entering a new line number, you may have to re-synchronize the inverse assembler by repeating steps 1 through 3.

Each time you inverse assemble a block of memory, the analyzer will keep that block in the inverse assembled condition. You can inverse assemble several different blocks in the analyzer memory, but the activity between those blocks will not be inverse assembled.

Assembler Pseudo-Operations

The only pseudo-operations handled by the inverse assembler are **nop** and **fnop**. The opcode "shl r0, r0, r0" is displayed as nop; the opcode "shrd r0, r0, r0" is displayed as fnop. Other assembler pseudo-operations, such as "shl r0, isrc2, idest," are displayed exactly as they occur.

Error Messages

The following list of messages will help you identify operation errors.

reserved The inverse assembler is unable to decode the opcode. The data is displayed along with the error message.

-------- No Byte Enables (BE#) are asserted

Note

Do not modify the ADDR, DATA, DATA_B, or STAT labels in the format specification if you want inverse assembly. Changes may cause incorrect results. Also note that if the trace specification is modified to store only selected bus cycles, incorrect or incomplete inverse assembly may result.

Endian Mode

The HP E2412A is set to interpret and display data in Little Endian mode. The Big Endian mode can be selected with a jumper, or an external signal can dynamically change Endian mode (see "Connecting External Signals" in Chapter 1).

The inverse assembler uses the Endian mode to interpret the Byte Enable signals correctly for data transfers of 32 bits or less, and to display the data in the order of its significance. Accesses of 64 and 128 data bits are not affected by the Endian mode, since they are always in Little Endian mode. Instruction accesses are also not affected, since they are always in Little Endian mode.

When the HP E2412A is in Little Endian mode, the inverse assembler always displays the data in the physical order as it appears on the bus, i.e., byte address 3 is on the left and byte address 0 is on the right. If the microprocessor and the HP E2412A are both in the same Endian mode, the inverse assembler displays the data in the logical order as it is used by the microprocessor. Logical order means the most significant word is left-justified, and the least significant word is right-justified, as it appears in the listing.

For the example listed in table 2-4, the 64-bit data PONMLKJIHGFEDCBA is located at an address stored in r0. Assume that this address is aligned on an eight-byte boundary. The following series of instructions are executed:

```
ld.s 0(r0), r16
ld.s 2(r0), r16
ld.s 4(r0), r16
ld.s 6(r0), r16
```

The example in table 2-4 shows the displays for Little and Big Endian data transfers with the four possible combinations of i860XP Endian mode and HP E2412A Endian mode. The microprocessor is transferring 16 data bits (four nibbles) per access. In box 1, both the physical order (bus transfer) and logical order (microprocessor operation) are displayed correctly. In box 2, the physical order is correct but the logical order is not. In box 3, neither the physical nor the logical order are correct; this combination should be avoided. In box 4, the physical order is incorrect but the logical order is correct.

For further information on the Endian mode, refer to the i860XP Reference Manual.

Table 2-4. Endian Mode

i860XP Mode	Data Transfer as it Occurs on Bus		Display – HP E2412A set to Little Endian		Display – HP E2412A set to Big Endian	
Little Endian	BE#	Data Bus	(1)		(3)	
	1:0	----------DCBA	----DCBA	<lsw>	DCBA----	<msw>
	3:2	--------HGFE----	HGFE----	<lsw>	----HGFE	<msw>
	5:4	----LKJI--------	----LKJI	<msw>	LKJI----	<lsw>
	7:6	PONM----------	PONM----	<msw>	----PONM	<lsw>
Big Endian	7:6	PONM----------	(2) PONM----	<msw>	(4) ----PONM	<lsw>
	5:4	----LKJI--------	----LKJI	<msw>	LKJI----	<lsw>
	3:2	--------HGFE----	HGFE----	<lsw>	----HGFE	<msw>
	1:0	----------DCBA	----DCBA	<lsw>	DCBA----	<msw>

Note

The Endian jumper on the HP E2412A does not affect the mode in which the microprocessor is operating. The jumper only affects how the inverse assembler displays the data.

State-Per-Clock Mode

The HP E2412A Preprocessor Interface normally clocks the logic analyzer on every CLK rising edge when valid data is on the bus. State-Per-Clock mode clocks the logic analyzer on every CLK rising edge regardless of whether or not valid transfers occur; therefore, every state which crosses the target system microprocessor's bus is captured. This allows the logic analyzer to capture wait states and idle states, in addition to valid data states.

When the logic analyzer is operating in State-Per-Clock mode, the Address and Status bits are captured following the assertion of ADS# or EADS#. Therefore, only valid addresses are captured in State-Per-Clock mode.

Since the Address and Status bits pass through two levels of latches on the preprocessor interface, they lag the data bits by one cycle. For further information, see "Interface Description" in Chapter 3.

Inverse assembly is not available when the preprocessor interface is operating in State-Per-Clock mode.

State Waveforms Using State-Per-Clock Mode

The State-Per-Clock mode can be used with the State Waveforms function of the logic analyzer to produce state timing diagrams. The horizontal axis displays state transitions rather than absolute time.

3 General Information

Introduction

This chapter contains additional reference information including the characteristics and signal mapping for the HP E2412A Preprocessor Interface.

Characteristics

The following operating characteristics are not specifications, but are typical operating characteristics for the HP E2412A Preprocessor Interface. These characteristics are included as additional information for the user.

Microprocessor Compatibility: Intel i860XP and all microprocessors made by other manufacturers that comply with Intel i860XP specifications.

Microprocessor Package: 262-pin PGA.

Accessories Required: None.

Maximum Clock Speed: 50 MHz CLK

Target Signal Timing: Meets all timing specifications in i860XP data book except the following:
10 ns setup for NA#
9 ns setup for BRDY# and KEN#
6 ns hold for A5 - A31 during BOFF#-initiated inquire cycles.

Signal Line Loading: One CMOS input plus 3 pF maximum on all lines except ADS#, HITM#, WB/WT#, and KEN#.
Two CMOS inputs plus 3 pF maximum on the ADS# line.
Three CMOS inputs plus 3 pF maximum on the HITM# line.
One CMOS input and one TTL input plus 3 pF maximum on the WB/WT# line.
Two CMOS inputs and one TTL input plus 3 pF maximum on the KEN# line.
One CMOS input plus 100 kOhm on Endian and StPrCk.

Power Requirements: 1.0 A at +5 Vdc maximum from the logic analyzer.

Logic Analyzer Required: HP 1660A, HP 16540A,D with three HP 16541A,D Expansion Cards, or HP 16550A (two cards).

Number of Probes Used: Nine 16-channel probes (eight for the HP 1660A Logic Analyzer).

Microprocessor Operations Displayed:

Interrupt Acknowledge
Special Cycle
I/O Read/Write
Code Read
Data Read/Write
- Normal Read
- Pipelined Load
- Page Directory Read/Write
- Page Table Read/Write
- Write Through
- Store Miss
- Write Back

Additional Capabilities: The logic analyzer captures all bus cycles, including prefetches. Unexecuted prefetches are marked with "*" (an asterisk).

The i860XP microprocessor must be operating with the internal cache memory disabled for the logic analyzer to provide correct inverse assembly. If the cache is left enabled, all data will still be captured and decoded but you may lose prefetch flagging for identifying the execution trace. An enabled cache allows you to view all data coming across the bus, although some of the execution trace information will be lost.

Environmental Temperature:

Operating:	0 to +55° C (+32 to +131° F)
Nonoperating:	-40 to +75° C (-40 to +167° F)

Altitude:

Operating:	4,600 m (15,000 ft)
Nonoperating:	15,300 m (50,000 ft)

Humidity: Up to 90% noncondensing. Avoid sudden, extreme temperature changes which could cause condensation within the instrument.

Interface Description

The primary function of a preprocessor interface is to connect the target microprocessor to the logic analyzer through the probe interface, and to perform any functions unique to that particular microprocessor. The HP E2412A Preprocessor Interface performs this primary function in the following ways:

- By latching and buffering the addresses, address status, data, and data status of the i860XP microprocessor so that address, status, and data can be sent to the logic analyzer at the same time.
- By generating the logic analyzer clocks from the appropriate i860XP microprocessor signals and bus conditions.

The preprocessor interface has two separate methods for latching and storing information. The Sample Flip-Flops latch and store data and the status signals which follow data timing. The Address/Status Pipeline Registers latch and store addresses and the status signals which follow address timing. The contents of the Address/Status Pipeline Registers are later relatched into the Sample Flip-Flops (sometimes several cycles later), so that the appropriate addresses, data, and status are sent to the logic analyzer at the same time (see figure 3-1).

The Sample Flip-Flops are latched on every rising CLK edge, to capture data/status and information released by the Address/Status Pipeline registers. The Address/Status Pipeline Registers are latched, stored, and released by clocks generated by the Control/Clocking PALs. The Control/Clocking PALs ensure that address, data, and status are aligned for all possible permutations of memory pipeline depth and burst transfers.

The preprocessor interface also provides some support for cache snooping. The Control/Clocking PALs provide the necessary timing and logic. BOFF#-initiated inquiry cycles are completely supported, while AHOLD- and HOLD-initiated cycles are partially supported. For BOFF#-initiated inquiry cycles, all snooped addresses are captured, and if a writeback is triggered it is also captured. AHOLD- and HOLD-initiated cache writebacks are captured; if no cache writeback occurs, the logic analyzer will indicate that an AHOLD-inquire cycle occurred, but will not provide the inquiry address or any further information.

There is a separate pipeline register for KEN# and WB/WT#, which is also controlled by the Control/Clocking PALs. KEN# is identified as a piped version or a real-time version, and the appropriate one is selected by the KEN/WBWT Mux. The appropriate version of WB/WT# is also selected by the KEN/WBWT Mux. Memory pipelining and burst transfers are therefore transparent, since data and addresses are always sent to the logic analyzer as one valid sample.

All signals which feed the Sample Flip-Flops directly are real time versions. All signals which feed the Address/Status Pipeline Registers are piped (as opposed to real-time) versions.

State-Per-Clock Mode

When the preprocessor interface is in State-Per-Clock mode, the Control/Clocking PALs hold the Pipeline Registers at a depth of one level, so that the registers function like normal flip flops. The 53 signals which pass through the Address/Status Pipeline Registers are delayed by one clock cycle (logic analyzer state). Since the Address/Status Pipeline Registers are loaded by ADS# or EADS#, one of those signals must be asserted to capture information, even in State-Per-Clock mode.

The Control/Clocking PALs multiplex four signals (AhInOc, InqCyc, BR0, and BR1). In State-Per-Clock mode, these signals are replaced with ADS#, EADS#, BRDY#, and BRDYC#.

Clocking

The Control/Clocking PALs monitor the i860XP bus activity and generate clocks for the following purposes:

- Control clocks for the Address/Status Pipeline Registers, so that addresses/status from memory pipelines and burst transfers are aligned with the proper data and clocked into the Sample Flip-Flops.
- Control clocks for the KEN/WBWT Pipeline Registers, so that the appropriate versions of KEN# and WB/WT# are sent to the KEN/WBWT Mux.
- CLK1 rising edges to clock BOFF#-initiated inquire-cycle addresses into the Sample Flip-Flops.
- CLK1 rising edges to clock valid addresses, status, and data to the logic analyzer. The same CLK1 clocks the contents of the KEN/WBWT Mux to the logic analyzer.

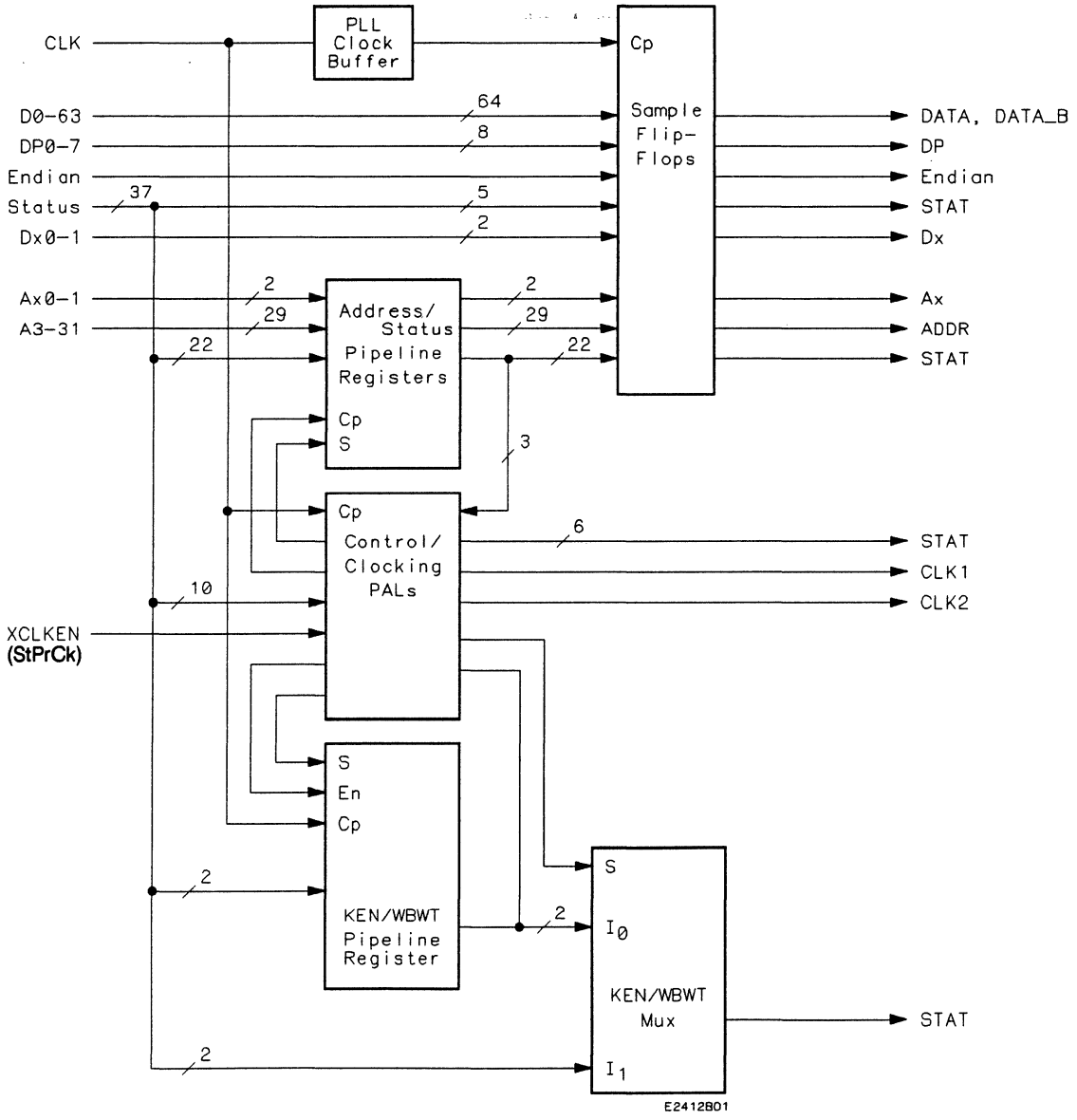

Figure 3-1. HP E2412A Block Diagram

i860XP Signal to HP E2412A Connector Mapping

The following table describes the electrical interconnections implemented with the HP E2412A Preprocessor Interface. Since the pods on the logic analyzers are numbered differently than the pods on the preprocessor interface, refer to table 1-1 to correlate the pod numbers.

Note

The interconnections implemented with the HP E2412A are not direct interconnections. The HP E2412A Preprocessor Interface places digital circuitry between the microprocessor pin and the logic analyzer.

Table 3-1. i860XP Signal List

Preprocessor Pod	Logic Analyzer Probe	i860XP Pin	Pin Mnemonic	Label(s)
P2	0	A7	D0	DATA
P2	1	D9	D1	DATA
P2	2	A13	D2	DATA
P2	3	A16	D3	DATA
P2	4	A17	D4	DATA
P2	5	D10	D5	DATA
P2	6	A18	D6	DATA
P2	7	C17	D7	DATA
P2	8	C16	D8	DATA
P2	9	B16	D9	DATA
P2	10	D11	D10	DATA
P2	11	B17	D11	DATA
P2	12	C15	D12	DATA
P2	13	B18	D13	DATA
P2	14	D12	D14	DATA
P2	15	B19	D15	DATA
P3	0	C18	D16	DATA
P3	1	D14	D17	DATA
P3	2	C19	D18	DATA
P3	3	D15	D19	DATA
P3	4	D16	D20	DATA
P3	5	E15	D21	DATA
P3	6	D19	D22	DATA
P3	7	E16	D23	DATA

Table 3-1. i860XP Signal List (Continued)

Preprocessor Pod	Logic Analyzer Probe	i860XP Pin	Pin Mnemonic	Label(s)
P3	8	F15	D24	DATA
P3	9	E17	D25	DATA
P3	10	F16	D26	DATA
P3	11	F19	D27	DATA
P3	12	G15	D28	DATA
P3	13	G19	D29	DATA
P3	14	G16	D30	DATA
P3	15	M19	D31	DATA
P4	0	A15	DP0	DP
P4	1	A19	DP1	DP
P4	2	D13	DP2	DP
P4	3	D18	DP3	DP
P4	4	Q19	DP4	DP
P4	5	J15	DP5	DP
P4	6	P16	DP6	DP
P4	7	N15	DP7	DP
P4	8	R8	PEN#	PEN#
P4	9	R11	**KB0	KB
P4	10	S10	**KB1	KB
P4	11	S11	**NENE#	NENE#
P4	12	S3	**LOCK#	LOCK#
P4	13	* (N4)	AhInOc (ADS#)	AhdInq
P4	14	*	AMux0	AdrOut
P4	15	*	AMux1	AdrOut

* These signals are generated by the preprocessor interface. In State-Per-Clock mode, the signals in parenthesis are sent to the logic analyzer.

** These signals are delayed one cycle in State-Per-Clock mode.

Table 3-1. i860XP Signal List (Continued)

Preprocessor Pod	Logic Analyzer Probe	i860XP Pin	Pin Mnemonic	Label(s)
P5	0	H15	D32	DATA_B
P5	1	R18	D33	DATA_B
P5	2	P19	D34	DATA_B
P5	3	R19	D35	DATA_B
P5	4	N19	D36	DATA_B
P5	5	S19	D37	DATA_B
P5	6	J16	D38	DATA_B
P5	7	T19	D39	DATA_B
P5	8	U19	D40	DATA_B
P5	9	L16	D41	DATA_B
P5	10	T18	D42	DATA_B
P5	11	K16	D43	DATA_B
P5	12	U18	D44	DATA_B
P5	13	K15	D45	DATA_B
P5	14	S17	D46	DATA_B
P5	15	M16	D47	DATA_B
P6	0	L15	D48	DATA_B
P6	1	T17	D49	DATA_B
P6	2	N16	D50	DATA_B
P6	3	U17	D51	DATA_B
P6	4	S18	D52	DATA_B
P6	5	M15	D53	DATA_B
P6	6	Q16	D54	DATA_B
P6	7	U16	D55	DATA_B

Table 3-1. i860XP Signal List (Continued)

Preprocessor Pod	Logic Analyzer Probe	i860XP Pin	Pin Mnemonic	Label(s)
P6	8	T16	D56	DATA_B
P6	9	R16	D57	DATA_B
P6	10	S16	D58	DATA_B
P6	11	P15	D59	DATA_B
P6	12	R15	D60	DATA_B
P6	13	Q15	D61	DATA_B
P6	14	S15	D62	DATA_B
P6	15	R14	D63	DATA_B
P1	0	T1	**W/R#	STAT, BusCyc, XfrTyp, CycLen
P1	1	T2	**LEN	STAT, CycLen
P1	2	Q4	**CACHE#	STAT, CycLen
P1	3	S4	**M/IO#	STAT, BusCyc, XfrTyp
P1	4	R5	**D/C#	STAT, BusCyc, XfrTyp
P1	5	P5	**CTYP	STAT, XfrTyp
P1	6	T4	**PCYC	STAT, XfrTyp
P1	7	* (S5)	InqCyc (EADS#)	STAT, BusCyc, XfrTyp, CycLen, XfrNum, AdrOut, BofInq, WB/WT#, PWT, PCD
P1	8	U2	KEN#	STAT, CycLen, AdrOut
P1	9	U4	WB/WT#	STAT, WB/WT#
P1	10	* (U1)	BQ0 (BRDY#)	STAT, XfrNum
P1	11	* (P4)	BQ1 (BRDYC#)	STAT, XfrNum
P1	12	S12	HIT#	STAT, BofInq
P1	13	N5	HITM#	STAT, HITM#
P1	14	S9	HLDA	STAT, HLDA
P1	15	S7	BERR	STAT, BERR

* These signals are generated by the preprocessor interface. In State-Per-Clock mode, the signals in parenthesis are sent to the logic analyzer.

** These signals are delayed one cycle in State-Per-Clock mode.

Table 3-1. i860XP Signal List (Continued)

Preprocessor Pod	Logic Analyzer Probe	i860XP Pin	Pin Mnemonic	Label(s)
P8	0	*	GND	ADDR
P8	1	*	GND	ADDR
P8	2	*	GND	ADDR
P8	3	S1	**A3	ADDR
P8	4	R1	**A4	ADDR
P8	5	M5	**A5	ADDR
P8	6	L5	**A6	ADDR
P8	7	F1	**A7	ADDR
P8	8	K5	**A8	ADDR
P8	9	E1	**A9	ADDR
P8	10	K4	**A10	ADDR
P8	11	D1	**A11	ADDR
P8	12	J4	**A12	ADDR
P8	13	C1	**A13	ADDR
P8	14	J5	**A14	ADDR
P8	15	B1	**A15	ADDR
P9	0	H4	**A16	ADDR
P9	1	A1	**A17	ADDR
P9	2	C3	**A18	ADDR
P9	3	C2	**A19	ADDR
P9	4	H5	**A20	ADDR
P9	5	B2	**A21	ADDR
P9	6	G4	**A22	ADDR
P9	7	A2	**A23	ADDR

* The following pins are grounds: B5, B8, B10, B12, B15, C6, C7, C8, C9, C10, C11, C12, C13, C14, D2, E2, E18, F3, F17, G3, G17, H2, H3, H17, H18, J3, J17, K2, K3, K17, K18, L3, L17, M2, M3, M17, M18, N3, N17, P3, P17, Q2, Q18, R2, T5, T6, T7, T8, T9, T10, T11, T12, T13, T14, and T15.

** These signals are delayed one cycle in State-Per-Clock mode.

Table 3-1. i860XP Signal List (Continued)

Preprocessor Pod	Logic Analyzer Probe	i860XP Pin	Pin Mnemonic	Label(s)
P9	8	B3	**A24	ADDR
P9	9	A3	**A25	ADDR
P9	10	G5	**A26	ADDR
P9	11	E4	**A27	ADDR
P9	12	F4	**A28	ADDR
P9	13	D4	**A29	ADDR
P9	14	F5	**A30	ADDR
P9	15	C4	**A31	ADDR
P7	0	E5	**BE0#	STAT, BE#
P7	1	D5	**BE1#	STAT, BE#
P7	2	D6	**BE2#	STAT, BE#
P7	3	B4	**BE3#	STAT, BE#
P7	4	C5	**BE4#	STAT, BE#
P7	5	A4	**BE5#	STAT, BE#
P7	6	D7	**BE6#	STAT, BE#
P7	7	A5	**BE7#	STAT, BE#
P7	8	T3	**PWT	STAT, PWT
P7	9	R6	**PCD	STAT, PCD
P7	10	R7	**INV	STAT, BofInq
P7	11	*	**Ax0	STAT, Ax
P7	12	*	**Ax1	STAT, Ax
P7	13	*	Dx0	STAT, Dx
P7	14	*	Dx1	STAT, Dx
P7	15	*	Endian	STAT, Endian, BE#

* These are external signals which the user can connect to the preprocessor interface (see Chapter 1).
** These signals are delayed one cycle in State-Per-Clock mode.

Table 3-1. i860XP Signal List (Continued)

Preprocessor Pod	Logic Analyzer Probe	i860XP Pin	Pin Mnemonic	Label(s)
P1	CLK1	M4	CLK	(logic analyzer clock)

Servicing

The repair strategy for the HP E2412A is board replacement. However, table 3-2 lists some mechanical parts that may be replaced if they are damaged or lost. Contact your nearest Hewlett-Packard Sales/Service Office for further information on servicing the board.

Exchange assemblies are available when a repairable assembly is returned to Hewlett-Packard. These assemblies have been set up on the "Exchange Assembly" program. This allows you to exchange a faulty assembly with one that has been repaired, calibrated, and performance verified by the factory. The cost is significantly less than that of a new assembly.

Table 3-2. Replaceable Parts

HP Part Number	Description
E2412-69501	Exchange Board/Cable Assembly
E2412-66501	Circuit Board/Cable Assembly
E2412-68703	Software Disk Pouch
01650-63204	Termination Module
1200-1678	Pin Protector
1258-0261	Jumper

Dimensions

Figure 3-2 lists the dimensions for the HP E2412A circuit board. The dimensions are listed in inches (millimeters).

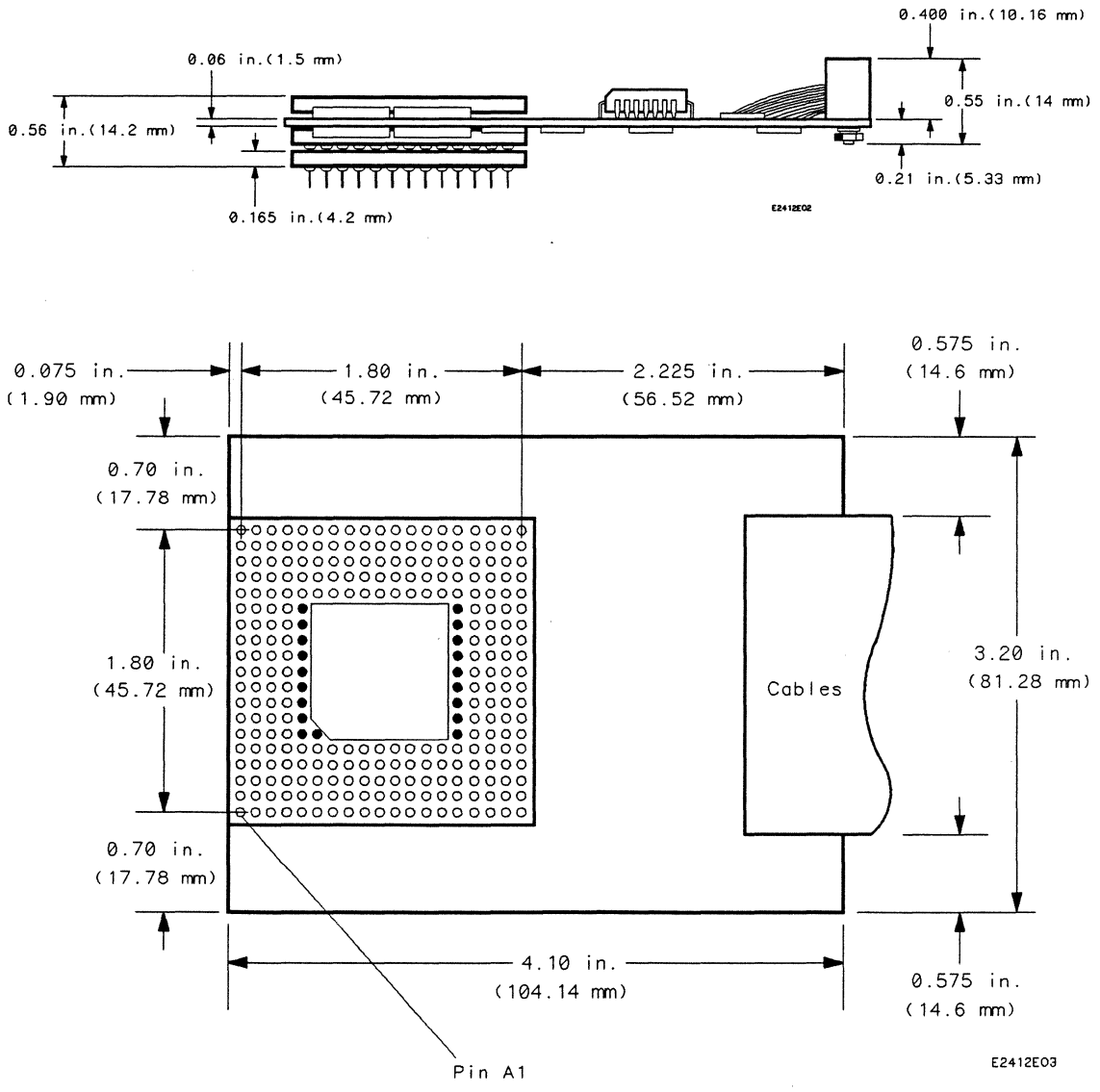

Figure 3-2. HP E2412A Dimensions - inches (mm)

A

Troubleshooting

If you encounter difficulties while making measurements, use this section to guide you through some possible solutions. Each heading lists a problem you may encounter, along with some possible solutions. Error messages which may appear on the logic analyzer are listed below in quotes " ". Symptoms are listed without quotes.

If you are still having difficulties after trying the suggestions below, please contact your local Hewlett-Packard service center for additional assistance.

Target Board Will Not Bootup

If the target board will not bootup after connecting the preprocessor interface, the microprocessor or the preprocessor interface may not be installed properly, or they may not be making electrical contact.

- Verify that the microprocessor and the preprocessor interface are properly rotated and aligned.
- Verify that the microprocessor and the preprocessor interface are securely inserted into their respective sockets.
- Verify that the logic analyzer cables are in the proper sockets of the preprocessor interface and firmly inserted.
- Reduce the number of extender sockets (see also "Capacitive Loading").

"Slow or Missing Clock"

This error message might occur if the logic analyzer cards are not firmly seated in the HP 16500A/16501A frame. Ensure that the cards are firmly seated.

This error might also occur if the target system is not running properly. Ensure that the target system is on and operating properly.

If the error message persists, check the that the logic analyzer pods are connected to the proper connectors, as listed in table 1-1.

No Activity on Activity Indicators

One of the cables, board connections, or preprocessor interface connections is probably loose. Check all connections.

Slow Clock

If you have the preprocessor interface hooked up and running and observe a slow clock or no activity from the interface board, the +5 V supply coming from the analyzer may not be getting to the interface board.

To check the +5 V supply coming from the analyzer, disconnect one of the logic analyzer cables from the HP E2412A and measure across pins 1 and 2 or pins 39 and 40 (see figure A-1).

- If +5 V isn't observed across these pins, check the internal preprocessor fuse or current limiting circuit on the logic analyzer. For information on checking this fuse or circuit, refer to the service manual for your logic analyzer.
- If +5 V is observed across these pins and you feel confident that the +5 V is getting to the preprocessor interface, contact your nearest Hewlett-Packard Sales/Service Office for information on servicing the board.

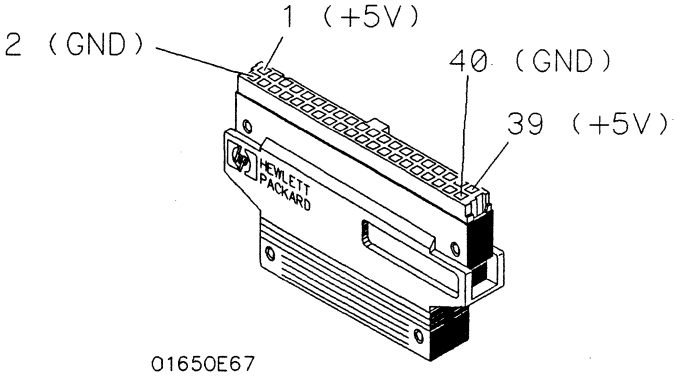

Figure A-1. Pinout of the Logic Analyzer Cable

"No Configuration File Loaded"

Verify that the appropriate module has been selected from the Load {module} from File {filename} in the HP 16500A disk operation menu. Selecting Load {All} will cause incorrect operation when loading most preprocessor interface configuration files.

"Selected File is Incompatible"

The logic analyzer displays this message if you try to load a configuration file for the wrong module. Ensure that you are loading the appropriate configuration file for your logic analyzer.

". . . Inverse Assembler Not Found"

This error occurs if you rename or delete the inverse assembler file that is attached to the configuration file. Ensure that the inverse assembler file is not renamed or deleted.

No Inverse Assembly

Verify that the inverse assembler has been synchronized by placing an opcode at the top of the display (not at the input cursor) and pressing the Invasm key (see "Inverse Assembler" in Chapter 2).

Incorrect Inverse Assembly

This problem is usually caused by a hardware problem in the target system. A locked status line will often cause incorrect or incomplete inverse assembly.

- Check the activity indicators for status lines locked in a high or low state.
- Verify that the STAT, DATA, and ADDR format labels have not been modified from their default values. These labels must remain as they are configured by the configuration file.
- Verify that all microprocessor caches and memory managers have been disabled. In most cases, if the microprocessor caches and memory managers remain enabled you should still get inverse assembly, but it may be incorrect since some of the execution trace was not visible to the logic analyzer.
- Verify that storage qualification has not excluded storage of all the needed opcodes and operands.

Unwanted Triggers

Unwanted triggers can be caused by unexecuted prefetches. Add the prefetch queue depth to the trigger address to avoid this problem.

"Waiting for Trigger"

If a trigger pattern is specified, this message indicates that the specified trigger pattern did not occur. Verify that the triggering pattern is correctly set.

Capacitive Loading

Excessive capacitive loading can cause signals to degrade, resulting in incorrect capture by the preprocessor interface or system lockup in the microprocessor. All preprocessor interfaces add additional capacitive loading. The following techniques will reduce the capacitive loading:

- Remove as many pin protectors, extenders, and adapters as possible.
- If multiple preprocessor interface solutions are available, try using one with lower capacitive loading.

Intermittent Data Errors

This problem is usually caused by incorrect signal levels. Adjust the threshold level of the data pod. Use an oscilloscope to check the signal integrity of the data lines, as needed.

Bent Pins

Bent pins on the preprocessor interface, pin protectors, or adapters can cause system errors or inverse assembly errors. Ensure all pins are properly aligned and making contact.

"Time from Arm Greater Than 41.93 ms."

The state/timing analyzers have a counter to keep track of the time from when an analyzer is armed to when it triggers. The width and clock rate of this counter allow it to count for up to 41.93 ms before it overflows. Once the counter has overflowed, the system does not have the data it needs to calculate the time between module triggers. The system must know this time to be able to display data from multiple modules on a single screen.

No Setup/Hold Field on Format Screen

The HP 16540/16541A,D Logic Analyzer cards are not calibrated. Refer to your logic analyzer reference manual for procedures to calibrate the cards.

"Default Calibration Factors Loaded" (16540/16541A,D)

The default calibration file for the logic analyzer was loaded. The logic analyzer must be calibrated when using HP 16540A,D and HP 16541A,D cards. Refer to your logic analyzer manual for procedures to calibrate the master clocking system, and ensure that the "cal factors" file is saved.

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