interface TECHNOLOGY

# RS-648

# TIMING SIMULATOR/WORD GENERATOR

# MAINTENANCE GUIDE

150 East Arrow Highway • San Dimas, California 91773 • (714) 599-0848 • TWX: 910-581-3847


TIMING SIMULATOR / WORD GENERATOR
MODEL RS-648
INTERFACE TECHNOLOGY
POWER
WORD PARAMETERS
LAST MEMORY ADDRESS
WORDS PER MEMORY WORD
WORDS PER LAST MEMORY WORD
LOAD
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MSEC
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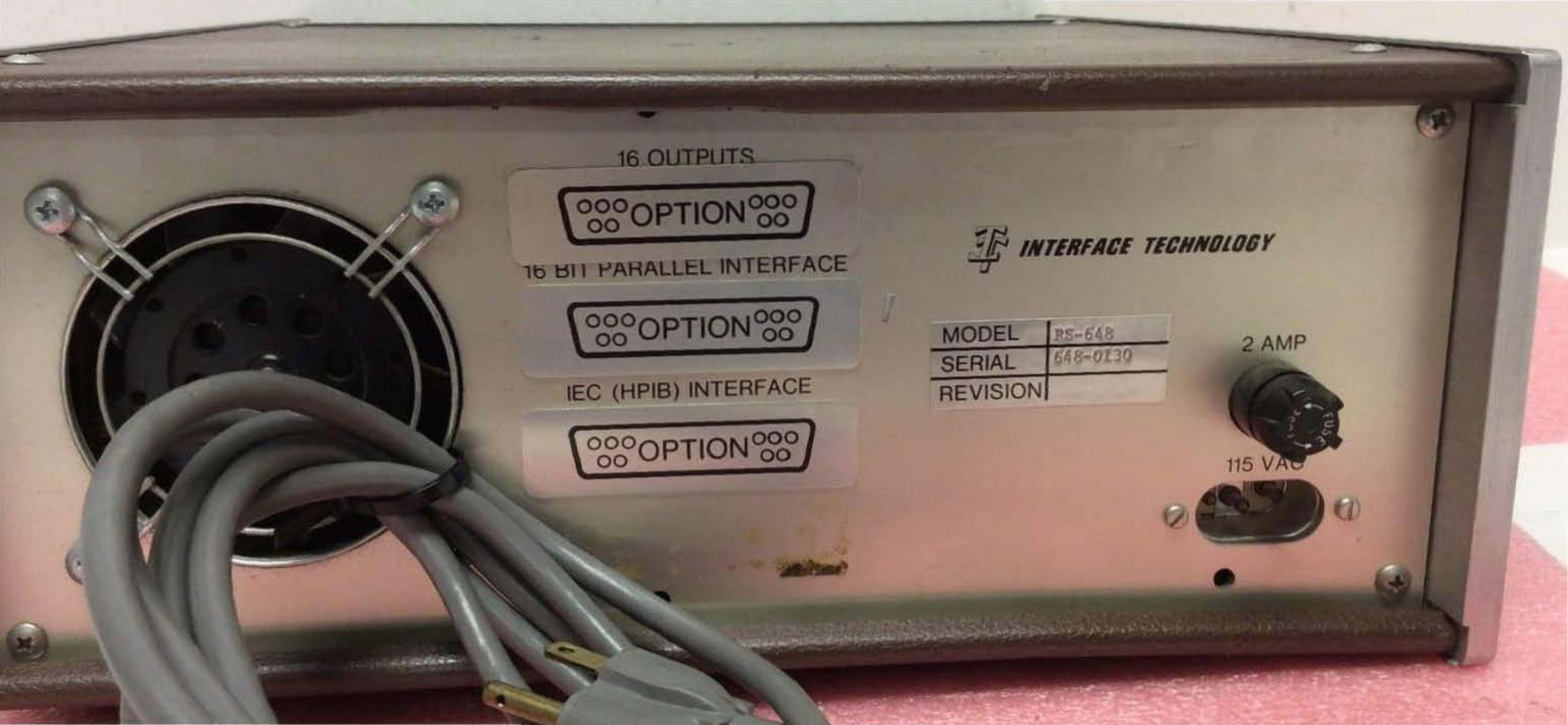
16 OUTPUTS
OPTION
16 BIT PARALLEL INTERFACE
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MODEL RS-648
SERIAL 648-0130
REVISION
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115 VAC

interface TECHNOLOGY

# RS-648

# TIMING SIMULATOR/WORD GENERATOR

# MAINTENANCE GUIDE

DOCUMENT CONTROL #648-MG-002



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CONTENTS

## GENERAL

The Timing Simulator/Word Generator Model RS-648 is a general purpose programmable digital signal generator. It is the first digital signal generator to allow independent control of time and output level data while using standard TTL circuitry for its implementation.

This Guide shall describe the physical characteristics of the RS-648, present the theory of operation, provide operation verification tests and also provide the logic and wiring diagrams which describe the RS-648. This Guide is intended to provide the basic information required to maintain the RS-648.

This Guide is written assuming that the reader is familiar with digital circuits, logic design and the Timing Simulator/ Word Generator Model RS-648 Users Guide (Document Control #648-UG-002).

## PHYSICAL DESCRIPTION

The RS-648 is packaged in a metal enclosure measuring 5¼"H x 12 3/4"W x 13"D. The top and bottom covers of this enclosure each slide off to the rear of the enclosure with the removal of 4 Phillips type screws. The side plates can also be removed, however, removal of these plates should only be necessary when full generator disassembly is required. The back panel holds the AC inlet, fuse, power supply and cooling fan. It is also used to mount connectors for the various generator options. The back panel is fastened to the enclosure by four screws and can be removed as a subassembly if required. Versions of the RS-648 which require ±15v power will also have this power supply mounted on the back panel.

CAUTION: Do not remove the back panel with the AC power plug in.

The front panel contains all RS-648 controls and indicators. It consists of a metal face plate and a printed circuit board which interconnects all the panel components. The front panel can also be removed as a subassembly. Note that interconnects made from the front panel to the logic panel via short cables with 28 pin connectors on both ends.

Inside the enclosure is a logic panel subassembly which consists of two sections. Section 1 contains 20 IC locations and two connectors. The connectors hold the expanded memory or ROM option cards. Section 2 contains 72 IC locations and cable connectors. The logic panel is wirewrapped to interconnect the IC's that comprise the RS-648. Power is distributed via power busses running the length of the logic panel.

Refer to Sheet 2 of drawing number 648-302 for a pictorial representation of the component side of the logic panel.

## THEORY OF OPERATION

This section discusses the theory of operation for both the Timing Simulator and Word Generator modes of the RS-648. It will first discuss the basic machine cycle for the two operating modes, then present a description of how the various mode, control, and parameter switches effect the machine operation.

Note that all page references in the following write-up are with reference to the Logic Block Diagrams drawing number 648-301 found in the DIAGRAMS section of this Guide.

## I. TIMING SIMULATOR MACHINE CYCLE (Reference Block Diagram 648-001, Timing Simulator Machine Cycle Flow Chart Figure 1, and the Logic Block Diagram).

This description assumes the following generator mode conditions:

1) Timing Simulator mode active.
2) Single Cycle not active.
3) Start Int active.

These generator mode conditions will cause the RS-648 to cycle indefinitely as defined by the Timing Simulator Machine Cycle Flow Chart Figure 1. Note that although Figure 1 depicts a sequential set of events, the RS-648 actually executes many of these events in parallel. This Flow Chart gives visual insight into the machine operation; it should be kept in mind when reading the following write-up.

The internal logic flow is best described with reference to the main clocks, CKCNT+ and CKCTA+ (Page 3). These clocks cause two parallel events to take place. First, CKCTA+ loads the OUTPUT SHIFT REGISTER (OSR01-, OSR02+, OSR03-, ..., and OSR16+ (Page 8)). The odd OUTPUT SHIFT REGISTER bits are routed via line drivers to the generator outputs. The even bits represent the TIMING REGISTER OSR02+, OSR04+ ...., and OSR16+ (Page 8). OTR16+ through OTR20+ (Page 10), and OTMRU+, OTMRN+ (Page 9)) are loaded with CKCNT+. Simultaneously, CKCNT+ increments the MEMORY ADDRESS COUNTER (WCNT1+ through WCNT6+ (Page 6)) in preparation for the next memory word.

At the same time that CKCTA+ loads the TIMING REGISTER, CNTOV- (Page 10) is resetting the TIMING COUNTERS (INCU1+ ...., INCT1+, ...., INCH1+ ..... (Page 10)).

Thereafter, the TIMING COUNTERS are enabled and begin the period timeout. TIMING REGISTER bits OTMRU+ and OTMRN+ (Page 9) select the basic time period of 1 msec, 1 usec, or 100 nsec by generating the TIMING COUNTER enable signal ENABL+ (Page 9). The TIMING COUNTERS are compared with the TIMING REGISTER which generates the compare signals MSBEQ+ and TSTEQ+ (Page 10). MSBEQ+, TSTEQ+ going true indicates the end of the timout period, and forces CNTOV- (Page 10) true which in turn forces ENINC+ true (Page 3). ENINC+ enables another main clock (CNCNT+ and CKCTA+) which again loads the OUTPUT SHIFT REGISTER, the TIMING REGISTER, and increments the MEMORY ADDRESS COUNTER.

The above sequence repeats until the MEMORY ADDRESS COUNTER equals the LAST MEMORY ADDRESS register and forces LAEWC+ (Page 6) true. LAEWC+ will force RSTCN- (Page 6) true which will cause the MEMORY ADDRESS COUNTER to reset to location zero on the next CKCNT+. The MEMORY ADDRESS COUNTER is again enabled to increment with each CKCNT+.

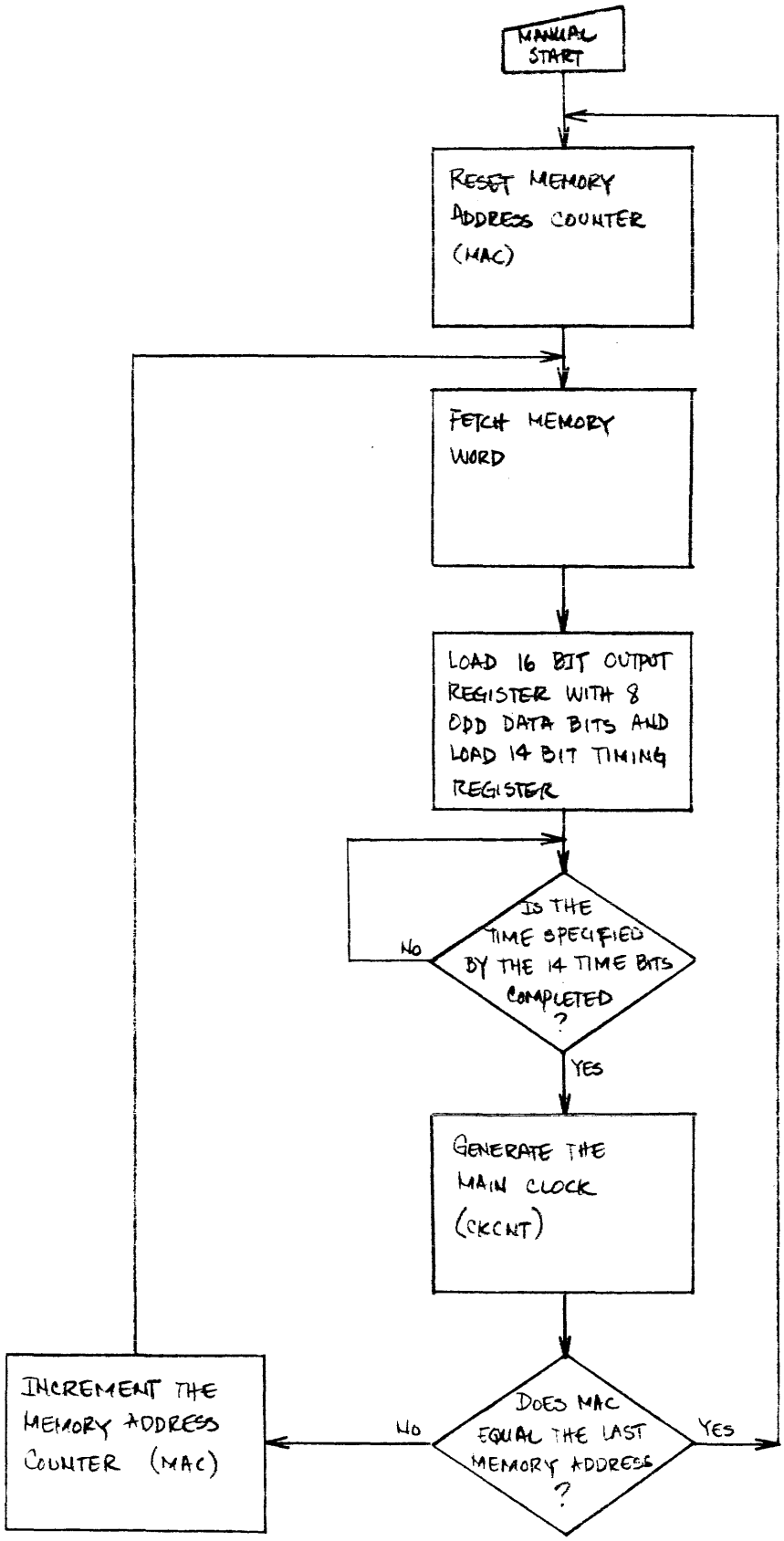



FIGURE 1

TIMING SIMULATOR MACHINE CYCLE FLOW CHART

Note that the TIMING COUNTERS are independently running, using CLOCK+ (Page 3), a 10 MHz signal, as the basic frequency source.

The above timing sequence is slightly altered by the decoding of a 50/50 NSEC time interval from ORMRN+ and OTMRU+. The time period for this memory access is forced to be 100 nsec. When this occurs the even numbered memory bits which normally defines time interval are now interpreted as data bits. Thus the OUTPUT SHIFT REGISTER is now a 16 bit word. This minimum time is forced by OTMRN+ and OTMRU+ being true, generating CNTOV- (Page 10). CNTOV- then enables another main clock (CKCNT+ and CKCTA+). This T5050+ signal also forces a 25 nsec pulse to occur 50 nsec after the leading edge of CKCNT+. This is accomplished by gating COBS3- (Page 3) and generating the signal CKCTA+ (Page 3).

Thus, CKCNT+ and CKCTA+ occur at the same time, however, CKCTA+ may have two pulses (if T5050+ is true) while CKCNT+ will have only one. The second pulse on CKCTA+ will force the OUTPUT SHIFT REGISTER to shift one bit (the nth bit to the n-1th bit). Thus, the even data bits in the OUTPUT SHIFT REGISTER (which normally contain timing information) define the second 50 nanosecond level of the respective output channel.

## II. WORD GENERATOR MACHINE CYCLE (Reference Block Diagram, 648-001, Word Generator Machine Cycle Flow Chart Figure 2, and the Logic Block Diagrams).

This description assumes the following generator mode conditions:

1) Word Generator mode active.
2) Single Cycle not active.
3) Start Int active.

These generator mode conditions cause the RS-648 to cycle indefinitely as defined by the Word Generator Machine Cycle Flow Chart, Figure 2. Note that although Figure 2 depicts a sequential set of events, the RS-648 actually executes many of these events in parallel. This Flow Chart gives visual insight into the machine operation; it should be kept in mind when reading the following write-up.

The internal logic flow is best described with reference to the main clock, CKCNT+ and CKCTA+ (Page 3). In the Word Generator mode CKCNT+ and CKCTA+ will always occur at the same time. These clocks cause two parallel events to take place. First, CKCTA+ loads the OUTPUT SHIFT REGISTER (OSR01-, OSR02+, OSR03-, .... OSR16+ (Page 8)) with a memory word that now contains output level data only (no time data as was the case for the Timing Simulator

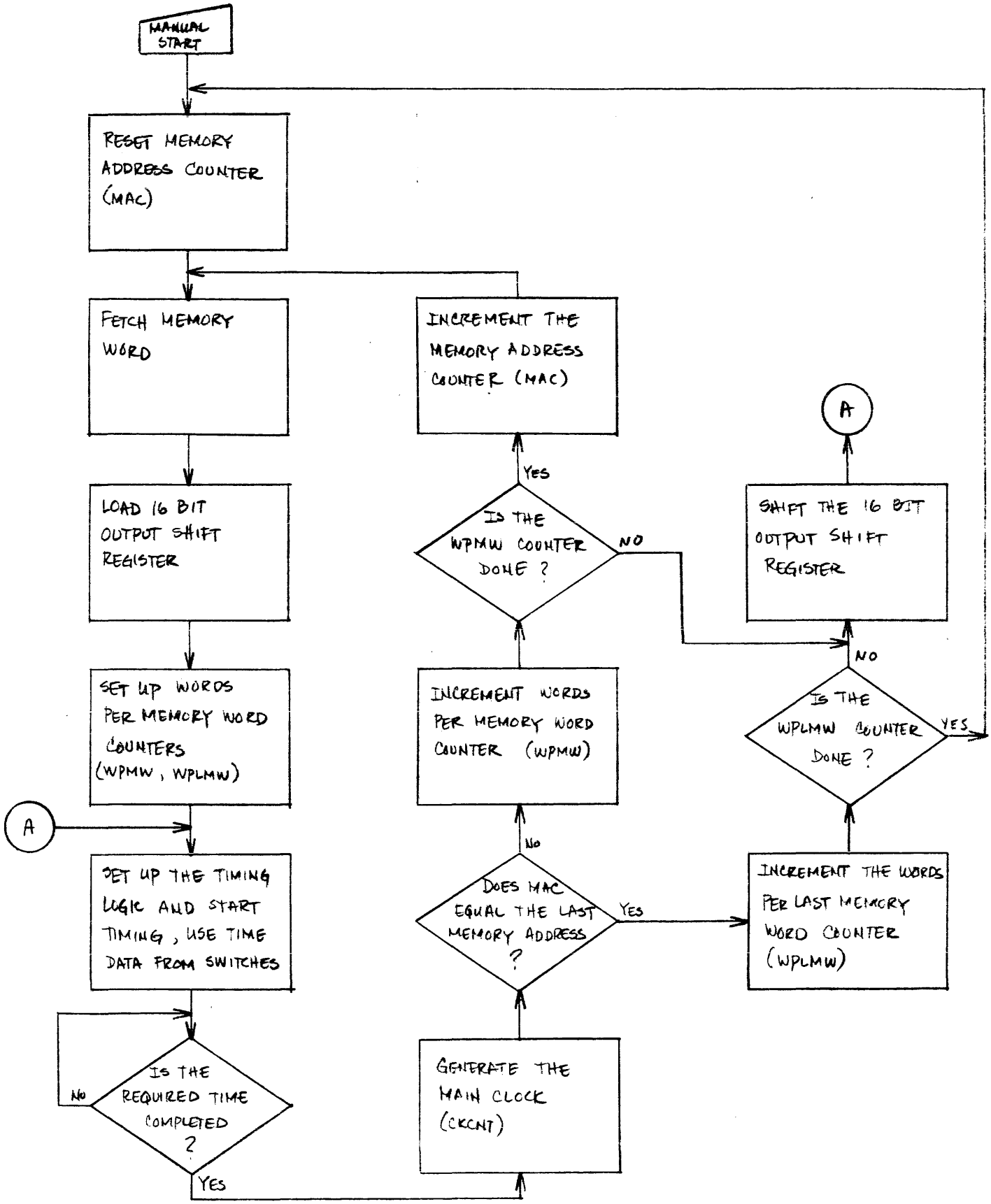



FIGURE 2

WORD GENERATOR MACHINE CYCLE FLOW CHART

mode). Simultaneously, CKCNT+ increments the MEMORY ADDRESS COUNTER (WCNT1+ through WCNT6+ (Page 6)) in preparation for the next memory word.

At the same time, CKCTA+ loads the OUTPUT SHIFT REGISTER, CNTOV- (Page 10) is resetting the TIMING COUNTERS (INCU1+ ...., INCT1+ ...., INCH1 .... (Page 10)). Thereafter, the TIMING COUNTERS are enabled and begin the period timeout. TIMING REGISTER bits OTMRU+ and OTMRN+ (Page 9) select a time period of 1 msec, 1 usec, or 100 nsec by generating TIMING COUNTER enable signal ENABL+ (Page 9). Note that in Word Generator mode ORMRU+ and OTMRN+ originate directly from the front panel thumbwheel switches and not from memory. Open collector NAND gates (Page 7) select SWTMU+ and SWTMN+ which come directly from front panel, to generate MEMDU- and MEMDN- (Page 7 and Page 9). The TIMING COUNTERS are compared with the front panel thumbwheel SWITCH data (SWU01+ ..., SWT01+ .... (Page 10)) to generate the compare signal for the units and tens digit. The TIMING COUNTER hundreds digit (INCH1+ ...) is compared with the TIMING REGISTER bits OTR17+ ..., OTR20+ (Page 10) for the hundred compare.

Note that in Word Generator mode these bits originate directly from the front panel thumbwheel switches. Open collector NAND gates (Page 7) select SWH01- through SWH08- (Page 7), which come directly from the front panel, to generate MMH01+ through MMH08+ (Page 7 and Page 9). When the units, tens, and hundreds compare is made, the compare signal WGTEQ+ (Page 10) is generated. WGTEQ+ forces CNTOV- (Page 10) true which in turn forces ENINC+ (Page 3) true. ENINC+ enables another main clock (CKCNT+ and CKCTA+) to be generated.

In Word Generator mode, unlike Timing Simulator mode, each main clock (CKCNT+ (Page 3 and Page 6)) does not always increment the MEMORY ADDRESS COUNTER. The MEMORY ADDRESS COUNTER requires the enable signal ENCNT+ (Page 5 and Page 6) in order to increment. ENCNT+ is generated from the WORDS PER MEMORY WORD and WORDS PER LAST MEMORY WORD counter (SHFC1+ through SHFC8+ (Page 5)). ENCNT+ performs three parallel functions. First, it enables the MEMORY ADDRESS COUNTER to increment. Second, it forces OSRSH- (Page 5 and Page 8) true which forces the OUTPUT SHIFT REGISTER (Page 8) to load 16 output level data bits from memory. Third, it feeds back and loads the WORDS PER MEMORY WORD counter (SHFC1+ through SHFC8+ (Page 5)) with data from either the WORDS PER MEMORY WORD register (WPMW1+ through WPMW8+ (Page 5) or the WORDS PER LAST MEMORY WORD register (WPLW+ through WPLW8+ (Page 5)) depending on the compare of the LAST MEMORY ADDRESS, LAEWC+ (Page 5 and Page 6)).

When a main clock (CKCNT+) is generated and ENCNT+ is not active, two parallel events take place. The OUTPUT SHIFT REGISTER (Page 8) is shifted one bit from the nth bit to the n-1th bit and the WORDS PER MEMORY WORD counter (SHFC1+ through SHFC8+ (Page 5)) is incremented.

## III. GENERATOR MODE SWITCH FUNCTIONS

TIMING SIM/WORD: This switch signal (TMSIM+) defines either Timing Simulator or Word Generator mode. TMSIM+ is true (high) in Timing Simulator mode and is inverted to generate WDGEN+ which is thus true (high) in Word Generator mode (Page 9). These signals make the following selections throughout the logic.

1) TMSIM+ (Page 5) high forces ENCNT- active in the Timing Simulator mode which in turn
   a) forces the MEMORY ADDRESS COUNTER to load at every main clock (CKCNT+, Page 6).
   b) forces the OUTPUT SHIFT REGISTER to load at every main clock.

   When TMSIM+ is low, the WORDS PER MEMORY WORD counter (SHFC1+ through SHFC8+ (Page 5)) is enabled.
2) TMSIM+ (Page 7) high forces WDGEN+ low which enables the period and hundreds timing data to be generated from memory. WDGEN+ (Page 7) high enables the period and hundreds timing data to be generated from the front panel thumbwheel switches.
3) WDGEN+ (Page 7) forces SELCT- true which selects, for input to memory, either the even numbered front panel switch data SWD02+, SWD04+, ...., SWD16+ (Page 7) in Word Generator mode or the units and tens thumbwheel time data (SWU08+, SWU04+, ...., SWT01+ (Page 7)) in Timing Simulator mode.
4) WDGEN (Page 9) low forces RSSYN+ high which forces a 50 nsec sync pulse in Timing Simulator mode.
5) TMSIM+ (Page 10) selects either the Timing Simulator (TSTEQ+) or Word Generator (WGTEQ) compare signal for the time period generation of CNTOV- (Page 10).

START INT/EXT: This switch enables either internal or external timing to sequence the RS-648. When in the off (center position), OFFSW- (Page 3) is low. This holds JK flip flop INTER+ (Page 3) reset which disables internal timing signal CNTOV+ (Page 3) from generating COBS5- (J3). OFFSW- also disables external timing signal EXCLK+ (Page c, gate 1-23).

In the START INT position, SINTM- (Page 3) is forced low (grounded at switch, reference 648-105 Front Panel Schematic Diagram) which in turn forces SETIN- low thus setting INTER+. INTER+ enables CNTOV+ via COBS5- (Page 3), which starts the internal timing.

When both OFFSW- and SINTM- are high, and SINGL- is low, this enables an external clock, EXCLK+ (Page 3) to generate EXCLA- (Page 3), which ten directly generates the two main clocks CKCNT+ and CKCTA+.

SINGLE CYCLE: When in Single Cycle, SINGL- is forced low which performs three gating functions. First, it disables the START INT function by inhibiting SETIN- (Page 3). Second, it disables the external clock function by inhibiting EXCLA- (Page 3). Third, it enables SETEC- (Page 3) which prepares for two functions. When the START INT/EXT switch is active (OFFSW- is high) and the next external clock EXCLK+ occurs, flip flop SEXCL+ is set. This flip flop is ten synchronized with the 10 MHz clock generating SEXCL- (Page 3) which in turn enables the first main clock, CKCNT+ and CKCTA+. INCLK+ (Page 3) also sets flip flop INTER+ which enables CNTOV+ (Page 10) to generate internal timing, and thus allow the single machine cycle.

The internal timing continues until the last address is detected and LAEWA+ (Page 6) generates SETEM- (J3). SETEM- forces flip flop INTER+ to reset thus disabling internal timing. The logic then awaits another external clock and the cycle can repeat.

## IV. PROGRAM CONTROLS

These switches share common control logic. Therefore, the logic common to all switches will be jointly discussed, then a unique description will be given for each switch function.

Four switch functions (LOAD MEMORY WORD, STEP, FETCH MEMORY WORD, and RESET) are debounced to generate LOADD-, STEPX-, FETCH-, and RESET- (Page 4). Each of these functions activates a timing sequence defined by the common logic shift register MAN00+ through MAN15+ (Page 4). Signals MAN11+ through MAN15+ are simply 100 nsec pulses shifted in time, as illustrated in Figure 3. Each of these pulses, depending on which switch activated them, performs some function in the generator.

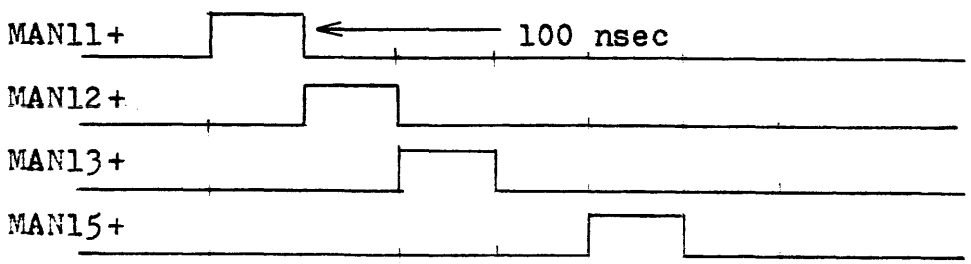



FIGURE 3

MANUAL SWITCH SHIFT REGISTER TIMING

Also of note for further understanding of the program controls, is that the MEMORY ADDRESS COUNTER is one address ahead of the displayed address on the front panel ADDRESS LED's. This occurs because as a memory word is loaded into the OUTPUT SHIFT REGISTER (Page 8), the associated memory address is also loaded into the PRESENT MEMORY ADDRESS register (BCNT1+ through BCNT6+ (Page 6)). The ADDRESS LED's are driven by the PRESENT MEMORY ADDRESS register. Thus, the output level data at the generators output connectors and the 16 data LED's are always the data associated with the address displayed on the ADDRESS LED's. As soon as the OUTPUT SHIFT REGISTER and PRESENT MEMORY ADDRESS register are loaded, the next memory address is immediately accessed (i.e., the MEMORY ADDRESS COUNTER is incremented). Therefore, the MEMORY ADDRESS COUNTER is one address location ahead of the rest of the machine.

## LOAD MEMORY WORD

This switch action causes loading of data from the front panel switches at a location in memory specified by the front panel ADDRESS switches. The LOAD function first loads the MEMORY ADDRESS COUNTER, WCNT1+ through WCNT6+ (Page 6) with the data from the PRESENT MEMORY ADDRESS register, BCNT1+ through BCNT6+ (Page 6). This is accomplished as MAN11+ generates LOADX- and GENSP+ (Page 4). LOADX- forces the MEMORY ADDRESS COUNTER to load the selected PRESENT MEMORY ADDRESS data, SWD01+ through SWD32+ (Page 6) on the next CKCNT+. GENSP+ generates COBS4- (Page 3) while ENINC+ enables the main clocks to be generated. MAN13+ then generates LOADD+ (Page 6) which generates the memory write signal WRITE- (Page 6).

Next, MAN15+ generates another GENSP+ (Page 4) which generates another set of main clocks. CKCNT+ and CKCTA+ loads the new data into the OUTPUT SHIFT REGISTER as well as again increments the MEMORY ADDRESS COUNTER.

## STEP

This control increments the MEMORY ADDRESS COUNTER by one. The STEP functions simply generates a GENSP+ (Page 4) signal at MAN15+ time. GENSP+ then enables a main clock, CKCNT+, which increments the MEMORY ADDRESS COUNTER by one.

## FETCH MEMORY WORD

The FETCH function loads the MEMORY ADDRESS COUNTER, WCNT1+ through WCNT6+ (Page 6) with data from the front panel ADDRESS switches SWD01+ through SWD32+ (Page 6). This is accomplished by MAN11+ generating LOADX- (Page 4) and

thus GENSP+. LOADX- forces the MEMORY ADDRESS COUNTER to load the front panel selected data on the next CKCNT+. GENSP+ generates COBS4- (Page 3) which enables CKCNT+ to be generated.

Next, MAN15+ generates another GENSP+ (Page 4) which generates another main clock, CKCNT+. This CKCNT+ loads the fetched memory data into the OUTPUT SHIFT REGISTER as well as increments the MEMORY ADDRESS COUNTER.

RESET

The RESET function first loads the MEMORY ADDRESS COUNTER, WCNT1+ through WCBT6+ (Page 6) with all zeroes. This is accomplished by MAN11+ generating LOADX- (Page 4) and thus GENSP+. LOADX- forces the MEMORY ADDRESS COUNTER to load the selected data, SW001+ through SW006+ (Page 6) on the next CKCNT+. Note that the selected data is zeroes because SMDUR- (from front panel reset switch, reference 648-105) disables the selector. GENSP+ generates COVS4- (Page 3) which enables a CKCNT+ to be generated.

Next, MAN15+ generates another GENSP+ (Page 4) which generates another main clock, CKCNT+. This CKCNT+ loads the data from memory location zero into the OUTPUT SHIFT REGISTER as well as increments the MEMORY ADDRESS COUNTER.

DYNAMIC UPDATE

The DYNAMIC UPDATE function loads front panel output level data and/or timing into memory when the MEMORY ADDRESS COUNTER equals the front panel ADDRESS switches. When in Dynamic Update, SDYNU- (Page 6) is low which enables flip flop SWDSB- (Page 6) to be set high. When the MEMORY ADDRESS COUNTER equals the front panel ADDRESS switches, SWEWC+ (Page 6) is high which sets flip flop SWBSB- (Page 6) high on the next 10 MHz clock, CLOCK+ (Page 6). SWEWC+ also inhibits the next main clock (CKCNT+) should it occur at that time via INHIB- (Page 6). SWBSB- generates a memory write pulse, WRITE- (Page 6) in coincidence with the memory address compare, which writes the new data into memory.

TIME

This switch does not perform a program control function. The TIME switch selects either the display of output level data or time data on the 16 front panel data LED's. When TIME is active, SEXTM- (Page 8) is low which forces the data selector RED01- through RED16- (Page 8) to select the timing data from the OUTPUT SHIFT REGISTER. When SEXTM- is not active (high) the output level data is displayed.

## WORD PARAMETERS

The three load functions load their respective registers with the data from the ADDRESS switches.

1) LAST MEMORY ADDRESS: LLASW- (Page 6) loads the LAST MEMORY ADDRESS register, LAST1+ through LAST6+ (Page 6).

2) WORDS PER MEMORY WORD: LWPMW- (Page 5) loads the WORDS PER MEMORY WORD register, WPMW1+ through WPM16+ (Page 5).

3) WORDS PER LAST MEMORY WORD: LWPLW- (Page 5) loads the WORDS PER LAST MEMORY WORD register WPLW1+ through WPL16+ (Page 5).

The three FETCH functions, ELAST-, EBITW-, and EBTLW- (Page 5) generate EXAMN+ (Page 5) which generates the select signals for the ADDRESS LED selector LED01- through LED32- (Page 5 and Page 6).

## SYNC OUT

The SYNC OUT pulse may be generated at each memory word accessed or at the address specified by the front panel ADDRESS switches. For EACH WORD, SELAD- (Page 9) is high which enables ENINC+ (Page 3 and Page 9) to generate CTBS1- (Page 9). This enables flip flop SYNC2+ to set, which generates the SYNC pulse SYNC0- and SYNCP- (Page 9). CTBS3+ (Page 9) resets flip flop SYNC2+ either 800 nsec or 800 usec after ENINC+ depending on the period defined by OTMRU+ (Page 9). If OTMRN+ is high, RSSYN+ (Page 9) is high and flip flop SYNC2+ is reset 50 nsec after ENINC+.

For SELECT ADDRESS, SELAD- is low which enables SYNCW+ (Page 6 and Page 9) to generate the sync pulse SYNC0- and SYNCP- (Page 9). SYNCW+ (Page 6) is generated from the MEMORY ADDRESS COUNTER and front panel ADDRESS switch compare SWEWC+ (Page 6).

## EXT CLK IN

The external clock from the EXT CLK IN connector generates EXCLK+ (Page 3). EXCLK+ may then start a single cycle operation by setting SEXCL+ (Page 3) or generate the main clocks by generating EXCLA- (Page 3).

## OPERATION VERIFICATION

This section includes static and dynamic tests which will verify correct operation of the RS-648. Use of these tests in conjunction with the THEORY OF OPERATION section allows malfunction detection. Two types of tests are provided, static and dynamic. The static tests require that the machine is on but need not contain a program. The dynamic tests require that the machine is on and running with the program specified in the specific test. The test equipment required for the tests are listed below:

1) The STATIC Test #1 through #4 requires no test equipment.

2) The DYNAMIC Test #5 and #6 require a dual channel (20 MHz bandwidth) oscilloscope, two BNC to BNC oscilloscope probes and one BNC "T" connector.

3) The DYNAMIC Test #7 and #8 requires a dual channel (20 MHz bandwidth) oscilloscope, two BNC to BNC oscilloscope probes, one BNC "T" connector and a second RS-648, or a pulse generator.

4) DYNAMIC Test #9 requires a dual channel (20 MHz bandwidth) oscilloscope and two BNC to BNC oscilloscope probes.

Note that Test #8 is a test for the 16 OUTPUT OPTION. This test need not be performed for RS-648's without this option. For those RS-648's with this option, verification of proper operation can simultaneously be made when running Test #5 through #7. When running these tests, all signals can be monitered and supplied via the back panel connector.

TEST #1 Verify WORD PARAMETERS:

This static test shall verify the ability to load and fetch the WORD PARAMETER registers of the RS-648.

GENERATOR MODE switch settings:

TIMING SIM/WORD: WORD (lower position)
START INT/EXT: OFF (center position)
SINGLE CYCLE: OFF (lower position)

INITIAL CONDITIONS: NONE

STEP 1: Set the ADDRESS toggle switches to Pattern 1-1 as specified in Table 1. Press the LAST MEMORY ADDRESS switch to the LOAD position. Press the LAST MEMORY ADDRESS switch to the FETCH position and observe the ADDRESS LED's. They should read-out as defined by the ADDRESS LED's in Pattern 1-1 of Table 1. Repeat for all patterns specified in Table 1.

| | ADDRESS SWITCHES | | | | | | ADDRESS LED'S | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 32 | 16 | 8 | 4 | 2 | 1 | 32 | 16 | 8 | 4 | 2 | 1 |
| Pattern 1-1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| " 1-2 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| " 1-3 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| " 1-4 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| " 1-5 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| " 1-6 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| " 1-7 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| " 1-8 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

TABLE 1.

STEP 2: Repeat Step 1 for the WORD PER MEMORY WORD switch. Only Pattern 1-2 through Pattern 1-6 should be tested.

STEP 3: Repeat Step 1 for the WORDS PER LAST MEMORY WORD switch. Only Pattern 1-2 through Pattern 1-6 should be tested.

TEST #2 Verify MEMORY ADDRESS COUNTER:

This static test shall verify the ability to preset, increment, and readout the MEMORY ADDRESS COUNTER. In addition, proper operation of several PROGRAM CONTROL switches will be verified. The 16 data LED's can be ignored for this test.

GENERATOR MODE switch settings:

TIMING SIM/WORD: WORD (lower position)
START INT/EXT: OFF (middle position)
SINGLE CYCLE: OFF (lower position)

INITIAL CONDITIONS:

1) Load LAST MEMORY ADDRESS with Pattern 1-8 of Table 1.

2) Load WORDS PER MEMORY WORD with Pattern 1-2 of Table 1.

3) Load WORDS PER LAST MEMORY WORD with Pattern 1-2 of Table 1.

STEP 1: Press the RESET switch. The ADDRESS LED's should readout Pattern 1-1 of Table 1.

STEP 2: Press the STEP switch. The ADDRESS LED's should have advanced by one (binary count).

STEP 3: Repeat Step 2 until the ADDRESS LED's have advanced through all 64 locations.

STEP 4: Press the FETCH MEMORY WORD switch with ADDRESS switch set to Pattern 1-1 of Table 1. The ADDRESS LED's should follow the ADDRESS switch pattern.

STEP 5: Repeat STEP 4 with Pattern 1-2 through 1-8 of Table 1.

TEST #3 Verify OUTPUT SHIFT REGISTER:

This Word Generator mode static test will verify the ability to load a prescribed data pattern into memory and observe the data pattern on the data LED's. Note that this test may be performed at any memory location. For the expanded memory option, it is desirable to test at least one location in each of the 4 sixteen bit memory segments, i.e., 0-15, 16-31, 32-47, 48-63.

GENERATOR MODE switch settings:

TIMING SIM/WORD: WORD (lower position)
START INT/EXT: OFF (center position)
SINGLE CYCLE: OFF (lower position)

PROGRAM CONTROL switch settings:

FETCH MEMORY WORD/TIME: Center position (Note that this will allow the data LED's to display the OUTPUT SHIFT REGISTER's 16 bits of data.)

INITIAL CONDITIONS:

1) Load LAST MEMORY ADDRESS with Pattern 1-8 of Table 1.

2) Load WORDS PER MEMORY WORD with Pattern 1-2 of Table 1.

3) Load WORDS PER LAST MEMORY WORD with Pattern 1-2 of Table 1.

STEP 1: Set the data toggle switches to Pattern 3-1 as specified in the INPUT PATTERN section of Table 2. Set the ADDRESS toggle switches to any address from 0-15. Press the FETCH MEMORY WORD/TIME switch to the FETCH MEMORY WORD position. Press the LOAD MEMORY WORD/STEP switch in the LOAD MEMORY WORD position. The 16 data LED's should immediately display the OUTPUT PATTERN specified for Pattern 3-1 of Table 2.

STEP 2: Repeat STEP 1 for all patterns in Table 2. If the expanded memory option is part of the generator under test, perform STEPS 3 through 5 also.

STEP 3: Change the ADDRESS switches to any address from 16-31 and perform STEP 2.

STEP 4: Change the ADDRESS switches to any address from 32-47 and perform STEP 2.

STEP 5: Change the ADDRESS switches to any address from 48-63 and perform STEP 2.

INPUT (16 DATA SWITCHES) PATTERN

| | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Pattern 3-1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| " 3-2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| " 3-3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| " 3-4 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| " 3-5 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| " 3-6 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| " 3-7 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| " 3-8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| " 3-9 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| " 3-10 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| " 3-11 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| " 3-12 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| " 3-13 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| " 3-14 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| " 3-15 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| " 3-16 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| " 3-17 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| " 3-18 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

OUTPUT (16 LED'S) PATTERN

| | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Pattern 3-1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| " 3-2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| " 3-3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| " 3-4 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| " 3-5 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| " 3-6 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| " 3-7 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| " 3-8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| " 3-9 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| " 3-10 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| " 3-11 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| " 3-12 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| " 3-13 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| " 3-14 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| " 3-15 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| " 3-16 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| " 3-17 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| " 3-18 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

TABLE 2

TEST #4 Verify TIMING REGISTER:

This Timing Simulator mode static test will verify the ability to load prescribed time data into memory and observe this time data on the data LED's. Note that this test may be performed at any memory location. For the expanded memory option, it is desirable to test at least one location in each of the 4 sixteen bit memory segments, i.e., 0-15, 16-31, 32-47, 48-63.

GENERATOR MODE switch settings:

TIMING SIM/WORD: TIMING SIM (upper position)
START INT/EXT: OFF (center position)
SINGLE CYCLE: OFF (lower position)

PROGRAM CONTROL switch settings:

FETCH MEMORY WORD/TIME: TIME (lower position)
(Note that this will allow the data LED's to display the TIMING REGISTER's data.)

INITIAL CONDITIONS:

Load LAST MEMORY ADDRESS with Pattern 1-8 of Table 1.

STEP 1: Set the thumbwheel time switches to Pattern 4-1 as specified in Table 3. Set the ADDRESS toggle switches to any address from 0-15. Press the FETCH MEMORY WORD/TIME switch to the FETCH MEMORY WORD position and return to the TIME position. Press the LOAD MEMORY WORD/STEP switch to the LOAD MEMORY WORD position. The 16 data LED's should now display the corresponding OUTPUT PATTERNS specified in Table 3.

STEP 2: Repeat STEP 1 for all patterns in Table 3. If the expanded memory option is part of the generator under test, perform STEP's 3 through 5 also.

STEP 3: Change the ADDRESS switches to any address from 16-31 and perform STEP 2.

STEP 4: Change the ADDRESS switches to any address from 32-47 and perform STEP 2.

STEP 5: Change the ADDRESS switches to any address from 48-63 and perform STEP 2.

| FRONT PANEL THUMBWHEEL TIMING DATA | | | OUTPUT (16 LED'S) PATTERN | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | HUNDREDS | | | | TENS | | | | UNITS | | | | MSEC | USEC | 100 NSEC | 50/50 NSEC |
| | | | 8 | 4 | 2 | 1 | 8 | 4 | 2 | 1 | 8 | 4 | 2 | 1 | | | | |
| | | | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 |
| PATTERN | 4-1 | 0 0 0 MSEC | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| " | 4-2 | 0 0 1 " | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| " | 4-3 | 0 0 2 " | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 |
| " | 4-4 | 0 0 3 " | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 |
| " | 4-5 | 0 0 4 " | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| " | 4-6 | 0 0 5 " | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 |
| " | 4-7 | 0 0 6 " | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 |
| " | 4-8 | 0 0 7 " | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |
| " | 4-9 | 0 0 8 " | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| " | 4-10 | 0 0 9 " | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| " | 4-11 | 0 0 0 USEC | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| " | 4-12 | 0 1 0 " | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| " | 4-13 | 0 2 0 " | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| " | 4-14 | 0 3 0 " | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| " | 4-15 | 0 4 0 " | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| " | 4-16 | 0 5 0 " | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| " | 4-17 | 0 6 0 " | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| " | 4-18 | 0 7 0 " | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| " | 4-19 | 0 8 0 " | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| " | 4-20 | 0 9 0 " | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| " | 4-21 | 0 0 0 100 NSEC | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| " | 4-22 | 1 0 0 " " | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| " | 4-23 | 2 0 0 " " | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| " | 4-24 | 3 0 0 " " | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| " | 4-25 | 4 0 0 " " | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| " | 4-26 | 5 0 0 " " | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| " | 4-27 | 6 0 0 " " | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| " | 4-28 | 7 0 0 " " | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| " | 4-29 | 8 0 0 " " | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| " | 4-30 | 9 0 0 " " | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| " | 4-31 | X X X 50/50 NSEC | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

X = Don't Care

TABLE 3.

TEST #5 Verify WORD GENERATOR Mode:

This test dynamically verifies the Word Generator mode of operation of the RS-648. The test shall be performed with a prescribed program and waveforms of the expected generator outputs are described for monitering purposes.

GENERATOR MODE switch settings:

TIMING SIM/WORD: WORD (lower position)
START INT/EXT: OFF (center position)
SINGLE CYCLE: OFF (lower position)

INITIAL CONDITIONS:

1) Load the generator as defined in the Word Generator programming sheet Table 3. Be sure to set the thumbwheel switches to 1 MSEC and also be sure to load all WORD PARAMETER registers as specified in Table 3. Reference the TIMING SIMULATOR/WORD GENERATOR, MODEL RS-648 Users Guide (Document Control #648-UG-001) for loading instructions.

2) Press the DYNAMIC UPDATE/RESET switch to the RESET (lower) position.

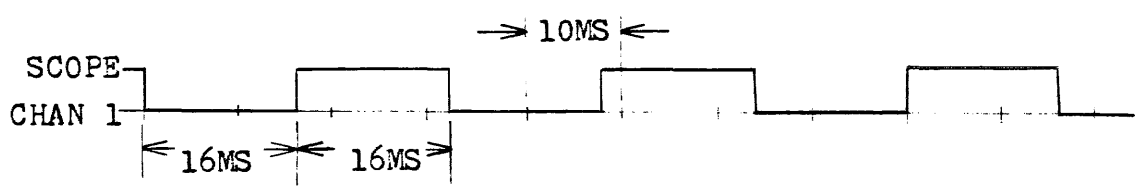
3) Set the ADDRESS toggle switches to all zeroes, (000000).

4) Set the SYNC OUT switch to SELECT ADDRESS (lower position).

STEP 1: Set the START INT/EXT switch to the START INT (upper position). The generator should now be running; this can be verified by data LED's 1 and 2 dimly glowing.

STEP 2: Sync the oscilloscope to the SYNC OUT output of the generator. Be sure to sync on negative going edge of the SYNC OUT signal.

STEP 3: Set the oscilloscope time scale to 10 MS per division. Set the vertical scale to 2 volts per division. SYNC OUT when viewed on channel 1 of the oscilloscope should appear as follows:



| ADDRESS | | | | | | DATA BITS TO BE PROGRAMMED | | | | | | | | | | | | OUTPUT WORD NUMBER |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 32 | 16 | 8 | 4 | 2 | 1 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 to 16 |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 17 to 32 |
| | | 0 | 0 | 1 | 0 | | | | | | | | | | | | | | | | | 33 to 48 |
| | | 0 | 0 | 1 | 1 | | | | | | | | | | | | | | | | | 49 to 64 |
| | | 0 | 1 | 0 | 0 | | | | | | | | | | | | | | | | | 65 to 80 |
| | | 0 | 1 | 0 | 1 | | | | | | | | | | | | | | | | | 81 to 96 |
| | | 0 | 1 | 1 | 0 | | | | | | | | | | | | | | | | | 97 to 112 |
| | | 0 | 1 | 1 | 1 | | | | | | | | | | | | | | | | | 113 to 128 |
| | | 1 | 0 | 0 | 0 | | | | | | | | | | | | | | | | | 129 to 144 |
| | | 1 | 0 | 0 | 1 | | | | | | | | | | | | | | | | | 145 to 160 |
| | | 1 | 0 | 1 | 0 | | | | | | | | | | | | | | | | | 161 to 176 |
| | | 1 | 0 | 1 | 1 | | | | | | | | | | | | | | | | | 177 to 192 |
| | | 1 | 1 | 0 | 0 | | | | | | | | | | | | | | | | | 193 to 208 |
| | | 1 | 1 | 0 | 1 | | | | | | | | | | | | | | | | | 209 to 224 |
| | | 1 | 1 | 1 | 0 | | | | | | | | | | | | | | | | | 225 to 240 |
| | | 1 | 1 | 1 | 1 | | | | | | | | | | | | | | | | | 241 to 256 |
| 0 | 0 | 0 | 0 | 0 | 1 | | | | | | | | | | | | | | | | 1 | |
| LAST MEMORY ADD. | | | | | | OUTPUT CHANNEL | | | | | | | | | | | | | | | | |
| 0 | 1 | 0 | 0 | 0 | 0 | | | | | | | | | | | | | | | | | |
| WORDS PER MEMORY WORD | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 0 | 0 | 0 | 0 | | | | | | | | | | | | | | | | | |
| WORDS PER LAST MEMORY WORD | | | | | | | | | | | | | | | | | | | | | | |

WORD GENERATOR SINGLE BIT CODING SHEET

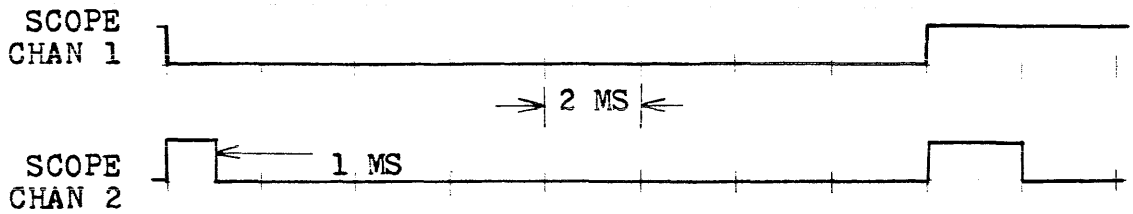
| TIME PERIOD | | | |
|---|---|---|---|
| HUND | TENS | UNIT | MULT |
| 0 | 0 | 1 | MSEC |

TABLE 4.

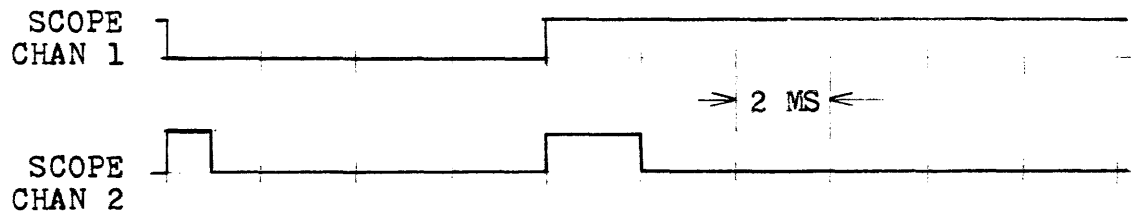
WORD GENERATOR PROGRAM

FOR TEST #5

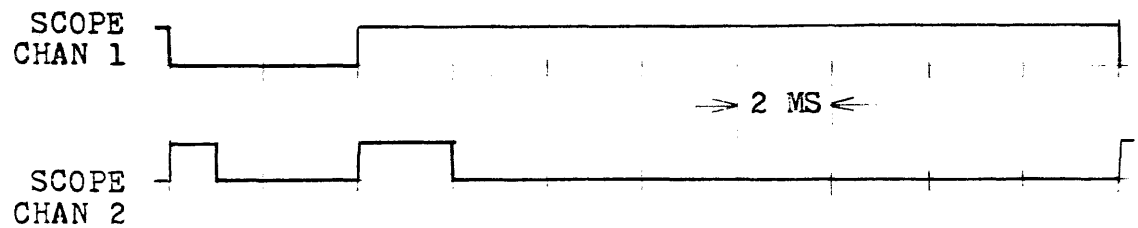
STEP 4: Set the oscilloscope time scale to 2 MS per division, and examine the generator's output Channel 1 with Channel 2 of the oscilloscope. The following waveform should be seen.



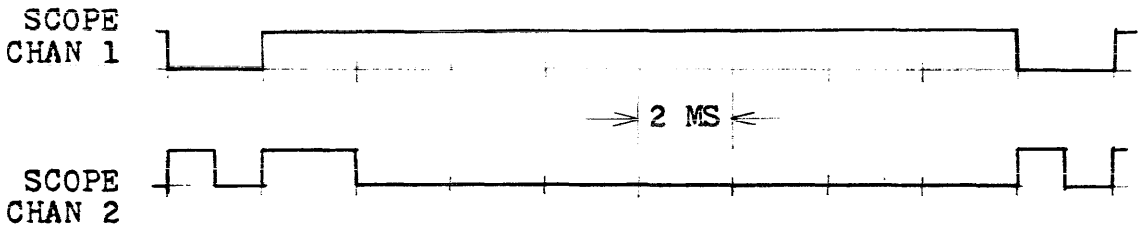

STEP 5: Change the WORDS PER MEMORY WORD register to 8 (001000). This is performed by setting the address toggle switches to 001000, pressing the WORDS PER MEMORY WORD switch into the LOAD position, and then finally resetting the ADDRESS toggle switches to 000000. The following waveforms should now be observed.



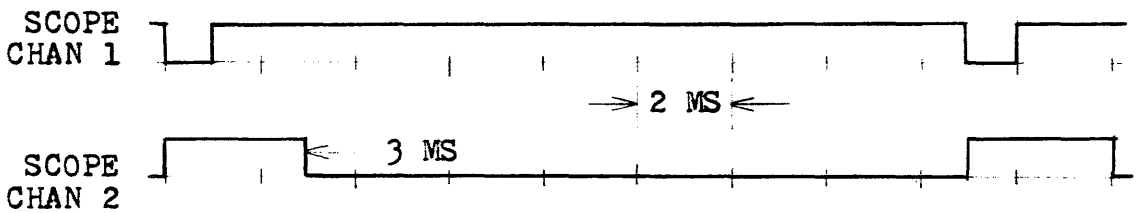

STEP 6: Change the WORDS PER MEMORY WORD register to 4 (000100) and observe the following waveforms.



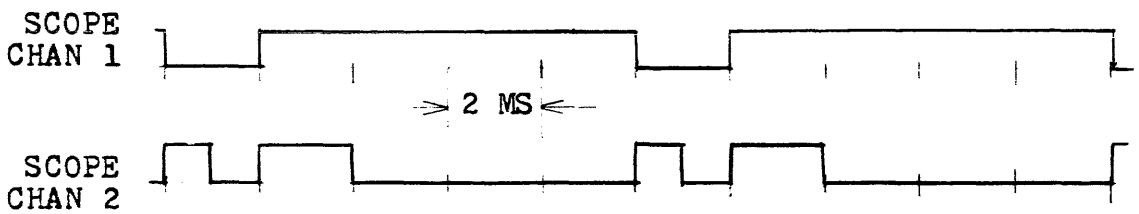
STEP 7: Change the WORDS PER MEMORY WORD register to 2 (000010) and observe the following waveform.



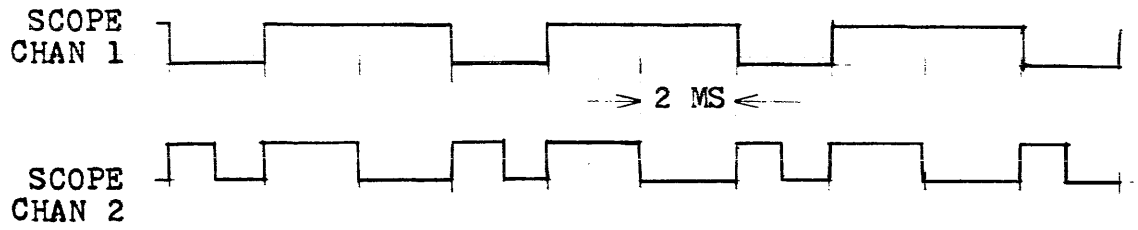

STEP 8: Change the WORDS PER MEMORY WORD register to 1 (000001) and observe the following waveforms.



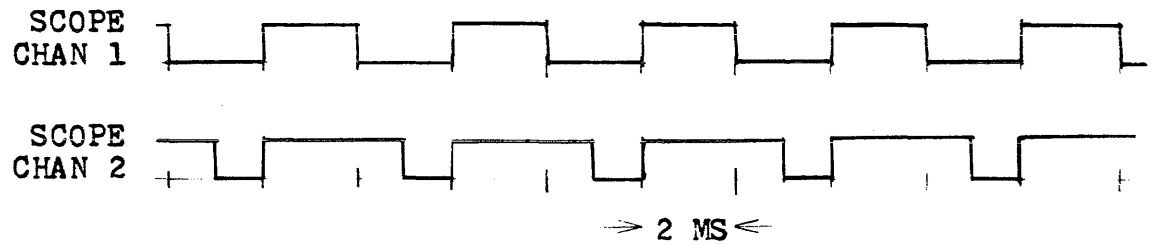

STEP 9: Change the WORDS PER MEMORY WORD register back to 2 (000010) and change the WORDS PER LAST MEMORY WORD register to 8 (001000). Note that changing the WORDS PER LAST MEMORY WORD is accomplished in the same manner that the WORDS PER MEMORY WORD was. Observe the following waveform.



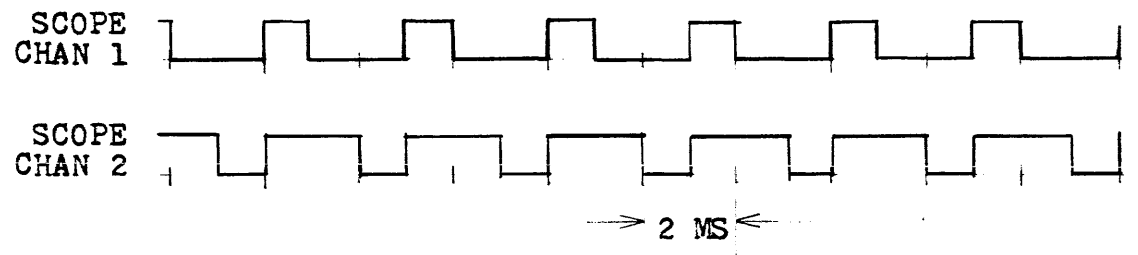
STEP 10: Change the WORDS PER LAST MEMORY WORD to 4 (000100) and observe the following waveform.



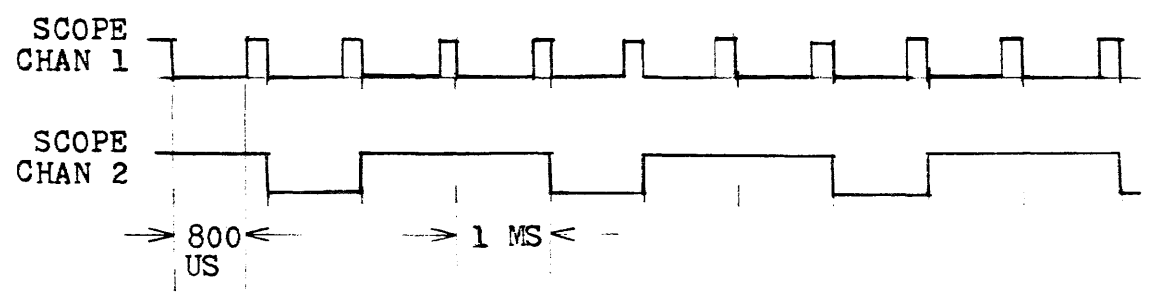

STEP 11: Change the WORDS PER LAST MEMORY WORD to 2 (000010) and observe the following waveform.




STEP 12: Change the WORDS PER LAST MEMORY WORD to 1 (000001) and observe the following waveforms.




STEP 13: Change the SYNC OUT switch to EACH WORD and observe the following waveforms. Note that the oscilloscope must now be resynchronized to output waveform.



TEST #6 Verify TIMING SIMULATOR Mode:

This test dynamically verifies the Timing Simulator mode of operation of the RS-648. It shall also verify the DYNAMIC UPDATE capability of the RS-648. The test shall be performed with a prescribed program and waveforms of the expected generator output are described for monitering purposes.

GENERATOR MODE switch settings:

TIMING SIM/WORD: TIMING SIM (upper position)
START INT/EXT: OFF (center position)
SINGLE CYCLE: OFF (lower position)

INITIAL CONDITIONS:

1) Load the generator as defined in the Timing Simulator programming sheet Table 5. Be sure to load the LAST MEMORY ADDRESS specified in Table 5. Reference the TIMING SIMULATOR/WORD GENERATOR, MODEL RS-648 User's Guide (Document Control #648-UG-001) for loading instructions.

2) Press the DYNAMIC UPDATE/RESET switch to the RESET (lower) position.

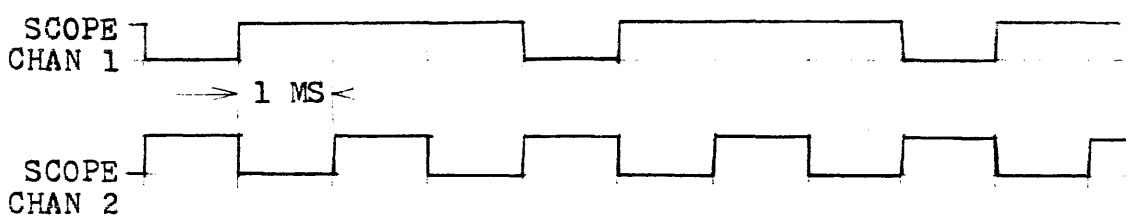
3) Set the ADDRESS toggle switches to all zeroes, (000000).

4) Set the SYNC OUT switch to SELECT ADDRESS (lower position).

STEP 1: Set the START INT/EXT switch to START INT (upper position). The generator should now be running.

STEP 2: Sync the oscilloscope to the SYNC OUT output of the generator. Be sure to sync on the negative going edge of the SYNC OUT signal.

STEP 3: Set the oscilloscope time scale to 1 millisecond per division, and set the vertical scale to 2 volts per division. View the SYNC OUT signal on Channel 1 of the oscilloscope. Sequentially examine the generator outputs 1 through 8 on the oscilloscope Channel 2. Each output channel should have the same relationship to SYNC OUT as shown below.



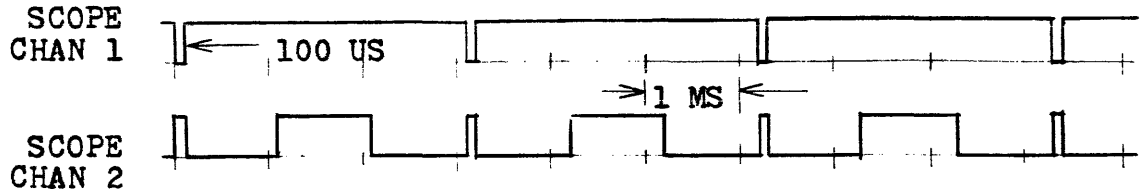
| TIME DIGITS TO BE PROGRAMMED | | | | ADDRESS | | | | | | DATA BITS TO BE PROGRAMMED (EVEN DATA BITS NOT USED) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| HUND | TENS | UNIT | MULT | 32 | 16 | 8 | 4 | 2 | 1 | 15 | 13 | 11 | 9 | 7 | 5 | 3 | 1 |
| 0 | 0 | 1 | MS | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 0 | 1 | MS | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | MS | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 0 | 1 | MS | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | | | | 0 | 1 | 0 | 0 | | | | | | | | |
| | | | | | | 0 | 1 | 0 | 1 | | | | | | | | |
| | | | | | | 0 | 1 | 1 | 0 | | | | | | | | |
| | | | | | | 0 | 1 | 1 | 1 | | | | | | | | |
| | | | | | | 1 | 0 | 0 | 0 | | | | | | | | |
| | | | | | | 1 | 0 | 0 | 1 | | | | | | | | |
| | | | | | | 1 | 0 | 1 | 0 | | | | | | | | |
| | | | | | | 1 | 0 | 1 | 1 | | | | | | | | |
| | | | | | | 1 | 1 | 0 | 0 | | | | | | | | |
| | | | | | | 1 | 1 | 0 | 1 | | | | | | | | |
| | | | | | | 1 | 1 | 1 | 0 | | | | | | | | |
| | | | | | | 1 | 1 | 1 | 1 | | | | | | | | |
| | | | | 0 | 0 | 0 | 0 | 1 | 1 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 |
| | | | | LAST MEMORY ADDRESS | | | | | | OUTPUT CHANNEL | | | | | | | |

TIMING SIMULATOR CODING SHEET

TABLE 5.

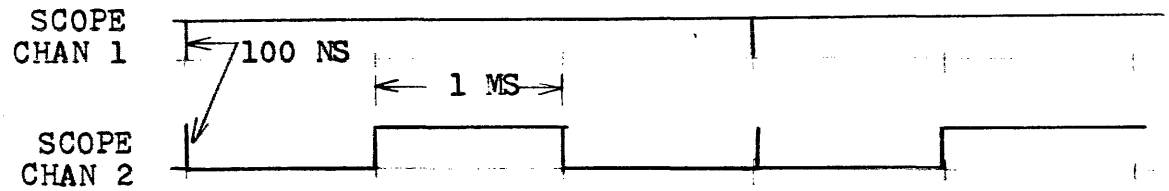
TIMING SIMULATOR PROGRAM FOR TEST #6

STEP 4: Set the 8 odd numbered data toggle switches to the upper (1) position. The 8 even data switches may be high or low, i.e., don't care. Set the thumbwheel time switches to 100 USEC and press the DYNAMIC UPDATE/RESET switch to the DYNAMIC UPDATE (upper) position. Observe each of the 8 generator output channels sequentially. They should all appear as shown below.

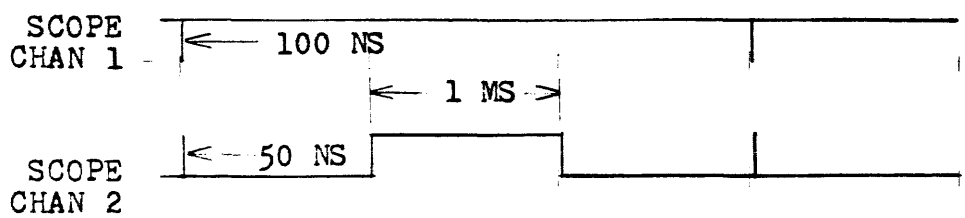



Note that STEP 4 dynamically updated the memory data stored at address zero.

STEP 5: Set the 8 odd numbered data toggle switches to the up (1) position. (The 8 even data switches may be high or low, i.e., don't care). Set the thumbwheel time switches to 001 100 NSEC (100 nanoseconds) and press the DYNAMIC UPDATE/RESET switch to the DYNAMIC UPDATE (upper) position. Observe each of the 8 output channels sequentially. They should all appear as shown below.




STEP 6: Set the 8 odd numbered data toggle switches in the up (1) position. Set the 8 even numbered data toggle switches in the down (0) position. Set the thumbwheel time switch to XXX 50/50 NSEC, where X is don't care. Press the DYNAMIC UPDATE/RESET switch to the DYNAMIC UPDATE (upper) position. Observe each of the 8 output channels sequentially. They should appear as shown below.



TEST #7 Verify EXT CLK and SINGLE CYCLE:

This test dynamically verifies the external clock (EXT CLK IN) and the SINGLE CYCLE function of the RS-648. The test shall be performed with a prescribed program and waveforms of the expected generator outputs are described for monitering purposes. This test requires an external signal source, either another RS-648 programmed to give the clock waveform specified in this test, or a pulse generator which can generate the specified waveform.

GENERATOR MODE switch settings:

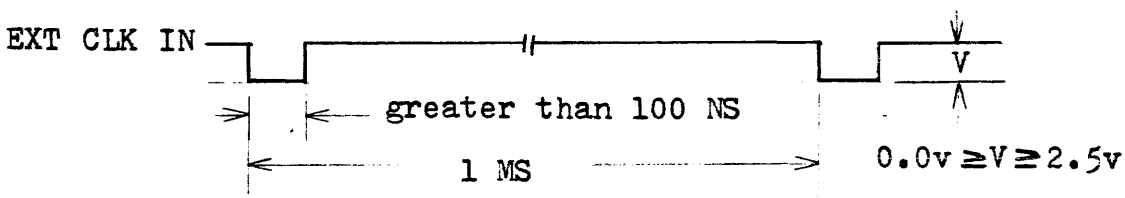
TIMING SIM/WORD: WORD (lower position)
START INT/EXT: OFF (center position)
SINGLE CYCLE: OFF (lower position)

INITIAL CONDITIONS:

1) Load the generator as defined in the Word Generator programming sheet Table 6. Be sure to load all the specified WORD PARAMETER registers and to set the time thumbwheel switches as specified. Reference the TIMING SIMULATOR/WORD GENERATOR, MODEL RS-648 User's Guide (Document Control #648-UG-001) for the loading instructions.

2) Press the DYNAMIC UPDATE/RESET switch to the RESET (lower) position.

3) Connect the external clock source (pulse generator) to the oscilloscope and verify that the clock signal is as shown below.




Then connect this external clock to the generators EXT CLK IN BNC connector on the front panel.

4) Set the ADDRESS toggle switches to all zeroes (000000).

5) Set the SYNC OUT switch to SELECT ADDRESS (lower) position.

STEP 1: Set the START INT/EXT switch to the EXT (lower) position. The generator should now be running. Sync the oscilloscope to the SYNC OUT output of the RS-648. Be sure to sync on the negative

| ADDRESS | | | | | | DATA BITS TO BE PROGRAMMED | | | | | | | | | | | | | | | | OUTPUT WORD NUMBER |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 32 | 16 | 8 | 4 | 2 | 1 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1,2 |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 3,4 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 5,6 |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 7,8 |
| | | 0 | 1 | 0 | 0 | | | | | | | | | | | | | | | | | 9,10 |
| | | 0 | 1 | 0 | 1 | | | | | | | | | | | | | | | | | 11,12 |
| | | 0 | 1 | 1 | 0 | | | | | | | | | | | | | | | | | 13,14 |
| | | 0 | 1 | 1 | 1 | | | | | | | | | | | | | | | | | 15,16 |
| | | 1 | 0 | 0 | 0 | | | | | | | | | | | | | | | | | 17,18 |
| | | 1 | 0 | 0 | 1 | | | | | | | | | | | | | | | | | 19,20 |
| | | 1 | 0 | 1 | 0 | | | | | | | | | | | | | | | | | 21,22 |
| | | 1 | 0 | 1 | 1 | | | | | | | | | | | | | | | | | 23,24 |
| | | 1 | 1 | 0 | 0 | | | | | | | | | | | | | | | | | 25,26 |
| | | 1 | 1 | 0 | 1 | | | | | | | | | | | | | | | | | 27,28 |
| | | 1 | 1 | 0 | 1 | | | | | | | | | | | | | | | | | 29,30 |
| | | 1 | 1 | 1 | 1 | | | | | | | | | | | | | | | | | 31,32 |
| 0 | 0 | 0 | 0 | 1 | 1 | | | | | | | | | | | | | | | | | |
| LAST MEMORY ADD. | | | | | | 8 | | 7 | | 6 | | 5 | | 4 | | 3 | | 2 | | 1 | | |
| | | | | | | OUTPUT CHANNELS | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 0 | 1 | 0 | | | | | | | | | | | | | | | | | |
| WORDS PER MEMORY WORD | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 0 | 1 | 0 | | | | | | | | | | | | | | | | | |
| WORDS PER LAST MEMORY WORD | | | | | | | | | | | | | | | | | | | | | | |

WORD GENERATOR EIGHT BIT PARALLEL CODING SHEET

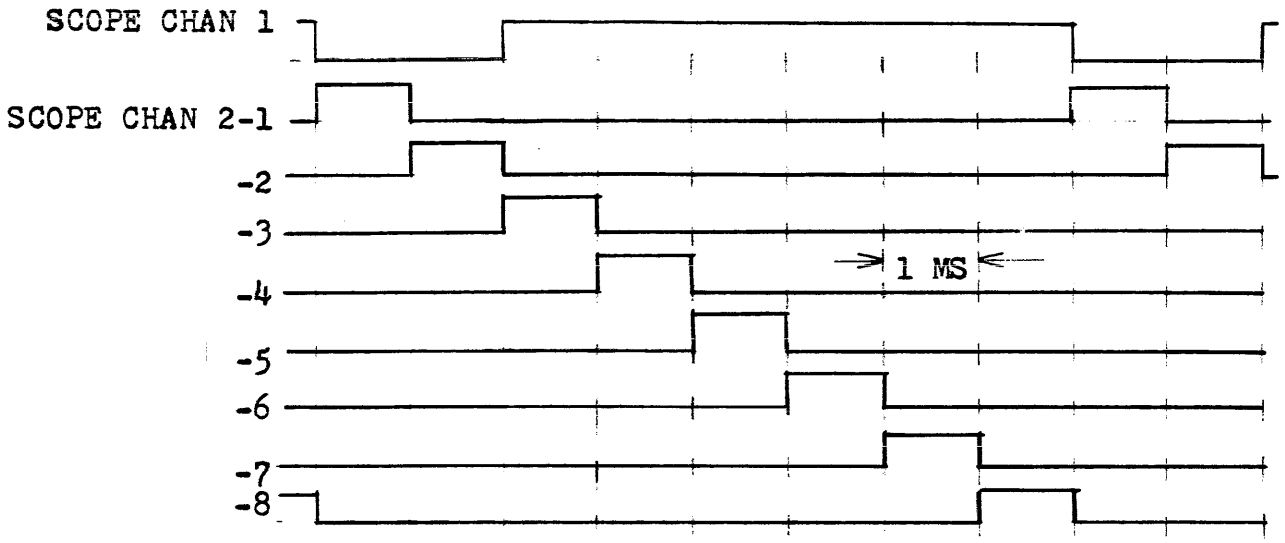
| TIME PERIOD | | | |
|---|---|---|---|
| HUND | TENS | UNIT | MULT |
| 0 | 1 | 0 | USEC |

TABLE 6.

WORD GENERATOR PROGRAM

FOR TEST #7

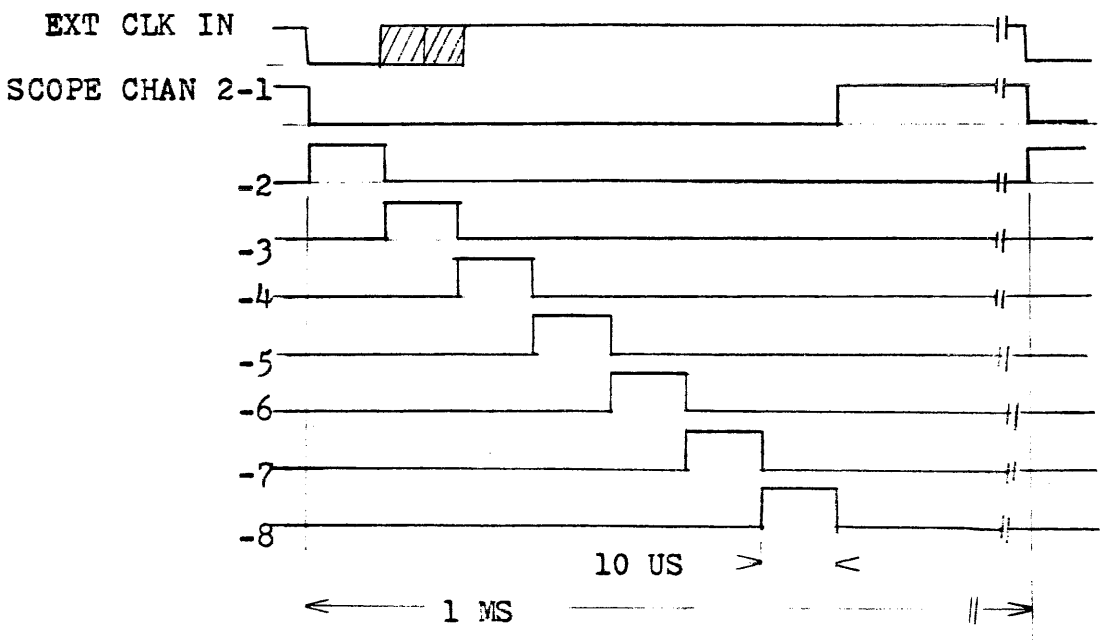
going edge of the SYNC OUT signal. Set the oscilloscope vertical scale to 2 volts per division and the oscilloscope time scale to 1 millisecond per division and examine the SYNC OUT signal on Channel 1 of the oscilloscope. Sequentially examine generators 8 output channels on Channel 2 of the oscilloscope. The timing relationships are shown below.




STEP 2: Set the SINGLE CYCLE switch to the on (upper) position. Set the START INT/EXT switch to START INT.

STEP 3: Sync the oscilloscope to the negative edge of the EXT CLK IN signal.

STEP 4: Set the oscilloscope time scale to 10 microseconds per division and sequentially examine the 8 output channels of the generator. The timing relationship is shown below.



TEST #8 Verify 16 OUTPUT OPTION:

This dynamic test verifies the 16 OUTPUT OPTION to the Standard RS-648. The test shall be performed with a prescribed program and waveforms of the expected generator outputs are described for monitering purposes. This test requires an external signal source, either another RS-648 programmed to give the clock waveform specified in this test or a pulse generator which can generate the specified waveform.

GENERATOR MODE switch settings:

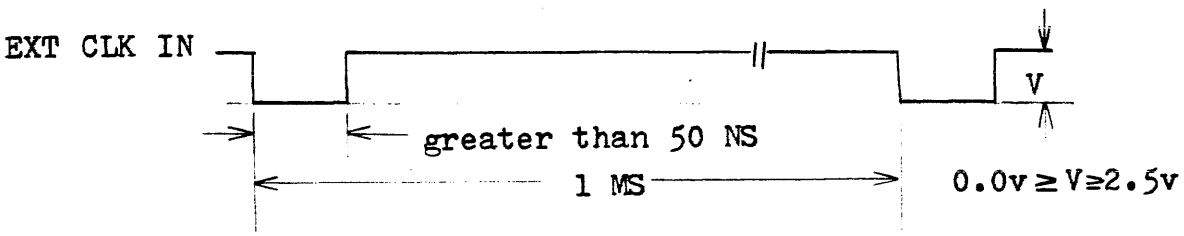
TIMING SIM/WORD: WORD (lower position)
START INT/EXT: OFF (center position)
SINGLE CYCLE: OFF (lower position)

INITIAL CONDITIONS:

1) Load the generator as defined in the Word Generator programming sheet Table 7. Be sure to load all WORD PARAMETER registers and set the time thumb-wheel switches as specified in Table 7. Reference the TIMING SIMULATOR/WORD GENERATOR, MODEL RS-648 User's Guide (Document Control #648-UG-001) for loading instructions.

2) Press the DYNAMIC UPDATE/RESET switch to the RESET (lower) position.

3) Connect external signal source with the following waveform to external clock input (pin 17 on the 16 OUTPUT OPTION back panel connector).




4) Set the ADDRESS toggle switches to all zeroes (000000).

5) Set the SYNC OUT switch to the SELECT ADDRESS position.

6) SYNC the oscilloscope to the generator SYNC OUT output. Be sure to sync on the negative edge of the SYNC OUT signal.

STEP 1: Set the START INT/EXT switch to EXT (lower) position.

| ADDRESS | | | | | | DATA BITS TO BE PROGRAMMED | | | | | | | | | | | | | | | | OUTPUT WORD NUMBER |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 32 | 16 | 8 | 4 | 2 | 1 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1,2 |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 3,4 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 5,6 |
| 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 7,8 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 9,10 |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 11,12 |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 13,14 |
| 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 15,16 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 17,18 |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 19,20 |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 21,22 |
| 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 23,24 |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 25,26 |
| 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 27,28 |
| 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 29,30 |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 31,32 |
| 0 | 0 | 1 | 1 | 1 | 1 | | | 8 | | 7 | | 6 | | 5 | | 4 | | 3 | | 2 | | 1 |
| LAST MEMORY ADD. | | | | | | OUTPUT CHANNELS | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 1 | | | | | | | | | | | | | | | | | |
| WORDS PER MEMORY WORD | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 1 | | | | | | | | | | | | | | | | | |
| WORDS PER LAST MEMORY WORD | | | | | | | | | | | | | | | | | | | | | | |

WORD GENERATOR EIGHT BIT PARALLEL CODING SHEET

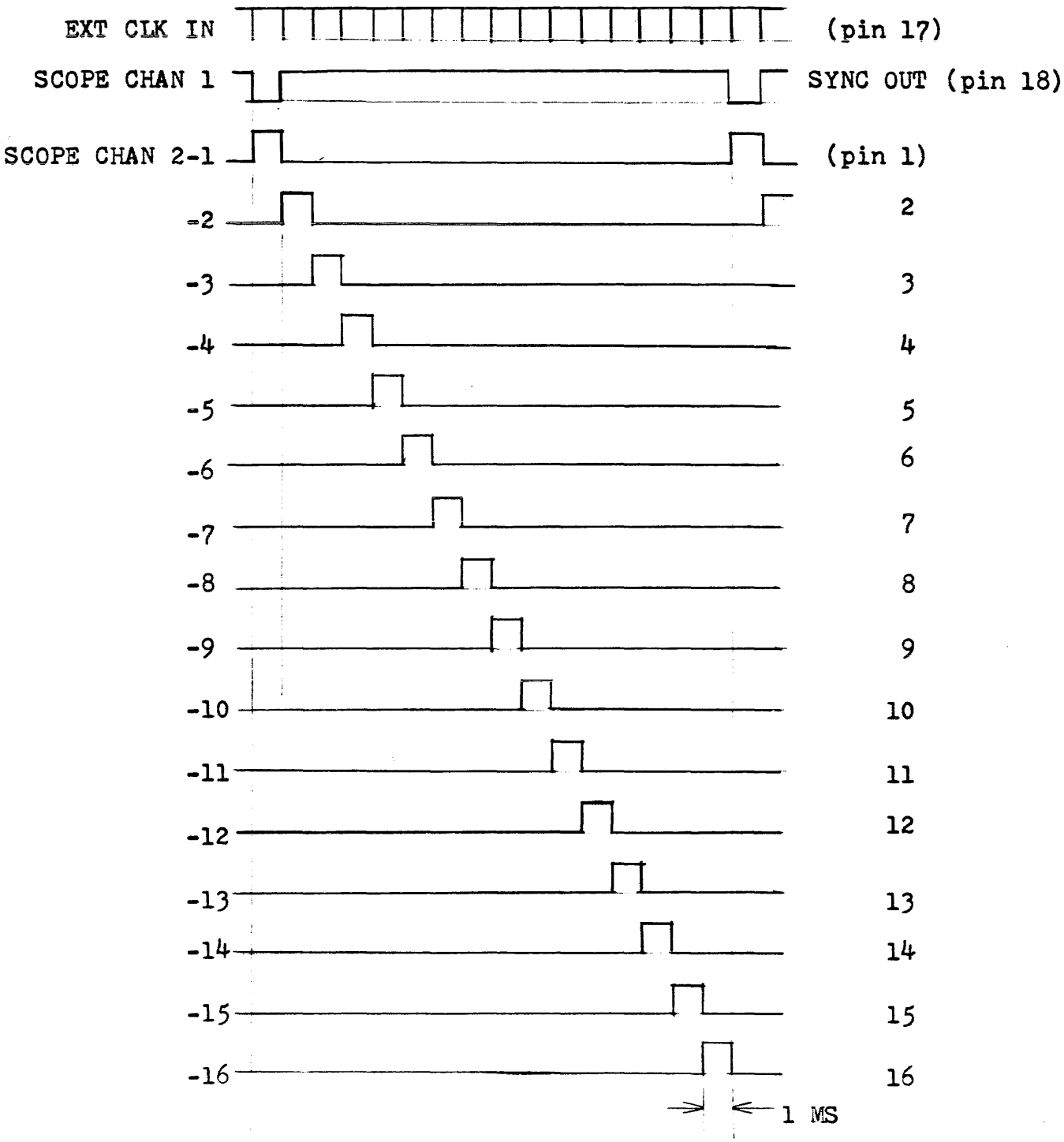
| TIME PERIOD | | | |
|---|---|---|---|
| HUND | TENS | UNIT | MULT |
| X | X | X | X |

TABLE 7.

WORD GENERATOR CODING SHEET

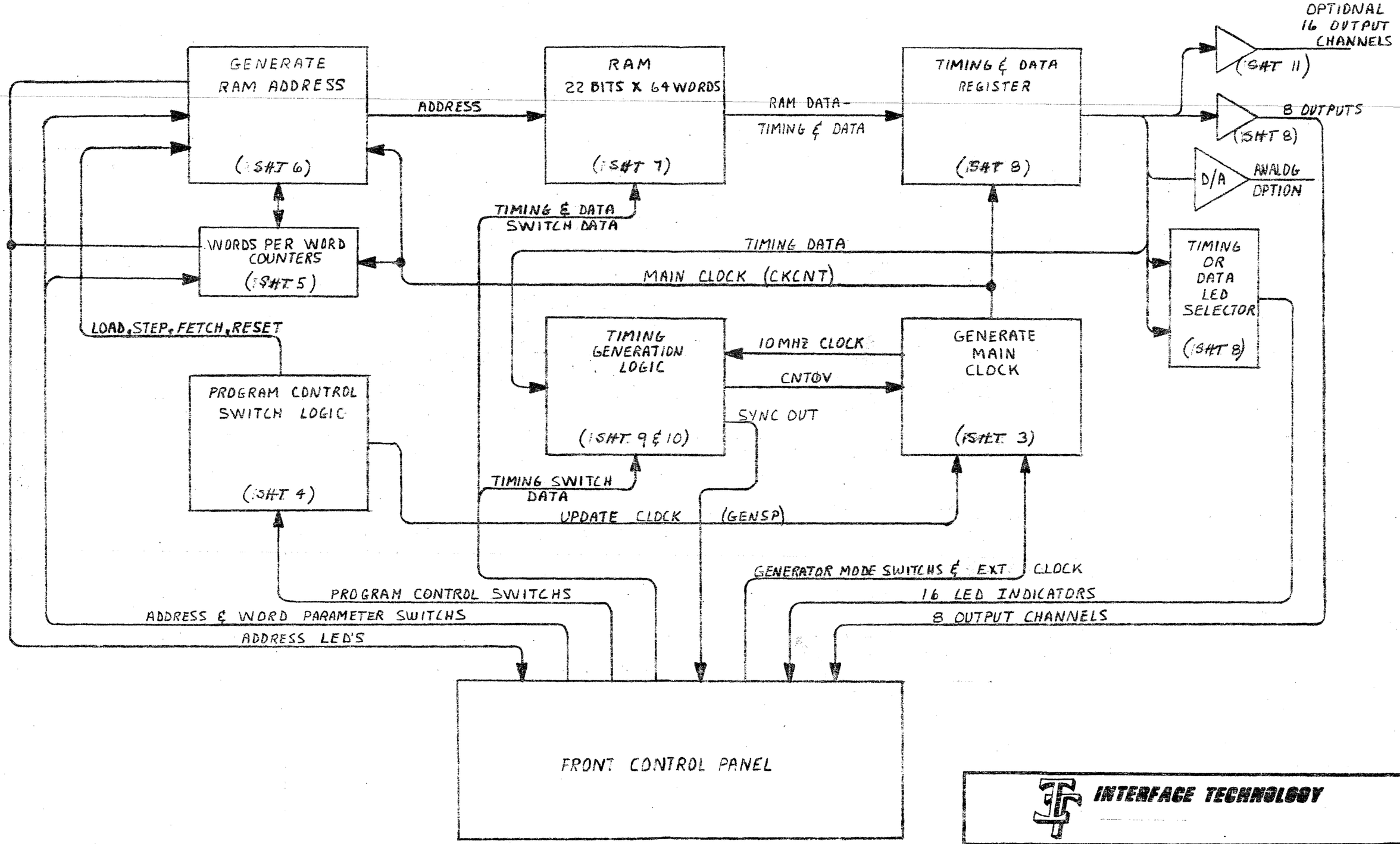
Used for the 16 OUTPUT OPTION Test #8

STEP 2: Set the oscilloscope time scale to 2 milliseconds per division, and the vertical scale to 2 volts per division. Observe the sync output waveform on pin 18 of the back panel connector with Channel 1 of the oscilloscope. Sequentially observe the 16 output channels with Channel 2 of the oscilloscope. The timing relationships are shown below:



## TABLE 8 DRAWING LIST

| TITLE | DRAWING NUMBER |
|---|---|
| Timing Simulator/Word Generator Model RS-648 | 648-302 |
| Block Diagram | Sheet 1 |
| Logic Panel Pictorial | Sheet 2 |
| Clock Generation | Sheet 3 |
| Program Switch Control Logic | Sheet 4 |
| Words Per Memory Word Logic | Sheet 5 |
| Memory Address Logic | Sheet 6 |
| Standard Memory | Sheet 7 |
| Optional Memory | Sheet 7A-7C |
| Output Register | Sheet 8 |
| Timing and Sync Generation | Sheet 9 |
| Timing Compare Logic | Sheet 10 |
| 16 Output Option | 648-304 |
| ROM Option | 648-305 |
| Front Panel Schematic | 648-105 |
| AC Power Schematic | 648-203 |




INTERFACE TECHNOLOGY

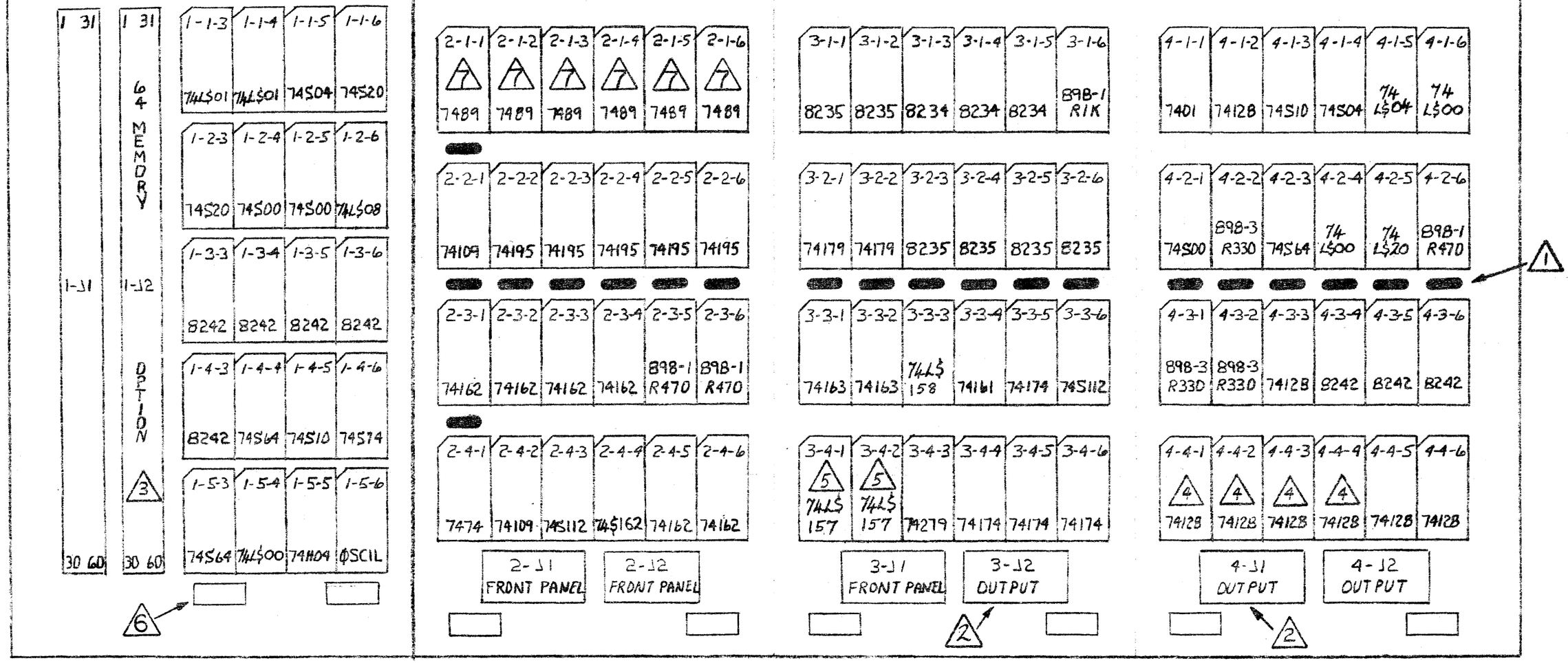
| | | |
|---|---|---|
| | ASSY/LBL, LOWER LOGIC PNL. FOR RS-648 | |
| 7/1/74 | 648-302 | SHT 1 OF 10 |

(1001 1306, SHT. 1 OF 11)

14-20-I/Ø

68-26-203

CARD 1 | CARD 2 | CARD 3 | CARD 4

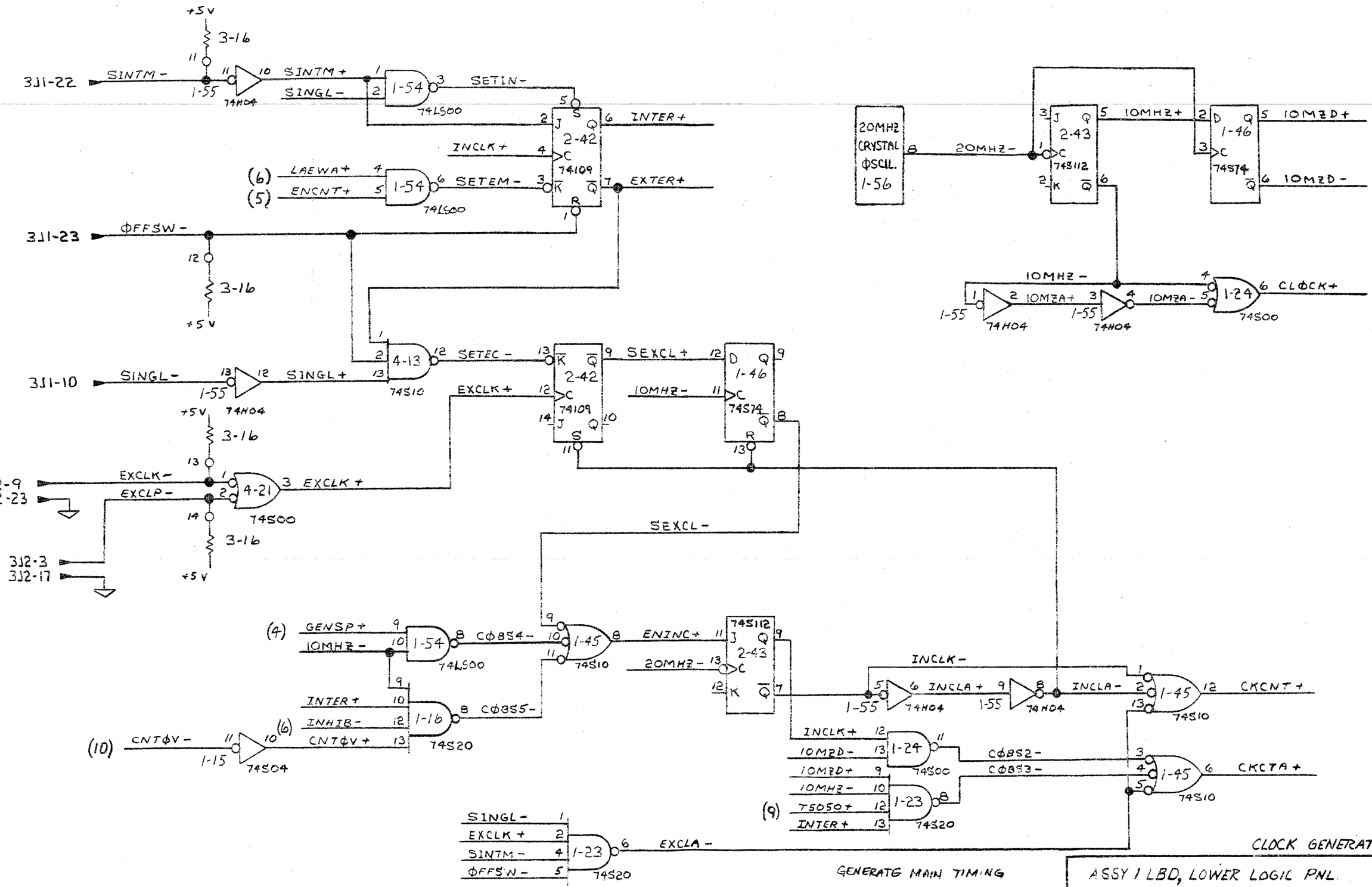



1. .01 uf 100V CAPACITOR - 20 PLACES
2. CONNECTORS FOR 16 OUTPUT OPTION
3. 64 WORD MEMORY OPTION CARD
4. INSERT IN 16 OUTPUT OPTION ONLY
5. FOR EXPANDED CHASSIS REPLACE WITH DM8123
6. 10PF 10V CAPACITOR – 8 PLACES.
7. BIPOLAR MEMORIES P/N SN7489N, 6561J OR AM27LS03PC

ASSY/ LBD, LOWER LOGIC PNL.
FOR RS-648

648-302 | SHT 2 OF 10

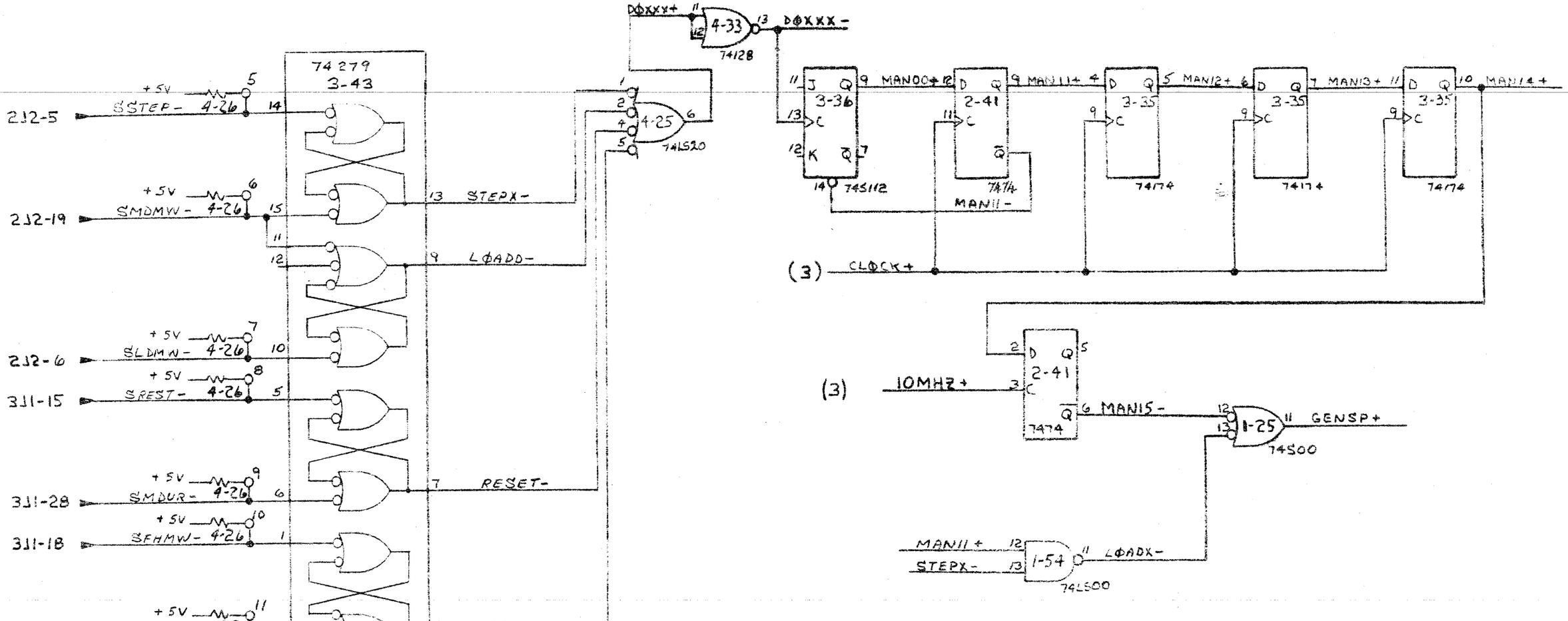
1001 1306, SHT. 2 OF 11




CLOCK GENERATION

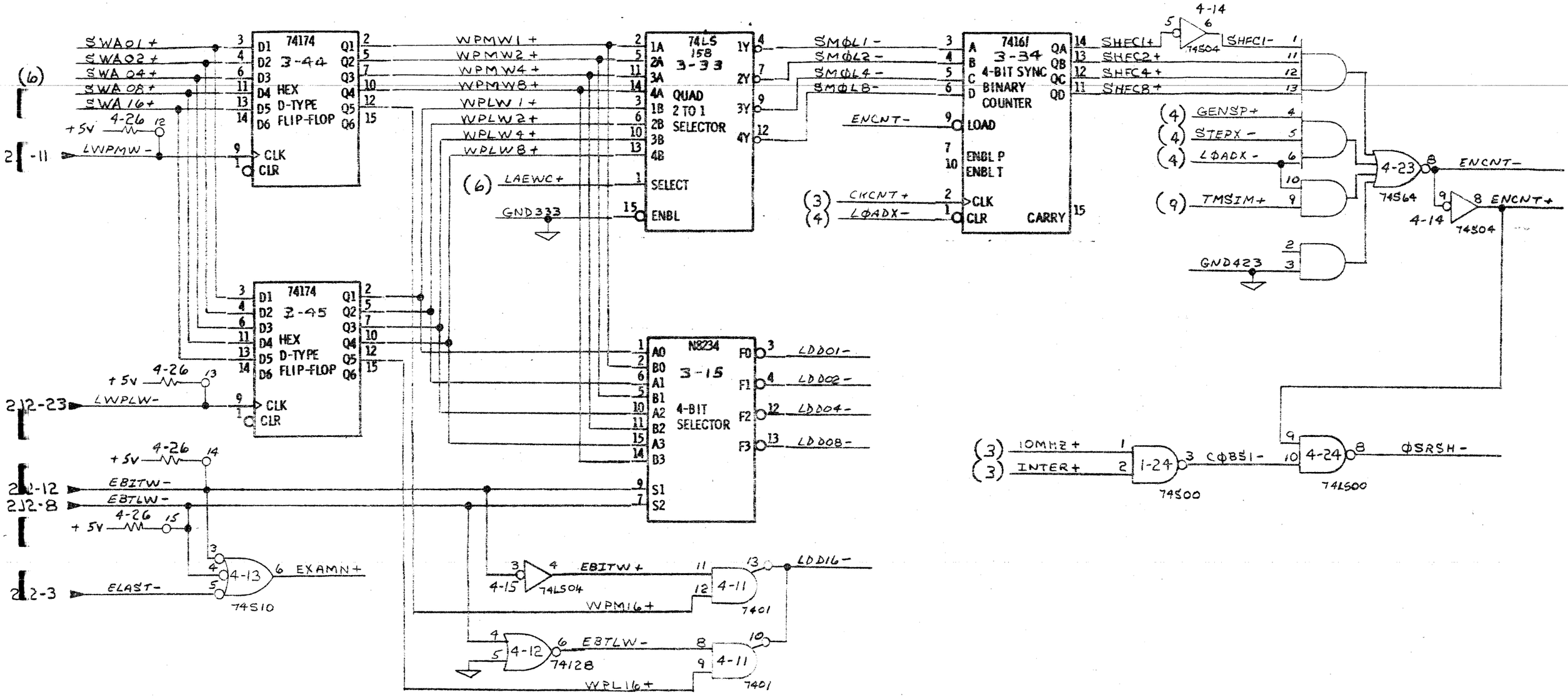
| ASSY 1 LBD, LOWER LOGIC PNL. FOR RS-648 | |
|---|---|
| 648-302 | SHT 3 OF 11 |

(1001 1306, SHT. 3 OF 11)




PROGRAM SWITCH CONTROL PROGRAM

| ASSY/ LBD, LOWER LOGIC PWR. FOR RS-648 | |
|---|---|
| 648-302 | SHT 4 OF 17 |




WORDS PER MEMORY WORD LOGIC

| | |
|---|---|
| ASSY/LBD, LOWER LOGIC PNL. FOR RS-648 | |
| 648-302 | SHT 5 OF 10 |

SWA01+
SWA02+
SWA04+
SWA08+
BCNT1+
BCNT2+
BCNT3+
BCNT4+
FETCH-
SMDUR-
74LS157 3-41 QUAD 2 TO 1 SELECTOR
SWØ01+
SWØ02+
SWØ03+
SWØ04+
74163 3-31 4-BIT SYNC BINARY COUNTER
LOAD
ENBL P
ENBL T
CLK
CLR
CARRY
WCNT1+
WCNT2+
WCNT3+
WCNT4+
74179 3-21 4-BIT PARALLEL SHIFT REGISTER
+5V
PUL36+ 2-36
CLR
CLK
ENCNT+
GND321
LOAD SERIAL SHIFT
BCNT1+
LAST1+
BCNT2+
LAST2+
BCNT3+
LAST3+
BCNT4+
LAST4+
N8234 3-13 4-BIT SELECTOR
A0 B0 A1 B1 A2 B2 A3 B3
F0 F1 F2 F3
S1 S2
LDD01-
LDD02-
LDD04-
LDD08-
4-22
LAD01-
LAD02-
LAD04-
LAD08-
2J1
12
26
13
17
SWA16+
SWA32+
74LS157 3-42 QUAD 2 TO 1 SELECTOR
SWØ05+
SWØ06+
LØADX-
ENCNT+
CKCNT+
WCNT5+
WCNT6+
SWEWC+
LAEWC+
CKCNT-
GND322
BCNT5+
LAST5+
BCNT6+
LAST6+
SYNCW+
LAEWA+
N8234 3-14 4-BIT SELECTOR
LDD16-
LDD32-
LAD16-
LAD32-
2J1
25
22
ELAST-
EXAMN+
4-14
74S04
RSTCN-
74LS00
1-25
1-15
1-26
74LS08
LØADD-
MANI3+
LØADB+
4-12
74128
WRITE-
INHIB-
SWBSB-
WCNT1+
WCNT2+
WCNT3+
WCNT4+
WCNT5+
WCNT6+
WCNT6-
74174 3-46 HEX D-TYPE FLIP-FLOP
D1 D2 D3 D4 D5 D6
Q1 Q2 Q3 Q4 Q5 Q6
4-26 1
LLASW-
2J2-17
N8242 4-34 4-BIT COMPARATOR
N8242 4-35 4-BIT COMPARATOR
N8242 4-36 4-BIT COMPARATOR
A0 A1 A2 A3
B0 B1 B2 B3
LAST1+
LAST2+
LAST3+
LAST4+
LAST5+
LAST6+
SWA16+
SWA32+
+5V
4-26
LAEWC+
SWEWC+
SWEWC+
SWASW-
SWDSB-
SWASW+
4-16
4-14
74S04
74LS00
CLOCK+
3-35
74174
3J1-16
SDYNU-
SWDSB-
MEMORY ADDRESS LOGIC
ASSY/LBD, LOWER LOGIC PNL.
FOR 25-648
648-302
SHT 6 OF 17

J1-5 SWU08+ 1 A0 N8235 3-11 F0 3 DØTB1-
3J1-7 SWD02+ 2 B0 F1 4 DØTB2-
J1-15 SWU04+ 6 A1 F2 12 DØTB3-
3J1-11 SWD04+ 5 B1 F3 13 DØTB4-
2J1-1 SWU02+ 10 A2 4-BIT
3J1-26 SWD06+ 11 B2 SELECTOR
J1-19 SWU01+ 15 A3
2J2-18 SWD08+ 14 B3
9 S1
7 S2

+5V 3-16
5 6 7 9

J1-4 SWT08+ 1 A0 N8235 3-12 F0 3 DØTB5-
2J2-22 SWD10+ 2 B0 F1 4 DØTB6-
2J1-16 SWT04+ 6 A1 F2 12 DØTB7-
2J2-25 SWD12+ 5 B1 F3 13 DØTB8-
J1-2 SWT02+ 10 A2 4-BIT
2J2-28 SWD14+ 11 B2 SELECTOR
2J1-18 SWT01+ 15 A3
2J2-2 SWD16+ 14 B3
+5V 9 S1
2-36 SELCT- 7 S2
11 SELCT+

51 M0015+ 1-15 74S04 M0015-

WCNT1+
WCNT2+
(6) WCNT3+
WCNT4+

2J1-27 SWH08- 4 D1 7489 2-15 16 x 4 RAM Y1 5 MMH08+
2J1-7 SWH04- 6 D2 Y2 7
2J1-6 SWH02- 10 D3 Y3 9
2J1-21 SWH01- 12 D4 Y4 11
MEM ENBL 2
(9) TMS1M+ 5 1-25 6 MEWG1- WRITE ENBL 3
74S00

SWH08- 2 1-13 1 74LS01
MMH04+ 3
SWH04- 5 1-13 4 74LS01
MMH02+ 6
SWH02- 8 1-13 10 74LS01
MMH01+ 9
WDGEN+ 11 1-13 13 74LS01
SWH01- 12

2J1-20 SWTMU+ 4 D1 7489 2-16 16 x 4 RAM Y1 5 MEMDU-
2J1-28 SWTMN+ 6 D2 Y2 7
10 D3 Y3 9
12 D4 Y4 11
MEM ENBL 2
(6) WRITE- WRITE ENBL 3

MEMDU- 1-14 SWTMU+ 2 3 1 74LS01
MEMDN- 5 6 4 74LS01
SWTMN+ 8 9 10 74LS01
11 12 13 74LS01

3J1-20 SWD01+ 4 D1 7489 2-11 16 x 4 RAM Y1 5 MMD01-
3J1-9 SWD03+ 6 D2 Y2 7
10 D3 Y3 9
12 D4 Y4 11
MEM ENBL 2
WRITE- WRITE ENBL 3

1 2 3 4 5 6 7 9 +5V 2-35

3J1-25 SWD05+ 4 D1 7489 2-12 16 x 4 RAM Y1 5 MMD05-
3J1-27 SWD07+ 6 D2 Y2 7
10 D3 Y3 9
12 D4 Y4 11
MEM ENBL 2
WRITE- WRITE ENBL 3

MMD05-
MMU02+
MMD07-
MMU01+

2J2-21 SWD09+ 4 D1 7489 2-13 16 x 4 RAM Y1 5 MMD09-
DØTB5- 6 D2 Y2 7
2J2-24 SWD11+ 10 D3 Y3 9
DØTB6- 12 D4 Y4 11
MEM ENBL 2
WRITE- WRITE ENBL 3

MMD09-
MMT08+
MMD11-
MMT04+

10 11 12 13 14 15 +5V 2-35
1 2 2-36 +5V

2J2-13 SWD13+ 4 D1 7489 2-14 16 x 4 RAM Y1 5 MMD13-
DØTB7- 6 D2 Y2 7
2J2-27 SWD15+ 10 D3 Y3 9
DØTB8- 12 D4 Y4 11
MEM ENBL 2
WRITE- WRITE ENBL 3

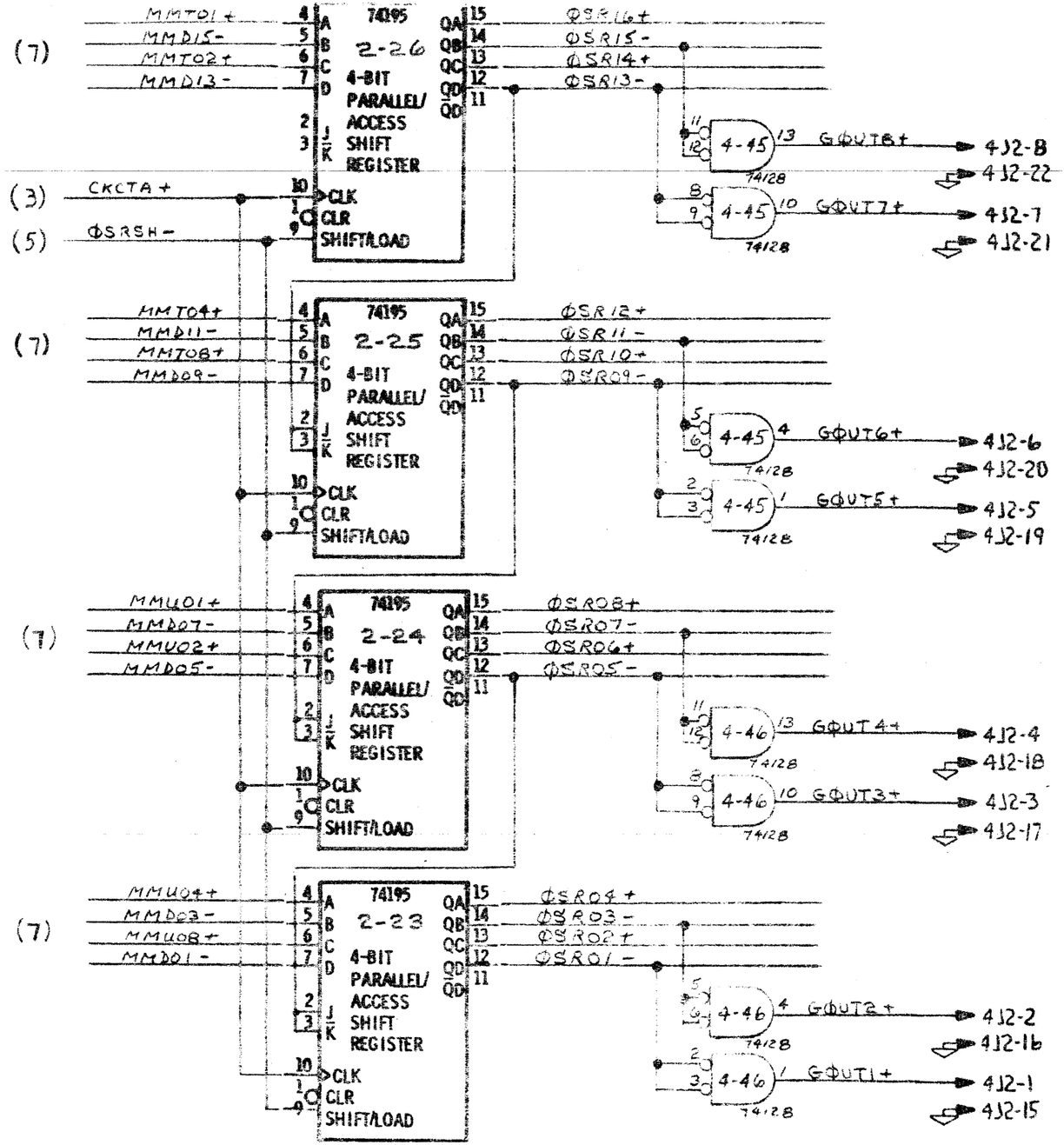
MMD13-
MMT02+
MMD15-
MMT01+

+5V 3-16
10
SELCT- 9 4-15 8 SELCT+ 74LS04

STANDARD 16 WORD MEMORY LOGIC

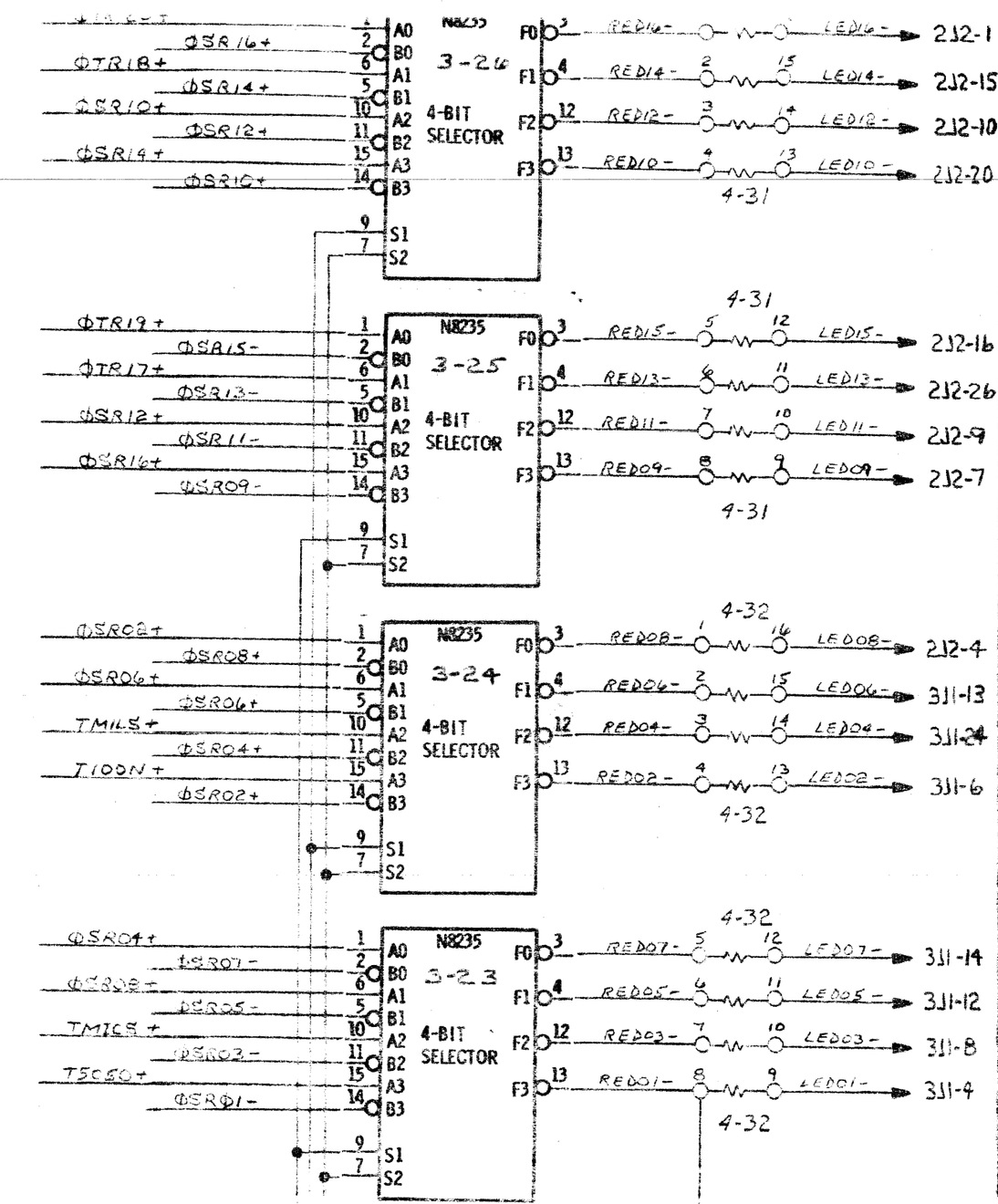
| ASSY/LBD, LOWER LOGIC PNL. FOR RS-648 | |
|---|---|
| 648-302 | SHT 7 OF 10 |

(1001 1366. SHT. 7 OF 11)




* NOTE: EEDAT- ⇒ ENABLE EVEN DATA BITS
IF EXAM DATA • WG OR EXAM DATA • T5050

ENTIM- ⇒ ENABLE TIME IF
EXAM TIME • TS • $\overline{T5050}$




TIMING AND OUTPUT REGISTER, 16 LED DISPLAY SELECT

| ASSY LRD, LOWER LOGIC PNL FOR RS-648 | |
|---|---|
| 648-302 | SHT 8 OF 10 |

74162 2-31 4-BIT SYNC DECADE COUNTER — LOAD, ENBLP, ENBLT, CLK, CLR, CARRY — QA QB QC QD — 800NS+

74162 2-32 4-BIT SYNC DECADE COUNTER — LOAD, ENBLP, ENBLT, CLK, CLR, CARRY — QA QB QC QD — 100KH+

74162 2-33 4-BIT SYNC DECADE COUNTER — LOAD, ENBLP, ENBLT, CLK, CLR, CARRY — QA QB QC QD — 10KHZ+

74162 2-34 4-BIT SYNC DECADE COUNTER — LOAD, ENBLP, ENBLT, CLK, CLR, CARRY — QA QB QC QD — 800US+

(3) CLOCK+ ENABL-

MHZCK+

1KHZC+

+5V 2-36

(7) MEMDU- CKCNT+ 2-21 74109 — 6 ΦTMRU- 7 ΦTMRU+

+5V 2-36

(7) MEMDN- 2-21 74109 — 10 ΦTMRN- 9 ΦTMRN+

1-26 74LS08 — 3 TMILS+

1-26 74LS08 — 6 TMICS+

1-26 74LS08 — 8 T100N+

1-24 74S00 — T5050-

1-15 74S04 — 8 T5050+

2J2-14 +5V SELAD-

4-15 74LS04 — SELAD+

(6) SYNCW+ (3) CKCNT+ (3) EXTER+ (3) SINGL- — 4-21 74S00 — CTBS7-

4-21 74S00 — SYNC1+

1-16 74S20 — CTBS6-

4-33 74128 — SYNCP- → 3J2-4, 3J2-18

4-33 74128 — SYNCΦ- → 4J2-10, 4J2-24

(3) ENINC+ — 4-21 74S00 — CTBS1-

1-15 74S04 — CTBS1+

(3) 10MHZ- — 3-36 74S112 J K — SYNC2+

ΦTMRU+ 800NS+ — 4-24 74LS00 — CTBS8-

SELAD- ENABL- — 4-25 74LS20 — CTBS3+

ΦTMRU- — 4-24 74LS00 — CTBS9-

SYNC2-

ΦTMRN- — 4-24 74LS00 — RSSYN+

10MHZ- — 4-13 74S10 — RSSYN-

3J1-5 TMSIM+ — 4-33 74128 — WDGEN+

SYNC2-

EXTER+ ΦTMRN+ ΦTMRU+ MHZCK+ — 1-53 74S64 — ENABL-

1-15 74S04 — ENABL+

TIMING AND SYNC GENERATION LOGIC

| ASSY/LBD, LOWER LOGIC PNL. FOR RS-648 | |
|---|---|
| 648-302 | SHT 9 OF 10 |

(1001 1306, SHT 9 OF 11)

74162 2-31 4-BIT SYNC DECADE COUNTER — LOAD, ENBLP, ENBLT, CLK, CLR, CARRY — QA QB QC QD — 800NS+

74162 2-32 4-BIT SYNC DECADE COUNTER — LOAD, ENBLP, ENBLT, CLK, CLR, CARRY — QA QB QC QD — 100KH+

74162 2-33 4-BIT SYNC DECADE COUNTER — LOAD, ENBLP, ENBLT, CLK, CLR, CARRY — QA QB QC QD — 10KHZ+

74162 2-34 4-BIT SYNC DECADE COUNTER — LOAD, ENBLP, ENBLT, CLK, CLR, CARRY — QA QB QC QD — 800US+

3) CLOCK+, ENABL−

MHZCK+

+5V, 2-36

(7) MEMDU−, CKCNT+ — 2-21, 74109 — ΦTMRU−, ΦTMRU+

+5V, 2-36

(7) MEMDN− — 2-21, 74109 — ΦTMRN−, ΦTMRN+

1-26, 74LS08: 3 TMILS+, 6 TMICS+, 8 T100N+

1-24, 74500: T5050−

1-15, 74504: T5050+

1KHZC+

3J1-5 TMSIM+ — 4-33, 74128 — WDGEN+

232-14 SELAD− (4-15) — 1-15, 74504 — SELAD+

(6) SYNCW+, (3) CKCNT+, (3) EXTER+, (3) SINGL− — 1-16, 74S20 — CTBS6−

4-21, 74500: CTBS7−, 4-21 — SYNC1+

4-33, 74128: SYNCP− → 3J2-4, 3J2-18; SYNCØ− → 4J2-10, 4J2-24

(3) ENINC+ — 4-21, 74500 — CTBS1−

1-15, 74504: CTBS1+

3-36, 74S112: SYNC2+, SYNC2−

(3) 10MHZ−

ΦTMRU+, 800NS+ — 4-24, 74LS00 — CTBS8−

SELAD−, ENABL− — 4-25, 74LS20 — CTBS3+

ΦTMRU− — 4-24, 74LS00 — CTBS9−

10MHZ−

ΦTMRN− — 4-24, 74LS00 — RSSYN+

4-13, 74S10: RSSYN−

SYNC2−

EXTER+, ΦTMRN+, ΦTMRU+, MHZCK+ — 1-53, 74S64 — ENABL−

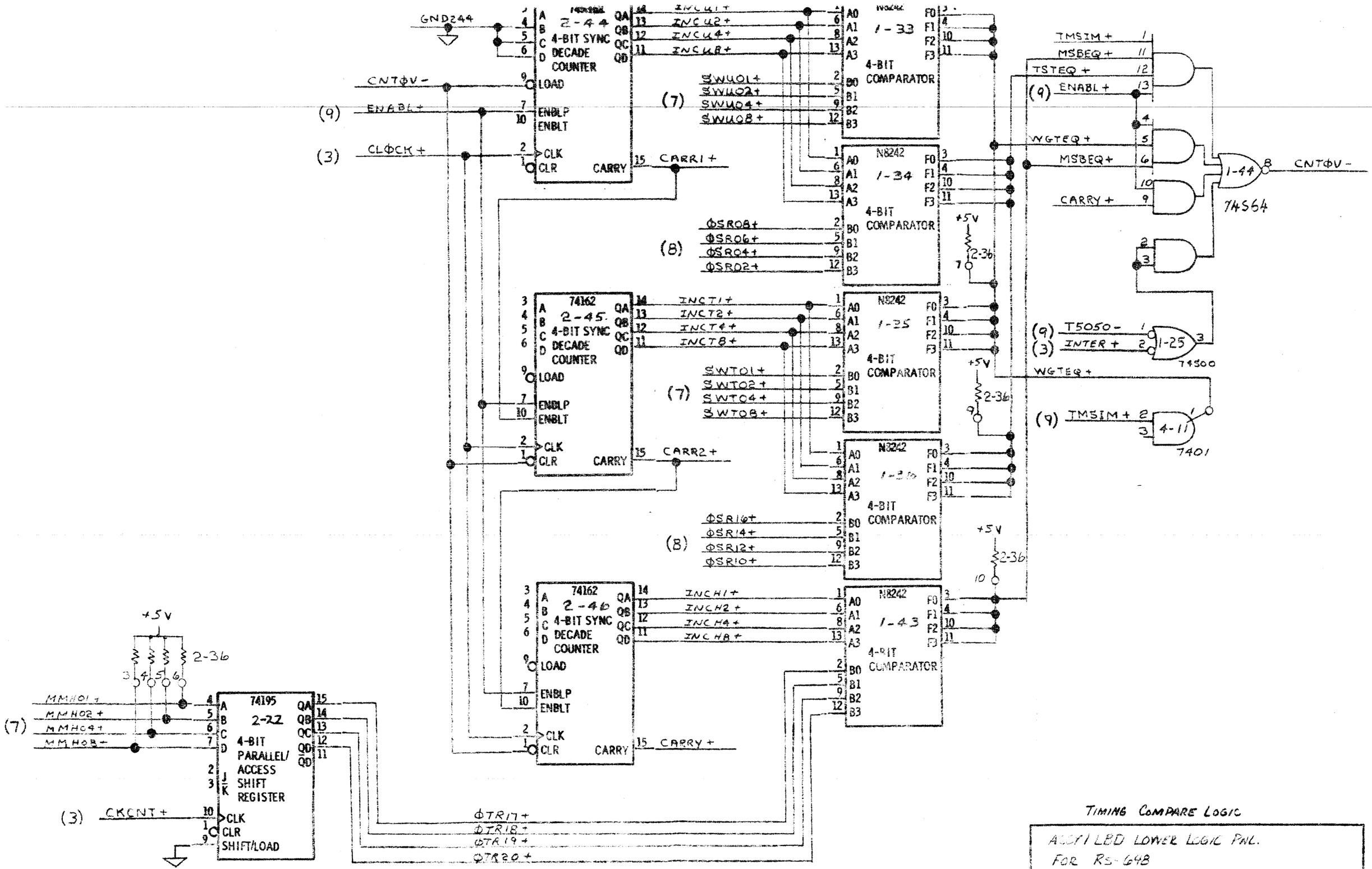
1-15, 74504: ENABL+

# TIMING AND SYNC GENERATION LOGIC

ASSY/LBD, LOWER LOGIC PNL. FOR RS-648

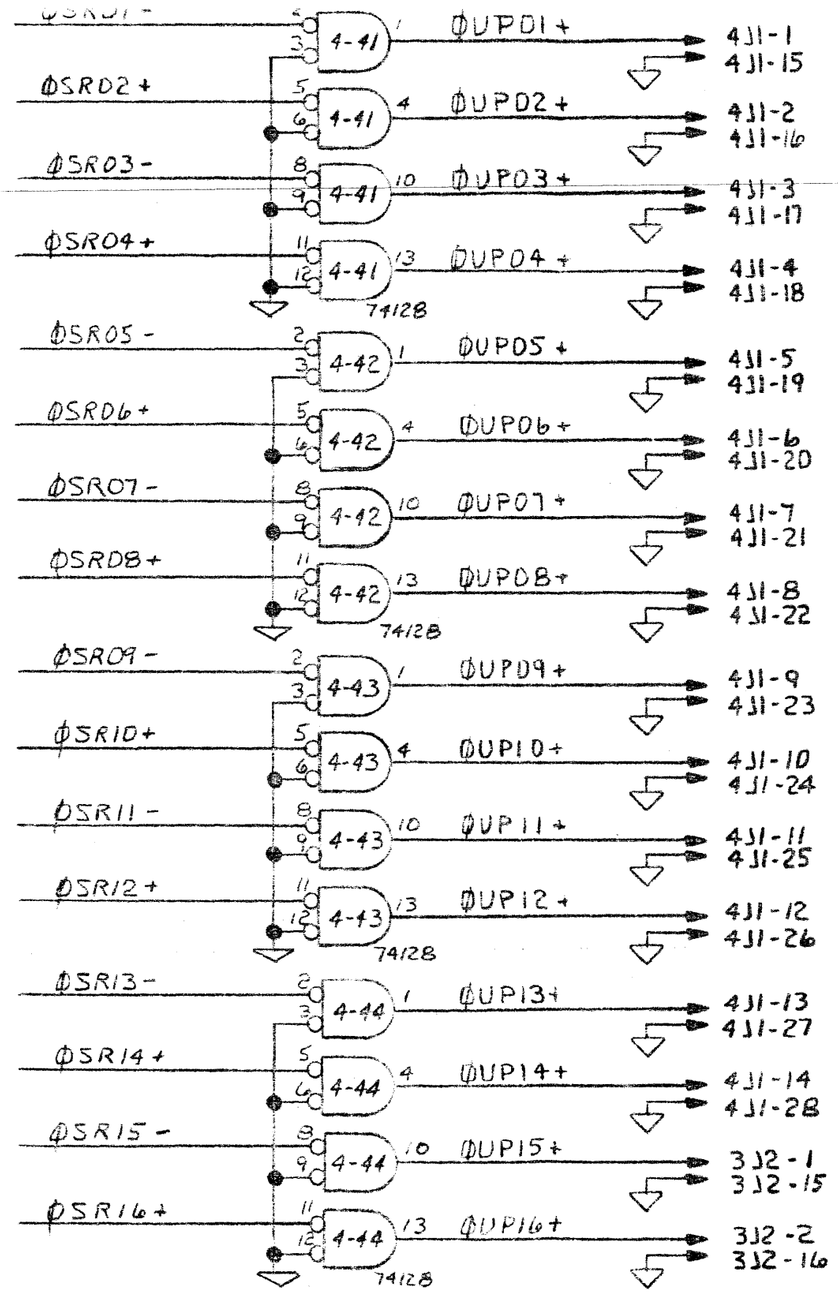
| 648-302 | SHT 9 OF 10 |
|---|---|

(1001 1306, SHT 9 OF 11)




TIMING COMPARE LOGIC

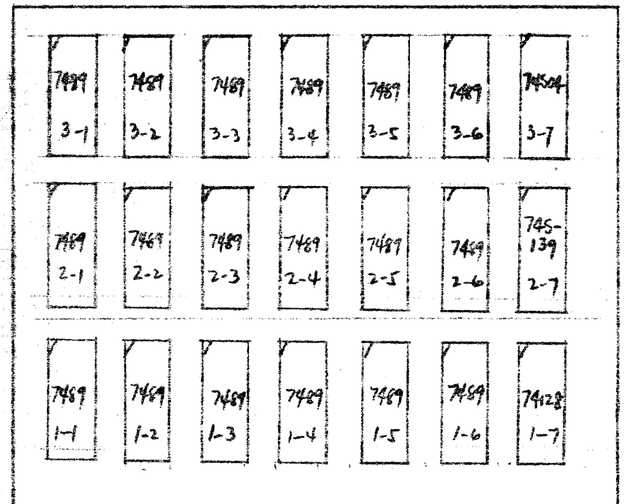
| | |
|---|---|
| ASSY LED LOWER LOGIC PWL. FOR RS-648 | |
| 648-302 | SHT 10 OF 10 |



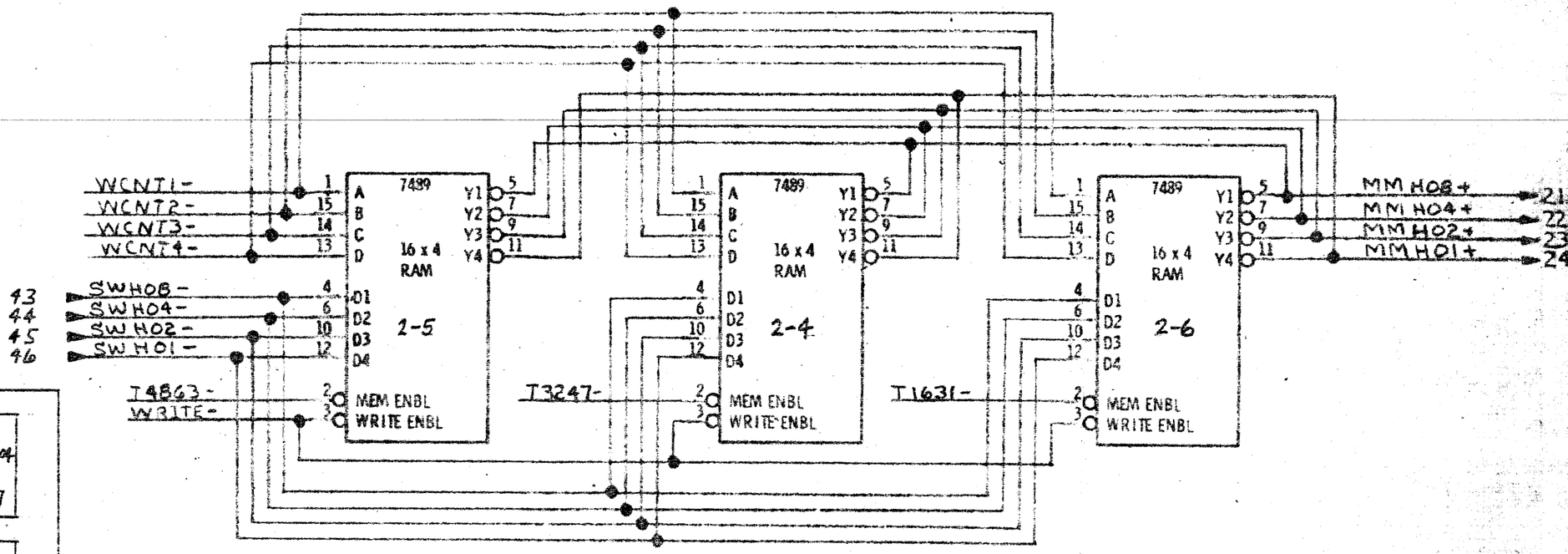

NOTE: ALL INPUTS FROM 648-302 SHT 8

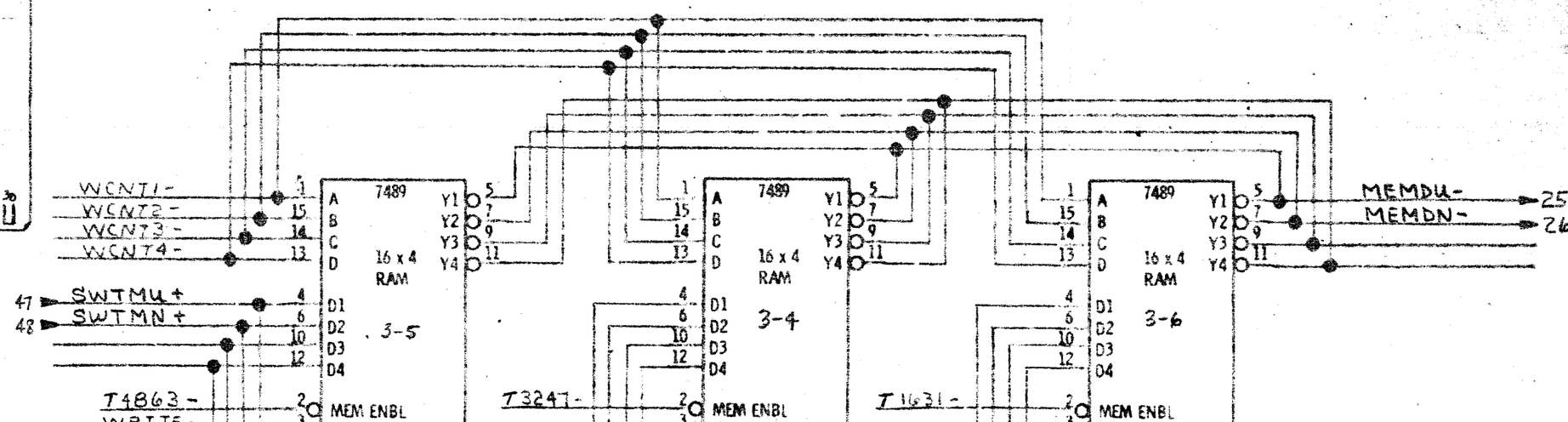
16 OUTPUT OPTION

| | | |
|---|---|---|
| INTERFACE TECHNOLOGY | | |
| | ASSY LSD LOWER LOGIC PNL. FOR RS 648 | |
| 7/1/74 | 648-304 | SHT 1 OF 1 |




COMPONENT SIDE VIEW

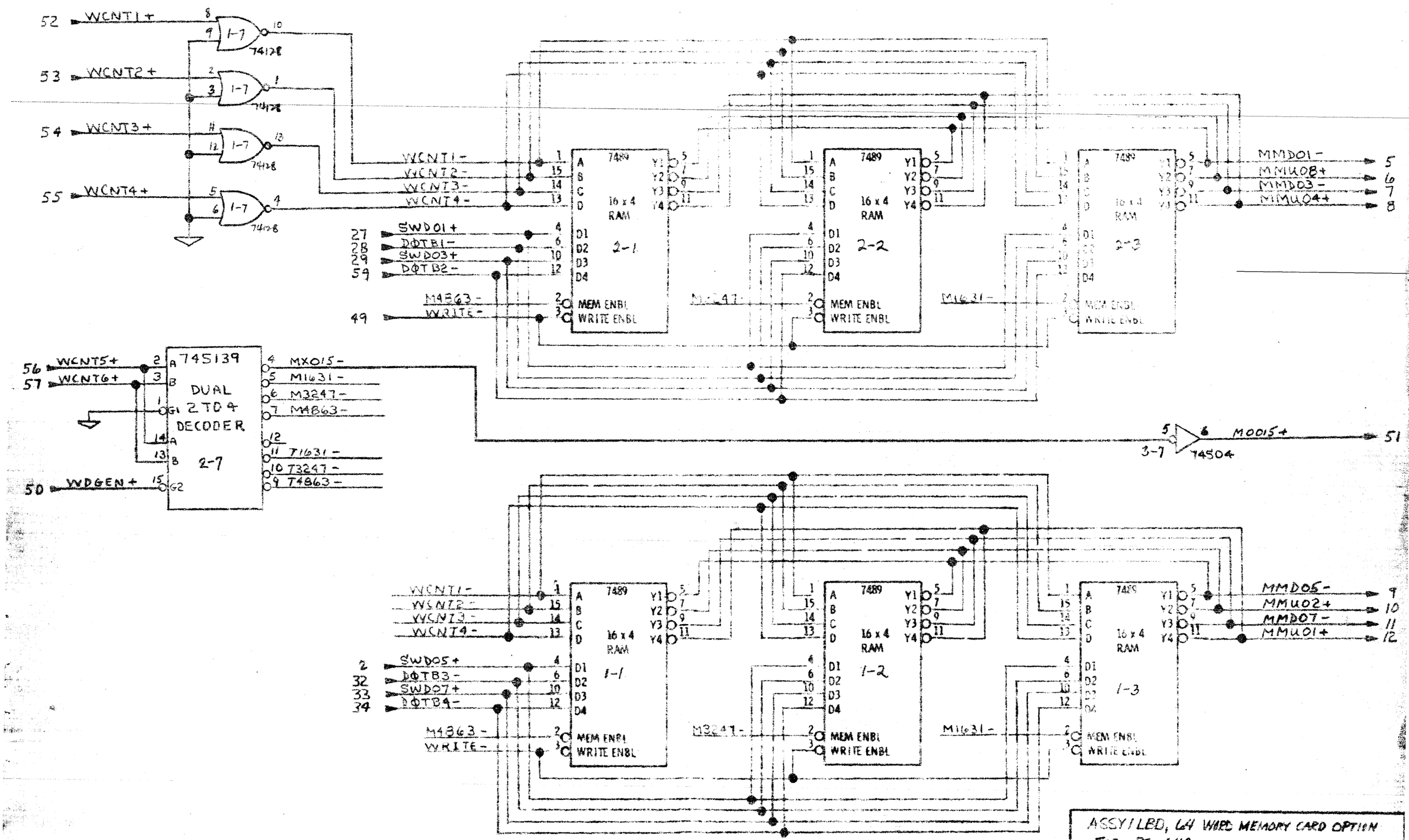



ASSY/LBD, 64 WORD MEMORY CARD OPTION FOR RS-648

| 648-302 | SHT 7A OF 10 |
|---|---|

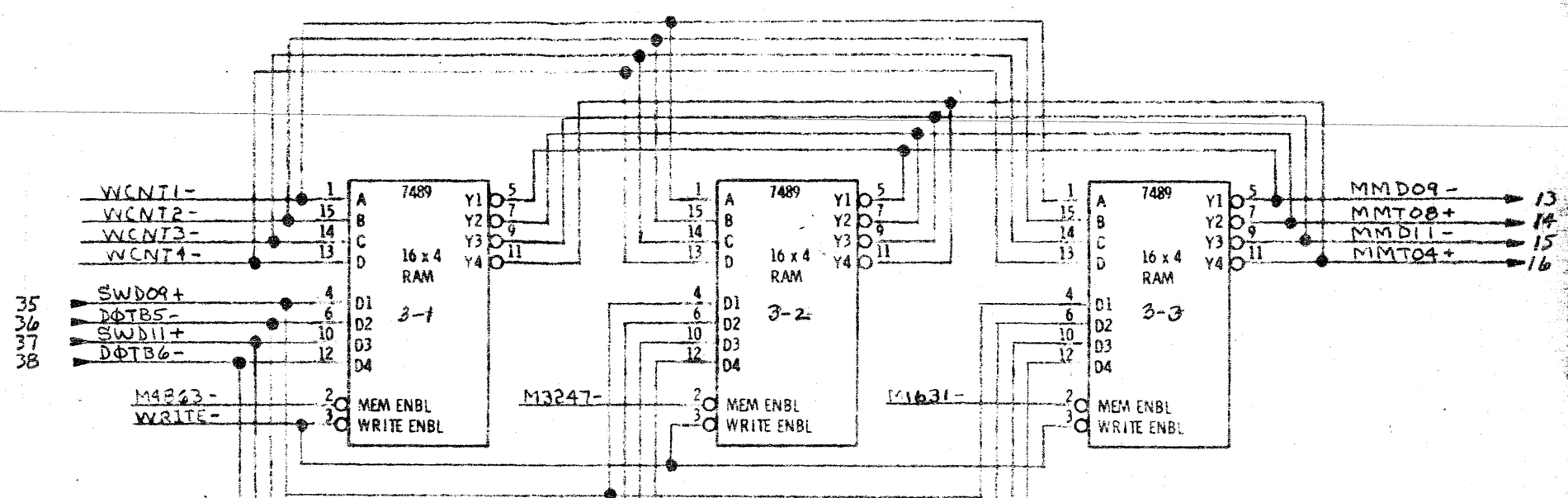
(1001 1117, SHT. 1 OF 3)

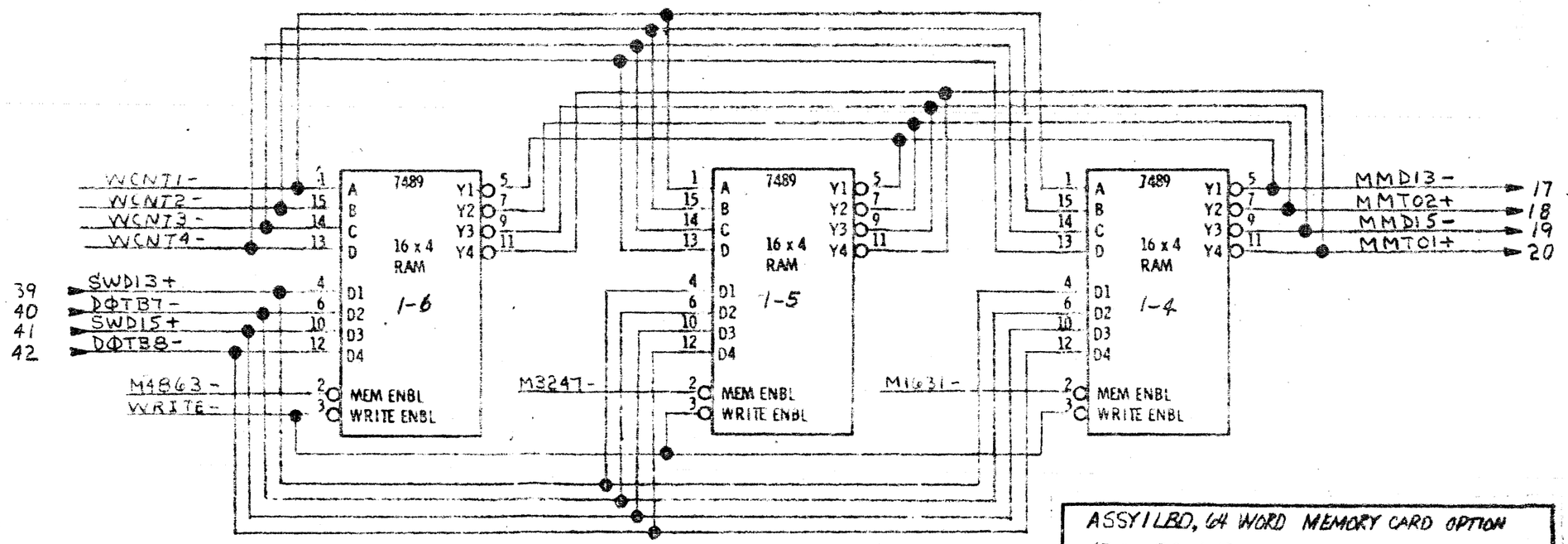



ASSY/LBD, 64 WORD MEMORY CARD OPTION FOR RS-648

| 648-302 | SHT 7B OF 11 |
|---|---|

(1001 UIT. SHT. 2 OF 3)

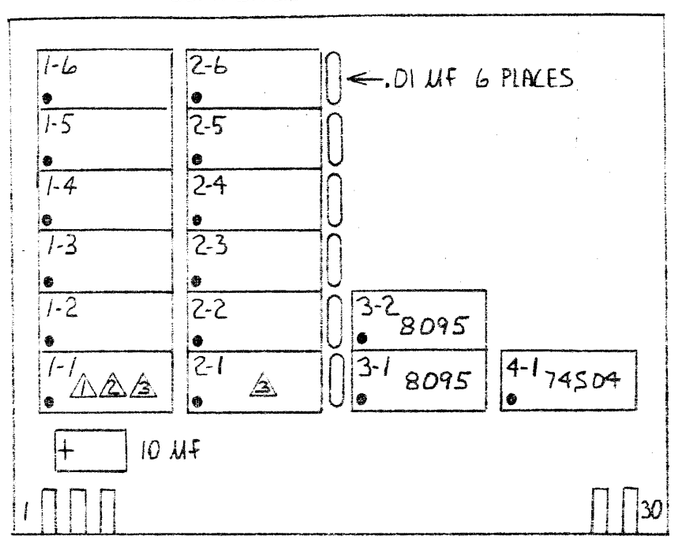


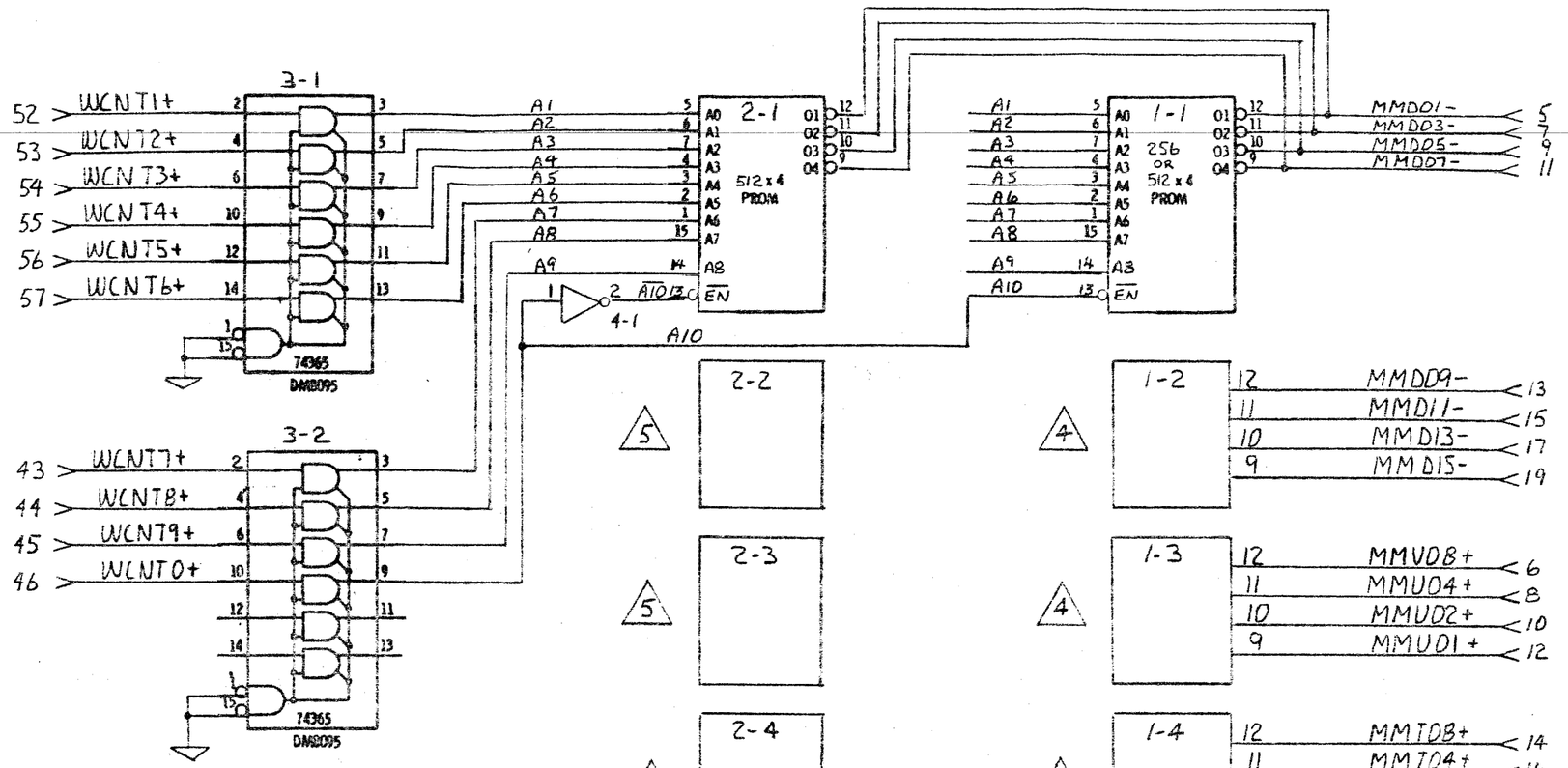




ASSY LBD, 64 WORD MEMORY CARD OPTION FOR RS-64B

| 648-302 | SHT 7C OF 10 |
|---|---|

(1001 1117, SHT 3 OF 3)




6 REFERENCE WIRELIST 10011083

⚠5 ADDRESS LINES COMMON TO IC 2-1

⚠4 ADDRESS LINES COMMON TO IC 1-1

⚠3 FOR 1K WORD CARD INSTALL HM7621 (512×4)
IN IC LOCATIONS 1-1 THRU 1-6
AND 2-1 THRU 2-6

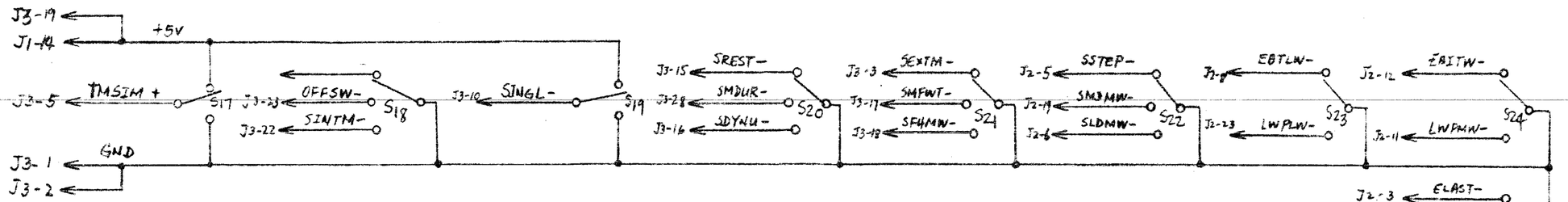
⚠2 FOR 512 WORD CARD INSTALL HM7621 (512×4)
IN IC LOCATIONS 1-1 THRU 1-6

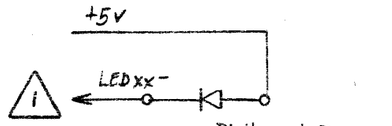
⚠1 FOR 256 WORD CARD INSTALL HM7611 (256×4)
IN IC LOCATIONS 1-1 THRU 1-6

NOTES

(1) All Prom Cards must be located in 1K R.A.M. slot.
(2) Remove 256 RAM Card and 1K RAM Card if present.
(3) Remove 4 RAM I.C.s in locations 3-3, 3-4, 4-3, and 4-4 on control card if present.

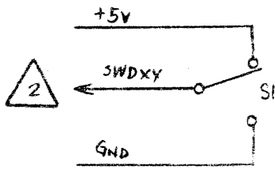
| INTERFACE TECHNOLOGY | | |
|---|---|---|
| ASSY/LBD, RS648 256/1K PROM CARD | | |
| SH 1 OF 1 | 55613 | DRAWING NO 10011082 |



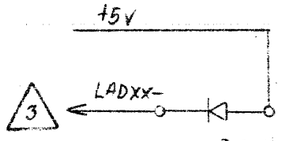




D1 through D16
typical of 16 data
LED's

| | | | |
|---|---|---|---|
| LED01- | J3-4 | LED09- | J2-7 |
| LED02- | J3-6 | LED10- | J2-20 |
| LED03- | J3-8 | LED11- | J2-9 |
| LED04- | J3-24 | LED12- | J2-10 |
| LED05- | J3-12 | LED13- | J2-26 |
| LED06- | J3-13 | LED14- | J2-15 |
| LED07- | J3-14 | LED15- | J2-16 |
| LED08- | J2-4 | LED16- | J2-1 |

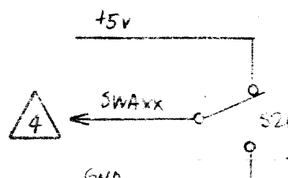



S1 through S16
typical of 16 data
switches



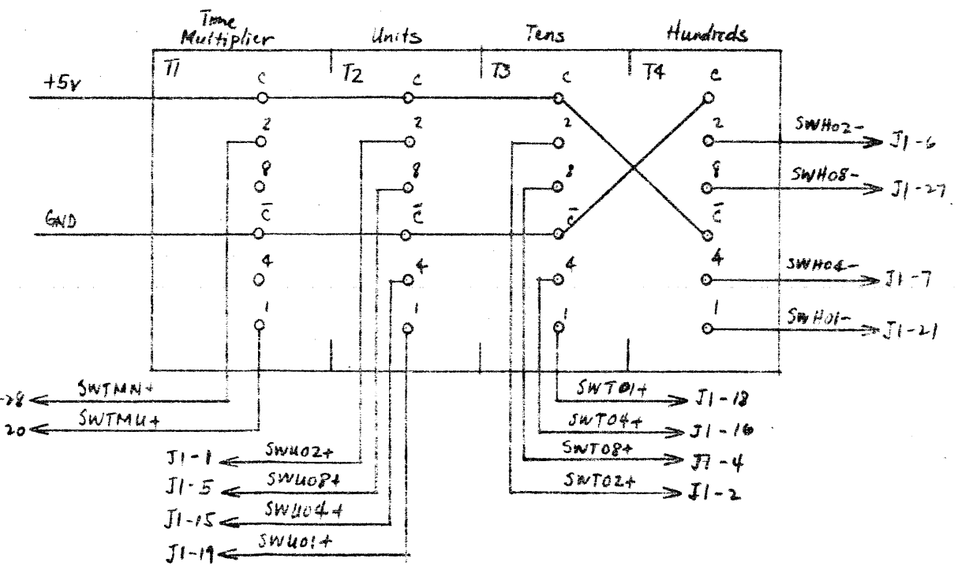

D17 through D22
typical of 6 address
LED's

| | |
|---|---|
| LAD01- | J1-12 |
| LAD02- | J1-26 |
| LAD04- | J1-13 |
| LAD08- | J1-17 |
| LAD16- | J1-25 |
| LAD32- | J1-22 |




S26 through S31
typical of 6 address
switches

| | |
|---|---|
| SWA01+ | J1-10 |
| SWA02+ | J1-24 |
| SWA04+ | J1-11 |
| SWA08+ | J1-9 |
| SWA16+ | J1-23 |
| SWA32+ | J1-8 |



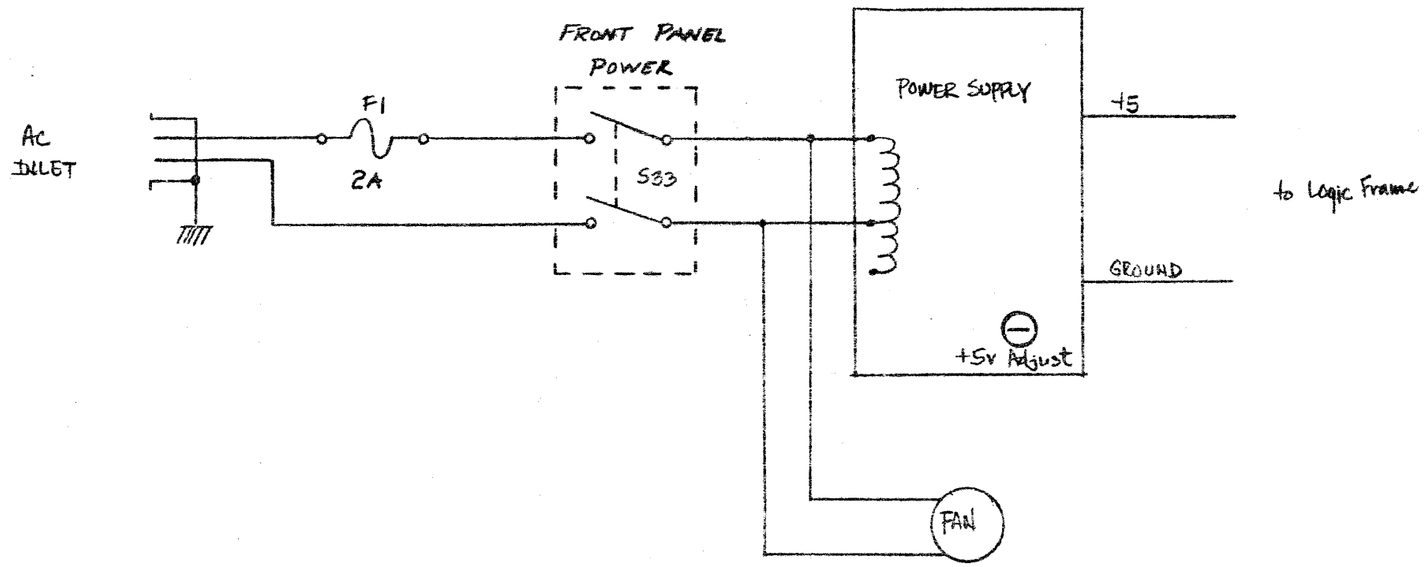

Thumbwheel Switches

| | | | |
|---|---|---|---|
| SWD01+ | J3-20 | SWD09+ | J2-21 |
| SWD02+ | J3-7 | SWD10+ | J2-22 |
| SWD03+ | J3-9 | SWD11+ | J2-24 |
| SWD04+ | J3-11 | SWD12+ | J2-25 |
| SWD05+ | J3-25 | SWD13+ | J2-13 |
| SWD06+ | J3-26 | SWD14+ | J2-28 |
| SWD07+ | J3-27 | SWD15+ | J2-27 |
| SWD08+ | J2-18 | SWD16+ | J2-2 |

Note: J1 on this drawing is 2-J1 on sht 2 of 648-302; J2 on this drawing is 2-J2 and J3 on this drawing is 3-J1.

INTERFACE TECHNOLOGY

| | | |
|---|---|---|
| | ASSY LED FRONT PNL FOR RS-645 | |
| 7/1/74 | 648-105 | SHT 1 OF 1 |




RS-648 AC POWER SCHEMATIC DIAGRAM

INTERFACE TECHNOLOGY

| | | |
|---|---|---|
| | TOP ASSY FOR RS-648 | |
| 7/1/74 | 648-203 | SHT 1 OF 1 |

(1001 1283, SHT. 2 OF 2)