TEK SERVICE MANUAL

070-4342-01
PRODUCT GROUP 57
(part of pkg. 062-7124-02)

The 1240/1241 Logic Analyzer

SERVICE MANUAL, VOL. I

PLEASE CHECK FOR CHANGE INFORMATION
AT THE REAR OF THIS MANUAL.

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Tektronix®
COMMITTED TO EXCELLENCE

WARNING

THE FOLLOWING SERVICING INSTRUCTIONS ARE FOR USE BY QUALIFIED PERSONNEL ONLY. TO AVOID PERSONAL INJURY, DO NOT PERFORM ANY SERVICING OTHER THAN THAT CONTAINED IN OPERATING INSTRUCTIONS UNLESS YOU ARE QUALIFIED TO DO SO. REFER TO OPERATORS SAFETY SUMMARY AND SERVICE SAFETY SUMMARY PRIOR TO PERFORMING ANY SERVICE.

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MANUAL REVISION STATUS

PRODUCT: 1240/1241 LOGIC ANALYZER SERVICE MANUAL VOL. I

This manual supports the following versions of this product: All

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PREFACE

The 062-7124-02 manuals package consists of the *1240/1241 Service Manual* (volumes 1 and 2) and various addenda. The *1241 Service Manual Addendum*, included in the two-volume set, provides additional support for the 1241 Logic Analyzer. Each manual and addendum in the set has its own part number starting with the prefix 070. Manual part numbers are located on the manual title page.

The *1240/1241 Service Manual* provides information that allows service technicians to check, troubleshoot, repair, and maintain the 1240 and 1241 Logic Analyzers. When servicing a 1241 Logic Analyzer, use both volumes of the service manual and the *1241 Service Manual Addendum* to find complete troubleshooting information. For detailed operating instructions, refer to the *1240/1241 Operator's Manual*.

This manual is designed for use by a qualified service technician having moderate experience with digital circuitry. Familiarity with both TTL and ECL logic families is assumed. Familiarity with and the ability to operate standard test instruments used on digital circuitry, such as an oscilloscope or logic analyzer, is also assumed.

Troubleshooting of the 1240 and 1241 Logic Analyzers is based on the internal diagnostics. The diagnostics produce an on-screen error index message that allows the service technician to quickly identify instrument failure. This manual translates these error indexes into a list of probable causes for instrument failure and lists recommended repair actions.

This manual is divided into 12 sections, found in two volumes. Each section is preceded by a tabbed page for quick reference. Other reference aids included:

- **Manual Table of Contents** – refer to the Table of Contents at the beginning of the manual for a breakdown of sections.
- **Section Table of Contents** – refer to the Table of Contents at the beginning of each section for a detailed breakdown of section contents.
- **Diagnostic Page-Bleed Tabs** – refer to the *Troubleshooting and Repair* section for page-edge bleed tabs that indicate, by their vertical page position, which module's diagnostic information is currently being accessed.

WHAT THIS MANUAL CONTAINS

VOLUME 1

Section 1 – GENERAL INFORMATION. Provides a basic description of the logic analyzers and an overview of the instrument controls and indicators. It also describes the operating and diagnostic menu layouts.

Section 2 – SPECIFICATIONS. Lists electrical, mechanical, and environmental specifications of the logic analyzer.

Section 3 – OPERATING INFORMATION. Describes the logic analyzer's power requirements, and lists the probe, pack, and I/O connections. Refer to the *1240/1241 Operator's Manual* for complete operating instructions.

Section 4 – THEORY OF OPERATION. Illustrates basic operation by introducing logical function blocks and by showing their relationship to the instrument modules. Also, this section describes the system architecture and the difference between the 1240D1 and 1240D2 acquisition cards.

Section 5 – VERIFICATION AND ADJUSTMENT PROCEDURES. Contains functional check procedures, adjustment procedures, and performance verification procedures.

Section 6 – DISASSEMBLY AND INSTALLATION PROCEDURES. Describes disassembly and reassembly procedures for instrument pieces.

Section 7 – MAINTENANCE. Contains information necessary to maintain the logic analyzers, including general precautions and preventive and corrective maintenance items.

Section 8 – TROUBLESHOOTING AND REPAIR. Contains information on the diagnostic tests. The diagnostic test descriptions, associated error indexes, and probable failure causes and solutions are grouped by module name with page-bleed tabs. Also provided are recommended repair practices for parts of the instrument not tested by diagnostics.

VOLUME 2

Section 9 – REPLACEABLE ELECTRICAL PARTS. Contains a list (including Tektronix part numbers) of all replaceable electrical parts in the logic analyzers.

Section 10 – SCHEMATIC DIAGRAMS. Contains schematics as well as board and component locator diagrams and tables. The schematic diamond numbers refer to instrument theory discussions located in the *Theory of Operation* section.

Section 11 – REPLACEABLE MECHANICAL PARTS. Contains a list (including Tektronix part numbers) of all replaceable mechanical parts in the logic analyzers and provides illustrations to show the location of each of these parts.

Section 12 – GLOSSARY. Provides an alphabetical list of signal names and their corresponding descriptions.

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OPERATOR'S SAFETY SUMMARY

The general safety information in this summary is for both operator and service personnel. Specific cautions and warnings are found throughout the manual where they apply, but may not appear in this summary.

TERMS IN THIS MANUAL

CAUTION statements identify conditions or practices that could result in damage to the equipment or other property.

WARNING statements identify conditions or practices that could result in personal injury or loss of life.

TERMS AS MARKED ON EQUIPMENT

CAUTION indicates a personal injury hazard not immediately accessible as one reads the marking, or a hazard to property including the equipment itself.

DANGER indicates a personal injury hazard immediately accessible as one reads the marking.

SYMBOLS AS MARKED ON EQUIPMENT


DANGER — High voltage.


Protective ground (earth) terminal.


ATTENTION — refer to manual.

GROUNDING THE PRODUCT

This product is intended to operate from a power source that does not apply more than 250 volts rms between the supply conductors or between either supply conductor and ground.

This product is grounded through the grounding conductor of the power cord. To avoid electrical shock, plug the power cord into a properly wired receptacle before connecting to the product. A protective-ground connection by way of the grounding conductor in the power cord is essential for safe operation.

DANGER ARISING FROM LOSS OF GROUND

Upon loss of the protective-ground connection, all accessible conductive parts (including knobs and controls that may appear to be insulating) can render an electric shock.

USE THE PROPER POWER CORD

Use only the power cord and connector specified for your product, and be sure it is in good condition.

Refer to the *Operating Information* section of this manual for information on power cords and connectors.

USE THE PROPER FUSE

To avoid fire hazard, use only a fuse of the correct type, voltage rating, and current rating as specified in the parts list for this product. Also, ensure that the line selector switch is in the proper position for the power source being used.

DO NOT OPERATE IN EXPLOSIVE ATMOSPHERES

To avoid explosion, do not operate this product in an explosive atmosphere unless it has been specifically certified for such operation.

SERVICE SAFETY SUMMARY

FOR QUALIFIED SERVICE PERSONNEL ONLY
Refer also to the Operator's Safety Summary.

DO NOT SERVICE ALONE

Do not perform internal service or adjustment of this product unless another person capable of rendering first aid and resuscitation is present.

USE CARE WHEN SERVICING WITH POWER ON

Dangerous voltages exist at several points in this product. To avoid personal injury, do not touch exposed connections and components while power is on.

Disconnect power before removing protective panels, soldering, or replacing components.

USE CAUTION WHEN SERVICING THE CRT

The CRT should be serviced only by qualified personnel familiar with CRT servicing procedures and precautions.

CRTs retain hazardous voltages for long periods of time after power-down. Before attempting any work inside the monitor, discharge the CRT by shorting the anode to chassis ground. When discharging the CRT, connect the discharge path to ground and then the anode.

Use extreme caution when handling the CRT. Rough handling may cause it to implode. Do not nick or scratch the glass or subject it to undue pressure during removal or installation. When handling the CRT, wear safety goggles and heavy gloves for protection.

REMOVE THE LOOSE OBJECTS

During disassembly or installation procedures, screws or other small objects may fall to the bottom of the mainframe. To avoid shorting out the power supply, do not power up the instrument until such objects have been removed.

SECTION 1 GENERAL INFORMATION

SECTION 1 GENERAL INFORMATION

GENERAL INFORMATION

INTRODUCTION

The Tektronix 1240 Logic Analyzer is a portable logic analysis instrument useful in the design, manufacture, and service of digital-based products. The 1240 Logic Analyzer has the following features:

- 9-channel (100 MHz) or 18-channel (50 MHz) acquisition cards, or a combination of both (total channel width from 9 to 72 channels using up to four acquisition cards)
- dual, independent timebases that allow correlation of synchronous and asynchronous data
- a nonvolatile memory that retains patterns of instrument setup parameters after power-down
- remote operation with the GPIB or RS232C interface
- self-test diagnostic routines that provide troubleshooting failure information

The 1240 Logic Analyzer displays information on a 7-inch (diagonal) raster-scan CRT. A keyboard consisting of numeric entry keys, menu selection keys, and other controls is located on the front panel of the instrument. Acquisition probe and ROM/RAM pack connections are made on the right side, while connections for external triggers and communication packs are made on the rear panel of the instrument.

1240 INSTRUMENT RECONFIGURATION

If, at any time, the specific application for which your 1240 Logic Analyzer was configured changes, it may be necessary to change the combination of 1240D1 and 1240D2 acquisition cards installed in the instrument. To order additional acquisition cards and probes, contact your local Tektronix representative.

NOTE

If, at any time, you change the 1240 acquisition card configuration, a qualified service technician should check the power supply jumper A07J444 to ensure that the 1240 is configured to supply the correct amount of power to the current number of installed acquisition cards. To determine the need for a power supply jumper change, refer to the Maintenance *section of this manual.*

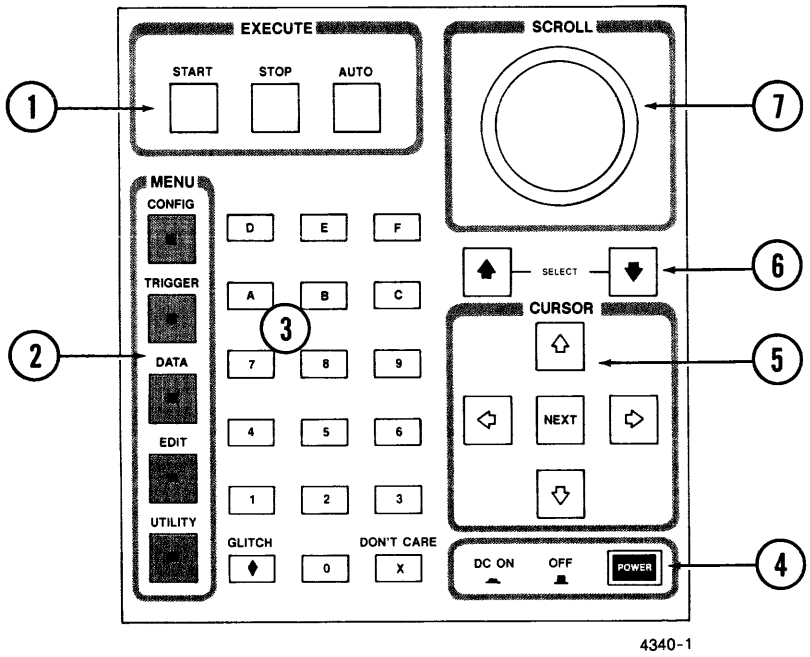


Figure 1-1. 1240 keyboard layout.

KEYBOARD DESCRIPTION

The keyboard is divided into seven functional areas (refer to Figure 1-1). The following paragraphs present general descriptions of these areas and their associated keys. For more information, refer to the *1240 Operator's Manual.*

(1) Execute Keys

START – Starts data acquisition. When the trigger event specified in the Trigger Spec menu is found, the 1240 fills acquisition memory, then automatically stops and displays the acquired data in State Table or Timing Diagram format. While the 1240 is running, it displays information on the status of the trigger search. In diagnostic testing, this key starts the test or tests selected by the soft keys. The 1240 will automatically stop and display the results when the tests are complete, unless looping was selected.

STOP – Stops data acquisition immediately (regardless of the status of the trigger search) and displays acquired data. During diagnostic testing, this key stops the 1240 from looping on a test or group of tests. STOP has no effect if looping is not selected.

AUTO – Starts a sequence of repeated data acquisitions based on the setup in the Trigger Spec and Auto-Run Spec menus. When the trigger event specified in the Trigger Spec menu is found, the conditions set up in Auto-Run Spec determine whether the 1240 stops, displays data, or continues to acquire. In diagnostic testing, this key has no effect except during the manual keyboard test.

(2) Menu Keys

These keys let you access groups of related menus. Each menu key has an LED in the center; the LED is lit when that menu group is in use. In diagnostic testing, none of these keys has any effect except during the manual keyboard test.

CONFIG – Lets you access the Operation Level, Timebase, Memory Config, and Channel Grouping menus. These menus work together to determine how the 1240 acquires and stores data.

TRIGGER – Lets you access the Trigger Spec and Auto-Run Spec menus. These menus define the trigger conditions.

DATA – Lets you access the State Table and Timing Diagram data display formats.

EDIT – Lets you access the Search Pattern Entry and Reference Memory Editor menus. These menus provide tools for manipulating stored data.

UTILITY – Lets you access the Storage Memory Manager menu. If a COMMunication pack is installed, a COMM Port Control menu is also available. Another menu may be available if a ROM pack is installed (though not all ROM packs provide menus).

(3) Data Entry Keys

In diagnostic testing, none of these keys has any effect except during the manual keyboard test.

0-F – Used for numeric data entry. If the field requires a specific radix, some keys may not be legal.

X – Indicates that the value of a channel or character is not considered.

Glitch – Indicates that a glitch, rather than data, is the value to be tested for.

(4) Power Switch

Controls dc power from the power supply. This switch and the MAIN POWER SWITCH on the back panel (refer to Figure 1-2) must both be ON for the 1240 to power up. This switch automatically begins execution of diagnostic testing when turned on. If no failures are detected, the 1240 will go directly into normal operation. Otherwise, the test results will be displayed on the screen.

(5) Cursor Control Keys

CURSOR – These four keys move the blinking field cursor within menu fields and from one menu field to another. The cursor must reside in a field before you can make changes to that field. In diagnostic testing, these keys function exactly as they do during normal operation.

NEXT – Advances the blinking field cursor to the next menu field to the right. If the cursor is positioned on the last field on a line, NEXT moves the cursor to the first field in the next line.

(6) Select Keys

These keys are used in some menu fields to choose from predetermined field values. In diagnostic testing, these keys function exactly as they do during normal operation.

(7) Scroll Knob

The knob's main function is to scroll through acquired data. It also serves as an alternative to the SELECT keys when choosing from predetermined values in certain menu fields. A label describing the current function of the knob is displayed in the upper-right corner of the screen. If the knob cannot be used in a particular situation, no label appears. During diagnostic testing, the scroll knob serves as an alternate to the Select keys.

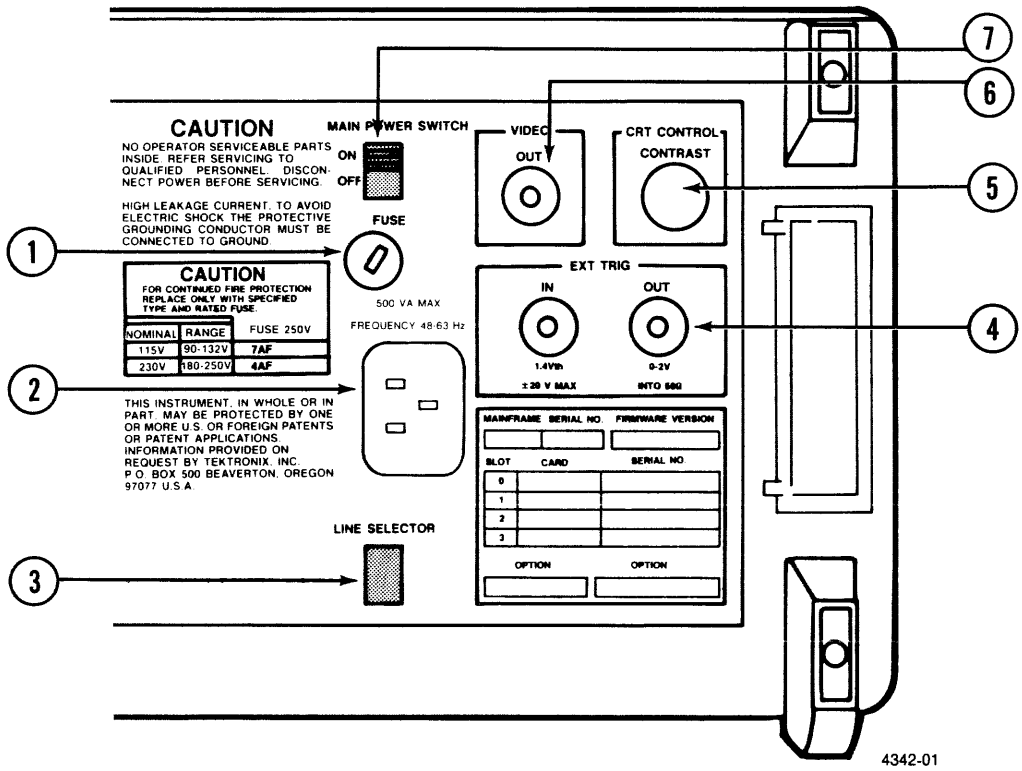


Figure 1-2. 1240 rear panel layout.

REAR PANEL DESCRIPTION

The following is a description of the 1240 rear panel input/output connectors and controls.

(1) Fuse

There are two versions of the 1240 Power Supply Board. Unless the board has been replaced, instruments with serial numbers B079999 and below contain board number 670-7534-05, and instruments with serial numbers B080000 and above contain board number 670-7534-06.

670-7534-06	670-7534-05	APPLICATION
7AF/250 V (3AG)	5AF/250 V (3AG)	115 V line select
4AF/250 V (3AG)	2.5AF/250 V (DIN)	230 V line select

Refer to the Replaceable Electrical Parts section for a list of fuse part numbers. Refer to the Replaceable Mechanical Parts section for a list of the fuse cap part numbers.

(2) AC Power Connector

The ac power connector accepts a detachable line cord. For a list of standard accessory power cords, refer to the *Replaceable Mechanical Parts* section.

NOTE

Before using a 230 V power source, install the correct size fuse and fuse cap.

(3) Line Selector

The LINE SELECTOR allows the choice of operating with either a 115- or 230-volt ac power source.

(4) Ext Trig (In/Out)

The external trigger input allows a separate instrument to start or stop 1240 acquisitions. The output supplies a pulsed or latched high TTL signal indicating a 1240 trigger.

(5) CRT Control (Contrast)

The CONTRAST knob controls the brightness of the CRT display.

(6) Video (Out)

The VIDEO OUT BNC connector supplies a composite video signal corresponding to the present 1240 screen display. The output is RS170-compatible.

(7) Main Power Switch

The rear panel MAIN POWER SWITCH applies or removes ac power from the 1240. The battery-powered nonvolatile memory retains information when the power is removed.

OPERATION MENU OVERVIEW

All 1240 operations are controlled by selections you enter into menus displayed on the screen. There are five groups of related menus; each group is accessed by a MENU key located on the front panel keyboard. Figure 1-3 shows which operation menus are accessed by each MENU key. Detailed descriptions of each menu are provided in the *1240 Operator's Manual*. The default menus are those at the far left of each group in Figure 1-3.

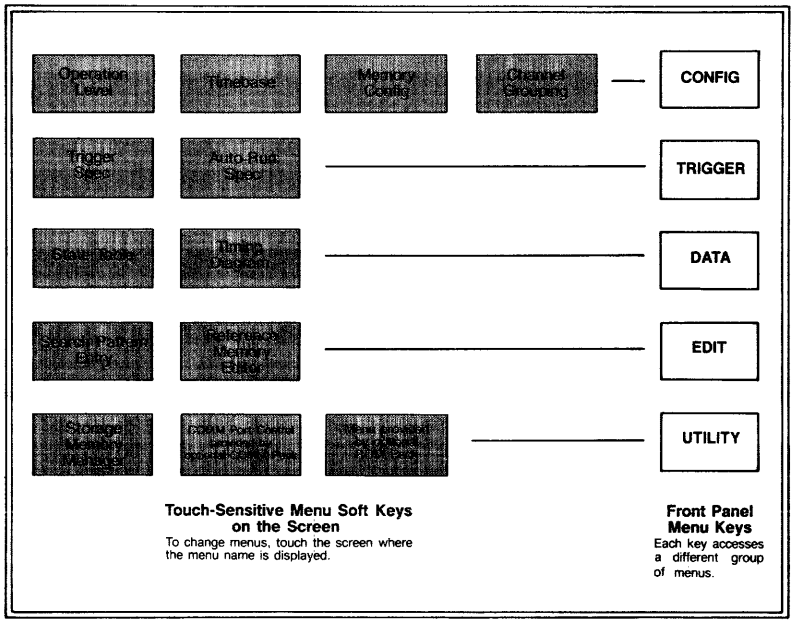


Figure 1-3. Operation Level menu overview showing list of menus accessed by each MENU key.

Along the top and bottom of the screen are touch-sensitive soft keys. The soft key in reverse video corresponds to the menu currently displayed on the screen. Change menus by touching the desired menu's soft key. The 1240 acknowledges the menu change with a short beep, displays the new menu, and changes that menu soft key to reverse video.

Many of the 1240 operation menus are interrelated; a change in one menu may affect selections available in other menus. Tables 8-1 through 8-4 in the *1240 Operator's Manual* list the effects on other menus after changes are made in the Operation Level, Memory Config, Timebase, and Channel Grouping menus. The 1240 changes entries in other menus only when you exit the altered menu. If you make a change, reversing it before you leave that menu, no change is made to other menus.

DIAGNOSTIC MENU OVERVIEW

The Main Diagnostic menu is automatically entered if the 1240 power-up diagnostics detect a failure. The diagnostics report test failure results using three different menu displays (refer to Figure 1-4). The menus, in hierarchical order are: Main Diagnostic, Module Diagnostic, and Area Diagnostic menus. The diagnostic menus display failure information ranging from the most general level (module testing) to the most specific (component group testing) by successively dividing the instrument tests into circuitry groups called modules, areas, and routines. Routines that run within a selected area provide the most specific level of testing information. The routine's test results indicate operational status (if possible) with a PASS, FAIL, or **** message and a corresponding error index number. The **** designation indicates a test not run for either of the following reasons: the test requires too much run time to be a power-up test, or an acquisition probe required for the test was not connected. The error index numbers point to a list of probable causes for failure and repair solutions, located in the *Troubleshooting and Repair* section.

Menu selections are made using soft keys located at the top of the 1240 screen. In addition to the MAIN, MODULE, and AREA DIAGNOSTIC menu soft keys, there is an ENTER NORMAL OPERATION soft key. This soft key allows you to bypass the diagnostics and enter normal operation when FAIL messages occur in areas not critical to the intended use of the 1240 (i.e., if the failure was on an acquisition card not required for the current application). Function selections within a menu are made using the soft keys at the bottom of the 1240 screen.

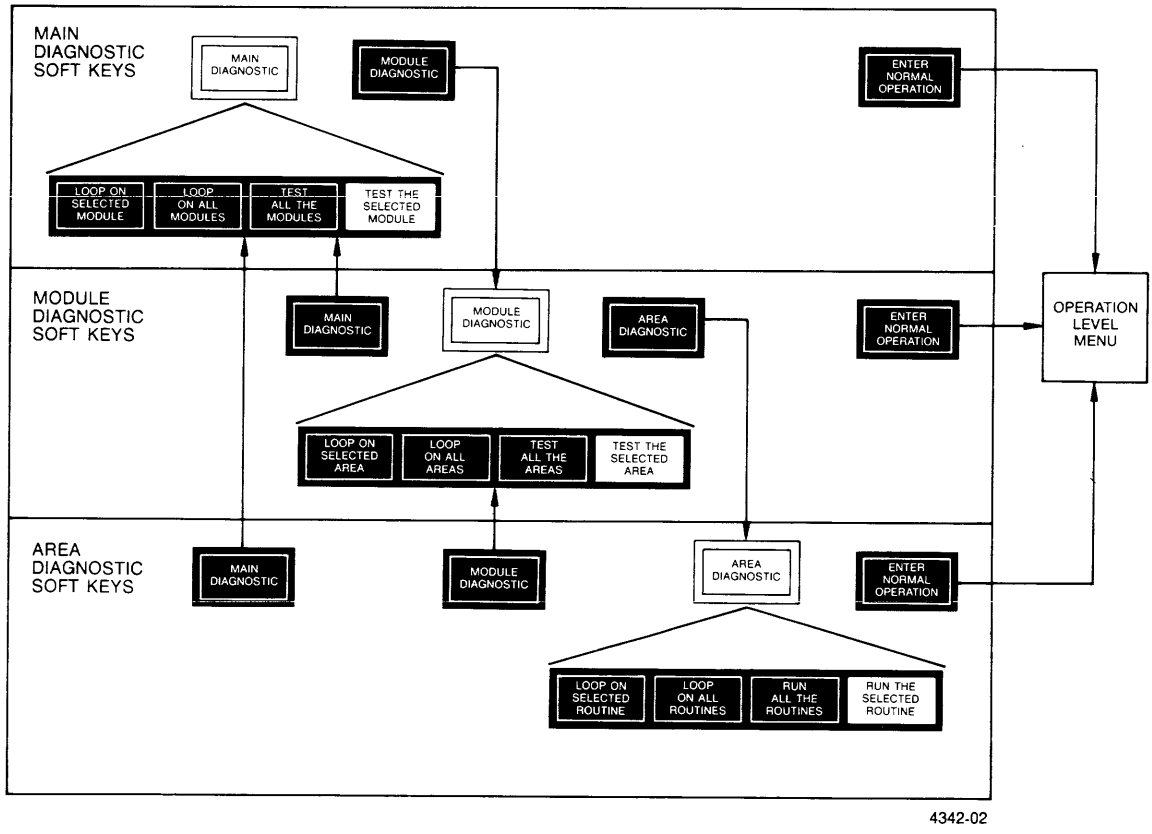


Figure 1-4. Diagnostics menu overview showing the link between diagnostic menus.

MAIN DIAGNOSTIC MENU

The 1240 automatically displays the Main Diagnostic menu (Figure 1-5) if an error occurs during the power-up tests. The Main Diagnostic menu divides the instrument into 11 testable modules. In this menu, the 1240 displays the module names, a PASS/FAIL message, the area name, the routine number, and resulting error index number for any modules that failed.

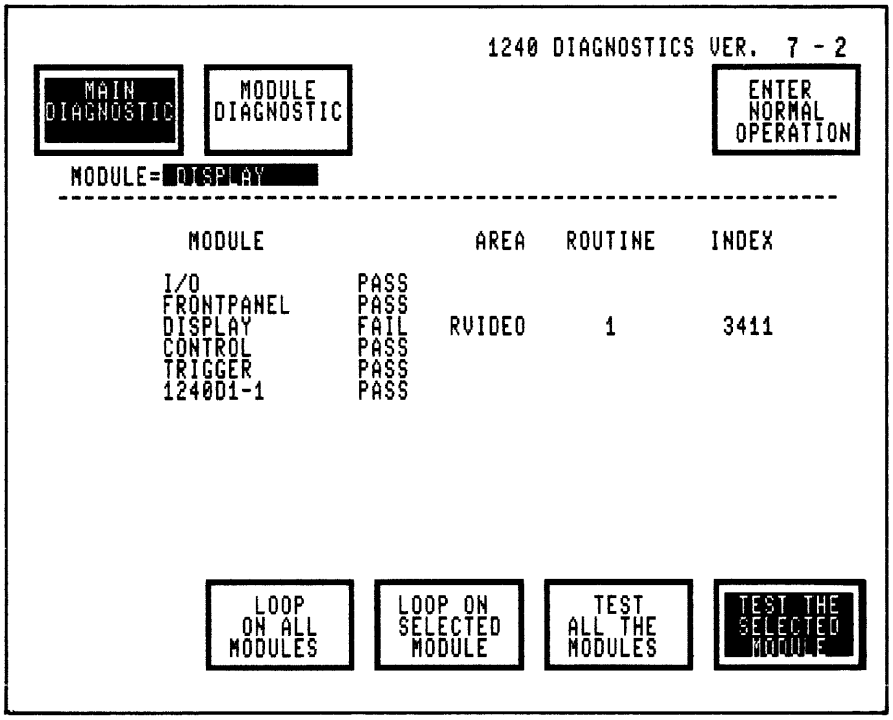


Figure 1-5. Main Diagnostic menu.

A description of the soft keys available in the Main Diagnostic menu follows.

1) TEST THE SELECTED MODULE. Pressing this soft key allows you to test only the module currently displayed in the Module Select field. This selection is the default setting. It is in effect when you enter the Main Diagnostic menu the first time after power-up. To choose the desired module, use the SELECT ↑ and ↓ keys or the knob. The tests begin when you press the START key. Testing ends when all tests for the module are completed or you press the STOP key.

2) TEST ALL THE MODULES. Pressing this soft key allows you to test all of the modules in the instrument. The tests begin when you press the START key. Testing ends when all modules are tested. Selection of the TEST ALL THE MODULES operation causes all the previously recorded failure information to be erased and replaced with the results of the tests currently running.

3) LOOP ON SELECTED MODULE. Pressing this soft key allows you to loop on tests available for the module currently displayed in the Module Select field. To choose the desired module, use the SELECT ↑ and ↓ keys or the knob. The tests begin when you press the START key. To end testing, press the STOP key.

4) LOOP ON ALL MODULES. Pressing this soft key allows you to loop on all tests for all modules. The tests begin when you press the START key. To end testing, press the STOP key. Selection of the LOOP ON ALL MODULES operation causes any previously generated PASS or FAIL message to be updated with the results of the tests currently running.

5) MODULE DIAGNOSTIC. Pressing this soft key places you in the Module Diagnostic menu for the module currently displayed in the Module Select field. To choose the desired module, use the SELECT ↑ and ↓ keys or the knob.

MODULE DIAGNOSTIC MENU

Enter the fault isolation tests by pressing the MODULE DIAGNOSTIC soft key. The Module Diagnostic menu of Figure 1-6 divides a selected module into two or more areas (an exception being RAM pack testing with only one area). Within these areas, numbered routines test a group of specific components. In this menu, the 1240 displays the area names, a PASS, FAIL, or **** message, the routine number, and resulting error index numbers for areas that failed.

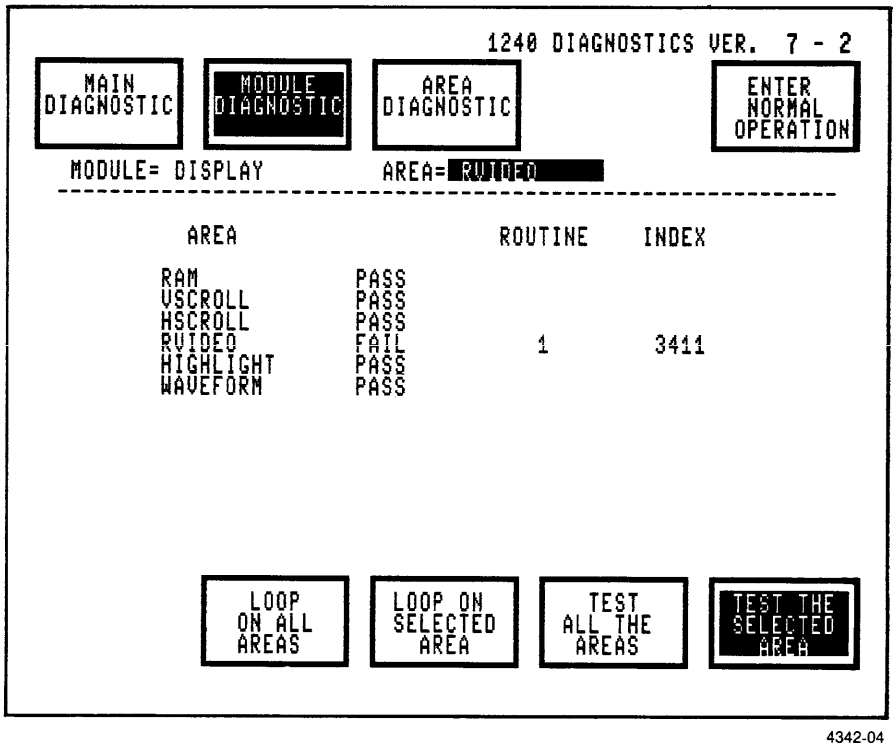


Figure 1-6. Module Diagnostic menu.

A description of the soft keys available in the Module Diagnostic menu follows.

1) TEST THE SELECTED AREA. Pressing this soft key allows you to run routines only on the area currently displayed in the Area Select field. To select the desired area, use the SELECT ↑ and ↓ keys or the knob. The tests begin when you press the START key. Testing ends when all routines for the area are completed or you press the STOP key.

2) TEST ALL THE AREAS. Pressing this soft key allows you to run all the routines in all the areas of this module. The tests begin when you press the START key. Testing ends when all areas are tested or you press the STOP key. Selection of the TEST ALL THE AREAS operation causes failure information to be displayed for any tests performed. A test that failed previously but now passes causes the 1240 display to indicate the previous failure with a highlighted PASS indication.

3) LOOP ON SELECTED AREA. Pressing this soft key allows you to loop on routines for the area currently displayed in the Area Select field. To choose the desired area, use the SELECT ↑ and ↓ keys or the knob. The routines begin when you press the START key. To end testing, press the STOP key.

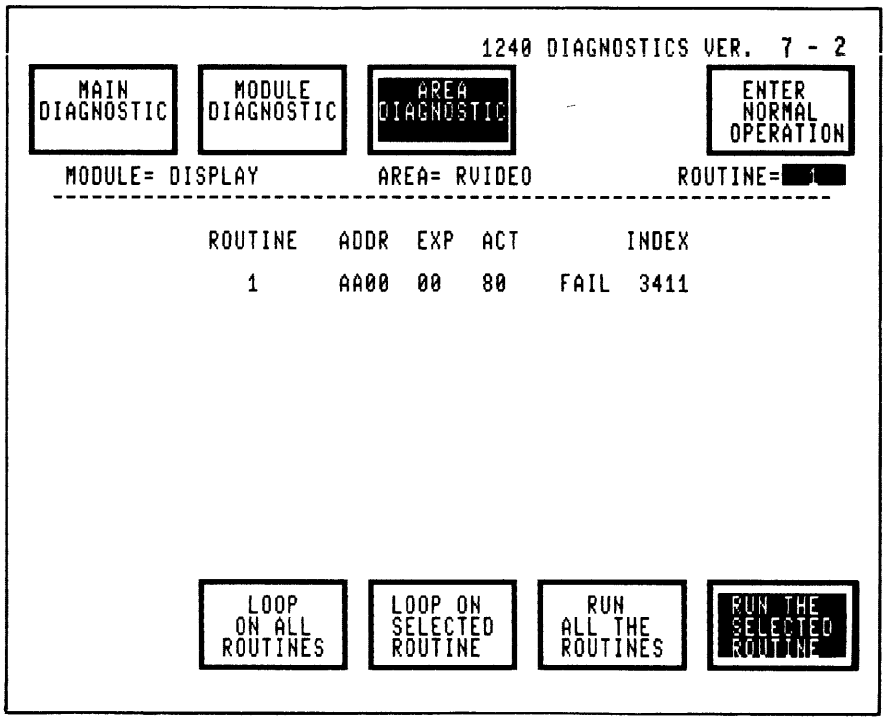
4) LOOP ON ALL AREAS. Pressing this soft key allows you to loop on all routines for all areas in this module. The tests begin when you press the START key. To end testing, press the STOP key. Selection of the LOOP ON ALL AREAS operation causes all previously generated PASS or FAIL messages for these areas to be updated with the results of the test currently running.

5) MAIN DIAGNOSTIC. Pressing this soft key places you in the Main Diagnostic menu.

6) AREA DIAGNOSTIC. Pressing this soft key places you in the Area Diagnostic menu for the area currently displayed in the Area Select field. To choose the desired area, use the SELECT ↑ and ↓ keys or the knob.

AREA DIAGNOSTIC MENU

Enter the most detailed level of fault isolation diagnostics by pressing the AREA DIAGNOSTIC soft key. The Area Diagnostic menu (Figure 1-7) tests a selected area with specific numbered routines. The routines isolate a problem to the fewest number of components possible. In this menu, the 1240 displays the routine number, address information, a PASS, FAIL, or **** message, and the resulting error index number for routines that failed.



4342-05

Figure 1-7. Area Diagnostic menu.

A description of the soft keys available in the Area Diagnostic menu follows.

1) RUN THE SELECTED ROUTINE. Pressing this soft key allows you to run only the routine displayed in the Routine Select field. To choose the desired routine, use the SELECT ↑ and ↓ keys or the knob. The test begins when you press the START key. Testing ends when the selected routine has been run or you press the STOP key.

2) RUN ALL THE ROUTINES. Pressing this soft key allows you to run all the routines in the displayed list. The tests begin when you press the START key. Testing ends when all routines in the list have been run or you press the STOP key. Selection of the RUN ALL THE ROUTINES operation causes all of the previously generated failure information for these routines to be replaced with the results of the tests currently running.

3) LOOP ON SELECTED ROUTINE. Pressing this soft key allows you to loop on the routine currently displayed in the Routine Select field. To choose the desired routine, use the SELECT ↑ and ↓ keys or the knob. The routine tests begin when you press the START key. Each time the 1240 executes a routine test, it updates the result, expected address, and actual address. To end testing, press the STOP key.

4) LOOP ON ALL ROUTINES. Pressing this soft key allows you to loop on all the routines for the specified area. Testing begins with Routine 1 when you press the START key. Selection of the LOOP ON ALL ROUTINES operation causes all previously generated PASS or FAIL messages for these areas to be updated with the results of the test currently running.

5) MAIN DIAGNOSTIC. Pressing this soft key places you in the Main Diagnostic menu.

6) MODULE DIAGNOSTIC. Pressing this soft key places you in the Module Diagnostic menu.

SECTION 2 SPECIFICATIONS

SPECIFICATIONS

INTRODUCTION

In this section of the manual are the following 1240 instrument specifications.

Table	Specification
2-1	1240 Electrical Specifications
2-2	1240D1 Electrical Specifications
2-3	1240D2 Electrical Specifications
2-4	Extender Board Limitations
2-5	1240 Environmental Specifications
2-6	1240 Physical Specifications

Items listed in the Performance Requirements columns are product specifications that can be verified. If verification of the listed electrical characteristics is required for incoming inspection or other purposes, the Verification and Adjustment procedures section lists the necessary steps and test equipment.

Items listed in the Supplemental Information columns are either explanatory notes or performance characteristics for which no limits are specified. They cannot be verified by the Verification and Adjustment procedures listed in this manual.

PERFORMANCE CONDITIONS

The performance characteristics in this section are valid under the following conditions:

1. The 1240 Logic Analyzer must be in an operating environment whose limits are listed in Table 2-5, 1240 Environmental Specifications.
2. The 1240 Logic Analyzer must have been calibrated at an ambient temperature between +20°C and +30°C, after a 30-minute warm-up.
3. All specifications whose measurement involves the use of a Data Acquisition Probe have been based on the P6460 probe. Any applicable conditions, not listed above but unique to a particular characteristic, are expressly stated as part of that characteristic.

Table 2-1
1240 ELECTRICAL SPECIFICATIONS

Characteristic	Performance Requirements	Supplemental Information
SAFETY		
General		Complies with the requirements of UL 1244, IEC 348, and CSA 556B.
CRT		UL, VDE (German X-radiation law), and TEK standard 062-1860-00 (Product Safety Standard for X-Radiation).
GLOBAL EVENT		Event consists of inputs from all groups.
Filter, global event UNCLOCKED		An event is not recognized unless it is accepted by the global filter. These specifications are based on a 1240 equipped with P6460 Data Acquisition Probes.
Separate 1240D1 and 1240D2 events		N is value of FILTER field; selections are 1-16. T is value of ON field (filter timebase); selections are T1 (when T1 active), T2 (when T2 active), and 10NS.
When N = 1: Min. guaranteed event accepted	Timebase period + 6 ns	
When N = 2-16: Max. guaranteed event rejected	(N−1) x T − 8 ns	
Min. guaranteed event accepted	(N x T) + 2 ns	
Mixed 1240D1 and 1240D2 events		
Max. guaranteed event rejected	(N−1) x T − 8 ns	N = 2-16
Min. guaranteed event accepted	(N x T) + 20 ns	N = 1-16
Filter, global event CLOCKED		N is value of FILTER field; selections are 1-16. T is value of ON field (filter timebase) and selection (T1, T2, 10NS) is same as sample clock. Filtered event becomes valid on Nth contiguous valid acquisition event.
Accept 1240D1 and/or 1240D2 clocked events	N x T	Combined 1240D1 and 1240D2 ASYNC acquisition requires additional 2 ns word width.
STORE ON (ON NOT) action	global event clocked:	global event unclocked:
T1 event or T2 event	Store data if event true for 20 ns or more.	Data valid ±12 ns - 20 ns with respect to data clock.
T1 event and T2 event	Store data for a timebase if both events meet indiv. timebase spec. and the other timebase event is valid for 10 ns after the storage clock.	Data valid ±12 ns - 20 ns with respect to data clock.

Table 2-1 (cont.)
1240 ELECTRICAL SPECIFICATIONS

Characteristic	Performance Requirements	Supplemental Information
SEQUENTIAL EVENT		Event may consist only of groups assigned the same timebase.
Filter, accept event	N x T	N is the value of the FILTER field; selections are 1-16. T is the period of the active timebase for that level.
Sequence level execution rate	30 ns	Time after sequential event occurs before next level is allowed.
RESET action	40 ns	
Storage qualification	30 ns	Maximum rate for enable/disable.
TO OCCUR nnnn TIMES	One count per valid event	Iteration counter; count of valid events before sequential event is satisfied. Range is 1 - 9,999 event occurrences.
Delay (nnnn CLOCKS)	1 - 9,999 system clocks	Count of clocks before sequential event is satisfied.
RESET	40 ns	Counter/timer reset takes 100 ns prior to restart.
TRIGGER		Trigger position is within one stored clock of event causing trigger. If reset and trigger occur together, a trigger occurs. When AFTER MEMORY FULL is the trigger position selection, a trigger before memory is full causes a reset. If the counter/timer causes a trigger at the same time that the sequential event causes a reset, the 1240 will trigger and the counter-/timer will be set to 0.
COUNTER/TIMER COUNT mode INCR CNTR	One count per valid event (must satisfy filter)	Range is 1 to 99,999,999,999 events.
TIME mode START TIMER TIME WHILE	Accuracy, start to stop: ± 20 ns	Timer value truncated to 4 digits. Filter clock must equal the sample clock.

Table 2-1 (cont.)
1240 ELECTRICAL SPECIFICATIONS

Characteristic	Performance Requirements	Supplemental Information
T2 DEMUX CONTROL Phase delay between first phase (T2 F) and last phase (T2 L)	10 ns min.	Only first occurrence of next phase is valid. Successive clocks without an intervening alternate phase are ignored.
Phase delay between last phase (T2 L) and first phase (T2 F)	20 ns min.	
ASYNC TIMEBASE		10 ns to 1 s in 1-2-5 increments (0.01% average accuracy).
TWO TIMEBASE CORRELATION Resolution of precedence between timebases	10 ns	The 1240 can resolve the difference between a T1 and a T2 event if they occur 10 ns or more apart. If they occur less than 10 ns from each other, the timebase that was previously indicated as occurring first will now be indicated as occurring last.
EXT TRIG OUT V_{out} high (open) V_{out} high (50 Ω) V_{out} low (either)		50 Ω source Z 3.8 V min. 1.9 V min. 0.6 V max., at 7 mA
Pulse width		70 ns min., 120 ns max.
Delay: probe tip clock to trigger out		65 ns min., 90 ns max.
EXT TRIG IN Input resistance Input capacitance V-input, max. Acceptance window		 1 MΩ ± 1% 37 pF ± 5 pF ± 20 V See Figure 2-1. Window length = 100 ns; window starts 50 ns after clock that causes trigger.
x1 PROBES AND 50 Ω TERMINATED COAX Input threshold Minimum pulse amplitude Minimum pulse width		 1.4 V ± 100 mV 1.8 V high, 1.0 V low 20 ns
x10 PROBES Input threshold Minimum pulse amplitude Minimum pulse width Minimum slew rate		 1.4V ± 500 mV 2.4 V high, 0.6 V low 30 ns 5 V/μs
TIME BETWEEN TRIGGERS FOR LINKED 1240s		Slave trigger located within 60 ns of master trigger.

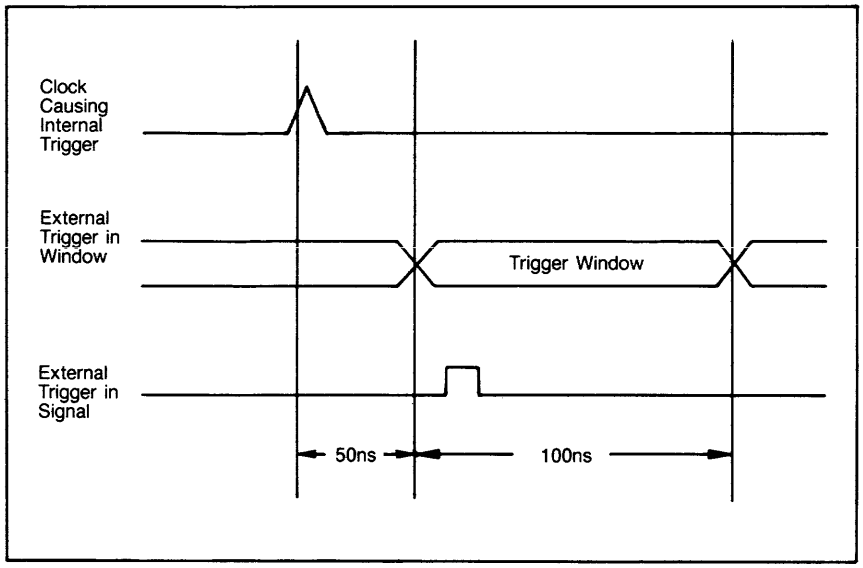


Figure 2-1. External Trigger in acceptance window.

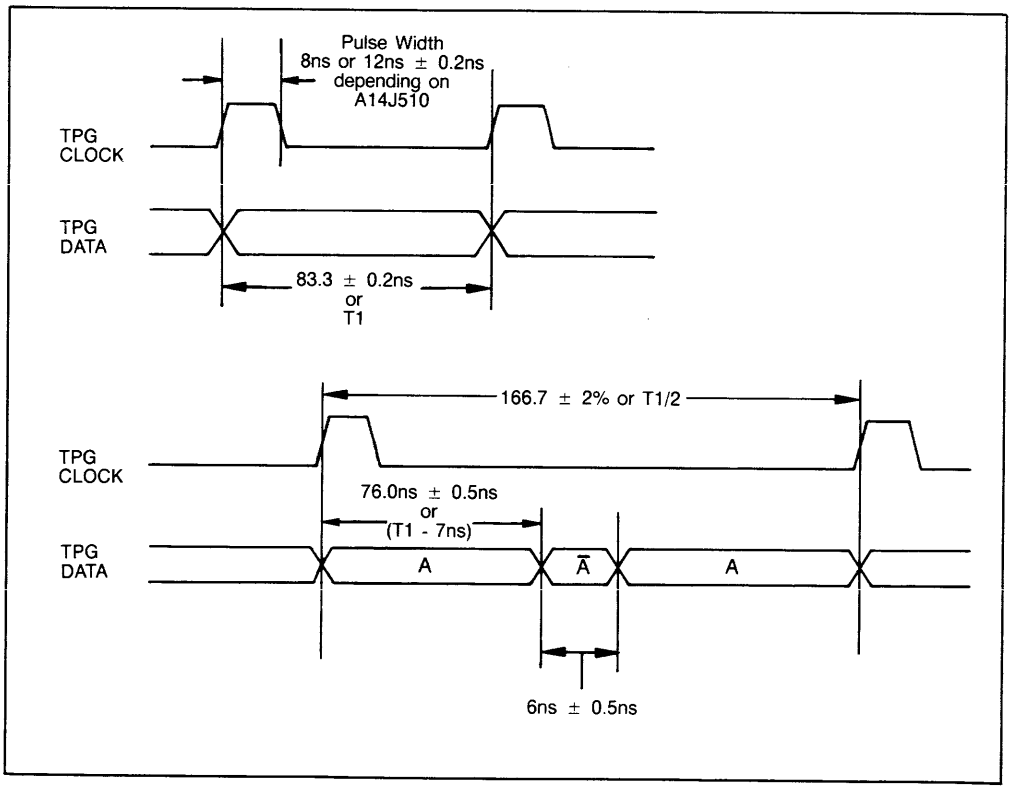


Figure 2-2. TPG clock and data outputs.

Table 2-1 (cont.)
1240 ELECTRICAL SPECIFICATIONS

Characteristic	Performance Requirements	Supplemental Information
DISPLAY (cont.)		
Video out		Conforms to RS170; compatible with standard CRT monitors.
Contrast ratio		Adjustable from 3:1 to 15:1 in a typically illuminated work environment (500 LUX)
FAN CONTROL		
Fan Speed **		With 4 1240D2's installed, fan switches between low and high speeds at approx. 30 deg. C room ambient. More lightly loaded inst. will switch at higher temp.
Low Speed Voltage		9.5 V to 11.5 V
High Speed Voltage		13.0 V to 15.0 V

**** For instruments with serial number B080000 and above.**

Table 2-1 (cont.)
1240 ELECTRICAL SPECIFICATIONS

Characteristic	Performance Requirements	Supplemental Information
TEST PATTERN GENERATOR		See Table 3-4 for patterns (18 bits hex).
Clock period		See Figure 2-2.
mode 0 (no glitches)	83.3 ns ± 2% (12 MHz)	
mode 1 (with glitches)	166.7 ns ± 2% (or 6 MHz)	
mode 2 (no glitches)	T1	Timebase T1 is specified in the Timebase menu. The TPG clock output is only valid when T1 is ≤ 50 MHz.
mode 3 (with glitches)	T1 x 2	
Pulse width	8 or 12 ns ± 0.5 ns	8 or 12 ns depending on strap A14J510 (12 ns - pins 1,2 or 8 ns - pins 2,3)
V_{out}	± 350 mV min. about V th	V th = +5 V (measured) − 1.30 V. Nominal V th = 3.70 V.
Skew, channel - channel		± 1.5 ns
Delay, clock - data	1 ns ± 1.50 ns max.	
Glitch modes (1 or 3)		
Clock period	166.7 ns ± 2% or T x 2	
Glitch width	6.5 ns ± 1.0 ns	See Figure 2-2.
Glitch amplitude	± 300 mV min. about V th	V th = +5 V (measured) − 1.30 V. Nominal V th = 3.70 V.
POWER		
AC power input requirements		
high line		132 V or 250 V
low line		90 V or 180 V
frequency		48 Hz to 440 Hz (single phase)
power		500 VA max., 5 A max.
+12 V supplies *		One supply is for the CRT Drive and COMM Pack port, the other is for the rest of the inst.
regulation	± 5% (11.4 V min., 12.6 V max.)	Measured on the Interface Bd.
ripple	1 V p-p max.	Measured on the Interface Bd.
rated		0 A min., 1 A max. (each)
current limit point		1.0 A min., 2.5 A max.
+13 V supply ** (12.5 V)		This supply was a +12 V supply; it is used by the CRT drive and the COMM Pack port.
regulation	± 3% (12.1 V min., 12.9 V max.)	Measured on the Interface Bd.
ripple	0.5 V p-p max.	Measured on the Interface Bd.
rated		0 A min., 1.5 A max.
current limit point		1.8 A min., 2.5 A max.

*** For instruments with serial number B079999 and below.**
**** For instruments with serial number B080000 and above.**

Table 2-1 (cont.)
1240 ELECTRICAL SPECIFICATIONS

Characteristic	Performance Requirements	Supplemental Information
POWER (cont.)		
+5 V supply		
regulation	± 3% (4.85 V min., 5.15 V max.)	Measured at any point on the Interface Bd. ± 1% measured at the voltage sense point on the Interface Bd.
ripple	100 mV max.	
rated current:		
1 or 2 acquisition cards		Low load setup: 11.6 A min. 29.0 A max.
3 or 4 acquisition cards		High load setup: 30.0 A min. 45.0 A max.
current limit @ 90 V line		Includes +3 V supply current. Measured w/max. specified load on all other supplies, fan running low speed.
1 or 2 acquisition cards		Low load setup: 29 A min. 34 A max.
3 or 4 acquisition cards		High load setup: 46 A min. 52 A max.
over-voltage protection point		6.2 V ± 10%
+ 3 V supply		
regulation	−1.90 to −2.10 V (below +5 V)	Measured at voltage sense point on Interface Bd.
ripple	100 mV max.	Measured on Interface Bd.
rated current		0 A min., 8.0 A max.
current limit point		8.0 A min., 9.0 A max.
−5 V supply		
regulation	± 5% (4.75 V min., 5.25 V max.)	Measured on Interface Bd.
ripple	200 mV max.	Measured on Interface Bd.
rated current		0 A min., 0.8 A max.
current limit point		0.8 A min., 2.2 A max.
−12 V supply		
regulation	± 5% (11.4 V min., 12.6 V max.)	Measured on Interface Bd.
ripple	1 V max.	
rated current		0 A min., 0.28 A max.
current limit point		0.3 A min., 1.0 A max.
DISPLAY		
Power requirements		+12 V DC at 1.0 A
Signal inputs		Video: high = ON Horiz.: Negative at connector Vert.: Positive at connector
Input levels		Standard TTL
Video Response		30 V in 20 ns with < 10% aberration
High voltage	10 ± 0.5 kV	At 40 μA beam current
Scanning Frequency		Horiz.: 15,360 Hz ± 500 Hz Vert.: 60 Hz

Table 2-2
1240D1 ELECTRICAL SPECIFICATIONS

Characteristic	Performance Requirements	Supplemental Information
MEMORY CONFIGURATION		
Width		9 stored data channels; 1 non-stored clock/-qualifier channel
Depth		Glitches On / Glitches Off
no chaining		257 513
2 1240D1s chained		513 1025
3 1240D1s chained		769 1537
4 1240D1s chained		1025 2049
TIMEBASE GENERATION		
Clock input		
pulse width	8 ns min.	Min. time between OR'd clocks is 25 ns.
period	20 ns min.	
amplitude	± 350 mV min. above and below programmed threshold	
Qualifier input		Values based on a 1240D1 with a P6460 acquisition probe.
setup time	11 ns max.	Single selected qualifier driven.
hold time	0 ns max.	
SYNCHRONOUS OPERATION		Uses signals specified by the operator in the Timebase menu. Can be used with all timebases.
Data, all channels		Data word width = 14 ns min. Setup and hold values based on a 1240D1 with a P6460 acquisition probe.
Setup time	7 ns	4 ns setup time for single channel driven.
Hold time	0.5 ns (T1 sourced from same 1240D1 card)	Hold time is 2 ns if data is acquired on one acq. card and the clock source is on the other acq. card.
Amplitude	± 350 mV min. above and below programmed threshold	
SYNC events		
global event for all channels		At max. SYNC rate, any input event meeting setup and hold times and minimum word width.
sequential event for all channels		At max. SYNC rate, recognize any input event meeting setup and hold times and minimum word width. Up to 14 different events, one per sequence level.
ASYNCHRONOUS OPERATION		
Data min. word width guaranteed to be sampled	Timebase period + 6 ns	Timebase period selectable from 10 ns to 1 s in 1-2-5 increments.
		Timebase period + 8ns with 1240D2
		N samples of word requires (N×T) + 6ns min. word width (or N×T + 8ns with 1240D2).

Table 2-2 (cont.)
1240D1 ELECTRICAL SPECIFICATIONS

Characteristic	Performance Requirements	Supplemental Information
Glitch capture		
glitch width		6 ns at threshold (single channel) at max. glitch/data transition rate of 30 ns. A glitch may be detected as both glitch and data if the transition occurs within 2 ns of the sample clock.
glitch amplitude	± 350 mV above and below programmed threshold	
ASYNC events		
Global event for all channels, min. data word width guaranteed to be sampled:		
clocked (1,0,X,)	Timebase period + 6 ns	Timebase period + 8 ns with 1240D2
unclocked (1,0,X)	16 ns min.	Minimum width of valid event when global filter = 1 at 10NS and no 1240D2 channels specified.
Sequential event (1,0,X)	Timebase + 6 ns	Up to 14 different events, one per sequence level. Timebase period + 8ns with 1240D2 For both global and sequential events, N samples of word requires (N×T) + 6ns min. word width (or N×T + 8ns with 1240D2).
PROBE THRESHOLD		
Threshold range		Selectable from +6.35 to −6.35 V in 50 mV increments; also includes preset values for TTL (+1.4 V), TPG (+3.70 V), −ECL (−1.30 V).
Threshold accuracy with probe	± 0.5% ± 65 mV	
Threshold accuracy on card only		±.25% of TH÷4 ±8mV (measured at probe connector, with offset sense connected to GND sense and 10.5K (0.1%) between J620-16 and -13)

Table 2-3
1240D2 ELECTRICAL SPECIFICATIONS

Characteristic	Performance Requirements	Supplemental Information
MEMORY CONFIGURATION		
Width		18 stored data channels; 2 non-stored clock/qualifier channels
Depth		
no chaining		513
2 1240D2s chained		1025
3 1240D2s chained		1537
4 1240D2s chained		2049
TIMEBASE GENERATION		
Clock input		
pulse width	8 ns min.	
period	20 ns min.	Min. time between OR'd clocks is 25 ns.
amplitude	± 350 mV min. above and below programmed threshold	
Qualifier input		Values based on 1240D2 with P6460 acquisition probes.
setup time	11 ns max.	Single selected qualifier driven.
hold time	0 ns max.	
SYNCHRONOUS OPERATION		Uses signals specified by the operator in the Timebase menu. Can be used with all timebases.
Data, all channels		Setup and hold values based on 1240D2 with P6460 acquisition probes.
Setup time	12 ns	
Hold time	0 ns	
Amplitude	± 350 mV min., above and below programmed threshold	
SYNC events		
global event for all channels		At max. SYNC rate, any input event meeting setup and hold times.
sequential event for all channels		At max. SYNC rate, recognize any input event meeting setup and hold times. Up to 14 different events, one per sequence level.
ASYNCHRONOUS OPERATION		
Data min. word width guaranteed to be sampled	Timebase period + 6 ns	Timebase period selectable from 20 ns to 1 s in 1-2-5 increments. Timebase period + 8ns with 1240D1 N samples of word requires (N×T) + 6ns min. word width (or N×T + 8ns with 1240D1).

Table 2-3 (cont.)
1240D2 ELECTRICAL SPECIFICATIONS

Characteristic	Performance Requirements	Supplemental Information
ASYNC events Global event for all channels		
clocked (1,0,X)	Timebase period + 6 ns	Data stored may be different than that recognized by event recognizer. Timebase period + 8ns with 1240D1
unclocked (1,0,X)	16 ns min.	Minimum width of valid event when global filter = 1 at 10NS and no 1240D1 channels specified.
Sequential event (1,0,X)	Timebase period+ 6 ns	Up to 14 different events, one per sequence level. Timebase period + 8ns with 1240D1
PROBE THRESHOLD Threshold range		Selectable from +6.35 to −6.35 V in 50 mV increments; also includes preset values for TTL (+1.4 V), TPG (+3.70 V), −ECL (−1.30 V).
Threshold accuracy with probe	± 0.5% ± 65 mV	
Threshold accuracy on card only		±.25% of TH÷4 ±8mV (measured at probe connector, with offset sense connected to GND sense and 10.5K (0.1%) between threshold sense and threshold out.)

Table 2-4
EXTENDER LIMITATIONS*

Characteristic	Description
1240D1 OR 1240D2 ON EXTENDER	
Sequence Level Execution Rate	Changes from 30 ns to 35 ns
Maximum Clock Rate	1240D1, GLITCHES OFF: 20 ns 1240D1, GLITCHES ON: 22 ns
Data Hold Time	Increases vary with configuration. Maximum increases are: 1240D1 data hold time increases from 2 ns to 4 ns. 1240D2 data hold time increases from 0 ns to 2 ns.
Qualifier Setup/Hold Times	Increases vary with configuration. Maximum increases are: Qualifier setup time increases from 11 ns to 15 ns. Qualifier hold time increases from 0 ns to 2 ns.
Two-Timebase Resolution	Increases from 10 ns to 12 ns
T2 DEMUX Control	Extender adds 5 ns to both minimum delays between phases. T2F-T2L phase delay increases from 10 ns to 15 ns. T2L-T2F phase delay increases from 20 ns to 25 ns.
Triggering	Global and sequential trigger are guaranteed only if the clock source and event recognizer source are both from the extended board or both from non-extended boards. Two-timebase sequential triggering is not guaranteed for timebases that are asychronous to each other.
DISPLAY BOARD ON EXTENDER	
Counter/Timer	Counter/timer output is delayed. Position of counter/timer trigger is within one stored clock of event causing trigger.
TRIGGER BOARD ON EXTENDER	
Sequence Level Execution Rate	Changes from 30 ns to 35 ns
Maximum Clock Rate	1240D1, GLITCHES OFF: 20 ns 1240D1, GLITCHES ON: 22 ns
T2 DEMUX Control	Extender adds 5 ns to both minimum delays between phases. T2F-T2L phase delay increases from 10 ns to 15 ns. T2L-T2F phase delay increases from 20 ns to 25 ns.
Triggering	Two-timebase sequential triggering is not guaranteed for timebases that are asychronous to each other.

* Refer to the *Extender Board Instructions* for more information.

Table 2-5
1240 ENVIRONMENTAL SPECIFICATIONS

Characteristic	Description
TEMPERATURE	
Maximum operating	+55°C
Minimum operating	−10°C
Non-operating	−62°C to +85°C
TPG calibrated operating	20°C to 30°C
HUMIDITY	95% to 97% relative humidity (Five 24 hr. cycles at 30°C to 60°C, instrument must reside in ≤ 70% relative humidity for two hours before and during operation)
ALTITUDE	
Operating	4.5 km (15,000 ft.)
Non-operating	15 km (50,000 ft.)
VIBRATION, operating	
Displacement	0.025 inch (0.64 mm)
Frequency range	10 to 55 Hz
SHOCK	30 Gs, halfsine, 11 ms duration, 18 shocks total, 3 on each face
ELECTROMAGNETIC INTERFERENCE	Meets FCC part 15, sub-part J, class A, without probes. Meets VDE 0871, class B, without probes.

Table 2-6
1240 PHYSICAL SPECIFICATIONS

Characteristic	Description
WEIGHT	12.0 kg (26.5 lbs.)
OVERALL DIMENSIONS	See also Figure 2-3.
Height (handle folded back)	19.7 cm (7.8 inches)
Width (including handle)	36.8 cm (14.5 inches)
Length (including protective front cover)	49.8 cm (19.6 inches)
Length (handle extended)	57.6 cm (22.7 inches)

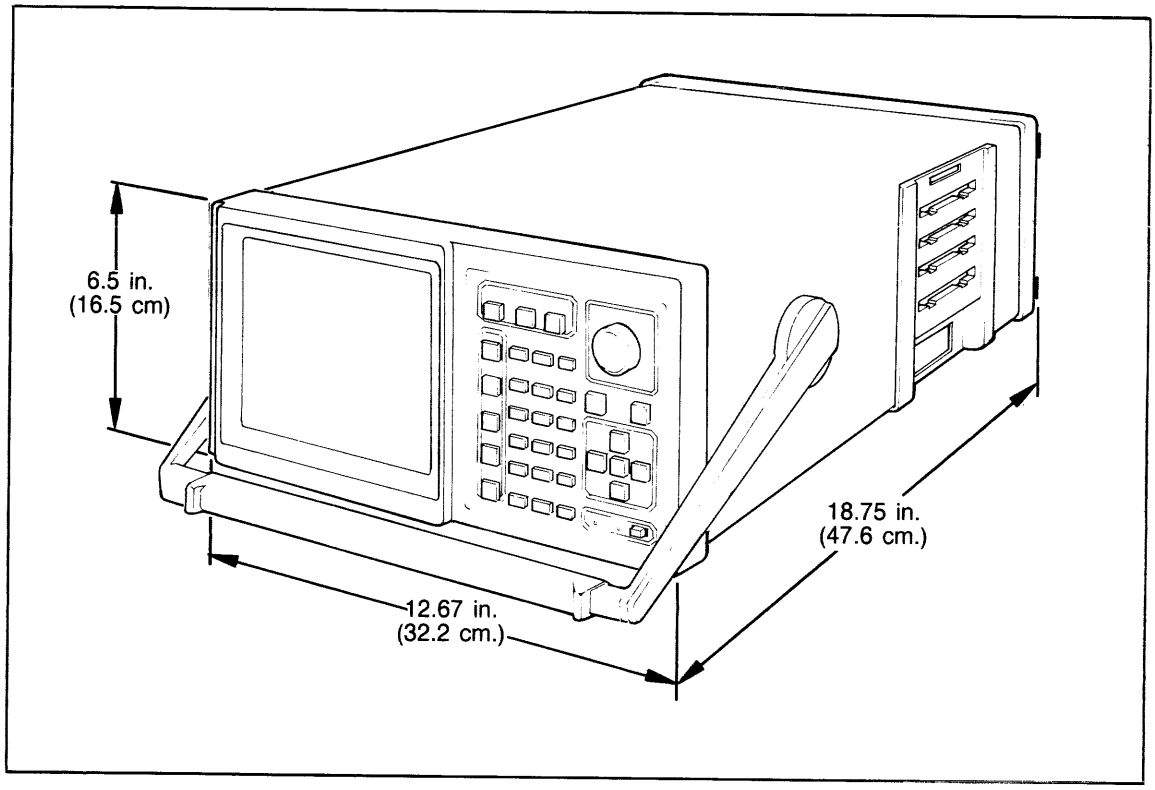


Figure 2-3. 1240 dimensions.

SECTION 3 OPERATING INFORMATION

SECTION 3 OPERATING INFORMATION

OPERATING INFORMATION

POWER REQUIREMENTS

The 1240 Logic Analyzer operates from a nominal 115 or 230 V, 48 to 63 Hz, single-phase power source. Before connecting the mainframe to a power source, verify that the LINE SELECTOR on the mainframe's rear panel shows the correct nominal voltage for the power source being used. Figure 3-1 shows the location of the LINE SELECTOR.

If the selector shows the wrong voltage for the power source being used, push the LINE SELECTOR switch to the appropriate position. Also, change the line voltage fuse located in the holder labeled FUSE, positioned above the LINE SELECTOR (refer to Figure 3-1). To access the fuse, twist the spring-loaded fuse holder counterclockwise. A label listing the fuse requirements is located beside the LINE SELECTOR. Refer to the *Replaceable Electrical Parts* section for a list of fuse part numbers.

CAUTION

Before applying power to the mainframe, verify that the LINE SELECTOR, the line voltage fuse, and the power cord are compatible with the power source being used.

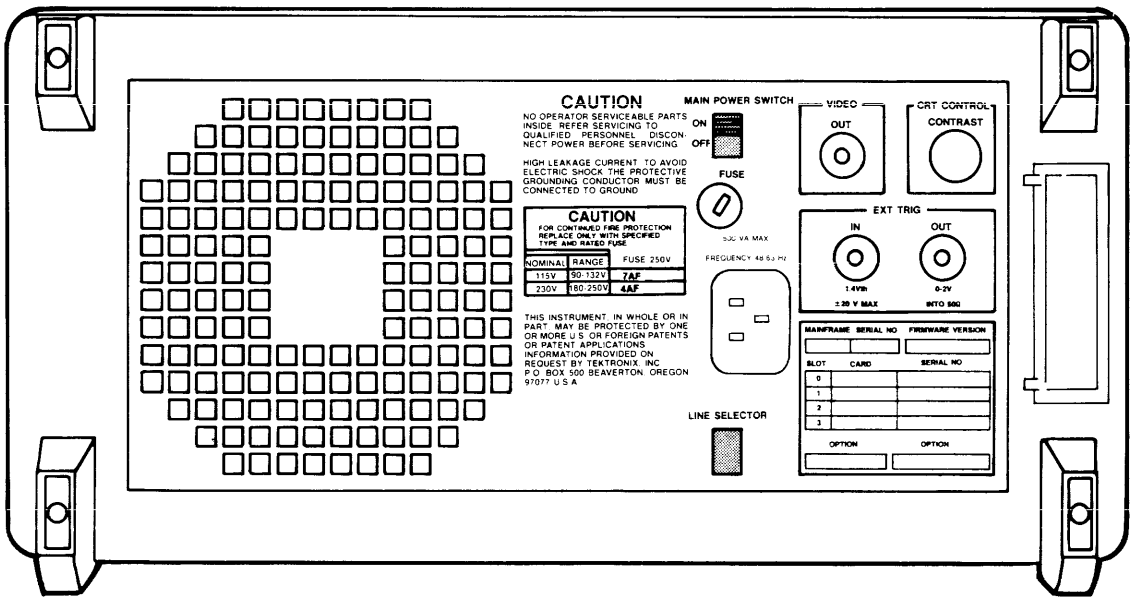


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Figure 3-1. 1240 rear panel.

POWER CORDS

The 1240 uses a three-wire power cord with a three-contact plug for connection to the power source and to protective ground. The plug protective-ground contact connects to the accessible metal parts of the instrument through the power cord protective-grounding conductor. For protection against electrical shock, insert this plug into a power source socket that has a securely grounded protective-ground contact.

WARNING

Hazardous voltages may be present on the exposed metal surfaces of the mainframe if the power source socket's protective ground connection is not securely grounded.

The 1240 is shipped with a 120 V power cord unless ordered differently. The power cords available for the 1240 are shown in Figure 3-2. For information regarding these power cords, refer to the *Replaceable Mechanical Parts* section, or contact your Tektronix representative, or the nearest Field Office.

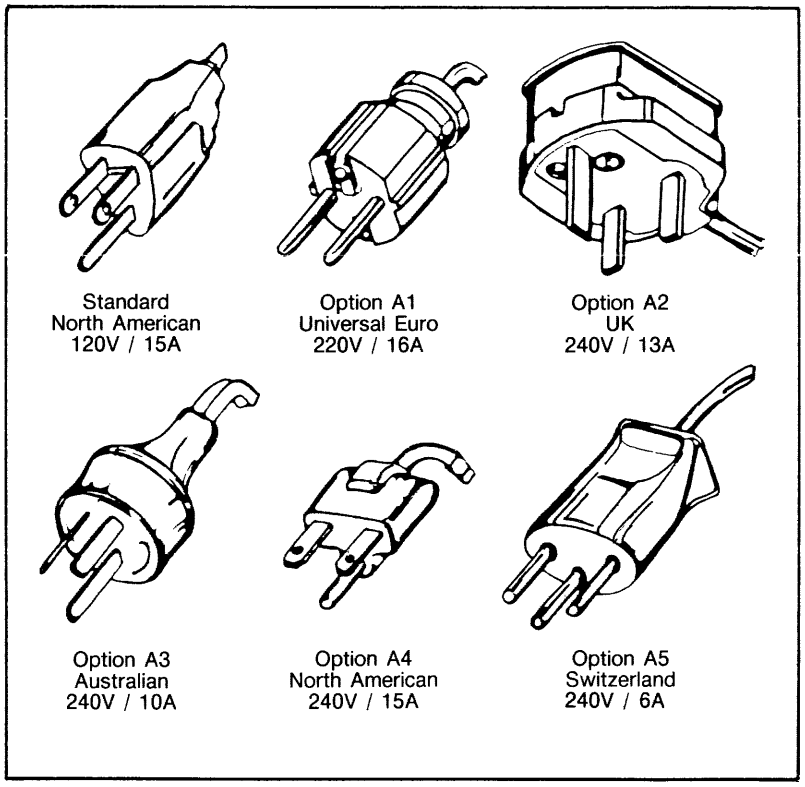

Figure 3-2. Optional 1240 power cords.

FUSES

There are two versions of the 1240 Power Supply Board. Unless the board has been replaced, instruments with serial numbers B079999 and below contain board number 670-7534-05, and instruments with serial numbers B080000 and above contain board number 670-7534-06.

670-7534-06	670-7534-05	APPLICATION
7AF/250 V (3AG)	5AF/250 V (3AG)	115 V line select
4AF/250 V (3AG)	2.5AF/250 V (DIN)	230 V line select

Refer to the Replaceable Electrical Parts section for a list of fuse part numbers. Refer to the Replaceable Mechanical Parts section for a list of the fuse cap part numbers.

1240 POWER SWITCHES

The 1240 has two power switches available: the front-panel POWER DC ON/OFF switch (refer to Figure 1-1), and the rear-panel MAIN POWER SWITCH (refer to Figure 3-1). The front-panel power switch controls dc power from the power supply circuitry. This switch is normally used by the operator for powering the instrument ON and OFF. The rear-panel MAIN POWER SWITCH controls the incoming ac line voltage to the 1240 power supply. This switch is normally used by the service technician for removing the line voltage to the instrument before servicing. The nonvolatile memory is not affected by either of these switches; it has a separate battery power source on the Control Processor Board.

It is possible to power ON the 1240 using either power switch, providing that the other switch is in the ON position.

CAUTION

To prolong the life of the 1240 Power Supply components, it is recommended that the following guidelines be observed:

- *If possible, power the 1240 ON and OFF using the front-panel DC ON/OFF POWER switch.*
- *If it is necessary to power up the instrument using the rear-panel MAIN POWER SWITCH, do so only if the instrument has been powered down for several minutes. This allows the internal power supply circuitry to handle current surges.*

POWER-UP DIAGNOSTICS

To power up the 1240, set the rear-panel MAIN POWER SWITCH to ON, then push the front-panel dc power switch.

The 1240 has internal diagnostic tests that run automatically at power-up. These tests check out major mainframe components and operating firmware. When power-up diagnostics are successfully completed, most processor and display functions, along with some acquisition and trigger functions, are verified.

If all tests pass, the Operation Level menu (Config menu group) is automatically displayed. If diagnostics fail, the Main Diagnostic menu is automatically displayed. The menu lists the functional modules tested and a corresponding PASS/FAIL message for each module (FAIL message shown in highlighted video).

Some error conditions only inhibit a portion of the 1240 functions. Table 3-1 lists and describes the possible power-up error conditions.

Table 3-1
POWER-UP ERROR CONDITIONS

Error Conditions	Definition
Display is blank or full raster.	A failure occurred on either the Display Board or the CRT Driver Board. No operation is possible. Refer the 1240 to qualified service personnel.
Display is filled with random characters or zeros.	A failure occurred on either the I/O Processor or the Display Board. No operation is possible. Refer the 1240 to qualified service personnel.
DIAGNOSTICS FAILURE IOP RAM XXXX XXXX	One of the I/O processor RAMs failed. No operation is possible. Refer the 1240 to qualified service personnel.
DIAGNOSTICS FAILURE IOP ROM n XXXX XXXX	A failure occurred in I/O processor diagnostic ROM n. Limited operation may be possible.
IMPROPER ACQUISITION CARD SEQUENCE: RE-READ INSTALLATION INSTRUCTIONS OR CALL YOUR TEKTRONIX SERVICE REP.	Any 9-channel cards must be installed in lower-numbered slots than 18-channel cards. There can be no empty slots between cards. Refer to the *Disassembly and Installation* section for acquisition card installation instructions.
INTER-PROCESSOR COMMUNICATION FAILURE	The control and I/O processors are unable to communicate. No operation is possible. Refer the 1240 to qualified service personnel.
CONTROL PROCESSOR RAM FAILURE XXXX XX XX	A failure occurred in one of the control processor RAMs. No operation is possible. Refer the 1240 to qualified service personnel.
CONTROL PROCESSOR ROM FAILURE XXXX XXXX	A failure occurred in one of the control processor ROMs. No operation is possible. Refer the 1240 to qualified service personnel.
I/O FAIL	A failure occurred in the specified area of the I/O processor. Limited operation may be possible.
FRONTPANEL FAIL	A failure occurred in the specified area of the front panel. Limited operation may be possible.
DISPLAY FAIL	A failure occurred in the specified area of the display. Limited operation may be possible.
COMMPACK FAIL	The specified area of the COMM pack failed. The pack will not operate properly, but the rest of the 1240 is not affected. Power down and remove the pack.

Table 3-1 (cont.)
POWER-UP ERROR CONDITIONS

Error Conditions	Definition
COMMPACK ROM FAILURE XXXX XXXX	The specified area of the COMM pack failed. The pack will not operate properly, but the rest of the 1240 is not affected. Power down and remove the pack.
CONTROL FAIL	A failure occurred in the specified area of the control processor. Limited operation may be possible.
TRIGGER FAIL	A failure occurred in the specified area of the Trigger Board. Limited operation may be possible.
9 CH ACQn FAIL	A failure occurred in the specified area of the 9-channel card in acquisition card position n. This card will not operate properly, and may affect other cards if it is left in the system. Refer the 1240 to qualified service personnel for card removal.
18 CH ACQn FAIL	A failure occurred in the specified area of the 18-channel card in acquisition card position n. This card will not operate properly, and may affect other cards if it is left in the system. Refer the 1240 to qualified service personnel for card removal.
RAMPACK FAIL	This message can be displayed for two reasons: 1. A failure occurred in the specified area of the pack. 2. The pack is not initialized. First, try to initialize the pack: touch the ENTER NORMAL OPERATION soft key, then press the UTILITY key on the front panel. In the Storage Memory Manager menu, touch the LOAD NEW PACK soft key; this key runs pack initialization routines. Next, turn the 1240 off, then on again. If the error message persists, the pack has failed; it will not operate properly, but the rest of the 1240 is not affected. Power down and remove the pack.
ROMPACK FAIL	A failure occurred in the specified area of the ROM pack. The pack will not operate properly, but the rest of the 1240 is not affected. Power down and remove the pack.
ROMPACK ROM FAILURE XXXX XXXX	A failure occurred in the specified area of the ROM pack. The pack will not operate properly, but the rest of the 1240 is not affected. Power down and remove the pack.

ACQUISITION BOARDS

The 1240 has available two types of acquisition cards: the 1240D1 9-channel and the 1240D2 18-channel acquisition cards. The 1240 can accomodate up to four acquisition cards in the slots numbered 0 to 3. The card installed in slot 0 is visible through the top opening; the card in slot 3 is visible through the bottom opening (see Figure 3-3).

The specific application of the 1240 defines the configuration with the most useful combination of these boards. The choice of board type affects the number of input channels, speed limitations, and memory depth for data acquisitions. The two types of acquisition boards are summarized in Table 3-2.

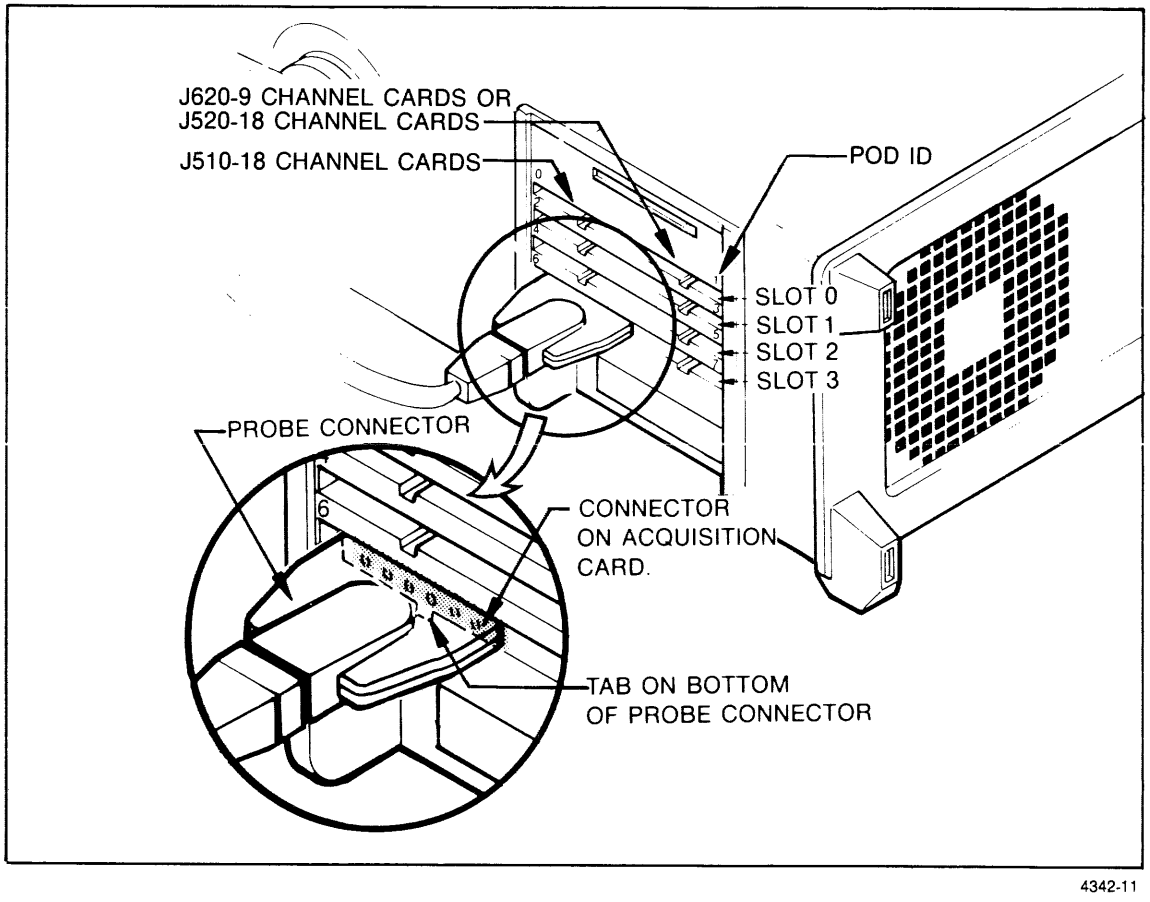

Figure 3-3. 1240 right side panel showing acquisition probe connection.

Table 3-2
ACQUISITION BOARD FEATURES

Feature	1240D1	1240D2
Channels per Card	9	18
Glitch Detection & Storage	5 ns min.	None
Asynchronous Acquisition Rate	10 ns	20 ns
Synchronous Acquisition Rate	20 ns	20 ns
Glitch Data Acquisition Rate	20 ns	n/a
Clock Qualification	Yes	Yes
Data Qualification	Yes	Yes
Memory Depth	513	513
Memory Depth w/ Glitch Storage	257	n/a
Sync & Async Correlation	Yes	Yes
Global & Sequential Word Recognition	Yes	Yes
Demultiplexing	Yes	Yes

ACQUISITION PROBES

Each 9-channel acquisition card uses one P6460 Data Acquisition Probe (refer to Figure 3-4); 18-channel cards use two P6460s. Each probe (or pod) has nine data lines (numbered 0-8) and one clock/qualifier (C/Q) line.

CONNECTION

The probes connect to acquisition cards or the Test Pattern Generator (TPG) through openings on the right side panel of the instrument (refer to Figure 3-3). A guide on the probe ensures that it cannot be connected incorrectly.

POD ID

Pod ID numbers are assigned to probes according to the slot position of the card they are attached to. When you install a probe, you can see the ID number molded into the plastic near the side opening where probes connect (refer Figure 3-3). A pod ID button is located on the back edge of each probe (refer to Figure 3-4). Press this button to get a screen readout of the probe's pod ID.

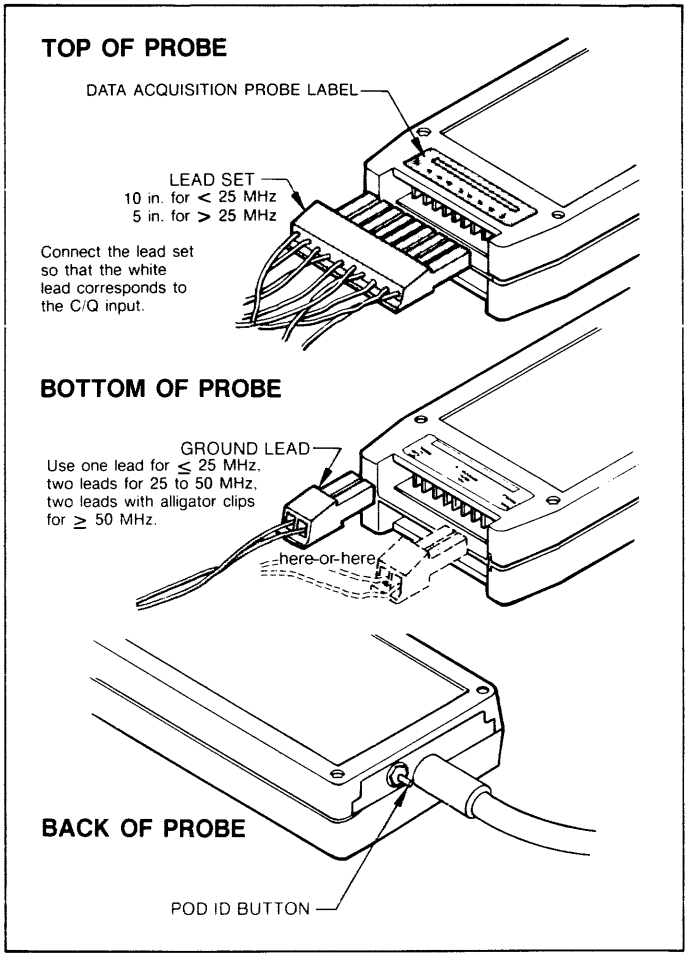

Figure 3-4. P6460 Data Acquisition Probe.

⚠ LEAD SET

A 10-inch lead set is supplied with each probe (refer to Figure 3-4). This lead set can be used to clock frequencies up to 25 MHz. Above 25 MHz, one of the optional five-inch lead sets may be required to meet all specifications. Refer to the documentation accompanying the P6460 for the part numbers of these lead sets.

Two ground leads are also provided with each probe. Below 25 MHz, only one ground lead is required with the 10-inch lead set. Between 25 MHz and 50 MHz, both ground leads should be used. In environments with unusual amounts of electrical noise, it may be nesessary to use both ground clips and/or a five-inch lead set.

A ten-inch lead set and one ground lead are supplied with each P6462 Data Acquisition Probe. For clock frequencies up to 25 MHz, use the ten-inch lead set. For clock frequencies over 25 MHz, use the five-inch lead set.

Figure 3-4 shows how to install lead sets and ground leads.

ROM, RAM, AND COMM PACKS

OVERVIEW

ROM, RAM, and COMM packs are available as optional accessories for the 1240. The ROM packs have many uses:

- information storage in blank ROM packs
- VLSI support (Tektronix generated)
- microprocessor disassembly (Tektronix generated)
- enhanced feature set (e.g., Tektronix-generated Performance ROM)

The nonvolatile RAM packs allow storage, retrieval, and deletion of instrument setups and memories. The COMM packs allow the 1240 to interface with either GPIB- or RS232C-based instruments or controllers. For more information regarding pack interfaces, refer to the documentation accompanying each specific pack.

PACK INSTALLATION

ROM and RAM packs are installed in the door-covered slot directly beneath the probe connections on the right side panel (refer to Figure 3-5). One ROM or RAM pack may be installed at any given time without powering down the 1240, providing the pack initialization procedures have been completed. (For more information, refer to *ROM/RAM Pack Initialization*). Slide either pack (label side up) past the hinged door and push it firmly into the connector. Two guides on the top cover of the pack ensure that the pack is installed correctly and that only 1240-compatible packs are used.

CAUTION

Static discharge can damage the semiconductor devices in a ROM or RAM pack. Discharge static from a pack before installing it by momentarily laying the pack (label side up) on top of the 1240.

When operating the 1240 in temperatures between -15° C and 0° C (5° F and 32° F), ensure that the instrument has been powered-up for at least 10 minutes before installing a ROM or RAM pack. This allows the 1240 interface circuitry to begin operating properly before attempting communication with the pack.

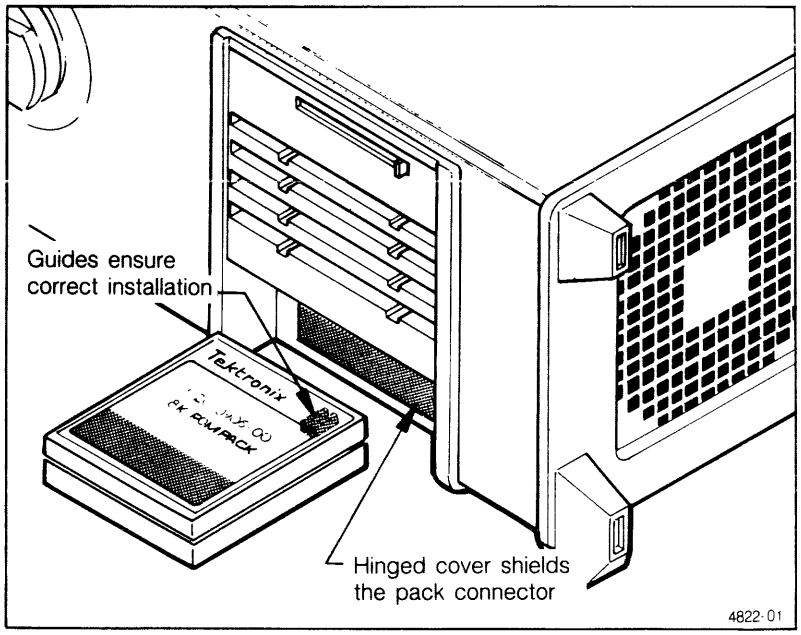

Figure 3-5. ROM or RAM pack door location.

COMM packs are installed in the back panel (refer to Figure 3-6). The 1240 must be powered down before a COMM pack is installed. To install a COMM pack, slide the pack past the hinged door with the pack's label toward the outside edge of the 1240. The 1240's pack connector is located about four inches past the hinged door. Remove a COMM pack from the 1240 by pulling on the pack handle. This handle anchors the pack to the 1240 once the pack is installed. To anchor the pack, snap the bow handle over the two small retaining spurs to the left of the slot.

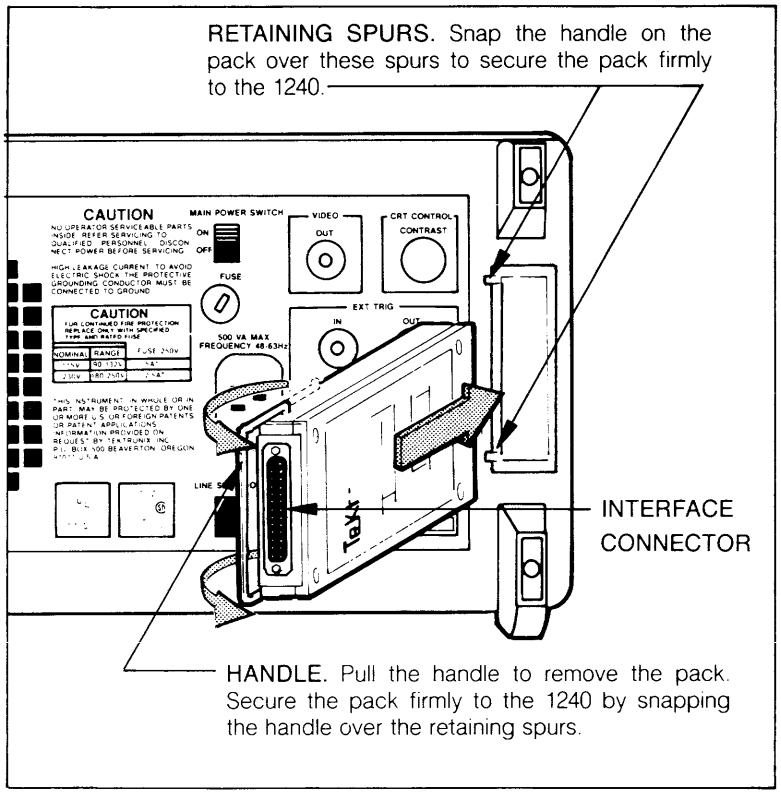

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Figure 3-6. COMM pack door location.

ROM/RAM PACK INITIALIZATION

In order to properly initialize the 1240 for ROM pack use, it is necessary to power-up the 1240 before installing a ROM pack. Once the 1240 is powered on, display the Storage Memory Manager menu (Utility menu group). Proceed by plugging in the desired ROM (or RAM) pack. Immediately after installing or removing a ROM or RAM pack, touch the LOAD NEW PACK soft key. An error message indicating that an unknown pack has been installed will appear at the top of the display screen. Press the X key on the front panel. This runs the pack initialization routines and ensures that the 1240 uses the pack properly. Thereafter, ROM and RAM packs may be exchanged without powering down the 1240.

A file stored in a RAM pack is not loaded into the 1240 until the LOAD FILE soft key is touched and the X key on the front panel is pressed.

TEST PATTERN GENERATOR

The Test Pattern Generator (TPG) circuitry, located on the Trigger Board, supplies two different signal stimulus patterns. The TPG stimulus output is used for:

- a signal source in application learning examples
- functionally checking 1240 circuitry during specific diagnostic tests

The two output connectors, A14J620 and J630, are located on the right side of the 1240 above the probe connections (refer to Figure 3-7). Each connector contains nine data lines, one clock/qualifier (C/Q) line, and two ground lines. The logic levels for these lines are 4.0 V (H), and 3.2 V (L). The default TPG input threshold selection (made in the Memory Config menu) is +3.70 V.

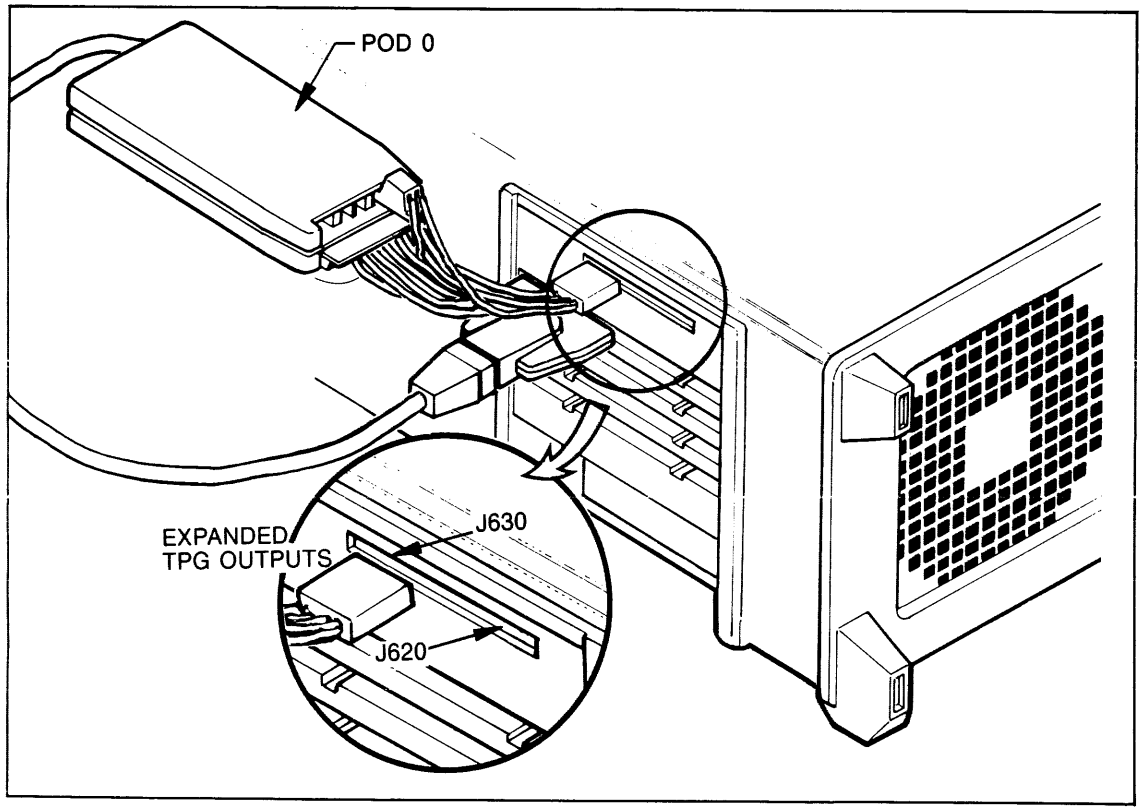

Figure 3-7. TPG output connections.

NOTE

Diagnostic tests require the acquisition probe to be a variable threshold probe, therefore the P6460 probe should be used for connection to the TPG during all diagnostic checks. To ensure true diagnostic test results, the TPG should be in a state of proper calibration. For calibration procedures, refer a qualified service technician to the Trigger Board adjustments in the Verification And Adjustment *section of this manual.*

The TPG outputs a different 9-bit word, 63-word-long pattern for each connector (refer to Table 3-3). The output patterns are selectable (frequency and 5 ns glitches available) according to the value programmed in the real-time Operation Level menu (displayed at power-up if no diagnostic errors are found). The patterns, numbered 0 to 3, are based on a standard 9-bit, pseudo-random binary sequence. The standard pattern may be clocked by the TPG's internal 12 MHz clock, clocked by timebase T1 (set up in the Timebase menu), or single-stepped under processor control (only when using the diagnostics). Table 3-4 summarizes the characteristics of the available patterns.

Table 3-3
TPG PSEUDO-RANDOM PATTERNS

J630*				J620*			
1FF	1AE	071	186	1FF	175	18E	030
1BE	15D	0A2	10C	1F7	0EB	114	061
17D	0FB	145	018	1EF	1DF	028	0C3
0BA	1B6	0CB	030	1D7	1B6	059	186
175	16D	1D7	061	1AE	16D	0BA	10C
0AA	09A	1EF	082	155	0D3	17D	010
155	134	19E	104	0AA	1A6	0F3	020
0EB	069	13C	008	15D	14D	1E7	041
196	092	079	010	0B2	092	1CF	082
12C	124	0B2	020	165	124	196	104
059	049	165	041	0CB	049	12C	008
0F3	0D3	08A	0C3	19E	09A	051	018
1A6	1E7	114	1C7	134	13C	0A2	038
14D	18E	028	1CF	069	071	145	079
0DB	11C	051	1DF	0DB	0E3	08A	0FB
1F7	038	0E3		1BE	1C7	11C	

* Read table top to bottom, left to right.

Table 3-4
PATTERNS AVAILABLE FOR OUTPUT BY THE TEST PATTERN GENERATOR

Pattern Number	With Glitches	Clocked At
0	No	12 MHz
1	Yes	6 MHz
2	No	T1
3	Yes	T1/2

REMOTE DIAGNOSTICS

When the 1240 is operating under the real-time operating system software, a TEST command from a remote controller causes the 1240 to execute its power-up diagnostics. The error information collected during the diagnostics is available after test completion while in the normal operating software. After executing the TEST command, the 1240 returns to the default power-up state. The previous setup, if any, is available in storage memory, but not in acquisition or reference memories. The 1240 notifies the controller that the diagnostics are completed with the Test Complete SRQ. After receiving the TEST command, but before sending the SRQ, the 1240 ignores all bus activity.

To read the collected error information, the remote controller sends the DIAG? query. Data returned to the controller is in the following format:

DIAG ERRORS NNNNN NNNNN NNNNN NNNNN...

or

DIAG "ERRORS NOT FOUND"

The leftmost digit of NNNNN is the test sequence number. If more than one of any type of acquisition card is installed, two 9-channel boards for example, this digit will show which module has the error. Use the remaining four digits as error indexes to locate the troubleshooting information in the *Troubleshooting And Repair* section of this manual.

SECTION 4 THEORY OF OPERATION

SECTION 4 THEORY OF OPERATION

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THEORY OF OPERATION

SECTION OVERVIEW

This section provides general and specific information on 1240 Logic Analyzer circuitry. The circuitry is grouped into functionally named modules that correspond to a specific board (e.g., Power Supply or I/O Processor Boards). In some cases, however, a board may contain circuitry for more than one module. In these cases, only the circuitry related to that board's function is discussed within that subsection. For example, the Display Board contains both display and trigger circuits, however, the trigger circuitry is discussed separately under the Trigger Board theory.

The *General System Description* is presented first. This outlines the logic analyzer mainframe and describes instrument functions at a system level. Next is a *Detailed System Description* that divides each board into functional blocks. When reading these descriptions, refer to the system block diagram, the appropriate functional block diagram, and the appropriate schematics. Each block in the functional block diagrams corresponds to a subheading in the detailed theory descriptions. The detailed descriptions also provide schematic diamond numbers referencing the appropriate schematic.

LOGIC CONVENTIONS

Digital logic techniques are used to perform most functions within this instrument. Function and operation of the logic circuits are represented by standard logic symbols and terms. All logic functions are described using the positive logic convention. Positive logic is a system of notation whereby the more positive of two levels is the true, or 1 state; and the more negative level is the false, or 0 state.

In logic descriptions, the more positive of the two logic voltages is referred to as high, and the more negative state as low. The specific voltages that constitute a high or low state vary between different electronic devices (e.g., ECL logic and TTL logic).

Active-low signals are indicated by an (L) following the signal name or by a horizontal line above the signal name (e.g., $\overline{\text{IRQ}}$). Signal names without indicators are considered active-high. Some active-high signals are indicated by an (H) following the signal name.

GENERAL SYSTEM DESCRIPTION

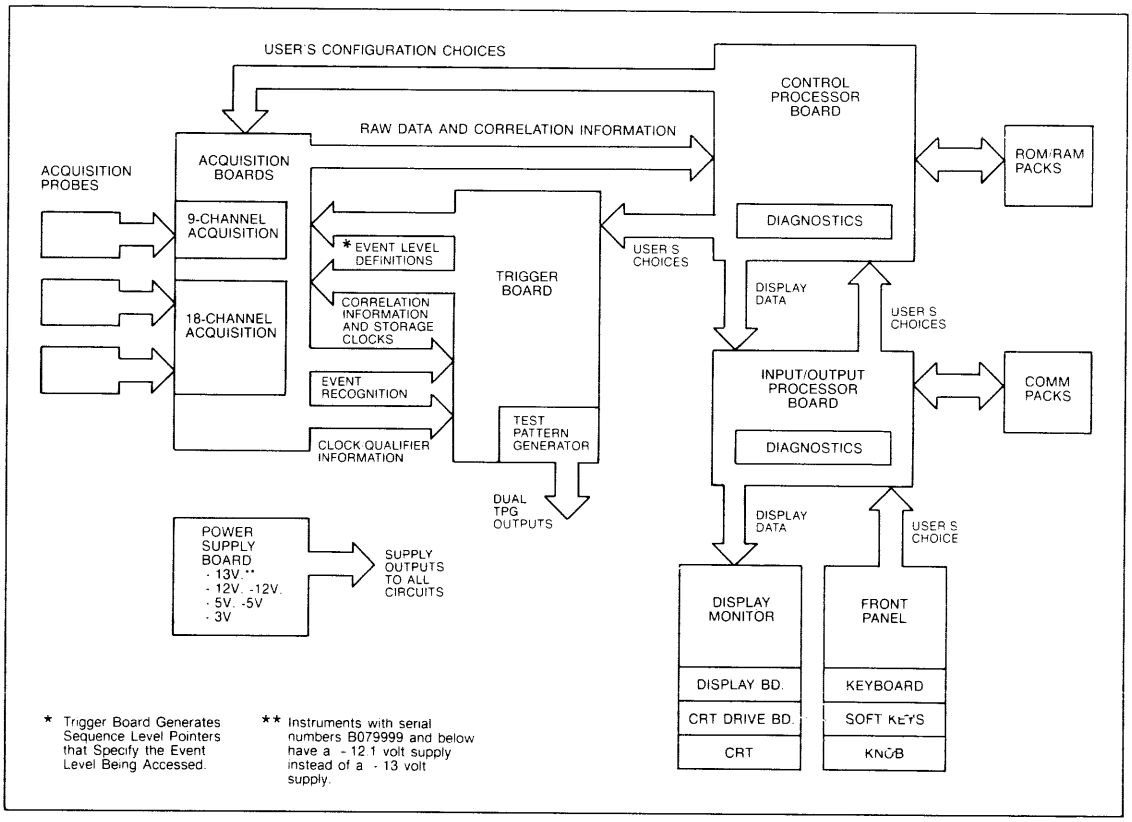

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Figure 4-1. 1240 system block diagram.

OVERVIEW

The 1240 is a menu-driven logic analyzer. The menus are displayed on a monitor screen and are accessible from the keyboard. Selections made in the menus control the 1240 during data acquisitions, triggering, and data display.

The Control Processor and I/O Processor Boards are the main controllers for all instrument operations. The I/O Processor Board accepts the keyboard and on-screen soft key information and passes these user menu choices to the Control Processor. The Control Processor sends these instructions to the Trigger Board and Acquisition Boards, specifying the configuration and conditions surrounding the data acquisition. When conditions are met, the data is stored and the Control Processor performs any necessary data manipulation. Data that is ready for display is read by the I/O Processor and passed to the Display Board. The Display Board generates the screen-display image on the CRT.

MAINFRAME

The 1240 mainframe consists of both chassis-mounted assemblies and a card cage that holds up to eight instrument boards. The hinged card cage, located on the right side of the instrument, allows access to boards plugged into an Interface Board. Refer to Figures 4-2 and 4-3 for illustrations of the 1240 mainframe and the location of instrument boards.

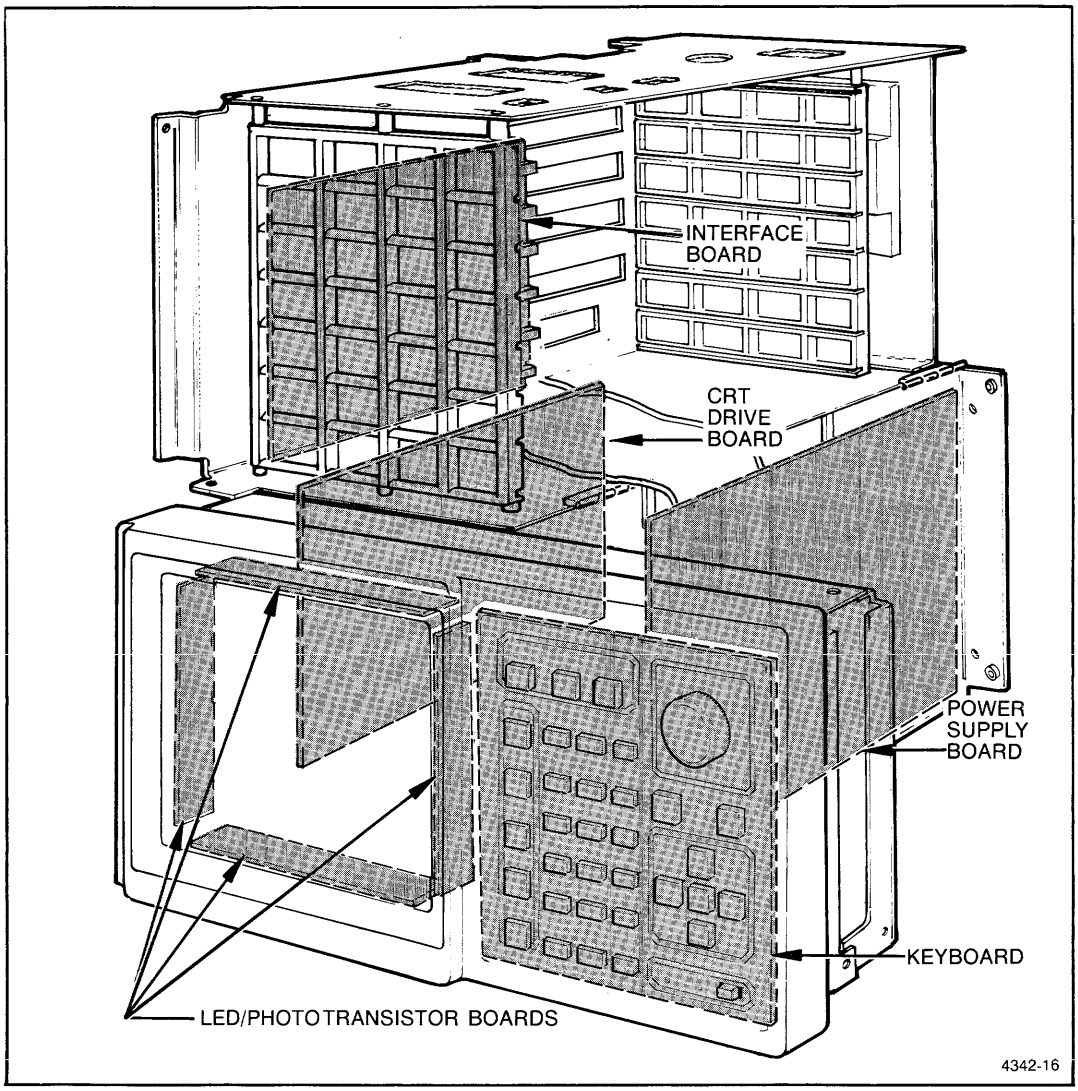


Figure 4-2. 1240 mainframe board locations.

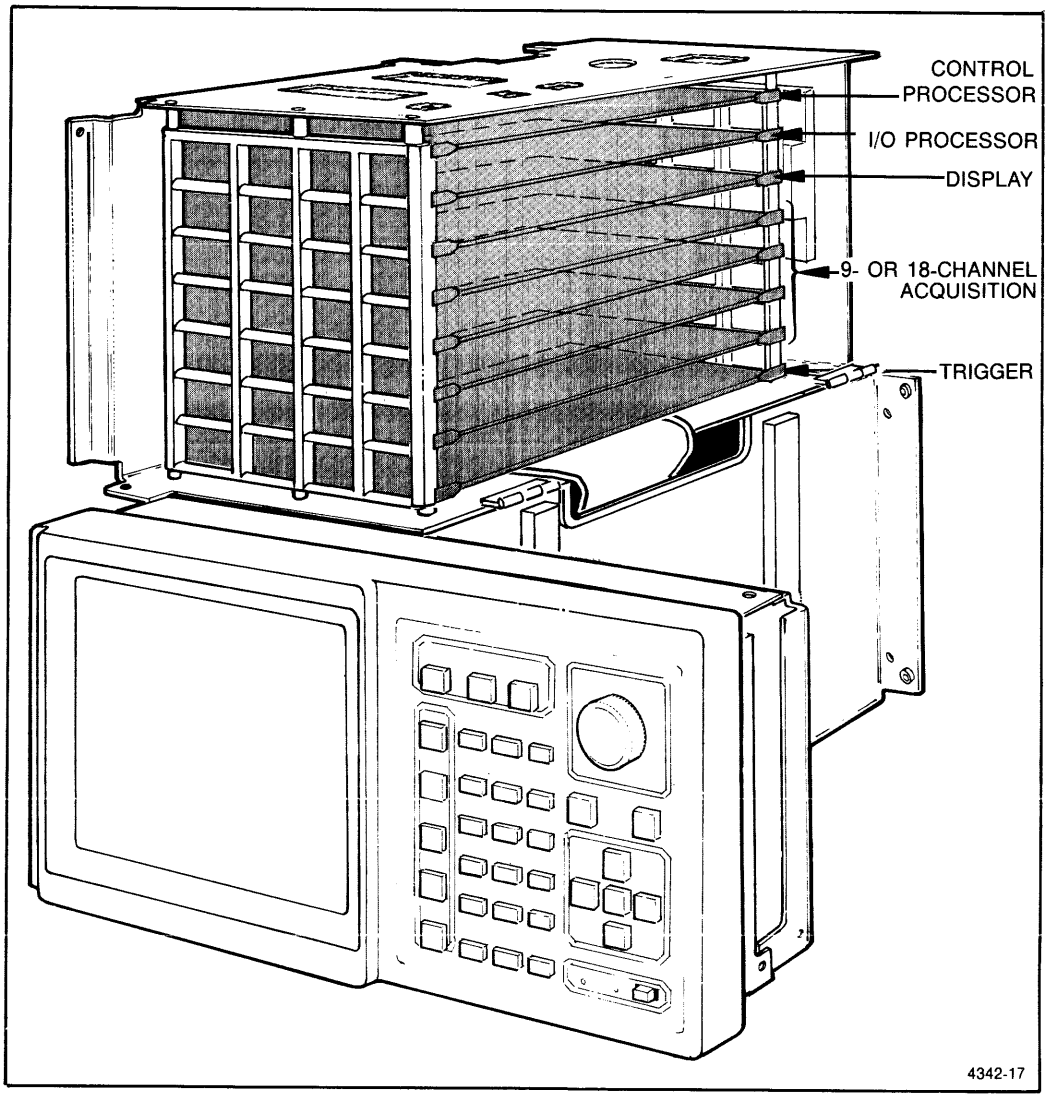


Figure 4-3. 1240 card-cage board locations.

Acquisition probes for the 9-Channel and 18-Channel Acquisition Boards attach through openings on the right side of the 1240 mainframe. ROM and RAM packs are installed in the slot directly beneath the probe connections. COMM (communication) packs are installed in a similar slot on the rear panel. Some instrument controls and connectors are also on the rear panel.

POWER SUPPLY

The 1240 power supply is a switching-type supply that provides +13vdc, +12vdc, -12vdc, +5vdc, -5vdc, and +3vdc to all system circuitry. These voltages are carried through a bus on the Interface Board and various ribbon cables. Test points on the Interface Board serve as power supply voltage reference points. The Line Select switch on the rear panel controls selection of either 115 vac or 230 vac power source. The power cord connection and instrument fuse are also on the rear panel.

A power supply load jumper, located on the Power Supply Board, adjusts the supply current limit to handle the current configuration (i.e., the number of installed acquisition boards).

NOTE

The jumper change should only be performed by qualified service personnel. To determine the need for a change, refer to the Maintenance *section of this manual.*

INTERFACE

The Interface Board provides a means of connecting various instrument boards together, forming an interactive system. The Interface Board is fixed to the inside of the card cage and has board edge connectors for the I/O Processor, Control Processor, Display, 9- and 18- Channel Acquisition, and Trigger Boards. Refer to Figure 6-2 for instructions on positioning these boards in their appropriate connectors. The interface uses ribbon cables for connection to the Power Supply, Keyboard, LED/Phototransistor Boards, and the CRT Drive Board.

Circuitry on the Interface Board supports trigger functions by logically ORing certain glitch qualifier information from all installed acquisition boards. In addition, word recognizer information from all aquisition boards is ANDed on the Interface Board. The outputs from this circuitry form sampling clocks that validate information on the probe's clock/qualifier lines.

A thermal fuse, located on the Interface Board, monitors the 1240's internal temperature. Should the fuse open due to excessive internal heat, instrument operation will not be possible until the fuse is replaced. For more information, refer to the *Troubleshooting and Repair* section.

DISPLAY MONITOR

The display monitor consists of a 7-inch CRT, a CRT Drive Board, and a Display Board (refer to Figure 4-2). The CRT Drive Board generates the high voltage and sweep synchronization for the CRT. The Z-axis signal is produced on the Display Board. Display Board logic outputs characters and timing diagram symbols according to the information it receives from the I/O Processor. The logic also tracks the positioning of the characters on the display screen, thereby supporting the text and timing diagram scrolling features.

The Display Board uses three different types of video patterns to display information. Most information is displayed in regular video. Reverse video (dark characters on a light background) and highlighted video (light characters on a shaded background) are used for indicating menu fields or emphasizing important information.

ROM and RAM packs plug into a connector mounted on the Control Processor Board. The connector is accessed through a door located on the right side of the instrument. The Control Processor handles all information storage and retrieval operations for these packs.

COMM PACKS

Communication packs provide a customized communication link between the 1240 and an external controller. COMM packs are available for RS232C, GPIB, and 8-bit parallel printer protocols.

COMM packs plug into a connector mounted on the CRT Drive Board. The connector is accessed through a door located on the rear panel. A ribbon cable carries the COMM pack address, data, and control lines from the CRT Drive Board to the Interface Board. The I/O Processor, plugged into the Interface, handles all COMM pack communications.

Tables 4-0a and 4-0b contain the signal-to-pin assignments for the COMM pack connector. The following glossary contains COMM pack connector signal descriptions.

Signal Name	Description
GND	Signal ground, (two connections).
SGND	Static ground to chassis, (two connections).
+5V	Five volt logic supply must be cabable of supplying 400 mA.
−12V	Minus twelve volts must be capable of supplying 100 mA.
+12V	Plus twelve volts must be capable of supplying 100 mA.
INT (H)	Interrupt. Output from the COMM Pack used to interrupt the MPU, causing a service routine to be executed.
CLK	2.4576 megahertz clock; input to the module.
RESET	Reset. Input to the COMM Pack that initializes the COMM Pack.
D0-D7	Data lines. Tristate input/output bus used for all data transfers.
A0-A13	Address lines; driven by the I/O P.
RD (L)	Read inverted; input to the module. Logic low on this line causes the DATA BUS to read data from the MPU.
WR (L)	Write inverted; input to the module. Logic low on this line causes the DATA BUS to write data to the MPU.
COMM (L)	I/O chip enable; input to the module. When true (logic low) the I/O addresses are active for reading or writing.
CROM (L)	Memory chip enable; input to the module. When true (logic low) will enable the ROM memory addresses to be read.

Table 4-0a
A Side Connector

Pin	Signal	Description
A1	WR (L)	Write
A2	RESET	Reset COMM Pack
A3	A5	Address, 6th bit
A4	D1	Data, 2nd bit
A5	D3	Data, 4th bit
A6	D5	Data, 6th bit
A7	D7	Data, MSB
A8	D6	Data, 7th bit
A9	D4	Data, 5th bit
A10	D2	Data, 3rd bit
A11	D0	Data, LSB
A12	FREQ	2.4576 MHz
A13	CROM (L)	Mem. Chip Select
A14	INT (H)	Interrupt
A15	RD (L)	Read
A16	A0	Address, LSB
A17	A2	Address, 3rd bit
A18	A4	Address, 5th bit
A19	+5V	+5V Power Supply
A20	GND	Ground

Table 4-0b
B Side Connector

Pin	Signal	Description
B1	A1	Address, 2nd bit
B2	A3	Address, 4th bit
B3	COMM (L)	I/O Chip Enable
B4	A7	Address, 8th bit
B5	A9	Address, 10th bit
B6	A11	Address, 12th bit
B7	A13	Address, MSB
B8	spare	Not Used
B9	spare	Not Used
B10	spare	Not Used
B11	SGND	Static Ground
B12	SGND	Static Ground
B13	A12	Address, 13th bit
B14	A10	Address, 11th bit
B15	A8	Address, 9th bit
B16	A6	Address, 7th bit
B17	+12V	+12V Power Supply
B18	−12V	−12V Power Supply
B19	+5V	+5V Power Supply
B20	GND	Ground

LED/PHOTOTRANSISTOR BOARDS AND KEYBOARD

The LED/Phototransistor Boards are arranged around the perimeter of the 1240 display screen. These LEDs and PTs form a light-beam matrix on the surface of the screen. The intersection of the light beams define a specific area on the screen (soft key boxes). When the user touches a soft key, the light beam is interrupted and that specific soft key is activated.

The hard keyboard contains 33 front panel push-button keys. The keys are grouped on the front panel by function (e.g., EXECUTE, CURSOR, or MENU). Surrounding the hard keyboard are other front panel controls such as the dc power switch and the rotary knob used for scrolling and selection.

I/O PROCESSOR

The Input/Output Processor consists of a Z80 microprocessor, ROM and RAM space, with a bidirectional bus for communication with the front panel, Display Board, Control Processor, and COMM packs. The I/O Processor monitors the front panel for any hard or soft key changes made by the user. The change instructions are passed to both the Control Processor and the Display Board. The Control Processor instructs the circuitry under its control to function as specified by the user. Display update information is sent from the I/O Processor to the Display Board's display memory.

Interrupt detection circuitry allows the I/O Processor to service any interrupts sent by the COMM pack port, the Control Processor, or the Display Board. The Control Processor sends an interrupt when it has completed the formatting and manipulating of data for the I/O Processor. The I/O Processor then passes the display information to the display monitor, but only after the Display Board signals that vertical retrace is occurring (display update time).

CONTROL PROCESSOR

The Control Processor consists of an 8088 microprocessor, ROM and dynamic RAM space (with a bidirectional bus for communication with the acquisition boards), and trigger circuits (some trigger circuits also reside on the Control Processor Board). The Control Processor communicates with any installed ROM or RAM Packs and the I/O Processor Board. The Control Processor directs the acquisition and trigger circuits according to instructions it receives from the user through the I/O Processor. After a data acquisition, the Control Processor performs any required data manipulation and sends this data to the I/O Processor for display. The Control Processor also handles all communications with installed ROM and RAM packs.

An on-board nonvolatile RAM provides storage of up to two instrument menu setups, retrievable after powering down and back up again.

ROM AND RAM PACKS

Nonvolatile RAM packs allow storage and retrieval of instrument setups and memories. RAM packs are available in different memory sizes, depending on the amount of storage space required. A variety of ROM packs are available for use in 1240 operations. ROM packs provide indelible storage for reference memories and setups. Some ROM packs configure the logic analyzer to acquire and disassemble data from specific microprocessors. Other ROM packs contain code that supports COMM Pack functions and diagnostic testing of the 1240.

9-CHANNEL ACQUISITION BOARD

The 1240D1 9-Channel Acquisition Board uses a single data acquisition probe when acquiring data and glitch information. Data storage occurs at a 10 ns asynchronous rate with an on-board memory 513 samples deep. Data/glitch storage occurs at a 20 ns synchronous rate with a memory 256 samples deep. Acquisition probe threshold voltage is variable from +6.35 volts to -6.35 volts.

The 9-channel acquisition card allows data storage to occur according to parameters set by the user. As data first enters the card, a global word recognizer compares the data to patterns previously defined by the user. If a match is found, the data is not necessarily stored. Storage is dependent on the clock/qualifier patterns also set by the user. If the patterns on the probe's C/Q lines also match, then data (and glitch information, if defined) is latched into the on-board storage RAM by store signals from the trigger board. Clock/qualifier lines from like acquisition cards (in this case 9-channel cards) are combined to allow qualification to occur from inputs on any attached 9-channel acquisition probes.

Incoming data is also fed to a sequential word recognizer. In this circuitry, up to 14 levels of different data patterns may be stored prior to data or data/glitch acquisitions. As user-specified patterns match on each level, the acquisition card signals the trigger board. The trigger board in turn advances the comparison to another level that contains the next pattern to be recognized. Storage of matching information on each level is also dependent on the probe's C/Q lines.

Chaining of like acquisition cards (in this case 9-channel cards) allows memory depth expansion. Incoming data that meets all storage qualification parameters is passed to the next available memory space on the chained cards. When storage is complete, the trigger board stops the acquisition. The Control Processor then reads the acquisition data, glitch, and correlation information stored in the acquisition's storage RAMs. The correlation information allows data acquired at different speeds to be displayed with the time relationship between probe data still preserved.

18-CHANNEL ACQUISITION BOARD

The 1240D2 18-Channel Acquisition Board uses two data acquisition probes when acquiring data information (glitch acquisitions not available). Data storage occurs at a 20 ns synchronous or asynchronous rate with a memory 513 samples deep. Different timebases may be chosen for the two input acquisition probes, allowing one 18-channel card to operate from a single timebase (T1 or T2), dual timebases (T1 and T2), or from a split timebase (T2F/T2L, i.e., timebase 2 first/timebase 2 last). Acquisition probe threshold voltage is variable from +6.35 volts to -6.35 volts.

The 18-channel card acquires data in much the same way as the 9-channel card, however, the 18-channel card handles both A and B probe data. Storage qualification is provided by both global and sequential word recognizers and by the probe's clock/qualifier lines. Clock/qualifier lines from like acquisition cards (in this case 18-channel cards) are combined to allow qualification to occur from inputs on any attached 18-channel acquisition probes. Memory chaining to other 18-channel cards allows memory expansion up to 2049 samples deep (four 18-channel cards installed).

TRIGGER BOARD

The trigger circuitry allows the 1240 to locate a unique state based on its inputs and user programming, and reference data storage to that unique state. Trigger circuitry is located on the Trigger Board, the Display Board, and the Control Processor Board. The overall trigger system can be divided into two major operating control systems. The first, trigger generation, recognizes and triggers on the unique state being searched for. The second, data storage control, monitors the valid (qualified) data being stored to determine the amount of memory space that surrounds the trigger point. This circuitry also generates correlation data that indicates storage-clock arrival time for each timebase.

Trigger Generation

The trigger generation control system consists of the various function blocks (refer to Figure 4-4) that are briefly described in the following.

The Sequential Event Timing and Control block generates the basic clocks used to sample sequential events and determines the sequential event level to advance or reset to. The Sequential Filter block forces a recognize sequential event to be active for a specified number of clocks before it is recognized as a true event. The Iteration Counter block forces the test on a specified sequence level to be qualified with a specific number of sequential events before the command portion of the sequence level is executed. The Global Filter block forces a recognized event to be active for a specified number of clock cycles before it is recognized as a true event. The Counter/Timer block can be used to count occurrences, to start a 10 ns timer, or to time the duration of the global filter output. The Trigger Control block tests the state of internal trigger conditions and external trigger inputs to determine when valid trigger states exist.

Data Storage Control

The data storage control system consists of the various function blocks that are briefly described in the following.

The Trigger Position Indicators (1 and 2) count the number of valid (qualified) data samples. Since the 1240 can acquire data using two independent timebases (T1 and T2), a trigger position indicator exists for each. Trigger position registers are loaded with a value representing the amount of memory to be filled before and after the trigger point. The Correlate Circuit uses inputs from Timebase 1 and Timebase 2 to produce data that indicates when a storage clock occurred from each timebase. This data is stored along with valid data in the acquisition board's storage RAMs. The Control Processor reads the data to reconstruct data for display as it occurred at the probe tip, preserving the time relationship of data stored with timebases set at different speeds.

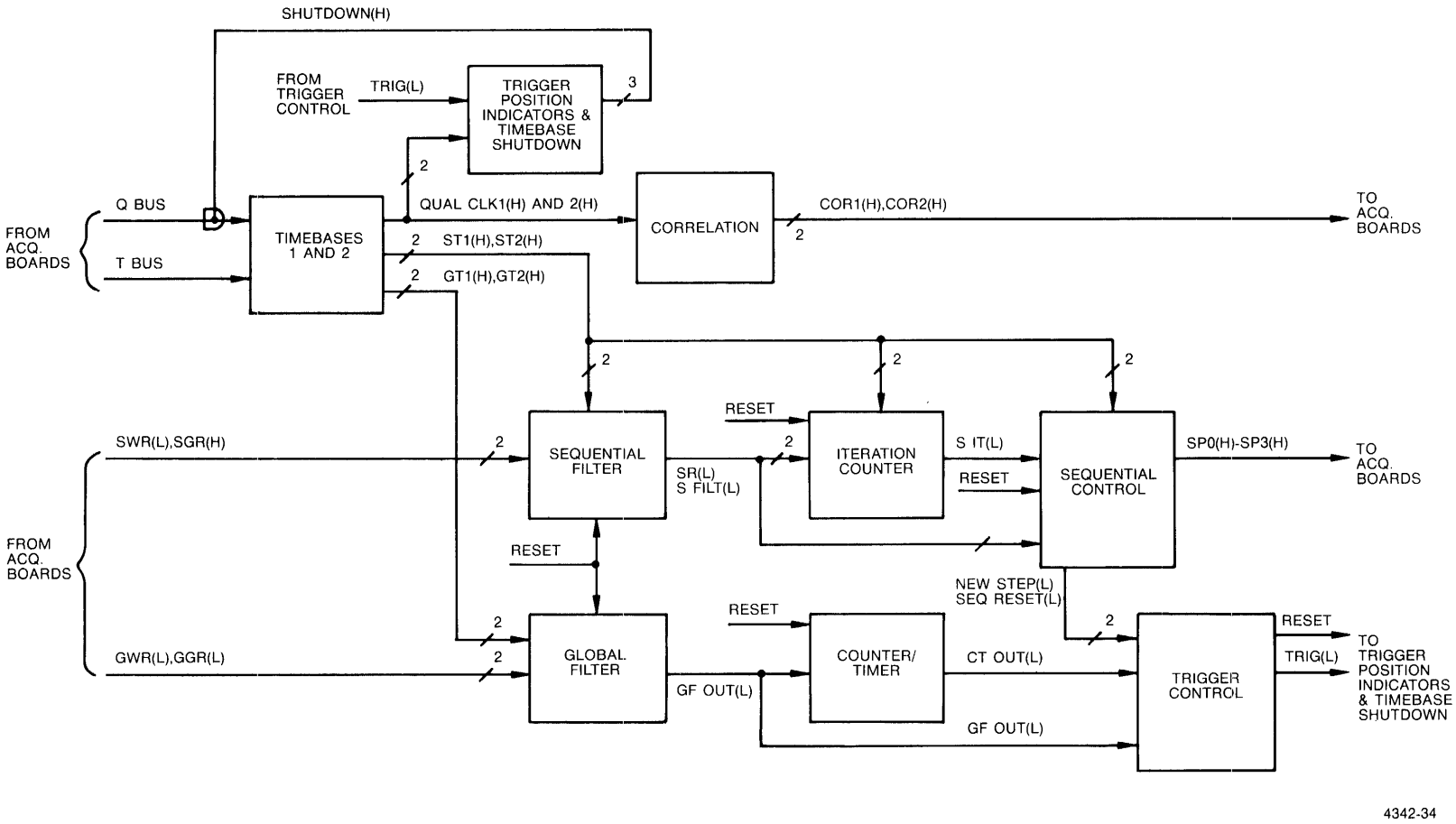


Figure 4-4. Simplified trigger block diagram.

DETAILED SYSTEM DESCRIPTION

OVERVIEW

Refer to schematics in the *Schematic Diagrams* section of this manual while reading this detailed circuit description. Numbers inside diamonds relate to subsection headings and are keyed to the diamond numbers on page tabs of the *Schematic Diagrams* section.

Active-low signals are indicated by an (L) following the signal name or by a horizontal line above the signal name (e.g., $\overline{\text{IRQ}}$). Signal names without indicators are considered active-high. Some active-high signals are indicated by an (H) following the signal name.

Assembly numbers (A numbers) identify components and the board these components are mounted on. The designation A10R100 identifies the board as assembly A10 the I/O Processor Board), and the component number as resistor R100.

To distinguish between each of the four identical acquisition board slots in the mainframe, the * symbol in a signal name takes on a letter from A to D. For example, the signal TEST*(H) is common to four different acquisition slots, but becomes TESTA(H) when referencing acquisition slot 0 (J250). The remaining designations are: * = B for slot 1 (J350), * = C for slot 2 (J450), and * = D for slot 3 (J550).

670-7534-06 POWER SUPPLY THEORY

LINE FILTER AND RECTIFIER ◇5◇

The incoming ac line is rectified by the full-wave bridge CR211 and filtered by C121 and C131 to approximately 350 volts dc (across TP411 and TP422). Switch S100 removes the ac line from the power supply circuitry (however, not from the fuse or switch itself). S401 selects internal circuitry for operation using either a 115 volt or 230 volt power source.

CAUTION

A lighted or blinking neon lamp (DS121) indicates that the line filter capacitors remain charged to at least 70 volts. This lamp is visible through a hole on the power supply cover, adjacent to the warning label. Do not touch the power supply circuitry while the lamp is on.

FRONT PANEL SHUTDOWN SWITCH ◇5◇

The dc power switch, S181, allows you to power up the 1240 from the front panel. A thermal fuse is mounted in series with S181 on the interface board. When the power supply switch is turned off (open), or when the thermal fuse is open, transistor A07Q273 holds the reset line low to the Main Regulator A07U375-5. When the power supply switch is turned on (closed), transistor Q273 allows the line to go high, removing U375's reset condition. T141 temporarily supplies current to Q283 in the Kick Start Circuitry until the supply begins to run.

The SHUTDOWN(L) signal is a wire-OR of Q273 and U375-8 and is activated by either the front panel switch (via Q273) or the shutdown signal (via U375-8). The active low shutdown signal from pin 8 comes in response to a current limit condition in the supply. SHUTDOWN(L) is sent through the Interface to the I/O Processor Board. The active low signal generates a processor reset. In addition, this reset signal is transmitted to the Control Processor Board on the IRST(H) interrupt line. This line, when activated, removes the vcc from the output buffer A09U217 in the ROM/RAM Pack Control circuit and tristates the outputs. This prevents the data in the Non-volatile Memory, A09U229, and any pack plugged in to the ROM/RAM Pack port from being changed while the power supplies are unstable. The IRST(H) line is converted to the RESET(H) line which resets the Control Processor's 8088.

KICK START CIRCUITRY ◇5◇

When powering up, the current from transformer T141 passes through Q283 and charges C465 to approximately +25 volts. At this time, the Schmitt trigger transistors (Q472 and Q485) turn on and deliver approximately +25 volts to the input of the +20 volt regulator U371. The capacitor C465 temporarily supplies the current passing through Q471 for the base drive transistors (Q341 and Q445, in the Main Regulator) until the +25 volt supply is up. When the Schmitt trigger fires, Q283 turns off and current is no longer drawn from T141.

When the front-panel switch S181 is opened, or when the thermal fuse has blown, Q273 pulls down on the reset and shutdown lines of U375. During power-down, the Schmitt trigger turns off when C465 reaches approximately +15 volts. This removes the voltages used by U375 and shuts down the power supply.

MAIN REGULATOR ◇5◇

The Pulse Width Modulator I.C. U375 is the main controller of the power supply. When the Kick Start Circuit's Schmitt trigger transistors turn on, approximately +25 volts is supplied to the +20 volt regulator U371. The regulator then provides the vcc to U375. This allows U375 to produce complementary base drive signals for A7Q341, Q441, Q445, and Q446. Components C364, R375, C379, and R365 control the timing of these base drive signals on pins 13 and 16. Q471 supplies current to the collectors of the base drive transistors Q341 and Q445. T431 couples the drive signal to the primary switching transistors, Q421 and Q422.

Primary current is sensed through T432 as a 20 kHZ primary signal. The amplitude of resulting waveform across R440 depends on the positioning of the primary current limit jumper, A07J444. Jumper A07J444 provides a method for increasing the primary current limit when the 1240's card cage contains more than two acquisition cards.

NOTE

Jumper A07J444 should be positioned in the low-load setup (pin 2 shorted to pin 3) when two acquisition cards, either 9-channel or 18-channel, are installed. If more than two 9- or 18-channel cards are installed, the jumper should be positioned in the high-load setup (pin 1 shorted to pin 2).

A precision rectifier, formed by U275C and D, rectifies the waveform across R440 into a unidirectional pulse. The low pass filter, R274 and C276, produces an average dc voltage proportional to the current in the primary winding of T241. This primary-sensed dc voltage is fed to comparator U275B.

U275B compares the primary-sensed current limit voltage value at U275B-6 against a +4.43 volt reference at U275B-5 to determine the load conditions in the Primary Switching Circuit. If the primary-sensed value is less than the +4.36 volt reference value, comparator U275B drives the current limit input high at U375-7 and shuts down the power supply.

U275A compares the voltage drop across thermistor RT271 against a 2.5 volt reference value to determine fan speed. For moderate room temperatures, the thermistor causes comparator U275A to operate the fan at a reduced speed. If the temperature in the 1240 begins to rise excessively, the fan is allowed to operate at full speed. Transistors Q379 and Q385 serve as a power amplifier to supply the fan operating voltage.

PRIMARY SWITCHING CIRCUIT ◇5◇

The half-wave bridge chopper (formed by Q422, Q421, C321, and C322) converts the 350 volt dc level to a 20 kHZ pulse width modulated wave. T431 couples a complementary pair of 20 kHZ base drive switching signals from the Main Regulator to Q421 and Q422. Power transformer T241 couples the square wave (at TP421) to the Secondary Rectifier And Filter.

OVER-VOLTAGE PROTECTION ◇5◇

Output over-voltage protection is provided by the SCR Q371. The SCR pulls down on the +20 volt line to U375 pin 17 when the +5 volt supply exceeds approximately +6.2 volts, or the −12 or −5 volt supplies are pulled positive. If Q371 is triggered, the power must be turned off, then on again, to restart the power supply.

SECONDARY RECTIFIER AND FILTER ◇5◇

A 20 kHZ pulse width modulated wave from the primary switching circuit is rectified and filtered on the secondary side of T241. The +5 volt output is full-wave rectified and filtered by CR445, CR451, L151, L351, and C451. Additional +5 volt filtering is provided by L461 and C161. Full-wave rectifying and filtering circuitry produces a +16 volt supply (balanced by A07T261) to feed the +13 volt regulator and the ±12 volt regulators. The −5 volt regulator is supplied with −8 volts by half-wave rectifying and filtering the 20 kHz waveform.

3-TERMINAL REGULATORS ◇5◇

The 3-terminal regulators convert voltages from the secondary rectifier circuitry to output supply voltages used by the 1240 circuitry. All four regulators have built-in current limiting and thermal shut down protection. The +13 volt regulator, U472, -12 volt regulator, U181, and the +12 volt regulator, U481, are fed by ±16 volt inputs. The -5 volt regulator, U471, is fed by a -8 volt input.

+3 VOLT SUPPLY ◇5◇

The +3 volt supply (TP162) is actually a -2 volt supply down from the +5 volt supply, forming a current sink instead of a current source. The comparator U385B controls the output voltage and switching frequency. The +5 volt sense line supplying a reference voltage to U385B causes the +3 volt supply to shutdown if the +5 volt supply shuts down. Transistors Q487 and Q387 act as signal buffers which feed the switching transistor Q461. Comparator U385A controls current limiting by using R461 as the current sense.

670-7534-05 POWER SUPPLY THEORY

LINE FILTER AND RECTIFIER ◇5

The incoming ac line is rectified by the full-wave bridge CR211 and filtered by C121 and C131 to approximately 350 volts dc (across TP411 and TP421). Switch S100 removes the ac line from the power supply circuitry (however, not from the fuse or switch itself). S401 selects internal circuitry for operation using either a 115 volt or 230 volt power source.

CAUTION

A lighted or blinking neon lamp (DS121) indicates that the line filter capacitors remain charged to at least 70 volts. This lamp is visible through a hole on the power supply cover, adjacent to the warning label. Do not touch the power supply circuitry while the lamp is on.

FRONT PANEL SHUTDOWN SWITCH ◇5

The dc power switch, S181, allows you to power up the 1240 from the front panel. When the power supply switch is turned off (open), transistor A07Q273 holds the shutdown line low to the Main Regulator A07U372. When turned on, transistor Q273 allows the shutdown line to go high, removing U372's shutdown condition. T141 also temporarily supplies current to Q281 in the Kick Start Circuitry until the supply begins to run.

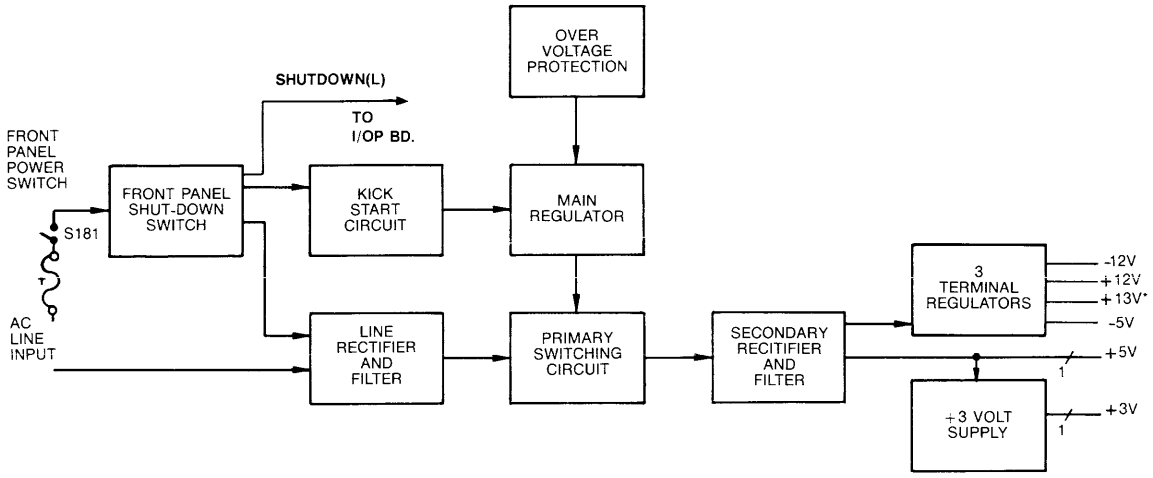
KICK START CIRCUITRY ◇5

When powering up, the current from transformer T141 passes through Q281 and charges C471 to approximately +25 volts. At this time, the Schmitt trigger transistors (Q472 and Q382) turn on and deliver approximately +25 volts to the input of the +20 volt regulator U371. The capacitor C471 temporarily supplies the current passing through Q471 for U372 (both in the Main Regulator) until the +25 volt supply is up. When the Schmitt trigger fires, Q281 turns off and current is no longer drawn from T141.

When the front-panel switch S181 is opened, Q273 pulls down on the reset and shutdown lines of U372. During power-down, the Schmitt trigger turns off when C471 reaches approximately +15 volts. This removes the voltages used by U372 and shuts down the power supply.

MAIN REGULATOR ◇5

The Pulse Width Modulator I.C. U372 is the main controller of the power supply. When the Kick Start Circuit's Schmitt trigger transistors turn on, approximately +25 volts is supplied to the +20 volt regulator U371. The regulator then provides the vcc to U372. This allows U372 to produce complementary base drive signals for A7Q367, Q368, Q370, and Q371. Components C374, R273, R274, and C274 control the timing of these base drive signals on pins 13 and 16. Q471 supplies current to the collectors of the base drive transistors Q367 and Q368. T431 couples the drive signal to the primary switching transistors, Q421 and Q422.



*Instruments with serial numbers B079999 and below have a +12.1 volt supply instead of a +13 volt supply.

Figure 4-5. Power Supply Board functional block diagram.

POWER SUPPLY BOARD THEORY

OVERVIEW

There are two board versions of the 1240 power supply, the 670-7534-06 and the 670-7534-05. Both power supplies are high-efficiency, switching-type supplies that rectify and filter the incoming ac line (115 V or 230 V) to provide a set of six dc power outputs. These voltages are referenced to the square pins at J658 on the Interface Board. The power supply compensates for line or load variations while supplying these regulated output voltages.

There are three major differences between the power supplies. First, the 670-7534-06 supply contains circuitry that regulates the fan speed according to the temperature inside the instrument. The fan in instruments containing the 670-7534-05 power supply operates at a constant speed. Another difference is that the 670-7534-06 power supply generates an early warning signal, SHUTDOWN(L), that provides the I/O Processor and Control Processor with an early warning signal that initiates a reset condition prior to a power failure. The third difference is in one of the six dc power outputs. The 670-7534-06 power supply has a +13 volt supply (nominal +12.5 V) on TP184; the -05 supply has a +12.1 volt supply (nominal +12 V) at that same test point. The other five dc power outputs are the same for both power supplies: +12 V (TP185), −12 V (TP183), +5 V (TP171), −5 V (TP182), and +3 V (TP162).

NOTE

When using the minimum 1240 configuration, the supply current-limiting resistor (R441) is removed from the circuit. If the 1240 is reconfigured, the 1240 may require a power supply jumper change due to the current number of installed acquisition cards. The jumper change allows the power supply to handle the increased demand for current from the supply. Jumper A07J444 should be positioned in the low-load setup (pin 2 shorted to pin 3) when one or two acquisition cards, either 9-channel or 18-channel, are installed. If more than two 9- or 18-channel cards are installed, the jumper should be positioned in the high-load setup (pin 1 shorted to pin 2).

Primary current is sensed through T432 as a 20 kHZ primary signal. The amplitude of resulting waveform across R440 depends on the positioning of the primary current limit jumper, A07J444. Jumper A07J444 provides a method for increasing the primary current limit when the 1240's card cage is fully loaded.

NOTE

Jumper A07J444 should be positioned in the low-load setup (pin 2 shorted to pin 3) when two acquisition cards, either 9-channel or 18-channel, are installed. If more than two 9- or 18-channel cards are installed, the jumper should be positioned in the high-load setup (pin 1 shorted to pin 2).

Primary current limiting is accomplished by sensing the 20 kHZ primary signal with T432, then rectifying and filtering this signal for the current limit input at U372 pin 7. If this input exceeds 100 mV, U372 shuts down the power supply.

PRIMARY SWITCHING CIRCUIT ◇5

The half-wave bridge chopper (formed by Q422, Q421, C321, and C322) converts the 350 volt dc level to a 20 kHZ pulse width modulated wave. T431 couples a complementary pair of 20 kHZ base drive switching signals from the Main Regulator to Q421 and Q422. Power transformer T241 couples the square wave (at TP422) to the Secondary Rectifier And Filter.

OVER-VOLTAGE PROTECTION ◇5

Output over-voltage protection is provided by the SCR Q371. The SCR pulls down on the +20 volt line to U372 pin 17 when the +5 volt supply exceeds approximately +6.2 volts, or the -12 or -5 volt supplies are pulled positive. If Q372 is triggered, the power must be turned off, then on again, to re-start the power supply.

SECONDARY RECTIFIER AND FILTER ◇5

A 20 kHZ pulse width modulated wave from the primary switching circuit is rectified and filtered on the secondary side of T241. The +5 volt output is full-wave rectified and filtered by CR445, CR451, L151, L351, and C451. Additional +5 volt filtering is provided by L461 and C161. Full-wave rectifying and filtering circuitry produces a +16 volt supply (balanced by A07T261) to feed the +12.1 volt regulator and the ±12 volt regulators. The -5 volt regulator is supplied with -8 volts by half-wave rectifying and filtering the 20 kHz waveform.

3-TERMINAL REGULATORS ◇5◇

The 3-terminal regulators convert voltages from the secondary rectifier circuitry to output supply voltages used by the 1240 circuitry. All four regulators have built-in current limiting and thermal shut down protection. The +12.1 volt regulator, U472, -12 volt regulator, U181, and the +12 volt regulator, U481, are fed by ±16 volt inputs. The -5 volt regulator, U471, is fed by a -8 volt input.

+3 VOLT SUPPLY ◇5◇

The +3 volt supply (TP162) is actually a -2 volt supply from the +5 volt supply, forming a current sink instead of a current source. The comparator U385B controls the output voltage and switching frequency. The +5 volt sense line supplying a reference voltage to U385B causes the +3 volt supply to shutdown if the +5 volt supply shuts down. Transistors Q481 and Q482 act as signal buffers which feed the switching transistor Q461. Comparator U381A controls current limiting by using R461 as the current sense.

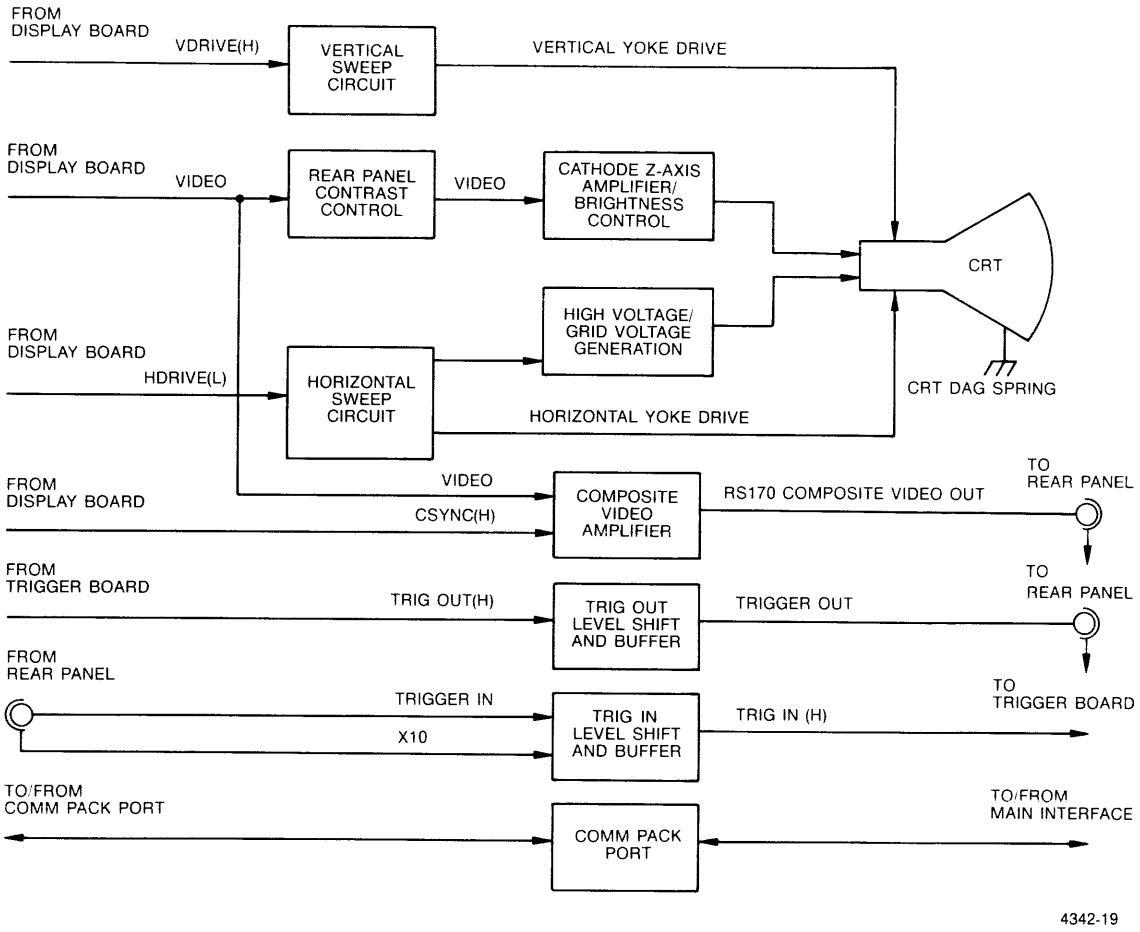


Figure 4-6. CRT Drive Board functional block diagram.

CRT DRIVE BOARD THEORY

OVERVIEW

The CRT Drive Board holds the circuitry necessary for driving the raster scan CRT. The video and sync signals from the Display Board are used in generating the Z-Axis, sweep signals, and grid bias voltages for the CRT. In addition to the basic monitor functions, this board also has circuitry supporting the rear panel functions. These circuits include trigger in and out buffering, composite video out, contrast control, and a COMM (communication) pack interface.

VERTICAL SWEEP CIRCUIT ◈4◈

The vertical processor, A6U311, generates the sweep current for the vertical deflection yoke. The vertical processor includes a voltage-controlled oscillator, a voltage ramp generator, a high-gain amplifier, and a flyback generator. These circuits provide vertical sweep synchronization, vertical height deflection, and vertical linearity.

A6U311 synchronizes to the 60 Hz, TTL-level VDRIVE(H) signal. The amplifier output at pin 4 provides the vertical yoke sweep current. During the vertical sweep, A6C312 charges to approximately +12 volts. When the sweep reaches the bottom of the screen, the voltage on C312, added to the +12 volt supply at A6U311 pin 2, is internally applied to the pin 4 output. This produces the +24 volt flyback signal that causes the vertical deflection beam to return to the top of the screen.

The vertical size control, A6R221, adjusts the magnitude of sweep current, thereby setting the amount of vertical deflection. The vertical hold control, A6R320, is part of an RC timing circuit that produces a ramp at the oscillator input pin 9. Adjusting the ramp's frequency rate to 60 Hz causes vertical synchronization to occur. The vertical linearity control, A6R300, compensates for any non-linearity in the ramp-generating circuitry.

HORIZONTAL SWEEP CIRCUITRY ◈4◈

The major parts of the horizontal sweep circuit are the horizontal processor A6U534, the horizontal deflection yoke, the S-shaping capacitor A6C424, the retrace capacitors A6C345 and C350, the clamping diode A6CR452, and the horizontal switching transistors A6Q445 and Q560. These parts work together to produce a horizontal deflection current that sweeps the video beam across the CRT. This circuit also produces a flyback signal to the flyback transformer that is in parallel with the horizontal deflection yoke.

The horizontal processor, A6U534, provides a drive signal for the sweep circuit. This square-wave drive signal, output at A6U534 pin 1, is coupled through A6T555 and applied to the base of the switching transistor A6Q560. The transistor's output signal is synchronized to the HDRIVE(L) signal through an integrating circuit at pin 4. A6U534 internally compares the two inputs (pin 3 and pin 4) for a phase shift between the two. If any phase shift is detected, the phase detector's output at pin 5 adjusts the oscillator's output frequency at pin 1.

A6Q560 is turned on while the horizontal beam is sweeping towards the left side of the screen. During this time, the deflection current from the yoke is routed to ground. When the base drive signal turns Q560 off, the beam is at its maximum sweep (deflection) and the voltage at Q560's collector flys up to approximately 150 volts. This is the horizontal flyback signal. At this time, the yoke current quickly ramps to a negative value, causing the beam to retrace to the right side of the screen.

Due to several factors (e.g., a flat image screen, non-linear components, etc.), a control is available to allow current ramp shaping. This affects the linearity of the screen image. The horizontal linearity control, A6L435, controls image shaping on the left side of the screen, while the non-adjustable capacitor, A6C424, controls image shaping on the right side of the screen. The horizontal width control, A6L600, allows a total circuit inductance adjustment that changes the current ramp for desired horizontal beam deflection. The horizontal hold control, A6R513, is part of an RC timing circuit that produces a ramp at the oscillator's input pin 7. Adjusting the ramp's frequency rate to approximately 15750 KHz causes horizontal synchronization to occur. The horizontal position control, A6R553, provides a variable phase shift to the feedback ramp at pin 4, thereby allowing a left or right shift in the screen image.

If an over-voltage condition arises due to an increase in flyback-generated supply voltages, the Zener diode, A6VR435, increases the voltage to the oscillator within A6U534. The resulting increase in the horizontal output frequency to the flyback transformer causes voltage limiting.

HIGH VOLTAGE/GRID VOLTAGE GENERATION ◇4◇

The 10 kV CRT anode potential and other bias voltages are generated by the flyback transformer A6T251 from the flyback waveform. This transformer is in parallel with the horizontal yoke and also supplies some of the sweep current for the yoke winding. The following list specify the voltages generated, and their uses.

10 kV	for CRT anode
+500 Vdc	for acceleration grid (pin 2) and focus grid (pin 4)
+55 Vdc	for video Z-axis amplifier
−75 Vdc	for brightness control

CATHODE Z-AXIS AMPLIFIER/BRIGHTNESS CONTROL ◇4◇

The video signal from the Display Board (attenuated by the rear panel Contrast control) is amplified by A6Q106. The resulting output is applied to the CRT through an inductive peaking network in the CRT cable assembly, W230. The Z-axis amplifier, A6Q106, operates in a common-emitter configuration with a 22 MHz bandwidth.

The screen brightness adjustment, A6R325, controls the bias voltage on grid 1 of the CRT, thereby allowing a variation of voltage potential between the cathode and grid 1.

COMPOSITE VIDEO AMPLIFIER ◇3◇

This amplifier uses the composite sync CSYNC(H) signal (a combination of the vertical drive VDRIVE(H) and horizontal drive HDRIVE(L) signals) and the VIDEO(H) signal to produce a composite video output. This non-interlaced composite video output signal (RS170-compatible) is used to drive an external monitor or video hard copy unit.

The Display Board's VIDEO(H) and CSYNC(H) signals are combined in A10Q471. Transistor A10Q472 provides level shifting for RS170-compatible output capability.

TRIG IN LEVEL SHIFT AND BUFFER ◇3◇

This level-shifting buffer accepts TTL-level trigger in signals from the rear panel TRIG IN BNC connector and converts them to buffered, ECL-level signals. The trigger in signal is used to externally trigger or enable the 1240.

Transistor A10Q373 acts as a buffer for the trigger in signal, supplying the needed current drive for transmission to the Trigger Board. A10Q271, Q371, and Q372 are TTL- to ECL- level shifting components. If a X10 attenuation trigger input probe is used at the rear panel, the probe connector contacts the outer ring of the TRIG IN BNC. This activates the threshold switch comprised of A10Q473 and Q571, effectively reducing the base drive to A10Q371 by a factor of 10.

TRIG OUT LEVEL SHIFT AND BUFFER ◇3◇

This level-shifting buffer accepts ECL-level trigger out signals from the Trigger Board and converts them to buffered, TTL-level signals available at the rear panel TRIG OUT BNC. The latched or pulsing trigger out signal to the Trigger Board is useful in triggering or enabling other external instruments.

A10Q461 and Q462 act together as a differential comparator. Components A10Q562 and A10CR561 control saturation of the comparator to maintain fast switching rates. A100Q561 supplies the necessary pull down for the TTL-level output at the rear panel TRIG OUT BNC.

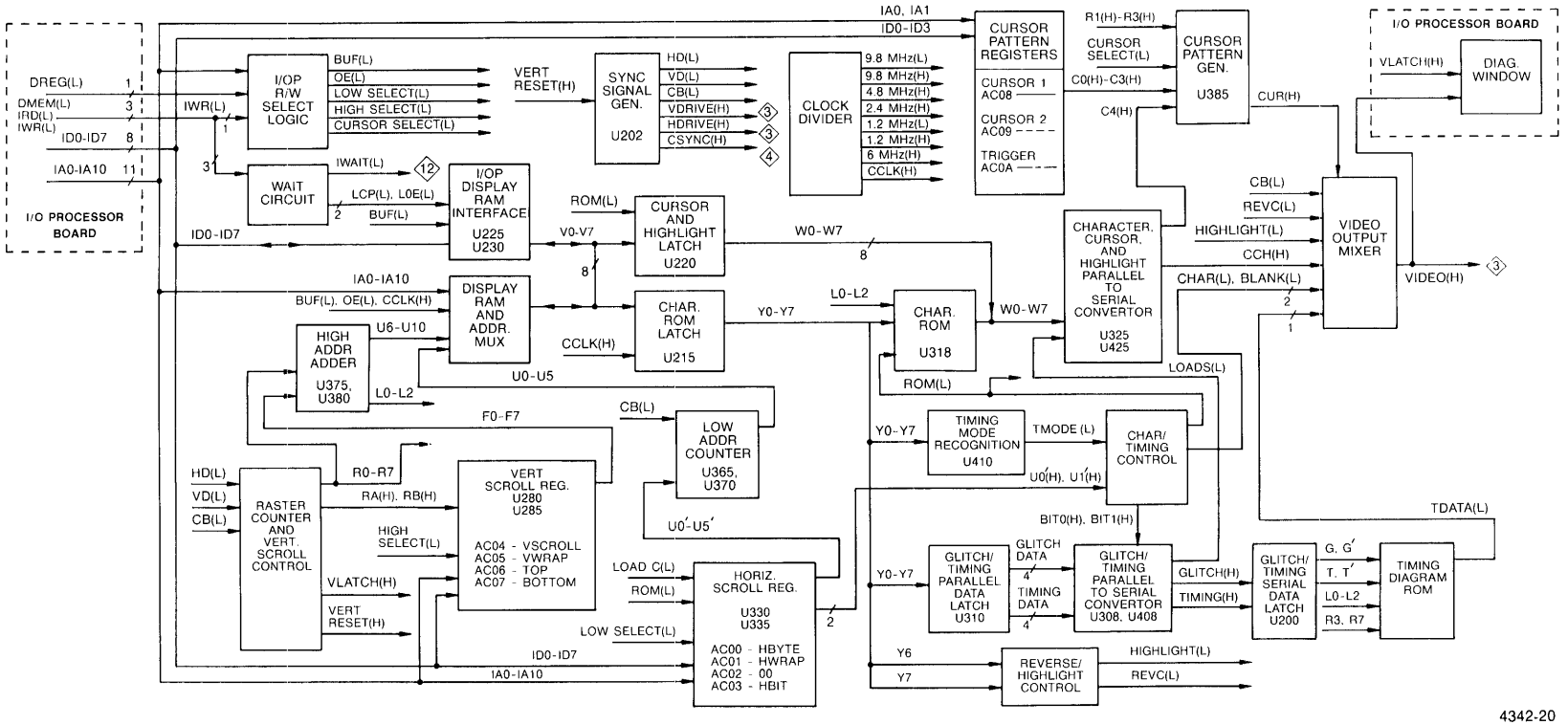


Figure 4-7. Display Board functional block diagram.

DISPLAY BOARD THEORY

OVERVIEW

The Display Board contains circuitry that performs the following functions:

- positions characters and timing diagrams on the display screen
- controls vertical smooth scrolling
- controls horizontal smooth scrolling
- controls reverse video and highlighting for characters
- produces three intensified timing diagram cursors

The display circuitry produces three types of display screens: basic text, text and a state table (with state table vertical scrolling), and text and a timing diagram (with timing diagram horizontal scrolling). For ease of discussion, the functional blocks necessary to produce a basic text display are described first under *Circuitry For Basic Display Operations*. State table vertical scrolling and timing diagram horizontal scrolling operations are supplemental to the production of basic text displays and are therefore described last under *Circuitry For Vertical (or Horizontal) Scrolling Operations*. Figure 4-8 illustrates the 1240 display screen.

The display board theory of operation discussion is limited to display circuitry, even though some trigger circuitry resides on the Display Board. Trigger circuitry is discussed in *Trigger Board Theory*.

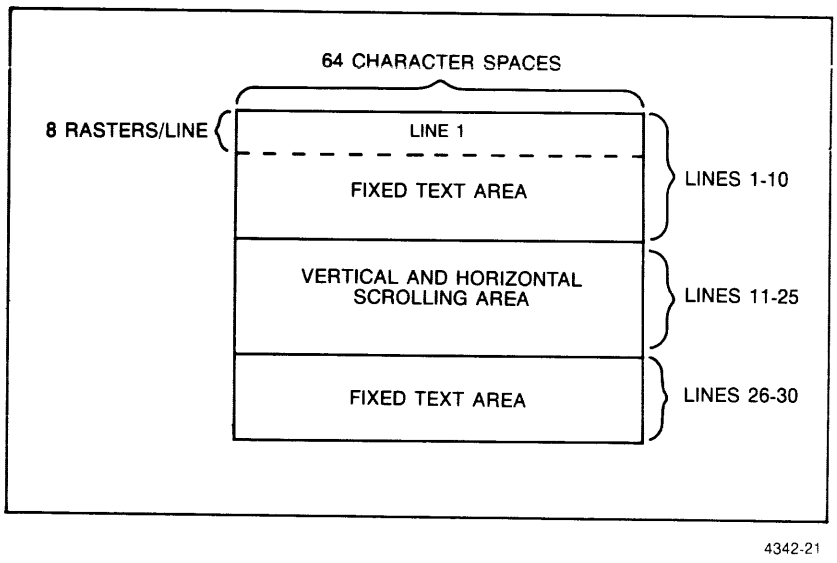


Figure 4-8. 1240 display screen.

CIRCUITRY FOR BASIC DISPLAY OPERATIONS

CLOCK DIVIDER <17>

A 19.6 MHz crystal oscillator provides a basic clock frequency that is divided into the following Display Board clock rates: 9.8 MHz(H) and (L), 4.8 MHz(H), 2.4 MHz(H), 1.2 MHz(H), and .6 MHz(H).

I/OP R/W SELECT LOGIC <25>

This select logic generates control signals for several operations. BUF(L), OE(L), LOE(L), and LCP(H) control data transmission for the Display RAM A11U238 and the I/O Processor-Display RAM Interface when the I/O Processor writes to or reads from the RAM. HIGH SELECT(L) and LOW SELECT(L) enable the Vertical Scrolling Registers and the Horizontal Scrolling Registers, respectively, that produce Display RAM addresses. CURSOR SELECT(L) selects the Cursor Pattern Generator Register A11U290.

WAIT CIRCUIT <17>

The Wait Circuit monitors the I/O Processor's IRD(L) read signal, IWR(L) write signal, and DMEM(L) display memory signals in combination with the Display Board's 1.2 MHz clock to determine when the I/O Processor should access the Display RAM. (For more information on accessing Display RAM, refer to *Display RAM and Address Multiplexing.*) The circuit produces LCP(L) and LOE(L) to control the I/OP-Display RAM Interface. It also generates the IWAIT(L) signal to the I/O Processor's Z80, which forces it to wait for its appropriate access time.

I/OP-DISPLAY RAM INTERFACE <15>

The interface, formed by A11U225 and U230, provides a communication link between the I/O Processor's ID data bus and the Display RAM's V data bus. The I/O Processor uses this link when transferring a screen image to the Display RAM, A11U238. The interface is also used during diagnostics when the I/O Processor reads back data from the Display RAM.

SYNC SIGNAL GENERATION <16>

Latch A11U208 holds the synchronization control states determined by the sync signal generator, A11U202. This generator, reset by VERT RESET(L) after raster 240, outputs control signals that synchronize raster counter operations on the Display Board and display monitor operations on the CRT Drive Board.

RASTER COUNTER AND VERTICAL SCROLLING CONTROL <15>

The raster counter tracks the output of raster lines for the display screen (240 raster lines per screen). The CB(L) composite blank signal clocks the dual 4-bit counter A11U195 that outputs the R0(H)-R7(H) raster count. The High Address Adder forms Display RAM upper addresses from 1) the current raster line count from this circuit, and 2) any offset value held in the Vertical Scrolling Register. These addresses specify the portion of Display RAM to be output.

When the video beam retraces to the top, upper-left corner of the screen, the raster counter is zeroed by VB(L). The VB(L) signal becomes the BLANK(L) signal in the Character/Timing Control circuit, causing a blank space to be output when active low. For each raster sweep across the screen, this counter is incremented. Eight raster scans produce one character line (because each letter is formed by an eight-by-eight dot matrix). The raster counter generates two signals, RB(H) and RA(H), to indicate raster scan 80 and 200 (lines 10 and 25 respectively). These lines mark the boundary of the vertical and horizontal scrolling regions. At raster 240, vertical retrace occurs and VB(L) once again resets the raster counter for the next screen display.

The VLATCH(H) signal to the I/O Processor is used during diagnostics when the I/O Processor reads back from the diagnostic window, A10U190 and U295.

HIGH ADDRESS ADDER ⟨15⟩

This adder, formed by A11U375 and 380, combines any offset value latched by the Vertical Scrolling Register with the current raster count. The sum of the two values forms an eight-bit word. The upper five bits, U6-U10, are the Display RAM's A6-A10 address bits that define one of 32 blocks in the Display RAM (see Figure 4-9) to be output. The lower three bits, L0-L2, indicate which of the eight raster rows is to be output by the Character ROM.

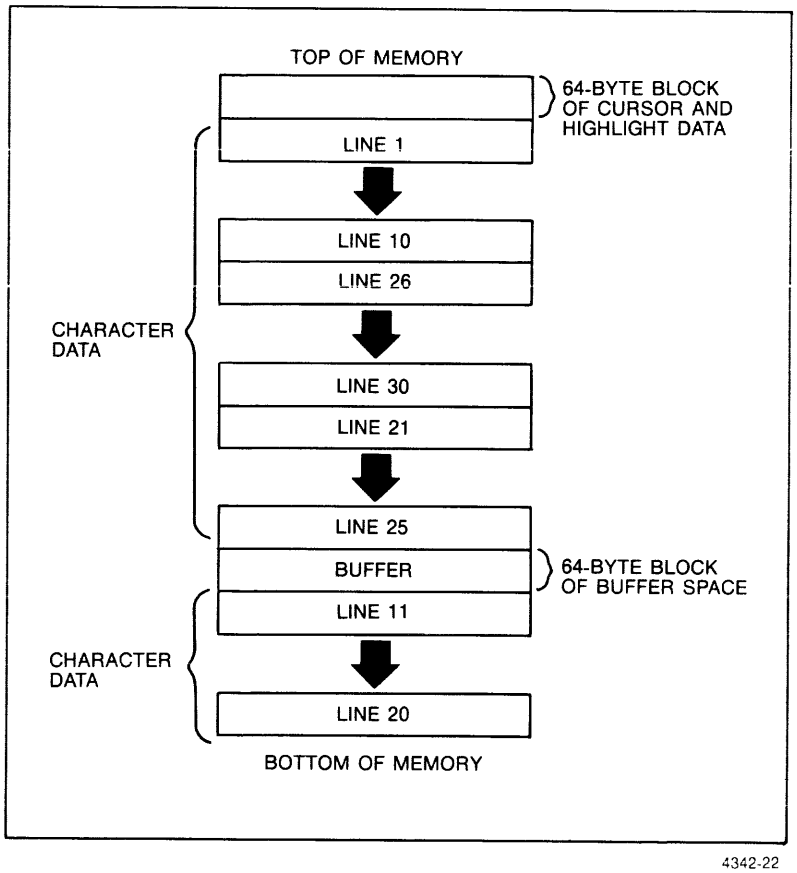


Figure 4-9. Display RAM memory map.

LOW ADDRESS COUNTER ◈15◈

This counter, formed by A11U365 and U370, outputs a count pattern on the lower six address lines to the Display RAM during normal text displays. During horizontal scrolling, the counter is loaded with an offset value obtained from the Horizontal Scrolling Registers. That value becomes the new address information pointing to Display RAM's horizontal scrolling data.

DISPLAY RAM AND ADDRESS MULTIPLEXING ◈15◈

The Display RAM, A11U238, is a 2K X 8-bit, 6116-type RAM. This RAM provides temporary storage of four types of data: character data, timing/glitch data, timing mode highlighting data, and timing mode cursor position data. Each of the 30 screen lines can be related to one 64-byte block of Display RAM memory (refer to Figure 4-9). The two remaining 64-byte blocks are used during scrolling operations and cursor/highlighting operations.

Display RAM accessing occurs according to an 800 ns-per-character cycle time (refer to Figure 4-10.) During the first 400 ns, the address multiplexers A11U265, U270, and U275 allow the I/O Processor to address the Display RAM on address lines A0-A10. The RAM then stores screen display data sent from the I/O Processor through the I/OP-Display RAM Interface. The remaining 400 ns of the cycle is split into two halves. During the second 400 ns of the cycle, the address multiplexers pass the adresses formed by the Low Address Counters and the High Address Adder. The first 200 ns period is used to output character or timing/glitch data sent from the Display RAM. The data is latched by A11U215 on the rising edge of CCLK(H). The second 200 ns period is used to output cursor position and highlight data and is latched by the falling edge of CCLK(H) (actually 1.2MHZ(L)'s rising edge).

Jumper A11J275, when put in the TEST position (pins 2 and 3 shorted), causes the address multiplexer to lock out I/O Processor addresses. This allows only the addresses from the Low Address Counter and the High Address Adder to pass. The address count may be used when troubleshooting the display circuitry, because only one set of addresses is being passed.

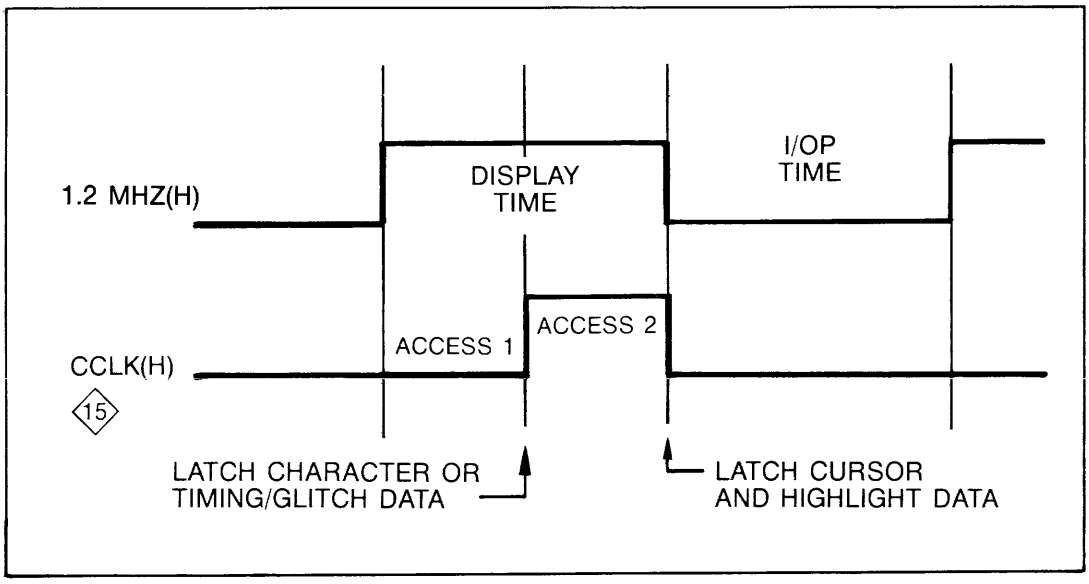


Figure 4-10. Display memory access times.

CHARACTER ROM AND LATCH 

The Character ROM, A11U318, is a 2K X 8-bit, 2716-type EPROM containing two 64-character sets of text characters. The two character sets provide a total of 128 possible display characters. (The timing diagram characters are generated by the Timing Diagram ROM.) The Character ROM decodes an FF data value as a blank character, output at the beginning of timing diagram waveforms. This special character code causes the display to enter the Timing Diagram mode of operation.

CHARACTER, CURSOR, AND HIGHLIGHT PARALLEL-TO-SERIAL CONVERTOR 

This parallel-in/serial-out shift register, A11U425, accepts text data from the Character ROM or cursor/highlight data directly from the Display RAM. This parallel data is then converted into a serial stream of data that is clocked by 9.8 MHz. When generating timing diagram displays, the timing of LOADS(L) is changed to accomplish horizontal scrolling (described in *Character/Timing Control II*).

CHARACTER/TIMING CONTROL I 

This circuitry outputs various control signals used by the Video Output Mixer when producing screen displays. TCL(H) and TCL(L) are used when producing timing diagram displays. BIT0(H) and BIT1(H) control the timing of the LOADS(L) signal (in the *Character, Cursor, and Highlight Parallel-to-Serial Convertor*) which causes a character to be loaded into the CCH Parallel-to-Serial Convertor A11U425.

An eight-input NAND gate, A11U410, decodes an FF condition on the Character ROM's data bus as the active low TMODE(L) timing mode signal. During this time, the Timing Diagram ROM outputs timing diagram waveforms. The ROM(L) signal to the Character ROM A11U318 disables the ROM during the timing diagram mode, allowing the cursor and highlight data from the Display RAM to be passed. The CHAR(L) signal, produced from ROM(L), switches Video Mixer circuitry between the character and timing diagram modes.

REVERSE/HIGHLIGHT CONTROL 

This circuitry determines character video attributes for the Video Output Mixer. Bits 6 and 7 from the latched Character ROM data bus are used to determine if the output character is to be normal video, reverse video (dark characters on a light background), or highlighted video (light characters on a shaded background). The 11 (one-one) combination of bits 6 and 7 is also used to control an upper address line to the Character ROM. The A9 address line to the Character ROM forces the character that is output to have the same attribute as the previously output character (copycat), but to be from the second set of characters within the ROM. The following Table 4-1 summarizes the four possible states.

Table 4-1
POWER-UP ERROR CONDITIONS

BIT 7 STATE	BIT 6 STATE	CHARACTER ATTRIBUTE
0	0	standard (use set 1)
0	1	highlighted (use set 1)
1	0	reverse (use set 1)
1	1	keep previous attribute (use set 2)

VIDEO OUTPUT MIXER ◇17◇

The Video Output Mixer combines the character, cursor, and timing diagram information with the appropriate type of video pattern. The resulting VIDEO(H) signal is sent to the CRT Z-Axis Amplifier on the CRT Drive Board.

The VIDEO(H) signal is also input to the I/O Processor's Video Readback (Diagnostic Window) circuitry. Diagnostics uses the screen readback circuitry to check a portion of the displayed video and verify that it is correct.

Jumper A11J155, when put in the TEST position (pins 2 and 3 shorted), applies a .6 MHz square wave video signal to the CRT's Z-Axis amplifier. The resulting pattern (jailbars) is useful when troubleshooting the CRT Drive Board.

CIRCUITRY FOR VERTICAL SCROLLING OPERATIONS

OVERVIEW

During basic text displays, the Display RAM's upper five address bits determine which of the 30 character lines are being output. The information on lines 11-25 may be shifted up or down by controlling the Display RAM addresses, thereby producing the vertical scrolling action. Only 30 of the 32 Display RAM memory blocks are used to store screen character data. One of the additional memory blocks is used as a buffer to hold the character row bits of off-screen characters (refer to Figure 4-8).

VERTICAL SCROLLING REGISTERS ◇15◇

The Vertical Scrolling Registers, A11U285 and U280, contain an offset value that is used to determine the portion of Display RAM to be read for vertical scrolling data. This offset value, sent by the I/O Processor, is used by the High Address Adder to calculate the Display RAM's upper five address bits.

CIRCUITRY FOR HORIZONTAL SCROLLING OPERATIONS

OVERVIEW

During basic text displays, the Display RAM's lower six bits determine which of the 64 characters in the screen line is being output. The information on lines 11-25 may be shifted left or right by controlling the time when the horizontal bit information is output, thereby producing the horizontal scrolling action. Horizontal scrolling is only possible for the timing diagram displays (the Character ROM is disabled). The Timing Diagram ROM uses the Display RAM data to form timing diagram waveforms.

HORIZONTAL SCROLLING REGISTERS ◇15◇

The Horizontal Scrolling Registers contain an offset value that is used to determine the portion of Display RAM to be read for horizontal scrolling data. This offset value, sent by the I/O Processor, is used by the Low Address Counter to form the Display RAM's lower six address bits.

CHARACTER/TIMING CONTROL II ◈16◈

When timing diagrams are to be generated, the I/O Processor outputs an FF data value to indicate a change to the timing display mode. The FF data value is decoded by the NAND gate A11U410 as the active TMODE(L) timing diagram mode signal. Two blank character positions are automatically inserted when TMODE(L) is asserted. The active TMODE(L) signal also initiates horizontal scrolling by causing an offset value to be loaded into the Low Address Counters.

Signals BIT0(H) and BIT1(H) control the timing of the LOADS(L) signal. During basic text displays, the LOADS(L) signal clocks the CCH Parallel-to-Serial Convertor at a rate that allows whole characters to be output. During the generation of timing diagram displays, the time at which the first character column bits are displayed may be changed by manipulation (short cycling) of the LOADS(L) signal. This effectively allows only the beginning or end columns of data to be output, thereby creating partially off-screen characters.

HIGHLIGHT AND CURSOR LATCH ◈16◈

This latch, A11U220, provides a bypass around the Character ROM for timing diagram cursor highlight and cursor position data from the Display RAM. Data to the Timing Diagram ROM is used during the generation of timing diagram displays. The lower four bits of the data word contain highlight data, while the upper four bits contain cursor position data. The ROM(L) signal enables latch A11U220 and disables the Character ROM when the NAND gate A11U410 decodes an FF condition on the data bus. The data then passes to the CCH Parallel-to-Serial Convertor.

GLITCH/TIMING PARALLEL-TO-SERIAL CONVERTOR ◈16◈

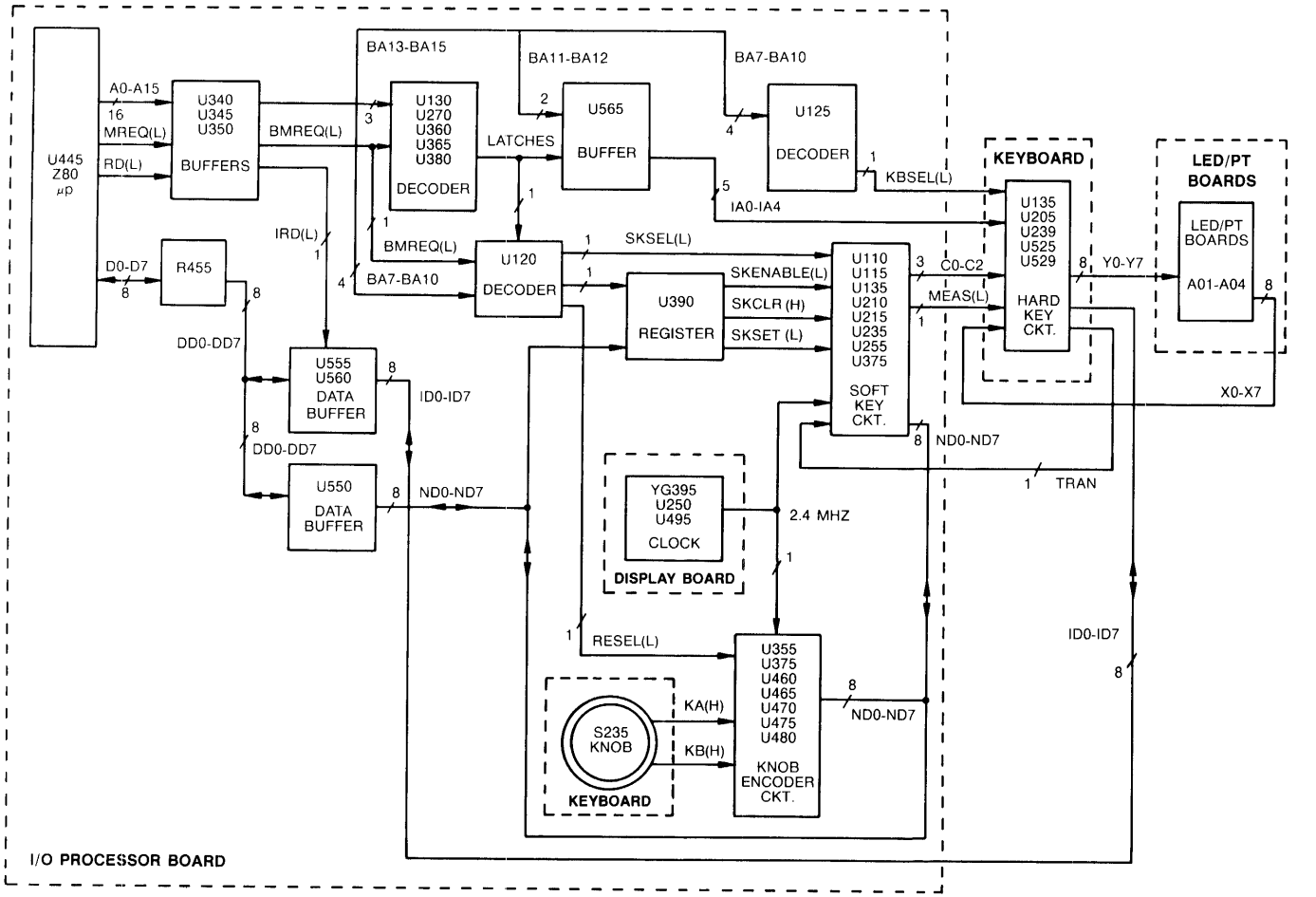
The parallel data latch A11U310 latches the data on Y0-Y3 as glitch data and Y4-Y7 as timing data. This parallel data is converted into two serial streams of data on the GLITCH(H) and TIMING(H) signal lines.

TIMING DIAGRAM ROM AND LATCH ◈17◈

The Timing Diagram ROM, A11U205, uses glitch and timing serial data in conjunction with the raster row information on L0(H)-L2(H) to determine the data to be output. A11U200 latches the serial data for the Timing Diagram ROM. The ROM outputs data that forms timing diagram rising and falling edges, top and bottom bars, and wide rising and falling edges (for glitches). Tick marks are generated when the GATE(L) signal blanks out the top and bottom bars, leaving only rising and falling edges.

CURSOR PATTERN GENERATOR AND REGISTERS ◈16◈

The attributes of the three cursor patterns are latched in the Cursor Pattern Registers A11U260D, U485A, and U290. The data on C0(H)-C3(H) provides cursor physical attribute information (e.g., a dash, dot-dash, or solid line cursor). The C4(H) signal provides cursor positioning information. The Cursor Pattern Generator, A11U385, uses the position information, along with the raster row information on R0(H)-R3(H), to form timing diagram cursors.



4342-24

Figure 4-11. LED/PT and Keyboard functional block diagram.

LED1, LED2, PT1, AND PT2 BOARDS THEORY

SOFT KEY LED/PHOTOTRANSISTOR MATRIX ◇1◇

The LED/PT (phototransistor) boards are arranged around the perimeter of the 1240 display screen. These LEDs and PTs form a light-beam matrix on the surface of the screen. The intersection of the light beams define a specific area on the screen (soft key boxes). When the user interrupts the light beam path, a specific soft key is activated.

The LEDs output infrared light beams as they are sequentially scanned. A phototransistor (one associated with each LED) receives the light beam through a plastic light filter that only passes infrared light. As each PT is sequentially turned on, it outputs a pulse to the keyboard. The keyboard's analog multiplexer, A05U205, sequentially scans the phototransistors and sends this information as a serial data stream to the I/O Processor's soft key circuitry.

KEYBOARD THEORY

HARD KEYS ◇2◇

The hard keyboard holds 33 front panel push-button keys. The keys (grouped on the front panel by function, e.g., EXECUTE, CURSOR, or MENU) are scanned by five column-address lines from the buffer A05U135 and eight row data lines. The column address lines A0-A4 are sequentially taken to a low logic level. Pressing any hard key causes the low to be coupled through to the Keyboard Readback register A05U239.

KEYBOARD READBACK ◇2◇

The register A05U239 provides a latch for the logic levels present on eight rows of keyboard keys. The I/O Processor reads the status of lines ID0-ID7 to determine which front panel key is pressed.

MENU KEY LEDS ◇2◇

The Menu Key LEDs indicate the current menu the user has displayed. The I/O Processor uses keyboard readback information to determine which menu-key LED to illuminate. A low logic level output by the I/O Processor on one of the ID0-ID5 lines is latched by A05U338. The logic low turns on a menu key LED.

SOFT KEY LED SELECTION ◇2◇

Decoder A05U529 uses control lines C0(H)-C2(H) and the 2.3 KHz MEAS(L) signal to produce a 0.43 msec, one-half duty-cycle sample time on each Y1-Y7 infrared LED line. Each sample sequentially turns on a soft key LED to be read by a corresponding phototransistor. The seven LED sample intervals plus one false sample (induced by A11U205 pin 4) set the approximate 4 msec total scan rate.

PHOTOTRANSISTOR 60 HZ FILTERS AND MULTIPLEXING ◇2◇

Multiplexer A05U205 accepts the softkey LED pulses produced by the seven LED/Phototransistor pairs on lines X1(H)-X7(H). Circuitry on each of the X1-X7 phototransistor lines acts as a 60 Hz high-pass filter, necessary to prevent external light sources from affecting the I/O Processor's Soft Key Circuitry. The multiplexed information on TRAN(H) is used by the I/O Processor's Soft Key Circuitry to determine when a soft key is activated.

FRONT PANEL KNOB ◇2◇

The infinite-turn rotary encoder, A05S235, outputs a two-bit Gray code. Each bit, output on KA(H) and KB(H), produces 200 pulses for every one knob revolution. The Gray code is used to determine the amount and direction the knob is turned.

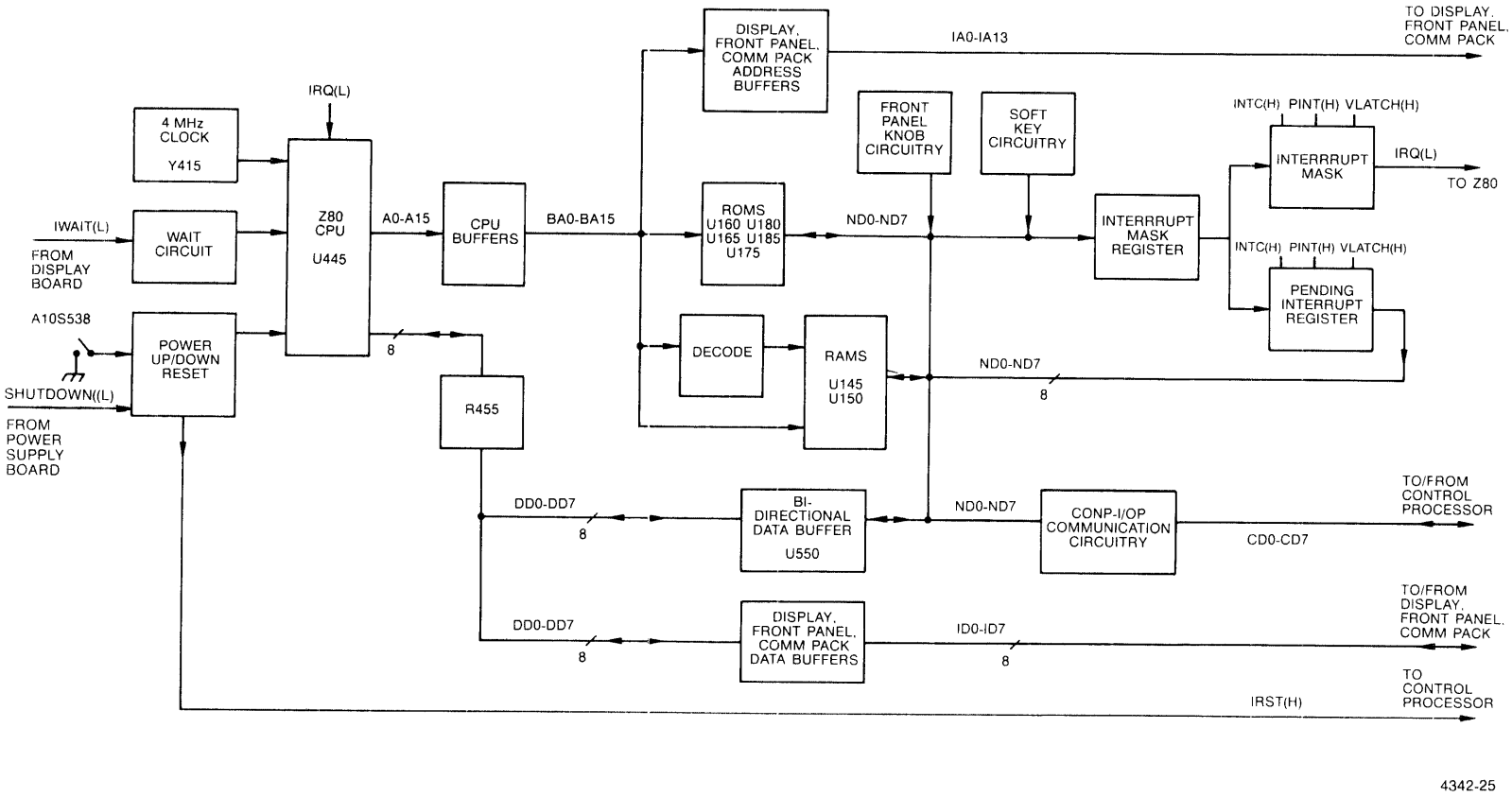


Figure 4-12. I/O Processor Board functional block diagram.

I/O PROCESSOR BOARD THEORY

OVERVIEW

The Z80 Central Processing Unit (CPU), A10U445, is the controlling part of the I/O Processor Board. This microprocessor handles the following operations:

- COMM pack communications
- front panel (hard or soft key) communications
- display updating
- instrument interrupts

CPU CLOCK ◈12◈

The crystal, A10Y415, supplies a 4 MHz, TTL-level clock signal to the Z80. Pull up transistor A10Q328 shapes the rising edge, while A10U225D shapes the falling edge of the clock. The edge-shaping circuitry forms a fast rising and falling edge clock signal.

POWER UP/DOWN RESET ◈12◈

The Power Up/Down Reset circuitry provides reset signals for both the I/O and Control Processors, and the COMM pack. On power-up, the capacitor A10C434 charges slowly so that A10Q426 is turned on with +5 volts on the emitter. This puts current into the base of A10Q424, producing a low to the Z80 at the RESET(L) input. On power-down, the charged capacitor A10C434, combined with the the decreasing +5 volt supply on the base of A10Q438, turns on Q438. This transistor now supplies the current to the base of A10Q424, producing the RESET(L) signal.

A manual reset of the processors may be accomplished with A10S538. Pressing this reset switch (located on the I/O Processor Board) discharges capacitor A10C434 and turns on A10Q426, effectively causing a power-up reset to occur.

Transistor A10Q425 inverts the RESET(L) signal, producing the active high reset signal IRST(H) for the Control Processor and the positive feedback to the base of A10Q424.

Z80 CPU AND BUFFERS ◈12◈

The Z80 CPU uses buffers A10U340, U345, and U350 to help in driving the address and control lines to other circuits. After buffering, these signal lines are preceded by the letter B to indicate the buffering action. The functions of the various microprocessor pins are described in the following microprocessor glossary:

Address Bus. The 16-bit address bus provides the addresses for memory and I/O data transfers.

Data Bus. The 8-bit, bidirectional data bus is used for data transfers with memory, the Control Processor, and any installed COMM pack.

M1(L). This output goes active when the microprocessor is in the opcode fetch cycle of an instruction execution.

RD(L). This output goes active when the microprocessor is ready to receive data on the bidirectional data bus from the currently addressed device.

WR(L). This output goes active when the microprocessor is writing data on the bidirectional data bus to the currently addressed device.

MREQ(L). This output goes active to indicate that the address bus holds a valid address for a memory-read or memory-write operation.

WAIT(L). This input goes active to signal the microprocesor to continue execution of the current instruction until the input is returned inactive.

IRQ(L). This input is made active to request an interrupt to the microprocessor. The request is honored at the end of the instruction currently being executed. Possible interrupt sources are: COMM Packs - INTC(H), Control Processor - PINT(H), and Display Board - VLATCH(H).

RESET(L). This input is made active to force the microprocessor to re-initialize. While RESET(L) is active, the address and data buses go to a high-impedance state, and all output control lines go inactive.

WAIT CIRCUIT 

The Wait Circuit has two functions. First, the circuit adds a wait state to the Z80 M1 bus cycle, providing extra time for accessing system ROMs. (Refer to Figure 4-13.) It does this by adding one cycle at the beginning of execution for each opcode fetch instruction cycle. For every opcode fetch cycle, the Z80's M1(L) output goes low. A10U230B monitors this input and, with its Q(L) output combined with A10U230A's Q output in A10U225C, the WAIT(L) input to the Z80 is pulled low for one clock cycle.

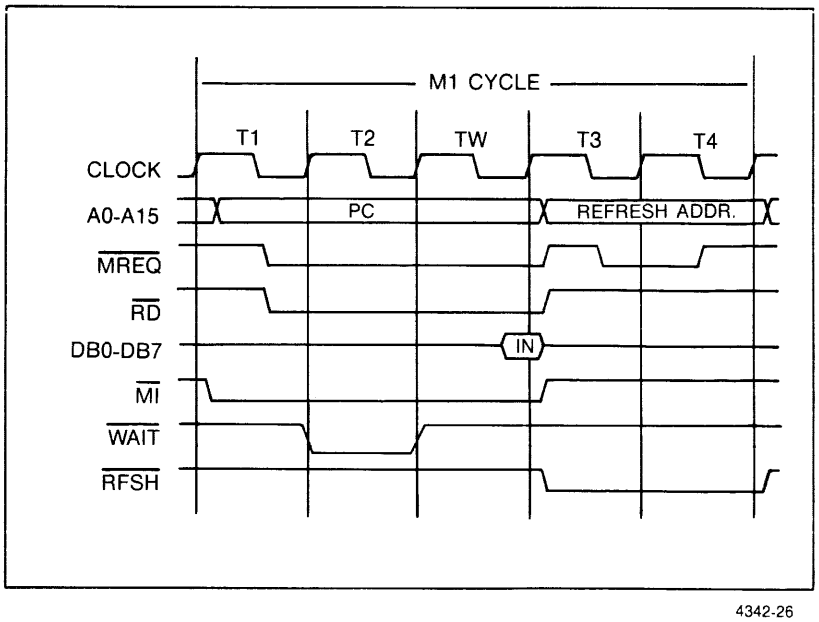


Figure 4-13. Instruction opcode fetch with wait states.

Second, the Wait Circuit prevents the Z80 from accessing the display memory while the Display Board is accessing it. The IWAIT(L) signal from the Display Board tells the Z80 to wait until the memory is free to be accessed. When the Display Board releases the IWAIT(L) signal high, the Z80 is allowed to complete the display memory access.

DECODE CIRCUITRY ◈12◈

The Decode Circuitry uses the Z80 address and control lines to produce the following control signals:

- Z80 ROM enable signals
- Z80 RAM select signals - RAM 1(L) and RAM 2(L)
- bidirectional data buffer direction control signal - IO(H)
- display memory select signal - DMEM(L)
- COMM pack ROM select signal - CROM(L)
- various registers' select signals

ROMS ◈12◈

The 40K of ROM space is provided by five 2764-type 8K x 8-bit ROMs. These ROMs contain the firmware that drives the front panel and display operations. Diagnostic code residing in ROM 1, A10U160, is used by the Z80 at power-up to check I/O Processor kernel circuitry.

The I/O Processor memory address assignments are as follows:

ADDRESS	DEFINITION
0000-1FFF	ROM 1, A10U160
2000-3FFF	ROM 2, A10U165
4000-5FFF	ROM 3, A10U170
6000-7FFF	ROM 4, A10U180
8000-9FFF	ROM 5, A10U185
A000-A7FF	display memory
A800-A87F	interrupt mask reg., video readback control
A880-A8FF	pending interrupt reg., queue status
A900-A97F	Control Processor communication
A980-A9FF	diagnostic LEDs and buzzer
AA00-AA7F	video readback
AA80-AAFF	rotary knob position
AB00-AB7F	soft keys
AB80-ABFF	data bus test
AC00-AC7F	display registers
AC80-ACFF	keyboard
AD00-AD7F	front panel LEDs
AD80-ADFF	clear 60 Hz interrupt
AE00-AE7F	CONP-I/OP communication queue clear
AE80-AEFF	COMM pack chip select
AF00-AF7F	not used
AF80-AFFF	not used
B000-B7FF	RAM 1, A10U150
B800-BFFF	RAM 2, A10U145
C000-FFFF	COMM pack ROM select

RAM ◇12◇

The 4K of RAM space is provided by two 6116 type 2K X 8-bit static RAMs. The RAMs provide read/write memory space for storage of volatile information. The RAM address assignments are as follows:

ADDRESS	DEFINITION
B000-B7FF	RAM 1, A10U150
B800-BFFF	RAM 2, A10U145

FRONT PANEL, COMM PACK, AND DISPLAY ADDRESS BUFFERS ◇12◇

Buffers A10U565 and U570 help in driving the 14 address lines BA0-BA13 used by the front panel, the COMM pack, and the Display Board. After buffering, the address lines are preceded by the letter I (IA0-IA13), indicating the I/O buffering action.

FRONT PANEL, COMM PACK, AND DISPLAY DATA BUFFERS ◇12◇

The Z80 microprocessor transfers data to/from the front panel, the COMM pack, and the Display Board on the 8-bit, bidirectional data bus ID0-ID7. During normal write cycles, A10U555 provides data latching so that slower receivers such as the COMM pack will have valid data for a longer period of time. The Z80 reads back data from the ID bus through the buffer A10U560.

The TEST(L) signal is used during diagnostics to check the ability of the Z80 to write a value out to the board edge connector and correctly read it back. The TEST(L) signal, decoded on address AB80H (the diagnostic data bus test), forces the latch A10U555 output to be enabled so that data previously written to this latch can be read back.

BIDIRECTIONAL DATA BUFFER ◇13◇

The bidirectional data buffer, A10U550, provides the communication link between the Z80's DD data bus and other I/O Processor functional blocks operating on the ND data bus. The following list shows some of the functions performed using this bus:

- RAM communication
- video readback for diagnostics
- data retrieval from the CONP-I/OP communication circuitry
- reporting of diagnostic LED status information
- interrupt masking
- interrupt readback
- soft key readback
- front panel knob readback

CONP-I/OP COMMUNICATION CIRCUITRY ◇13◇

The Control and I/O Processors communicate through two asynchronous data buffers. The Control Processor puts data into a 64-byte queue and the I/O Processor reads it out. The I/O Processor, however, puts data into a four-register queue for the Control Processor to read out (refer to Figure 4-14). Independent communication queues ensure that there is no contention for the inter-processor communication circuitry.

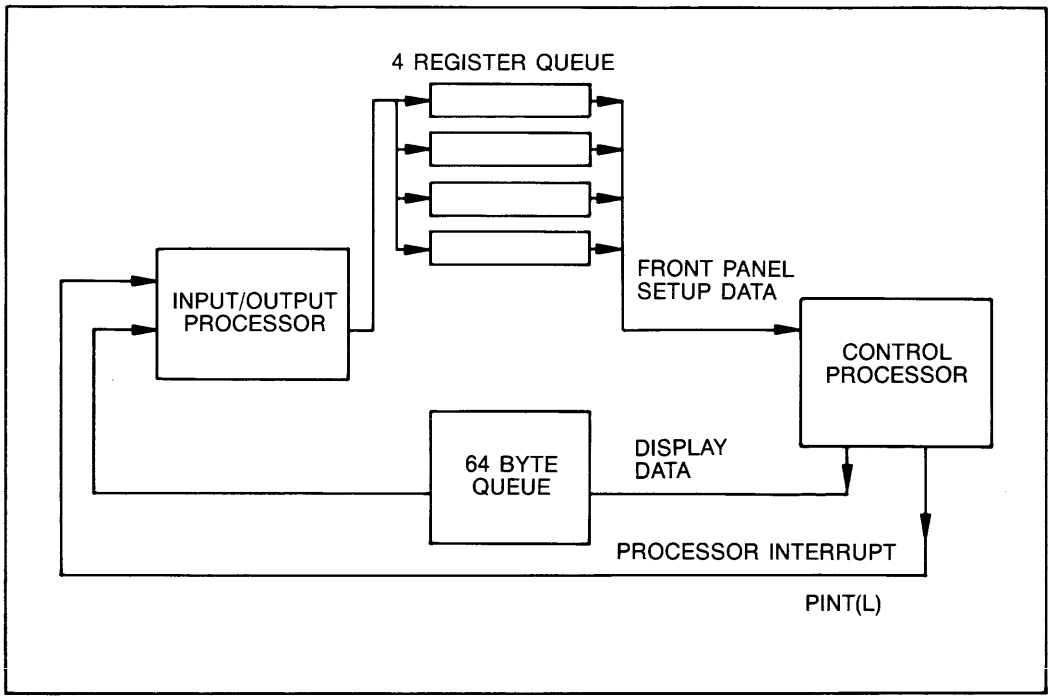


Figure 4-14. Inter-processor communication path.

The Control Processor sends data over its CD data bus to the 64-byte queue consisting of A10U580 and U585. If the Control Processor wishes to transfer display data to the I/O Processor, it activates the PINT(H) interrupt signal. Unless masked, the I/O Processor receives this interrupt on the IRQ(L) line. The Control Processor strobes in the data with PSEL(L) and CWR(L). The I/O Processor reads the condition of a bit (on A10U580 pin 14) through A10U490 to determine if there is data in the queue. When the I/O Processor is ready to read the data, it strobes the queue with the IRD(L) signal (actually IRD(L) ANDed with a select line). Also at this time, the strobe signal enables this data through the queue buffer A10U485 onto the I/O Processor's ND data bus.

The I/O Processor transfers data that describes instrument setup changes (made from the front panel) and handshaking of data from the Control Processor through the four-register queue consisting of A10U590 and U595. The I/O Processor writes data into these registers with the IWR(L) signal (actually IWR(L) ANDed with a select line). When the Control Processor is ready to read the data over its CD data bus, it gates the data out of the queue with the CRD(L) and PSEL(L) signals.

INTERRUPT MASK REGISTER ◇13◇

The Interrupt Mask Register, A10U390A, allows the I/O Processor to individually enable or disable any of the three available interrupt sources: COMM pack INTC(H), Control Processor PINT(H), and 60 Hz retrace VLATCH(H).

The flip-flop, A10U385B, controls the 60 Hz interrupt, VLATCH(H). The 60 Hz interrupt is set when a screen retrace occurs. At this time, the interrupt signals the processor to update display information before the vertical retrace is finished. The interrupt is removed when the Z80 writes to address $FB00_{hex}$, resetting A10U385B. A10U385 uses the 60 Hz interrupt for a readback of the video information through the Diagnostic Window circuitry.

The INTC(H) interrupt, coming from any installed COMM pack, signals that communication with the instrument is necessary. The PINT(H) signal from the Control Processor requests an interrupt for inter-processor communication.

INTERRUPT GATING ◇13◇

The Interrupt Gate, A10U495, monitors the three available interrupt sources: INTC(H), PINT(H), and VLATCH(H). When any of these signals goes active high, the IRQ(L) line to the Z80 becomes active low. The interrupts are passed on to the I/O Processor only if they are not set to be masked by the Interrupt Mask Register A10U390A.

PENDING INTERRUPT BUFFER ◇13◇

A10U490 allows a processor readback of the current mask value and current interrupt status. The Z80 performs the readback over the ND data bus.

BUZZER AND DIAGNOSTIC LEDS ◇13◇

The buzzer and diagnostic LED information is latched from the ND data bus at address $A980_{hex}$ by the LED/buzzer latch A10U335. The buzzer provides an audible tone, indicating such events as menu changes, the touch of a soft key, and the occurrence of a trigger. The buzzer's frequency and duration is controlled by outputs from the latch A10U335. Bits 4, 5, and 6 determine the buzzer frequency, and bit 7 enables the buzzer. The frequency control outputs and associated resistors set the input voltage to the 555 timer A10U425, thereby determining the buzzer operating frequency. The jumper A10J315 provides a means of disabling the buzzer.

The diagnostic LEDs are used to track the progress of the I/O Processor power-up diagnostics. As the power-up routines progess, the LEDs indicate which test is currently being run. If, at any time, the I/O Processor fails power-up diagnostics, the lighted LEDs convey information useful in determining the problem area. (Complete LED error information is listed in the *Troubleshooting and Repair* section of this manual.) The diagnostic LEDs are controlled by bits 0 through 3 of the LED/buzzer latch A10U335. A low output turns on the associated LED, and a high output turns the LED off. Since the latch is reset upon power-up, all LEDs are turned on at power-up until the I/O Processor turns them off.

VIDEO READBACK (DIAGNOSTIC WINDOW) ◈13◈

The Video Readback circuitry is not used during normal 1240 operations. Diagnostic tests use this circuitry to check displayed video. The video readback circuitry is checked by alternately loading latch A10U190 from A10U295 with all zeros, then all ones, and checking for correct values during readback on the ND data bus. The diagnostics then used this circuitry to latch a portion of the displayed video and verify that it is correct.

SOFT KEY CIRCUITRY ◈14◈

The soft key circuitry converts the soft key information (detected by the LED/Phototransistor boards) into an equivalent binary code. This code is used by the I/O Processor to determine if a soft key has been activated.

The multiplexed signal TRAN(H) at A10TP312 from the Keyboard contains the status of seven phototransistors on the PT1 and PT2 phototransistor boards. This information is fed to the sample and hold circuit, A10U210. The sample and hold I.C. (clocked basically by the MEAS signal from counter A10U115) first samples the phototransistor ambient light output, then holds this level at its output. Next, the phototransistor is turned on. The two phototransistor readings are fed to the subtractor, A10U215C, to produce a high-going output pulse. If one of the soft keys was being touched, only ambient light output levels would be present for both inputs to the subtractor. The subtractor would therefore have no output pulse, indicating the activation of that soft key. Subtractor output pulses available at A10TP322 (refer to Figure 4-15) are integrated in A10U215B. The soft key adjustment, A10R320, controls the integrator input bias to set input sensitivity. An analog switch, A10U110, shorts out the integrating capacitor, A10C211, to restart the next integrating ramp at a zero-volt threshold. Comparator A10U215A shapes the ramp available at A10TP210 into a TTL-level pulse for the shift register A10U235. The seven states (plus one false state produced by the multiplexer A05U205 pin 4) describing the condition of each soft key box are clocked onto the ND data bus by SKSEL(L) through A10U135, latched on each occurrence of A10U115's carry out signal.

Signal lines SKCLR(L) and SKSET(L) are used only during diagnostic tests to verify the shift register and latch operation.

FRONT PANEL KNOB CIRCUITRY ◈14◈

The knob circuitry converts the rotational movement of the front panel rotary knob into an equivalent Gray code. This code is used by the I/O Processor firmware to determine incremental value changes corresponding to knob movement.

The front panel knob outputs a two-bit Gray code on the KA(H) and KB(H) lines. A10U460 and U375B produce the up (high signal)/down (low signal) count at A10TP375 and the clocking signal for every pulse edge at A10TP370. The four-bit up/down counters A10U470 and U475 decode the knob's clockwise movement as a count up and the counter-clockwise movement as a count down. This binary count is buffered onto the ND data bus by A10U480.

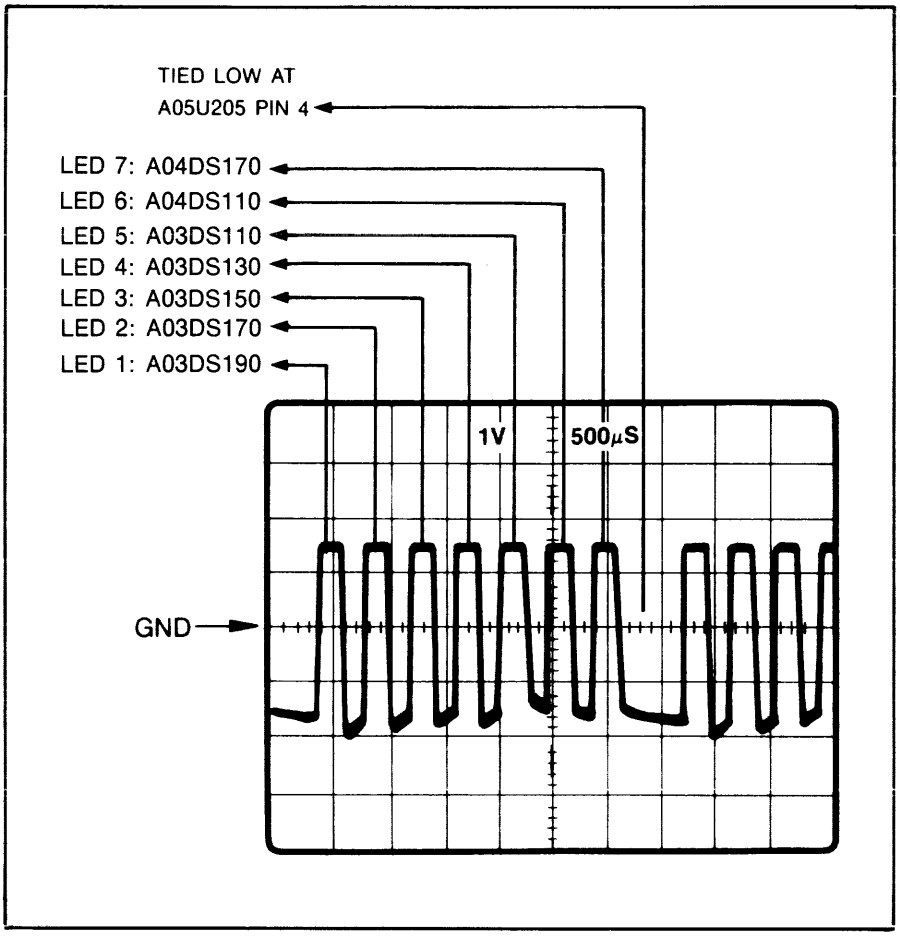


Figure 4-15. Data pulses corresponding to soft key boxes.

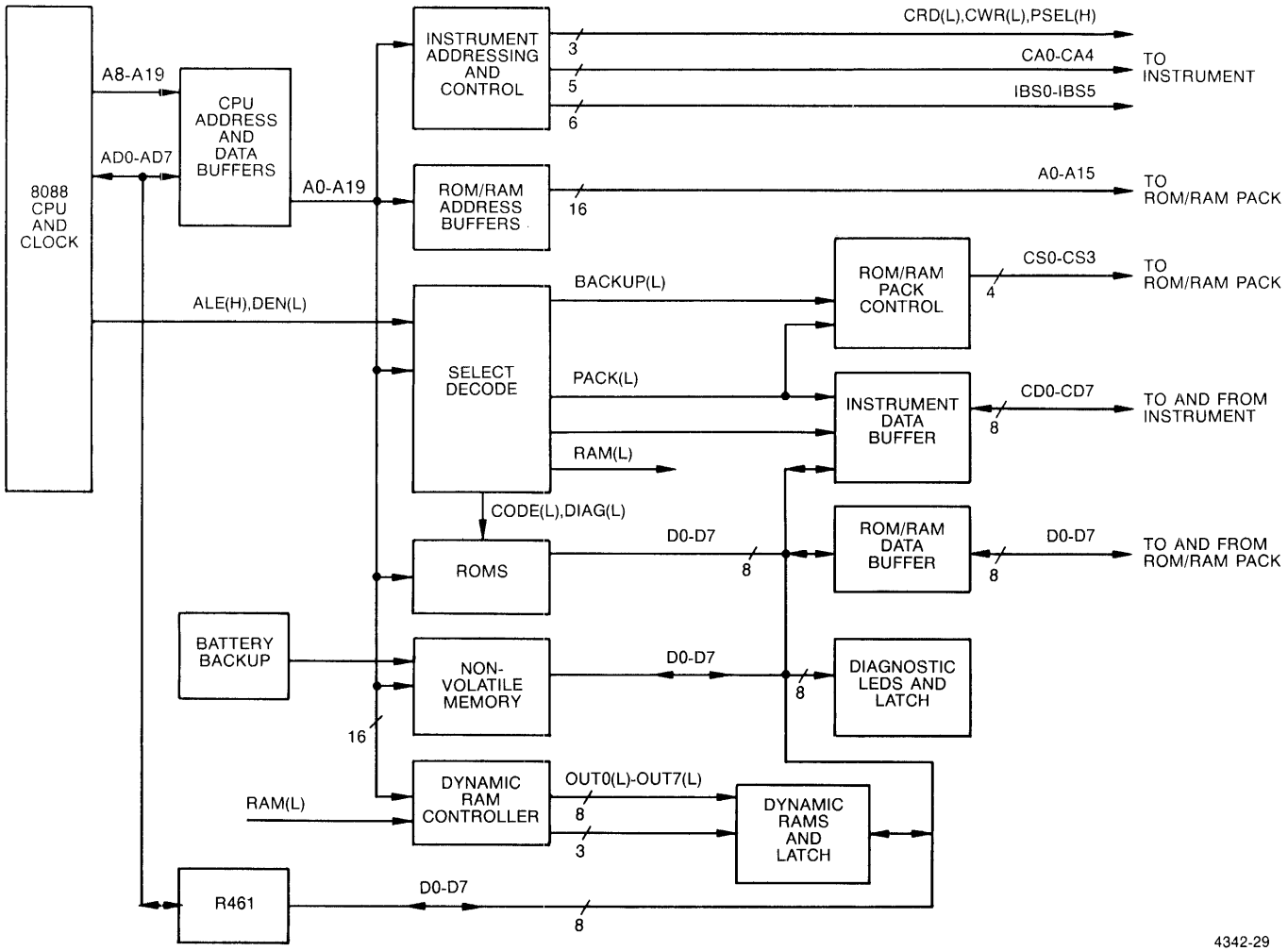


Figure 4-16. Control Processor functional block diagram.

CONTROL PROCESSOR BOARD THEORY

OVERVIEW

The 8088 Central Processing Unit (CPU), A9U347, is the controlling part of the Control Processor Board. This CPU runs the majority of the 1240 according to directions it receives from the user through the I/O Processor. The Control Processor performs the following tasks:

- controls data acquisition configuration setups
- controls timebase setup parameters
- controls triggering setup parameters
- performs formatting and manipulation of acquired data
- handles ROM and RAM pack communications

8088 CPU AND CLOCK ◈9◈

A9U246 is a clock generator/driver containing a crystal-controlled oscillator, a divide-by-three counter, and decoding circuitry that outputs a ready signal for the 8088's READY input. The clock, operating from the 14.7 MHz crystal A9Y250, is divided into to a 4.9 MHz, one-third/two-thirds duty cycle rate by A9U246. Two inputs to A9U246, SACK(L) and RAM(L), control the READY line to the 8088.

The READY(H) signal allows the insertion of a wait state into the 8088's four- state bus cycle. When the Dynamic RAM is being addressed, the decoded RAM(L) signal goes active low during the CPU clock's T2 state and remains low until the T4 state. If the SACK(L) signal becomes active low before the rising edge of the clock in the T2 state, no wait states are inserted in the 8088's bus cycle (see Figure 4-17). Conversely, if the SACK(L) signal does not go active low before the rising edge of the clock in the T2 state, then the READY line affects the 8088's bus cycles by adding an extra wait cycle (see Figure 4-18). As long as SACK(L) continues to be high, wait states continue to be generated.

The functions of the various 8088 microprocessor pins are described in the following microprocessor glossary:

AD0-AD7 Address Bus. This bidirectional eight-bit bus is multiplexed with both address and data information. The lower eight bits of the address bus are present during the first part of the 8088 bus cycle, and eight bits of data are present during the last part of the bus cycle.

A8-A15 Address Bus. The upper eight bits of the 8088 address bus provide output addresses for memory data transfers. These addresses are valid during the entire bus cycle.

ALE(H). The Address Latch Enable signal latches address information on the multiplexed address bus.

DEN(L). The Data Enable signal enables the bidirectional Instrument Data Buffer (A9U457) that connects the 8088's AD data bus with the instrument's CD data bus. The enable signal prevents bus contention while the 8088 is transferring data on the AD data bus lines.

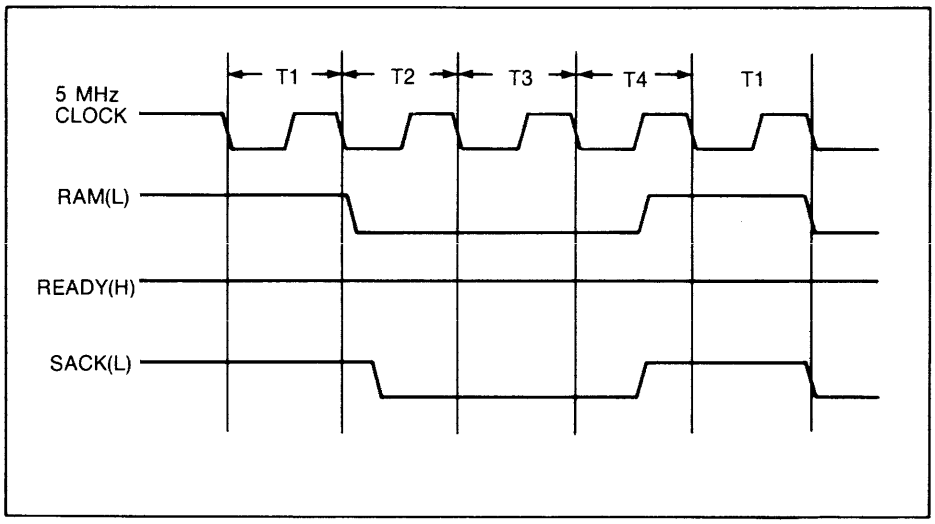


Figure 4-17. READY signal not causing a wait state.

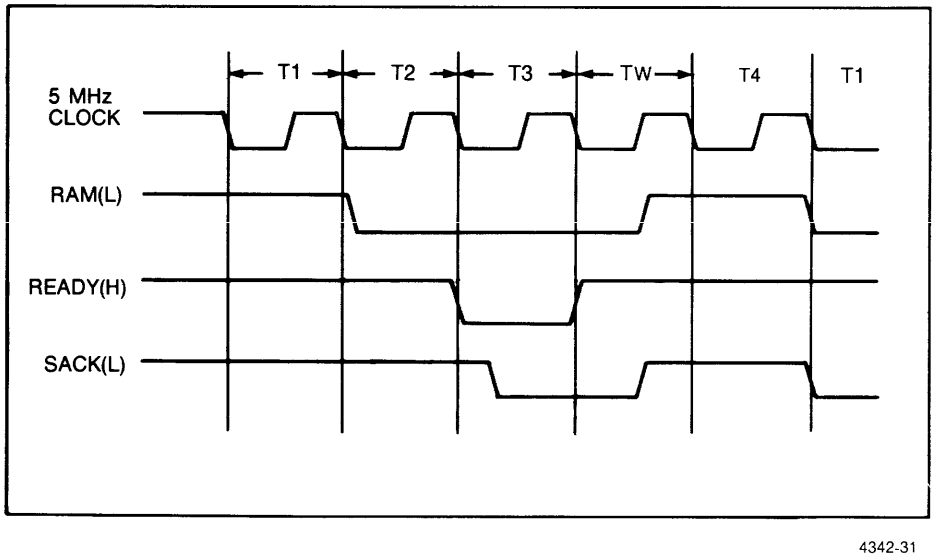


Figure 4-18. READY signal causing one extra wait state.

DT(H)/R(L). The Data Transmit/Receive signal controls data direction for two bidirectional buffers: the Instrument Data Buffer (A9U457), and the ROM/RAM Data Buffer (A9U211).

INTR(L). The Interrupt Request input is used for low battery-voltage detection to ensure that the nonvolatile memory has a continuous power supply.

IO(H)/M(L). The Input Output/Memory signal specifies whether the current address is for a memory device (active low) or for an input/output device (active high).

RD(L). The Read signal indicates that the 8088 is reading data from a memory device.

READY(H). The READY signal is used to add wait states to the 8088's four- state bus cycle to allow for slow memory devices.

RESET(H). The active RESET signal causes the 8088 to immediately suspend execution of instructions. When this signal goes low, the CPU begins executing instructions from memory location FFFF0$_{hex}$.

WR(L). The Write signal indicates that the 8088 is writing data to a memory device.

CPU ADDRESS/DATA BUFFERS ◈9

The 8088 CPU uses address buffers A9U351 and U354 to help in driving the address lines to other circuits. The AD0-AD7 address/data lines, buffered by A9U451, are time multiplexed, first with the lower eight bits of address information and then with data information (refer to Figure 4-19). The bi-directional AD bus into the 8088 is used when reading data from the bus or writing data onto the bus.

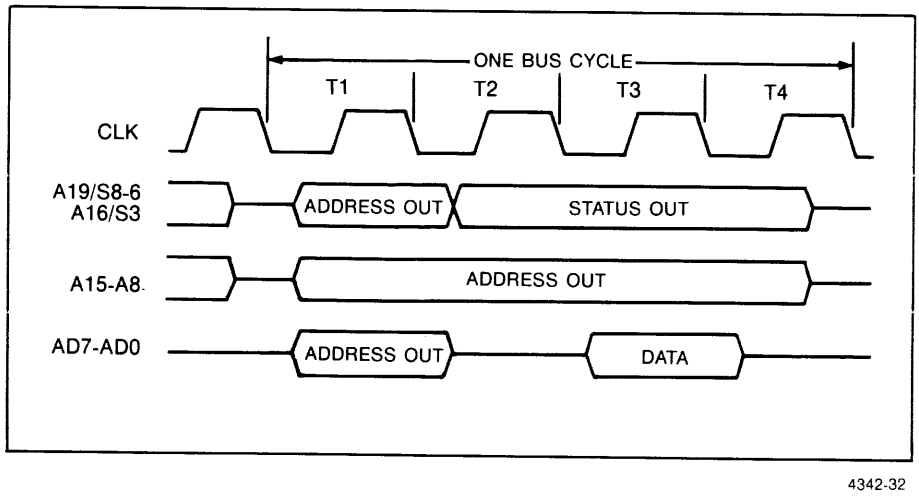


Figure 4-19. Bus cycle with multiplexed address/data on AD bus.

SELECT DECODE ◈9

This circuitry uses the 8088's clock, address, and control lines to produce the following control signals:

- CPU buffers latch-enable signal
- Instrument Addressing and Control decoder enable signal
- ROM/RAM Data Buffer enable signal - PACK(L)
- Dynamic RAM controller enable signal - RAM(L)
- Nonvolatile memory select signal - BACKUP(L)
- ROM decoder enable signals - CODE(L), DIAG(L)

Since the information on the CPU address lines is stable before the ALE (Address Latch Enable) becomes active high, it is possible to shorten the time when ALE is active. Turning off the ALE signal sooner causes the address to be latched sooner, allowing faster memory access times. To accomplish this, the 8088's CLK(L) and ALE(H) signal are ANDed together. This produces an ALE(H) signal that returns inactive low upon the rising transition of the clock in the T1 state.

ROMS AND ROM DECODER ◈10◈

The 128K of ROM space is provided by eight 27128 type 16K x 8-bit EPROMs. These ROMs contain firmware to run the majority of the instrument's operations. Diagnostic code residing in ROM 6, A9U135, is used for instrument diagnostic testing.

The Control Processor memory address assignments are as follows:

ADDRESS	DEFINITION
00000-03FFF	ROM 0
04000-07FFF	ROM 1
08000-0BFFF	ROM 2
0C000-0FFFF	ROM 3
10000-1FFFF	ROM pack
20000-2F7FF	62K Dynamic RAM
2FF00-2FF3F	CON P - I/O P communications
2FF40-2FF43	IBS5 Counter-Timer
2FF44-2FF47	Trigger Position Indicator 1 (upper 8 bits readback)
2FF48-2FF4B	Trigger Position Indicator 2 (trig position value)
2FF4C-2FF4F	Trigger Position Indicator 1 (memory full value)
2FF50-2FF53	Control Latch
2FF54-2FF57	Trigger Position Indicator 1 (trig position value)
2FF58-2FF5B	Trigger Position Indicator 2 (memory full value)
2FF5C-2FF5F	Trigger Position Indicator 2 (upper 8 bits readback)
2FF80-2FFBF	IBS0 Trigger
2FFC0-2FFCF	IBS1 Acquisition slot 0
2FFD0-2FFDF	IBS2 Acquisition slot 1
2FFE0-2FFEF	IBS3 Acquisition slot 2
2FFF0-2FFFF	IBS4 Acquisition slot 3
F0000-F3FFF	ROM 7
F4000-F7FFF	ROM 4
F8000-FBFFF	ROM 5
FC000-FFFFF	ROM 6 Diagnostics

DYNAMIC RAMS, CONTROLLER, AND LATCH ◈10◈

The 62K of RAM space is provided by eight 4864-type 64K X 1-bit Dynamic RAMs. The RAMs provide read/write memory space for storage of volatile information.

The RAM controller, A9U329, handles both types of memory access cycles (read or write) the same way except in the control of the WE(L) Write Enable output (activated only during write cycles). When a memory access occurs, RAM(L) goes active low. The inverted RAM(L) signal's rising edge clocks the MWR(L) and MRD(L) information through A9U325A and A9U325B. These flip-flops accept the decoded read and write signals from A9U214B's DT(H)/R(L) Data Transmit/Receive line. U214B's output is enabled during a memory access by the active low IO(H)/M(L) Input-Output/Memory signal. At the end of each read or write operation, the ENABLE(L) line (from A9U361C) goes high, clocking a low from A9U425B to clear A9U325A and A9U325B. Then, when the RAM(L) signal returns inactive high, the inverted low to the set input of U425B resets that flip-flop.

During a read operation from the RAMs, the MRD(L) signal goes active low. Next, the RAS(L) output from A9U329 goes active low, latching the row address from the OUT0(L)-OUT7(L) lines into the RAMs. The RAM controller then sends CAS(L) active low to latch the multiplexed column information from the OUT0(L)-OUT7(L) lines into the RAMs. Valid data is available on the RAM data outputs approximately 135 ns after the low-going transition of CAS(L). Refer to Figure 4-20.

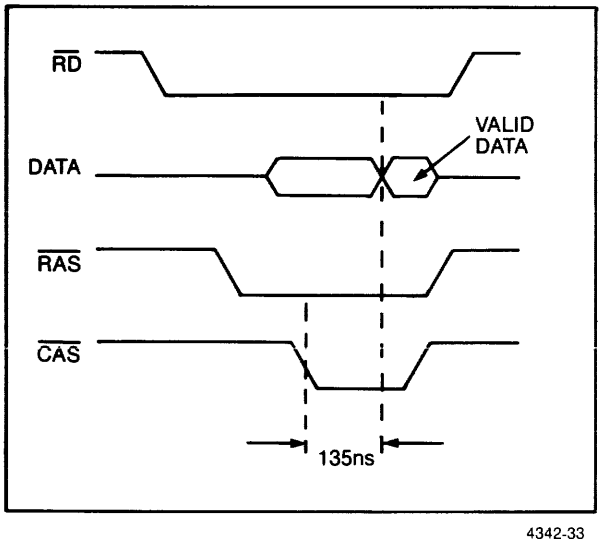


Figure 4-20. Timing of RAS(L) and CAS(L) for RAM data outputs.

INSTRUMENT ADDRESSING AND CONTROL ◈9

A9U454 buffers the 8088 CPU address lines A0-A4, as well as the RD(L) and WR(L) control lines. After buffering, these signals (now preceded by a C) are used by various processor, trigger, and acquisition circuits.

Decoder A9U357 uses 8088 address lines A4-A7 to produce control lines used by various processor, trigger, and acquisition circuits.

INSTRUMENT DATA BUFFER ◇9◇

The eight-bit, bidirectional data buffer A9U457 provides the data communication link between the 8088's AD data bus and the remainder of the instrument operating on the CD data bus. The DT(H)/R(L) Data Transmit/Receive signal controls the direction of data transmission. The following is a list of boards that use the CD data bus:

- I/O Processor: for communication between the CON P and I/O P
- Display: for communication with trigger circuitry
- 9 and 18 Channel Acquisition: for setup, acquisition, and status readback data
- Trigger: for obtaining trigger parameter setups

ROM/RAM ADDRESS BUFFERS ◇9◇

The 8088 CPU address lines A0-A15 are buffered by A9U204 and U207. The buffering helps to drive address lines to any installed ROM or RAM pack.

ROM/RAM DATA BUFFER ◇9◇

The eight-bit, bidirectional data buffer A9U211 provides the data bus communication link between the ROM or RAM pack's data bus and other Control Processor functional blocks operating on the D data bus. The DT(H)/R(L) Data Transmit/Receive signal controls the direction of the data transmission on the 8088's data bus, the Dynamic RAM data bus, and the nonvolatile memory data bus.

ROM/RAM PACK CONTROL ◇11◇

The ROM/RAM Pack Control circuit produces the CS0(L)-CS3(L) signals used to select individual ROMs or RAMs residing in the currently installed pack. When PACK EXPAND (H) to multiplexer A9U201 is low, the SEL0(H) and SEL1(H) inputs control the outputs to decoder A9U214. When pin 1 is high, the A18(H) and A19(H) address lines control the outputs. SEL0(H) and SEL1(H) are actually address lines supplied by the currently installed ROM or RAM pack. Decoding different pairs of address lines allows each chip-select line to address a different amount of memory space. Refer to the following table for a list of the address lines and the corresponding memory space.

Table 4-2
ROM/RAM PACK ADDRESSING

Address Lines	Memory Space Per Chip Select Line
A11 and A12	2K possibility for 8K RAM packs
A13 and A14	8K possiblity for 32K ROM packs
A14 and A15	16K possibility for 64K ROM packs
A18, A19, and PACK(L)	64K possibiltiy for multiple ROM packs

The IRST(H) interrupt line from the I/O Processor controls the chip-select-line buffer A9U217. When low, the IRST(H) line keeps the buffer outputs enabled. This low also turns on the transistor A9Q219, supplying the Vcc to the buffer. When the interrupt line is sent active high, the line not only turns off A9Q219 (removing the buffer's power), but also causes the buffer outputs to float. This action prevents the outputs from unwanted strobing of other nonvolatile memory circuits.

NONVOLATILE MEMORY <11>

The nonvolatile RAM A9U229 supplies 2K of memory space, allowing storage of up to two sets of instrument setup parameters. One set of parameters (the current instrument setup) is automatically stored upon power-down. Remaining space is user-available for storage of one other desired instrument setup. Both sets are retrievable after powering the instrument back up again.

BATTERY BACKUP <11>

Normally, A9Q141 supplies the Vcc to the Nonvolatile Memory A9U229. When the +5 volt supply starts to drop in voltage, A9Q140 turns off A9Q141. This allows the battery A9BT150 to supply the Vcc to U229, the Nonvolatile Memory. This Vcc line also supplies a pull-up to the chip select of U229 when A9U217's outputs are floated during a reset operation.

The comparator A9U140A monitors the Nonvolatile Memory's backup battery voltage. It supplies an active high interrupt signal to the 8088 CPU interrupt input when a low battery supply voltage is detected.

DIAGNOSTIC LEDS AND LATCH <11>

The diagnostic LEDs are used to track the progress of the Control Processor power-up diagnostics. As the power-up routines progess, the LEDs indicate which test is currently being run. If, at any time, the Control Processor fails power-up diagnostics, the lighted LEDs convey information useful in determining the problem area. (Complete LED error information is listed in the *Troubleshooting and Repair* section of this manual.) The diagnostic LEDs are controlled by bits 0 through 5 of the LED latch A9U220. Bit 6 is used for diagnostic purposes and bit 7 is used to interrupt the I/O Processor during inter-processor communications. A low output turns on the associated LED, and a high output turns the LED off. Since the latch is reset upon power-up, all LEDs are turned on at power-up until the Control Processor turns them off.

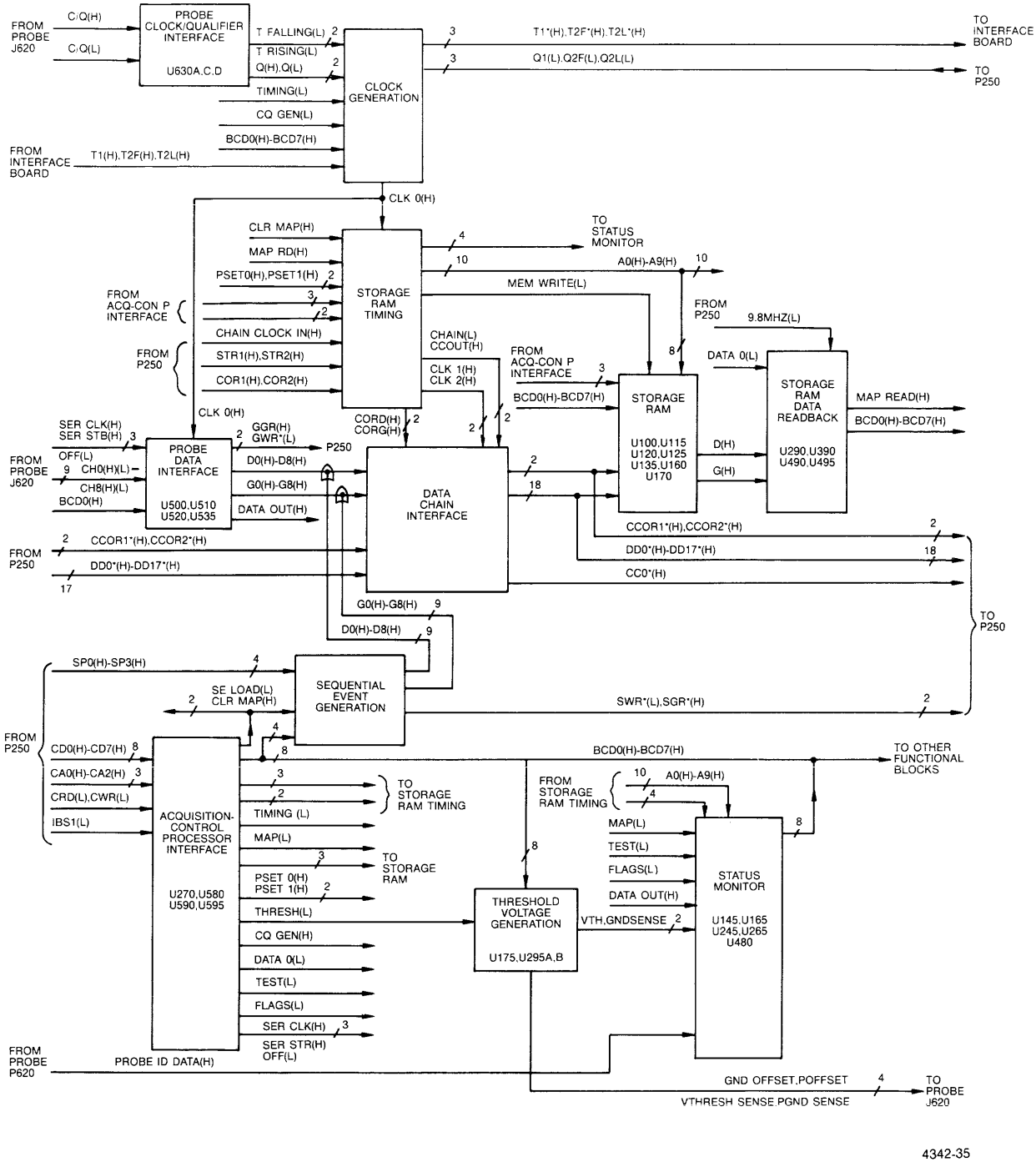


Figure 4-21. 9-Channel Acquisition Board functional block diagram.

9-CHANNEL ACQUISITION THEORY

OVERVIEW

The 1240D1 9-Channel Acquisition Board supports the following functions:

- 10 ns probe data latch, memory 513 samples deep
- 20 ns probe data/glitch latch, memory 257 samples deep
- clock qualification and data storage qualification
- event generation for triggering
- contributes to timebase generation
- memory chaining to other 1240D1 9-Channel Acquisition Boards

Chaining of data from the first acquisition card to the next requires common data bus lines and control lines. To distinguish between each of the four identical acquisition board slots on the Interface Board, the * symbol in a signal name takes on a letter from A to D. For example, the signal TEST*(H) is common to four different acquisition slots, but becomes TESTA(H) when referencing acquisition slot 0 (J250). The remaining designations are: * = B for slot 1 (J350), * = C for slot 2 (J450), and * = D for slot 3 (J550).

ACQUISITION-CONTROL PROCESSOR INTERFACE 

The interface provides a communication link between the Control Processor's CD data bus and the 1240D1 9-Channel Acquisition's BCD data bus. The Control Processor uses this link for the following operations:

- loading event values for Sequential Event Generation
- loading qualifier values into the Clock Generation circuitry
- loading voltage levels for Threshold Voltage Generation
- reading probe data from the Storage RAMs
- reading board status bits from the Status Monitor

A15U595 is a bidirectional buffer that gates data on and off the acquisition card. A15U580 and U590 are one-of-eight decoders that output write control lines (from U580) and read control lines (from U590) for Control Processor read and write operations. The Control Processor uses the read, write, instrument address, and board select lines to access various 9-channel registers. A15U270, a miscellaneous control register, latches data from the BCD data bus as mode control signals (such as probe interface signals and some RAM select signals for other 9-channel circuitry).

PROBE CLOCK/QUALIFIER INTERFACE ◈28◈

Differential line receivers A15U635A and C accept the ECL-level clock/qualifier lines C/Q(L) and C/Q(H) from the installed acquisition probe. The resulting Q signals, Q(H) and Q(L) from A15U440B, are used by the Clock Generation circuitry as logic level indicators (logic high or logic low). The Q signals are also used in the generation of the T signals, T RISING(L) and T FALLING(L). The T signals are also used by the Clock Generation circuitry to indicate rising and falling edge transisitons. Transitions on the differential C/Q lines pass through U635C. A falling edge on the C/Q probe line causes U635C pin 7 to go low (the active T FALLING (L) signal). The delay-invert path through U635A, U440B, and U635D pulls the active low line high again. The same process occurs for a rising edge on the C/Q probe input line, causing the active low T RISING(L) signal.

CLOCK GENERATION ◈31◈

The qualification parameters set up in the menu are sent from the Control Processor over the BCD0(H)-BCD7(H) lines to latches A15U275 and U475. The latch outputs are sent, along with the T and Q signals from the Probe Clock/Qualifier Interface, to the OR-AND-INVERT gates A15U445, U540, and U550. These gates produce a total of six outputs. Three of these are T-signal edge indicators T1∗OUT(H), T2L∗OUT(H), and T2F∗OUT(H). These T signals are ORed on the Interface Board with T signals from other installed acquisition cards. (When the asynchronous timebase is selected, it generates transitions onto the T1 signal line only.) The three remaining outputs are the Q-signal level indicators Q1(L), Q2F(L), and Q2L(L). The Q signals are ANDed on the Interface Board with Q signals from other installed acquisition cards.

The circuitry consisting of A15U545A and B, and U550A is used to select the current sample clock timebase, T1(H), T2F(H), or T2L(H) from the ORed T signals. When a T signal edge selected by the user in the Timebase menu occurs with its corresponding true Q signal (active low), the master sample clock CLK0(H) is generated. The CLK 0(H) signal, controlling the sampling of data in the front end hybrids, latches data present on the probe CH0(H)(L)-CH8(H)(L) lines into the front-end hybrids A15U500, U510, and U520 located in the Probe Data Interface.

STORAGE RAM TIMING ◈31◈

This circuitry generates timing and control signals used during the storage of probe data into the storage RAMs. The master sample clock from the Clock Generation circuitry, CLK0(H), and the master storage signals from the Trigger Board, STR1(H) and STR2(H), are the main inputs to this circuitry.

A15U455 is a dual one-of-four selector that produces two outputs based on the pin 7 (active when using timebase T2) and pin 9 (active when using timebase T1) select lines. U445 pin 15 outputs correlation data from COR1(H) or COR2(H) inputs. The correlation information, stored with the probe data, is used when reconstructing data for display if two asynchronous timebases were used during the acquisition.

The pin 2 output from A15U455 transmits a storage clock signal used by the storage RAM timing circuitry. Based on the selections present at pin 7 or 9, A115U455 outputs STR1(H) used with time-base 1, STR2(H) used with timebase 2, or CHAIN CLOCK IN(H) used when storage is controlled by a previous card in the chain. The circuitry comprised of A15DL360, U345B, U350B and C, and U355 A and B, generates write pulses to the storage RAMs at the wire OR on the output of U350C. A15U355A operates only when using the data/data acquisition mode. U355B is used in this same mode as a divide-by-two, generating write pulses on every-other store cycle. A15U355B is also used in the data/glitch acquisition mode as a one-shot, generating write pulses on every store cycle. When the write pulse from A15U140B goes inactive high, OR gate U350D passes this signal to increment the Memory Address Pointer (MAP) circuitry (during storage or retrieval of data from the RAMs).

The MAP circuitry generates the addresses used to access the storage RAMs. These addresses also serve as a memory address pointer value used by the Control Processor when reconstructing data for display. The MAP circuitry, consisting of counters A15U150 and U250, is clocked by the MAP READ(H) signal (from the Storage RAM Data Readback circuitry). Counter A15U390 supplies a four count to the memory address pointer circuitry and the readback shift registers. Each count loads a bit into the readback shift register and increments the MAP counter. The Control Processor reads the MAP count through the Status Monitor on the A0(H)-A7(H) lines.
The MAP counters produce an eight-bit count on address lines A0(H)-A7(H). The terminal count from A15U150 and U250 enable a third counter, A15U255. As a count is produced on address lines A8(H) and A9(H), a comparison to the memory chain depth indicators PSET 0(H) and PSET 1(H) is made by A15U155A. If the depth indicators are set at 00 (no cards chained), the logic causes the counter A15U255 to output an active FO(H) Filled Once signal when the first acquisition card is filled. If the depth indicators were set at 11 (binary code indicating four cards chained), the FO(H) signal would become active on this card after all cards in the chain are filled.

Address lines A8(H) and A9(H) are also used to decode the following signals:

- CHAIN(L) - indicates that memory chaining is in progress
- MEM WRITE(L) - writes data at current location into Storage RAM on this card
- CCOUT(H) - chain clock signal that causes data to be stored on chained cards

A15U345 A and C produces the CLK 1(H) and CLK 2(H) signals from the master sample CLK 0(H) signal (generated by the Clock Generation circuitry). These signals clock the probe data latches in the Data Chain Interface. The CLK 1(H) signal latches in the data information, and CLK 2(H) latches in data or glitch information.

A15U260A and C, along with its associated circuitry, monitors the CLK 0(H) line to determine if a master sample clock is occurring. The FLAGS(L) signal allows the control processor to read the status of the monitoring circuitry. When the readback occurs on the SLOW CLK(H) line, any record of a previous clock occurrence is cleared. By routinely checking for clocks generated on the CLK 0(H) line, it may be determined that clocks are infrequent.

A15U340 produces a holdoff signal to stop any global event from becoming true until a clock on its associated timebase occurs. It also generates the NO CLK(H) signal to the Status Monitor, indicating to the Control Processor that no clock has ever occurred.

PROBE DATA INTERFACE ◈28◈

The nine differential ECL-level channels CH0(H)(L)-CH8(H)(L) carry probe data to the front-end hybrids A15U520, U510, and U500. The hybrids provide a latch for probe data, and compare incoming data and glitch information against previously selected event patterns. When a data word match occurs, A15U635 outputs the active-low global word recognizer GWR*(L) signal. When a data/glitch acquisition match occurs, both the global word recognizer and global glitch recognizer, GGR(H), outputs go to their active states. A15U635 is a dual OR-gate package that produces the global word and global glitch recognizer signals sent to the trigger board.

Data latched by the hybrids is sent on the D0(H)-D8(H) and G0(H)-G8(H) lines to the Sequential Event Generation circuitry and the Data Chain Interface. Once at the chain interface, the information may be chained to the next acquisition card or sent to the Storage RAMs.

The serial global-event pattern information is loaded on BCD0(H). Each front-end hybrid has 16 internal shift/store control registers that hold the event patterns. (The registers also control selections for data/glitch storage.) After sequentially shifting the global data and glitch recognizer values into the hybrids with the SER CLK(H) signal, the SER STB(H) signal latches the data into the hybrids. An internal mode of operation for the front-end hybrids, also programmed into the control registers, allows the global word recognizer to operate separately from the selected timebase. This allows data unrelated to the sample clock to be compared against global event patterns.

The DATA OUT(H) signal line carries the serial pattern information previously clocked in on the BCD0(H) line. Diagnostics use this read back information to verify the shift/store registers.

During data chaining operations, the data inputs on cards not connected to data probes are forced to be a logic low. Activating transistors A15Q600 - Q628 (on the hybrid's inverting inputs) with the OFF(L) line puts a logic high on the inputs, thereby causing the logic low.

SEQUENTIAL EVENT GENERATION ◈28◈

This circuitry uses sequential event RAMs for storage of up to 14 different event recognition patterns. The five-bit counter, A15U300, preloads the sequential event RAMs A15U415, U410, U435, and U425 with desired event patterns. The values are stored into 14 separate memory blocks per RAM (according to the user's Trigger menu setup) by controlling the BSP0(L)-BSP3(L) buffered stack pointer lines from A15U535. The Trigger Board generates these stack pointer lines to control which block is currently being accessed. The incoming probe data and glitch information from the Probe Data Interface is compared to the previously stored patterns. When the outputs of the sequential word RAMs (A15U415 and U410) are both true indicating a match was found, buffer A15U440-15 passes the active low SWR*(L) signal. When the outputs of the sequential glitch RAMs (A15U435 and U425) are both true indicating a match was found, buffer A15U440-12 passes the active high SGR*(H) signal.

DATA CHAIN INTERFACE ◈30◈

The interface consists of two sets of data latches. The probe data latches A15U320, U310, U335, and U330 accept data on the D0(H)-D8(H) and G0(H)-G8(H) signal lines from the Probe Data Interface. Output data from these latches is available for either the Storage RAMs or the data chain bus, if chaining is in effect. Refer to Figure 4-22. The chain bus latches A15U575, U570, U565, and U560 transmit data to the next acquisition card in the data chain, allowing each acquisition card to pass (i.e., chain) data to the next like acquisition card.

The CCOR1*(H) and CCOR2*(H) signals are the correlation chaining signals that carry correlation information to the next acquisition card in the chain. This information, stored with the probe data, is used when reconstructing data for display if two asynchronous timebases were used during the acquisition.

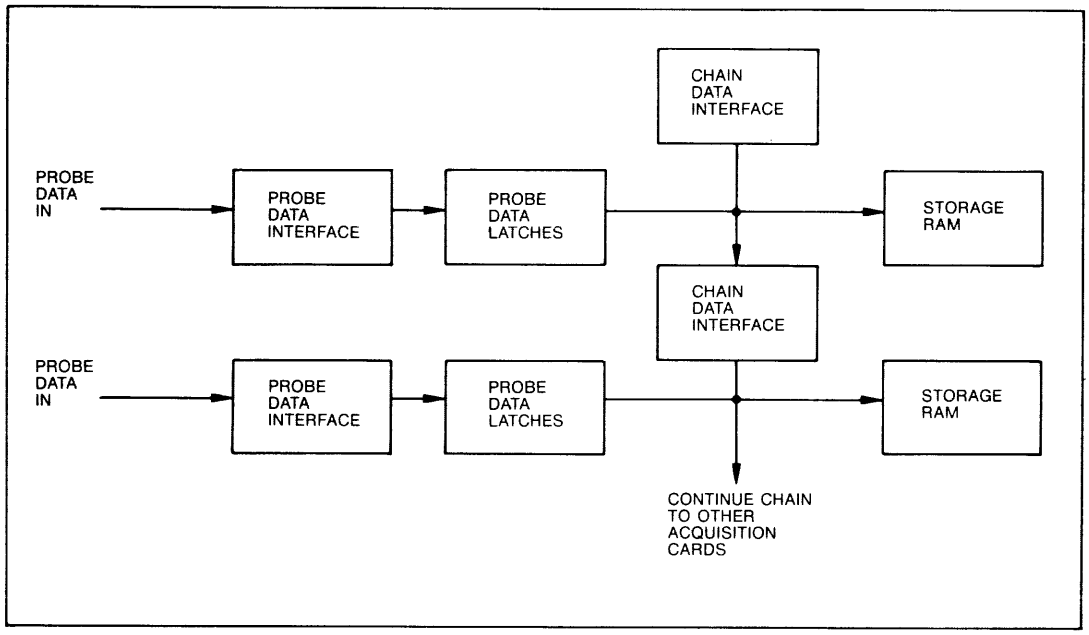


Figure 4-22. Data chain interface.

Chaining of data from the first acquisition card to the next requires connecting data bus lines and control lines. To distinguish between each of the four identical acquisition board slots in the mainframe, the * symbol in a signal name takes on a letter from A to D. For example, the signal TEST*(H) is common to four different acquisition slots, but becomes TESTA(H) when referencing acquisition slot 0 (J250). The remaining designations are: * = B for slot 1 (J350), * = C for slot 2 (J450), and * = D for slot 3 (J550).

STORAGE RAMS ◈30◈

The Storage RAMs A15U100, U115, U120, U125, and U135 are 256 x 4-bit ECL RAMs that provide temporary buffer storage for data coming from the probe, or data being chained from a previous card. When the Control Processor reads data out of the Storage RAMs, it accesses one 256 x 2-bit block at a time. The serial ECL-level data is converted to TTL-level data by the high-speed comparators A15U160A and B. The serial data is then converted into parallel data by the Storage RAM Data Readback circuitry.

STORAGE RAM DATA READBACK ◈29◈

This circuitry provides the Control Processor with a readback path for data stored in the Storage RAMs. The circuitry accepts serial RAM data and glitch information on D(H) and G(H), respectively. Shift registers A15U490 and U495 convert the serial data into parallel data for the Control Processor to read on the BCD data bus. Counter A15U390 supplies a four count to the shift registers and memory address pointer circuitry (located in the Storage RAM Timing circuitry) after a processor read. Each count from A15U390 pin 14 loads a bit into each of the registers, then the DATA 0(H) signal clocks the two 4-bit blocks of storage RAM data onto the bus.

STATUS MONITOR ◈29◈

This circuitry allows the Control Processor to read back the condition of certain control and address lines, as well as the attached probe's I.D. and the board's own I.D. Buffers A15U145 and U245 gate the memory address pointer (MAP) values as addresses A0(H)-A7(H) onto the BCD data bus. The Control Processor uses the MAP value when manipulating the acquisition board's data for display. Buffers A15U165 and U265 gate the upper two MAP address bits, A8(H) and A9(H), onto the BCD data bus. A15U480 buffers the following lines onto the BCD data bus:

- BCD0(H): used for readback of the front-end hybrid's serial control registers
- BCD1(H): used to carry pod I.D. information from each probe as an identifier
- BCD2(H)-BCD7(H): used to carry the board's own identification data, indicating that it is a 1240D1 9-Channel Acquisition Board.

THRESHOLD VOLTAGE GENERATION ◈28◈

This circuitry produces variable threshold voltages for probe data channels acccording to user-specified values in the Memory Config menu. The digital-to-analog convertor, A15U175, and the gain amplifier, A15U295A, translates the user's data on BCD0(H)-BCD7(H) into a voltage level. Each bit change produces a 50 mV threshold voltage change, with a total range from +6.35 volts to −6.35 volts.

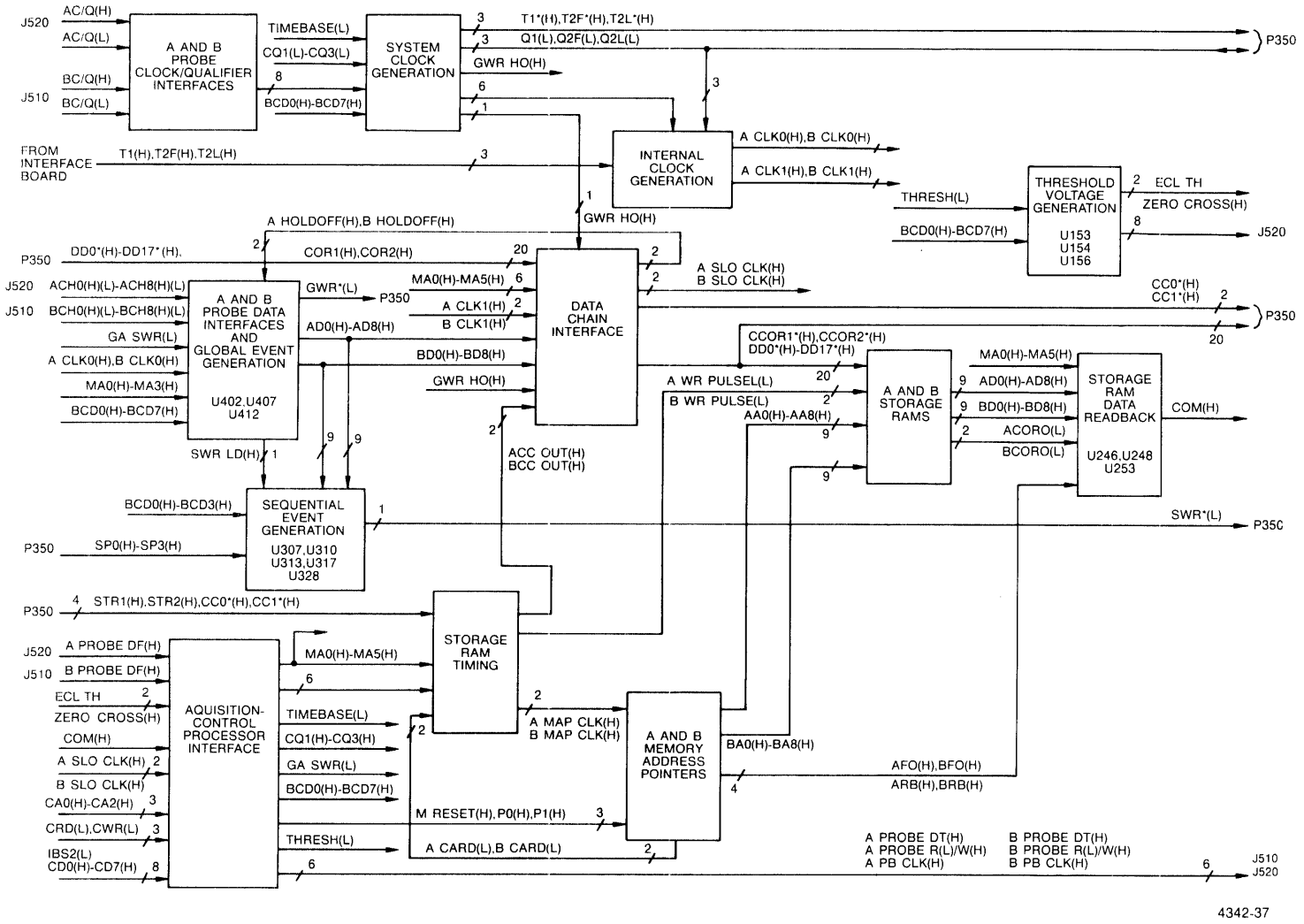


Figure 4-23. 18-Channel Acquisition Board functional block diagram.

18-CHANNEL ACQUISITION THEORY

OVERVIEW

The 18-Channel Acquisition Board holds circuitry that supports the following functions:

- two separate data probe inputs
- bus demultiplexing capabilities allowing A probe (only) to store in both A and B memory sections
- 20 ns acquisition rate, memory 513 samples deep
- operation from two timebases
- clock qualification and data storage qualification
- event generation for triggering
- contributes to timebase generation
- memory chaining to other 18-Channel Acquisition Boards

Chaining of data from the first acquisition card to the next requires connecting data bus lines and control lines. To distinguish between each of the four identical acquisition board slots in the mainframe, the * symbol in a signal name takes on a letter from A to D. For example, the signal TEST*(H) is common to four different acquisition slots, but becomes TESTA(H) when referencing acquisition slot 0 (J250). The remaining designations are: * = B for slot 1 (J350), * = C for slot 2 (J450), and * = D for slot 3 (J550).

ACQUISITION-CONTROL PROCESSOR INTERFACE 

The interface provides a communication link between the Control Processor's CD data bus and the 1240D2 18-Channel Acquisition's BCD data bus. The Control Processor uses this link for the following operations:

- loading event values for Global Event Generation
- loading event values for Sequential Event Generation
- loading voltage levels for Threshold Voltage Generation
- loading data delay values for the Probe Data Interface
- loading selections for System Clock Generation
- reading back acquisition data from the Storage RAMs
- readback of miscellaneous 18-channel circuitry

A16U557 is a bidirectional buffer that gates data onto the acquisition card's data bus. A16U553 and U348A are decoders that output write control lines (from U553) and read control lines (from U348A) for control processor read and write operations. A16U266B is a high-speed comparator that converts ECL levels to TTL levels for the readback register U561. This register passes the following information:

- A and B memory slow clock indicators on BCD0(H) and BCD1(H)
- probe threshold zero crossing detection on BCD2(H)
- board identification (18-channel) on BCD3(H)-BCD5(H)
- A and B pod (probe) identifier on BCD6(H) and BCD7(H)

A16U461 and U457 are write registers that output miscellaneous address and control lines to 18-channel circuitry.

The combination of A16U261 and U361 form a serial-to-parallel converter for data from the Storage RAM Data Readback circuitry. In addition, memory filled and memory address pointer information is read back through the converter. The parallel data is sent to the Control Processor on the BCD data bus.

PROBE CLOCK/QUALIFIER INTERFACE 

Line receivers accept the ECL-level clock/qualifier signals from the connected probes. The resulting signals are used for the generation of T clocks and Q qualifiers in the System Clock Generation circuitry. Since operation of the A- and B-side circuits are the same, only the A side is discussed.

Differential line receivers A16U417B and C accept the AC/Q(H)(L) clock/qualifier lines from the 18-channel's A-side probe. The falling edge of a signal on the C/Q line causes U417B pin 7 to go low. The delay-invert path through U417C and U417A pulls the active low signal line high again. The T-pulse rising and falling edge output signals serve as clock pulses for the System Clock Generation circuitry. The clock pulses may be gated onto the specified timebase (T) bus by the System Clock Generation circuitry. Qualifier outputs from U417C are also gated onto the Q-bus by the System Clock Generation circuitry.

SYSTEM CLOCK GENERATION

This circuitry accepts the Timebase menu setup selections. These selections are sent by the Control Processor to latches A16U566, U357, and U453. The latch outputs are sent, along with T-clock and Q-qualifier signals from the Probe Clock/Qualifier Interface, to the OR-AND-INVERT gates A16U532, U428, U521, U435, U432, and U425. These gates produce a total of six outputs that allow chosen T clocks and Q qualifiers (none, any, or all) to be gated onto their respective buses. All active high T-bus signals are ORed together on the Interface Board, allowing T-bus clocks from any installed acquisition cards to contribute to the generation of the master sample clock (for the gate arrays in the Probe Data Interface). In addition, all active low Q-bus signals are ANDed together on the Interface Board.

A16U466 latches selections sent by the Control Processor for use in the Internal Clock Generation circuitry. These selections choose the timebase that will drive the A- and B-side master sample clocks.

INTERNAL CLOCK GENERATION <35>

This circuitry is used to produce the master sample clock for both A and B sides of the Probe Data Interface. The A and B circuits are duplicates of each other; therefore, only the A side is discussed.

A16U535A, U528A, and U525A produce the A CLK0(H) master sample clock that latches data into the gate arrays A16U412, U407, and U402. The inputs to this circuitry are the T clocks that are ORed with other T clocks from any installed acquisition cards and Q qualifiers that are ANDed with other Q-bus signals from any installed acquisition cards. When a T-signal edge selected by the user in the Timebase menu occurs with its corresponding true Q signal, the master sample clock is generated.

The A CLK1(H) signal clocks the A-side probe data into the Data Chain Interface.

STORAGE RAM TIMING <36>

This circuitry generates timing and control signals used during the storage and retrieval of data in the Storage RAM. Trigger Board master-storage signals STR1(H) used with timebase 1, and STR2(H) used with timebase 2, are the main inputs along with the A and B chain clocks ACC IN(H) and BCC IN(H).

The A and B circuits are duplicates of each other; therefore, only the A-side circuitry is discussed.

The OR-AND-INVERT package A16U332 produces the timing signals used to generate the A storage RAM write signal A WR PULSE(L). A16U346C produces a clock signal A MAP CLK(H) used to increment circuitry in the Memory Address Pointer. A16U346A provides a storage RAM memory write signal to the next card in the chain when memory chaining is in progress.

PROBE DATA INTERFACE AND GLOBAL EVENT GENERATION <32>

The 18 differential ECL-level channels from both A and B probes carry probe data to the gate arrays A16U412, U407, and U402. The gate arrays provide a sample latch for probe data, and compare incoming data against previously selected event patterns. When a match occurs, the gate arrays output an active low Global Word Recognizer GWR(L) signal from U324B pin 15. The latched data is sent to the Data Chain Interface and the Sequential Event Generation circuitry, and into storage RAM (via the chain interface).

The global event pattern information is loaded into the gate arrays A16U412, U407, and U402 on BCD0(H)-BCD6(H). Each gate array has four internal registers. Two of these hold the global event patterns for the A and B sides. One register controls the delay of data through the gate array, and the other latches data used during programming of the sequential word recognizer.

An internal mode of operation for the gate arrays, also programmed into the control registers, allows the global word recognizer to operate separately from the selected timebase. This allows data unrelated to the sample clock to be compared against global event patterns.

During data chaining operations, the data inputs on the cards not connected to data probes are forced to a logic low by internal gate array programming.

DATA CHAIN INTERFACE 33

The interface consists of two sets of data latches. The probe data latches A16U438, U442, U445, and U448 accept data from the Probe Data Interface for both A and B probes. Output from these latches is available for either the storage RAMs or the data chain bus if chaining is in progress. Refer to Figure 4-24 The chain bus latches A16U538, U542, U545, and U548 transmit data to the next acquisition card in the data chain, allowing each acquisition card to pass (i.e., chain) data to the next like acquisition card.

The CCOR1*(H) and CCOR2*(H) signals are the correlation chaining signals that carry correlation information to the next acquisition card in the chain. The correlation information, stored with the probe data, is used when reconstructing data for display if two timebases were used during the acquisition.

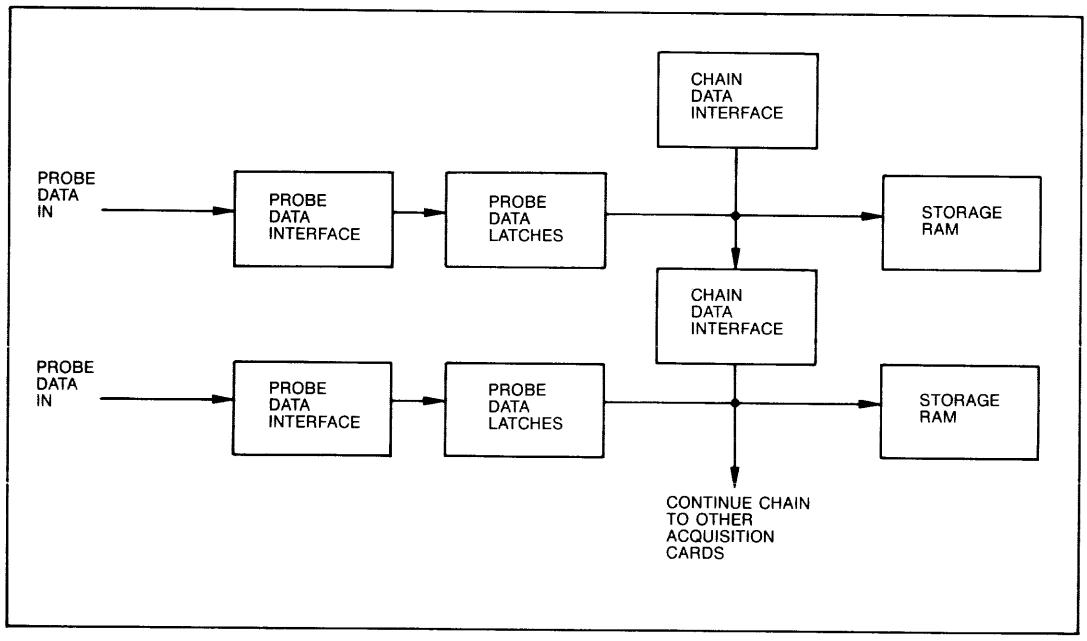


Figure 4-24. Data chain interface.

Chaining of data from the first acquisition card to the next requires connecting data bus lines and control lines. To distinguish between each of the four identical acquisition board slots in the mainframe, the * symbol in a signal name takes on a letter from A to D. For example, the signal TEST*(H) is common to four different acquisition slots, but becomes TESTA(H) when referencing acquisition slot 0 (J250). The remaining designations are: * = B for slot 1 (J350), * = C for slot 2 (J450), and * = D for slot 3 (J550).

MEMORY ADDRESS POINTER 34

The MAP circuitry creates addresses for the Storage RAM during storage and retrieval of data. These addresses also serve as memory address pointers for the Control Processor when it reconstructs data for display. The circuitry for the A and B sides are duplicates of each other; therefore, only the A side is discussed.

Three 4-bit counters A16U119, U116, and U111 form the addresses for the A-side Storage RAM. Counters A16U119 and U116 form a count on address lines AA0-AA7. The terminal count from A16U116 enables the third counter, A16U111. As the count is produced on the remaining address lines, a comparison to the chain depth indicators P0(H) and P1(H) is made by A16U124A and D. If the indicators are set to 00 (no cards chained), the logic causes the counter to output an active AFO(H) Filled Once signal when the first acquisition card is filled with data. If the chain depth indicators were set to 11 (binary code indicating four cards chained), the filled once signal would become active on this card after all cards in the acquisition chain were filled.

The ARB(H) and BRB(H) signals (A- and B-side MAP readback bits) indicate when the MAP end count ($1FF_{hex}$) has been reached. This information is used to determine the oldest/newest data boundary in memory.

STORAGE RAMS ◈34◈

The Storage RAMs consist of two sections with five ECL static RAMs per section. Five RAMs (each 2 bits x 512 locations) hold A-probe data and the remaining five RAMs hold the B-probe data. The A side, comprised of RAMs A16U203, U207, U211, U215, and U219, provides temporary buffer storage for DD17*(H)-DD9*(H) and CCOR1*(H). The B side, comprised of RAMs A16U224, U228, U232, U236, and U240, provides temporary storage for DD0*(H)-DD8*(H) and CCOR2*(H).

STORAGE RAM DATA READBACK ◈34◈

The readback circuitry multiplexes the ECL-level data from the storage RAMs for serial output to the Acquisition-Control Processor Interface. Multiplexers A16U246, U253, and U248 select outputs from the A-and B-side storage RAMs, as well as memory address pointer outputs and correlation data. The ECL-level serial information is converted to TTL-level parallel information in the Acquisition-Control Processor Interface.

SEQUENTIAL EVENT GENERATION ◈33◈

The Sequential Event Generation circuitry allows the user to specify recognition of up to 14 unique data patterns. The sequential word recognizer control signal SWR(L) is generated for trigger circuitry upon recognition of any of the data patterns.

The sequential event RAMs A16U307, U310, U313, and U317 are loaded with the data patterns specified by the user in the Timebase menu. The data patterns, sent on AD0(H)-AD8(H) and BD0(H)-BD8(H), is from the gate arrays in the Probe Data Interface. All levels of the stack (which is controlled by the Trigger Board) are programmed with data patterns to output a true (low) signal for a pattern match or a false (high) signal for no pattern match. The RAMs, acting as word recognizers, output the true low signal when the pattern match occurs. AND gate A16U324A outputs the Sequential Word Recognizer SWR(L) signal when all inputs are true low.

THRESHOLD VOLTAGE GENERATION ◈35◈

This circuit produces variable threshold voltages for both A and B acquisition probes. The data channel threshold is specified by the user in the Memory Config menu. The digital-to-analog convertor, A16U156, latches and translates the data on BCD0(H)-BCD7(H). Operational amplifiers A16U153A and B produce the A-side threshold voltages, while A16U154A and B produce the B-side threshold voltages. Each bit change produces a 50 mV threshold voltage change, with a total range from +6.35 volts to -6.35 volts.

A16U226A is a zero crossing detector that indicates when the threshold voltage reaches a 0 volt level. This detector is used during diagnostic testing of the threshold circuitry.

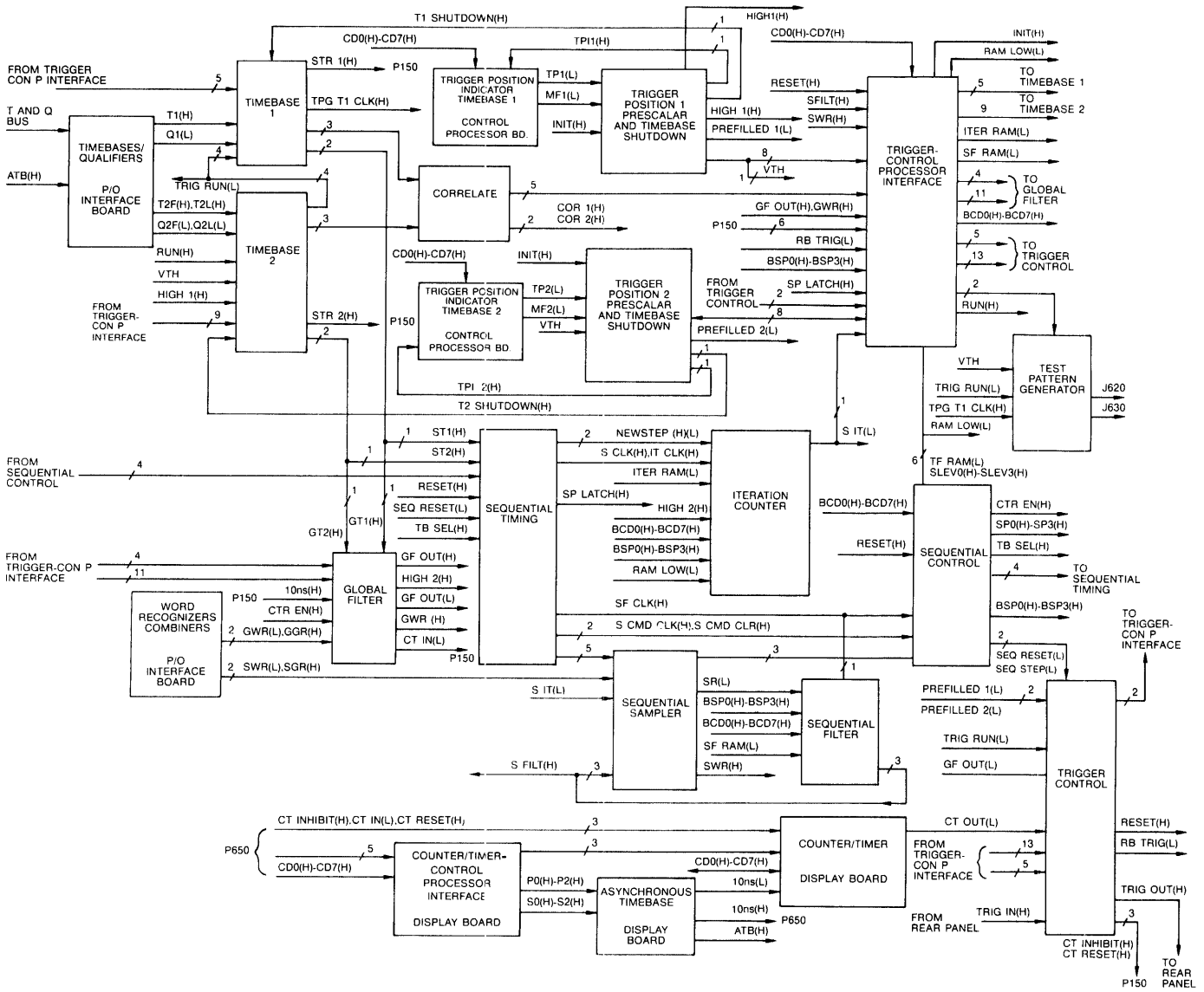


Figure 4-25. Trigger Board functional block diagram.

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TRIGGER BOARD THEORY

OVERVIEW

The trigger circuitry allows the 1240 to locate a unique state based on its inputs and user programming, and reference data storage to that unique state. Trigger circuitry is located on the Trigger Board, the Display Board, and the Control Processor Board. The overall trigger system can be divided into two major operating control systems. The first, Trigger Generation, recognizes and triggers on the unique state being searched for. The second, Data Storage Control, monitors the valid (qualified) data being stored to determine the amount of memory space that surrounds the trigger point. This circuitry also generates correlation data that indicates storage-clock arrival time for each timebase. With this information, the stored data may be reconstructed and displayed as it occurred at the probe tip.

In addition to these two major control systems, there are three Supplemental Circuit Blocks that are incidental to basic triggering functions. A Test Pattern Generator (residing on the Trigger Board) produces two sets of outputs used during diagnostics. An Asynchronous Timebase that can be used for timebase T1 resides on the Display Board. Also, a Trigger-Processor Interface (residing on the Trigger Board) serves as the interface link between the Trigger and Control Processor Boards.

TRIGGER GENERATION

Sequential Event Timing 

These circuits generate strobes required for control of the Sequential Sampler, Iteration Counter, Sequential Filter, stack pointer, and command decoding circuits. By using the stack information, the circuit is able to determine which level of the programmed sequential event definitions it should advance or reset to. This function block also controls storage qualification for each sequence level and selection of Timebase T1 or T2 used on the current sequence level. Timebase selection produces an SE CLK(H) signal from which all other strobes and clocks are generated.

Reloading of counters after execution of a reset or level change introduces a set of load signals to the sequence state machine (as well as disabling certain clocks to the state machine).

Sequential Event Timing circuits consists of three basic sections: Timebase Select, Strobe Generation, and Reset Synchronization. The following lists these sections and their functions:

1. Timebase Select:

- T1 or T2 for current level
- Hold off during level change
- Generates base sequence clock

2. Strobe Generation:

- Generate latch and event strobes
- Generate Iteration clock
- Generate Sequential Filter clock
- Generate Sequential Pointer latch
- Command clock

3. Reset Synchronization:

- Reload signals for Iteration and Sequential Filter
- Hold off signals for strobe generation
- Control asynchronous reset

Timebase Select

The output of this section is SE CLK(H), a signal used as the base strobe for all sequential clock circuits. Inputs are ST1(H), ST2(H), TB SEL(H), and a hold off signal from the Reset Synchronization section.

A14U315 is used as a pulse generator for SE CLK(H) by clocking the independent sections with delayed versions of Timebases 1 and 2. Selection of the correct timebase is done per sequence level with A14U240B qualifying the correct section of A14U315 at the D input with a low (true) signal.

A positive pulse is generated on the Q(L) output of either section when selected. This pulse gates through A14U415D to clear itself via the set inputs to both sections. A14U415D is also used to disable SE CLK(H) generation while TB SEL is in transition (due to the changing of a sequence level).

Strobe Generation

Strobes for the sequential state machine are derived from SE CLK(H). The outputs include: S LAT STB(H) and (L), S EVT STB(H) and (L), S CMD CLK(H), SF CLK(H), SP LATCH(H), and IT CLK(H). The S CMD CLEAR(H) signal is an input to this section from the Reset Synchronization section, and is used to generate reload clocks for the Sequential Filter and Iteration Counter.

The pulse widths for the S LAT STB and S EVT STB signals are critical. The S LATSTB signal needs to be 3.2 ns and be 0.5 ns after the start of S EVT STB. In addition, it must return inactive 0.5 ns before S EVT STB. The basic pulse width for S EVT STB is adjusted using A14R414 to control the loop time from clock to set on A14U525. The delay difference between edges is controlled with two 0.5 ns runs (internal to the Trigger Board) that are in series with A14U420A-10. The S EVT STB signal transitions 0.5 ns after the signal enters the run delay (through A14U420A-5). Then 0.5 ns later, A14U420A-10 goes low, generating S LAT STB. the S LAT STB signal ends 0.5 ns before S EVT STB since A14U420A realizes the false (high) transition to A14U525A that amount earlier.

Gate and run delays are used to position IT CLK(H), SF CLK(H), and S CMD CLK(H) relative to the strobes, since these clocks are sampling data processed through specific delay paths.

Reset Synchronization

The inputs to this section are SEQ NEW STEP(H), SEQ RESET(L), and RESET(H). Outputs include NEW STEP(H) and (L), S CMD CLEAR(H), and GLOB-RES. This circuit generates the NEW STEP(H) signal with a controlled pulse width signals for reloading the Sequential Filter and Iteration Counter, as well as to hold the generation of strobes until the new sequence level is established.

A14U425A generates the NEW STEP(H) reload pulse on the occurrence of a sequence level change by SEQ NEW STEP(H), or in the event of a system reset by RESET(H). A14R410 and C410 disharge after a level change request and, when the ramp down is complete, S CMD CLEAR(H) is generated to load the Sequential Filter and the Iteration Counter.

NEW STEP(H) is used to disable the Timebase Select and Strobe Generation sections while the counter new preload values are set up and loaded. This hold off is also required to allow new sequence pointer values to propagate to the acquisition cards and generate the new values on that level.

A system reset can be derived from the sequence or from some other asynchronous source (such as the Counter/Timer). If the source is from the sequence, less time is required to reinitialize the system. A14U425B checks the system reset, RESET(H), to see if it was generated from the sequence. If not, A14U425B-10 goes false (high) and any pending sequence operation is aborted. The New Step one-shot, A14U425A, is cleared by charging A14C410 with A14U425B-15, and then restarted through A14U415C-14 to A14U425A-4.

Sequential Control ◈23◈

Sequential Control circuits of two basic sections: the Sequential Sampler, and the Sequence Pointer. The following lists the functions performed by these sections:

- Accept sequential word and glitch recognizer outputs from the acquisition cards
- Control sequence pointer to acquisition cards
- Produces Wait, Jump, Reset, and Trigger commands
- Filters Sequential Events (1 to 16)
- Counts filtered events (1 to 9999 counts)

Sequential Sampler

Each acquisition card produces a Sequence Word Recognizer (SWR) signal. These signals are combined on the Interface Board. When all SWR outputs are true (low), then the SWR input to the Trigger Board goes true (low).

Each 1240D1 card produces a Sequence Glitch Recognizer (SGR) signal. These signals are combined on the Interface Board. When any SGR output goes true (high), then the SGR input to the Trigger Board goes true (high).

Sequence commands may be true on either the presence or absence of a particular word recognizer value. For example: TRIGGER ON 55 or the opposite polarity, TRIGGER ON NOT 55. EXOR gates A14U535B and C select the ON/ON NOT polarity of the word and glitch recognizers, and combine the word and glitch together. This combined sequence recognizer signal is sampled by A14U525B to eliminate meta-stable glitches produced when the acquisition cards are sampling data asynchronously. This sampled Sequence Recognizer signal, SR(L), is sent to the Sequential Filter and Iteration Counter.

Outputs from the Sequential Filter S FILT(L), the Sequential Iteration Counter S IT(L), and the Sequence Recognizer, SR(L), are combined with timing strobes by A14U530 and U533 in the Sequential Sampler.

For a true event to be found, the word recognizer must satisfy the values set for both the Sequential Filter and the Iteration Counter. A14U530A combines the outputs of the Iteration Counter and the Filter with the word recognizer to generate a true event strobe. The output of A14U530A strobes low when a sequence command has been found true.

For a false event to be found, only the word recognizer need go false; the filter and counter are not checked. The output of A14U533D strobes low when a sequence command has been found false. The output of A14U530B and U533C (wire-OR) goes high when a sequence command has been found either true or false.

Sequence Control

The sequence pointer tells the acquisition cards which word value to use for the sequence word and glitch recognizers.

One bit of the sequence pointer is produced by A14U630 through U640. RAM A14U135 holds the value that the sequence level will go to when a true event is found. RAM A14U235 holds the value that the sequence level goes to when a false event is found. The feedback on A14U630-U640 (pin 2 to pin 5), latches the value taken from the RAM and holds the value until a new true or false event is found.

Four different commands may be performed on each level of the sequence: do nothing, change level, reset the trigger machine, and trigger. RAM A14U330 holds the commands for all sequence levels (for both true and false events). Lines C0(H) and C2(H) are the command for a false event; C1(H) and C3(H) for a true event. A14U430 selects the command for either the true or false event and presents the command to A14U433 which latches it. Table 4-3 shows the encoding of the C0(H)-C3(H) lines.

Table 4-3
ENCODING FOR TRUE AND FALSE EVENTS

TRUE FALSE	C3 C2	C1 C0
Do Nothing	1	1
Change Level	1	0
Reset	0	1
Trigger	0	0

Sequential Filter ◈24◈

The sequential filter, when used, requires the sequential recognizer to be true for a specified number of clock cycles (up to 16 cycles) before it is recognized as a true sequential event. When the event duration is one count less than the user-selected value, the filter outputs an enable signal, S FILT(L).

For a filter value of one, the sequential filter is not used. For a filter value of two, A14U440B requires the word recognizer to be true for one clock before asserting S FILT(L). The OR gate, A14U445B, and A14U340A force S FLIT(L) de-asserted on the next clock cycle.

For a filter value of three or more, A14U435 provides four bits of counter. For each clock during the time the word recognizer is true, A14U435 increments once. When the word recognizer is false, the counter is reloaded with its filter value on the next clock.

When a sequence level is using Timebase 1 - ASYNC, and the word recognizer on that level is not all don't cares (Xs), then the edge/level signal from A14U333 is set low. This enables the Edge mode. In the edge mode when S FILT(L) is asserted, further assertions of S FILT(L) are inhibited by A14U440A until the word recognizer goes false. The iteration counter is also inhibited at this time.

Iteration Counter ◈24◈

The iteration counter, when used, requires the filtered sequential recognizer to occur a user-specified number of times. When the count reaches a value one less than the user selected value, the counter outputs an enable signal, S IT(L).

For an iteration count of one, the iteration counter is not used. For an iteration count of two, A14U215B requires that an event be found by the filter one time before the S IT(L) signal is asserted. On the second true filter output, the command is executed.

For an iteration count of 3 to 9999, the counters A14U220 -U233 require that an event be found by the filter a number of times before asserting S IT(L).

Global Filter ◈25◈

The global filter, when used, forces a recognized global event to be active for a specified number of clock cycles (up to 16 cycles) before it is recognized as a true global event. A global event consists of word and glitch recognition signals derived from the inputs to 1240D1 and D2 cards. The filter can be used with either T1, T2, or 10 ns timebases, and can run from the event edge or during the event level. If the recognized global event is active for the specified duration, a global-event-valid (found) signal is generated. Otherwise, no output is produced. The global filter output goes to both the counter/timer circuitry and the trigger control circuitry.

The global filter consists of four basic sections: Event Polarity, Clock Select, Duration Count, and Edge/Level Control. The following lists these sections and their functions:

1. Event Polarity:

- Word recognizer polarity
- Glitch recognizer polarity
- AND of word and glitch forming Global Event

2. Clock Select:

- Select T1 to sample Global Event
- Select T2 to sample Global Event
- Select 10 ns to sample Global Event

3. Duration Count:

- Detect Global Event false
- Detect Event true 1 to 16 clock cycles
- Reset of current filter count on system reset

4. Edge/Level Control:

- Edge mode holds filter true until Global Event false
- Level mode clears filter true after filter duration, re-arms G.E.

Polarity

The polarity section combines the low true GWR signal and the high true GGR signal to form a low true composite signal, GE(L). This signal is used by the timebase circuitry for storage qualification and is the input to the Duration Count section.

The polarity control is implemented with two EXOR gates, A14U660A and B. A control signal is applied (under processor control) to invert or buffer the GWR and GGR signals. Normally, the GWR(L) line is buffered and the GGR(H) line is inverted, then the signals are wire-ORed (negative logic AND).

If no glitch is specified in the recognizer, then the GGR(H) signal is low (false). In order to allow GE(L) to be true under this condition, the GGR(H) line is buffered.

Clock Selection

The global filter clock is output from A14U345, a one-of-four selector with inputs from Timebase 1, Timebase 2, and 10 ns (from the Asynchronous Timebase). The selector is controlled from user choices applied through A14U185-12, -2, and -15. The 10 ns clock is useful when two asynchronous timebases are inputting events to the Global Filter, and a specific overlap time is required.

The global event may be pre-sampled on any acqusition card in the 1240 by either T1 or T2, or it may be buffered from the user's device under test. In order to correctly re-sample data on the global filter, the data sample clocks, T1 and T2, are time delayed to account for signal propagation and gating of GE(L). The implication of this phase delay is that a Global Event is sampled by the Global Filter on exactly the same system clock cycle in which it was logged into the Front End of the acquisition card.

Duration Count

The inputs to this section are the GE(L) signal, RESET(H), Global Filter clock, and an output from the Edge/Level Control section. The output of this section is the GF OUT signal, indicating the filter condition specified by the user is satisfied.

The Global Filter has special cases for handling counts 1, 2, 3, and 4 to 16. A duration of one means that the Global Event is true at the occurrence of the global filter clock..A duration of two means that the event was true from one clock until the second clock. This implies that the minimum duration of the GE for a filter of two is one clock cycle plus set up time and hold time of the event prior to the global filter clock.

The Duration Count has two contributors: the current GE(L) and the duration qualify signal. These signals are negative-logic NANDed in A14U590C, then sampled by A14U485B. For a filter selection of one, the duration qualifier signal is forced true (low) under processor control and GE(L) is directly sampled by the log-in register.

When a value of two is selected, the reset line on the 2 count flip-flop, A14U585B, is released. When the GE line goes true, the set line of A14U585B is released and the D input can be sampled as a low. If the GE(L) line stays stays low for a period of time until the next clock, the log-in register will sense the AND of the GE(L) and the duration qualifier as true, and GF OUT will go true.

For a value of three selected by the user, on the first clock after GE(L) goes true, A14U585B goes true. Since the output of U585B was false prior to the clock, and the filter is three (GF<3 is cleared which releases A14U585A), U585A samples U585B as false on the first clock. Before the second clock, the output of A14U585A is false (low), so on the second clock A14U490 is preloaded to F (the terminal count value). Since A14U585A was true at the occurrence of the second clock, U585A goes true. A14U690C inverts this signal (low) and the wire-OR of A14U585B, A14U690C and A14U490 is input to A14U590C-13 as true (low). After the third clock, then, assuming that the GE(L) has stayed true, A14U485B senses a duration satisfied condition and GF OUT is true. Other duration values work in a similar way, with values greater than three requiring that counter A14U490 time out.

Edge/Level Control

The inputs to this section are the current GE(L), GF OUT(L), and GE FILT(L). The output is a false signal that is applied to the first stage false detector.

In edge mode, the Global Filter output goes true as soon as the duration is satisfied. The control signal GF EDGE(H) is high, and the edge clear signal is disabled (A14U590B-11). In level mode, if the current filter becomes true (with GF OUT and GE(L) still true), A14U590B-6 goes high. This signal forces a false condition into the duration count circuit by setting A14U585B. This false condition is cleared at the next clock, but the reset of the duration circuit must cycle to completion before the GF OUT signal can be re-asserted.

The GF OUT signal cycles true one clock cycle out of the duration set for the filter. For example, if the filter value is seven, the GF OUT signal is false for six cycles and true for one cycle (if the GE(L) signal is always true).

If the Global Filter is set to one, Edge/Level control is asserted by ANDing the Global Filter clock with the GF OUT signal to give one true pulse per clock cycle. This signal is only applied to the counter/timer. Other systems using the Global Event are executed as soon as the GF OUT signal occurs.

Counter/Timer  A

This circuitry can be used to count occurrences of the output from the Global Filter, to start a 10 ns timer, or to time the duration of the global filter output. The programmed action is halted and any count or time values are stored when a trigger occurs. If the circuitry is pre-programmed with a value when the terminal count is reached or the timer times out, a trigger or reset command is sent to the Trigger Control block.

The counter/timer is a 37-bit, 100 MHz count-up circuit that can increment, start timing, or time while the CT IN(L) signal is active low. When used as a count-down circuit (increment to a limit), the circuit is preset to the terminal count minus the count down value. It then counts up to the terminal value.

The counter/timer consists of four basic sections: Synchronizer, Prescaler, Accumulator, and Terminal Count. The following lists these sections and their functions:

1. Synchronizer:

- Controls input for each mode
  - -increment on CT IN
  - -start 10 ns count on CT IN
  - -count 10 ns clocks while CT IN is true
- Controls reset of circuits
  - -synchronize with 10 ns counts
  - -reload Accumulator and Prescaler
  - -clear Terminal Count register

2. Prescaler:

- Modulo-32 counter
  -reduce cycle speed for counter
  -clock and reload on 10 ns clock
- State control for Accumulator
  -generate write pulse for Accumulator
  -generate address for Accumulator
  -output carry for incrementing Accumulator

3. Accumulator:

-32-bit sum of modulo-32 counts
-RAM has preload value and current count
-read/add/write cycle

4. Terminal Count:

- AND of individual terms
  -present input
  -Prescaler terminal count
  -Accumulator carry
- Latched output at trigger condition
- Cleared on reset before trigger

Synchronizer

The main output of this block, INCR, is from A11U555-3. This is derived from CT IN(L), which is applied to A11U555A and B at pin 9. CT IN(L) is gated with 10 ns(L), CT INHIBIT(H), CT RESET(H), and user-derived control bits. In addition, CT OUT(L) is buffered and applied to terminate input to the counter when the terminal count is reached.

For the increment counter mode, A11U555A enables CT IN(L) directly for INCR pulses. CT INHIBIT(H) and mode select both gate this signal directly on A11U555-7 and -6.

The two 10 ns modes are selected with A11U400-15. This signal (via A11U510-9 and -15) disables the Increment mode on A11U555-6 and enables the 10 ns path on A11U555B pin 10. The Start Timer mode and Time While mode both use A11U450A to sample CT IN synchronously with the 10 ns clock. In Start Timer mode, A11U450A latches true low by releasing A11U555B-12 after detecting CT IN true. A11U555B-13 must be low (Start Timer mode) for A11U450A to latch this case.

Time While mode is set when A11U555-13 is high. When CT IN is true, A11U450A synchronously enables the 10 ns clock (through A11U555-5) in the same fashion as the Start Timer mode. However, because A11U555-13 is high, the enable does not latch and A14U450A continues to sample CT IN(L) at each 10 ns clock.

Both timer modes use the Counter/Timer to total 10 ns pulses based on A11U450A-2 which is applied to A11U555A-5, gating 10 ns on A11U555A-4. The timer modes can be terminated with CT INHIBIT(H) on A11U550-9, or CT OUT(L) wire-ORed from inverter A11U550C-14. Reset also halts the timer.

Synchronizer (670-7525-04) ◇18◇

Reset is now synchronized to the Counter/Timer on the Display board. When the timer is reset A11U451B latches the reset input untill sampled by A11U450A. The prescaler is reset by A11U540-5.

Prescaler

The Prescaler counts modulo-32. Inputs are INCR and Sync Reset from the Synchronizer. The outputs from the Prescaler include control lines for the Accumulator RAM A11U525, the support circuitry for it, and the clock and prescaler carry for the Terminal Count block.

The INCR pulse clocks a divide-by-two, A11U540A and B. U540A preloads the Prescaler after a reset. A11U540B is the divide-by-two portion. It is preloaded through the multiplexer consisting of A11U545A and B which is switched by the preload at the first increment pulse. The preload bit for A11U540B is 4(H) from A11U400-12, and is the odd or even bit for the Counter/Timer LSB. After preloading, A11U540B is a divide-by-two through A11U545A-5.

As the state control, A11U540B alternates the INCR pulses into clock and write cycles. The clock cycle counter, A11U535, increments when pin 6 is low. This changes SP0(H)-SP3(H), the state address lines that are applied to the Accumulator RAM. The next increment pulse is a write cycle, and A11U608B checks for this state by sampling A11U540B and generating a write pulse if it is true. During a write state, A11U540-14 is applied to the Accumulator block to latch data from the Accumulator RAM.

On the terminal count of A11U535, the Accumulator preload register, A11U610, is clocked and the Terminal Count block checks for Accumulator Carry (indicating full terminal count of the Counter-/Timer. The Accumulator preload register is used by the Prescaler to control preloading the Accumulator RAM after a Reset operation. There are two cycles of the Prescaler before a carry is added into the Accumulator RAM.

Accumulator & Terminal Count (670-7525-04) ◈18◈

Reset to the accumulator and terminal count blocks is latched and held. A11U451A resets these two blocks on the first clock after the reset. Reset sets A11U540A-2 high, which is sampled by A11U451-7 on the next clock. A11U451A-2 then asserts reset to the accumulator and terminal clock blocks. A11U530D-15 is now delayed and is used to reset A11U451A-4. This clears reset to the accumulator and terminal count blocks.The pulse width of the edge detector, A11U530D, is set by A11U475A.

Accumulator (670-7525-03) ◈18◈ A

The Accumulator block contains the current count information and outputs a terminal count signal in the event that sufficient counts have been received to warrant it. The Accumulator is controlled by the Prescaler.

The Accumulator has two 16 × 2 (32 bits each) values located within RAM A11U525. One value (A0, A2) is the preload count (which is zero for count up and the number of modulo-32 counts (minus 2) in the Counter/Timer program specification in count-down applications). The other value (C0, C1) is the current count. The RAM preload value is initialized under processor control prior to running the acquisition.

Initialization consists of asserting 7(H) from A11U400-19 to a low to reset the Prescaler counter A11U535. A11U505 can then be used to force the Accumulator RAM address lines to load P0 and P1 (the preload values A0 and A2) to each respective address where they are written using ECL STB(H).

The Accumulator RAM contents are transferred from the preload value to the current count after a reset has occurred. R0(H) and R1(H) control this action. All writes to the RAM are disabled until state 0,1 is entered to guarantee that valid data has been latched and set up for storage. R0(H) and R1(H) are forced to a one-one (1 1) state at reset, and cycle on the terminal count from the Prescaler.

RAM data is switched from preload to count with A11U515, a dual 2-to-1 multiplexer. Data from the RAM is passed through a two-bit adder implemented with discrete logic, and added to a carry bit stored in A11U608A. Data from the adder is stored into the same address it was read from. A11U520 implements a latch with AND gates to hold data during the write cycle (since the write signal sets the D output of the RAM to low).

The entire read-modify-write cycle for the accumulator occurs once every other increment pulse, once every 20 ns in either of the timer modes. To compensate for delay variances, the address-hold time versus write pulse timing is adjusted by changing the timing on the clock to the Prescaler (relative to the write pulse generator, A11U608B). This timing is verified directly on A11U525 as a part of the adjustment.

The Accumulator RAM is read back in the same way that it is initialized. The Prescaler is read back directly through A11U500 and U600. These read back bits include the odd/even information from A11U540B; the reset information from A11U540A; R0(H) and R1(H) that tell where in the reload cycle the system is; and SP0-3 which complete the modulo-32 count. The next step is to reset the Prescaler (especially counter A11U535) by asserting 7(H) to a low. The data from the RAM is then read back by A11U605 while selecting SP levels under processor control (through A11U505).

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Terminal Count

The terminal count is derived from the carry out of the Accumulator and the terminal count from the Prescaler. It is clocked on the transition of the write generator of the Prescaler, which occurs on the LSB boundary. The output signal is passed to the Trigger Control block as a command; it also is used to inhibit future 10 ns clocks in the Counter/Timer via the Synchronizer.

A11U620D negative-logic ANDs the carry from the Accumulator adder with the terminal count from the Prescaler counter, A11U535-4. This signal is sampled on the next increment transition, which is applied to the write generator, A11U608B-11. U608B senses that A11U540B is valid for a write (low), and U608B-14 goes high while the write (pin 15) is generated. Pin 14 clocks A11U470B-11 which senses the terminal condition from A11U620D-14 and latches due to the feedback.

Trigger Control ◈25◈

The Trigger Control circuitry is responsible for source selection and combination for triggering, resetting, and auto-run control of the 1240. The circuitry tests the state of the internal trigger conditions and the external trigger input from the rear panel to determine when valid states (that should generate a trigger) exist. Outputs are produced for other internal circuits, as well as the external trigger out signal to the rear panel.

Trigger Control circuits consist of four basic sections: Trigger Source Select, Reset Source Select, Trigger Enable, and External Trigger Out. The following lists these sections and their functions:

1. Trigger Source Select:
   - Sequence trigger
   - Counter/Timer trigger
   - Global Filter trigger
2. Reset Source Select:
   - Sequence reset
   - Counter/Timer reset
   - Global reset
   - Trigger attempt reset

3. Trigger Enable:

- Prefilled enable
- External trigger in enable
- Auto-run enable
- Attempt trigger
- Counter/Timer inhibit

4. External Trigger Out:

- External trigger out duration
- External trigger out pulsed/latched

Trigger Source Select

The output of this section is a signal indicating a Trigger attempt. Inputs to this block include control bits from the Trigger-Processor Interface which (under user specification) enables GF OUT and CT OUT, as well as the Counter/Timer or the Global Filter to attempt a trigger.

A14U675 is a quad-OR/AND gate that generates (with a low at any input) the trigger attempt signal. Sequence triggering, since it is a complete command conditional on level, does not require a processor control line. Instead, the sequence trigger attempt is encoded as a simultaneous sequence step and reset. These low signals applied to the OR inputs A14U657-7 and -9 generate a trigger attempt.

The CT OUT(L) signal indicates the termination of the current Counter/Timer test. For triggering, the processor enable line is set low (A14U675-5), and A14U675-4 is low since the trigger has not occurred yet. When CT OUT(L) goes true low, the trigger attempt is propagated through the system. If a trigger is allowed by the Trigger Enable section, A14U675-4 is set high and the trigger attempt is cleared.

The GF OUT signal is processed much in the same way as the CT OUT(L) signal. The GF OUT signal is delayed with A14DL575 to line up with the CT OUT signal and the sequence trigger. It is important for trigger positioning to have triggers derived from the same input state, but routed through any of the three possible trigger paths (to obtain the same propagation delay). This allows the signal to arrive at the timebase circuitry at the same point (approximately) to correctly identify the input state causing the trigger.

The GF OUT signal is also differentiated in order to prevent locking up the system in the reset condition. This is done with A14U465B, inverting and delaying GF OUT(L) and then applying that signal to the other OR input at A14U675-11.

Reset Source Select

This section has a similar layout to the Trigger Select section. Additional inputs include the trigger attempt signal from A14U675, and processor control lines for reset on Counter/Timer, and reset on Global Filter. The output of this Reset Source Select section is a system RESET(H) signal, used as a general reset of the entire trigger system.

Sequence reset is decoded directly as a command in the sequence state machine, and therefore needs no processor control for enable. CT OUT and GF OUT function the same as for the Trigger Select section.

The trigger attempt signal is also used to force a system reset. This signal is applied directly as a command with no processor enable, the same way a sequence reset is applied since it is a direct command with no user intervention or selection.

RESET(L) is delayed slightly and gated with TRIG(H) to reset the Counter/Timer. This prevents resetting the Counter/Timer at a trigger, but allows it to be cleared otherwise.

Trigger Enable

The inputs to this section include the trigger attempt signal (active high) from A14U675, TRIG IN(H), TRIG EN(H), prefilled information, and a sequential control that enables triggers on each level. The output of this block is a TRIG bit that indicates the trigger has or has not occurred.

A14U570 implements an AND of the conditions required to trigger, and latches when those conditions occur due to the feedback from A14U570-2 into the OR inputs of the condition gates. A14U570-4 is the unlatch signal as well as a disable for trigger. The bit is set low under processor control for auto-run in continuous trigger out mode. In this mode, trigger attempts are applied to the Trigger Enable section, but the trigger signal can not go true. The external trigger out is still generated, however, the trigger system resets and continues.

TRIG IN(H), the external trigger arm mode signal, is applied when the 100 ns one-shot (A14U470A and B and U475) is enabled by asserting ETI OFF(H) false (low). This requires that a TRIG IN(H) pulse be received within the 100 ns window defined by the attempt trigger signal starting the one-shot (A14U470-4 is the trigger). The pulse width is set with A14R378 and C384. The output of the one-shot extends the attempt trigger signal through A14U570-14.

When the TRIG IN(H) signal is not enabled (A14U570-9 is high), if A14U570-12 is pulsed high with the attempt trigger signal after prefill is true (A14U545D-12 and -13 both low), and if the trigger enable on this level is true (A14U470-7 is low), the OR-AND is satisfied and latches TRIG(H) true.

External Trigger Out

The input to this section is the trigger attempt signal from A14U675, and control signals that enable and allow the latching process. The output is the external trigger out TRIG OUT(H) signal. The trigger out pulse width is set by the trigger in window timing circuit. The trigger in and trigger out circuits share the same latch. Therefore, if trigger in is set to latched mode, trigger out will also be latched.

The trigger attempt signal is applied to the set input of the the controllable latch (consisting of the gates in A14U475 and U470A). The latch happens from A14U470-2 to U475-12 to U470-5. In normal operation (external trigger out pulsed), A14U475C-10 senses the level on the timing circuit A14R380/C384 and clears the latch by lowering A14U470-5. In the latch mode (external trigger out latched), A14U475 is disabled from taking this action since A14U475C-10 is set high. The external trigger out is disabled when A14U475-7 is set high.

The external trigger loop (including the translation from ECL to TTL levels on the CRT Drive Board) takes approximately 40 ns depending upon the length of the coaxial cable used. This can be observed by running at 10 ns in the Auto mode with the External Trigger In connected to the External Trigger Out. The trigger position is proportional to the delay through the external loop.

DATA STORAGE CONTROL

Trigger Position Indicator Timebases 1 and 2 ◈11◈

The trigger position indicators, in conjunction with the trigger position prescalers, count the number of stored data samples. Since the 1240 can acquire data using two independent timebases (T1 and T2), a trigger position indicator exists for each. Data stored before the trigger point is called prefilled data, data stored subsequent to the trigger point is called postfilled data. The user can specify the amount of postfill data and when the specified amount has been stored, the trigger position circuitry shuts down the acquisition system. If the After Memory Full mode is selected, the trigger position circuitry also inhibits the Trigger Control circuits until the prefill section of the memory is filled. Once prefill is complete, the Trigger Control circuit is allowed to detect a trigger.

The upper 8-bit counters for Timebase 1 are A09U261 and U267; counters for Timebase 2 are A09U264 and U164. When both counters reach their terminal count, A09U236B (and U236D) generate a low TP1(L) and TP2(L) (to signal that the prefill is complete). The outputs of the high-order counters are to an 8-bit magnitude comparator A09U467 (and U367). Firmware sets the magnitude (depending on the postfill depth) for the comparator into an 8-bit register A09U464 (and U364). When the value of the counters matches the value in the register, the memory full signals MF1(L) and MF2(L) are generated.

Trigger Position 1 and 2 Prescalers and Timebase Shutdowns ◈20◈ ◈21◈

When the prefill count is reached, A14U260B (and U260A) latches, setting the preload on A14U165 (and U160). The timebase then waits for a trigger. The system requires approximately 35 ns to decide if a trigger has occurred. The Timebase T-clocks are delayed by approximately 38 ns, then they clock A14U565A and B. U565A and B sample the TRIG(L) signal from the Trigger Control block.

When a trigger is detected, A14U565A and B allow A14U160 and U165 (respectively) to begin counting the postfill. A14U160 (or U165) outputs the lower four bits of the 12-bit counter. The upper 8-bits of the counter reside on the Control Processor Board. Comparators A14U150A and B convert the ECL-level signals to TTL-levels to clock the upper 8-bit counters.

When both the Prescaler on the Trigger Board and the counters on the Control Processor Board reach their final count, then A14U265C (and U265B) goes high. On the next clock, the output of A14U255B (and U255A) goes low. On successive clocks, the flip-flop chain propagates the signal. The low-order counters A14U165 (and U160) begin their count from a non-zero value to compensate for this flip-flop chain. Eventually A14U645A (or U145B) shuts down the timebase via the timebase qualifier lines.

Since the T1 timebase can run at 10 ns, and the delay to A14U155B is approximately twice that time; T1 stores one more sample after the trigger than it stores at slower speeds.

When storage qualification is used,if the last sample is not storage qualified, then the timebase shuts down with one sample fewer than normal. The trigger, however, is correctly located positioned.

Timebases 1 and 2 ◈20◈ ◈21◈

The timebases control system start-ups, T2L/T2F alternations, storage of data on acquisition card, as well as generating delayed clocks for the Global and Sequential circuits. When the system is started, firmware raises the RUN(H) line to A14U450C. This is inverted and sent to the Q lines (Q1, Q2F, and Q2L). After a short delay, the clock receivers on the Trigger Board are enabled. This assures that the acquisition cards are ready to run when the Trigger Board begins.

When Timebase 2 is in the demux mode, A14U655B and U545B and C first enables Q2F. When a clock occurs on T2F, U655B flops setting Q2F high and Q2L low. Any future clocks on T2F are ignored. When a clock occurs on T2L, U655B flips back and future clocks on T2L are ignored while waiting for T2F.

Storage of data on the acquisition cards can be turned on or off for each level of the sequence word recognizer. Storage may also be qualified by the global word recognizer. The global word recognizer is combined with store on level by A14U560. Storage qualification is sampled by A14U460A (and U460B). Sampling on U460 is delayed from the bus clock to allow time for the global word recognizer to be set up.

The word recognizers require time to be generated on the acquisiton cards, combined on the Interface Board, then propagate to the Trigger Board. To compensate for the delay of the word recognizers, the T-clocks are delayed before they are sent to the global and sequential circuits. These clocks are not storage qualified, so they continue to run when the acquisition cards are storing no data.

Correlate Circuit ◈22◈

Correlation data is used by the Control Processor to determine the time alignment between the two timebases. When the Control Processor reads acquisition data from the storage RAMs, it also reads correlation data. The Correlate circuit (residing on the Trigger Board) generates the correlation data that is sent to the acquisition cards for storage in the RAMs.

The correlate circuitry produces one correlation data bit for each timebase (1 and 2). The correlate circuit is comprised of two sections: the correlate portion which produces the correlation data, and the pipe portion which synchronizes the correlation data with the acquisition cards.

In the correlate section, log-in registers A14U590B and U685A accept qualified clocks, QUAL CLK1(H) and 2(H), from the timebases. If the opposing timebase was clocked last, then the log-in register will load in a one (1). Otherwise, the log-in register is set to a zero (0). Also, if the opposing register was clocked last, then the AND gate (either A14U480C or U480D) admits a delayed version of QUAL CLK to A14U485A. U485A tracks which timebase was clocked last.

The pipe section accepts the outputs of the log-in registers. A delayed store pulse is sent to clock the pipe when receiving data from the log-in registers. Timebase 1 also requires a second stage of pipe (that operates from a earlier clock) to provide for proper correlation data setup time when running at 10 ns. A14U590A is used during the 10 ns timebase.

Firmware retrieves the data from the correlation pipeline through a combination of direct readback in the CORR RB signals, and through clocking Timebase 1 to read back A14U485A and U590B.

SUPPLEMENTAL CIRCUIT BLOCKS

Trigger-Processor Interface (26)

The processor interface provides data transfer control from the Control Processor to the trigger circuitry. The Processor Interface block includes circuitry to pre-program the functional blocks on the Trigger Board, monitor the status of the trigger during an acquisition cycle and read back the trigger position indicators.

The trigger-processor interface consists of three basic sections: Bus Interface, Readback, and Control. The following lists these sections and their functions:

1. Bus Interface:

- Register decode
- Bidirectional data buffering

2. Readback:

- Register Segmentation
- Level Conversion and buffering

3. Control:

- Static register segmentation
- ECL RAM interface and segmentation
- ECL interfacing

Bus Interface

Inputs to this section include the register address lines and data lines from the Control Processor bus: CA0-CA2, CWR, CRD, IBS0, and CD0(H)-CD7(H). The Trigger side of the interface has a buffered version of the Control Procesor data bus, BCD0(H)-BCD7(H) and strobes for read and write registers.

The eight possible read and write locations are divided into: five static write locations and three ECL RAM locations by A14U495 (a one-of-eight select), and four static read locations, and two control/initialization strobes with A14U395 (also a one-of-eight select).

The data bus is buffered with A14U295 when this card is selected for a read or write operation. CRD(L) controls the direction of this buffer. The pull-up resistors on the BCD0(H)-BCD7(H) lines are required for interfacing the TTL with CMOS parts (such as the ones used for static control registers).

Readback

Internal data is readback on the BCD internal bus using quad comparators A14U110, U210, U270, U275, U280, U285, and U290. These comparators are reference to the ECL threshold voltage used on this board (3.65 volts approximately). Inputs consist of the data required for control and data display.

Control

The control registers receive data from the BCD bus on strobes, 0-4. The CMOS octal registers are A14U170, U175, U180, U185, and U190. The functions of the control are described in the appropriate block descriptions.

The ECL RAM is loaded four bits at a time from the BCD bus. There are three functional registers, two of which are eight bits wide. A static control bit, RAM LOW(L), is used to differentiate loading into the high or low segment of these registers. The sequence pointer is used to cycle through the RAM while it is being loaded.

Asynchronous Timebase (670-5725-04) ◈19◈

This circuitry, located on the Display Board (assembly A11), generates acquisition clocks on timebase T1 at rates from 10 ns to 1 second in a 1-2-5 sequence. It also generates a 10 ns clock used by the global filter and counter/timer circuitry.

Components A11U545C, D and their associated passive components form a 100 MHz oscillator. This is the 10 ns asynchronous timebase sample rate. A11U450B, configured as a divide-by-two, produces a 20 ns sample rate. A11U455 is configured to produce a divide-by-five count and a divide-by-ten count. A11U465 selects the high speed clock rate to be either 10, 20, 50, or 100 ns. The firmware can select any of the four rates, or a logic high, or a logic low, through control of the P0(H)-P2(H) lines. A logic low is selected with a value of 4 or 6 on P0(H)-P2(H); a logic high is selected with a value of 5 or 7.

The output of multiplexer A11U465 is therefore a clock of period 10, 20, 50, or 100 ns, or a processor-derived rate determined by the firmware when it alternately selects a logic high and then a logic low.

A divide-by-ten prescaler, A11U565, produces output periods from 200 ns to 1 μs. A11U498B converts the ECL-level signals to TTL-level signals. The TTL counters, A11U580-590, are each configured to divide the signal frequency by a factor of ten. The final counter, A11U590B, produces a clock rate from 200 ms to 1 second. Multiplexer A11U570 selects the final output clock rate, while A11U475C, D, and the associated passive components form a pulse generator. This generator produces a 4 ns pulse width (approximately) for the output clock regardless of the rate selected. The clock pulse is ORed onto Timebase 1 by circuitry located on the Interface Board.

Asynchronous Timebase (670-5725-03) ◈19◈

This circuitry, located on the Display Board (assembly A11), generates acquisition clocks on timebase T1 at rates from 10 ns to 1 second in a 1-2-5 sequence. It also generates a 10 ns clock used by the global filter and counter/timer circuitry.

Components A11U545C, D and their associated passive components form a 100 MHz oscillator. This is the 10 ns asynchronous timebase sample rate. A11U450B, configured as a divide-by-two, produces a 20 ns sample rate (on A11J460-3). A11U455 is configured to produce a divide-by-five count (on J460-4) and a divide-by-ten count (on J460-7). A11U465 selects the high speed clock rate to be either 10, 20, 50, or 100 ns. The firmware can select any of the four rates, or a logic high, or a logic low, through control of the P0(H)-P2(H) lines. A logic low is selected with a value of 4 or 6 on P0(H)-P2(H); a logic high is selected with a value of 5 or 7.

The output of multiplexer A11U465 is therefore a clock of period 10, 20, 50, or 100 ns, or a processor-derived rate determined by the firmware when it alternately selects a logic high and then a logic low.

A divide-by-ten prescaler, A11U565, produces output periods from 200 ns to 1 μs. A11U498B converts the ECL-level signals to TTL-level signals. The TTL counters, A11U580-590, are each configured to divide the signal frequency by a factor of ten. The final counter, A11U590B, produces a clock rate from 200 ms to 1 second. Multiplexer A11U570 selects the final output clock rate, while A11U475C, D, and the associated passive components form a pulse generator. This generator produces a 4 ns pulse width (approximately) for the output clock regardless of the rate selected. The clock pulse is O'Red onto Timebase 1 by circuitry located on the Interface Board.

Test Pattern Generator ◈27◈

This circuitry has two output connectors that supply stimulus patterns for diagnostic testing and application learning examples. Each TPG output at A14J620 and J630 consists of nine data lines, one clock/qualifier line, and two ground lines. The test pattern generator outputs a different 9-bit word, 63-word-long pattern at each connector. (For a listing of outputs available from the test pattern generator, refer to the *Operating Information* section of this manual.) Table 4-4 summarizes the characteristics of the available patterns.

Table 4-4
PATTERNS AVAILABLE FOR OUTPUT BY THE TEST PATTERN GENERATOR

Pattern Number	With Glitches	Clocked At
0	No	12 MHz
1	Yes	6 MHz
2	No	T1
3	Yes	T1/2

The patterns, numbered 0 through 3, allow timebase selection (T1 or 12 MHz) and Glitch ON or OFF selection. If Glitch ON is selected, the timebase rate is divided by two and a narrow temporary inversion of the data is forced halfway through each TPG output clock cycle.

A 12 MHz oscillator consists of A14Y614, U615B and C, and the surrounding passive components. This 12 MHz base clock rate is applied to the dual 4-to-1 multiplexer A14U520. This multiplexer selects between the four possible TPG clock selections: T1, T1/2, 12 MHz, and 6 MHz. Multiplexer outputs are to a divide-by-two, A14U515B, and an output pulse width controller, A14U515A and DL510. If select TPG T1(H) is active high (A14U520-9), then multiplexer inputs 2 and 3 (U520-4, 10, and 12) for each section become the selected inputs. Conversely, when it is inactive low, inputs 0 and 1 become the selected inputs. When select TPG GL(H) is active high, multiplexer inputs 0 and 2 are selected; when low, inputs 1 and 3 are the selected inputs. In addition, TPG GL(H) selects the divide-by-two, U515B, which divides the TPG output frequency in half. The positive transition of U515-14 is used to trigger the one-shot A15U515A; the negative transition triggers the one-shot A14U615A which inverts the output data for the period of that one-shot.

The period of the output clock, ACK(H), is established through the delay difference between the the clock to U515A-6 and the set input pin 5. Repositioning jumper A14J510 between 6 ns and 10 ns changes the pulse width of the output clock from 8 ns to 12 ns. A14R510 is used as a fine adjust due to signal integrity and component deviations. The data versus clock-time delay is adjusted by positioning jumper A14J514 and R610 to change delay in the output clock path. Jumper A14J615 is used to provide complementary clock outputs on the two TPG connectors, A14J620 and J630.

The output data is a pseudo-random binary sequence that is created by the six-bit shift register, A16U620, with the data into the register being the binary sum of bits 0 and 5. The initial state is 11 1111. A14U625 is a Hex EXOR with a common input used to switch from buffer to inverter (for glitch generation).

SECTION 5 VERIFICATION AND ADJUSTMENT PROCEDURES

SECTION 5 VERIFICATION AND ADJUSTMENT PROCEDURES

TABLE OF CONTENTS (cont.)

VERIFICATION AND ADJUSTMENT PROCEDURES

INTRODUCTION

This section contains three main parts: *Functional Check Procedures, Performance Verification Procedures,* and *Adjustment Procedures.* These parts, along with the setup information supplied in the beginning of this section, should allow a qualified technician to adjust and verify proper operation for any configuration of the 1240.

Functional Check Procedures. These procedures may be used as a form of incoming inspection to verify that the instrument is operational.

Performance Verification Procedures. These procedures should be performed by a service technician for a detailed check of the product characteristics. All specifications listed in the performance requirements column of the *Specifications* section are verified. These checks may be extensive and time consuming. Under normal circumstances, the *Functionality Checks* within these *Performance Verification Procedures* provide an adequate test of product performance in a less costly, less time consuming manner.

Adjustment Procedures. These procedures describe the steps used by a technician for adjusting the 1240 to meet product specifications. If the instrument does not meet the product specifications, repair is necessary.

Table 5-1
REQUIRED TEST EQUIPMENT

Equipment	Specification	Equivalent Tektronix Instrument Or Part
Two-channel oscilloscope with two 1-meter probes	300 MHz	485 with two P6106's
Acquisition Probes with short lead set,two grounds		P6460
High Voltage Probe	20 kV max.	P6015
Universal Counter/Timer with 5X probe	200 MHz	DC 5010 w/P6125
Digital Multimeter	4.5 digit, 0.05% dc volts accuracy	DM 501A
Pulse Generator	250 MHz pulse rate, variable output levels	PG 502
Mainframe (optional) for TM5000 equipment	6 plug-in compartments	TM 5006

Table 5-1 (cont.)
REQUIRED TEST EQUIPMENT

Equipment	Specification	Equivalent Tektronix Instrument Or Part
Variable Transformer	500 VA, 5A sec., 50 - 117%	
Video Monitor	RS-170 compatible	
Service Maintenance Kit		Tektronix P/N 067-1103-01
Setup/Hold Time Test Fixture w/ lead sets; 8 inch cable		Tektronix P/N 067-1037-00
Coaxial Cables, 50 Ω		
	8 inch	Tektronix P/N 012-0118-00
	10 inch	Tektronix P/N 012-0208-00
	20 inch	Tektronix P/N 012-0076-00
	3 foot	Tektronix P/N 012-0482-00
50 Ω Termination		Tektronix P/N 011-0049-01
BNC DC Block		Tektronix P/N 015-0221-00
BNC Probe Adapter		Tektronix P/N 013-0084-00
BNC T-Connector		Tektronix P/N 103-0030-00
BNC Female-to-Female		Tektronix P/N 103-0028-00
Adjustment Tool (hex and slot heads)		Tektronix P/N 003-0301-00
Dual Lead Adaptor (scope probe accessory)		Tektronix P/N 015-0325-00
Acquisition Threshold Fixture	See V & A section for quantities; consists of:	
	Terminal Conn. Holder	Tektronix P/N 352-0484-00
	Mini PV Female Conn.	Tektronix P/N 131-0707-00
	resistor, 10.5 K ohm, 1%	Tektronix P/N 321-0291-00
	26-gauge wire	

Table 5-1 (cont.)
REQUIRED TEST EQUIPMENT

Equipment	Specification	Equivalent Tektronix Instrument Or Part
Threshold Accuracy Fixture	Consists of:	
	BNC Connector (one)	Tektronix P/N 131-0602-00
	Terminal Lugs (two)	Tektronix P/N 210-0255-00
	BNC Nut (one)	Tektronix P/N 210-0413-00
	1 μf ceramic cap. (one)	Tektronix P/N 283-0177-00
	12 square pin set; 2 rows, 6 pins per row	Tektronix P/N 131-2230-00
C/Q Connection Fixture	Consists of:	
	BNC Connector (one)	Tektronix P/N 131-1847-00
	Terminal Lugs (one)	Tektronix P/N 210-0255-00
	BNC Nut (one)	Tektronix P/N 210-0413-00
	5 square pin set (one)	Tektronix P/N 131-1614-00
Data Communications Tester (For testing RS232 COMM packs)		834
Self-Test Adapter (For testing RS-232 COMM packs)		Tektronix P/N 013-0173-01
Graphics Terminal (For testing GPIB COMM packs)		Tektronix 4051
Spare GPIB COMM Pack (For testing GPIB COMM packs)		Tektronix 1200C02 GPIB COMM Pack

USING THE 1240 EXTENDER BOARDS

The 1240 Service Maintenance Kit contains two extender boards that are used in the troubleshooting, adjustment, and performance verification procedures. The first board, assembly A21, should be used when working with the trigger, display, and both processor boards. The second board, assembly A22, should be used with the 9- and 18-channel acquisition boards. Both extenders allow a board under test to be at a convenient position away from the other boards so the signal test points and components are accessible.

NOTE

In some instances, either extender board will degrade system performance. For complete details, refer to the timing limitations in the Specifications *section of this manual and the instruction sheet that accompanies each extender board.*

OPERATING THE 1240 IN THE SERVICE POSITION

When operating the 1240 in the service position (the card cage rolled up to expose plug-in boards), some guidelines should be observed. The following subsections deal with concerns that arise during 1240 servicing procedures.

WARNING

After removal of the rear panel, the cooling fan blades are not completely shielded. Guard against injury by keeping fingers and loose objects away from the moving fan blades.

PROPER COOLING OF THE 1240

CAUTION

DO NOT operate the instrument with the cabinet removed for extended periods of time unless it is raised off the working surface at least one-half inch.

If it is necessary to run the 1240 for extended periods of time, raising the instrument admits air to the power supply for cooling purposes. Additionally, another fan should be positioned to blow air onto the instrument bulkhead just below the card cage (when the card cage is rolled into the service position). This additional air supply should particularly be aimed at the power supply heat sink, located on the bottom of the bulkhead.

When operating the 1240 in the service position, the rear panel fan does not provide adequate cooling for some boards installed on an extender board. To circumvent this problem, a fan should be positioned to blow air across these extended boards. The boards that require additional cooling are:

- any 9-Channel Acquisition Boards
- any 18-Channel Acquisition Boards
- the Trigger Board

TIMING LIMITATIONS

In some instances, either extender board will degrade system performance. For complete details, refer to the timing limitations in the Specifications section of this manual and the instruction sheet that accompanies each extender board.

CONSTRUCTING AN ACQUISITION THRESHOLD FIXTURE

The acquisition threshold fixture shown in Figure 5-1 should be used when checking and adjusting the threshold setting on the 9- and 18-channel acquisition boards. The fixture is also required for the *Procedure 3: Threshold Functionality Check*. The part numbers for the following materials are listed in *Table 5-1, Required Test Equipment*.

Equipment Required

- one Terminal Connector Holder, (2 holes x 8 holes)
- five Mini PV Female Connectors
- one resistor, 10.5 K ohm, 1%
- three 26-gauge wires, each approx. 1 inch long

Build Procedure

1. Connect three of the Mini PV connectors to the three lengths of wire.
2. Connect the remaining two Mini PV connectors to the resistor, one at each end.
3. Install the three wire/Mini PV connector combinations into holes 1, 4, and 7 of the Terminal Holder Connector. Refer to Figure 5-1.
4. Solder the three free ends of the wires together.
5. Install the two ends of the resistor/Mini PV connector combinations in holes 13 and 16 of the Terminal Connector Holder.

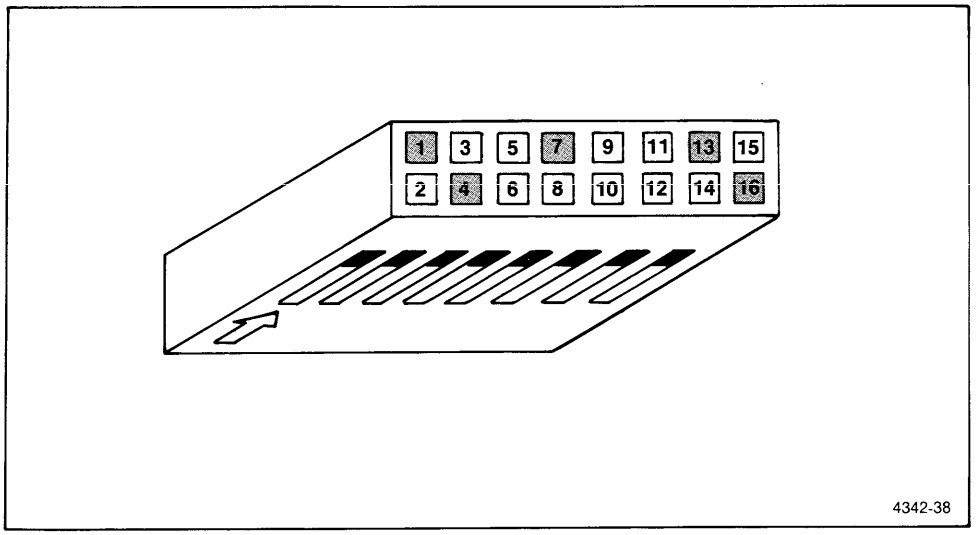


Figure 5-1. Acquisition threshold adjust fixture.

FUNCTIONAL CHECK PROCEDURES

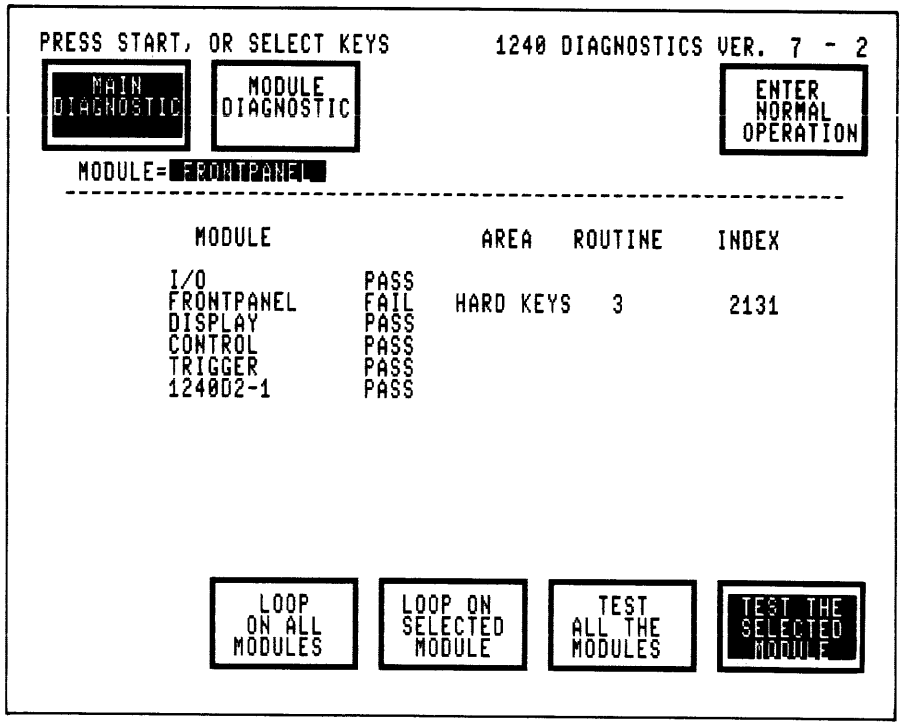
INTRODUCTION

The Functional Check Procedures are a limited number of quick tests that an operator can perform as an incoming inspection. These procedures provide a check of the 1240 operational status in a less costly and less time consuming manner than the *Functionality Checks* in the *Performance Verification Procedures* part of this section.

(1) INTERNAL DIAGNOSTIC FUNCTIONAL CHECK PROCEDURE

These diagnostic checks are limited to diagnostic tests that reside internally in the 1240. The tests verify major 1240 functions, but only a small part of the trigger and acquisition circuitry. For more extensive diagnostic testing using the Diagnostic ROM pack, refer to the *Functionality Checks* in the *Performance Verification Procedures* part of this section.

1. To access the diagnostic tests, hold down any front panel key while powering ON the 1240. Note that the tests initially indicate a keyboard failure due to the key being held down. Refer to Figure 5-2 for a typical power-up display. Note that some modules (e.g., COMMPACK or ROMPACK) may not be displayed depending upon the configuration of the instrument.
2. While in the Main Diagnostic menu, touch the TEST ALL MODULES soft key.
3. Press the front panel START key to begin testing. When testing is completed, the diagnostics will report the operational status with PASS and FAIL messages.



4342-39

Figure 5-2. Typical diagnostic power-up display.

(2) FRONT PANEL FUNCTIONAL CHECK PROCEDURE

1. While in the Main Diagnostic menu, select the FRONTPANEL module. Touch the Module Diagnostic soft key and select the FP VERIFY area. Touch the Area Diagnostic soft key and select 1 for the routine number.
2. Press the START key. The 1240 should produce a screen display similar that shown in Figure 5-3.
3. Check the keyboard-key action by pressing one key at a time and verifying that the corresponding screen key disappears and then returns when the key is released. (Remember that pressing the STOP key causes the test to end.)
4. Check the rotary knob. The asterisk should move on the circle in the same direction as the knob and the count in the center of the circle should be equal to 200 ±8 counts (between C0 and D0 in hex) for one full knob revolution.
5. Press the front panel STOP key.

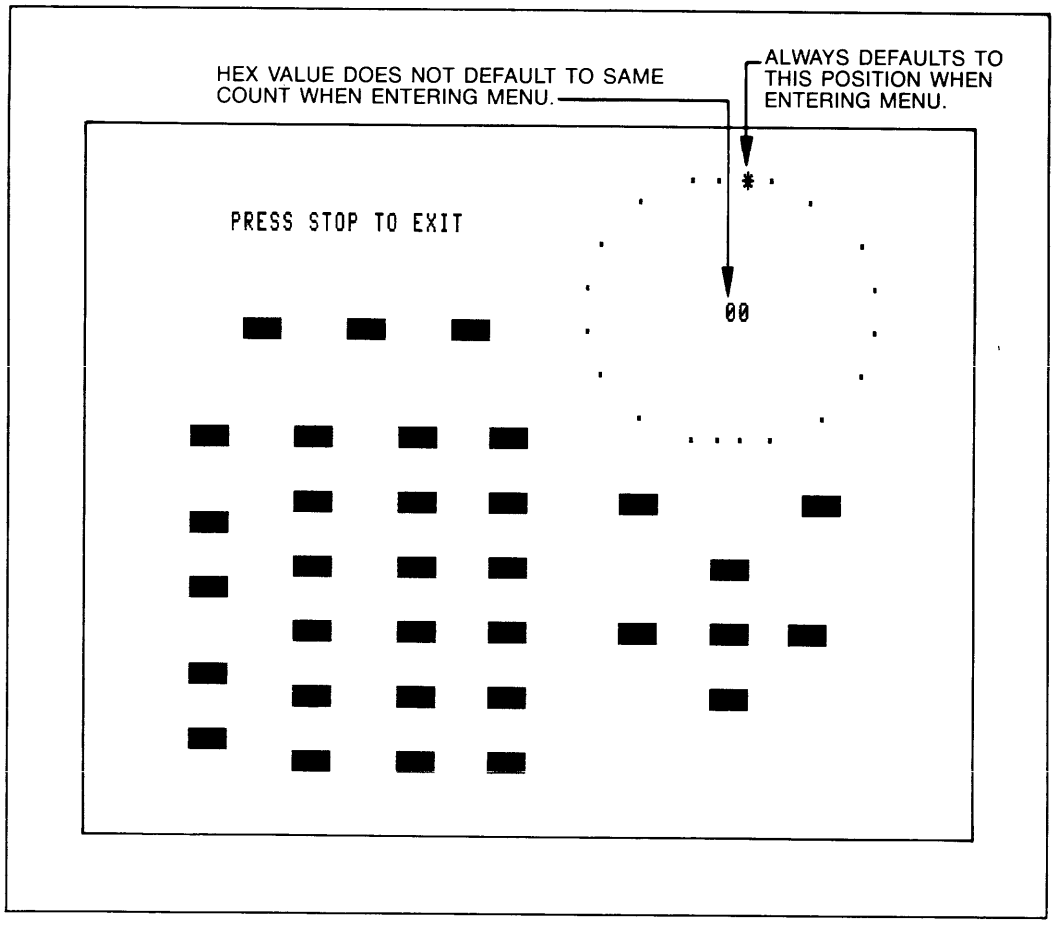


Figure 5-3. Front panel keyboard manual test display.

(4) RS-232 COMM PACK FUNCTIONAL CHECK PROCEDURE

This is an optional check procedure intended for use with 1200C01 COMM Packs. Equipment required to complete this check includes a Tektronix 834 Programmable Data Communications Tester.

The Bit Error Rate Tests (BERT), when performed with an 834, provide a check of the RS232 data communications link. During these tests, the 834 accumulates error information that identifies communication link failures. When the tests are complete, test results stored in the 834 may be examined to determine the operational status of the communication link. (The 1240 does not report any errors during this manual test.) For a more detailed explanation of the tests, refer to the RS-232 COMM Pack Manual Test in section 8.

1240 Setup For BERT Testing

Program the 1240 menus as follows:

1. Power down the 1240 and install an RS232 COMM pack in the door-covered slot on the rear of the instrument.
2. Power up the 1240 and enter diagnostics by simulating a keyboard failure (hold down a key during power-up).
3. Using the SELECT keys or the KNOB, choose the COMMPACK module and touch the MODULE DIAGNOSTIC soft key.
4. Choose the MANUAL area and touch the AREA DIAGNOSTICS soft key.
5. Press the START key and set the desired baud rate (50 to 9600 baud).

834 Setup For BERT Testing

Set up the 834 as follows:

1. Remove the interconnect cable and jumper wires from the 834 storage compartment (bottom of the 834).
2. Open switches 2 and 3 on the Interface Access panel; all other switches should be closed.
3. Using the jumper wires, connect pin 2 of the Interface Access panel to the pin labeled RXD, then connect pin 3 to TXD.
4. Connect the male end of the interconnect cable to the 834, then connect the female end of the cable to the 1240 RS232 COMM pack.
5. Power on the 834.
6. Turn the MODE switch to BERT, then press the SETUP key.
7. Using the left- or right-arrow keys, select the same baud rate (50 to 9600 baud) as previously set in the 1240 menu.
8. Press the down-arrow twice. Select the test length (in total bits received per test) with the left- or right-arrow keys according to your testing needs:
   - 10E5: 100,000 bits
   - 10E6: 1,000,000 bits
   - CONT: continuous testing for intermittent failures until STOP is pressed

9. Press the down-arrow key once, then select ASYNC (with the left- or right-arrow keys).
10. Press the down-arrow key once, then select BITS/CHR=8.
11. Press the down-arrow key once, then select PARITY=EVEN.
12. Press the down-arrow key once, then select STOPBITS=2.
13. Press the START key.

BERT Test Results

The BERT test is now running. Check that the 834's NO SYN LED is not lighted. Using the up- and down-arrow keys, you can examine bit errors, block errors, blocks, and faults. The number of tested blocks will increment while the test is running. No bit errors, block errors, or faults should occur.

When testing is complete, the 834 displays BERT TEST DONE. Note, however, that this does not indicate the tests have passed. To review the test results, press the DATA key and use the up- or down-arrow keys. There should be no errors.

(5) GPIB COMM PACK FUNCTIONAL CHECK PROCEDURE

This is an optional check procedure intended for use with 1200C02 COMM Packs. Equipment required to complete this check includes a Tektronix 4051 Graphic Terminal.

The procedure first verifys that a spare 1200C02 is functioning properly. Then, this COMM pack is used in setting up the 1240 menus to test the suspect 1200C02 GPIB COMM pack.

1. Power down the 1240 and install a known-good 1200C02 GPIB COMM pack in the door-covered slot on the rear of the instrument.
2. Power up the 1240. When power-up diagnostics are completed, verify that a PASS condition is displayed for the COMMPACK module.
3. Press the UTILITY menu key and touch the COMM PORT CONTROL soft key.
4. Move the cursor to the GPIB PORT STATUS field and select OFFLINE.
5. Move the cursor to 1240'S GPIB ADDRESS field and select 01.
6. Move the cursor to the MESSAGE TERMINATION field and select EOI.
7. Move the cursor back to the GPIB PORT STATUS field and select ONLINE.
8. Turn the 1240 OFF and remove the known-good COMM pack.

4051 Setup

1. Connect a GPIB cable to the rear panel of the 4051.
2. Turn on the 4051 and load the test program given in Table 5-1a into the 4051. (If this test program will be used often, store the contents on magnetic tape to avoid re-entering the program.)

GPIB Functional Test

1. With the 1240 power OFF, install the suspect 1200C02 GPIB COMM pack and connect the GPIB cable from the 4051 to the GPIB connector on the pack.
2. Start the test program running. The 4051 should prompt you to enter a GPIB address for the 1240. Enter a 1 followed by a Carriage Return for the GPIB address.
3. After the 4051 prompts you, turn the 1240 power ON.
4. When the 1240 has finished the power-up diagnostics, the 4051 should poll the GPIB port and print the message POWER ON on the 4051 display screen.
5. Press User Definable Key (UDK) #1 on the 4051. The 4051 will indicate the GPIB test has begun by printing periods (20, one at a time) on the second line of the 4051 screen. While the test is running, the 1240 screen should be blank from the second line down (the first line displays the message REMOTE WITH LOCKOUT). The two GPIB status LED's on the COMM pack should be flashing, the NRFD LED flashing twice as fast as the NDAC LED.
6. When the test is complete, the 4051 prints a 1240 identification message and a TEST COMPLETE message on its display screen. Any failures will also be detailed at this time.
7. Press the 1240's UTILITY menu key and touch the COMM PORT CONTROL soft key. The first line in this menu should indicate the 1240 is in LOCAL mode.
8. Turn the 1240 OFF, disconnect the GPIB cable from the pack, and remove the tested COMM pack.

Table 5-1a
4051 PROGRAM FOR 1200C02 COMM PACK TEST

```
1 REM *** 1240 GPIB CHECKOUT PROGRAM ***
2 GO TO 100
3 REM *** UDK #1 GPIB/LED CHECKOUT ***
4 GOSUB 1000
5 RETURN
7 REM *** UDK #2 PRINT INSTRUCTIONS TO DISPLAY ***
8 GOSUB 4000
10 RETURN
11 REM *** UDK #3 PRINT INSTRUMENT IDENTIFICATION ***
12 GOSUB 3000
13 PRINT I$
14 RETURN
38 REM *** UDK #10 RUN PROGRAM ***
40 RUN 100
100 PAGE
120 PRINT "1240 GPIB CHECKOUT PROGRAM V2.0"
130 PRINT "****************************************"
140 PRINT
150 PRINT "USE USER DEFINED KEYS TO INITIATE TESTS"
160 PRINT "----------------------------------------"
170 PRINT
180 PRINT "UDK #1 - GPIB/LED CHECKOUT SEQUENCE"
190 PRINT "UDK #2 - TEST SETUP AND PROCEDURE OUTLINE"
200 PRINT "UDK #3 - PRINT INSTRUMENT ID"
```

Table 5-1a (cont.)
4051 PROGRAM FOR 1200C02 COMM PACK TEST

```
210 PRINT
220 PRINT
230 PRINT "ENTER ADDRESS FOR 1240: ";
240 INPUT D1
250 ON SRQ THEN 2010
260 PRINT
270 PRINT "PLEASE TURN ON THE 1240"
280 SET KEY
290 WAIT
300 END
1000 REM ***** CHECKOUT IEEE 488 INTERFACE *****
1010 ON SRQ THEN 2010
1020 PAGE
1030 PRINT "*****GGG IF BUS HANGS THEN FAILURE SHOULD BE ASSUMEDGGG*****"
1040 WBYTE @17:
1050 FOR I=1 TO 35
1060 WBYTE @D1+64:
1070 RBYTE X
1080 X=ABS(X)
1090 IF X<>255 THEN 1210
1100 PRINT ". ";
1110 GOSUB 3000
1120 GO TO 1130
1130 NEXT I
1140 PRINT
1150 PRINT "JJ" ,I$, "JJ"
1160 PRINT "GGGGTEST COMPLETED"
1170 WBYTE @95:
1180 WBYTE @1:
1190 ON SRQ THEN 2010
1200 RETURN
1210 PRINT
1220 PRINT "GGGFAILURE - DATA LINES NOT CORRECT GGG"
1230 PRINT "DAB SHOULD BE: 255 INSTEAD OF : ";X
1240 RETURN
2000 REM *** SRQ HANDLERS ***
2010 POLL A,B;D1
2020 POLL A1,B1;D1
2030 IF B1=B THEN 2250
2040 IF B<>65 THEN 2070
2050 PRINT "POWER ON"
2060 GO TO 2230
2070 IF B<>97 THEN 2100
2080 PRINT "COMMAND ERROR"
2090 GO TO 2200
2100 IF B<>98 THEN 2130
2110 PRINT "EXECUTION ERROR"
2120 GO TO 2200
2130 IF B<>99 THEN 2160
2140 PRINT "SYSTEMS ERROR"
```

Table 5-1a (cont.)
4051 PROGRAM FOR 1200C02 COMM PACK TEST

```
2150 GO TO 2200
2160 IF B<>101 THEN 2190
2170 PRINT "POD CHECK"
2180 GO TO 2230
2190 PRINT "SRQ: ";B;
2200 RETURN
2210 INPUT @D1:E$
2220 PRINT " ";A$
2230 ON SRQ THEN 2010
2240 RETURN
2250 PRINT "GGGGINTERRUPT FAILURE"
2260 PRINT "CHECK GPIB INTERUPT PATH - CHECK INTERRUPT MUX PIN #4"
2270 D1=5
2280 GO TO 2010
3000 REM *** IDENTIFICATION TEST ***
3010 PRINT @D1:"ID?"
3020 INPUT @D1:I$
3030 H$=SEG(I$,1,11)
3040 K$="ID TEK/1240"
3050 IF H$=K$ THEN 3070
3060 PRINT "NOT A WORKING 1240GGGG!"
3070 RETURN
4000 REM *** GPIB TEST INSTRUCTIONS ***
4010 PAGE
4020 PRINT " 1240 GPIB CHECKOUT PROGRAM VERSION 2.0"
4030 PRINT "****************************************"
4040 PRINT "J 1) TURN 1240 ON."
4050 PRINT " 2) WAIT FOR DIAGNOSTICS."
4060 PRINT "J 3) SET COMM PORT PARAMETERS AS FOLLOWS:"
4070 PRINT " (if already set up then go to step #4)"
4080 PRINT "J A) Enter ""UTILITY"" menu."
4090 PRINT " B) Enter ""COMM PORT CONTROL"" sub-menu."
4100 PRINT " C) Select ""OFFLINE"" port status."
4110 PRINT " D) Select GPIB ADDRESS ""';D1;"".""
4120 PRINT " E) Select ""ONLINE"" port status."
4130 PRINT "J 4) PRESS ""UDK #1"" (GPIB TEST) ON 4051."
4140 PRINT "J 5) LOOK FOR THE FOLLOWING RESULTS DURING THE TEST:"
4150 PRINT "J A) Screen blanks."
4160 PRINT " B) Top line says ""REMOTE WITH LOCKOUT"".""
4170 PRINT " C) Both LED's on COMM PACK flash."
4180 PRINT " D) The ""NRFD"" LED flashes twice as fast as"
4190 PRINT " the ""NDAC""LED."
4200 PRINT " E) The 4051 display draws a dotted line."
4210 PRINT "J 6) LOOK FOR THE FOLLOWING RESULTS WHEN THE TEST IS DONE:"
4220 PRINT "J A) the 4051 prints the 1240's ID message."
4230 PRINT " B) The 4051 prints ""TEST COMPLETED"".""
4240 PRINT " C) The 1240 ""COMM PORT CONTROL"" sub-menu is displayed."
4250 PRINT " D) The top line of the 1240 display says ""LOCAL"".""
4260 RETURN
```

(3) SOFT KEY FUNCTIONAL CHECK PROCEDURE

1. While in the Main Diagnostic menu, select the FRONTPANEL module. Touch the Module Diagnostic soft key and select the FP VERIFY area. Touch the Area Diagnostic soft key and select 2 for the routine number.
2. Press the START key. The soft keys are represented as boxes on the 1240 screen. As you touch each soft key, check that the soft key becomes activated and that a buzzer sounds. Refer to Figure 5-4.

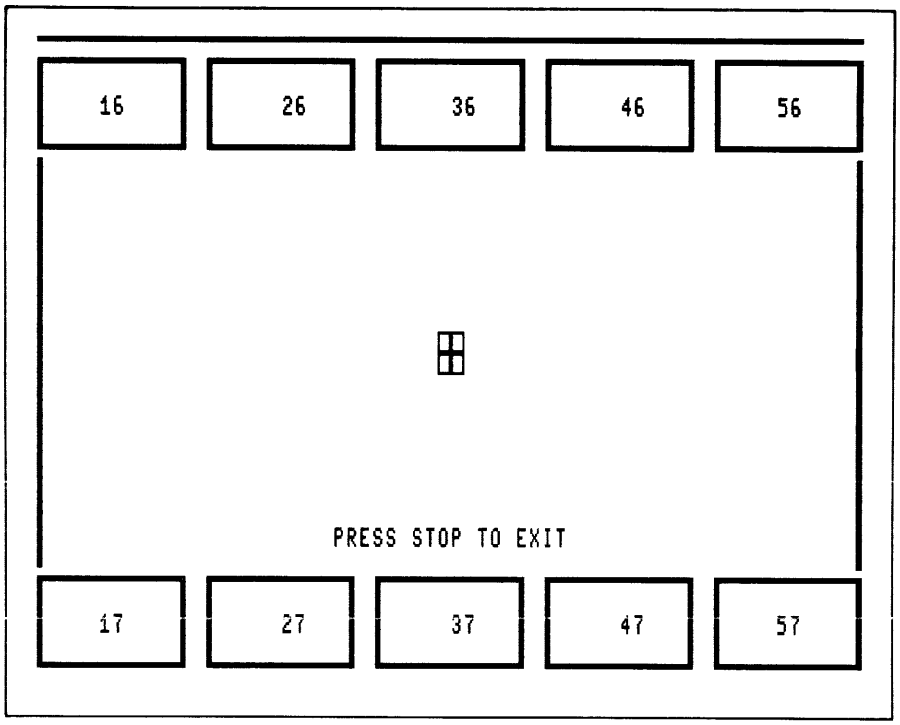


Figure 5-4. Soft key adjustment pattern.

PERFORMANCE VERIFICATION PROCEDURES

INTRODUCTION

These procedures contain checks on specifications listed in the performance requirements column of the *Specifications* section. Items listed in the performance requirements columns are specifications that the instrument must meet. If verification of the listed electrical specifications is required for incoming inspection or other purposes, perform the appropriate procedures outlined in this portion of the *Verification and Adjustments* section.

The Performance Verification Procedures consist of three main parts, *Part 1: Supply And TPG Checks*, *Part 2: Functionality Checks,* and *Part 3: Acquisition And System Performance Checks.* Parts 1 and 3 do not require a Diagnostic ROM pack to be available for use during the performance tests. Use both of these parts for verification of specifications listed in the Performance Requirements column. If, however, the Diagnostic ROM pack is available, *Part 2: Functionality Checks* should be performed in addition to these checks. These Functionality Checks instruct the user to run diagnostic tests that reside externally in the Diagnostic ROM pack. These diagnostic tests, along with other tests, provide a functional verification of approximately 95% of the 1240 circuitry. The test results aid in showing the operational status of the instrument as a system.

PART 1: SUPPLY AND TPG PERFORMANCE CHECKS

The checks outlined in Table 5-2 provide testing of performance specifications listed in the performance requirements column of the *Specifications* section. The tests do not require the use of the Diagnostic ROM pack. If a thorough check of all specifications is necessary, also complete in order the *Part 2: Functionality Checks* (a Diagnostic ROM pack is required) and *Part 3: Acquisition And System Performance Checks* (no ROM pack required). If a procedure has more than one part (e.g., 1A and 1B), perform all parts of the procedure.

NOTE

The specifications tested during these part 1 checks must be within tolerance for this instrument to operate properly. It is therefore recommended that the part 1 checks be performed before the Part 2: Functionality Checks and *the Part 3: Acquisition And System Performance Checks.*

Table 5-2
SPECIFICATIONS TESTED IN THE PART 1 PERFORMANCE CHECKS

NAME	VALUE	T.P. #	CHECK #
POWER			
+13 V *	+12.1 V to +12.9 V 0.5 V p-p max.	A8J658-1	Procedure 1
+12.1 V **	+11.4 V to +12.6 V 1 V p-p max.	A8J658-1	Procedure 1
+12 V	+11.4 V to +12.6 V 1 V p-p max.	A8J658-2	Procedure 1
+5 V	+4.85 V to +5.15 V 100 mV p-p max.	A8J658-3	Procedure 1
+3 V	−1.90 V to −2.10 V (ref. to +5 V) 100 mV p-p max.	A8J658-4	Procedure 1
−5 V	−4.75 V to −5.25 V 200 mV p-p max.	A8J658-5	Procedure 1
−12 V	−11.40 V to −12.60 V 1 V p-p max.	A8J658-6	Procedure 1
GND	0.00 V	A8J658-7	Procedure 1
DISPLAY			
High Voltage	10 kV ± 0.5 kV	Anode cup	Procedure 2
TEST PATTERN GEN.			
Clock Period	83.3 ns ± 2%	A14J620-1	Procedure 3A
Pulse Width	12 ns ± 0.5 ns	A14J620-1	Procedure 3B
Amplitude (Vout)	± 350 mV min. about V th. V th = +5V (meas) − 1.30 V. Nominal V th = 3.70 V.	TPG data pins	Procedure 3C
Glitch Width	6.5 ns ± 1.0 ns	TPG data pins	Procedure 3D
Delay, clock - data	1 ns ± 1.50 ns max.	TPG data pins	Procedure 3D

* For instruments with serial numbers B080000 and above.
** For instruments with serial numbers B079999 and below.

PROCEDURE 1: POWER SUPPLY PERFORMANCE CHECK

Test Point Locations

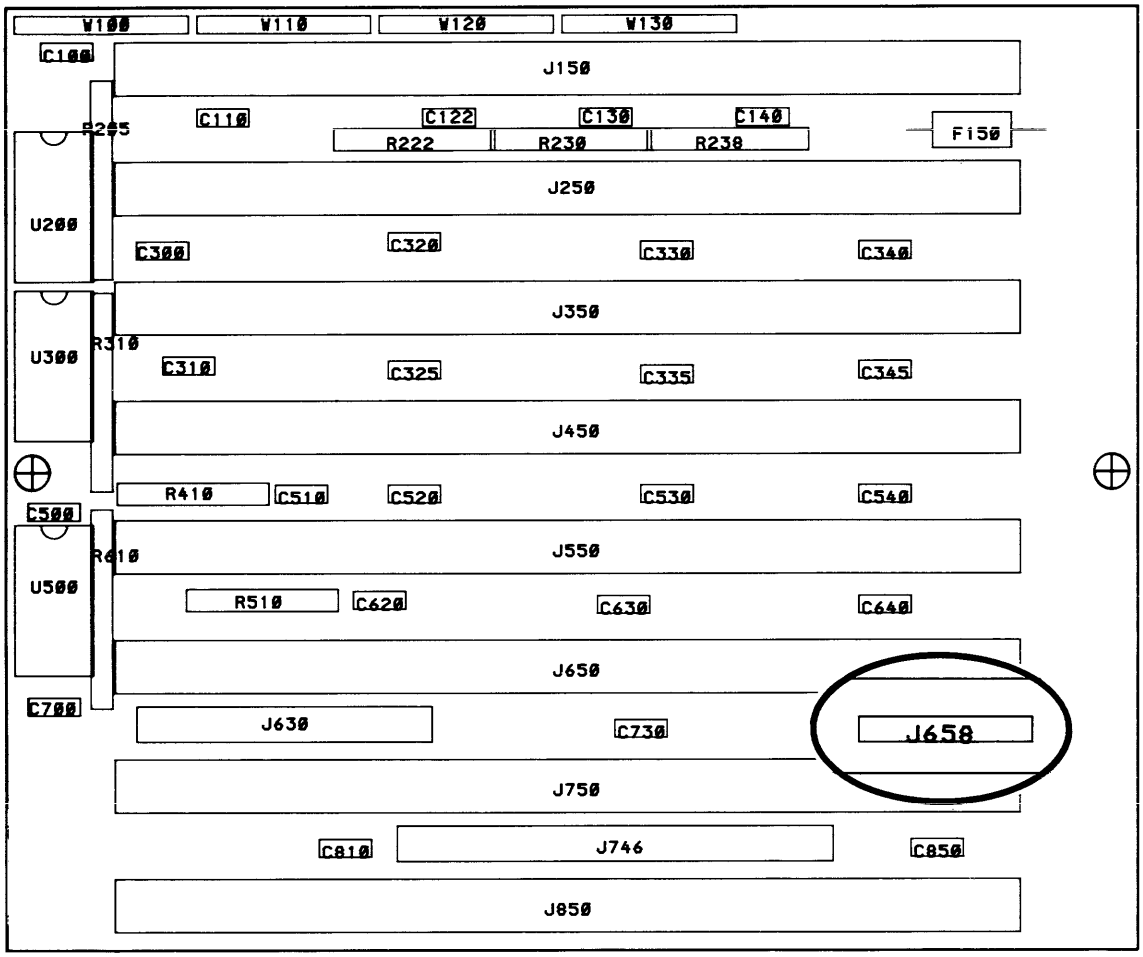


Figure 5-5. Expanded view of the Interface Board shows power supply measurement pins.

Equipment Required

- digital multimeter
- test oscilloscope
- variable transformer

Check Procedure

1. Perform procedure #1 (cabinet removal) of the *Disassembly and Installation Procedures* section of this manual.
2. Locate the set of square pins labeled J658 on the Interface Board (Figure 5-5). This set of supply pins should be used as the reference point for all power supply measurements.

3. Set the variable transformer for the appropriate low-line voltage setting (90 volts when Line Select is set to 115 V; 180 volts when Line Select is set to 230 V).
4. Check all power supplies for correct voltages using a DMM on the appropriate dc volts scale. The power supply may be in either the low-load setup (A07J444 pin 1 shorted to pin 2) or the high-load setup (A07J444 pin 2 shorted to pin 3). Refer to Table 5-3 for tolerances.

NOTE

The +3 volt supply should be measured with reference to the +5 volt supply.

5. Check all power supplies for ripple using an oscilloscope set at 0.1 V/Div, 5 ms/Div, AC input coupling, and 20 MHZ bandwidth limit ON. Refer to Table 5-3 for tolerances.
6. Reset the variable transformer output for the appropriate high-line voltage setting (132 volts when Line Select is set to 115 V; 250 volts when Line Select is set to 230 V). Re-check the supplies for the high-line setting.

Table 5-3
POWER SUPPLY READINGS

SUPPLY	dcV	ripple
+13 V *	+12.1 V to 12.9 V	0.5 V p-p max.
+12.1 V **	+11.40 V to 12.60 V	1 V p-p max.
+12 V	+11.40 V to 12.60 V	1 V p-p max.
+5 V	+4.85 V to +5.15 V	100 mV p-p max.
+3 V	−1.90 V to −2.10 V (ref. to + 5 V)	100 mV p-p max.
−5 V	−4.75 V to −5.25 V	200 mV p-p max.
−12 V	−11.40 V to −12.60 V	1 V p-p max.

*** For instruments with serial numbers B080000 and above.**
**** For instruments with serial numbers B079999 and below.**

PROCEDURE 2: DISPLAY HIGH VOLTAGE PERFORMANCE CHECK

Equipment Required

- P6015 High-Voltage Probe
- test oscilloscope

Check Procedure

1. Perform Procedure #1 (cabinet removal), #2 (rear panel removal) of the *Disassembly and Installation Procedures* section of this manual.
2. Connect the high-voltage probe to the oscilloscope and set the range scale to 2 volts/div.

3. Access the CRT module by removing the CRT Drive Board bracket. Refer to the *Disassembly And Installation Procedures* section for specific removal procedures.
4. With the instrument power OFF, connect the probe ground lead to the chassis.
5. Touch the probe tip to the anode prongs located under the anode cup (on the back of the CRT).
6. Power ON the 1240 and check that the high voltage is 10 V ± 0.5 V (1000x attenuation).
7. Power down the 1240 and remove the probe. Re-install the CRT Drive Board bracket.

PROCEDURES 3A - 3E: TEST PATTERN GENERATOR PERFORMANCE CHECKS

Equipment Required

- DC 5010 Digital Counter
- P6125 probe for DC 5010
- test oscilloscope

Procedure 3A: TPG Clock Period Check

1. Power on the 1240; the 1240 displays:

- OPERATION LEVEL: 0
- TPG MODE: 0

2. Press the front panel TRIGGER menu key. Using the Cursor and Select keys, set the following parameters:

- GLOBAL EVENT: OFF
- SEQUENTIAL EVENT: (all steps deleted using the DELETE LEVEL soft key)

3. Press the START key.
4. Connect a P6125 probe to the DC 5010 CHA input and set the DC 5010 CHA controls as follows:

- TERM: 1 M ohm
- ATTENUATION: x1
- SLOPE: POS
- COUPLING: DC

5. Press the CHA LEVEL button (ensure it is lighted). Using the up and down arrow keys, select 0.740 volts.
6. Press the 10↑N AVGS button and using the up and down arrow keys, set the number of averages for 6 (actually ten to the sixth power).
7. Connect the CHA probe to A14J620 pin 1, ground at J620 pin 12. (J620 and J630 are TPG outputs from the Trigger Board.)

8. On the DC 5010, press the PERIOD A button and observe that the period is 83.3 ns ± 2% (81.63 ns to 84.97 ns).

Procedure 3B: TPG Clock Width Check

9. Set up the oscilloscope as follows:
   - Input Sensitivity: 500 mV/Div
   - Timebase: 2 ns/Div
   - Trigger Mode: AUTO - INT - AC COUPLING
   - Display Mode: CHOP
   - Trigger Source: CH1
   - Trigger Slope: + (positive)
   - Input Coupling: DC
10. Connect the CH1 probe to A8J658-3 (the +5 volt supply on the Interface Board), ground at A8J658-7. Using the oscilloscope vertical position control, move the CH1 trace to +1.3 volts above the center graticule. Repeat procedure for CH2 probe.
11. Move the CH1 oscilloscope probe to A14J630-1 (TPG CLK), ground at A14J630-12.
12. Check that the displayed pulse is 12.0 ns wide ± 0.5 ns at the center graticule.

Procedure 3C: TPG Data Amplitude and Hold Time Check

13. With the CH1 oscilloscope probe still at A14J630-1 (from Procedure 3B), connect the CH2 oscilloscope probe to A14J630-2 (TPG data bit 0), ground at J630-6.
14. Check that the amplitude of the CH2 signal is at least 350 mV above and below the center graticule.
15. Verify that TPG data hold time is at 1 ns ± 1.5 ns (with reference to rising edge of the TPG clock).
16. Move the CH2 probe to all other TPG data pins on A14J630 and check for same amplitude and hold time.
17. Press the STOP key and remove the oscilloscope probes.

Procedure 3D: TPG Glitch Check

18. With the Trigger menu selections still the same as in Procedure 3A, press the CONFIG menu key.
19. Touch the OPERATION LEVEL soft key and select TPG MODE: 1. Press the START key.
20. Connect the CH1 oscilloscope probe to A14J630-2, ground at A14J630-6 or 12.
21. Verify glitches of 6.5 ns wide ± 1.0 ns and 300 mV above and below center graticule.
22. Press the STOP key and remove the oscilloscope probes.

Procedure 3E: Asynchronous Timebase Check

23. Press the CONFIG menu key and touch the OPERATION LEVEL soft key. Select the TPG MODE = 2 (TPG clock = T1, T1 - ASYNC - 20 ns).
24. Press the START key.
25. Connect the CHA probe to A14J630 pin 1, ground at J630 pin 6. (J620 and J630 are TPG outputs from the Trigger Board.)
26. On the DC 5010, press the PERIOD A button and observe that the period is 20.0 ns ± 0.01 % (19.998 ns to 20.002 ns).

PART 2: FUNCTIONALITY CHECKS

If the diagnostic ROM pack is available, these checks can be used in addition to the *Part 1: Supply And TPG Performance Checks* and the *Part 3: Acquisition And System Performance Checks*. Both parts 1 and 3 are used for verification of specifications listed in the performance requirements column in the *Specifications* section. These *Part 2: Functionality Checks* provide a functional verification of approximately 95% of the 1240 circuitry by using the diagnostics resident in the ROM pack. In addition to these tests, other tests allow operational checks on various instrument functions. The test results aid in showing the operational status of the instrument as a system.

PROCEDURE 1: TRIGGER FUNCTIONALITY CHECK

Equipment Required

- P6460 with diagnostic lead set (2 maximum)

Check Procedure

1. Using a P6460 probe and diagnostic lead set, connect the 9-channel pod (P0) in the first slot to the TPG connector closest to the front of the instrument (white lead on lead diagnostic lead set towards front of instrument). If an 18-channel board is in the first slot, connect probes attached at both P0 and P1 to the TPG output connectors.
2. With the 1240 power off, plug in the Diagnostic ROM pack at the ROM/RAM pack connector.
3. Enter the diagnostics mode by holding down a front panel key while powering on the 1240. This method of entering the diagnostics causes an expected Frontpanel module failure to be displayed.
4. Select MODULE: TRIGGER.
5. While the TEST THE SELECTED MODULE soft key is on, press START. The test results should give a PASS indication.

PROCEDURE 2: ACQUISITION FUNCTIONALITY CHECKS

Equipment Required

- P6460 with diagnostic lead set (2 maximum)

Check Procedure

1. If not done previously, plug in the Diagnostic ROM pack at the ROM/RAM pack connector (with the 1240 power off). Enter the diagnostics mode by holding down a front panel key while powering on the 1240.
2. Select MODULE: 1240DX-1 (where X is a 1 or 2 for 9-channel or 18-channel boards, respectively). Using a P6460 probe and diagnostic lead set, connect the 9-channel pod (P0) in the first slot to the TPG connector closest to the front of the instrument (white lead on lead diagnostic lead set towards front of instrument). If an 18-channel board is in the first slot, connect probes attached at both P0 and P1 to the TPG output connectors.
3. While the TEST THE SELECTED MODULE soft key is on, press the START key. The test results should give a PASS indication.
4. Move the necessary number of probes to the next acquisition card.
5. Select MODULE: 1240DX-2 (to test the number 2 acquisition card).
6. Press the START key. The test results should give a PASS indication.
7. Repeat same steps to test all remaining installed acquisition cards.

PROCEDURE 3: THRESHOLD FUNCTIONALITY CHECK

Equipment Required

- Acquisition Threshold Fixture
- digital multimeter

Check Procedure

NOTE

This check is duplicated in the threshold adjustment procedures for the 9- and 18-channel boards. If these procedures have already been performed, continue to Procedure 4: External Trigger Functionality Check.

1. If the cabinet has not previously been removed, remove the two screws holding the probe guide and remove the guide.
2. Install the threshold fixture (described previously in this section under *Constructing An Acquisition Threshold Fixture*) onto A15J620 of the 9-Channel board (or onto A16J510 if checking an 18-Channel board).

NOTE

The threshold voltage generated on the Acquisition Threshold Fixture is an inverse value approximately one-fourth that of the threshold setting (refer to Table 5-4). For example, if the acquisition threshold value is set to +6.35 V, the multimeter will typically show −1.587 mV.

Table 5-4
THRESHOLD SETTINGS AND READINGS

Threshold setting	Reading for 9- or 18-channel cards
0.00 V	0.00 V ± 8 mV
+6.35 V	−1.587 V ± 12 mV
−6.35 V	+1.587 V ± 12 mV

3. Power on the 1240, press the TRIGGER menu key, then touch the AUTO-RUN SPEC soft key.
4. Using the Cursor and Select keys, set the following parameters:
   - AUTO-RUN CONDITION: COMPARE ACQMEM TO REFMEM
   - WHEN EQUAL: DISPLAY AND REACQUIRE
   - WHEN NOT EQUAL: DISPLAY AND REACQUIRE
   - DISPLAY DATA FOR AT LEAST 60 SECONDS (Use a larger number if more adjustment time is required.)
5. Press the front panel AUTO key and set the following parameter:
   - CARD 0: 0.0 V
6. Connect the DMM high lead at pin 13 of the threshold fixture, ground lead at the three-wire combination.
7. Check that the DMM reading is 0.00 V ± 8 mV.
8. Using the Select keys, set the following 1240 parameter:
   - CARD 0: −6.35 V
9. Check that the DMM reading is +1.587 V ±12 mV.
10. Using the Select keys, set the following 1240 parameter:
    - CARD 0: +6.35 V
11. Check that the DMM reading is −1.587 V ± 12 mV.
12. If checking an 18-channel board, move the test fixture to J520 and repeat the checks.
13. Press the front panel STOP key.

PROCEDURE 4: EXTERNAL TRIGGER FUNCTIONALITY CHECK

Equipment Required

- 50 Ω termination
- coaxial cable; 50 Ω, approx. 8 inches

Check Procedure

1. If you are in a diagnostic menu, touch the ENTER NORMAL OPERATION soft key. If you are in the normal operating mode, press the CONFIG menu key and then touch the OPERATION LEVEL soft key.
2. Select the following parameters:
   - OPERATION LEVEL: 3
   - TPG MODE: 0
3. Touch the TIMEBASE soft key and select the listed parameters:
   - ACTIVE TIMEBASE: T1 ONLY
   - TIMEBASE T1: ASYNC - 20 ns
4. Touch the MEMORY CONFIG soft key and select THRESHOLD: TPG.
5. Press the TRIGGER menu key. Using the Cursor and Select keys, set the following parameters:
   - GLOBAL EVENT: OFF
   - SEQUENTIAL EVENT:GRPA CTL1
WAIT FOR AA 0
THEN TRIGGER
6. Touch the AUTO-RUN SPEC soft key and select the following parameter:
   - AUTO-RUN CONDITION: TRIGGER IN
   - EXTERNAL TRIGGER OUT: PULSED
7. Using a P6460 Data Acquisition Probe with a diagnostic lead set, connect probe pod P0 to the Test Pattern Generator output.
8. Press the front panel AUTO key. The 1240 should not trigger.
9. Press the STOP key.
10. Connect the 50 Ω termination to the rear-panel BNC labeled EXT TRIG IN.
11. Connect the rear-panel BNC labeled EXT TRIG OUT to the 50 Ω termination with a 50 Ω, 8 inch coaxial cable.
12. Press the AUTO key and the 1240 should trigger (no later than the fourth sample of AA 0).
13. Press the STOP key and remove the coaxial cable and termination BNC.

PROCEDURE 5: GLITCH DETECTION FUNCTIONALITY CHECK

The glitch detection check provides a functional test of the following 1240 functions:
#1 Detection, triggering, and storage of glitches on all channels.
#2 Operation of the global glitch recognizer.
#3 Operation of the sequential glitch recognizer.

Glitch Detection checks 1, 2, and 3 should be performed in order and only on one 9-channel board at a time.

#1 Check Procedure

1. Connect a P6460 probe to the 9-channel board under test and to the Test Pattern Generator at A14J630.
2. Power ON the 1240 and set the following parameters:

- OPERATION LEVEL: 3
- TPG MODE: 3

3. Touch the Timebase soft key and set the following parameters:

- TIMEBASE

ACTIVE TIMEBASES: T1 ONLY
TIMEBASE 1: ASYNC - 100ns
GLOBAL EVENT: CLOCKED

4. Touch the Memory Config soft key and set the following parameters:

- MEMORY CONFIG

9-CHANNEL CARDS: GLITCHES ON
CARD THRESHOLD: TPG

5. Touch the Channel Grouping soft key and set the following parameters:

- CHANNEL GROUPING

CARD TYPE: 9-CHAN
INPUT: HEX
DISPLAY: BIN

6. Press the Trigger menu key and set the following parameters:

- TRIGGER

TRIGGER POSITION: [· · · · T]
LOOK FOR TRIGGER: IMMEDIATELY

GLOBAL EVENT: INCR CNTR ON 55 ♦
DO NOTHING FILTER: 01 ON T1

SEQUENTIAL EVENT: 1/WAIT FOR AA ♦
TO OCCUR 100 TIMES FILTER: 01 STORAGE: OFF
2/WAIT FOR ♦♦ ♦
TO OCCUR 1 TIMES FILTER: 01 STORAGE: ON
THEN TRIGGER

2. Press the Trigger menu key and set the following parameters:

```
GLOBAL EVENT: INCR CNTR ON ♦XXX XXXX X
                  RESET IF CT= 50     FILTER: 01 ON T1

SEQUENTIAL EVENT: 1/RESET IF NOT 1111 1111 1 (FF 1 hex)
                        FILTER: 01
                  2/WAIT FOR 1011 1110 1 (BE 1 hex)
                  TO OCCUR 02 TIMES     FILTER: 01
                  THEN TRIGGER
```

3. Press START and the 1240 should not trigger. If the 1240 triggers, refer to *Glitch Check Failures*.

4. Repeat the previous steps for the remaining channels by putting a glitch (♦) on each channel (one at a time) in the Global Event menu and checking that the 1240 does not trigger. All channels not under test should be Xs (Don't Cares).

#3 Check Procedure

1. Using the menu setups entered for check #2, continue the glitch checks by making the following menu changes:

```
GLOBAL EVENT: INCR CNTR ON 1011 1110 1 (BE 1 hex)
                  TRIGGER IF CT= 02     FILTER: 01 ON T1

SEQUENTIAL EVENT: 1/RESET IF NOT 1111 1111 1 (FF 1 hex)
                        FILTER: 01
                  2/WAIT FOR ♦XXX XXXX X
                  TO OCCUR 05 TIMES     FILTER: 01
                  3/WAIT FOR X♦XX XXXX X
                  TO OCCUR 05 TIMES     FILTER: 01
                  4/WAIT FOR XX♦X XXXX X
                  TO OCCUR 05 TIMES     FILTER: 01
                  5/WAIT FOR XXX♦ XXXX X
                  TO OCCUR 05 TIMES     FILTER: 01
                  6/WAIT FOR XXXX ♦XXX X
                  TO OCCUR 05 TIMES     FILTER: 01
                  7/WAIT FOR XXXX X♦XX X
                  TO OCCUR 05 TIMES     FILTER: 01
                  8/WAIT FOR XXXX XX♦X X
                  TO OCCUR 05 TIMES     FILTER: 01
                  9/WAIT FOR XXXX XXX♦ X
                  TO OCCUR 05 TIMES     FILTER: 01
                  A/WAIT FOR XXXX XXXX ♦
                  TO OCCUR 05 TIMES     FILTER: 01
                  THEN RESET
```

2. Press START and the 1240 should not trigger. If the test triggers, refer to *Glitch Check Failures*. If the 1240 does not trigger, then levels 2 through A of the Sequential Glitch recognizer are operating properly. Testing of these levels is sufficient to assume correct operation of the remaining levels B through E. If desired, modify the test to check the remaining levels of the Sequential Glitch recognizer.

Glitch Check Failures

The Glitch Detection Functionality Check may fail if the voltage levels from the Test Pattern Generator outputs are not centered around the nominal threshold voltage of 3.70 volts. Refer to Section 2, *Specifications,* for the tolerance on the TPG output voltages.

To determine the correct threshold selection in the Memory Config menu, you will make measurements, calculate the correct threshold value, and set the card threshold nearest that value. This is the only test that may require changing the card threshold setting in the Memory Config menu.

1. With instrument power ON, press the STOP key.
2. Connect the low lead of a multimeter to pin 6 or 12 (GND) on either set of TPG output pins (A14J620 or J630). Using the high lead, measure and record the V hi (typically 4.1 V) and V lo (typically 3.3 V) voltages out of the TPG. The threshold value is [V lo] + [(V hi − V lo)/2].
3. For the card under test, set the Memory Config menu's card threshold field to the numeric selection closest to the calculated threshold value.
4. Rerun the test now that the correct threshold voltage has been selected.

7. Press the START key. The data acquired is shown in Figure 5-6; the global event counter value (displayed in the EVTS=field) should indicate 100 events. If the value in the global event counter is incorrect, refer to *Glitch Check Failures*.

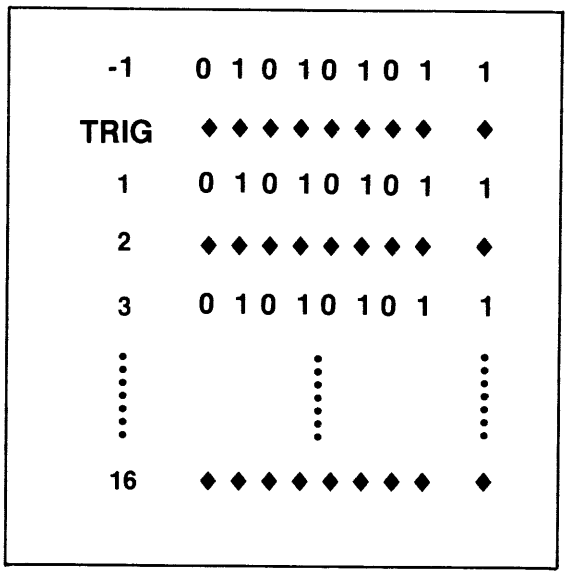


Figure 5-6. Glitch detection functionality check results.

8. Touch the ACQMEM TO REFMEM soft key and then press the X key.
9. Press the Trigger menu key. Touch the AUTO RUN soft key and set the following parameters:

- AUTO RUN SPEC

AUTO RUN CONDITION: COMPARE ACQMEM TO REFMEM
WHEN EQUAL: DISPLAY AND REACQUIRE
WHEN NOT EQUAL: DISPLAY AND STOP
MASK: Set the mask for 9-channel pods under test; clear the mask for all other pods.
COMPARISON LIMITS: FIXED
-1 - 16

10. Press the front panel AUTO key to begin the next series of acquisitions. Duplicate acquisition memories should occur and if they do not, the 1240 will display the difference and stop. Press the STOP key to end the test.

#2 Check Procedure

1. Using the menu setups entered for check #1, continue the glitch checks by making the following menu changes:

- CHANNEL GROUPING

CARD TYPE: 9-CHAN
INPUT: BIN
DISPLAY: BIN

PART 3: ACQUISITION AND SYSTEM PERFORMANCE CHECKS

These *Part 3: Acquisition And System Performance Checks*, when used in addition to the *Part 1: Supply And TPG Performance Checks*, provide the test setups necessary to verify specifications listed in the Performance Requirements column of the *Specifications* section. These checks do not use the Diagnostic ROM pack, and therefore may be extensive and time consuming. Under normal circumstances, the *Part 2: Functionality Checks* provide an adequate test of product performance in a less costly or time consuming manner.

These part 3 performance checks are divided into two categories. The first category, *Acquisition Performance Checks*, contains the procedures necessary to verify performance requirement specifications for the 1240D1 and 1240D2 (9- and 18-channel) acquisition boards. Table 5-5 lists the specifications covered by the Acquisition Performance Checks. The second category of the part 3 checks, *System Performance Checks*, contains procedures necessary to verify specifications for the 1240 as a system. Table 5-11 lists the specifications covered by the System Performance Checks.

The procedures outlined in these part 3 performance checks are constructed to fit any configuration of acquisition cards, although you may need to slightly modify some of the tests depending upon your specific acquisition configuration. If a performance verification procedure has more than one part (e.g., Procedure 1A and Procedure 1B), perform all parts of the procedure.

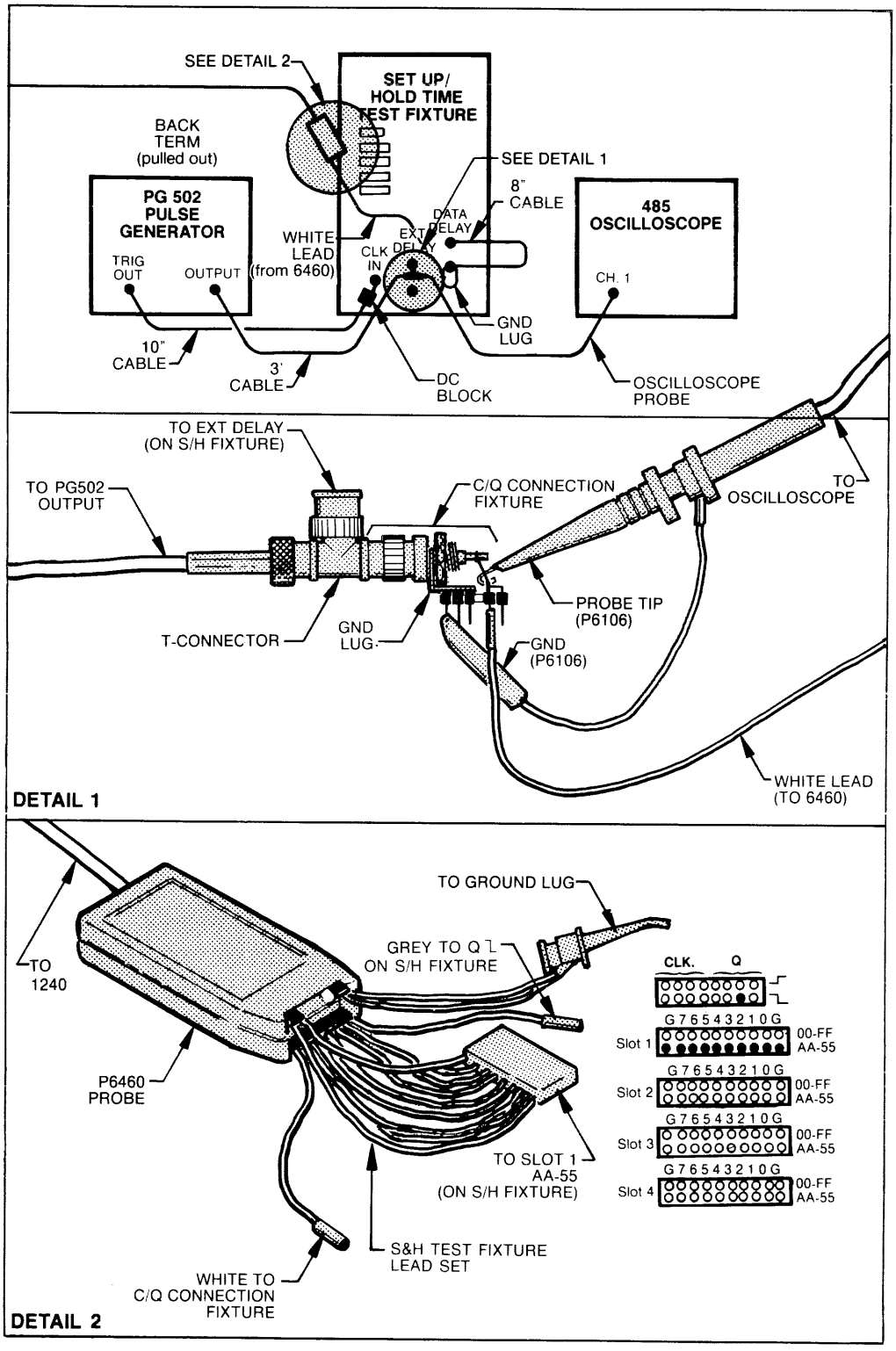
NOTE

When performing the verification procedures, use all default menu settings unless changes are indicated. All tests should be performed using Operation Level: 3 (full operation).

When using the Setup and Hold Test Fixture, connect data pods to one pin row per slot (i.e., in slot 1, connect only to 00-FF pins or only to AA-55 pins). Connect to the pins that correspond to the events programmed in the Trigger menu. Do not connect to both pin rows in any given slot.

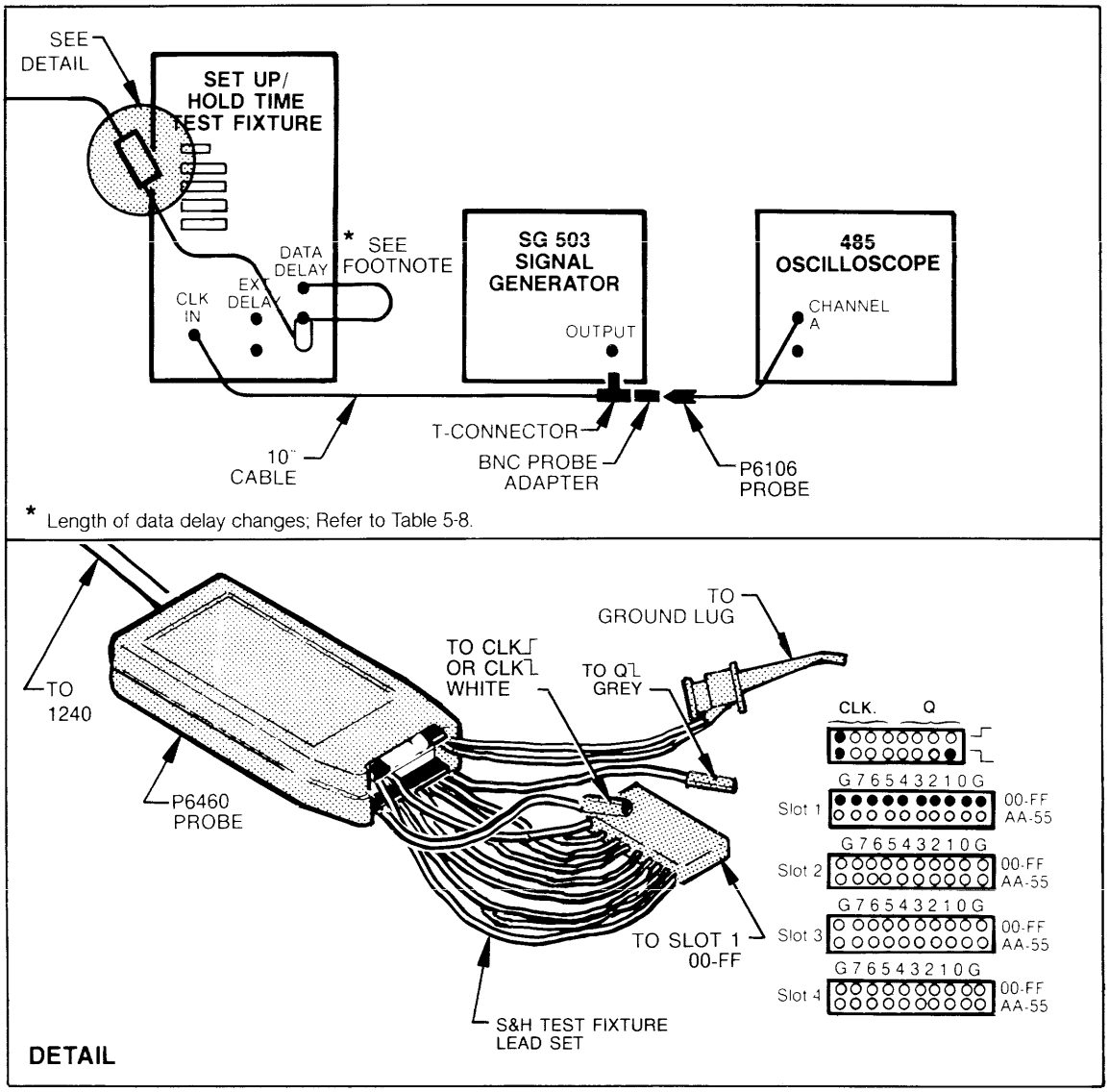
VERIFICATION SETUP ILLUSTRATIONS

Use verification setup illustrations A through E when performing these *Part 3: Acquisition And System Performance Checks*. The illustrations, found in figures 5-7 through 5-11, show the test equipment setups used in many of the performance check procedures. Some tests require a change to the basic instrument-setup figure; changes are specified when necessary.



4342-51

Figure 5-7. Verification setup A.



4342-52

Figure 5-8. Verification setup B.

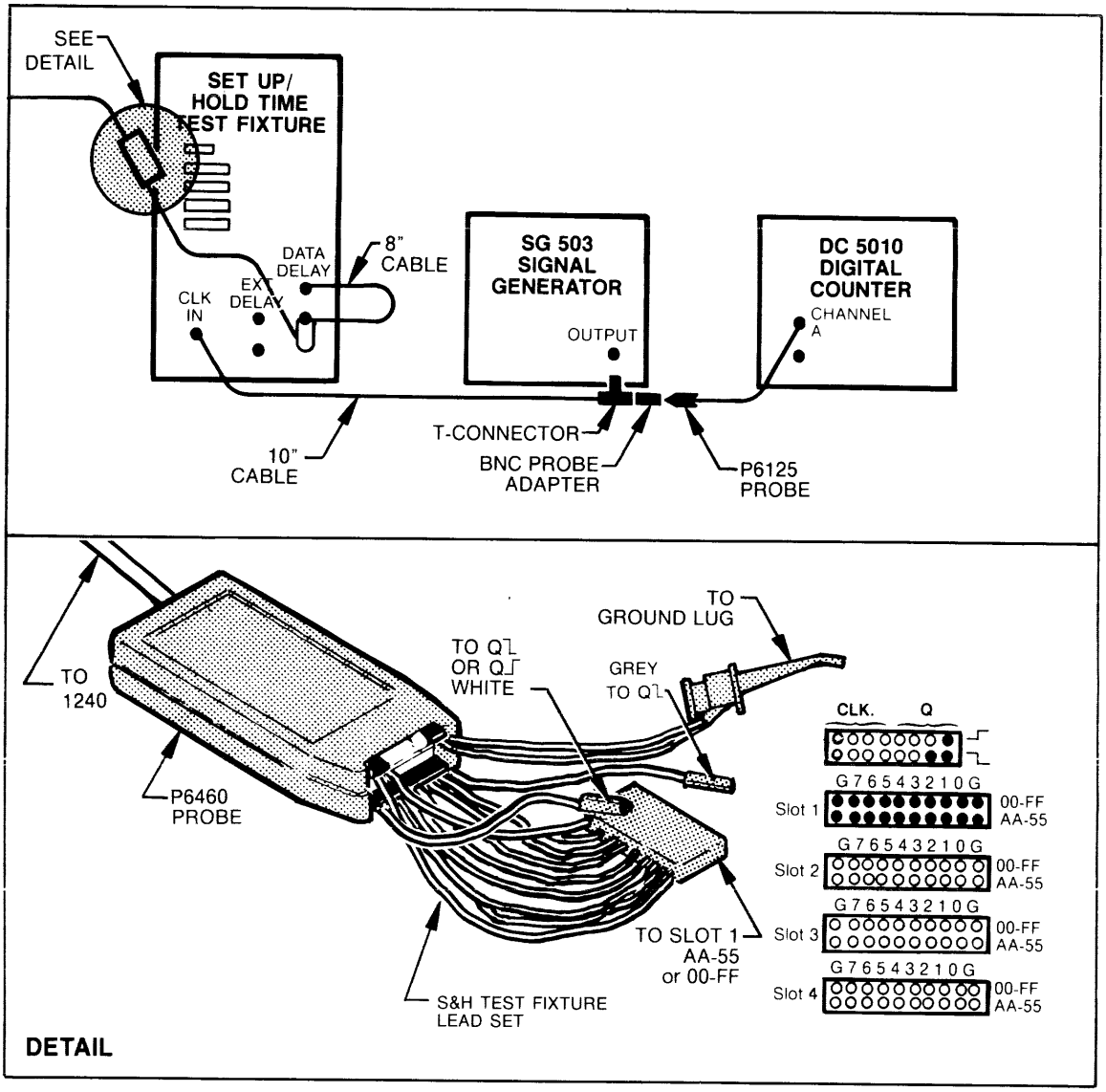
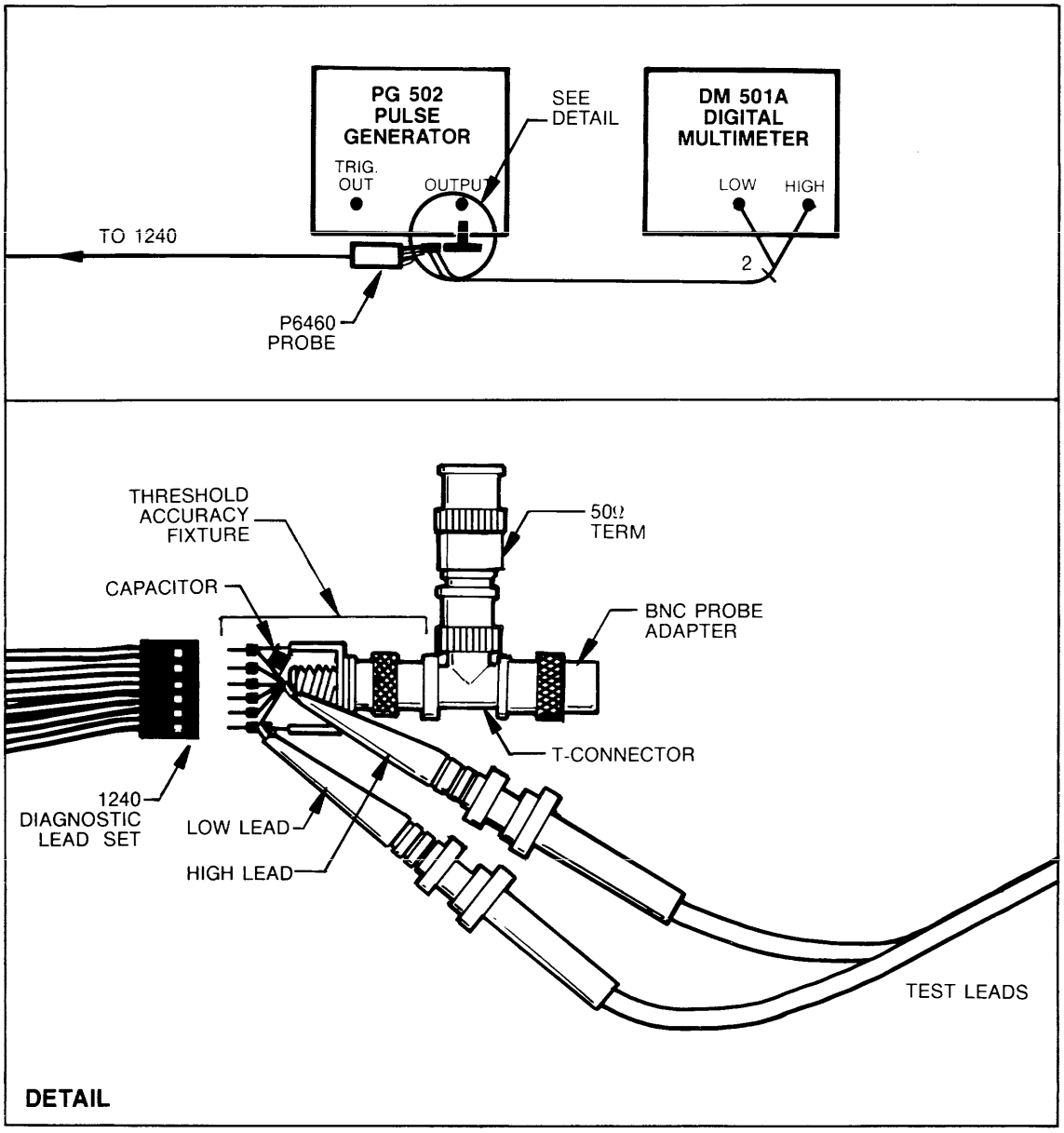


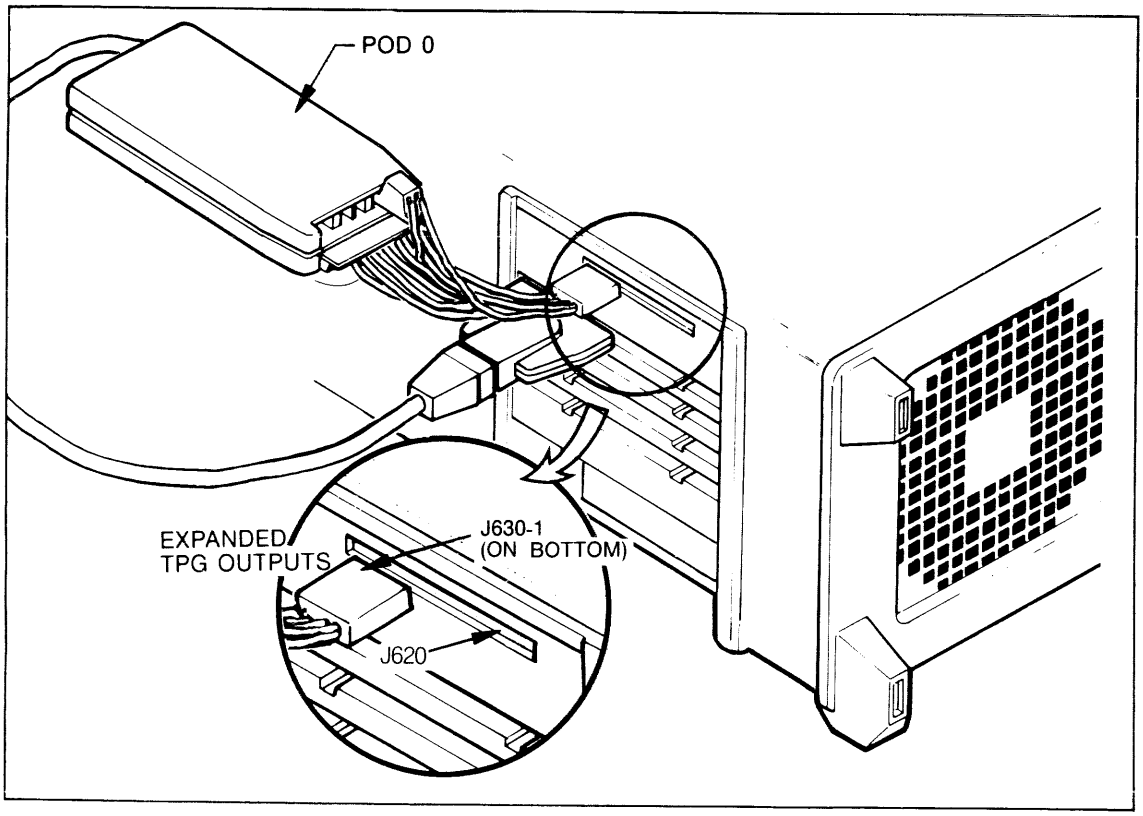
Figure 5-9. Verification setup C.

4342-53



4342-54

Figure 5-10. Verification setup D.



4342-55

Figure 5-11. Verification setup E.

ACQUISITION PERFORMANCE CHECKS

The following Table 5-5 lists the specifications covered by the Acquisition Performance Checks. Use this table as a quick reference guide to find a specification and the corresponding test procedure.

Table 5-5
SPECIFICATIONS TESTED IN THE PART 3 ACQUISITION PERFORMANCE CHECKS

NAME	VALUE	CHECK #
TIMEBASE GENERATION		
1240D1 & D2 Clock Inputs		
Pulse Width	8 ns min.	Procedure 1A
Period	20 ns min.	Procedure 1A
Amplitude	±350 mV around threshold	Procedure 1A
1240D1 & D2 Qualifier Inputs		
Setup Time	11 ns max.	Procedures 1B, 1C
Hold Time	0 ns max.	Procedures 1B, 1C
SYNCHRONOUS OPERATION		
Data, all channels		
1240D1		
Setup Time	7 ns	Procedures 2A, 2B
Hold Time	0.5 ns	Procedures 2A, 2B
	T1 sourced from 1240D1	
Amplitude	± 350 mV around threshold	Procedures 2A, 2B
1240D2		
Setup Time	12 ns	Procedures 2A, 2B
Hold Time	0 ns	Procedures 2A, 2B
Amplitude	±350 mV around threshold	Procedures 2A, 2B
ASYNCHRONOUS OPERATION		
1240D1		
Glitch Amplitude	±350 mV around threshold	Procedure 3C
1240D1 & D2		
Data min. word guaranteed to be sampled	*TB period + 6 ns	Procedure 3A

*TB for D1s= 10 ns min.; TB for D2s= 20 ns min.

Table 5-5 (cont.)
SPECIFICATIONS TESTED IN THE PART 3 ACQUISITION PERFORMANCE CHECKS

NAME	VALUE	CHECK #
ASYNC Events		
Global event for all channels, min. data word guaranteed to be sampled		
Clocked (1, 0, X)	*TB period + 6 ns	Procedure 3B
Unclocked (1,0,X)	16 ns min.	Procedure 3B
Sequential Event (1,0,X)	*TB period + 6 ns	Procedure 3A
PROBE THRESHOLD		
1240D1 & D2		
Threshold accuracy with probe	± 0.5% ± 65 mV	Procedure 4

*TB for D1s= 10 ns min.; TB for D2s= 20 ns min.

PROCEDURES 1A , B, & C: TIMEBASE GENERATION

Table 5-6
SPECIFICATIONS TESTED IN PROCEDURES 1A, B, AND C

NAME	VALUE	CHECK #
TIMEBASE GENERATION		
1240D1 & D2 Clock Inputs		
Pulse Width	8 ns min.	Procedure 1A
Period	20 ns min.	Procedure 1A
Amplitude	±350 mV around threshold	Procedure 1A
1240D1 & D2 Qualifier Inputs		
Setup Time	11 ns max.	Procedures 1B, 1C
Hold Time	0 ns max.	Procedures 1B, 1C

Equipment Setup For Procedures 1A, B, and C

- Use Figure 5-7: Verification Setup A
- Ensure that PG 502 BACKTERM is pulled out

Procedure 1A: 1240D1 & D2 Menu Setups

1. Set the following 1240 CONFIG menu parameters:

- TIMEBASE

  ACTIVE TIMEBASES: T1 ONLY
  TIMEBASE 1: SYNC - rising clock on pod under test

- MEMORY CONFIG

  CARD THRESHOLD: −ECL

2. Set the following 1240 TRIGGER menu parameters:

- TRIGGER SPEC

  TRIGGER POSITION: [· · T · ·]
  LOOK FOR TRIGGER: IMMEDIATELY
  GLOBAL EVENT: OFF
  SEQUENTIAL EVENT: WAIT FOR (*event)
  TO OCCUR 1 TIMES FILTER: 01
  THEN TRIGGER

*Connect pods to setup and hold test fixture at AA-55 pins and use AA or 55 event.

- AUTO-RUN SPEC

  MASK: Set the mask for pods under test; clear the mask for pods not under test.

  COMPARISON LIMITS: FIXED
  0 - 255

Procedure 1A: 1240D1 & D2 Check Procedure And Test Results

NOTE

Clocks generated from the PG 502 provide acceptable setup and hold times when output polarity and clock edges are properly selected. The rising edge clock (normal PG 502 output) to data hold time is greater than or equal to +5 ns. If you are uncertain that sufficient data setup or hold time exists, verify the timing with the test oscilloscope.

3. Connect a P6460 probe to the clock pod being tested. Connect the probe's data channels to the AA - 55 pin outputs (channel 8 connects to the Q ⌊ output). Connect the P6460 probe ground to the test fixture ground lug. Connect the P6460 white C/Q lead to the center conductor of the C/Q Connection Fixture.

4. Connect the oscilloscope at the output of the C/Q Connection Fixture. Set the PG 502 for Normal (+) output. Adjust the PG 502 output for a signal having a 20 ns period, 8 ns pulse width, 350 mV amplitude above and below a −1.30 V level.

5. Press the front panel START key to make the first acquisition. When the acquisition is complete and the state table is displayed, observe the trigger position on the programmed word.
6. Touch the ACQMEM TO REFMEM soft key and press the X key. Press the front panel AUTO key to begin the next series of acquisitions. Duplicate acquisition memories should occur. If clocks are missed (indicating the 1240 did not meet the specification), an incorrect acquisition will halt the auto run mode.
7. Press the STOP key and set the following 1240 CONFIG menu parameters:

- TIMEBASE

  TIMEBASE 1: SYNC - falling clock on pod under test

8. Set the PG 502 for Complement (−) output and press the AUTO key; observe correct operation.
9. Press the STOP key and set the following 1240 CONFIG menu parameters:

- TIMEBASE

  ACTIVE TIMEBASES: T2 ONLY
  TIMEBASE 2: SYNC - falling clock on pod under test

10. Repeat steps 5 and 6.
11. Press the STOP key and set the following 1240 CONFIG menu parameters:

- TIMEBASE

  ACTIVE TIMEBASES: T2 ONLY
  TIMEBASE 2: SYNC - rising clock on pod under test

12. Set the PG 502 for Normal (+) output and press the AUTO key; observe correct operation.
13. To check other clock pods, do the following:

- move the P6460 probe to the appropriate pod connection
- re-select the clock source in the Timebase menu
- reprogram the sequential event recognizer in the Trigger Spec menu for the pattern on the appropriate pod
- re-select the mask values for the current pod (Auto-Run Spec menu)
- perform steps 5 through 12.

Procedure 1B: 1240D1 & D2 Menu Setups

Before starting this performance test, refer to the *Test Selection Information* found at the end of Procedure 1C. The information provided helps the technician decide which instrument configuration will narrow the field of possible worst case clock, qualifier, and data receiver combinations. By first defining the configuration under test, the setup menus can then be defined.

1. Set the following 1240 CONFIG menu parameters:

- TIMEBASE

  ACTIVE TIMEBASES: T1 ONLY (or T2 ONLY)
  TIMEBASE 1 (or 2): SYNC

  Clocks: select source and edge
  Qualifiers: select source and level

NOTE

The clock and qualifier can be from the same pod or from two different pods. Use Clock ⎍ with Qualifier=0; use Clock ⎏ with Qualifier=1.

- MEMORY CONFIG

  CARD THRESHOLD: −ECL

  Assign the clock source selected above to desired data receiver pod.

2. Set the following 1240 TRIGGER menu parameters:

- TRIGGER SPEC

  TRIGGER POSITION: [· · T · ·]
  LOOK FOR TRIGGER: IMMEDIATELY
  GLOBAL EVENT: OFF
  SEQUENTIAL EVENT: WAIT FOR (*event)
  TO OCCUR 1 TIMES FILTER: 01
  THEN TRIGGER

*Connect pods to setup and hold test fixture at 00-FF pins and use 00 or FF event.

- AUTO-RUN SPEC

  MASK: Set the mask for the data receiver pod; clear the mask for all other pods.

  COMPARISON LIMITS: FIXED
  0 - 255

Procedure 1B: 1240D1 & D2 Check Procedure And Test Results

3. Data, clock, and qualifer can be sourced by the same data pod or by different pods. Install P6460 probes to all pods involved. Connect the data channels of the data receiver pod to the 00-FF pins of the test fixture (channel 8 to the Q⅂ output). Connect the white C/Q leads of the clock and qualifier sourcing probes to the center conductor of the C/Q Connection Fixture. Connect all probe grounds to the test fixture ground lug.

4. Connect the oscilloscope probe to the Q/Q Connection Fixture. Set the PG 502 for Normal (+) output. Adjust the PG 502 output for a signal having a 40 ns period, 400 mV amplitude above and below a −1.30 V level (adjust so the high portion is 29 ns and low is 11 ns). Use the PG 502 Normal (+) output for clock ⌐⌐ and qualifier=0; use Complemented (−) output for clock ⅂ and qualifier=1. The clock and qualifer are taken from the same signal source. In both cases, the qualifer setup and hold times, referenced to the selected clock edge, are 11 ns and 0 ns respectively.

6. Press the front panel START key to make the first acquisition. When the acquisition is complete and the state table is displayed, observe the trigger position on the programmed word.

7. Touch the ACQMEM TO REFMEM soft key and press the X key. Press the front panel AUTO key to begin the next series of acquisitions. Duplicate acquisition memories should occur. Qualifier setup and hold failures are indicated by incorect data samples and/or failure to trigger.

8. Press the STOP key and change the qualifier selection in the Timebase menu to the opposite polarity. Press START and the 1240 should display WAITING FOR TRIGGER and SLOW CLOCK messages.

9. Repeat the previous procedure for the worst case 1240D1 and D2 qualifier setup and hold configurations with the existing board configuration.

Procedure 1C: 1240D1 & D2 Menu Setups

This procedure is used to verify setup and hold times of the qualifier Q2F when Timebase 2 is in the demux mode.

10. Set the following 1240 CONFIG menu parameters:

- TIMEBASE

  ACTIVE TIMEBASES: T2 ONLY
  TIMEBASE 2: DEMUX

  First clock (T2F):
  -Clocks: select source and edge
  -Qualifiers: select source and level

  Last clock (T2L):
  -Clocks: select source and edge
  -Qualifiers: not selected

NOTE

The T2F clock and qualifier can be sourced from the same pod. The T2L clock must be sourced by a pod other than T2F clock or T2F qualifer pods. Use T2F Clock ⌐ with Qualifier=0 and T2L Clock ⌐; or use T2F Clock ⌙ with Qualifier=1 and T2L Clock ⌙.

- MEMORY CONFIG

  CARD THRESHOLD: −ECL

  Assign T2F to the data receiver pod.

Procedure 1C: 1240D1 & D2 Check Procedure And Test Results

This test requires that at least two pods since T2L clock must be sourced by another pod other than T2F clock or qualifier pods. T2F clock and qualifier can be sourced by the same pod or by two different pods; data can be sourced by any pod.

11. Install the P6460 probes to all pods involved. Connect the data channels of the data receiver pod to the 00-FF pins of the test fixture (channel 8 to the Q⌙ output). Connect the white C/Q leads of the T2F clock- and qualifier-sourcing probes to the center conductor of the C/Q Connection Fixture. Connect the C/Q lead of the T2L clock-source probe to the appropriate CLK output on the test fixture (CLK⌐ if T2L clock is ⌐). Select TSU=10 ns on the test fixture. Connect all probe grounds to the test fixture ground lug.

12. Connect the oscilloscope probe to the C/Q Connection Fixture. Set the PG 502 for Normal (+) output. Adjust the PG 502 output for a signal having a 40 ns period, 11 ns pulse width, 400 mV amplitude above and below a −1.30 V level (adjust so the high portion is 29 ns and low is 11 ns). Use the PG 502 Normal (+) output for T2Fclock ⌐; use Complemented (−) output for T2F clock ⌙.

13. Press the front panel START key to make the first acquisition. When the acquisition is complete and the state table is displayed, observe the trigger position on the programmed word.

14. Touch the ACQMEM TO REFMEM soft key and press the X key. Press the front panel AUTO key to begin the next series of acquisitions. Duplicate acquisition memories should occur. Qualifier setup and hold failures are indicated by incorect data samples and/or failure to trigger.

15. Press the STOP key and change the qualifier selection in the Timebase menu to the opposite polarity. Press START and the 1240 should display WAITING FOR TRIGGER and SLOW CLOCK messages.

Test Selection Information

For qualifier setup, the slowest qualifier and the fastest clock path provides the smallest margin. For the qualifier hold, the fastest qualifier and the slowest clock path implies the smallest margin. The specification refers to the type of board (1240D1 or D2) sourcing the qualifier. Refer to the following guidelines to narrow the field of possible worst case qualifier/data receiver configurations.

- 1240D2 setup:
  -Q generated from upper most D2 board (pod B)
  -Select data receiver at slot 0 (pod A if D2 there)
  -Select clock generated from D1 (D2 if no D1s)
- 1240D2 hold:
  -Q generated from pod A, clock generated and data received by pod B D2 most distant from slot 1
- 1240D1 setup:
  -Same as 1240D2 setup (Q generated from upper D1)
- 1240D1 hold:
  -D1s only: Q and clock generated, and data received on D1 most distant from slot 1
  -Mixed D1s and D2s: Q generated from upper most D1 board, clock generated and data received from pod B on bottom most D2
- Q2 is the fastest D2 qualifier path; Q1 is the fastest D1 qualifier path.

PROCEDURES 2A & B: SYNCHRONOUS OPERATION

Before starting this performance test, refer to the *Test Selection Information* found at the end of Procedure 2B. The information provided helps the technician decide which instrument configuration will narrow the field of possible worst case clock and data receiver combinations. By first defining the configuration under test, the setup menus can then be defined.

Table 5-7
SPECIFICATIONS TESTED IN PROCEDURES 2A & B

NAME	VALUE	CHECK #
SYNCHRONOUS OPERATION 1240D1		
Setup Time	7 ns	Procedures 2A, 2B
Hold Time	0.5 ns T1 sourced from 1240D1	Procedures 2A, 2B
Amplitude	±350 mV around threshold	Procedures 2A,12B
SYNCHRONOUS OPERATION 1240D2		
Setup Time	12 ns	Procedures 2A, 2B
Hold Time	0 ns	Procedures 2A, 2B
Amplitude	±350 mV around threshold	Procedures 2A, 2B

Equipment Setup For Procedures 2A & B

- Use Figure 5-8: Verification Setup B

In Procedures 2A and B, the boards under test are the data receiver boards. Change the test fixture setup (TSU/TH) and data delay cables according to the specification being checked on the board under test. Refer to the following Table 5-8.

Table 5-8
DATA DELAY CABLE LENGTHS

SPECIFICATION	TSU/TH ON FIXTURE	DATA DELAY CABLES
1240D1 SYNC. OPERATION		
SetupTime: 7.0 ns	10 ns	20 inch cable
Hold Time: 0.5 ns	0 ns	8 in. + BNC female-female + std. 8 inch cable
1240D2 SYNC. OPERATION		
SetupTime: 12 ns	15 ns	20 inch + BNC female-female + std. 8 inch cable
Hold Time: 0.0 ns	0 ns	std. 8 inch cable

Procedure 2A: 1240D1 & D2 Menu Setups

1. Set the following 1240 CONFIG menu parameters:

- TIMEBASE

  ACTIVE TIMEBASES: T1 ONLY (or T2 ONLY)
  TIMEBASE 1 (or 2):

  Clocks: select source and edge
  Qualifiers: not selected

NOTE

To test the 1240D1 hold time, the clock must be sourced by a D1 pod.

- MEMORY CONFIG

  CARD THRESHOLD: −ECL

2. Set the following 1240 TRIGGER menu parameters:

- TRIGGER SPEC

  TRIGGER POSITION: [· · T · ·]
  LOOK FOR TRIGGER: IMMEDIATELY
  GLOBAL EVENT: OFF

  SEQUENTIAL EVENT: WAIT FOR (*event)
  TO OCCUR 1 TIMES FILTER: 01
  THEN TRIGGER

*Connect pods to setup and hold fixture at 00-FF pins; use either 00 or FF as event value.

- AUTO-RUN SPEC

  MASK: Set the mask for pods under test; clear the mask for all other pods.

  COMPARISON LIMITS: FIXED
  0 - 255

Procedure 2A: 1240D1 & D2 Check Procedure And Test Results

3. Data and clock can be sourced by the same pod or by different pods. Use the board under test as the data receiver. Install the P6460 probes on all pods involved. Connect the data receiver pod's data channels to the 00 - FF pin outputs (channel 8 connects to the $\overline{Q}$ output). Connect the C/Q channel of the clock-sourcing probe to the appropriate CLK output on the test fixture. Connect all probe grounds to the test fixture ground lug.

4. Connect the oscilloscope at the output of the SG 503 Signal Generator. Adjust the SG 503 amplitude control for 3 V p-p. Adjust the output frequency for 50 MHz.

5. Press the front panel START key to make the first acquisition. When the acquisition is complete and the state table is displayed, observe the trigger position on the programmed word.

6. Touch the ACQMEM TO REFMEM soft key and press the X key. Press the front panel AUTO key to begin the next series of acquisitions. Duplicate aquisition memories should occur and if they do not, the 1240 will display and stop. A setup and hold failure occurs with incorrect data on the individual bits.

7. To verify the amplitude specification, offset the programmed threshold voltage (−ECL= −1.30 V) to provide a signal ± 350 mV above and below threshold. Observe the setup and hold fixture data output high and low logic levels at 10 MHz. Set the threshold value (typically at −1.25 V) for 350 mV below the observed V high value and repeat steps 5 and 6. Set the threshold value (typically at −1.45 V) for 350 mV above the observed V low value and repeat steps 5 and 6.

8. Perform the previous procedure for worst case 1240D1 setup and hold, and 1240D2 setup and hold with the existing board configuration.

Procedure 2B: 1240D1 & D2 Menu Setups

This procedure is used to verify data setup and hold times when Timebase 2 is in the demux mode.

9. Set the following 1240 CONFIG menu parameters:

- TIMEBASE

  ACTIVE TIMEBASES: T2 ONLY
  TIMEBASE 2: DEMUX

  First clock (T2F):
  -Clocks: select source and edge
  -Qualifiers: not selected

  Last clock (T2L):
  -Clocks: select source and edge
  -Qualifiers: not selected

NOTE

To test the 1240D1 hold time, the clock must be sourced by a D1 pod. Use T2F Clock ⎍ with T2L Clock ⎣; and use T2F Clock ⎣ with T2L Clock ⎍.

- MEMORY CONFIG

  CARD THRESHOLD: −ECL

  Assign T2F to the data receiver pods.

- TRIGGER:

  Use the same settings as in Procedure 2A

Procedure 2B: 1240D1 & D2 Check Procedure And Test Results

10. Data, T2F clock, and T2L clock can be sourced by the same pod or by different pods. Use the board under test as the data receiver. Install the P6460 probes to all pods involved. Connect the data channels of the data receiver probe to the 00-FF pins of the test fixture (channel 8 to the Q⎣ output). Connect the white C/Q leads of the T2F and T2L clock pods to the appropriate CLK output on the test fixture (CLK⎍ with T2F clock ⎍ and T2L clock ⎣; or use CLK⎣ with T2F clock ⎣ and T2L clock ⎍). Connect all probe grounds to the test fixture ground lug.
11. Adjust the SG 503 output for a frequency of 25 MHz (40 ns).
12. Press the front panel START key to make the first acquisition. When the acquisition is complete and the state table is displayed, observe the trigger position on the programmed word.
13. Touch the ACQMEM TO REFMEM soft key and press the X key. Press the front panel AUTO key to begin the next series of acquisitions. Duplicate aquisition memories should occur and if they do not, the 1240 will display and stop. A setup and hold failure occurs with incorrect data on the individual bits.

Test Selection Information

For data setup, the fastest clock path provides the smallest margin. For the data hold, the slowest clock path implies the smallest margin. Refer to the following guidelines to narrow the field of possible worst case clock source/data receiver configurations.

- For 9-channel specifications, use a 1240D1 as the clock source for data setup. The 1240D1 is a faster clock generation source than the 1240D2 (1 to 1.5 ns faster).
- For 18-channel specifications, use a 1240D1 as the clock source (if possible) for data setup; use a 1240D2 as the clock source for data hold.
- When checking the 1240D2 specifications, use pod A for the setup data receiver; use pod B as the hold data receiver. The 1240D2 pod A is a faster clock receiver than the 1240D2 pod B (approx. 0.7 ns faster).
- For data setup, use the data receiver nearest board slot 1. For data hold, use the data receiver furthest from slot 1.
- For both clock generators and data receivers, timebase T1 is the fastest 1240D1 timebase; timebase T2 is the fastest 1240D2 timebase.

PROCEDURES 3A, B, & C: ASYNCHRONOUS OPERATION

Table 5-9
SPECIFICATIONS TESTED IN PROCEDURES 3A, B, & C

NAME	VALUE	CHECK #
ASYNCHRONOUS OPERATION		
1240D1		
Glitch Amplitude	±350 mV around threshold	Procedure 3C
1240D1 & D2		
Data min. word guaranteed to be sampled	*TB period + 6 ns	Procedure 3A
ASYNC Events		
Global event for all channels, min. data word guaranteed to be sampled		
Clocked (1, 0, X)	*TB period + 6 ns	Procedure 3B
Unclocked (1,0,X)	16 ns min.	Procedure 3B
Sequential Event (1,0,X)	*TB period + 6 ns	Procedure 3A

*TB for D1s= 10 ns min.; TB for D2s= 20 ns min.

Equipment Setup For Procedures 3A & B

- Use Figure 5-9: Verification Setup C

Procedure 3A: 1240D1 & D2 Menu Setups

1. Set the following 1240 CONFIG menu parameters:

- TIMEBASE

  TIMEBASE 1: ASYNC - TB (where TB is the timebase rate)

  If checking D1s at TB= 10 ns and D2s are installed, then:
  TIMEBASE 2: SYNC - rising on pod 0

- MEMORY CONFIG

  9-CHANNEL CARDS: GLITCHES OFF
  CARD THRESHOLD: −ECL
  Assign T1 as clock source to all pods unless TB= 10 ns; if so, assign T2 to all D2s pods.

- CHANNEL GROUPING

  If testing 1240D1s, delete all 1240D2 channels
  If testing 1240D2s, delete all 1240D1 channels

2. Set the following 1240 TRIGGER menu parameters:

- TRIGGER SPEC

  GLOBAL EVENT: INCR CNTR ON X
  DO NOTHING FILTER: 01 ON T1

  SEQUENTIAL EVENT: T1 WAIT FOR (*event)
  TO OCCUR 100 TIMES FILTER: 01
  THEN TRIGGER

*Pods connected to setup and hold test fixture at 00-FF pins use 00 or FF event; pods connected to AA-55 pins use AA or 55 event.

- AUTO-RUN SPEC

  WHEN NOT EQUAL: DISPLAY AND REAQUIRE

Procedure 3A: 1240D1 & D2 Check Procedure

3. Connect all 1240D1 data channels (or all 1240D2 data channels if testing D2s) to the data outputs on the setup and hold fixture (channel 8 to $\overline{Q}$ output). Connect the second ground lead from each probe to the fixture's ground lug.

NOTE

When using the setup and hold fixture, connect to the pins that correspond to the events programmed in the Trigger menu. Only connect D1s and D2s to one pin row per slot (i.e., in slot 1, connect only to 00-FF pins or only to AA-55 pins). Do not connect to both pin rows in any given slot.

4. Remember, if more than two 1240D2s are present in the system, it will be necesary to divide the 1240D2 channels into two groups and perform the tests twice. Menu selections will change according to the channels selected.

5. If you are checking a 1240D1 at TB= 10 ns and D2s are installed, then clock the 1240D2 pods from a spare Q output on the S&H Test Fixture. Connect the C/Q lead of pod 0 to a Q output of the test fixture.
6. Set the SG 503 signal generator output period to TB + 6 ns (data pulse width).
7. Press the front panel START key to make the first acquisition. When the acquisition is complete and the state table is displayed, touch the ACQMEM TO REFMEM soft key and press the X key.
8. Press the front panel AUTO key to begin the next series of acquisitions.

Procedure 3A: Test Results

Each time the sequential occurrence counter reaches 100, the global event counter value (displayed in the EVTS= field) is updated. If the displayed count value is within the tolerance given by the following equation, then the specification is being met.

$$\text{Count} = [2 \cdot 100 \cdot (\text{TB} + 6\text{ ns})]/\text{TB} \pm 5$$

For example, if TB= 20 ns, then Count= 260 ± 5

Procedure 3B: 1240D1 & D2 Menu Setups

1. Set the following 1240 CONFIG menu parameters:

- TIMEBASE for testing Clocked mode

  GLOBAL EVENT= CLOCKED
  TIMEBASE 1: ASYNC - TB (where TB is the timebase rate)

  If checking D1s at TB= 10 ns and D2s are installed, then:
  TIMEBASE 2: SYNC - rising on pod 0

- TIMEBASE for testing Unclocked mode

  GLOBAL EVENT= UNCLOCKED
  TIMEBASE 1: ASYNC - 20 ns

- MEMORY CONFIG

  9-CHANNEL CARDS: GLITCHES OFF
  CARD THRESHOLD: −ECL
  Assign T1 as clock source to all pods unless TB= 10 ns; if so, assign T2 to all D2s pods.

- CHANNEL GROUPING

  If testing 1240D1s, delete all 1240D2 channels
  If testing 1240D2s, delete all 1240D1 channels

2. Set the following 1240 TRIGGER menu parameters:

- TRIGGER SPEC

If using Clocked mode:
GLOBAL EVENT: INCR CNTR ON (event)
DO NOTHING FILTER: 01 ON T1

SEQUENTIAL EVENT: T1 WAIT FOR X
TO OCCUR 1000 TIMES FILTER: 01
THEN TRIGGER

If using Unclocked mode:
GLOBAL EVENT: INCR CNTR ON (event)
DO NOTHING FILTER: 01 ON 10 ns

SEQUENTIAL EVENT: T1 WAIT FOR X
TO OCCUR 1000 TIMES FILTER: 01
THEN TRIGGER

- AUTO-RUN SPEC

  WHEN NOT EQUAL: DISPLAY AND REAQUIRE

Procedure 3B: 1240D1 & D2 Check Procedure

3. Connect all 1240D1 data channels (or all 1240D2 data channels if testing D2s) to the data outputs from the setup and hold fixture (channel 8 to Q⌝⌞ output). Connect the second ground lead from each probe to the fixture's ground lug.
4. Remember, if more than two 1240D2s are present in the system, it will be necesary to divide the 1240D2 channels into two groups and perform the tests twice. Menu selections will change according to the channels selected.
5. If you are checking a 1240D1 or D2 specification at TB= 10 ns, then clock the 1240D2 pods from a spare Q output on the S&H Test Fixture. Connect the C/Q lead of pod 0 to a Q output on the test fixture.
6. Set the SG 503 signal generator output period to:
   - Clocked mode: TB + 6 ns (data pulse width)
   - Unclocked mode: 16 ns (62.5 MHz)
7. Press the front panel START key to make the first acquisition. When the acquisition is complete and the state table is displayed, touch the ACQMEM TO REFMEM soft key and press the X key.
8. Press the front panel AUTO key to begin the next series of acquisitions.

Procedure 3B: Test Results

Each time the sequential occurrence counter reaches 1000, the global event counter value (displayed in the EVTS= field) is updated. If the displayed count value is within the tolerance given by the following equations, then the specification is being met.

- Clocked mode: Count= $1000 \cdot TB/[2 \cdot (TB + 6\ ns)] \pm 2$

For example, if TB= 20 ns, then Count= 384 ± 2

- Unclocked mode: Count= 1000·TB/(2 × 16 ns) ± 2

For example, if TB= 20 ns, then Count= 625 ± 2

Equipment Setup For Procedure 3C

- Use the C/Q Connection Fixture shown in Figure 5-7: Verification Setup A

This procedure checks the minimum glitch amplitude as a single channel specification for 1240D1 boards. The procedure is time consuming. An alternate functional check, *Procedure 5: Glitch Detection Functionality Check* found in the *Part 2: Functionality Checks*, provides adequate testing of the glitch amplitude specification.

Procedure 3C: 1240D1 & D2 Menu Setups

1. Set the following 1240 CONFIG menu parameters:

- TIMEBASE

  ACTIVE TIMEBASES: T1 ONLY
  TIMEBASE 1: ASYNC - 20 ns

- MEMORY CONFIG

  9-CHANNEL CARDS: GLITCH ON
  CARD THRESHOLD: −ECL

- CHANNEL GROUPING

  9-CHANNEL (card under test):
  -INPUT: BIN
  -DISP: BIN

2. Set the following 1240 TRIGGER menu parameters:

- TRIGGER SPEC

  GLOBAL EVENT: OFF
  SEQUENTIAL EVENT: WAIT FOR (*♦XXX XXXXX X)
  TO OCCUR 1 TIMES FILTER: 01
  THEN TRIGGER

*The specification check is made on one channel at a time. Enter a glitch (♦) in the Sequential Event menu for the channel under test.

Procedure 3C: 1240D1 & D2 Check Procedure And Test Results

3. Connect the C/Q Connection Fixture to the PG 502 Output BNC via a 50 Ω termination. Pull the PG 502 BACKTERM control out.

4. Connect the oscilloscope probe to the C/Q Connection Fixture via the BNC Probe Adapter. Set the PG 502 for a Normal (+) output, 43 ns period, 6 ns pulse width, 350 mV above and below a −1.30 V level.

5. Install a P6460 probe to the 1240D1 pod under test; connect the data channel under test to the center conductor of the C/Q Connection Fixture. Connect the probe ground to the connection fixture's ground.
6. Press the front panel START key to make the first acquisition. When the acquisition is complete and the state table is displayed, touch the TIMING DIAGRAM soft key and select EXPANSION = ×5. Use the scroll knob to move the timing diagram of the data channel under test across the screen. There should be a glitch or a 1 acquired every 2 or 3 clocks (there should be no groups of three consecutive 0s).
7. Select the Complemented (−) output from the PG 502 and make another acquisition. There should be a glitch or a 0 acquired every 2 or 3 clocks (there should be no groups of three consecutive 1s).
8. Replace the data channel lead connected to the C/Q Connection Fixture with another channel for test. Repeat steps 6 and 7; check for similar results.

PROCEDURE 4: PROBE THRESHOLD

Table 5-10
SPECIFICATIONS TESTED IN PROCEDURE 4

NAME	VALUE	CHECK #
PROBE THRESHOLD 1240D1 & D2		
Threshold Accuracy	± 0.5% ± 65 mV	Procedure 4

Equipment Setup For Procedure 4

- Use Figure 5-10: Verification Setup D

Procedure 4: 1240D1 & D2 Menu Setups

1. Set the following 1240 CONFIG menu parameters:

- TIMEBASE

  ACTIVE TIMEBASES: T1 ONLY
  TIMEBASE 1: ASYNC - 1 μs

- MEMORY CONFIG

  9-CHANNEL CARDS: GLITCHES OFF
  CARD THRESHOLD: 0.00 V

2. Set the following 1240 TRIGGER menu parameters:

- TRIGGER SPEC

  GLOBAL EVENT: OFF
  SEQUENTIAL EVENT: WAIT FOR X
  TO OCCUR 1 TIMES FILTER: 01
  THEN TRIGGER

- AUTO-RUN SPEC

  MASK: Set the mask for pods under test; clear the mask for all other pods.

Procedure 4: 1240D1 & D2 Check Procedure And Test Results

3. Connect the 1240 Data Acquisition Probe to the pod being tested. Connect the probe's diagnostic lead set to the PG 502 via the Threshold Accuracy Fixture. (Ensure that the PG 502's BACK TERM control is pulled out.) Connect the digital multimeter leads; high lead to center post of the fixture, low lead to the fixture's ground.
4. Set the PG 502 Pulse Generator in the EXT TRIG/EXT DURATION mode. Adjust the amplitude control to get a +65 mV DC voltage level. If necessary, use a test oscilloscope to ensure the DC level has no AC components or noise. (Connect the oscilloscope probe via the BNC Probe Adapter; refer to Figure 5-10. Verification Setup D.)
5. Press the front panel START key to make the first acquisition. When the acquisition is complete and the state table is displayed (observe all ones in the state table), touch the ACQMEM TO REFMEM soft key and press the X key.
6. Press the front panel AUTO key to begin the next series of acquisitions. The reference memory should match the results of each acquisition. If it does not, the 1240 stops acquiring data. The threshold accuracy error is indicated by samples of data having the opposite polarity.
7. Press the 1240 STOP key and press the CONFIG menu key. Touch the TIMEBASE soft key and select QUALIFIER= 0 for the pod under test.
8. Press the front panel START key. The 1240 should indicate that it is waiting for a trigger and should display the SLOW CLOCK message. If the 1240 does trigger, the clock/qualifier channel failed the accuracy specification.
9. Readjust the PG 502 amplitude for a −65 mV output. Repeat steps 5 and 6 (you should acquire zeros (0s) for data bits). When performing steps 5 and 6, there should be no Qualifiers selected in the Timebase menu.
10. Press the 1240 STOP key and press the CONFIG menu key. Touch the TIMEBASE soft key and select QUALIFIER=1 for the pod under test. Repeat step 8.
11. Remove the 50 Ω termination at the PG 502 output and push the PG 502's BACKTERM control in.
12. Touch the MEM CONFIG soft key and select +6.35 V for the CARD THRESHOLD field. Repeat steps 4 through 10 with the PG 502 amplitude control adjusted for +6.45 V output in step 4 and +6.25 V output in step 9. When performing steps 5 & 6, there should be no Qualifiers selected in the Timebase menu.
13. Repeat step 11 with CARD THRESHOLD set to −6.35 V and the PG 502 amplitude control adjusted for −6.25 V output in step 4 and −6.45 V output in step 9. When performing steps 5 & 6, there should be no Qualifiers selected in the Timebase menu.

SYSTEM PERFORMANCE CHECKS

The following Table 5-11 lists the specifications covered by the System Performance Checks. Use this table as a quick reference guide to find a specification and the corresponding test procedure.

Table 5-11
SPECIFICATIONS TESTED IN THE PART 3 SYSTEM PERFORMANCE CHECKS

NAME	VALUE	CHECK #
GLOBAL EVENT		
—Filter, global event Unclocked		
--Separate D1 and D2 events		
When N=1:		
Min. guaranteed event accept	Timebase period + 6 ns	Procedure 1A
When N=2 to 16:		
Max. guaranteed event reject	(N−1) × T − 8 ns	Procedure 1B
Min. guaranteed event accept	(N × T) + 2 ns	Procedure 1C
--Mixed D1 and D2 events		
Max. guar. event reject (N=2-16)	(N−1) × T − 8 ns	Procedure 1B
Min. guar. event accept (N=1-16)	(N × T) + 20 ns	Procedure 1C
—Filter, global event Clocked		
Accept D1 and/or D2 clocked events	N × T	Procedure 1D
—STORE ON (ON NOT) action	global event clocked	
T1 event or T2 event	Store data if event true for 20 ns or more	Procedure 1E
T1 event and T2 event	Store data for a timebase if both events meet indiv. timebase spec. and the other timebase event is valid for 10 ns after the storage clock	Procedure 1F
SEQUENTIAL EVENT		
Filter, accept event	N × T	Procedures 2B, 1D
Sequence level execution rate	30 ns	Procedure 2A
RESET action	40 ns	Procedure 2D
Storage qualification	30 ns	Procedure 2A
TO OCCUR nnnn TIMES	One count per valid event	Procedure 2C
Delay (nnnn CLOCKS)	1 - 9,999 system clocks	Procedure 2C

Table 5-11 (cont.)
SPECIFICATIONS TESTED IN THE PART 3 SYSTEM PERFORMANCE CHECKS

NAME	VALUE	CHECK #
RESET	40 ns	Procedure 3
COUNTER/TIMER		
COUNT mode: INCR CNTR	One count per valid event (must satisfy filter)	Procedure 4A
TIME mode:		
START TIMER	Accuracy, start to stop:	Procedure 4B
TIME WHILE	± 20 ns	Procedure 4B
T2 DEMUX CONTROL		
Phase delay between first phase (T2F) and last phase (T2L)	10 ns min.	Procedure 5
Phase delay between last phase (T2L) and first phase (T2F)	20 ns min.	Procedure 5
2 TIMEBASE CORRELATION		
Resolution of precedence between timebases	10 ns	Procedure 6

PROCEDURES 1A - F: GLOBAL EVENT

Table 5-12
SPECIFICATIONS TESTED IN PROCEDURES 1A, B, C, D, E, & F

NAME	VALUE	CHECK #
GLOBAL EVENT		
—Filter, global event Unclocked		
--Separate D1 and D2 events		
When N=1:		
Min.guaranteed event accept	Timebase period + 6 ns	Procedure 1A
When N=2 to 16:		
Max. guaranteed event reject	(N−1) × T − 8 ns	Procedure 1B
Min.guaranteed event accept	(N × T) + 2 ns	Procedure 1C
--Mixed D1 and D2 events		
Max. guar. event reject (N=2-16)	(N−1) × T − 8 ns	Procedure 1B
Min.guar. event accept (N=1-16)	(N × T) + 20 ns	Procedure 1C
—Filter, global event Clocked		
Accept D1 and/or D2 clocked events	N × T	Procedure 1D
—STORE ON (ON NOT) action	Global event clocked	
T1 event or T2 event	Store data if event true for 20 ns or more	Procedure 1E
T1 event and T2 event	Store data for a timebase if both events meet indiv. timebase spec. and the other timebase event is valid for 10 ns after the storage clock	Procedure 1F

Equipment Setup For Procedures 1A, B, C, & D

- Use Figure 5-9: Verification Setup C

Procedure 1A: 1240 Menu Setups

1. Set the following 1240 CONFIG menu parameters:

- TIMEBASE

GLOBAL EVENT= UNCLOCKED
TIMEBASE 1: ASYNC - TB (where TB is the timebase rate)

If checking D1s at TB= 10 ns ands D2s are installed, then:
TIMEBASE 2: SYNC - rising on P0

- MEMORY CONFIG

  9-CHANNEL CARDS: GLITCHES OFF
  CARD THRESHOLD: −ECL
  Assign T1 as timebase to all pods unless TB= 10 ns; if so, then assign T2 to all D2s pods.

- CHANNEL GROUPING

  If testing 1240D1 event, delete all 1240D2 channels
  If testing 1240D2 event, delete all 1240D1 channels

2. Set the following 1240 TRIGGER menu parameters:

- TRIGGER SPEC

  GLOBAL EVENT: INCR CNTR ON (*event)
  DO NOTHING FILTER: 01 ON T1

*Pods connected to setup and hold test fixture at AA-55 pins use AA or 55 event; pods connected at 00-FF pins use 00 or FF event.

SEQUENTIAL EVENT: T1 WAIT FOR X
TO OCCUR 1000 TIMES FILTER: 01
THEN TRIGGER

- AUTO-RUN SPEC

  WHEN NOT EQUAL: DISPLAY AND REAQUIRE

Procedure 1A: Check Procedure

3. Connect all 1240D1 data channels (or all 1240D2 data channels if testing D2 event) to the data outputs from the setup and hold fixture (channel 8 to Q⌐ output). Connect the second ground lead from each probe to the fixture's ground lug.

NOTE

When using the setup and hold fixture, connect to the pins that correspond to the events programmed in the Trigger menu. Only connect D1s and D2s to one pin row per slot (i.e., in slot 1, connect only to 00-FF pins or only to AA-55 pins). Do not connect to both pin rows in any given slot.

4. Remember, if more than two 1240D2s are present in the system, it will be necesary to divide the 1240D2 channels into two groups and perform the tests twice. Menu selections will change according to the channels selected.
5. If you are checking a 1240D1 or D2 event at TB= 10 ns, then clock the 1240D2 pods from a spare Q output on the S&H test fixture. Connect C/Q lead of P0 to a Q output.
6. Set the SG 503 signal generator output period to TB + 6 ns (data pulse width).

7. Press the front panel START key to make the first acquisition. When the acquisition is complete and the state table is displayed, touch the ACQMEM TO REFMEM soft key and press the X key.
8. Press the front panel AUTO key to begin the next series of acquisitions.

Procedure 1A: Test Results

Each time the sequential occurrence counter reaches 1000, the global event counter value (displayed in the EVTS= field) is updated. If the displayed count value is within the tolerance given by the following equation, then the specification is being met.

$$\text{Count} = 1000 \cdot TB/[2 \cdot (TB + 6\text{ ns})] \pm 2$$

For example, if TB= 10 ns, then Count= 313 ± 2

Procedure 1B: 1240 Menu Setups For Separate D1 Or D2 Events

1. Set the following 1240 CONFIG menu parameters:

- TIMEBASE

  GLOBAL EVENT= UNCLOCKED
  TIMEBASE 1: ASYNC - TB (where TB is the timebase rate)

  If checking global filter at N=2, select TB≥ 20 ns

  If checking D1s at TB= 10 ns and D2s are installed, then:
  TIMEBASE 2: SYNC - rising on P0

- MEMORY CONFIG

  9-CHANNEL CARDS: GLITCHES OFF
  CARD THRESHOLD: −ECL
  Assign T1 as timebase to all pods unless TB= 10 ns; if so, then assign T2 to all D2s pods.

- CHANNEL GROUPING

  If testing 1240D1 event, delete all 1240D2 channels
  If testing 1240D2 event, delete all 1240D1 channels

2. Set the following 1240 TRIGGER menu parameters:

- TRIGGER SPEC

  GLOBAL EVENT: TRIGGER ON (*event)
  DO NOTHING FILTER: N ON T1

*Pods connected to setup and hold test fixture at AA-55 pins use AA or 55 event; pods connected 00-FF pins use 00 or FF event.

- AUTO-RUN SPEC

  WHEN NOT EQUAL: DISPLAY AND REAQUIRE

Procedure 1B: Check Procedure And Results For Separate D1 Or D2 Events

If checking 1240D1 and D2 as mixed events, proceed to step 8.

3. Connect all 1240D1 data channels (or all 1240D2 data channels if testing D2 event) to the data outputs from the setup and hold fixture (channel 8 to Q⌝ on all pods connected). Connect the second ground lead from each probe to the fixture's ground lug.
4. If more than two 1240D2s are present in the system, it will be necesary to divide the 1240D2 channels into two groups and perform the tests twice. Menu selections will change according to the channels selected.
5. If you are checking a 1240D1 or D2 event at TB= 10 ns, then clock the 1240D2 pods from a spare Q output on the S&H test fixture. Connect C/Q lead of P0 to a Q output.
6. Set the SG 503 signal generator output period to (N−1) TB−8 ns for the data pulse width. If checking global filter at N=2, select TB≥ 20 ns
7. Press the front panel START key; the 1240 should not trigger. A trigger is an indication that the 1240 did not meet the specification.

Procedure 1B: Menu Setups, Procedure, And Results For Mixed D1 Or D2 Events

8. Select all available pods in the CHANNEL GROUPING menu.
9. Program the TRIGGER SPEC menu for global events on all avaliable channels.
10. Connect the data outputs from the setup and hold fixture to all 1240D1 and D2 data channels. Connect the second ground lead from each probe to the fixture's ground lug.
11. If more than two 1240D2s are present in the system, it will be necesary to divide the 1240D2 channels into two groups and perform the tests twice. Menu selections will change according to the channels selected.
12. If you are checking a 1240D1 and D2 event at TB= 10 ns, then clock the 1240D2 pods from a spare Q output on the S&H test fixture. Connect C/Q channel of P0 to a Q output.
13. Set the SG 503 signal generator output period to (N−1) TB−8 ns for the data pulse width. If checking global filter at N=2, select TB≥ 20 ns
14. Press the front panel START key; the 1240 should not trigger. A trigger is an indication that the 1240 did not meet the specification.

Procedure 1C: 1240 Menu Setups For Separate D1 Or D2 Events

1. Set the following 1240 CONFIG menu parameters:

- TIMEBASE

  GLOBAL EVENT= UNCLOCKED
  TIMEBASE 1: ASYNC - TB (where TB is the timebase rate)

  If D2s are installed and TB= 10 ns, then:
  TIMEBASE 2: SYNC - rising on P0

- MEMORY CONFIG

  9-CHANNEL CARDS: GLITCHES OFF
  CARD THRESHOLD: −ECL
  Assign T1 as timebase to all pods unless TB= 10 ns; if so, then assign T2 to all D2s pods.

- CHANNEL GROUPING

  If testing 1240D1 event, delete all 1240D2 channels
  If testing 1240D2 event, delete all 1240D1 channels

2. Set the following 1240 TRIGGER menu parameters:

- TRIGGER SPEC

  GLOBAL EVENT: INCR CNTR ON (*event)
  DO NOTHING FILTER: N ON T1

*Pods connected to setup and hold test fixture at AA-55 pins use AA or 55 event; pods connected at 00-FF pins use 00 or FF event.

SEQUENTIAL EVENT: T1 WAIT FOR X
TO OCCUR 1000 TIMES FILTER: 01
THEN TRIGGER

- AUTO-RUN SPEC

  WHEN NOT EQUAL: DISPLAY AND REAQUIRE

Procedure 1C: Check Procedure And Results For Separate D1 Or D2 Events

3. Connect all 1240D1 data channels (or all 1240D2 data channels if testing D2 event) to the data outputs from the setup and hold fixture (channel 8 to Q⎍ on all pods). Connect the second ground lead from each probe to the fixture's ground lug.
4. If more than two 1240D2s are present in the system, it will be necesary to divide the 1240D2 channels into two groups and perform the tests twice. Menu selections will change according to the channels selected.
5. If you are checking a 1240D1 or D2 event at TB= 10 ns, then clock the 1240D2 pods from a spare Q output on the S&H test fixture. Connect C/Q channel of P0 to a Q output.
6. Set the SG 503 signal generator output period to N × TB + 2 ns for the data pulse width.
7. Press the front panel START key to make the first acquisition. When the acquisition is complete and the state table is displayed, touch the ACQMEM TO REFMEM soft key and press the X key.
8. Each time the sequential occurrence counter reaches 1000, the global event counter value (displayed in the EVTS= field) is updated. If the displayed count value is within the tolerance given by the following equation, then the specification is being met.

$$\text{Count} = 1000 \cdot TB/2[(N \times TB) + 2\text{ ns}] \pm 2$$

For example, if TB= 10 ns and N= 2, then Count= 227 ± 2

Procedure 1C: Menu Setups, Procedure, And Results For Mixed D1 And D2 Events

9. Select all available pods in the CHANNEL GROUPING menu.
10. Program the TRIGGER SPEC menu for global events on all available channels.
11. Connect the data outputs from the setup and hold fixture to all 1240D1 and D2 data channels. Connect the second ground lead from each probe to the fixture's ground lug.
12. If more than two 1240D2s are present in the system, it will be necesary to divide the 1240D2 channels into two groups and perform the tests twice. Menu selections will change according to the channels selected.
13. If you are checking a 1240D1 and D2 event, select TB$\geqslant$ 20 ns.
14. Set the SG 503 signal generator output period to N $\times$ T + 20 ns for the data pulse width.
15. Press the front panel START key to make the first acquisition. When the acquisition is complete and the state table is displayed, touch the ACQMEM TO REFMEM soft key and press the X key.
16. Each time the sequential occurrence counter reaches 1000, the global event counter value (displayed in the EVTS= field) is updated. If the displayed count value is within the tolerance given by the following equation, then the specification is being met.

$$\text{Count} = 1000 \cdot TB/2[(N \times TB) + 20\text{ ns}] \pm 2$$

For example, if TB= 20 ns and N= 1, then Count= 250 $\pm$ 2

Procedure 1D: 1240 Menu Setups

1. Set the following 1240 CONFIG menu parameters:

- TIMEBASE

  GLOBAL EVENT= CLOCKED
  ACTIVE TIMEBASES: T1 ONLY
  TIMEBASE 1: ASYNC - 20 ns

- MEMORY CONFIG

  9-CHANNEL CARDS: GLITCHES OFF
  CARD THRESHOLD: −ECL

2. Set the following 1240 TRIGGER menu parameters:

- TRIGGER SPEC

  LOOK FOR TRIGGER: IMMEDIATELY

  GLOBAL EVENT: TRIGGER ON (*event)
  DO NOTHING FILTER: N ON T1

*Pods connected to setup and hold test fixture at AA-55 pins use AA or 55 event; pods connected at 00-FF pins use 00 or FF event.

Procedure 1D: Check Procedure And Results For D1, D2, or Mixed D1/D2 Events

3. Connect 1240D1 and D2 pods (if only one type available, connect only one pod) to the data outputs from the setup and hold fixture (connect all channel 8s to $\overline{Q}$ outputs). Connect the second ground lead from each probe to the fixture's ground lug.
4. Set the SG 503 signal generator output period to a 350 ns data pulse width.
5. Set the Filter value to N= 16 (in the Trigger Spec menu) and press the front panel START key.
6. When the acquisition is complete and the state table is displayed, check that the 1240 triggered on the 16th contiguous valid occurrence of the event pattern value. Valid occurrences of the event pattern should begin at location −15. This should also be the first occurrence of a valid filtered event that is stored in memory.
7. Decrease the Filter value to N= 15 and repeat step 7. Valid occurrences of the event pattern should begin at location −14 with the trigger position on the 15th valid occurrence of the event pattern.
8. Repeat this process for the Filter= 14 through 1; each time checking for the correct starting sequence for the event and the correct trigger position.
9. Make the following menu changes:

- TRIGGER SPEC

  GLOBAL EVENT: OFF
  SEQUENTIAL EVENT: WAIT FOR (event)
  TO OCCUR 1 TIMES FILTER: N
  THEN TRIGGER

10. Repeat the process described in steps 5 through 8.

Equipment Setup For Procedure 1E

- Use Figure 5-7: Verification Setup A
- Ensure the PG 502 BACKTERM control is pulled out

Procedure 1E: 1240 Menu Setups For T1 or T2 Events

1. Set the following 1240 CONFIG menu parameters:

- TIMEBASE

  GLOBAL EVENT= CLOCKED
  ACTIVE TIMEBASES: T1 ONLY
  TIMEBASE 1: SYNC - rising on pod 0

- MEMORY CONFIG

  9-CHANNEL CARDS: GLITCHES OFF
  CARD THRESHOLD: ECL

- CHANNEL GROUPING

  Assign GRPA to P0 (all channels)

2. Set the following 1240 TRIGGER menu parameters:

- TRIGGER SPEC

TRIGGER POSITION [· · · · T]

LOOK FOR TRIGGER: IMMEDIATELY

GLOBAL EVENT: STORE ON 1 FF (GRPA)
DO NOTHING

SEQUENTIAL EVENT: WAIT FOR 1 FF (GRPA)
TO OCCUR 400 TIMES FILTER: 01 WITH STORAGE OFF
THEN TRIGGER

Procedure 1E: Check Procedure And Results For T1 or T2 Events

3. Connect the P6460 data acquisition probe from P0 to the setup and hold test fixture at the 00-FF outputs (connect channel 8 to the QL). Connect the white clock lead to the center conductor of the C/Q Connection Fixture. Connect all ground leads to the test fixture's ground lug.
4. Using the Normal (+) output, adjust the PG 502 output for a 20 ns period, 10 ns pulse width, 400 mV above and below a −1.30 volt level (check with the oscilloscope at the connection fixture).
5. Press the front panel START key and observe the state table display after the 1240 triggers. The trigger should be positioned at the 400th sample of the pattern 1 FF. Check to see that all stored data is the pattern: 1 FF.
6. Repeat the previous procedure with the following changes:

- TIMEBASE

ACTIVE TIMEBASES: T2 ONLY
TIMEBASE 2: SYNC - rising on P0

Equipment Setup For Procedure 1F

- Use Figure 5-7: Verification Setup A
- Ensure that PG 502 BACKTERM is pulled out

Procedure 1F: 1240D1 & D2 Menu Setups

This test requires that a minimum of two acquisition probes be connected.

1. Set the following 1240 CONFIG menu parameters:

- TIMEBASE

ACTIVE TIMEBASES: T1 AND T2
TIMEBASE 1: SYNC - rising clock on pod 0
TIMEBASE 2: SYNC - falling clock on pod 0

- MEMORY CONFIG

  9-CHANNEL CARDS: GLITCHES OFF

  CARD THRESHOLD: −ECL

  Assign T1 to pod 0; assign T2 to pod 1 (or pod 2).

- CHANNEL GROUPING

  Assign GRPA to P0, all channels; assign GRPB to P2 (or P1 if only 1 1240D2), all channels

2. Set the following 1240 TRIGGER menu parameters:

- TRIGGER SPEC

  TRIGGER POSITION [· · · · T]

  LOOK FOR TRIGGER: IMMEDIATELY

  GLOBAL EVENT: STORE ON 0 00 (GRPA) 1 FF (GRPB)

  SEQUENTIAL EVENT: T1 WAIT FOR 0 00 (GRPA)
  TO OCCUR 400 TIMES FILTER: 01 WITH STORAGE OFF
  THEN TRIGGER

Procedure 1F: 1240D1 & D2 Check Procedure And Test Results

3. Connect the data acquisition probes to pod 0 and pod 1 (or pod 2). Connect the data channels to the 00 - FF pin outputs on the setup and hold fixture (channel 8 connects to the Q ⌊ output). Connect the P6460 probe grounds to the test fixture ground lug. Connect the P6460 white clock leads to the center conductor of the C/Q Connection Fixture.

4. Connect the oscilloscope at the output of the C/Q Connection Fixture. Set the PG 502 for a Complemented (−) output. Adjust the PG 502 output for a signal having a 30 ns period, and 10 ns from rising edge to falling edge. Set the output for a 400 mV amplitude above and below a −1.30 V level.

5. Press the front panel START key and the 1240 should indicate a triggered condition (Timebase 1:Memory Full, Timebase 2: Delay Counter = 16). Press the STOP key. Correct data display is 399 or 398 pre-trigger data samples. All T1 data samples should be 00; there should be no T2 samples.

6. Make the following menu changes:

- TIMEBASE
  TIMEBASE 1: SYNC - falling clock on P0
  TIMEBASE2: SYNC - rising clock on P0

- MEMORY CONFIG
  Assign T2 to pod 0; assign T1 to pod 1 (or pod 2).

- TRIGGER SPEC
  SEQUENTIAL EVENT: T2 WAIT FOR 1 FF (GRPA)
  TO OCCUR 400 TIMES FILTER: 01 WITH STORAGE OFF
  THEN TRIGGER

7. Press the START key and the 1240 should indicate a trigger condition (Timebase 1: Delay Counter = 16; Timebase 2: Memory Full).

8. Press the STOP key. Correct data display is 399 or 398 pre-trigger data samples. All T2 data samples (GRPA) should be 1 FF; there should be no T1 sample in GRPB.

9. Make the following menu changes:

- TIMEBASE
  ACTIVE TIMEBASES: T1 AND T2
  TIMEBASE 1: SYNC - rising clock on pod 0
  TIMEBASE 2: SYNC - rising clock on pod 0
- MEMORY CONFIG
  Re-assign T1 to pod 0; re-assign T2 to pod 1 (or pod 2).
- TRIGGER SPEC
  GLOBAL EVENT: STORE ON 1 FF (GRPA) 1 FF (GRPB)
  SEQUENTIAL EVENT: T1 WAIT FOR 1 FF (GRPA)
  TO OCCUR 01 TIMES FILTER:
  01 WITH STORAGE OFF
  THEN TRIGGER

10. Press the front panel START key. Verify the acquired data in the state table is alternating 1 FF patterns being stored on T1 and T2. Refer to the following Table 5-13:

Table 5-13
DATA STORED IN PROCEDURE 1F

Location	Stored on T1	Stored on T2
TRIG	1 FF	1 FF
·	space	1 FF
·	1 FF	space
·	1 FF	1 FF
·	space	1 FF
·	·	·
·	·	·
·	space	1 FF
23	1 FF	space

PROCEDURES 2A - D: SEQUENTIAL EVENT

Table 5-14
SPECIFICATIONS TESTED IN PROCEDURES 2A, B, C, & D

NAME	VALUE	CHECK #
SEQUENTIAL EVENT		
Filter, accept event	N × T	Procedure 2B
Sequence level execution rate	30 ns	Procedure 2A
RESET action	40 ns	Procedure 2D
Storage qualification	30 ns	Procedure 2A
TO OCCUR nnnn TIMES	One count per valid event	Procedure 2C
Delay (nnnn CLOCKS)	1 - 9,999 system clocks	Procedure 2C

Equipment Setup For Procedure 2A

- Use Figure 5-7: Verification Setup A
- Also refer to Figure 5-11: Verification Setup E

Procedure 2A: 1240D1 & D2 Menu Setups

This test requires at least two acquisition cards (1240D1 or D2).

1. Set the following 1240 CONFIG menu parameters:

- OPERATION LEVEL

  TPG MODE: 2

- TIMEBASE

  GLOBAL EVENT= CLOCKED
  TIMEBASE 1: SYNC - rising clock from pod 0
  TIMEBASE 2: SYNC - rising clock from pod 2

- MEMORY CONFIG

  9-CHANNEL CARDS: GLITCHES OFF

  CARD THRESHOLD: –ECL for pod 0, TPG for pod 2

  Assign T2 as the timebase for all pods.

- CHANNEL GROUPING

  Assign GRPB to P2, all channels

2. Set the following 1240 TRIGGER menu parameters:

- TRIGGER SPEC

  TRIGGER POSITION [· · · · T]

  LOOK FOR TRIGGER: IMMEDIATELY

  GLOBAL EVENT: OFF

  SEQUENTIAL EVENT: 1) T2 WAIT FOR 1 55 (GRPB)
  TO OCCUR 1 TIMES FILTER: 01 WITH STORAGE OFF

  2) T2 JUMP IF 0 AA
  TO LEVEL 4 FILTER: 01 WITH STORAGE ON

  3) T2 TRIGGER IF X XX
  FILTER: 01 WITH STORAGE ON

  4) T2 RESET IF NOT 1 5D
  FILTER: 01 WITH STORAGE ON

  5) T2 TRIGGER IF NOT 0 B2
  FILTER: 01 WITH STORAGE ON

  6) T2 JUMP IF NOT 1 65
  TO LEVEL 1 FILTER: 01 WITH STORAGE ON

  7) T2 WAIT FOR NOT 0 CB
  TO OCCUR 1 TIMES FILTER: 01 WITH STORAGE ON

  8) T2 TRIG IF 1 34
  FILTER: 01 WITH STORAGE ON
  ELSE RESET

- AUTO-RUN SPEC

  MASK: Set the mask for P2 channels; clear the mask for all other pods.

  COMPARISON LIMITS: FIXED
  −6 - 16

Procedure 2A: 1240D1 & D2 Check Procedure And Test Results

3. Install two P6460 probes on P0 and P2. Connect the C/Q lead of P0 to the center conductor of the connection fixture; connect the P6460 probe grounds to the test fixture ground lug. Connect P2, with a diagnostic lead set, to the Test Pattern Generator at A14J620 (refer to Figure 5-11. Verification Setup E).

4. Connect the oscilloscope at the output of the C/Q Connection Fixture. Adjust the PG 502 output for for a signal having a 30 ns period, at least 8 ns wide, 400 mV above and below a −1.30 volt level.

5. Press the front panel START key. When the 1240 triggers, observe the stored data; refer to the following example acquisition in Table 5-15:

Table 5-15
DATA STORED IN PROCEDURE 2A

Location	Data Sample
– 6	0 AA
– 5	1 5D
– 4	0 B2
– 3	1 65
– 2	0 CB
– 1	1 9E
TRIG	1 34
	Pattern Repeats
–16	1 5D

6. Touch the ACQMEM TO REFMEM soft key and press the X key, then the AUTO key. The 1240 should continue to reacquire data.
7. Press the STOP key. Change level 8 in the sequential word recognizer in the Trigger menu to:
   T2 RESET IF 1 34 (GRPB)
   ELSE TRIGGER
8. Press the START key and the 1240 should not trigger; the sequence progress indicator should move from 1 to 8.
9. Press the STOP key.

Equipment Setup For Procedure 2B

- Use Figure 5-11: Verification Setup E

Procedure 2B: 1240D1 & D2 Menu Setups

1. Set the following 1240 CONFIG menu parameters:

- OPERATION LEVEL

  TPG MODE: 0

- TIMEBASE

  GLOBAL EVENT= CLOCKED
  TIMEBASE 1: ASYNC - 20 ns
  TIMEBASE 2: SYNC - rising clock from pod 0

- MEMORY CONFIG

  9-CHANNEL CARDS: GLITCHES OFF

  CARD THRESHOLD: TPG

  Assign T1 as timebase for all pods.

- CHANNEL GROUPING

  Assign GRPA to P0 (all channels).

2. Set the following 1240 TRIGGER menu parameters:

- TRIGGER SPEC

  LOOK FOR TRIGGER: AFTER MEMORY FULL

  GLOBAL EVENT: INCR CTR ON 1 BE (GRPA)
  DO NOTHING FILTER: 02 ON T1

  SEQUENTIAL EVENT: 1) T1 WAIT FOR 1 BE (GRPA)
  TO OCCUR 1 TIMES FILTER: 02

  2) T1 WAIT FOR 0 XX (GRPA)
  TO OCCUR 1600 TIMES FILTER: 01
  THEN TRIGGER

- AUTO-RUN SPEC

  WHEN NOT EQUAL: DISPLAY AND REAQUIRE

Procedure 2B: 1240D1 & D2 Check Procedure And Test Results

3. Connect the data acquisition probe from P0 to A14J630 on the Test Pattern Generator.
4. Press the front panel START key to make the first acquisition. When the acquisition is complete and the state table is displayed, touch the ACQMEM TO REFMEM soft key and press the X key, then the AUTO key.
5. The global event counter value (displayed in the EVTS= field) should indicate 100 events; the trigger should occur on data sample 0 08.
6. Press the STOP key and change the following parameters:

- MEMORY CONFIG

  Assign T2 as the timebase for all pods.

- TRIGGER SPEC

  GLOBAL EVENT: INCR CTR ON 1 BE (GRPA)
  DO NOTHING FILTER: 01 ON T2

  SEQUENTIAL EVENT: 1) T2 WAIT FOR 1 BE (GRPA)
  TO OCCUR 1 TIMES

  2) T2 WAIT FOR 0 XX (GRPA)
  TO OCCUR 3100 TIMES
  THEN TRIGGER

7. Press the front panel START key to make the first acquisition. When the acquisition is complete and the state table is displayed, touch the ACQMEM TO REFMEM soft key and press the X key, then the AUTO key.
8. When the acquisition is complete, the global event counter value (displayed in the EVTS= field) should indicate 100 events; the trigger should occur on data sample 0 C3.

Equipment Setup For Procedure 2C

- Use Figure 5-11: Verification Setup E

Procedure 2C: 1240D1 & D2 Menu Setups

1. Set the following 1240 CONFIG menu parameters:

- OPERATION LEVEL

  TPG MODE: 2

- TIMEBASE

  GLOBAL EVENT= CLOCKED
  TIMEBASE 1: ASYNC - 20 ns
  TIMEBASE 2: SYNC - rising clock from pod 0

- MEMORY CONFIG

  9-CHANNEL CARDS: GLITCHES OFF

  CARD THRESHOLD: TPG

  Assign T2 as the timebase for all pods.

- CHANNEL GROUPING

  Assign GRPA to P0 (all channels)

2. Set the following 1240 TRIGGER menu parameters:

- TRIGGER SPEC

  TRIGGER POSITION [· · · · T]

  LOOK FOR TRIGGER: IMMEDIATELY

  GLOBAL EVENT: OFF
  SEQUENTIAL EVENT: T2 WAIT FOR 0 XX (GRPA)
  TO OCCUR 200 TIMES FILTER: 01
  THEN TRIGGER

- AUTO-RUN SPEC

  WHEN NOT EQUAL: DISPLAY AND REAQUIRE

Procedure 2C: 1240D1 & D2 Check Procedure And Test Results

3. Connect the data acquisition probe from P0 to A14J630 on the Test Pattern Generator.
4. Press the front panel START key to make the first acquisition. When the acquisition is complete and the state table is displayed, check that the trigger location is 0 71 and the first data sample (at location −410) is 1 FF.
5. Change the following parameters:

- TRIGGER SPEC

  SEQUENTIAL EVENT: T2 DELAY 200 CLOCKS
  FILTER: 01
  THEN TRIGGER

6. Press the START key. When the acquisition is complete and the state table is displayed, check that the trigger location is 0 59 and the first data sample (at location −199) is 1 FF.

Equipment Setup For Procedure 2D

- Use Figure 5-11: Verification Setup E

Procedure 2D: 1240D1 & D2 Menu Setups

1. Set the following 1240 CONFIG menu parameters:

- OPERATION LEVEL

  TPG MODE: 3

- TIMEBASE

  GLOBAL EVENT= CLOCKED
  TIMEBASE 1: ASYNC - 20 ns
  TIMEBASE 2: SYNC - rising clock from pod 0

- MEMORY CONFIG

  9-CHANNEL CARDS: GLITCHES OFF

  CARD THRESHOLD: TPG

  Assign T2 as the timebase for all pods.

- CHANNEL GROUPING

  Assign GRPA to P0 (all channels)

2. Set the following 1240 TRIGGER menu parameters:

- TRIGGER SPEC

  GLOBAL EVENT: INCR CTR ON 1 55 (GRPA)
  TRIG IF CTR= 10,000 FILTER: 01 ON T2

  SEQUENTIAL EVENT: 1) T2 WAIT FOR 0 AA
  TO OCCUR 9999 TIMES FILTER: 01
  DO NOTHING

- AUTO-RUN SPEC

  WHEN NOT EQUAL: DISPLAY AND REAQUIRE

Procedure 2D: 1240D1 & D2 Check Procedure And Test Results

3. Connect the data acquisition probe from P0 to A14J630 on the Test Pattern Generator.
4. Press the START key; when the 1240 triggers, the global event counter value (displayed in the EVTS= field) should indicate 10,000 events.
5. Change the DO NOTHING statement in the sequential word recognizer to RESET. Press the START key; the 1240 should not trigger.

PROCEDURE 3: RESET

Table 5-16
SPECIFICATIONS TESTED IN PROCEDURE 3

NAME	VALUE	CHECK #
RESET	40 ns	Procedure 3

Equipment Setup For Procedure 3

- Use Figure 5-11: Verification Setup E

Procedure 3: 1240D1 & D2 Menu Setups

1. Set the following 1240 CONFIG menu parameters:

- OPERATION LEVEL

  TPG MODE: 3

- TIMEBASE

  GLOBAL EVENT= CLOCKED
  TIMEBASE 1: ASYNC - 20 ns
  TIMEBASE 2: SYNC - rising clock from pod 0

- MEMORY CONFIG

  9-CHANNEL CARDS: GLITCHES OFF

  CARD THRESHOLD: TPG

  Assign T2 as the timebase for all pods.

- CHANNEL GROUPING

  Assign GRPA to P0 (all channels)

2. Set the following 1240 TRIGGER menu parameters:

- TRIGGER SPEC

  LOOK FOR TRIGGER: IMMEDIATELY

  GLOBAL EVENT: OFF
  SEQUENTIAL EVENT: 1) T2 WAIT FOR 1 FF (GRPA)
  TO OCCUR 1 TIMES FILTER: 01

  2) T2 WAIT FOR 0 BA
  TO OCCUR 1 TIMES FILTER: 01

  3) T2 WAIT FOR 1 55
  TO OCCUR 1 TIMES FILTER: 01
  THEN TRIGGER

Procedure 3: 1240D1 & D2 Check Procedure And Test Results

3. Connect the data acquisition probe to P0 on the 1240D1 and to A14J630 on the Test Pattern Generator.
4. Press the front panel START key; the trigger location should be on first sample of 1 55.

5. Change the following parameters:

- TRIGGER SPEC

  GLOBAL EVENT: RESET ON 0 AA (GRPA)
  FILTER: 01 ON T2

6. Press the START key; the 1240 should indicate that it is waiting for a trigger with the sequence progress indicator moving through 1, 2, and 3.

PROCEDURE 4: COUNTER/TIMER

Table 5-17
SPECIFICATIONS TESTED IN PROCEDURES 4A & B

NAME	VALUE	CHECK #
COUNTER/TIMER		
COUNT mode: INCR CNTR	One count per valid event (must satisfy filter)	Procedure 4A
TIME mode:		
START TIMER	Accuracy, start to stop:	Procedure 4B
TIME WHILE	± 20 ns	Procedure 4B

Equipment Setup For Procedures 4A & B

- Use Figure 5-11: Verification Setup E

Procedure 4A: 1240D1 & D2 Menu Setups

1. Set the following 1240 CONFIG menu parameters:

- OPERATION LEVEL

  TPG MODE: 0

- TIMEBASE

  GLOBAL EVENT= CLOCKED
  TIMEBASE 1: ASYNC - 20 ns
  TIMEBASE 2: SYNC - rising clock from pod 0

- MEMORY CONFIG

  9-CHANNEL CARDS: GLITCHES OFF

  CARD THRESHOLD: TPG

  Assign T1 as timebase for all pods

- CHANNEL GROUPING

  Assign GRPA to P0, all channels

2. Set the following 1240 TRIGGER menu parameters:

- TRIGGER SPEC

  LOOK FOR TRIGGER: AFTER MEMORY FULL

  GLOBAL EVENT: INCR CTR ON 0 XX (GRPA)
  DO NOTHING FILTER: 01 ON T1

  SEQUENTIAL EVENT: 1) T1 RESET IF NOT 1 FF (GRPA)
  FILTER: 02
  2) T1 WAIT FOR 1 BE (GRPA)
  TO OCCUR 101 TIMES FILTER: 02
  TRIGGER

- AUTO-RUN SPEC

  WHEN NOT EQUAL: DISPLAY AND REAQUIRE

Procedure 4A: 1240D1 & D2 Check Procedure And Test Results

3. Connect the data acquisition probe from P0 to A14J630 on the Test Pattern Generator.
4. Press the front panel START key to make the first acquisition. When the acquisition is complete and the state table is displayed, touch the ACQMEM TO REFMEM soft key and press the X key, then the AUTO key.
5. The global event counter value (displayed in the EVTS= field) should indicate 1600 events.
6. Press the STOP key and change the following parameters:

Procedure 4A: 1240D1 & D2 Check Procedure And Test Results

3. Connect the data acquisition probe from P0 to A14J630 on the Test Pattern Generator.
4. Press the front panel START key to make the first acquisition. When the acquisition is complete and the state table is displayed, touch the ACQMEM TO REFMEM soft key and press the X key, then the AUTO key.
5. The global event counter value (displayed in the EVTS= field) should indicate 1600 events.
6. Press the STOP key and change the following parameters:

- MEMORY CONFIG

  Assign T2 as timebase for all pods.

- TRIGGER SPEC

  GE Filter clock: 1 ON T2
  SEQUENTIAL EVENT: 1) T2 RESET IF NOT 1 FF (GRPA)
  FILTER: 01
  2) T2 WAIT FOR 1 BE (GRPA)
  TO OCCUR 101 TIMES FILTER: 01
  THEN TRIGGER

7. Press the front panel START key to make the first acquisition. When the acquisition is complete and the state table is displayed, touch the ACQMEM TO REFMEM soft key and press the X key, then the AUTO key. (Ensure the S.E. filter is set to 01.)
8. When the 1240 triggers, the global event counter value (displayed in the EVTS= field) should indicate 3100 events.

Procedure 4B: 1240D1 & D2 Menu Setups

1. Set the following 1240 CONFIG menu parameters:

- OPERATION LEVEL

  TPG MODE: 2

- TIMEBASE

  GLOBAL EVENT= CLOCKED
  TIMEBASE 1: ASYNC - 50 ns
  TIMEBASE 2: SYNC - rising clock from pod 0

- MEMORY CONFIG

  9-CHANNEL CARDS: GLITCHES OFF

  CARD THRESHOLD: TPG

  Assign T2 as timebase for all pods.

- CHANNEL GROUPING

  Assign GRPA to P0 (all channels)

2. Set the following 1240 TRIGGER menu parameters:

- TRIGGER SPEC

  LOOK FOR TRIGGER: AFTER MEMORY FULL

  GLOBAL EVENT: START TIMER ON 0 AA (GRPA)
  DO NOTHING FILTER: 01 ON T2

  SEQUENTIAL EVENT: 1) T2 WAIT FOR 0 AA (GRPA)
  TO OCCUR 1 TIMES FILTER: 01

  2) T2 DELAY 316 CLOCKS
  THEN TRIGGER FILTER: 01

- AUTO-RUN SPEC

  WHEN NOT EQUAL: DISPLAY AND REAQUIRE

Procedure 4B: 1240D1 & D2 Check Procedure And Test Results

3. Connect the data acquisition probe from P0 to A14J630 on the Test Pattern Generator.
4. Press the front panel START key to make the first acquisition. When the acquisition is complete and the state table is displayed, touch the ACQMEM TO REFMEM soft key and press the X key and the AUTO key.
5. The timer value (displayed in the NSEC= field) should indicate 15.800 μs $\pm$ 20 ns.
6. Press the STOP key and change the following parameters:

- TIMEBASE

  TIMEBASE 1: ASYNC - 1 μs
  TIMEBASE 2: SYNC -rising from P0

- TRIGGER SPEC

  LOOK FOR TRIGGER: IMMEDIATELY

  GLOBAL EVENT: TIME WHILE ON 0 AA (GRPA)
  DO NOTHING FILTER: 01 ON T2

  SEQUENTIAL EVENT: 1) T2 WAIT FOR 1 55
  TO OCCUR 5 TIMES FILTER: 01
  THEN TRIGGER

7. Press the front panel START key to make the first acquisition. When the acquisition is complete and the state table is displayed, touch the ACQMEM TO REFMEM soft key and press the X key and the AUTO key.
8. When the acquisition is complete, the timer value (displayed in the NSEC= field) should indicate 5.000 μs $\pm$ 50 ns.

PROCEDURE 5: T2 DEMUX CONTROL

Before starting this performance test, refer to the *Test Selection Information* found at the end of procedure 5. The information provided helps the technician decide which instrument configuration to use. By first defining the configuration under test, the setup menus can then be defined.

Table 5-18
SPECIFICATIONS TESTED IN PROCEDURE 5

NAME	VALUE	CHECK #
T2 DEMUX CONTROL		
Phase delay between first phase (T2F) and last phase (T2L)	10 ns min.	Procedure 5
Phase delay between last phase (T2L) and first phase (T2F)	20 ns min.	Procedure 5

Equipment Setup For Procedure 5

- Use Figure 5-7: Verification Setup A
- Ensure that PG 502 BACKTERM is pulled out

Procedure 5: 1240D1 & D2 Menu Setups

This test requires at least two pods.

1. Set the following 1240 CONFIG menu parameters:

- TIMEBASE

  ACTIVE TIMEBASES: T2 ONLY
  T2 DEMUX (choose T2F pod and T2L pod)

  Use: T2F⌉⌊ & T2L⌊⌈, or
  T2F⌊⌈ & T2L⌉⌊

- MEMORY CONFIG

  CARD THRESHOLD: −ECL

  Assign T2F and T2L to two different pods

- CHANNEL GROUPING

  Keep the grouping of the pods used to receive T2F and T2L data; delete all other pods.

2. Set the following 1240 TRIGGER menu parameters:

- TRIGGER SPEC

LOOK FOR TRIGGER: IMMEDIATELY
GLOBAL EVENT: OFF
SEQUENTIAL EVENT: WAIT FOR (*event)
TO OCCUR 1 TIMES FILTER: 01
THEN TRIGGER

*Connect pods to setup and hold test fixture at AA-55 pins use AA or 55 event.

- AUTO-RUN SPEC

MASK: Set the mask for data-receiving pods; clear the mask for all other pods.

COMPARISON LIMITS: FIXED
0 - 255

Procedure 5: 1240D1 & D2 Check Procedure And Test Results

NOTE

Clocks generated from the PG 502 provide acceptable setup and hold times when output polarity and clock edges are properly selected. The rising edge clock (normal PG 502 output) to data hold time is greater than or equal to +5 ns. If you are uncertain that sufficient data setup or hold time exists, verify the timing with the test oscilloscope.

3. T2F and T2L clocks can be sourced by the same pod or by two different pods. T2F and T2L data must be sourced by two different pods. Install P6460 probes to all involved pods. Connect the white C/Q leads of the clock sourcing probes to the center conductor of the C/Q Connection Fixture. Connect the data channels of the data-sourcing probes to the AA-55 pins on the setup and hold fixture (channel 8s to the Q ⌊ pins). Connect all probe grounds to the test fixture ground lug.

4. Connect the oscilloscope at the output of the C/Q Connection Fixture. Set the PG 502 at Normal (+) output. Adjust the PG 502 output for a signal having a 30 ns period, 400 mV amplitude above and below a −1.30 V level (20 ns high; 10 ns low). Set the PG 502 to Normal (+) output for T2F⌊ & T2L⌈; otherwise use Complement (−) output for T2F⌈ & T2L⌊.

5. Press the front panel START key to make the first acquisition. When the acquisition is complete and the state table is displayed, observe the trigger position on the programmed word. The acquisition should be the test fixture's pattern with T2F clocked memory equal to T2L clocked memory and in sync.

6. Touch the ACQMEM TO REFMEM soft key and press the X key. Press the front panel AUTO key to begin the next series of acquisitions. Duplicate acquisition memories should occur. T2 demux control failure is indicated by incorrect acquisition and/or failure to trigger.

7. Perform the above procedure for the worst cases of the selected T2F→T2L configuration and of the selected T2L→T2F configuration.

Test Selection Information

The following information helps when deciding selections for T2F and T2L as clock generators, as well as assigning timebases to data pods. For T2F→T2L holdoff, the slowest T2F and the fastest T2L clock path provides the smallest holdoff margin. For T2L→T2F holdoff, the fastest T2F and the slowest T2L clock path implies the smallest margin. Refer to the following guidelines to narrow the field of possible worst case configurations.

For T2F→T2L:

1. Select a 1240D2 for T2F generator if available; otherwise use D1.
2. Select a 1240D1 for T2L generator if available; otherwise use D2.
3. Assign T2L to pod selected in number 2 (above).
4. Assign T2F to all other pods.

For T2L→T2F:

1. Select a 1240D1 for T2F generator if available; otherwise use D2.
2. Select a 1240D2 for T2L generator if available; otherwise use D1.
3. Assign T2F to pod selected in number 1 (above).
4. Assign T2L to all other pods.

PROCEDURE 6: TWO TIMEBASE CORRELATION

Before starting this performance test, refer to the *Test Selection Information* found at the end of procedure 6. The information provided helps the technician decide which instrument configuration to use. By first defining the configuration under test, the setup menus can then be defined.

Table 5-19
SPECIFICATIONS TESTED IN PROCEDURE 6

NAME	VALUE	CHECK #
2 TIMEBASE CORRELATION		
Resolution of precedence between timebases	10 ns	Procedure 6

Equipment Setup For Procedure 6

- Use Figure 5-7: Verification Setup A
- Ensure that PG 502 BACKTERM is pulled out

Procedure 6: 1240D1 & D2 Menu Setups

This test requires the use of at least two pods.

1. Set the following 1240 CONFIG menu parameters:

- TIMEBASE

  T1 AND T2 (choose T1 pod and T2 pod)

  Use: T1⎣ & T2⎍, or
  T1⎍ & T2⎣

- MEMORY CONFIG

  CARD THRESHOLD: −ECL

  Assign T1 and T2 to two different pods

- CHANNEL GROUPING

  Keep the grouping of the pods used as T1 and T2 data receivers; delete all unused pods.

2. Set the following 1240 TRIGGER menu parameters:

- TRIGGER SPEC

  TRIGGER POSITION: [· · T · ·]
  LOOK FOR TRIGGER: IMMEDIATELY
  GLOBAL EVENT: OFF
  SEQUENTIAL EVENT: T1 WAIT FOR (*event)
  TO OCCUR 1 TIMES FILTER: 01
  THEN TRIGGER

*Connect pods to setup and hold test fixture at AA-55 pins and use AA or 55 event.

- AUTO-RUN SPEC

  MASK: Set the mask for data-receiving pods; clear the mask for all other pods.

  COMPARISON LIMITS: FIXED
  0 - 255

Procedure 6: 1240D1 & D2 Check Procedure And Test Results

NOTE

Clocks generated from the PG 502 provide acceptable setup and hold times when output polarity and clock edges are properly selected. The rising edge clock (normal PG 502 output) to data hold time is greater than or equal to +5 ns. If you are uncertain that sufficient data setup or hold time exists, verify the timing with the test oscilloscope.

3. T1 and T2 clocks can be sourced by the same pod or by two different pods. T1 and T2 data must be sourced by two different pods. Connect the P6460 probes to all pods involved. Connect the white C/Q leads of the clock sourcing probes to the center conductor of the C/Q Connection Fixture. Connect all data channels of the data-sourcing probes to the AA-55 pin outputs of the setup and hold test fixture (channel 8s connect to the Q ⅂ outputs). Connect all the probe grounds to the test fixture ground lug.

4. Connect the oscilloscope at the output of the C/Q Connection Fixture. Set the PG 502 at Normal (+) output. Adjust the PG 502 output for a signal having a 30 ns period, 400 mV amplitude above and below a −1.30 V level (20 ns high; 10 ns low). Use the PG 502 Normal (+) output for T1⅂ prior to T2⌐; otherwise use Complement (−) output for T1⌐ prior to T2⅂.

5. Press the front panel START key to make the first acquisition. When the acquisition is complete and the state table is displayed, observe the trigger position on the programmed word. The acquisition should be the test fixture's pattern on both T1 and T2 data and in sync.

6. Touch the ACQMEM TO REFMEM soft key and press the X key. Press the front panel AUTO key to begin the next series of acquisitions. Duplicate acquisition memories should occur. Correlation resolution failure is indicated by alternating precedence of T1 and T2 clocked data.

7. Repeat the above procedure for the selected T2 prior to T1 configuration. Use the PG 502 Normal (+) output for T2⅂ prior to T1⌐; otherwise use Complement (−) output for T2⌐ prior to T1⅂.

8. The correctly acquired T2 data pattern should be shifted one sample relative to the T1 data pattern.

9. Disconnect the P6460 probes from the setup and hold test fixture. Connect a probe to pod 0 and the TPG at A14J630. Connect a second probe to pod 2 (pod 1 if single D2), and attach it to the TPG at A14J620.

10. Make the following menu changes:

- TIMEBASE

  T1: SYNC - rising on pod 0
  T2: SYNC - falling on pod 0
  (Ensure TPG MODE is set to 0)

- MEMORY CONFIG

  CARD THRESHOLD: TPG

  Assign T1 as timebase for pod 0; assign T2 as timebase for pod 2 (or pod 1)

- CHANNEL GROUPING

  Keep the grouping of pod 0 and pod 2 (or pod 1); delete all other pods.

- TRIGGER SPEC

  SEQUENTIAL EVENT: T1 WAIT FOR 1FF
  TO OCCUR 1 TIMES FILTER: 01
  THEN TRIGGER

- AUTO-RUN SPEC

  MASK: Set the mask for pods under test; clear the mask for pods not under test.

  COMPARISON LIMITS: FIXED
  0 - 255

11. Press the START key to make a single acquisition; the resulting acquisition is shown in Table 5-20. The T1 and T2 data are the TPG patterns from the trigger at A14J630 and J620. Refer to Table 5-20.

Table 5-20
DATA STORED IN FIRST PART OF PROCEDURE 6

Location	Stored on T1	Stored on T2
TRIG	1 FF	1 FF
1	1 BE	1 EF
2	1 7D	1 D7
.	.	.
.	.	.
256	1 75	1 55

12. Check for a repeatable acquisition with auto run feature.

13. Change the edge polarity for T2 ⌋; make a single acquisition. The resulting acquisition is shown in Table 5-21. The order of precedence alternates starting with T1 prior to T2. The TPG pattern is acquired by each timebase.

Table 5-21
DATA STORED IN THE SECOND PART OF PROCEDURE 6

Location	Stored on T1	Stored on T2
TRIG	1 FF	1 FF
	space	1 F7
	1 BE	space
	1 7D	1 EF
	space	1 D7
	.	.
	.	.
384	175	1AE

14. Check for a repeatable acquisition with auto run feature.

Test Selection Information

The following information helps when deciding selections for T1 and T2 as clock generators, as well as assigning timebases to data pods. For T1 prior to T2 resolution, the slowest T1 and the fastest T2 clock path provides the smallest margin. For T2 prior to T1 resolution, the slowest T2 and the fastest T1 clock path implies the smallest margin. Refer to the following guidelines to narrow the field of possible worst case configurations.

For T1 prior to T2:

1. Select a 1240D2 for T1 generator if available; otherwise use D1.
2. Select a 1240D1 for T2 generator if available; otherwise use D2.
3. Assign T1 to smallest pod number selected in numbers 1 and 2 (above).
4. Assign T2 to other pods used above, delete all other pods.

For T2 prior to T1:

1. Select a 1240D1 for T1 generator if available; otherwise use D2.
2. Select a 1240D2 for T2 generator if available; otherwise use D1.
3. Assign T1 to smallest pod number selected in numbers 1 and 2 (above).
4. Assign T2 to other pods used above, delete all other pods.

ADJUSTMENT PROCEDURES

INTRODUCTION

The Adjustment Procedures provide instructions for adjusting instrument variables so that the instrument meets or exceeds the specifications listed in the performance requirements column of the *Specifications* section. If the product cannot be made to meet or exceed the listed specifications by following these procedures, repair is necessary.

PURPOSE

The adjustment procedures provide a sequence for adjustments. They are not a troubleshooting guide or a verification procedure. In some cases, the adjustment procedures refer to generic disassembly instructions. If specific disassembly instructions are required, refer to the *Disassembly and Installation Procedures* section.

LIMITS AND TOLERANCES

All limits and tolerances given in the following procedures are adjustment guides. They should not be interpreted as instrument specifications unless they are also found in the performance requirements column of the *Specifications* section.

Tolerances given are for the instrument and do not include test equipment error.

EQUIPMENT REQUIRED

The equipment listed at the beginning of this *Verification and Adjustment Procedures* section, or equivalent, is necessary to complete all of the adjustment procedures. A partial list of equipment needed for each individual check and adjustment is also provided at the beginning of each procedure.

The performance requirements given in tables of the *Specifications* section are the minimum necessary to produce accurate results. Therefore, the related equipment must meet or exceed the listed specifications. Detailed instructions for operating the test equipment are not offered in this manual. Refer instead to the specific test equipment manual if operating instructions are required.

Equipment Alternatives

When substituting equipment other than recommended test equipment, control settings or adjustment setups may need to be altered. If the exact equipment listed in Table 5-1 is not available, check the minimum specification column carefully to see if any other equipment will suffice.

ADJUSTMENT INTERVAL

To ensure correct instrument operation, adjustment should be checked every 5000 hours of operation or once every year if used infrequently. Before performing the adjustment procedures, perform preventive maintenance as outlined in the *Maintenance* section.

TEST SEQUENCE

Before starting any of the 1240 adjustment procedures, perform the listed Pre-Adjustment Procedure. After that, perform the subsequent adjustment procedures in any order. (Sequential order is recommended when performing all the adjustment procedures.) If an adjustment procedure has more than one part (e.g., 1A and 1B), perform all parts of the procedure.

PRE-ADJUSTMENT PROCEDURE

Equipment Required

- digital multimeter
- test oscilloscope
- variable transformer

Check Procedure

1. Perform procedures #1 and #3 (cabinet removal and card cage roll) of the *Disassembly and Installation Procedures* section of this manual.
2. Locate the set of square pins labeled J658 on the Interface Board (Figure 5-12). This set of supply pins should be used as the reference point for all power supply measurements.
3. Set the variable transformer for the appropriate low-line voltage setting (90 volts when Line Select is set to 115 V; 180 volts when Line Select is set to 230 V).
4. Check all power supplies for correct voltages using a DMM on the appropriate dc volts scale. The power supply may be in either the high-load setup (A07J444 pin 1 shorted to pin 2) or the low-load setup (A07J444 pin 2 shorted to pin 3). The jumper should be positioned in the low-load setup when two acquisition cards, either 9-channel or 18-channel, are installed. If more than two 9- or 18-channel cards are installed, the jumper should be positioned in the high-load setup. Refer to Table 5-22 for tolerances.

NOTE

The +3 volt supply should be measured with reference to the +5 volt supply.

5. Check all power supplies for ripple using an oscilloscope set at 0.1 V/Div, 5 ms/Div, AC input coupling, and 20 MHZ bandwidth limit ON. Refer to Table 5-22 for tolerances.
6. Reset the variable transformer output for the appropriate high-line voltage setting (132 volts when Line Select is set to 115 V; 250 volts when Line Select is set to 230 V). Re-check the supplies for the high-line setting.

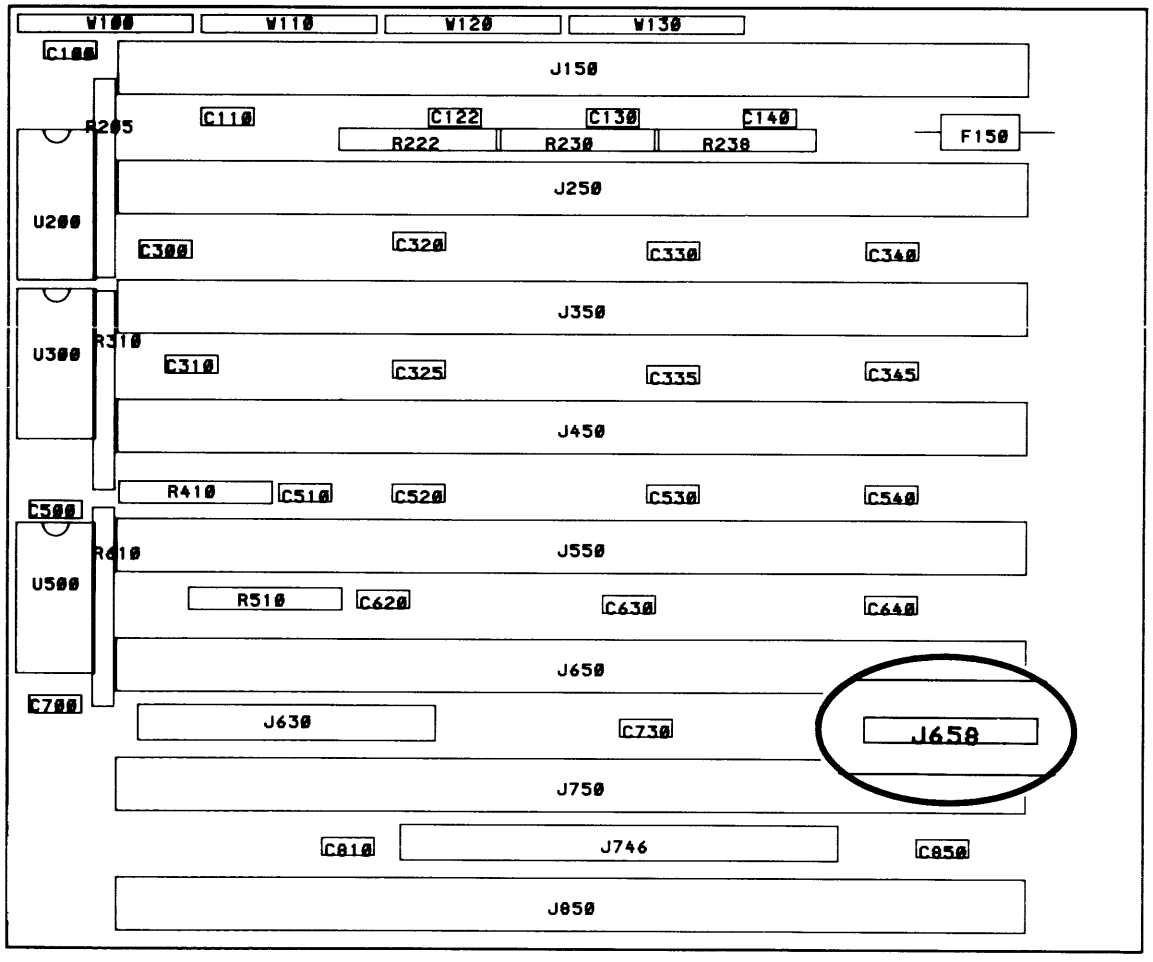
NOTE

If the 1240 power supply does not meet the listed tolerances, repair is necessary before starting any adjustment procedures.

Table 5-22
POWER SUPPLY READINGS

SUPPLY	dcV	ripple
+13 V*	+12.1 V to 12.9 V	0.5 V p-p max.
+12.1 V**	+11.40 V to 12.60 V	1 V p-p max.
+12 V	+11.40 V to 12.60 V	1 V p-p max.
+5 V	+4.85 V to +5.15 V	100 mV p-p max.
+3 V	−1.90 V to −2.10 V (ref. to + 5 V)	100 mV p-p max.
−5 V	−4.75 V to −5.25 V	200 mV p-p max.
−12 V	−11.40 V to −12.60 V	1 V p-p max.

* For instruments with serial numbers B080000 and above.
** For instruments with serial numbers B079999 and below.



4342-56

Figure 5-12. Expanded view of the Interface Board shows power supply measurement pins.

1A. CRT: ALIGNMENT ADJUST

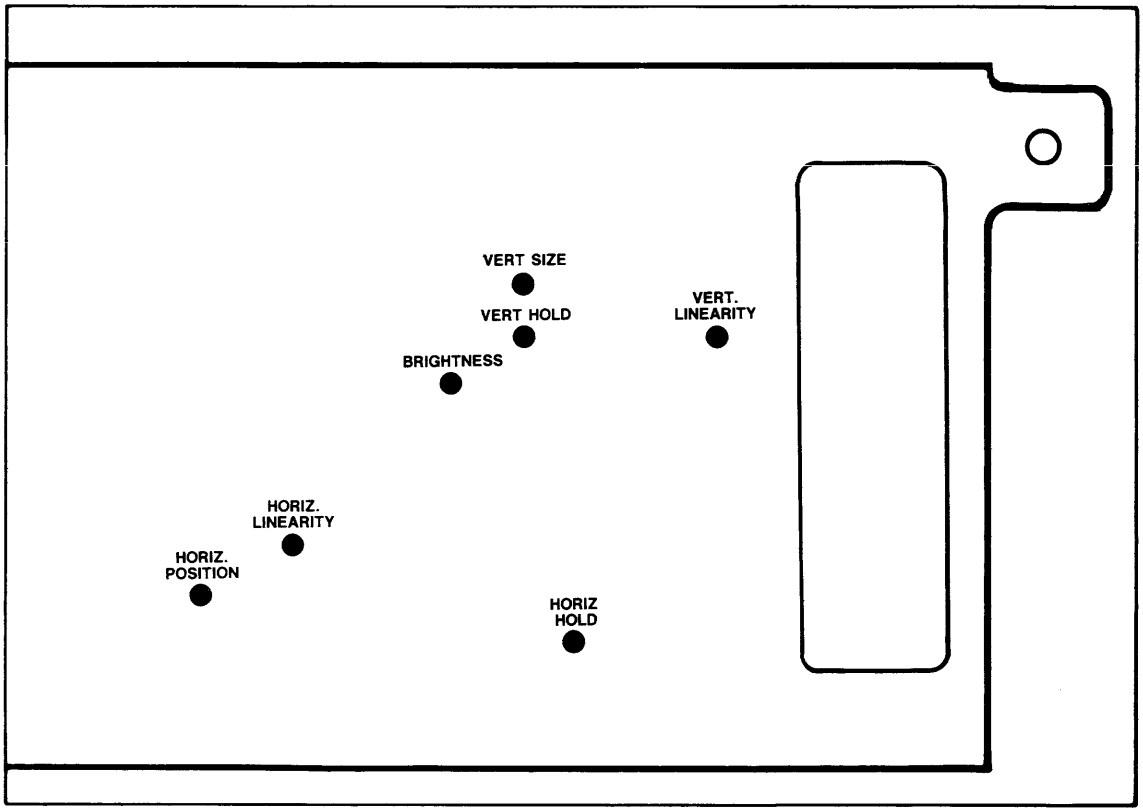


Figure 5-13. 1240 side showing CRT Drive Board adjustment holes.

Equipment Required

- adjustment tool

Adjustment Procedure

Allow 15 minutes for CRT warmup. If the pattern on the screen does not look square, perform the following adjustments as necessary. Refer to Figure 5-13 during the adjustment procedure.

1. Access the diagnostic tests by holding down any front panel key while powering ON the 1240. The tests initially indicate a keyboard failure due to the key being held down.
2. While in the Main Diagnostic menu, select the FRONTPANEL module. Touch the Module Diagnostic soft key and select the FP VERIFY area. Touch the Area Diagnostic soft key and select 2 for the routine number. Press the START key.
3. If necessary, adjust the Horizontal Hold, A06R513, to center of the range where horizontal synchronization is achieved.

4. If necessary, adjust the Vertical Hold, A06R320, to center of the range where vertical synchronization is achieved.
5. Adjust the Horizontal Position, A06R555, to place the cross in the center of the screen.
6. Adjust the Horizontal Linearity, A06L435, to make the corner soft keys match. All soft key widths should be within 0.02 inches of each other.

NOTE

The soft key boxes in the middle of the screen are normally narrower than ones at the outer edges of the screen.

7. Adjust the Horizontal Width L600, located on the deflection yoke of the CRT, until the picture is 5.1 inches wide. Access to the adjustment is provided by removing the CRT Drive Board bracket (refer to the *Disassembly And Installation Procedures* section). The adjustment tool fits through a hole in the CRT shield.

NOTE

The horizontal linearity and size controls interact. For proper adjustment, repeat both adjustments until both are correct.

8. Adjust the Vertical Linearity, A06R300, to make the top and bottom soft keys match. The soft key heights should be within 0.02 inches of each other.
9. Adjust the Vertical Size, A06R221, until the picture height is 3.7 inches.

NOTE

The vertical linearity and size controls interact. For proper adjustment, repeat both adjustments until both are correct.

10. Turn the rear panel CONTRAST control fully counterclockwise. Adjust the Main Brightness, A06R325, so that the background raster and retrace lines are just extinguished. Readjust the CONTRAST control to a desired level.
11. Continue with adjustment 1B.

1B. CRT: SOFT KEY SENSITIVITY ADJUST

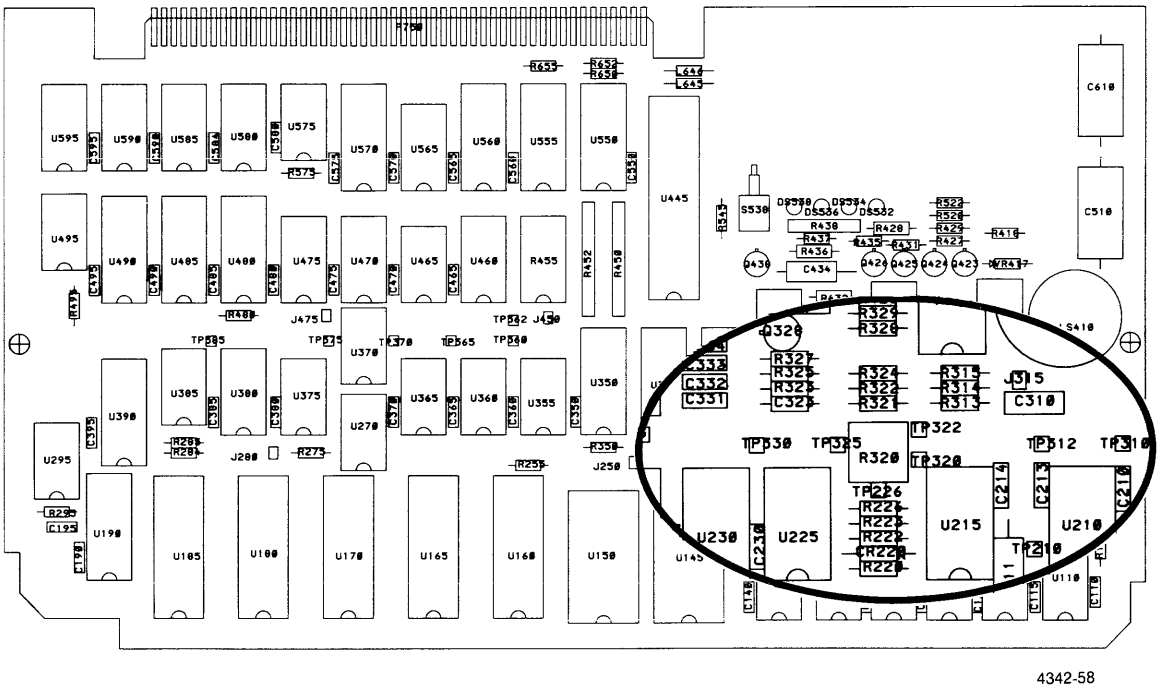


Figure 5-14. Expanded view of the I/O Processor Board shows components used in Soft Key Sensitivity Adjust.

Equipment Required

- adjustment tool
- test oscilloscope

Adjustment Procedure

1. Power down the 1240 and place the I/O Processor Board on the processor extender board (assembly A21).
2. Enter diagnostics by simulating a keyboard failure (hold down a key upon power-up). While in the Main Diagnostic menu, select the FRONTPANEL module. Touch the Module Diagnostic soft key and select the FP VERIFY area. Touch the Area Diagnostic soft key and select 2 for the routine number. Press the START key.
3. The 1240 displays a screen pattern used for adjusting the soft keys. (Refer to Figure 5-15.)

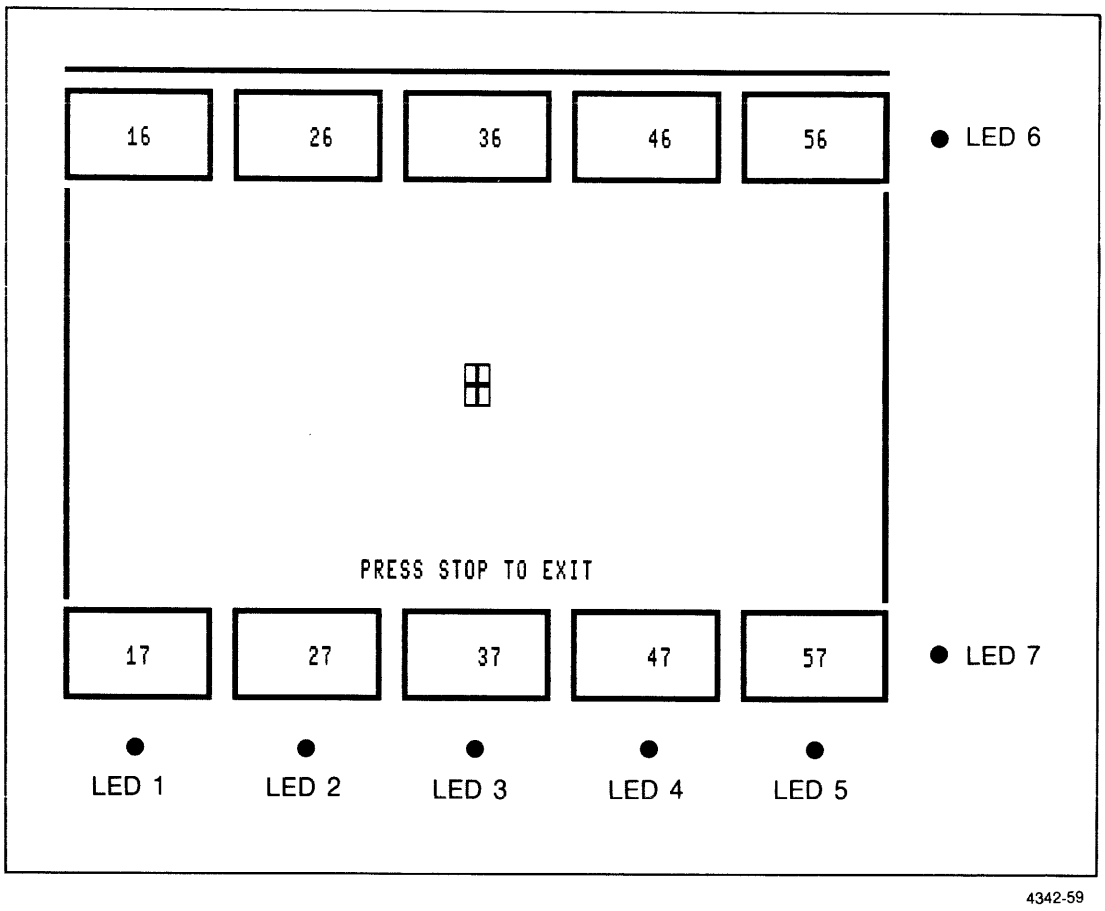


Figure 5-15. Soft key adjustment pattern showing screen boxes and corresponding LED pairs (e.g., box 17 uses LEDs 1 and 7).

4. Set up the following parameters on the oscilloscope:
   - Input sensitivity - 1 volt/div
   - Horizontal sweep - 500 μs/div
   - Display - Channel 2
   - Trigger source - Channel 1
   - Ground level - center graticule
5. On the I/O Processor Board, connect the Channel 1 probe at test point A10TP320 and the Channel 2 probe at test point A10TP322 (ground leads at TP330). Refer to Figure 5-14.
6. The oscilloscope should display seven pulses approximately 3 volts in amplitude (refer to Figure 5-16). Adjust A10R320 to center the shortest pulse around the center graticule (ground).
7. Using your forefinger, touch the center of each 1240 soft key box and check that each corresponding oscilloscope pulse goes below the ground reference line.
8. Power the 1240 down and replace the I/O Processor Board in its original slot.

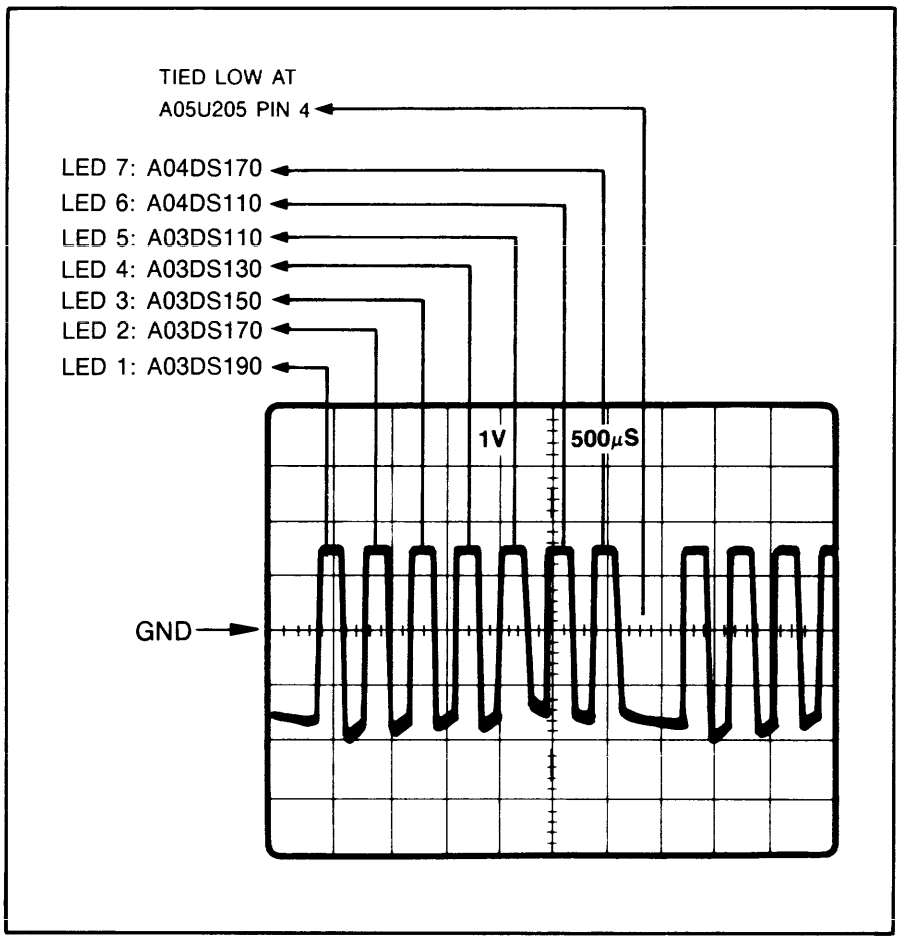


Figure 5-16. Soft key adjustment pulses and corresponding LEDs.

2. 1240D1 ACQUISITION CARD: THRESHOLD ADJUST

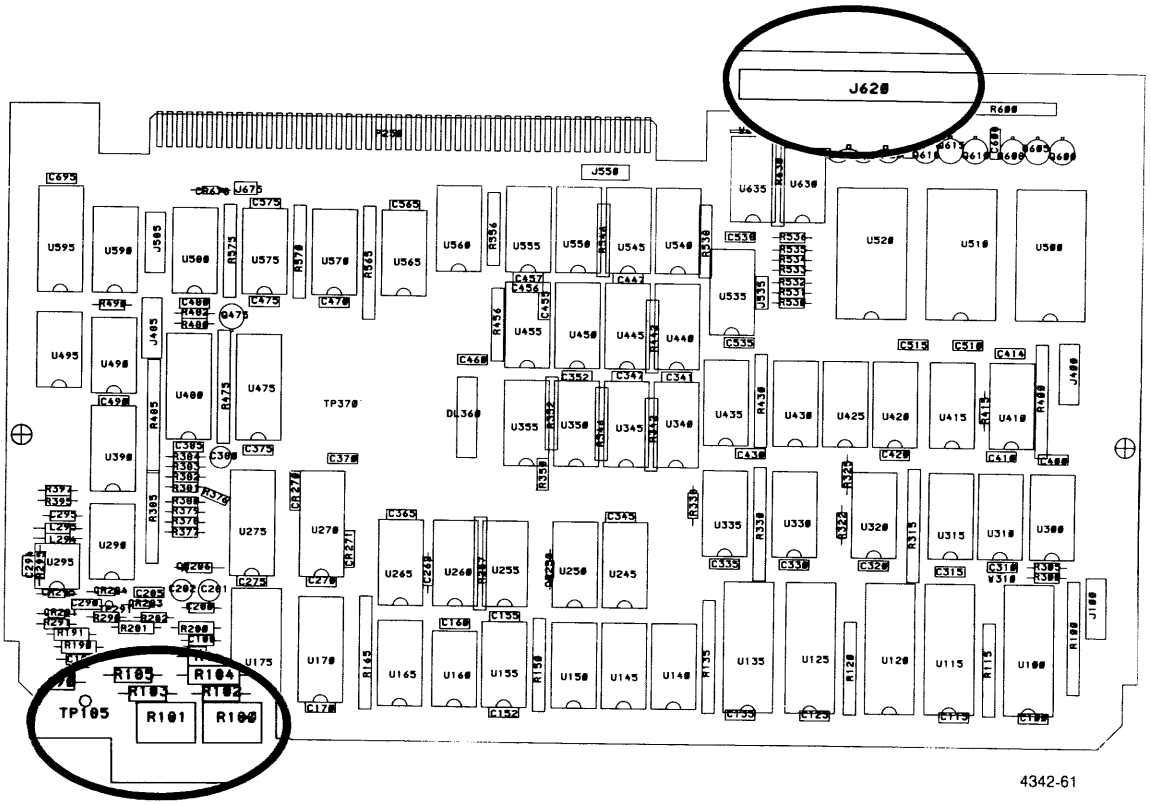


Figure 5-17. Expanded view of the 1240D1 9-Channel Acquisition Board shows components used in the Threshold Adjust.

Equipment Required

- digital multimeter
- adjustment tool
- Acquisition Threshold Fixture

Adjustment Procedure

1. Install the threshold special fixture (described previously in this section under *Constructing An Acquisition Threshold Fixture*) onto A15J620 of the 9-Channel board. Refer to Figure 5-17.
2. Power on the 1240, press the TRIGGER menu key, then touch the AUTO-RUN SPEC soft key.
3. Using the Cursor and Select keys, set the following parameters:

- AUTO-RUN CONDITION: COMPARE ACQMEM TO REFMEM
- WHEN EQUAL: DISPLAY AND REACQUIRE
- WHEN NOT EQUAL: DISPLAY AND REACQUIRE
- DISPLAY DATA FOR AT LEAST 60 SECONDS (Use a larger number if more adjustment time is required.)

4. Press the front panel AUTO key and set the following parameter:

- CARD 0: 0.0 V

5. Connect the DMM high lead at pin 13 of the threshold fixture, ground lead at the three-wire combination.

6. Adjust A15R180 for 0.00 V ± 2 mV.

7. Using the Select keys, set the following 1240 parameter:

- CARD 0: −6.35 V

8. Adjust A15R181 for +1.587 V (or as close as possible).

9. Using the Select keys, set the following 1240 parameter:

- CARD 0: +6.35 V

10. Check for −1.587 V ± 12 mV. By switching between the two range extremes, readjust for R181 (if necessary) to equalize the difference in voltage (for no more than ± 12 mV) between the two extremes at the pin 13 side of the test-fixture resistor.

11. Press the front panel STOP key.

3. 1240D2 ACQUISITION BOARD: THRESHOLD ADJUST

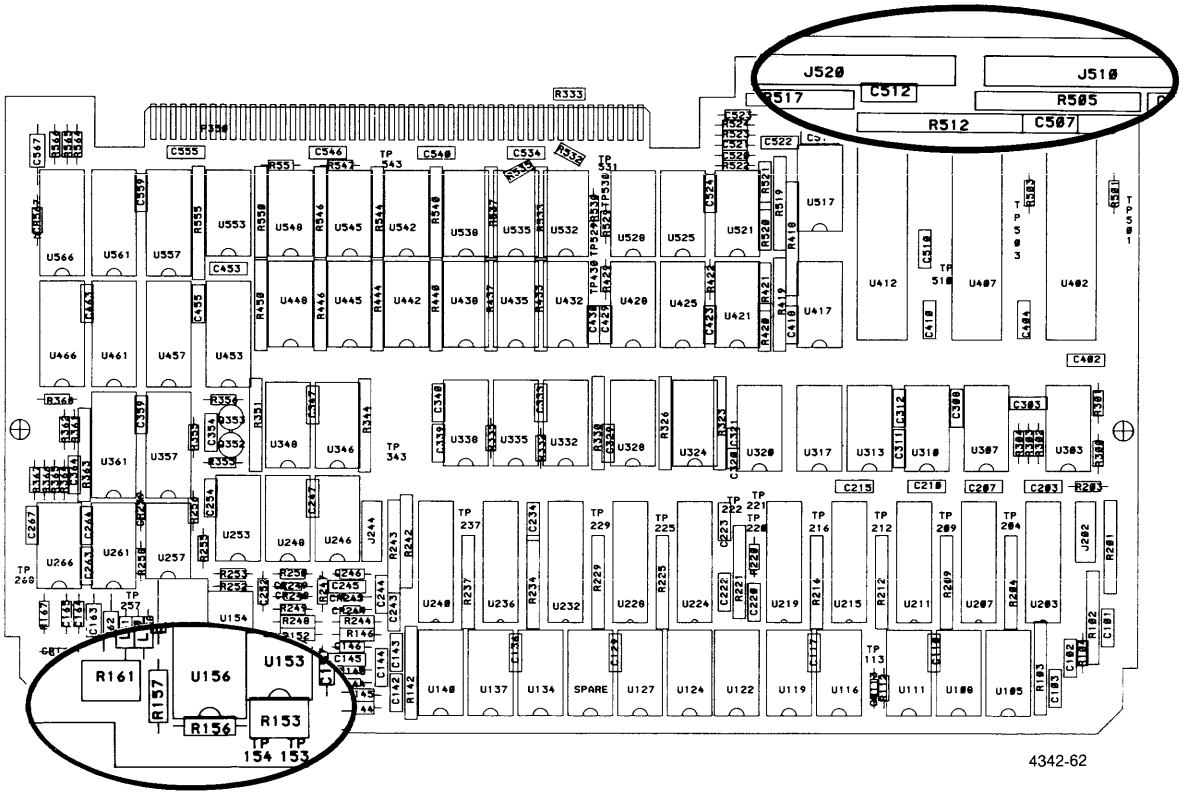


Figure 5-18. Expanded view of 1240D2 18-Channel Acquisition Board shows components used in the Threshold Adjust.

Equipment Required

- digital multimeter
- adjustment tool
- Acquisition Threshold Fixture

Adjustment Procedure

1. Install the Acquisition Threshold Fixture (previously described in this section under *Constructing An Acquisition Threshold Fixture*) onto A16J510 of the 18-Channel board. Refer to Figure 5-18.
2. Power on the 1240, press the TRIGGER menu key, then touch the AUTO-RUN SPEC soft key.
3. Using the Cursor and Select keys, set the following parameters:
   - AUTO-RUN CONDITION: COMPARE ACQMEM TO REFMEM
   - WHEN EQUAL: DISPLAY AND REACQUIRE
   - WHEN NOT EQUAL: DISPLAY AND REACQUIRE
   - DISPLAY DATA FOR AT LEAST 60 SECONDS (Use a larger number if more adjustment time is required.)
4. Press the front panel AUTO key and set the following parameter:
   - CARD 0: 0.0 V
5. Connect the DMM high lead at pin 13 of the threshold fixture, ground lead at the three-wire combination.
6. Adjust A16R161 for 0.00 V ± 2 mV.
7. Using the INCR and DECR keys, set the following 1240 parameter:
   - CARD 0: −6.35 V
8. Adjust A16R153 for +1.587 V (or as close as possible).
9. Using the INCR and DECR keys, set the following 1240 parameter:
   - CARD 0: +6.35 V
10. Check for −1.587 V ±12mV. By switching between the two range extremes, readjust for R153 (if necessary) to equalize the difference in voltage for the two settings (no more than ±12 mV from specification for each).
11. Note the adjustment error for future reference.
12. Remove the test fixture on A16J510 and install it on J520.
13. Check the threshold values at the pin 13 side of the test-fixture resistor for both ±6.35 V threshold settings. If either value is outside the ±12 mV range, compare the values to the previously noted adjustment error readings and repeat step 11.
14. If re-adjustment was necessary, recheck the setting for A16J510 to ensure it is still within specification.
15. Remove the threshold fixture.

4A. TRIGGER BOARD: TEST PATTERN GENERATOR ADJUST

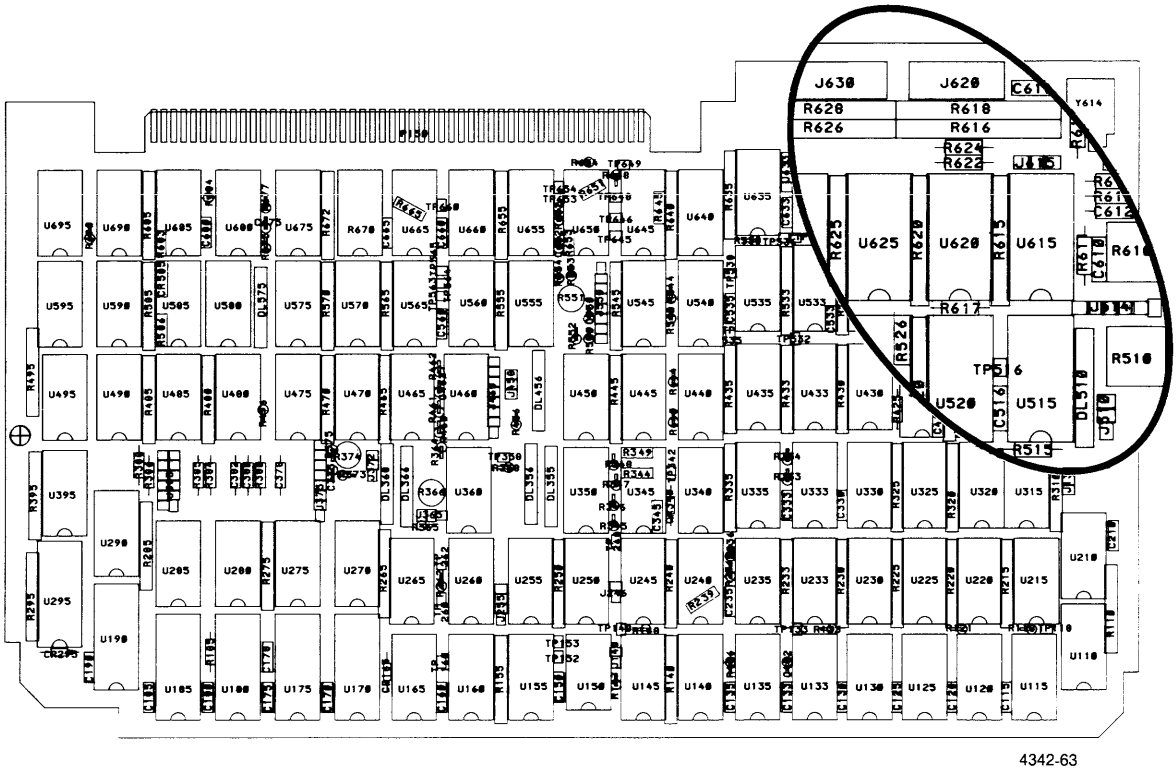


Figure 5-19. Expanded view of the Trigger Board shows components used in the TPG Adjust.

Equipment Required

- test oscilloscope
- adjustment tool
- DC 5010 Digital Counter w/P6125 probe

Adjustment Procedure

1. With the 1240 power OFF, remove the Trigger Board and replace it on the appropriate extender board (assembly A21).
2. Power on the 1240, the 1240 displays the following:
   - OPERATION LEVEL: 0
   - TPG MODE: 0
3. Press the front panel TRIGGER menu key. Using the Cursor and Select keys, set the following parameters:
   - GLOBAL EVENT: OFF
   - SEQUENTIAL EVENT: (all steps deleted using the DELETE LEVEL soft key)

4. Set up the oscilloscope as follows:
   - Input Sensitivity: 500 mV/Div
   - Timebase: 1 ns/Div
   - Trigger Mode: AUTO - INT - AC COUPLING
   - Display Mode: CHOP
   - Trigger Source: CH1
   - Trigger Slope: + (positive)
   - Input Coupling: DC
5. Connect the CH1 oscilloscope probe to A14U615 pin 1 (+5 volts), ground at A14J630 pin 12. Using the oscilloscope vertical position control, move the CH1 trace to +1.3 volts above the center graticule. Refer to Figure 5-19.
6. Repeat step 5 for the CH2 probe; ground at A14J630 pin 6.
7. Press the front panel START key.

TPG Clock/Data Delay Adjust

8. Connect the CH 1 oscilloscope probe to A14J630 pin 1, ground lead to J630 pin 12. Connect the CH 2 oscilloscope probe to A14J630 pin 2, ground lead to J630 pin 6. There should be clock and data signals 300 mV min. above and below the center graticule.
9. Move the jumper at J514 until the rising edge of the CH1 signal is approximately 1 ns before the transition of the CH2 signal.
10. Use A14R610 as a fine adjustment for bringing the delay as close to 1 ns as possible. Refer to Figure 5-20.

NOTE

As an optional TPG setting in steps 9 and 10, use 0 ns instead of 1 ns.

TPG Clock Width Adjust

11. Change the oscilloscope timebase to 2 ns/div and the display mode to CH1.
12. Move the jumper A14J510 to short pins 1 and 2 for the 12 ns adjust.
13. Adjust R510 for a 12 ns pulse ± 0.5 ns wide (as it crosses the center graticule). Refer to Figure 5-20.

NOTE

The following replacement steps are optional: Step 12 - short pins 2 and 3 for an 8 ns adjust. Step 13 - adjust R510 for 8 ns ±0.5 ns. Place jumper A14J615 to short pins 1 and 2 for normal clock at J620-1 or place the jumper to short pins 2 and 3 for inverted clock.

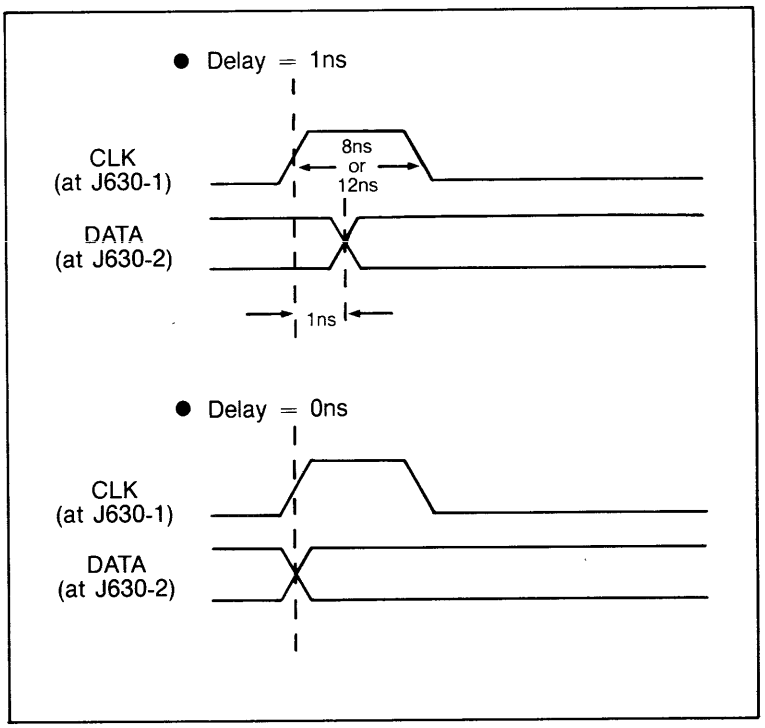


Figure 5-20. TPG clock and data delays.

TPG Clock Period Verify

14. Check to verify that A14J615 is jumpered to short pins 1 and 2.
15. Connect a P6125 probe to the DC 5010 CHA input and set the DC 5010 controls as follows:
    - CHA TERM: 1 M ohm
    - ATTENUATION: x1
    - SLOPE: POS
    - COUPLING: DC
16. Press the CHA LEVEL button (ensure it is lighted). Using the up and down arrow keys, select 0.740 volts.
17. Press the 10↑N AVGS button and using the up and down arrow keys, set the number of averages for 6 (actually ten to the sixth power).
18. Connect the CHA probe to A14J620 pin 1, ground at J620 pin 12.
19. Press the PERIOD A button and observe that the period is 83.3 ns ± 2% (81.63 ns to 84.97 ns).

TPG Glitch Verify

20. Press the CONFIG menu key and touch the Operation Level soft key.
21. Change the TPG MODE to 1 and press the START key.
22. Connect the CH1 oscilloscpe probe to A14J630-2.
23. The oscilloscope should display the TPG data with glitches. The glitches should be 6.5 ns wide at the center graticule (± 1 ns), at least 300 mV above and below center graticule.

4B. TRIGGER BOARD: TIMEBASE 1 ADJUST

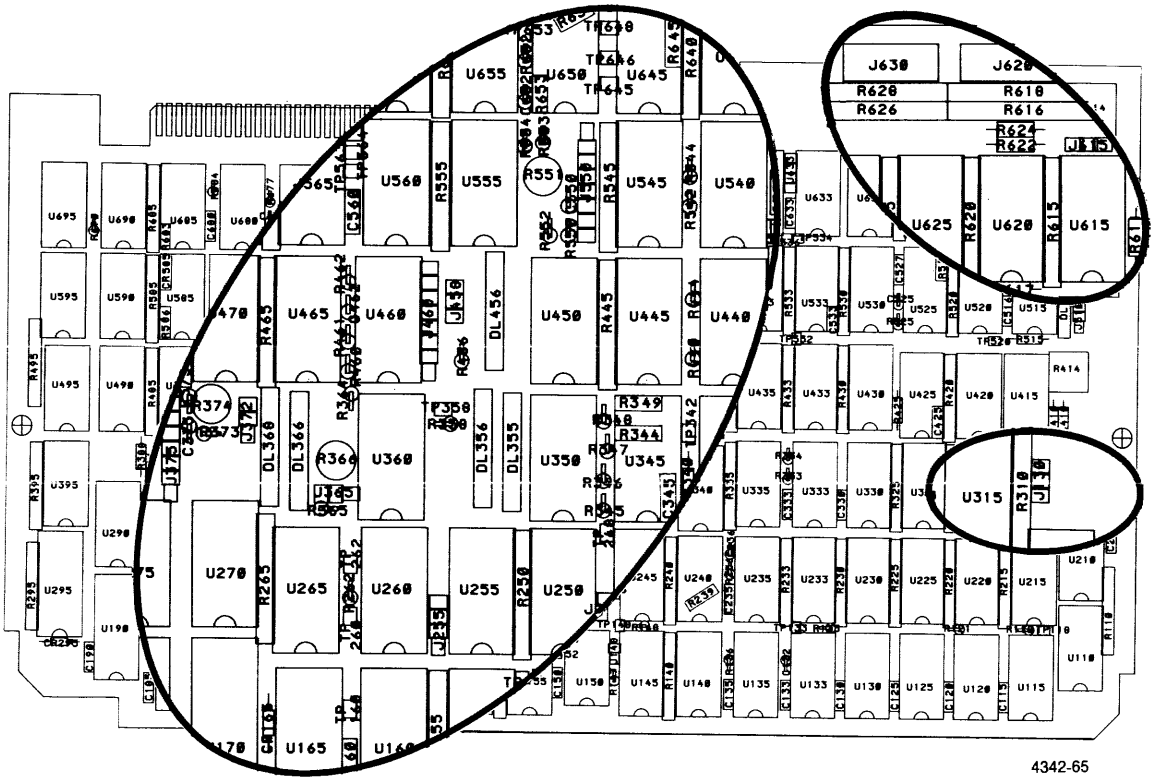


Figure 5-21. Expanded view of the Trigger Board shows components used in Timebase 1 Adjust (Board versions 670-7523-09 and below only. For subsequent versions, refer to Section 10).

Table 5-23
SUMMARY OF TIMEBASE 1 ADJUSTMENTS (670-7523-10)

NAME	CONNECTIONS	ADJUST	RESULTS
TPG T1 Clock	TP645; Gnd: TP646	J550: start 7-8	4.0-4.5 ns
ST1 Pulse Width	J310-2; Gnd: J310-3	J460: start 7-8	4.0-4.5 ns
T1 Trigger Sampler Pulse Width	TP563; Gnd: TP660	J375: start 5-6	4.0-4.5 ns
GT1 Delay	TP344; Gnd: TP248	R551/J452: start 1-2 & 3-4	15.0 ns ±0.5 ns
ST1 Delay	J310-2; Gnd: J310-3	none	20.0 ns ±0.5 ns
T1 Trigger Sampler Delay	TP563; Gnd: TP660	J255: start 1-2 & 5-6	39.5 ns ±0.5 ns

Table 5-23a
SUMMARY OF TIMEBASE 1 ADJUSTMENTS (670-7523-09 and below)

NAME	CONNECTIONS	ADJUST	RESULTS
TPG T1 Clock	TP645; Gnd: TP646	J550: start 7-8	4.0-4.5 ns
ST1 Pulse Width	J310-2; Gnd: J310-3	J460: start 7-8	4.0-4.5 ns
T1 Trigger Sampler Pulse Width	TP563; Gnd: TP564	J375: start 7-8	4.0-4.5 ns
GT1 Delay	U345-9; Gnd: TP248	R551/J458-2,3	15.0 ns ±0.5 ns
ST1 Delay	J310-2; Gnd: J310-3	none	20.0 ns ±0.5 ns
T1 Trigger Sampler Delay	TP563; Gnd: TP564	J255: start 2-3	38.5 ns ±0.5 ns

Adjustment Procedure

1. Press the front panel CONFIG menu key and touch the OPERATION LEVEL soft key.
2. Using the Cursor and Select keys, set the following parameters:
   - OPERATION LEVEL: 3
   - TPG MODE: 2
3. Touch the TIMEBASE soft key. Using the Cursor and Select keys, set the following parameters:
   - TIMEBASE: T1 AND T2
   - T1: ASYNC - (any value)
   - T2: SYNC - rising on P0
4. Touch the MEMORY CONFIG soft key. Using the Cursor and Select keys, set the following parameters:
   - CARD THRESHOLD: TPG
   - TIMEBASE (all pods): T2
   - GLITCHES: OFF
5. Touch the TIMEBASE soft key again. Using the Cursor and Select keys, set the following parameter:
   - TIMEBASE T1: ASYNC - 10 ns
6. Press the front panel TRIGGER menu key. Ensure the following parameters:
   - GLOBAL EVENT: OFF
   - SEQUENTIAL EVENT: (all steps deleted)
7. Setup the oscilloscope as follows:
   - Input Sensitivity: 500 mV/Div
   - Timebase: 1 ns/Div
   - Display Mode: CHOP
8. Connect the CH1 oscilloscope probe to A14U615 pin 1 (+ 5 volts), ground at A14J630 pin 12. Using the oscilloscope vertical position control, move the CH1 trace to +1.3 volts above the center graticule. Refer to Figure 5-21.
9. Repeat step 8 for the CH2 probe; ground at A14J630 pin 6.
10. Press the START key.

T1 (for TPG) Pulse Width Adjust

11. Connect the CH1 oscilloscope probe to A14TP645, ground to TP646.
12. Move the jumper A14J550 to short pins 7 and 8.
13. Verify that pulses are 4.0 ns to 4.5 ns wide and the repetition rate is 10 ns.
14. If pulses do not meet the stated width and repetition rate, move the jumper J550 to short pins 5 and 6 and re-check.
15. If necessary, continue moving jumper to next set of pins until the pulse width and repetition rate conditions are met. Refer to Figure 5-22.

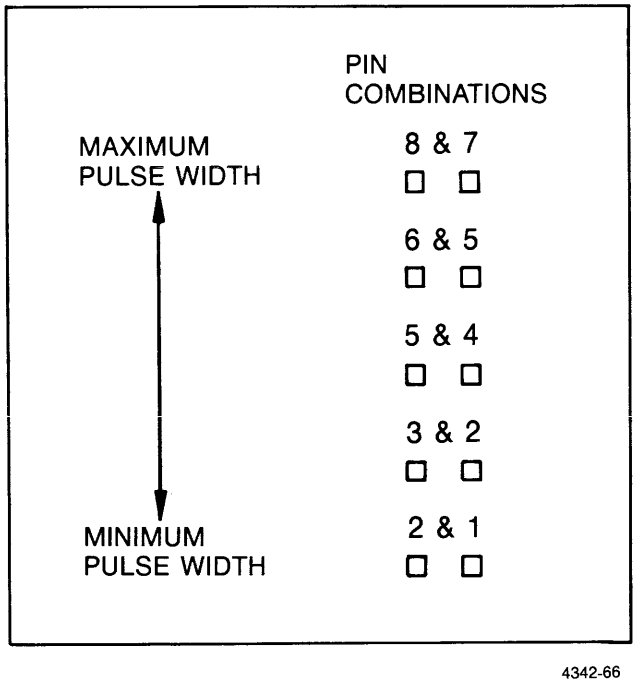


Figure 5-22. Pin combinations for Timebase 1 adjust. (Note: A14J375 on board version 670-7523-10 does not have pins 7 and 8.)

ST1 Pulse Width Adjust

16. Move the CH1 oscilloscope probe to A14J310 pin 2; ground at J310-3.
17. Move the jumper A14J460 to short pins 7 and 8.
18. Verify that pulses are 4.0 ns to 4.5 ns wide and the repetition rate is 10 ns.
19. If pulses do not meet the stated width and repetition rate, move the jumper J460 to short pins 5 and 6 and re-check.
20. If necessary, continue moving jumper to next set of pins until the pulse width and repetition rate conditions are met.

T1 Trigger Sampler Pulse Width Adjust (670-7523-10)

21. Move the CH1 oscilloscope probe to A14TP563; ground at TP660.
22. Move the jumper A14J375 to short pins 5 and 6.
23. Verify that pulses are 4.0 ns to 4.5 ns wide and the repetition rate is 10 ns.
24. If pulses do not meet the stated width and repetition rate, move the jumper J375 to short pins 3 and 4 and re-check.
25. If necessary, continue moving jumper to next set of pins until the pulse width and repetition rate conditions are met.
26. Press the STOP key.

T1 Trigger Sampler Pulse Width Adjust (670-7523-09 and below)

21. Move the CH1 oscilloscope probe to A14TP563; ground at TP660.
22. Move the jumper A14J375 to short pins 7 and 8.
23. Verify that pulses are 4.0 ns to 4.5 ns wide and the repetition rate is 10 ns.
24. If pulses do not meet the stated width and repetition rate, move the jumper J375 to short pins 5 and 6 and re-check.
25. If necessary, continue moving jumper to next set of pins until the pulse width and repetition rate conditions are met.
26. Press the STOP key.

GT1 Delay Adjust (670-7523-10)

26. Press the CONFIG menu key and touch the TIMEBASE soft key. Using the Cursor and Select keys, set the following parameter:

- TIMEBASE T1: ASYNC - 50 ns

27. Press the START key.
28. Connect the CH1 oscilloscope probe to A14TP648, ground at TP646. Connect the CH2 probe to A14TP344, ground at TP248.
29. Change the oscilloscope timebase to 5 ns/Div.

30. Move the jumper A14J452 to short pins 1 and 2 and pins 3 and 4. Adjust A14R551 for a delay of 15.0 ns ± 0.5 ns between the rising edges of the CH1 and CH2 signals.

31. If the delay is greater than 15.5 ns, move the jumper A14J452 to short pins 2 and 3 and pins 1 and 4. Readjust A14R551 to achieve 15.0 ns ± 0.5 ns.

GT1 Delay Adjust (670-7523-09 and below)

26. Press the CONFIG menu key and touch the TIMEBASE soft key. Using the Cursor and Select keys, set the following parameter:

- TIMEBASE T1: ASYNC - 50 ns

27. Press the START key.

28. Connect the CH1 oscilloscope probe to A14TP648, ground at TP646. Connect the CH2 probe to A14U345 pin 9, ground at TP248.

29. Change the oscilloscope timebase to 5 ns/Div.

30. Move the jumper A14J458 to short pins 2 and 3 and adjust A14R551 for a delay of 15.0 ns ± 0.5 ns between the rising edges of the CH1 and CH2 signals.

31. If the delay is greater than 15.5 ns, move the jumper A14J458 to short pins 1 and 2. Readjust A14R551 to achieve 15.0 ns ± 0.5 ns.

NOTE

If proper delay cannot be achieved with A14R551 adjusted to no greater than midrange (approximately 100 ohms), contact your local Tektronix Service Center.

ST1 Delay Verify

32. Move the CH2 oscilloscope probe to A14J310 pin 2 (ground at J310-3) and verify a delay of 20.0 ns ± 0.5 ns between the rising edges of CH1 and CH2 signals.

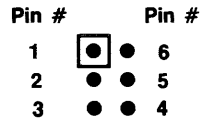
T1 Trigger Sampler Delay Adjust (670-7523-10)

33. Move the CH2 oscilloscope probe to A14TP563; ground at TP660.

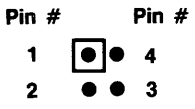
34. Move jumper A14J255 to short pins 1 and 2 and pins 5 and 6.

35. Verify that the delay between the rising edges of the CH1 and CH2 signals is 39.5 ns ± 0.5 ns.

36. If the delay is less than 39.5 ns, remove the jumper on A14J255 shorting pins 1 and 2 and pins 5 and 6. Now, short pins 2 and 3 and pins 4 and 5. If the delay is greater than 39.5 ns, short pins 2 and 5. Store the unused jumper across pins 1 and 6 (shorting these pins has no effect on the delay).



A14J255 Pin Layout



A14J452 Pin Layout

37. Again, verify that the delay between the rising edges of the CH1 and CH2 signals is 39.5 ns ± 0.5 ns.

38. Press the STOP key.

T1 Trigger Sampler Delay Adjust (670-7523-09 and below)

33. Move the CH2 oscilloscope probe to A14TP563; ground at TP564.

34. Move jumper A14J255 to short pins 2 and 3.

35. Verify that the delay between the rising edges of the CH1 and CH2 signals is 38.5 ns ± 0.5 ns.

36. If the delay is less than 38.0 ns, remove the jumper on A14J255 shorting pins 2 and 3. Now, short pins 1 and 2, as well as 3 and 4. If an additional jumper is not available, short the two pins on the back side of the board with a short piece of strapping wire.

37. Again, verify that the delay between the rising edges of the CH1 and CH2 signals is 38.5 ns ± 0.5 ns.

38. Press the STOP key.

4C. TRIGGER BOARD: TIMEBASE 2 ADJUST

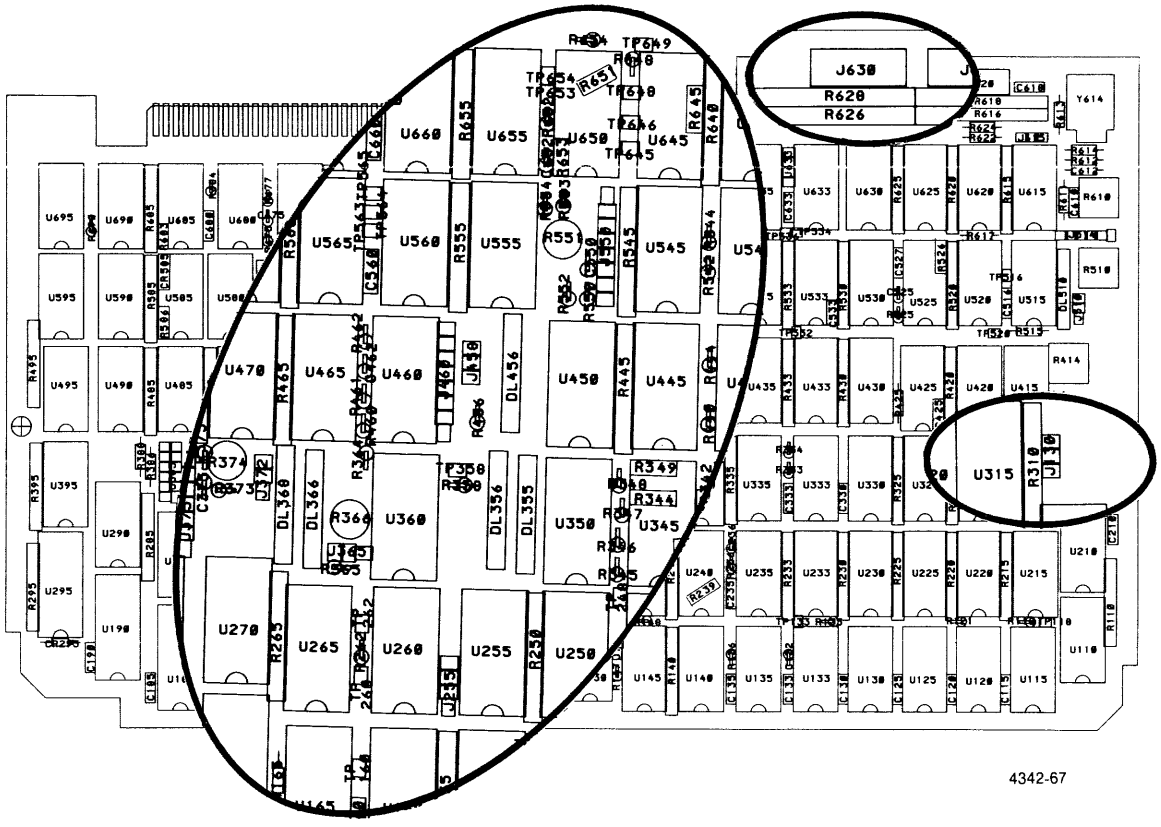


Figure 5-23. Expanded view of the Trigger Board shows components used in Timebase 2 Adjust (Board versions 670-7523-09 and below. For version 670-7523-10, refer to Section 10).

Table 5-24
SUMMARY OF TIMEBASE 2 ADJUSTMENTS (670-7523-10)

NAME	CONNECTIONS	ADJUST	RESULTS
GT2 Delay	TP343; Gnd: TP248	R374/J372-2,3	15.0 ns ±0.5 ns
ST2 Delay	J310-1; Gnd: J310-3	none	20.0 ns ±0.5 ns
T2 Trigger Sampler Delay	TP262; Gnd: TP260	R366/J365-2,3	39.0 ns ±0.5 ns

Table 5-24a
SUMMARY OF TIMEBASE 2 ADJUSTMENTS (670-7523-09 and below)

NAME	CONNECTIONS	ADJUST	RESULTS
GT2 Delay	UJ345-11; Gnd: TP248	R374/J372-2,3	15.0 ns ±0.5 ns
ST2 Delay	J310-1; Gnd: J310-3	none	20.0 ns ±0.5 ns
T2 Trigger Sampler Delay	TP262; Gnd: TP260	R366/J365-2,3	38.5 ns ±0.5 ns

Adjustment Procedure

1. Ensure that the timebase parameter setup in 4B. Trigger Board: Timebase 1 Adjust is still set at T1: ASYNC - 50 ns and T2: SYNC - rising on P0.
2. Connect the P6460 Data Acquisition Probe from the acquisition card's P0 connector to the TPG connector A14J630 on the Trigger Board (refer to Figure 5-23). Press the START key.

GT2 Delay Adjust (670-7523-10)

3. Connect the CH1 oscilloscope probe to A14TP654, ground to TP649. Connect the CH2 probe to A14TP343, ground at TP248.
4. Change the oscilloscope timebase to 5 ns/div. Move jumper A14J372 to short pins 2 and 3 together.
5. Adjust A14R374 for a delay of 15.0 ns ± 0.5 ns between the rising edges of CH1 and CH2 signals.
6. If the delay is more than 15.5 ns, move jumpers on A14J372 to short pins 1 and 2. Readjust R374 for a delay of 15.0 ns ±0.5 ns between CH1 and CH2 signals.

GT2 Delay Adjust (670-7523-09 and below)

3. Connect the CH1 oscilloscope probe to A14TP654, ground to TP649. Connect the CH2 probe to A14U345 pin 11, ground at TP248.
4. Change the oscilloscope timebase to 5 ns/div. Move jumper A14J372 to short pins 2 and 3 together.
5. Adjust A14R374 for a delay of 15.0 ns ± 0.5 ns between the rising edges of CH1 and CH2 signals.
6. If the delay is more than 15.5 ns, move jumpers on A14J372 to short pins 1 and 2. Readjust R374 for a delay of 15.0 ns ±0.5 ns between CH1 and CH2 signals.

ST2 Delay Verify

7. Move the CH2 oscilloscope probe to A14J310-1; ground at J310-3.
8. Verify a delay of 20.0 ns ±0.5 ns.

T2 Trigger Sampler Delay Adjust (670-7523-10)

9. Move the CH2 oscilloscope probe to A14TP262, ground at TP260.
10. Move the jumper on A14J365 to short pins 2 and 3. Adjust A14R366 for a delay of 39.0 ns ± 0.50 ns between rising edges of the CH1 and CH2 signals.
11. If the delay is more than 39.0 ns, move the jumper on A14J365 to short pins 1 and 2. Re-adjust A14R366 for a delay of 39.0 ns ± 0.5 ns.
12. Press the STOP key.

T2 Trigger Sampler Delay Adjust (670-7523-09 and below)

9. Move the CH2 oscilloscope probe to A14TP262, ground at TP260.
10. Move the jumper on A14J365 to short pins 2 and 3. Adjust A14R366 for a delay of 38.5 ns ± 0.50 ns between rising edges of the CH1 and CH2 signals.
11. If the delay is more than 39.0 ns, move the jumper on A14J365 to short pins 1 and 2. Re-adjust A14R366 for a delay of 38.5 ns ± 0.5 ns.
12. Press the STOP key.

4D. TRIGGER BOARD: SEQUENTIAL TIMING ADJUST

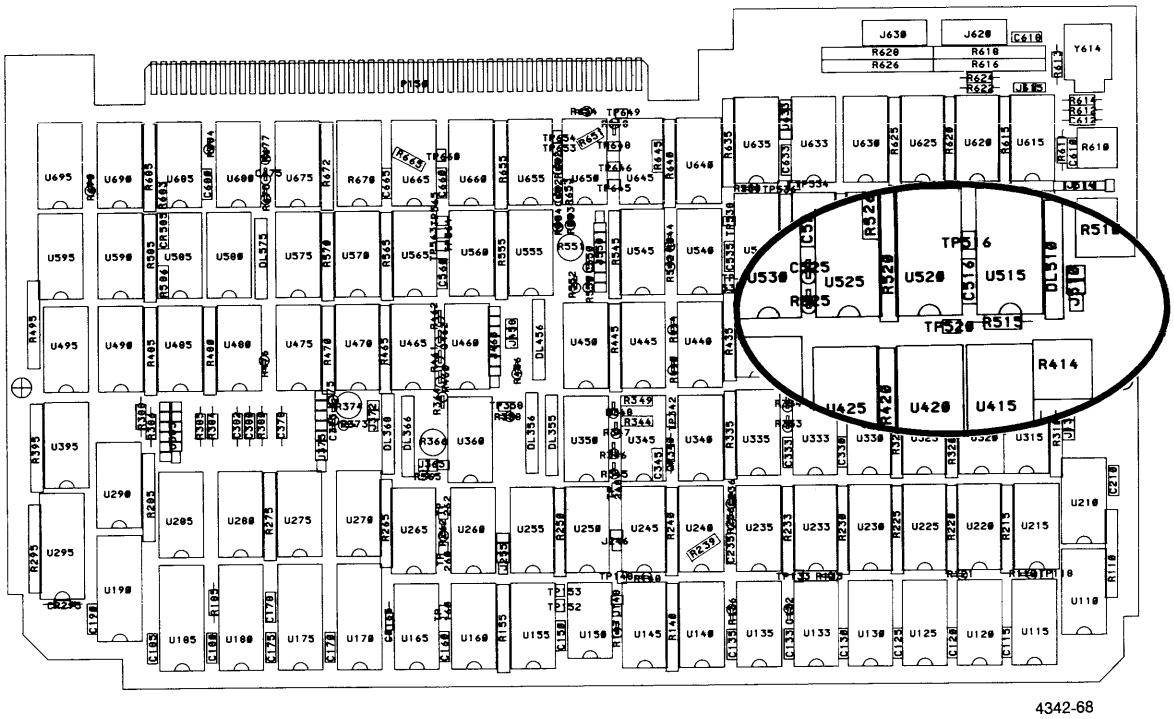


Figure 5-24. Expanded view of the Trigger Board shows components used in the Sequential Timing Adjust.

Adjustment Procedure

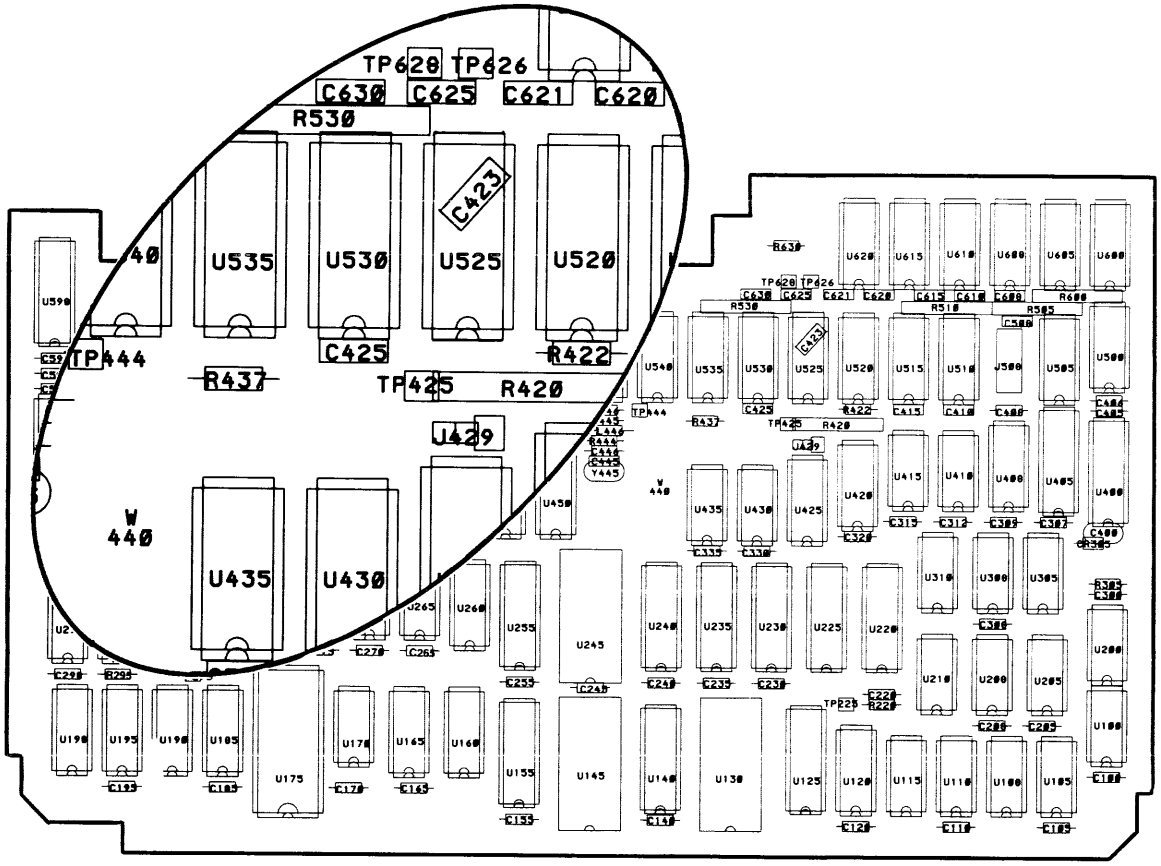
1. Press the front panel TRIGGER menu key and make the following parameter changes:

   • SEQUENTIAL EVENT: 1/ T2 JUMP IF XX X

   TO LEVEL 1
   ELSE DO NOTHING

2. Connect the CH1 oscilloscope probe to A14U525 pin 2; ground at TP516. Refer to Figure 5-24.
3. Change the test oscilloscope timebase to 1 ns/div.
4. Press the START key and adjust A14R414 for a pulse width (negative going) of 4.0 ns.

5. DISPLAY BOARD: COUNTER/TIMER ADJUST (670-7525-04)



5378-17

Figure 5-25a. Expanded view of the Display Board shows components used in the Counter/Timer Adjust.

Equipment Required

- test oscilloscope
- P6106 probe

Adjustment Procedure

1. Power down the 1240 and remove the Display Board.
2. Replace the Display Board on the appropriate extender board (assembly A21) and power up the 1240 in NORMAL OPERATION mode.
3. Press the front panel TRIGGER menu key and set the following parameters:
   - GLOBAL EVENT: START TIMER ON XX X
     DO NOTHING
   - SEQUENTIAL EVENT: (all steps deleted using the DELETE LEVEL soft key)
4. Press the START key and set the oscilloscope timebase to 1 ns/div.
5. Connect the CH1 oscilloscope probe to the Display Board at TP626, ground at TP628. Connect the CH2 probe to the Display Board at TP425, ground at TP444.

NOTE

Because probe loading affects the measurement, use only P6106 probes.

6. Check that the rising edge of the CH2 signal occurs 2.5 ns ± 0.5 ns before the signal transition on CH1. Record the measurement. If the measurement is not out of tolerance, continue to adjustment #6 for the CRT Drive Board. If it is out of tolerance, the amount of delay through A12W440 should be changed by restrapping W440.

7. Before restrapping, power-down the instrument. Note the current delay strapping on A12W440. If no restrapping has been previously performed, W440 will have circuit-board runs that strap for a nominal 2.0 ns of added delay. If W440 has been previously restrapped, compare the strapping connections to those shown in the table to find the current delay setting.

ADDED DELAY	W440 STRAPPING
0.0 ns	1-8
0.5 ns	1-4 & 5-8
1.0 ns	1-6 & 7-8
1.5 ns	1-2 & 3-8
2.0 ns (nominal set)	1-2 & 3-4 & 5-8
2.5 ns	1-2 & 3-6 & 7-8
3.0 ns	1-2 & 3-4 & 5-6 & 7-8

8. If the delay measured in step 6 was less than 2.0 ns, restrap W440 from the current setting to increase the delay by 0.5 ns. If the delay measured in step 6 was more than 3.0 ns, restrap W440 from the current setting to decrease the delay by 0.5 ns. Find the desired delay value and corresponding strapping information in the strapping table.

9. To restrap, first disconnect the undesired current strapping connections by unsoldering W440 strapping wires or cutting circuit-board runs on W440. Then use 26-guage wire to restrap W440 for the desired new delay setting determined in step 8.

10. After restrapping is complete, repeat step 6 to verify that the delay is within tolerance.

5. DISPLAY BOARD: COUNTER/TIMER ADJUST (670-7525-03)

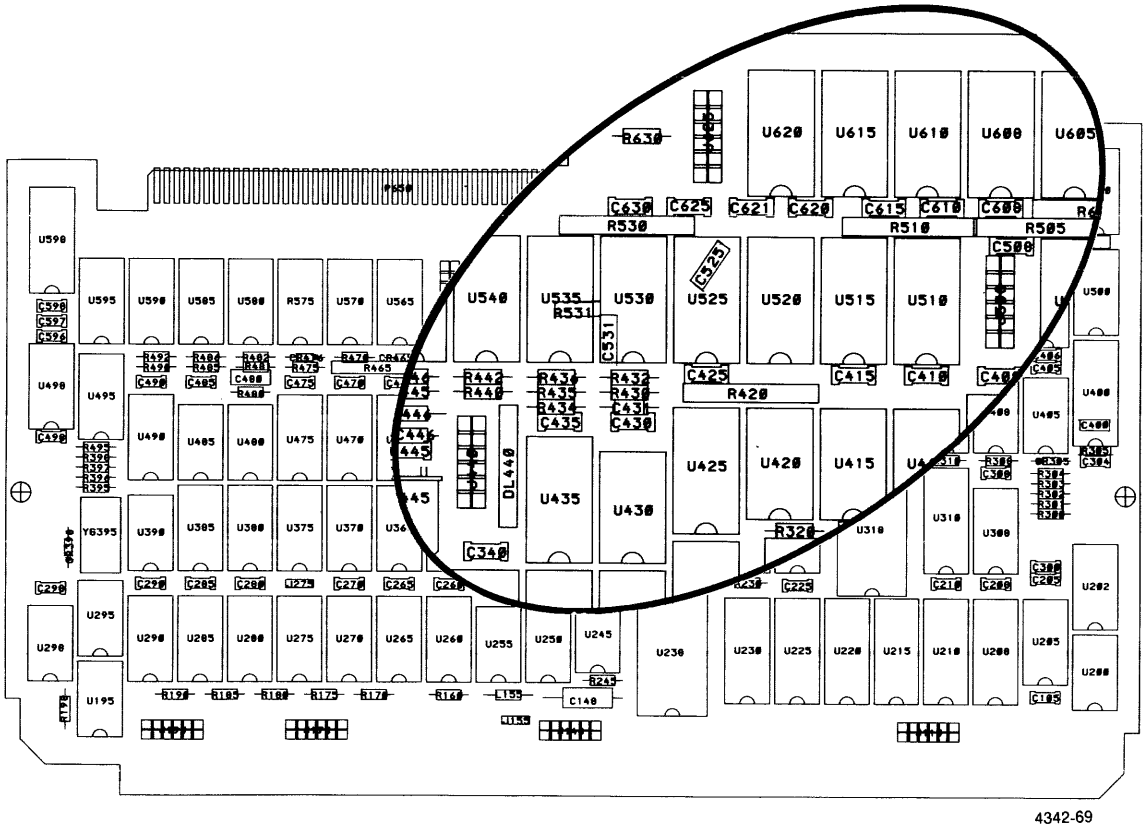


Figure 5-25b. Expanded view of the Display Board shows components used in the Counter/Timer Adjust.

Equipment Required

- test oscilloscope

Adjustment Procedure

1. Power down the 1240 and remove the Display Board.
2. Replace the Display Board on the appropriate extender board (assembly A21) and power up the 1240 in NORMAL OPERATION mode.
3. Press the front panel TRIGGER menu key and set the following parameters:

- GLOBAL EVENT: START TIMER ON XX X
  DO NOTHING
- SEQUENTIAL EVENT: (all steps deleted using the DELETE LEVEL soft key)

4. Press the START key and set the oscilloscope timebase to 1 ns/div.
5. Connect the CH1 oscilloscope probe to the Display Board at J508 pin 2, ground at J508 pin 12 (refer to Figure 5-25). Connect the CH2 probe to the Display Board at A11U525 pin 13, ground at A11J625 pin 12.
6. Move the jumper on A11J440 until the rising edge of the CH2 signal is 3.0 ns ± 0.5 ns before the transition of the CH1 signal.
7. Press the STOP key.

6. CRT DRIVE BOARD: EXTERNAL TRIGGER ADJUST

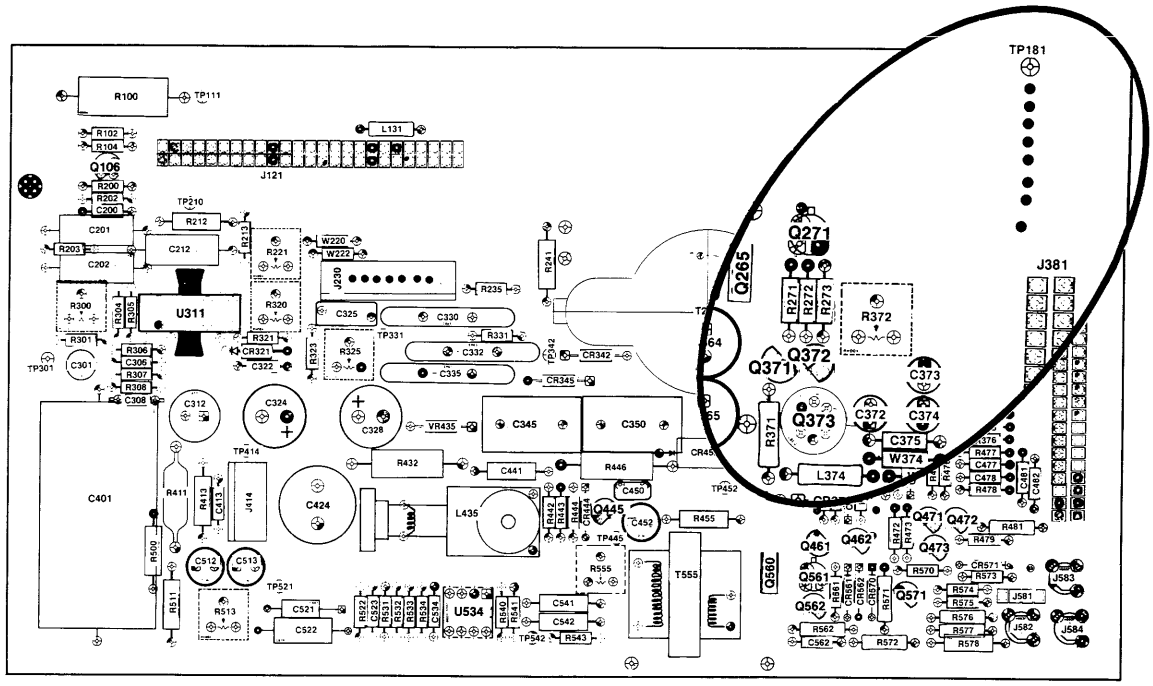


Figure 5-26. Expanded view of the CRT Drive Board shows components used in the External Trigger Adjust.

Equipment Required

- digital multimeter
- adjustment tool

Adjustment Procedure

1. Access the CRT module by removing the CRT Drive Board bracket. Refer to the *Disassembly And Installation Procedures* section for specific removal procedures.
2. Set the DMM to the 200 mV range. Connect the DMM high lead to the end of R371 (effectively the base of transistor Q372), the low lead to TP181. Refer to Figure 5-26.
3. Adjust R372 for a reading of 0.000 V (± 2 mV).

SECTION 6 DISASSEMBLY AND INSTALLATION PROCEDURES

SECTION 6 DISASSEMBLY AND INSTALLATION PROCEDURES

DISASSEMBLY/INSTALLATION PROCEDURES

OVERVIEW

In the following procedures, directional terms (top, bottom, left, right, etc.) are based on the assumption that your 1240 is in a normal, upright position and that you are facing the front of the instrument.

Installation or reassembly procedures are the reverse of the disassembly procedures unless otherwise noted. In some cases, installation hints are provided to aid in reassembly procedures.

CAUTION

Dangerous electric-shock hazards inside the mainframe may be exposed when the covers are removed. Be sure both front and rear panel power switches are off and the power cord is disconnected before removing the covers. Disassembly procedures should only be attempted by qualified service personnel.

WARNING

A lighted or blinking neon lamp on the power supply board, visible through a hole on the power supply cover adjacent to the warning label, indicates that a lethal voltage is present on that board. Wait for at least 15 minutes after power-down before accessing the power supply or related assemblies.

GENERAL DISASSEMBLY/INSTALLATION PRECAUTIONS

- DO NOT attempt any disassembly or installation procedures if power is ON.
- DO NOT operate the 1240 with the cabinet removed or the card cage in the service position (rolled out) unless additional instrument cooling is provided. Refer to the information provided in the *Verification and Adjustment Procedures* section of this manual.
- DO NOT place the 1240 onto its front face with the front panel removed. Damage may result due to excessive force on boards and components.
- DO NOT place the instrument onto its front face without covering the emblem; abrasion may wear off the coloring. To protect the front face, install the front panel cover.
- DO NOT exceed the following torque values when re-assembling any 1240 plastic parts:

PLASTIC AREA	MAX. TORQUE (IN/LBS)
Mainframe	4.5
Card cage	4.5
Power supply	3.0
Control Processor Board.	4.5
COMM packs	4.5
ROM or RAM packs	4.5

- DO NOT disconnect probes from the side of the 1240 by pulling on the cables; pull only on the plastic cable holders.
- DO NOT press or pull on components when manipulating circuit boards.
- GUARD against static discharge damage by following the precautions listed in the *Maintenance* section.

TOOLS REQUIRED

- magnetic screwdriver, 1/4 inch drive
- POZIDRIV-type bit #1
- POZIDRIV-type bit #2
- Phillips-type bit #0
- Allen wrench, 1/16 inch
- flat-blade screwdriver

PROCEDURE #1: CABINET

DISASSEMBLY

1. Remove the six #6 pan-head screws holding the rear cabinet frame ring. Remove the frame ring.
2. Remove the two #6 pan-head screws holding the probe guide and remove the probe guide from the 1240.
3. Position the carrying handle over the top of the 1240.
4. Slide the cabinet off toward the rear of the instrument.

INSTALLATION HINTS

- Ensure cabinet is fitted into front panel frame ring before installing the rear frame ring.
- Before installing the center-bottom frame-ring screw, ensure hole alignment by compressing the sides of the instrument.

PROCEDURE #2: REAR PANEL

DISASSEMBLY

1. Perform Procedure #1.
2. Remove the four corner hex posts from the rear panel.
3. Remove the CONTRAST knob using the Allen wrench.
4. Remove the rear panel.

WARNING

After removal of the rear panel, the cooling fan blades are not completely shielded. Guard against injury by keeping fingers and loose objects away from the moving fan blades.

PROCEDURE #3: CARD CAGE ROLL

DISASSEMBLY

1. Perform Procedure #1. If Procedure #2 has been performed, continue to the next step. If not, remove the two hex posts on the card-cage side of the rear panel.
2. Remove the three #4 flat-head screws shown in Figure 6-1.
3. Roll the card cage out to the upright service position.

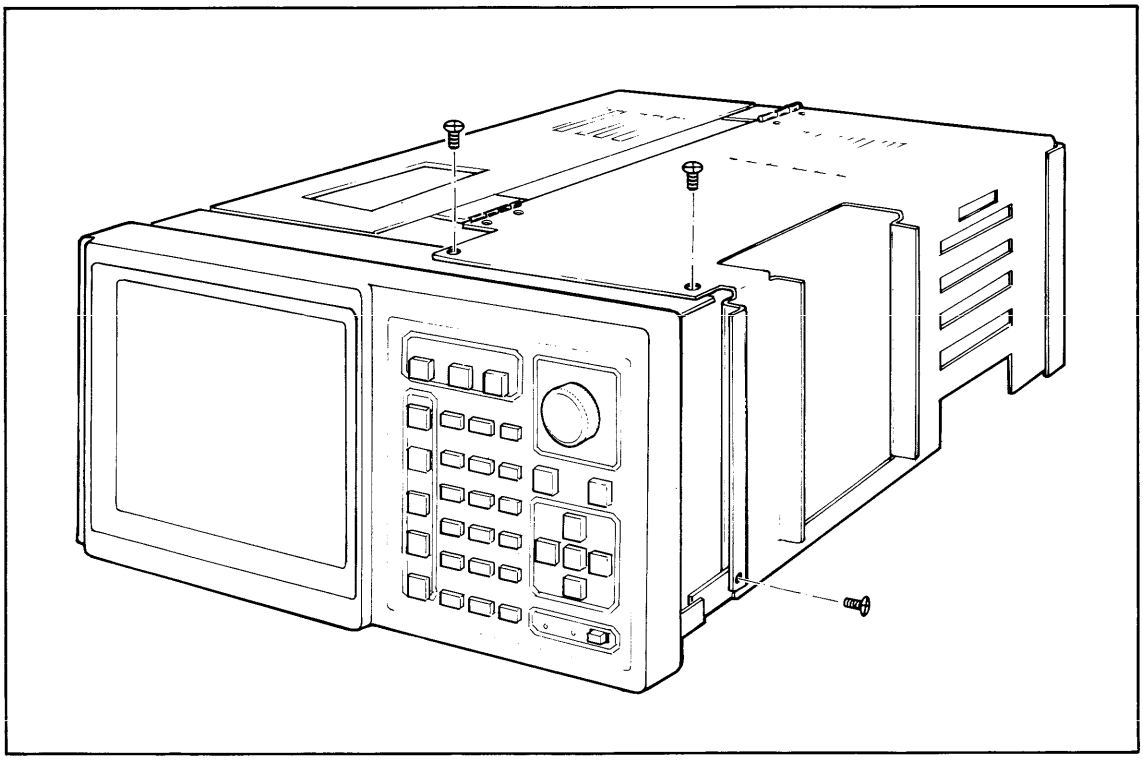


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Figure 6-1. Location of screws for card cage roll.

PROCEDURE #4: BOARD REMOVAL

DISASSEMBLY

1. Perform Procedures #1 and #3.
2. Remove the two #4 flat-head screws holding the board guide in place.
3. Grasp the two board ejector tabs for the board being removed. Swing each tab outwards until the board becomes freed from the edge connector.

INSTALLATION HINTS

CAUTION

1240 cards operate only in specific card-cage slots. If you apply power to a card installed in the wrong slot, the card will be damaged. To prevent damage, follow the card-slot assignments shown in Figure 6-2. (There is an exception for the Control and I/O Processor Boards; refer to Soft Key Sensitivity Adjust *in Section 5 for details.) If the number of acquisition cards is being changed, refer to the* Maintenance *section for power supply load-jumper information.*

- Install the boards in a top-down fashion according to the following list:

  Control Processor Board
  I/O Processor Board
  Display Board
  Acquisition Board (slot 3*)
  Acquisition Board (slot 2*)
  Acquisition Board (slot 1*)
  Acquisition Board (slot 0*)
  Trigger Board

- For * acquisition slots, install acquisition cards in every slot starting from the trigger card. (The trigger card is on the bottom when the card cage is in its rolled out position.) All unused slots should be next to the display board. Refer to Figure 6-2 for a map of the card-cage slots (in the service position).

NOTE

If your instrument contains 18-channel cards, it will be necessary to remove them before installing new 9-channel cards in order to follow these installation rules correctly.

- Replace the circuit board guide before closing the card cage.

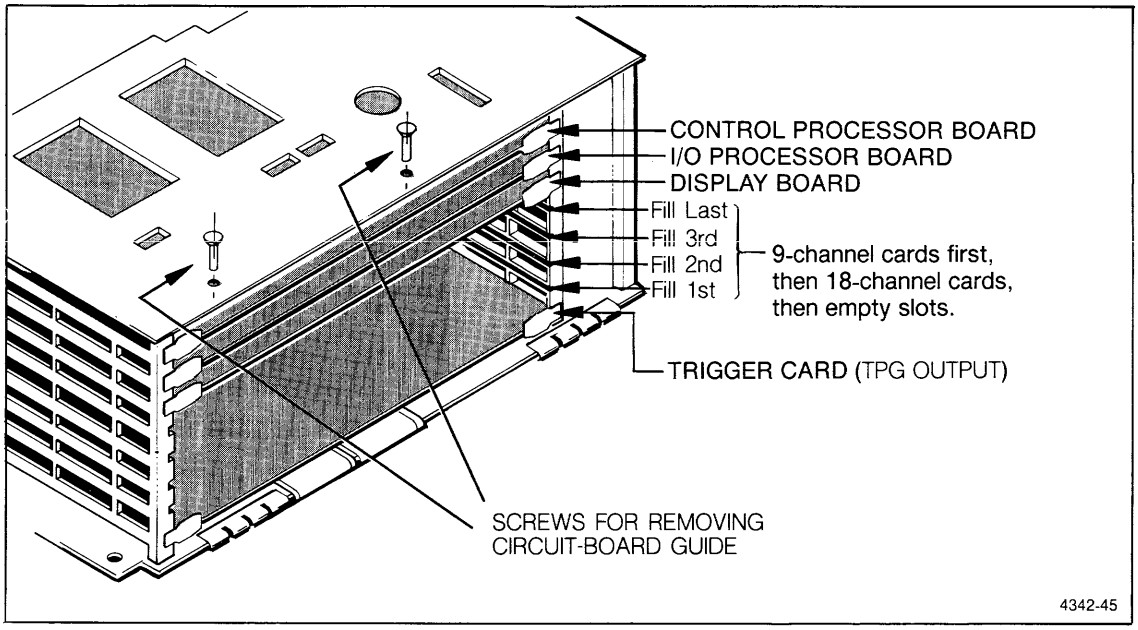


Figure 6-2. 1240 card-cage board assignments.

PROCEDURE #5: FRONT PANEL

DISASSEMBLY

1. Perform Procedures #1 and #3.
2. From the back side of the front panel, disconnect the cables at P125 and P218 on the Keyboard.
3. From the back side of the front panel, remove the four #6 pan-head screws (this releases the Keyboard for removal).
4. Swing open the front panel frame until the tab along the left-side releases.

CAUTION

Do not place the instrument on its front face with the front panel removed. Damage to the power switch or LED/Phototransistor Boards may result.

INSTALLATION HINTS

- Remove the POWER switch cap from the switch shaft before installing the front panel.
- Place front panel onto the mainframe along the left-hand side first, then swing the front panel closed.
- Replace the POWER switch cap with the word OFF facing up.

PROCEDURE #6: KEYBOARD

DISASSEMBLY

1. Perform Procedures #1, #3, and #5.
2. Remove the SCROLL knob using the Allen wrench.
3. Remove the four hex posts holding the Keyboard.

INSTALLATION HINTS

- When placing the Keyboard into the front panel, partially tighten the keyboard hex posts, then check for proper key action (no sticking keys). Continue and tighten the Keyboard hex posts.
- Position the SCROLL knob with approximately 0.05 inches of space between it and the front-panel surface before tightening.

PROCEDURE #7: LED/PHOTOTRANSISTOR BOARDS

DISASSEMBLY

1. Perform Procedures #1, #3, and #5.
2. Disconnect the cable at A4P150 on the LED-2 Board.
3. Remove the four #6 pan-head tapping screws holding the LED/PT boards and light filter to the CRT retainer ring.

WARNING

USE EXTREME CAUTION WHEN WORKING AROUND THE CRT. Do not nick or scratch the glass or subject it to undue pressures. Rough handling may cause it to violently implode. Always replace the CRT implosion shield before powering up the instrument.

4. Unsnap the four boards from their mounting posts.

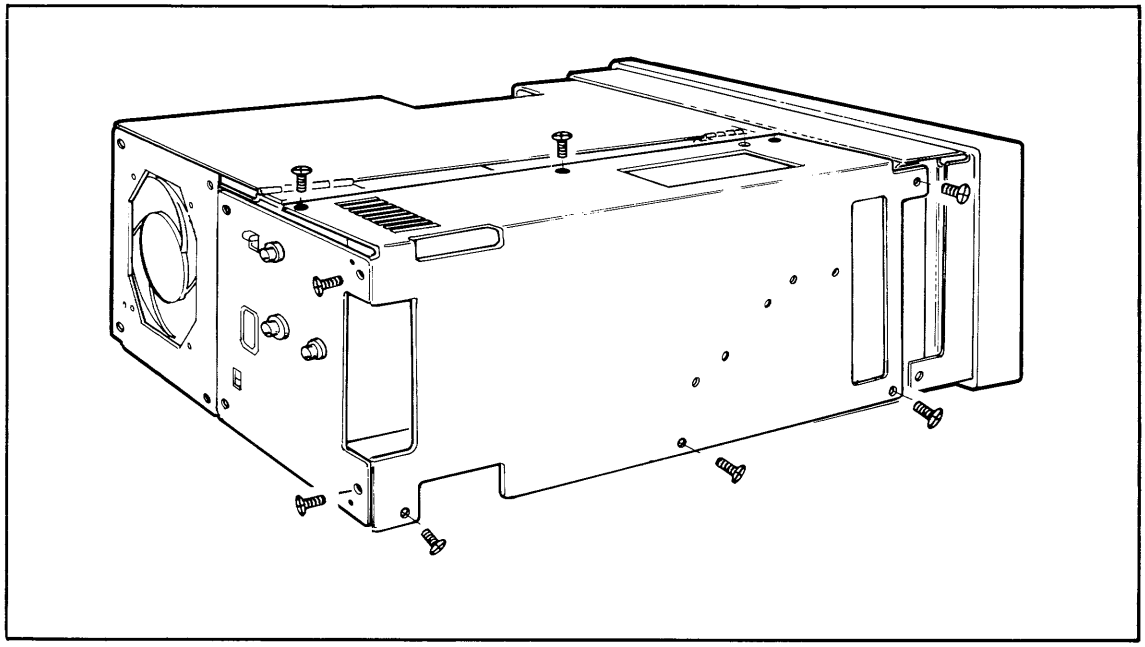
PROCEDURE #8: CRT DRIVE BOARD REMOVAL

DISASSEMBLY

1. Perform Procedures #1 and #2.
2. Remove the ten #4 flat-head screws holding the CRT Drive Board bracket and the Rear Panel to the mainframe. Refer to Figure 6-3.
3. If necessary, unplug the cabling from the CRT, the rear panel, and the Interface Board to the CRT Drive Board for removal of the bracket from the mainframe.
4. If necessary, remove the eight #4 pan-head screws holding the CRT Drive Board to the CRT Drive Board bracket.

CAUTION

Always re-install the CRT Drive Board bracket as soon as possible to remove exposed voltages from the work environment.



4342-46

Figure 6-3. Location of screws for CRT Drive Board bracket removal.

INSTALLATION HINTS

- If the wires to the CRT Drive Board were disconnected, reconnect as follows:
  1. Four 9-2 (White/Red) wires to J414
  2. Seven multi-colored wires to J230
  3. Flat laminated cable to J121
  4. Four wire cable from rear panel to J581
  5. 9-1 (White/Brown) wire from VIDEO OUT BNC to J582
  6. 9-2 (White/Red) wire from EXT TRIG IN to J584
  7. 9-3 (White/Orange) wire from EXT TRIG OUT to J583

PROCEDURE #9: CRT REMOVAL

DISASSEMBLY

WARNING

CRTs RETAIN HAZARDOUS VOLTAGES FOR LONG PERIODS OF TIME AFTER POWER-DOWN. The CRT should be serviced only by qualified personnel familiar with CRT servicing procedures and precautions.

USE EXTREME CAUTION WHEN HANDLING THE CRT. Do not nick or scratch the glass or subject it to undue pressures during removal or installation. Rough handling may cause it to violently implode. When handling the CRT, wear safety goggles and heavy gloves for protection.

1. Perform Procedure #8, then #5.

WARNING

*BEFORE ATTEMPTING ANY WORK ON THE CRT, discharge the CRT by **simultaneously** shorting the anode connection to chassis ground using a plastic-handle screwdriver. When discharging, place the screwdriver against the chassis, then slip the screwdriver tip under the CRT anode cup.*

2. Discharge the CRT by simultaneously touching the chassis ground with the plastic-handle screwdriver shank and slipping the screwdriver tip under the CRT anode cup. Refer to Figure 6-4.
3. Unplug the LED/PT Board cable, the anode, and CRT end cap.
4. Remove four #6 screws holding the CRT retainer.
5. Remove the CRT out the front side of the instrument.

INSTALLATION HINTS

- If previously removed, re-install the DAG spring across the back side of the CRT to ensure proper grounding.

WARNING

The CRT anode forms a capacitor with the external CRT DAG coating. If the DAG spring is not present to ground the CRT, hazardous voltages may exist on the outside of the CRT. Always replace the CRT implosion shield before powering up the instrument.

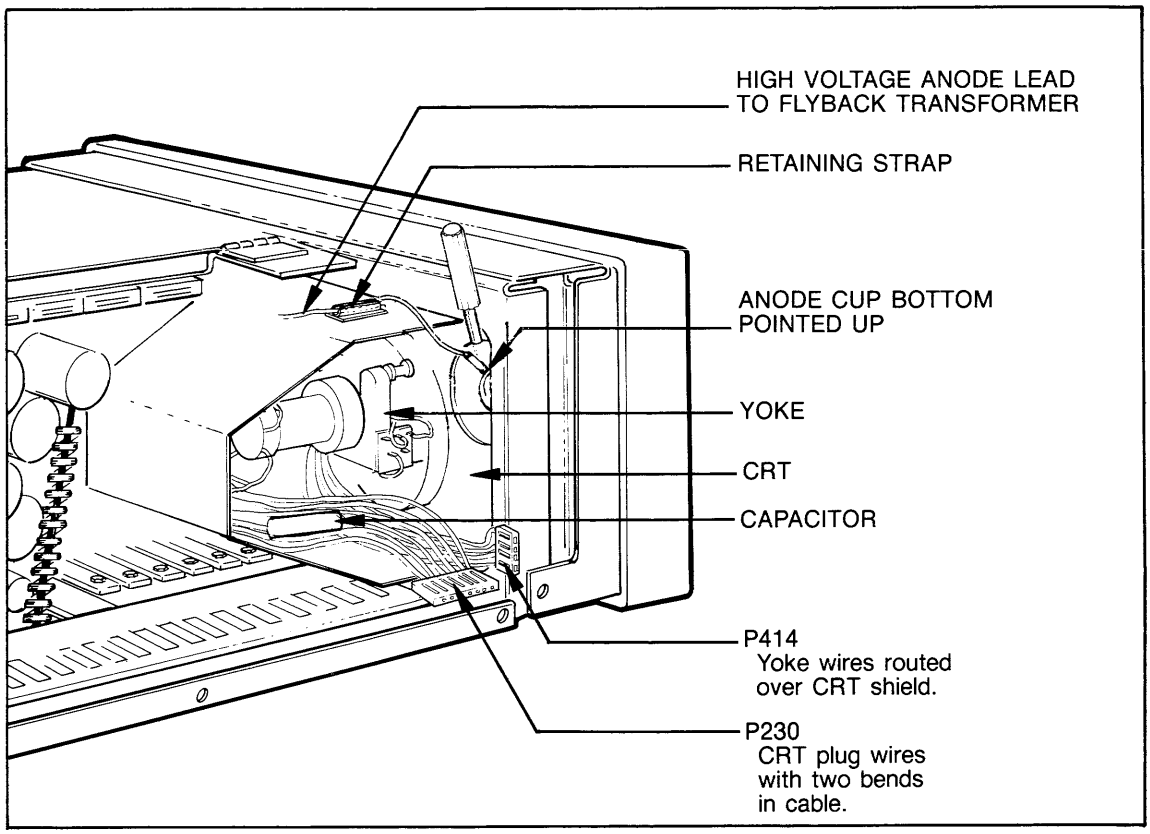


Figure 6-4. Discharging a CRT using a flat-blade screwdriver.

- Roll the CRT anode cup back then install one prong into the CRT at a time. Ensure that both prongs are secured in the CRT anode cavity. Straighten the anode lead towards the top of the instrument. Refer to Figure 6-4.
- When installing the CRT end cap, ensure proper pin to connector alignment before installing the end cap. CRT pins are fragile; avoid unnecessary bending to guard against CRT tube cracking. Route the CRT end cap cabling as shown in Figure 6-4.
- If previously removed, re-connect the wires to the CRT Drive Board as follows:

  1. Four 9-2 (White/Red) wires to J414
  2. Seven multi-colored wires to J230
  3. Flat laminated cable to J121
  4. Four wire cable from rear panel to J581
  5. 9-1 (White/Brown) wire from VIDEO OUT BNC to J582
  6. 9-2 (White/Red) wire from EXT TRIG IN to J584
  7. 9-3 (White/Orange) wire from EXT TRIG OUT to J583

PROCEDURE #10: POWER SUPPLY BOARD

DISASSEMBLY

CAUTION

Dangerous electric-shock hazards inside the mainframe may be exposed when the covers are removed. Be sure both front and rear panel power switches are off and the power cord is disconnected before removing the covers. Disassembly procedures should only be attempted by qualified service personnel.

WARNING

A lighted or blinking neon lamp on the power supply board, visible through a hole on the power supply cover adjacent to the warning label, indicates that a lethal voltage is present on that board. Wait for at least 15 minutes after power-down before accessing the power supply or related assemblies.

1. Perform Procedures #1, #3, and #8.
2. Disconnect the ground wire from the chassis by removing the screw.
3. Remove the nine screws holding the Power Supply Board. Remove cables P100, P110, P120, P130, P145, and P161 (P181 for instruments with serial numbers B080000 and above) from the board. (Refer to Figure 6-5.)

CAUTION

When removing or installing the Power Supply Board, be careful not to bend the CRT shield. Bending causes the shield's metallic properties to change.

INSTALLATION HINTS

- Note the cable dressing to the Interface Board. When re-connecting the power supply cables, dress the cables so there is slack in the area where they enter the card cage.

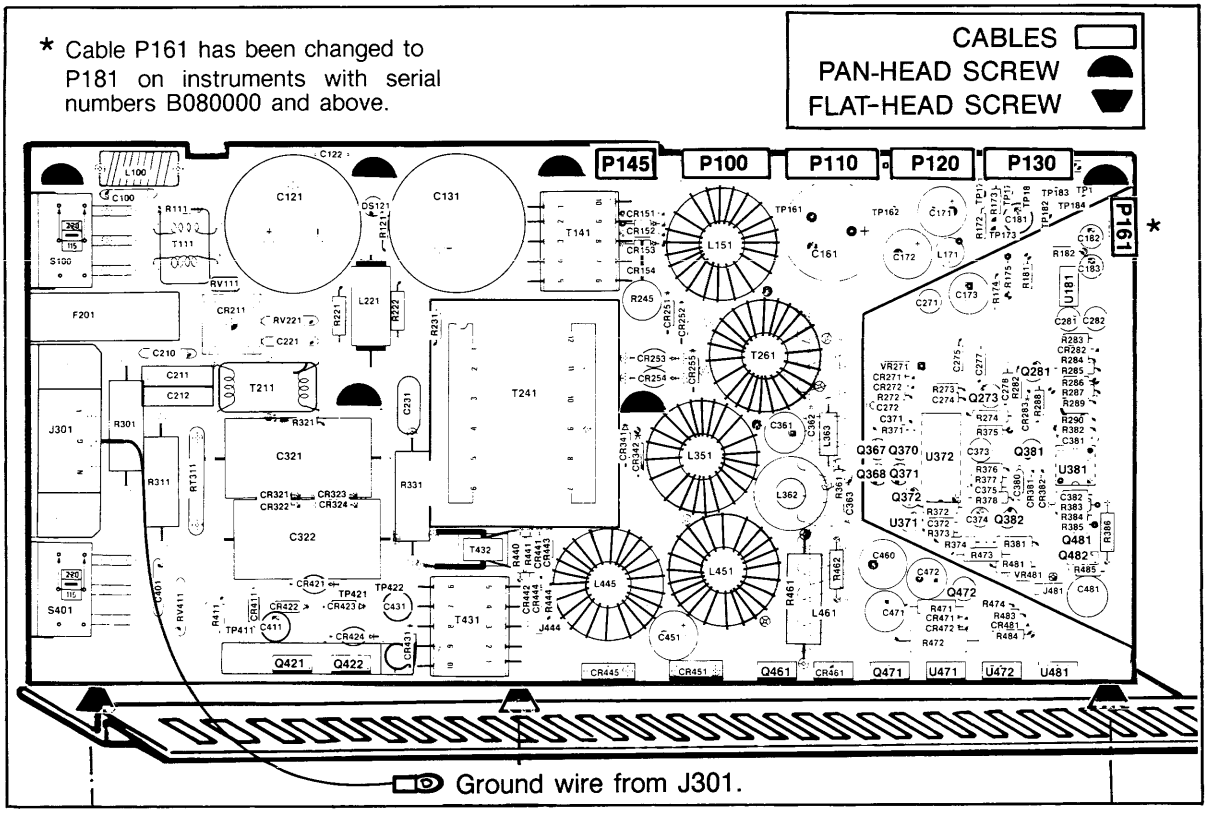


Figure 6-5. Location of screws and cables for Power Supply Board removal.

PROCEDURE #11: INTERFACE BOARD

DISASSEMBLY

1. Perform Procedure #3, then #4.
2. Unsnap the outer layer of the cable shield from the Interface Board (outside of the card cage).
3. Unplug the two flat cable connectors from the Interface Board and remove the cable shield.
4. Remove the four #4 screws holding the plastic shield (located inside the card cage).
5. Remove the six #4 screws holding the Interface Board to the card cage.
6. Remove the four power supply cables P100, P110, P120, and P130 from the Interface Board.
7. Lift the Interface Board out of the card cage.

INSTALLATION HINTS

- Note the cable dressing to the Interface Board. When re-connecting the power supply cables, dress the cables so there is slack in the area where they enter the card cage.

CAUTION

1240 cards operate only in specific card-cage slots. If you apply power to a card installed in the wrong slot, the card will be damaged. To prevent damage, follow the card-slot assignments shown in Figure 6-2. (There is an exception for the Control and I/O Processor Boards; refer to Soft Key Sensitivity Adjust *in Section 5 for details.)*

- Install the boards in a top-down fashion according to the following list:

Control Processor Board
I/O Processor Board
Display Board
Acquisition Board (slot 3*)
Acquisition Board (slot 2*)
Acquisition Board (slot 1*)
Acquisition Board (slot 0*)
Trigger Board

- For * acquisition slots, install acquisition cards in every slot starting from the trigger card. (The trigger card is on the bottom when the card cage is in its rolled out position.) All unused slots should be next to the Display Board. Refer to Figure 6-2 for a map of the card-cage slots (in the service position).

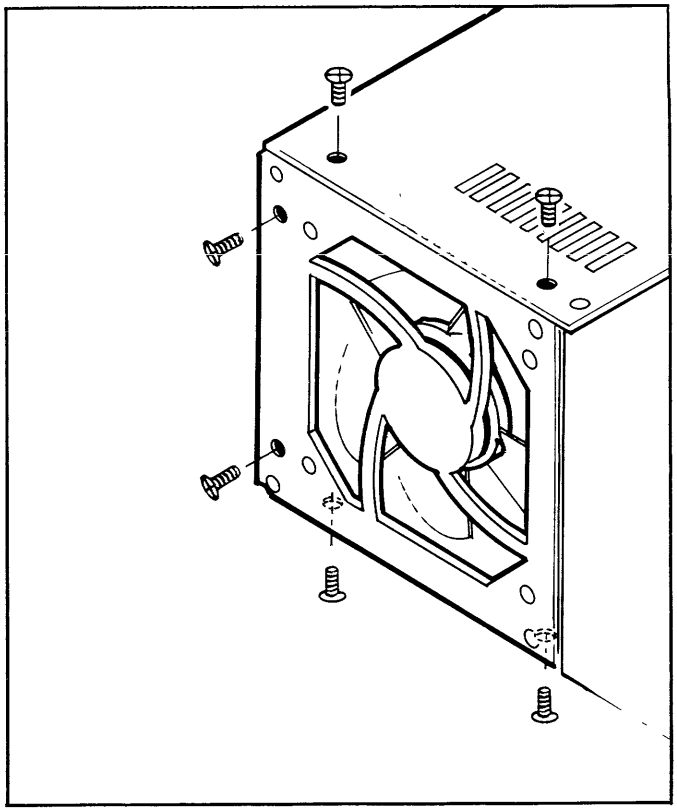
NOTE

If your instrument contains 18-channel cards, it will be necessary to remove them before installing new 9-channel cards in order to follow these installation rules correctly.

PROCEDURE #12: FAN REMOVAL

DISASSEMBLY

1. Perform Procedures #1, and #3.
2. Disconnect the fan cable from the power supply at P145.
3. Remove the six #4 flathead screws shown in Figure 6-6.
4. Remove the fan bracket and remove the four #4 flathead screws holding it to the bracket.



4342-49

Figure 6-6. Location of screws for fan removal.

SECTION 7 MAINTENANCE

SECTION 7 MAINTENANCE

MAINTENANCE

Tektronix maintains repair and recalibration facilities at its local Field Service Centers and the Factory Service Center. For further information or assistance, contact your local Tektronix Field Office or representative.

TOOLS REQUIRED FOR MAINTENANCE

The following tools are those most often needed when servicing the 1240 Logic Analyzer.

- soldering iron, (15 W)
- rosin core solder, 60/40
- isopropyl alcohol
- lint-free dust cloth
- soft-bristle brush
- IC extractor
- desolder tool
- solder wick
- slotted screwdriver
- magnetic screwdriver (1/4 inch drive)
- POZIDRIV-type bit #1
- POZIDRIV-type bit #2
- Phillips-type bit #0
- TORX-type magnetic bit, size T-20 (Tek P/N 003-0866-00)
- angled tweezers, 6 inch
- long-nose pliers
- 1/4, 5/16, 1/2, and 9/16 inch combination wrenches
- Allen wrench, 1/16 inch

MAINTENANCE PRECAUTIONS

WARNING

Dangerous electric-shock hazards outside and inside the mainframe may be exposed when the cabinet is removed. Be sure both front and rear panel power switches are off and the power cord is disconnected before removing the cabinet. Disassembly procedures should only be attempted by qualified service personnel.

A lighted or blinking neon lamp on the power supply board, visible through a hole on the power supply cover adjacent to the warning label, indicates that a lethal voltage is present on that board. Wait for at least 15 minutes after powering down before accessing the power supply or related assemblies.

SOLDERING

Most of the components in the instrument are soldered in place. If it is necessary to replace a soldered part, use a 15 W soldering iron to prevent heat damage to the circuit board or components. Excessive heat will lift circuit runs on the circuit board.

The flux in solder may leave a residue on the circuit board that can provide a high-resistance leakage path and affect instrument operation. Be sure to clean off this residue. Isopropyl alcohol is recommended.

LIGHT-EMITTING DIODES (LEDs)

To avoid damage to the LEDs, always keep soldering time and temperature to a minimum. Do not bend the leads or apply force when inserting them into circuit board holes. Clean the circuit board holes of all excess solder before attempting to install a new LED.

NOTE

Damage to the LEDs may not be immediately apparent. Always follow the precautionary measures previously listed when handling the LEDs.

STATIC PRECAUTIONS

CAUTION

Static discharge can damage any semiconductor in this instrument.

Observe the following precautions to avoid damage:

- Minimize handling of static-sensitive components.
- Transport and store static-sensitive components or assemblies in their original containers, on a metal rail, or on conductive foam. Label any package that contains static-sensitive components or assemblies.

- Discharge the static voltage from your body by wearing a wrist strap while handling these components. Servicing static-sensitive assemblies should be performed only in a static-free work station by qualified service personnel.
- Nothing capable of generating or holding a static charge should be allowed on the work station surface.
- Keep the component leads shorted together whenever possible.
- Pick up components by the body, never by the leads.
- Do not slide the components over any surface.
- Avoid handling components in areas that have a floor or work-surface covering capable of generating a static charge.
- Use a soldering iron that is connected to earth ground.
- Use only special anti-static suction type or wick type desoldering tools.

NOTE

Damage to electrical components may not be immediately apparent. Always follow the precautionary measures previously listed when handling static-sensitive components.

PREVENTIVE MAINTENANCE

Preventive maintenance consists of periodic cleaning and inspection. Accumulation of dust on electrical components acts as an insulating blanket and prevents efficient heat dissipation. This condition can cause overheating and component breakdown within the instrument. Dust accumulated on parts around the display screen can render the on-screen soft keys inoperative; refer to *Soft Key LED Cleaning* later in this section. Periodic cleaning and inspection will reduce instrument breakdown and increase instrument reliability.

This instrument should be cleaned as often as the operating environment requires. A convenient and appropriate time to perform these procedures is immediately prior to instrument adjustment.

EXTERIOR CLEANING

Dust the exterior surfaces with a dry, lint-free cloth or a soft-bristle brush. If hard dirt remains, use a cloth or swab dampened with 5% mild detergent and warm water solution. The swab is also useful for cleaning in narrow spaces around the controls. Use the detergent solution for cleaning the screen also. Do not use abrasive compounds on any part of the instrument.

CAUTION

To prevent getting water inside the instrument during external cleaning, use only enough water to dampen the cloth or swab.

DO NOT use chemical cleaning agents as they may damage the plastics used in the instrument. In particular, avoid chemicals that contain benzene, toluene, xylene, acetone, or similar solvents.

INTERIOR CLEANING

To gain access to internal portions of the instrument, refer to the instructions in the *Disassembly and Installation Procedures* section of this manual.

Internal cleaning should be done with a dry, low-velocity stream of air. A soft-bristle brush is useful for cleaning around components. If a liquid must be used for minor internal cleaning, use isopropyl alcohol, denatured ethyl alcohol, or a solution of 1% mild detergent and 99% de-ionized water.

Should the interior of the instrument require a thorough cleaning, wash according to the following cautionary *Cleaning Guidelines.*

CLEANING GUIDELINES

CAUTION

DO NOT wash the front or rear panel power switches. The power switches must be covered during washing procedures.

Spray-wash dirty parts with a cleaning solution listed under Interior Cleaning, *then use de-ionized water to THOROUGHLY RINSE all parts. IMMEDIATELY DRY all parts with low air pressure.*

When washing near unsealed electromechanical components, use as little washing action as possible. This prevents washing the lubricant out of the components and getting an excess of detergent into the contact areas of the switches. DETERGENT RESIDUE WILL CAUSE CORROSION, which may degrade instrument performance.

DO NOT immerse the front panel rotary encoder for cleaning purposes. Because the shaft is lubricated, clean it by only wiping it externally with a damp cloth.

DO NOT use a freon-based cleaner for cleaning the circuit boards. Freon will damage aluminum capacitors.

DO NOT use fluorocarbon-based spray cleaners or silicon spray lubricants on switches or switch contacts. These sprays may damage the circuit board material or plastic parts, and leave a dust-collecting residue. If necessary, Tektronix, Contact Lubricant and Cleaner (006-0442-00)® *may be used as a lubricant.*

To prevent damage from electrical arcing, ensure that all circuit boards, switches, and board interface connectors are completely dry. Do this by heating the board or switch in an oven at 75 degrees Celsius (167 degrees Fahrenheit) for 15 minutes before applying power.

INSPECTION

Inspect the instrument for broken connections, frayed wires, poorly seated components, leaking capacitors, damaged hardware, and heat-damaged components.

Repair any obvious problems. However, take particular care if you find any heat-damaged parts. Overheating usually indicates other circuit problems. To prevent recurrence of the damage, find and correct the cause of the overheating. Note that replacement of instrument electrical components may necessitate readjustment of the affected circuitry. Refer to the *Replaceable Electrical Parts* section for a list of part and component descriptions.

SOFT KEY LED CLEANING

The 1240 soft keys are displayed along the top and bottom of the screen. Sensing of keystrokes on these keys is done using a combination of LEDs and phototransistors attached to a frame surrounding the screen. Dust may accumulate on the LEDs, phototransistors, or other parts, resulting in diagnostic failures. To avoid these diagnostic failures, perform the soft key LED cleaning procedure. Depending on the environment, it may be necessary to clean the interior of the 1240/1241 periodically. Under very dusty conditions, cleaning every six months or less may be required.

The steps listed in the following are LED cleaning procedures for the 1240 Logic Analyzer; for 1241 LED cleaning procedures, refer to the *1241 Service Manual Addendum.*

1. Section 6 of this manual contains disassembly procedures; read *Overview* and *General Disassembly/Installation Precautions* in that section before attempting any disassembly.
2. Also in Section 6, follow disassembly procedure #7 to remove the 1240 LED/Phototransistor Boards from the front of the instrument; it is not necessary to remove the boards from their mounting posts.
3. Clean all surfaces of the mounting frame, the circuit boards, and the components on those boards by following the instructions provided under *Interior Cleaning* in this section.

NOTE

It is recommended that you also clean all of the surfaces surrounding the LED/Phototransistor Boards to prevent the rapid re-accumulation of dust on the soft key components.

4. Reassemble the 1240 by reversing the steps for disassembly.
5. Power ON the 1240 and verify that the disgnostics pass. If the soft key test fails, perform procedure *1B. CRT: Soft Key Sensitivity Adjust* in Section 5 of this manual. If the soft key diagnostics continue to fail (or other diagnostic tests fail), refer to the troubleshooting information in Section 8 of this manual or contact your local Tektronix Service Center.

CORRECTIVE MAINTENANCE

OBTAINING REPLACEMENTS

Electrical And Mechanical Parts

All electrical and mechanical parts for the instrument can be obtained through your Tektronix Field Office or representative. However, many of the standard electrical components can be obtained locally. Before purchasing an ordinary part, check the *Replaceable Electrical Parts* section for a listing of value, tolerance, rating, and description.

CAUTION

Check the parts list before replacing electrical components. If the part is called out as screened or burned-in, the replacement part must also be screened or burned-in or the repair may not be effective.

NOTE

When selecting replacement parts, remember that the size and shape of the component may affect its performance in the instrument. All replaceable parts should be direct replacements unless it is known that a different part will not adversely affect instrument performance.

Some of the mechanical parts and electrical parts in this instrument are manufactured by Tektronix. Some parts are manufactured or selected by Tektronix, to satisfy particular requirements, or are manufactured to certain specifications for Tektronix. To determine the manufacturer of a part, refer to the *Parts List Cross Index of Code Number to Manufacturer.* This is found in the *Replaceable Electrical Parts* section.

When ordering replacement parts from Tektronix, include the following information:

1. instrument type
2. instrument serial number
3. a description of the part (if electrical, include the component number)
4. Tektronix part number

Acquisition Boards And Probes

If it becomes necessary to send in an acquisition board for repair, also send the associated acquisition probe. Along with the board and the probe, write a brief description of the problem and the circumstance in which it was discovered.

Replaceable As Assemblies

The following 1240 instrument pieces are replaceable as assemblies:

1. LED/Phototransistor Boards A01 - A04
2. CRT Drive Board wire sub-assembly
3. some parts of the P6460 Data Acquisition Probe (A70)
4. any multi-conductor cables

REPAIRING MULTI-CONDUCTOR CONNECTORS

Some of the interconnecting cable assemblies in the instrument consist of multi-conductor cable with machine-installed terminal connectors, mounted in plastic holders (refer to Figure 7-1). The plastic holders can be replaced easily. However, if the cable is defective it must be replaced as a complete cable assembly. If one of the terminal connectors comes loose from the plastic holder, it can be re-installed as shown in Figure 7-1. When re-installing the connectors onto the circuit-board pins, be sure to match the triangle on the connector to the board.

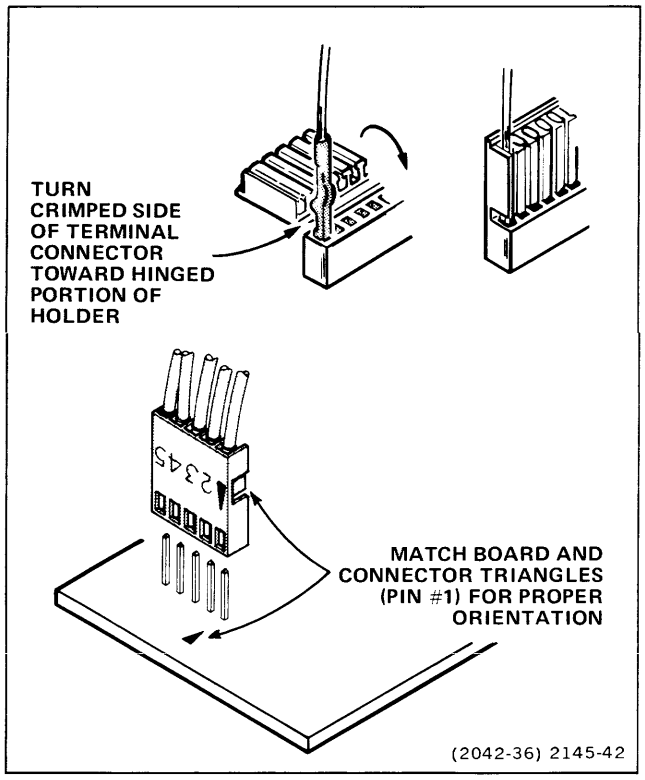


Figure 7-1. Multi-conductor terminal connectors.

CIRCUIT BOARD PIN REPLACEMENT

A circuit-board pin replacement kit, including necessary tools, instuctions, and replacement pins with attached spare ferrules, is available from Tektronix. Refer to Figure 7-2.

CAUTION

Replace circuit board pins on multi-layer boards with extreme care. These boards have conductive paths laminated between the top and bottom board layers. All soldering, removal, and re-insertion of pins must be done with care to prevent breaking any electrical paths on the board.

1. Use a 15 W soldering iron to unsolder the pin while pulling it out of the board with a pair of pliers. If the pin is too short to use pliers, it can be pushed out with any round device not over 0.028 inches in diameter.

2. If the ferrule remained in the board, carefully ream the solder out with a 0.031 inch drill. If the ferrule came out with the pin, clean the excess solder out of the hole with a solder-removing wick and a scribe.
3. If the ferrule remained in the board, remove the ferrule from the new pin and insert the pin into the old ferrule in the same orientation as the old pin. If the ferrule came out with the old pin, insert the new pin with ferrule in the same orientation as the old pin.
4. When the new pin is properly positioned, carefully solder it on both sides of the board.
5. Clean remaining residue from the board according to the *Interior Cleaning* instructions.

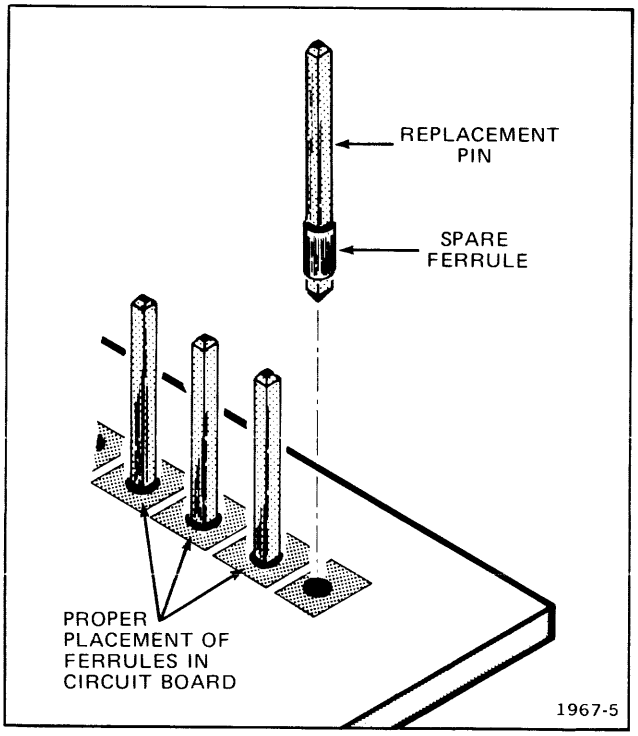


Figure 7-2. Circuit board pin replacement.

BATTERY REPLACEMENT ON THE CONTROL PROCESSOR AND RAM PACK

If the backup-battery voltage goes below approximately 2.2 volts, data stored in RAM may be lost. To determine the condition of the battery, measure the battery voltage across the appropriate capacitor:

- Control Processor: A09C145
- 8K RAM Pack: A41C128

When it becomes necessary to replace the backup battery on the Control Processor or RAM pack, use the following procedure:

1. Connect an external +5 volt supply across the capacitor that was used to measure the battery voltage. This puts +5 volts on the vcc pin of the RAM.

CAUTION

Before connecting the external supply, observe the polarity of the supply and the capacitor to ensure proper connection. Connect the minus (-) lead of the supply to the grounded side of the capacitor.

2. Remove the battery using a 15 W soldering iron that has been connected to an isolation transformer. A desoldering tool should be used to clean the holes in preparation for the new battery.

CAUTION

A floating (ungrounded) soldering iron must be used to ensure the battery is not grounded during removal and installation procedures.

3. Place the new battery in position and solder it in place using standard soldering procedures.
4. Disconnect the external +5 volt power supply.
5. Install the Control Processor Board or RAM Pack and check for proper operation by using diagnostic tests.

WARNING

To avoid personal injury, observe proper procedures for handling and disposal of lithium batteries. Improper handling may cause fire, explosion, or severe burns. Don't recharge, crush, disassemble, heat the battery above 212° F (100° C), incinerate, or expose contents of the battery to water. Dispose of battery in accordance with local, state, and national regulations.

Typically, small quantities (less than 20) can be safely disposed of with ordinary garbage in a sanitary landfill.

Larger quantities must be sent by surface transport to a Hazardous Waste Disposal Facility. The batteries should be individually packaged to prevent shorting and packed in a sturdy container that is clearly labeled "Lithium Batteries--DO NOT OPEN."

POWER SUPPLY JUMPER CHANGE

The power supply jumper A07J444 provides a method for changing the amount of available output current for the instrument. The jumper should be positioned in the low-load setup (pin 2 shorted to pin 3) when two acquisition cards, either 9-channel or 18-channel, are installed. If more than two 9- or 18-channel cards are installed, the jumper should be positioned in the high-load setup (pin 1 shorted to pin 2).

SECTION 8 TROUBLESHOOTING AND REPAIR

SECTION 8 TROUBLESHOOTING AND REPAIR

TABLE OF CONTENTS (cont.)

TABLE OF CONTENTS (cont.)

TROUBLESHOOTING AND REPAIR

OVERVIEW

This section contains procedures a technician should use to troubleshoot and repair a faulty 1240 Logic Analyzer. Depending upon the conditions of the failure, various troubleshooting strategies may be used to locate the specific problem. Table 8-1 lists categories of fault conditions and related troubleshooting information sources that should be used to repair the faults.

Table 8-1
RECOMMENDED SERVICING APPROACH

Fault Condition	Servicing Approach
1. No power-up	1. Refer to: • Power Supply Troubleshooting • Damage Resulting From Incorrect Board Installation
2. Power-up failure (display may not be useable)	2. Refer to: • Processor LEDs • CRT Drive Board Troubleshooting • Soft Key Troubleshooting • Kernel Signature Analysis • Theory of Operation
3. Power-up failure (with error indexes)	3. Refer to: • Diagnostic Error Indexes • Extended Diagnostics (with diagnostic ROM pack) • Diagnostic Block Diagrams
4. General failure (problems not detected during power-up diagnostics)	4. Refer to: • Extended Diagnostics (with diagnostic ROM pack) • Theory of Operation • Troubleshooting Intermittent Failures • 1240 Manual Tests

TROUBLESHOOTING EQUIPMENT

The following equipment, or equivalent, is recommended for troubleshooting the 1240 Logic Analyzer.

- SONY/TEK 308 Data Analyzer
- 1240 Service Maintenance Kit
- TEKTRONIX 485 Oscilloscope with two P6106 probes

USING THE 1240 EXTENDER BOARDS

The 1240 Service Maintenance Kit contains two extender boards that are used in the troubleshooting, adjustment, and verification procedures. The first board, assembly A21, should be used when working with the trigger, display, and both processor boards. The second board, assembly A22, should be used with the 9- and 18-channel acquisition boards. Both extenders allow a board under test to be at a convenient position away from the other boards so the signal test points and components are accessible.

NOTE

In some instances, either extender board will degrade system performance. For complete details, refer to Table 2-4 Extender Limitations in the Specifications *section of this manual and the instruction sheet that accompanies each extender board.*

REPLACING DEFECTIVE PARTS

If it becomes necessary to replace defective parts found during troubleshooting procedures, refer to the *Maintenance* section of this manual for cautionary guidelines and recommended practices. In addition, note that replacement of instrument electrical components may necessitate readjustment of the affected circuitry. Refer to the *Verification and Adjustment Procedures* section for readjustment procedures.

LIST OF ASSEMBLIES

A list of assemblies and subassemblies can be found at the beginning of the *Replaceable Electrical Parts* section. The assemblies are listed in numerical order. A complete component number is useful for identifying the assembly where the part resides, as well as the circuit number being referenced.

TROUBLESHOOTING PRECAUTIONS

To gain access to the interior of the instrument, use the directions provided in the *Disassembly and Installation Procedures* section.

WARNING

Electric shock hazards inside the instrument may be exposed when certain covers are removed. Servicing should be performed only by qualified service personnel.

DISCHARGING THE CRT

The following precautions should be observed when working on the CRT:

WARNING

CRTs RETAIN HAZARDOUS VOLTAGES FOR LONG PERIODS OF TIME AFTER POWER-DOWN. The CRT should be serviced only by qualified personnel familiar with CRT servicing procedures and precautions.

ENSURE that both front and rear panel power switches are in the OFF position before attempting servicing procedures.

USE EXTREME CAUTION WHEN HANDLING THE CRT. Rough handling may cause it to violently implode. Do not nick or scratch the glass or subject it to undue pressures during removal or installation. When handling the CRT, wear safety goggles and heavy gloves for protection.

BEFORE ATTEMPTING ANY WORK ON THE CRT, discharge the CRT by shorting the anode connection to chassis ground using a plastic-handle screwdriver. When discharging, place the screwdriver against the chassis, then slip the screwdriver tip under the CRT anode cup.

STATIC DISCHARGE DAMAGE (Special Handling Required)

CAUTION

All semiconductor devices in the instrument are susceptible to damage by static discharge.

Most of the devices used in the 1240 are static-sensitive and may be damaged by improper handling. See Table 8-2 for the relative susceptibility of various classes of semiconductors. Static voltages of 1 to 30 kV are common in unprotected environments.

Table 8-2
STATIC DAMAGE TABLE

Semiconductor Class	Danger Voltage*
MOS or CMOS	100 - 500 V
ECL	200 - 500 V
Schottky signal diodes	250 V
Schottky TTL	500 V
High-frequency bipolar transistors	400 - 600 V
JFETs	600 - 800 V
Linear microcircuits	400 - 1000 V
Low-power Schottky TTL	1200 V

*voltage discharged from a 100 pF capacitor through 100 ohms resistance

OPERATING THE 1240 WITH THE CABINET REMOVED

CAUTION

DO NOT operate the instrument with the cabinet removed for extended periods of time unless it is raised off the working surface at least one-half inch.

If it is necessary to run the 1240 for extended periods of time, raising the instrument admits air to the power supply for cooling purposes. Additionally, another fan should be positioned to blow air onto the instrument bulkhead just below the card cage (when the card cage is rolled into the service position). This additional air supply should particularly be aimed at the power supply heat sink, located on the bottom of the bulkhead.

When operating the 1240 in the service position, the rear panel fan does not provide adequate cooling for some boards installed on the Extender board. To avoid this problem, a fan should be positioned to blow air across these extended boards. The boards that require additional cooling are:

- any 9-Channel Acquisition Boards
- any 18-Channel Acquisition Boards
- the Trigger Board

1240 TROUBLESHOOTING WITHOUT ERROR INDEXES

If the 1240 fails and some part of either the I/O Processor or the Control Processor is non-functional, the 1240 may not be able to produce on-screen error messages. If this occurs, the service technician has available alternative courses for troubleshooting the failure. Table 8-1, Recommended Servicing Approach, outlines the troubleshooting procedures available.

DAMAGE RESULTING FROM INCORRECT BOARD INSTALLATION

The following table lists the components that could be damaged when a 1240 board is installed in an incorrect card-cage slot. In some cases, components may not display failure symptoms until sometime later.

NOTE

If only one board was placed in the wrong slot, you need only find component information for that board/slot combination. However, if two boards were incorrectly installed (i.e., two boards placed in each others slots), you must find component information for both board/slot combinations.

Table 8-3
POSSIBLE COMPONENTS DAMAGED WHEN A BOARD IS INSTALLED INCORRECTLY

Board \ Slot	Control or I/O Processor Slot	Display Slot	Acquisition Slots	Trigger Slot
Control Processor Board	correct slot	A09U261, U264 A14U150	A09U261 A14U150, U635 A14U640	A09U261, U264 A14U150
I/O Processor Board	correct slot	no problems	A14U635 A14U640	no problems
Display Board	A09U264 A14U150	correct slot	A10U295, U385 A11U405, U495 A15U390, CR678 A16U261, CR259	no problems
18-Channel Board	no problems	won't fit	correct slot	won't fit
9-Channel Board	may disable power switch; use rear panel power switch	won't fit	correct slot	won't fit
Trigger Board	instrument may not power up	won't fit	A10U295, U385 A11U405, U495 A15U390, CR678 *A15U565 A16U261, CR259 *A16U538	correct slot

*only the acquisition board immediately below the Trigger Board

670-7534-06 POWER SUPPLY TROUBLESHOOTING TREE

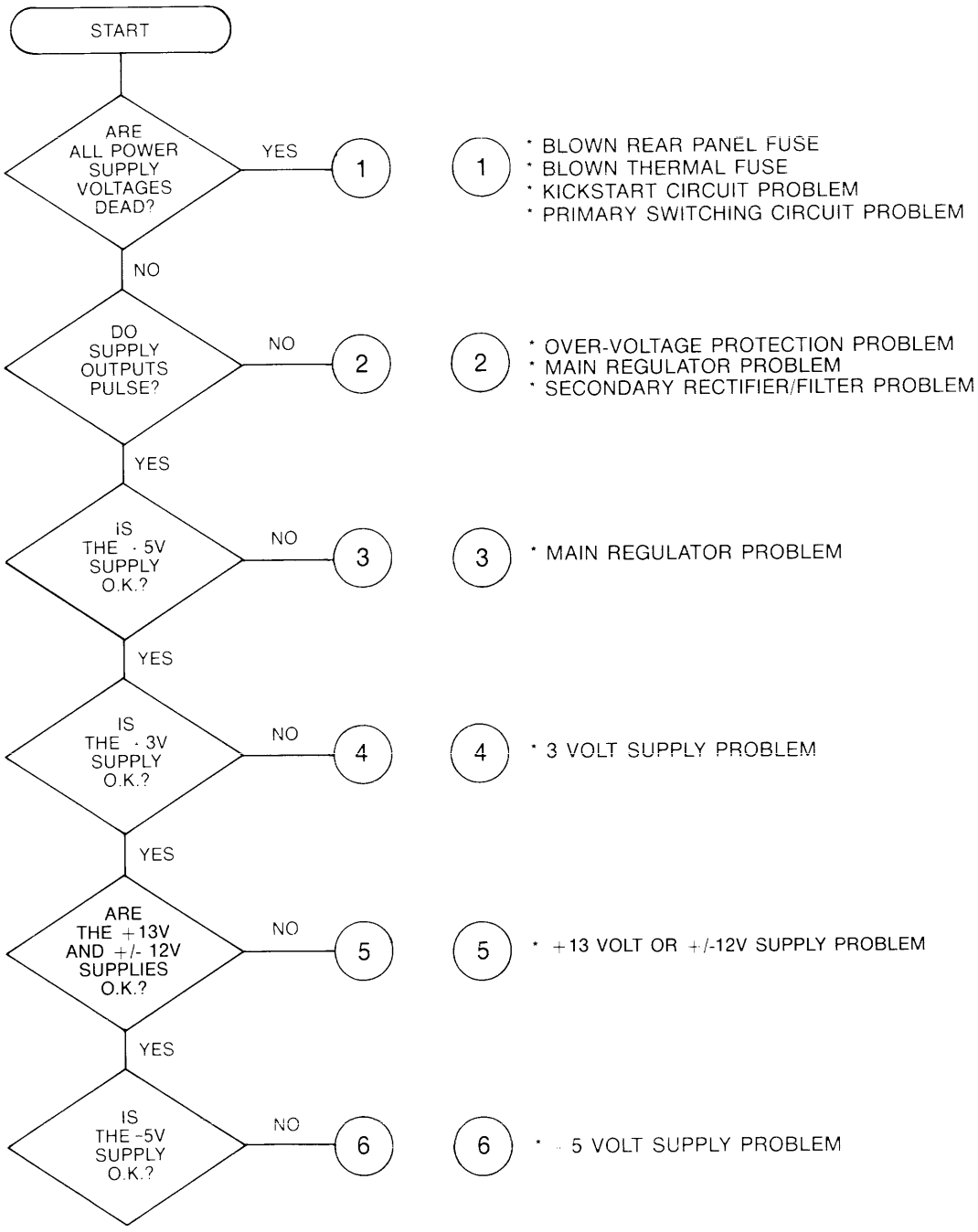


Figure 8-1A. 670-7534-06 power supply troubleshooting tree.

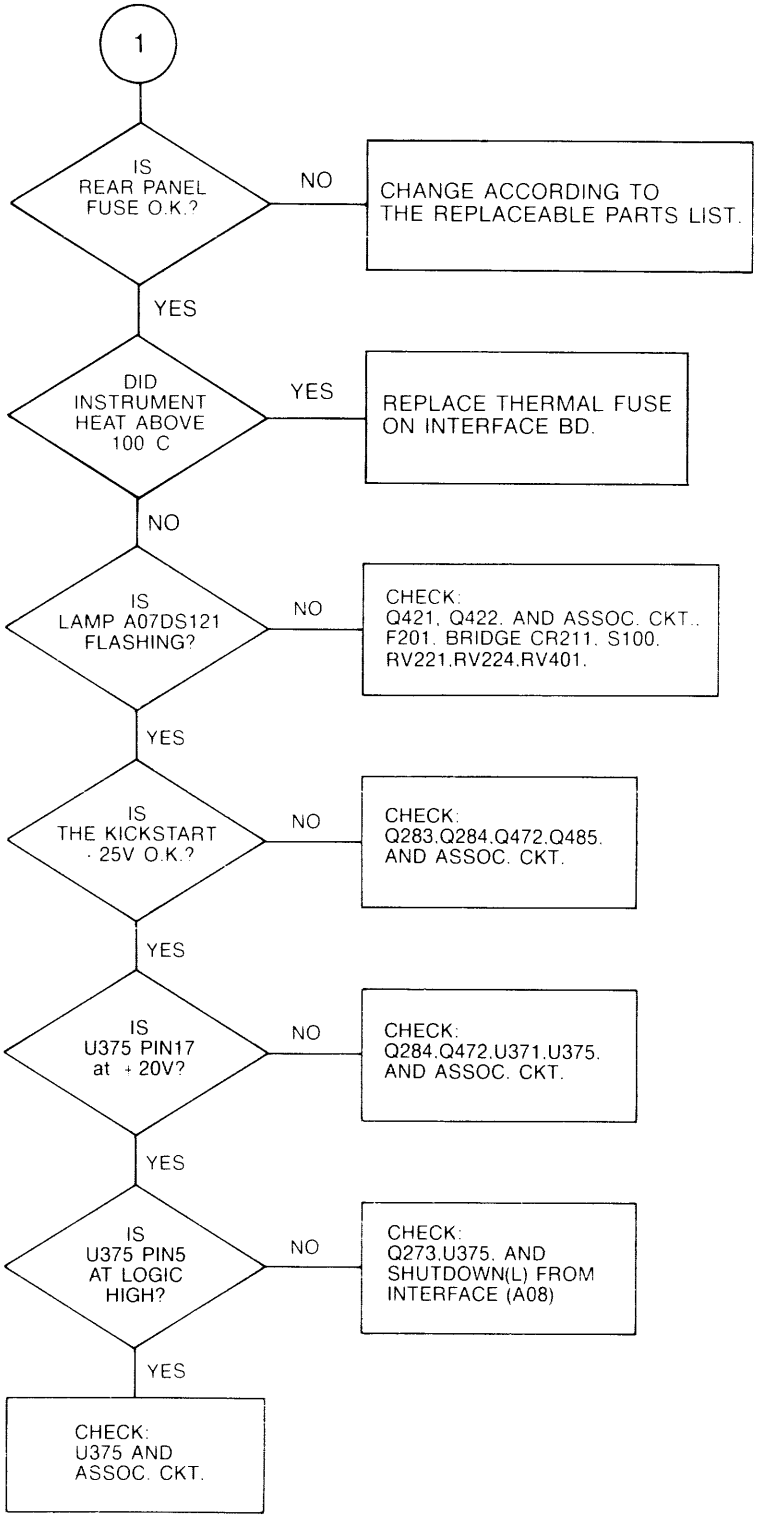


Figure 8-1A. 670-7534-06 power supply troubleshooting tree (cont.).

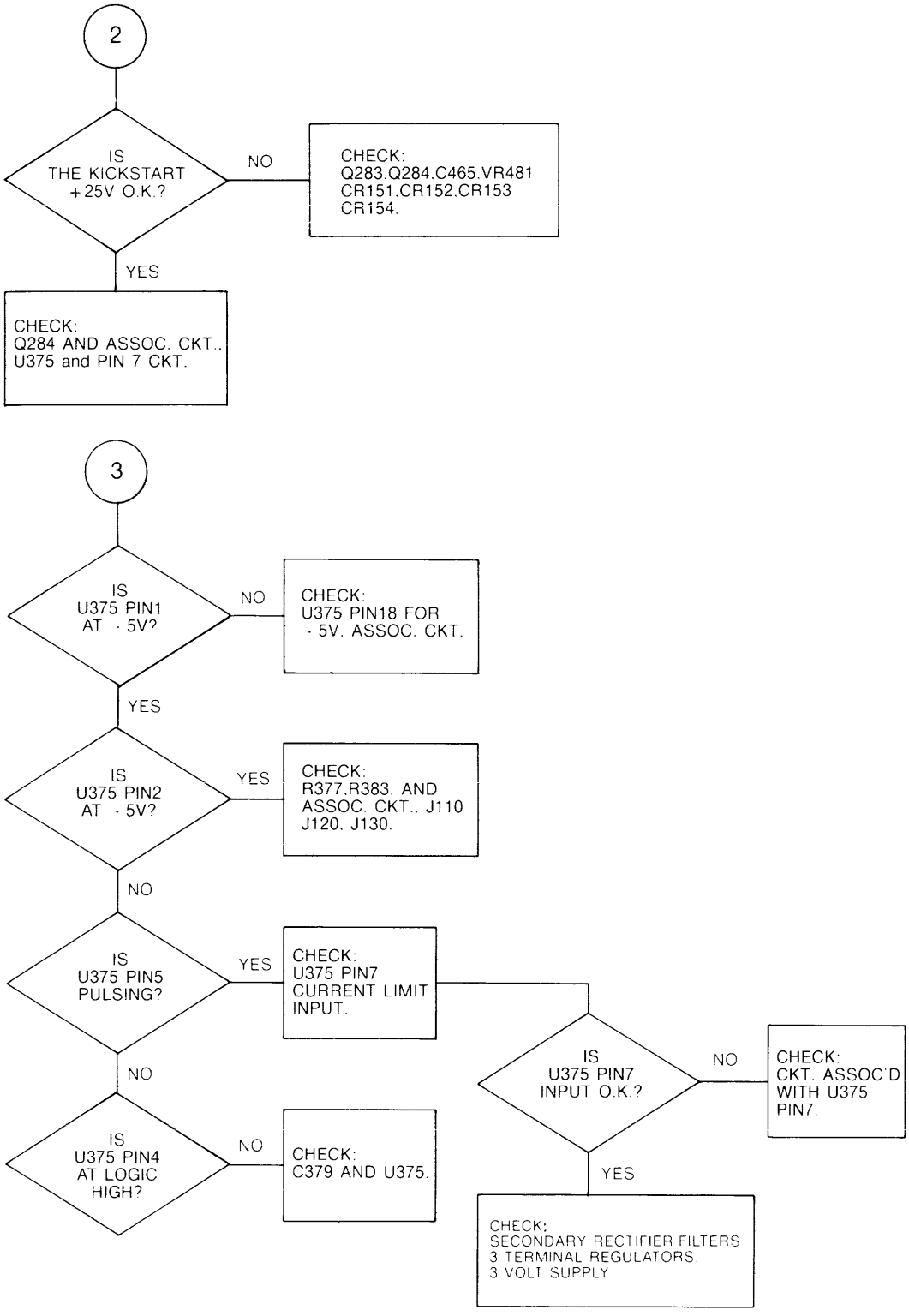


Figure 8-1A. 670-7534-06 power supply troubleshooting tree (cont.).

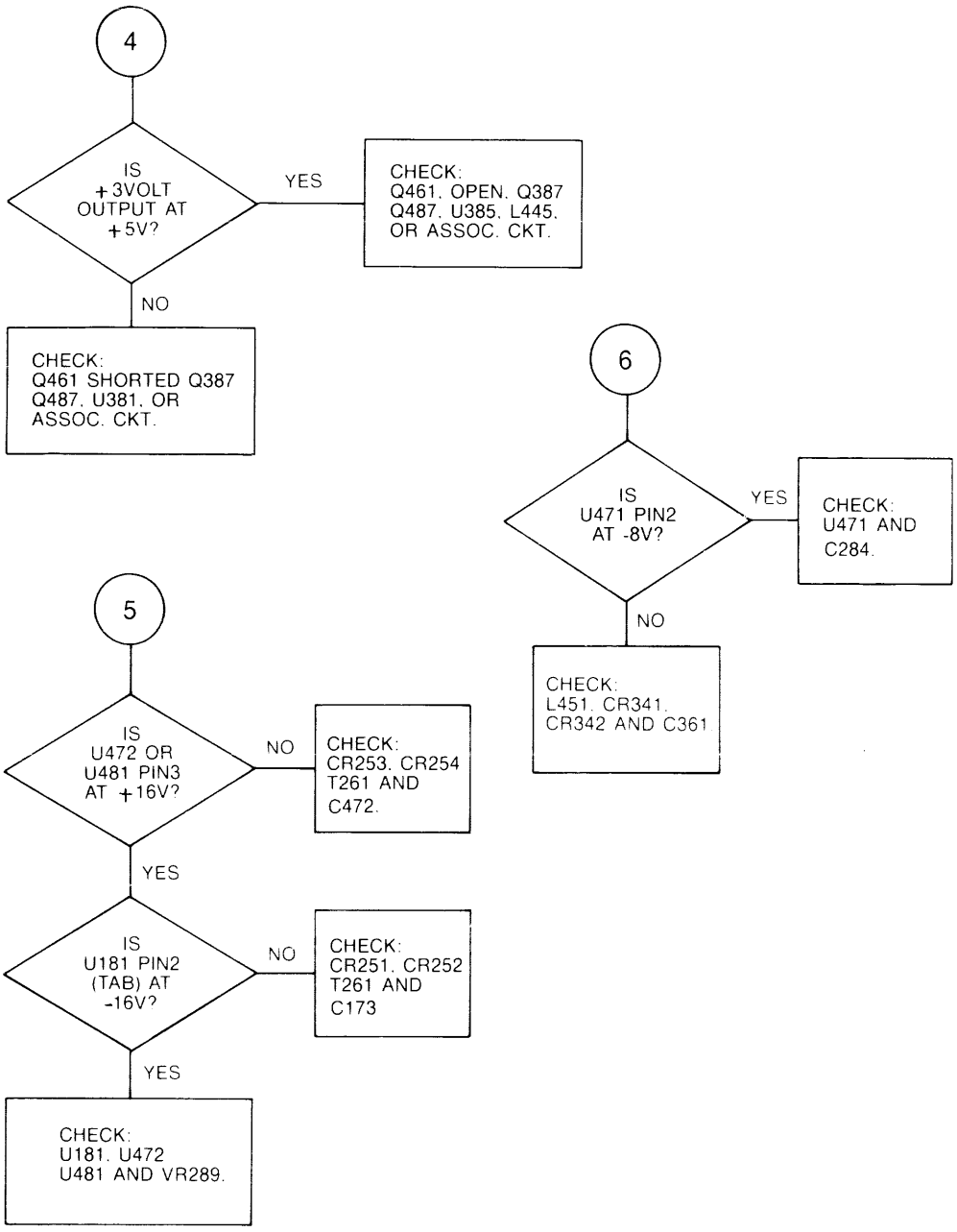


Figure 8-1A. 670-7534-06 power supply troubleshooting tree (cont.).

POWER SUPPLY TROUBLESHOOTING

Troubleshooting of the 1240 power supply should only be performed by qualified service personnel. If a power supply is suspected of being faulty, check the following areas before continuing with troubleshooting procedures:

- ac line cord properly installed
- rear panel MAIN POWER SWITCH in proper position
- rear panel line selector switched to the proper position
- rear panel ac line fuse in good condition
- thermal fuse on the Interface Board not blown due to excessive instrument temperature
- power supply load jumper in proper position (refer to the *Maintenance* section)

CAUTION

When troubleshooting the 1240 power supply, do not defeat the operation of any voltage or current protection circuitry. If protection circuitry is disconnected, damage may occur to the power supply and other boards.

1240 Thermal Fuse

The 1240 is equipped with an over-temperature fuse that opens when the internal temperature of the instrument reaches 100° C (212° F). If the fuse (located on the Interface Board) should open, instrument operation will not be possible until the fuse is replaced. For replacement part numbers, refer to the *Replaceable Electrical Parts* section.

1240 Power Supply Troubleshooting Trees

Power supply troubleshooting trees should be used when troubleshooting a 1240 power supply. The first tree points the technician to the correct troubleshooting trees (1-6) that follow. Each of these trees (corresponding to the six failure areas) then guide the technician to the problem source.

There are two versions of the 1240 Power Supply Board. Unless the board has been replaced, instruments with serial numbers B079999 and below contain board number 670-7534-05, and instruments with serial numbers B080000 and above contain board number 670-7534-06. Figure 8-1A is the troubleshooting tree for the 670-7534-06 board. Figure 8-1B is the troubleshooting tree for the 670-7534-05 board.

670-7534-05 POWER SUPPLY TROUBLESHOOTING TREE

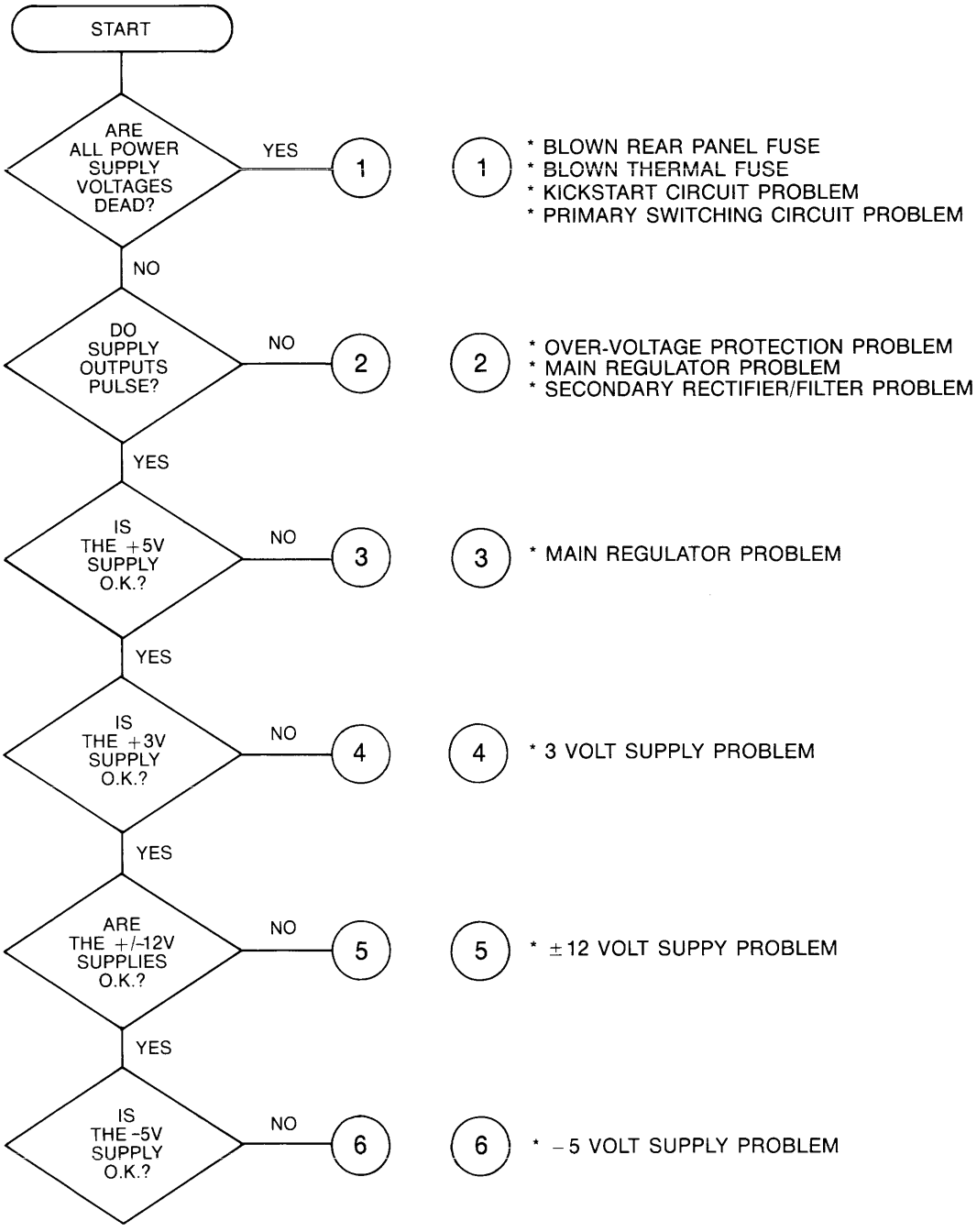


Figure 8-1B. 670-7534-05 power supply troubleshooting tree.

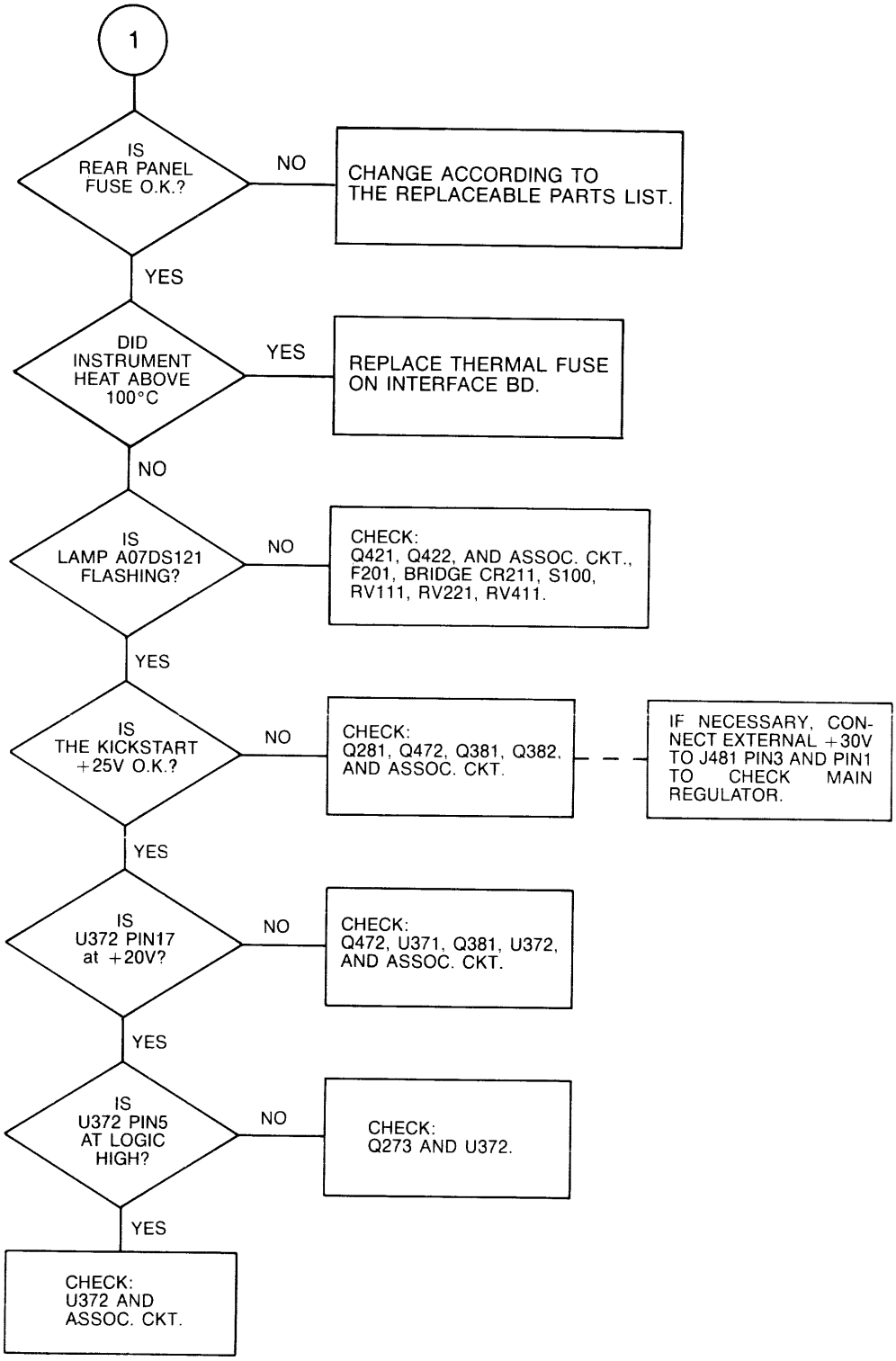


Figure 8-1B. 670-7534-05 power supply troubleshooting tree (cont.).

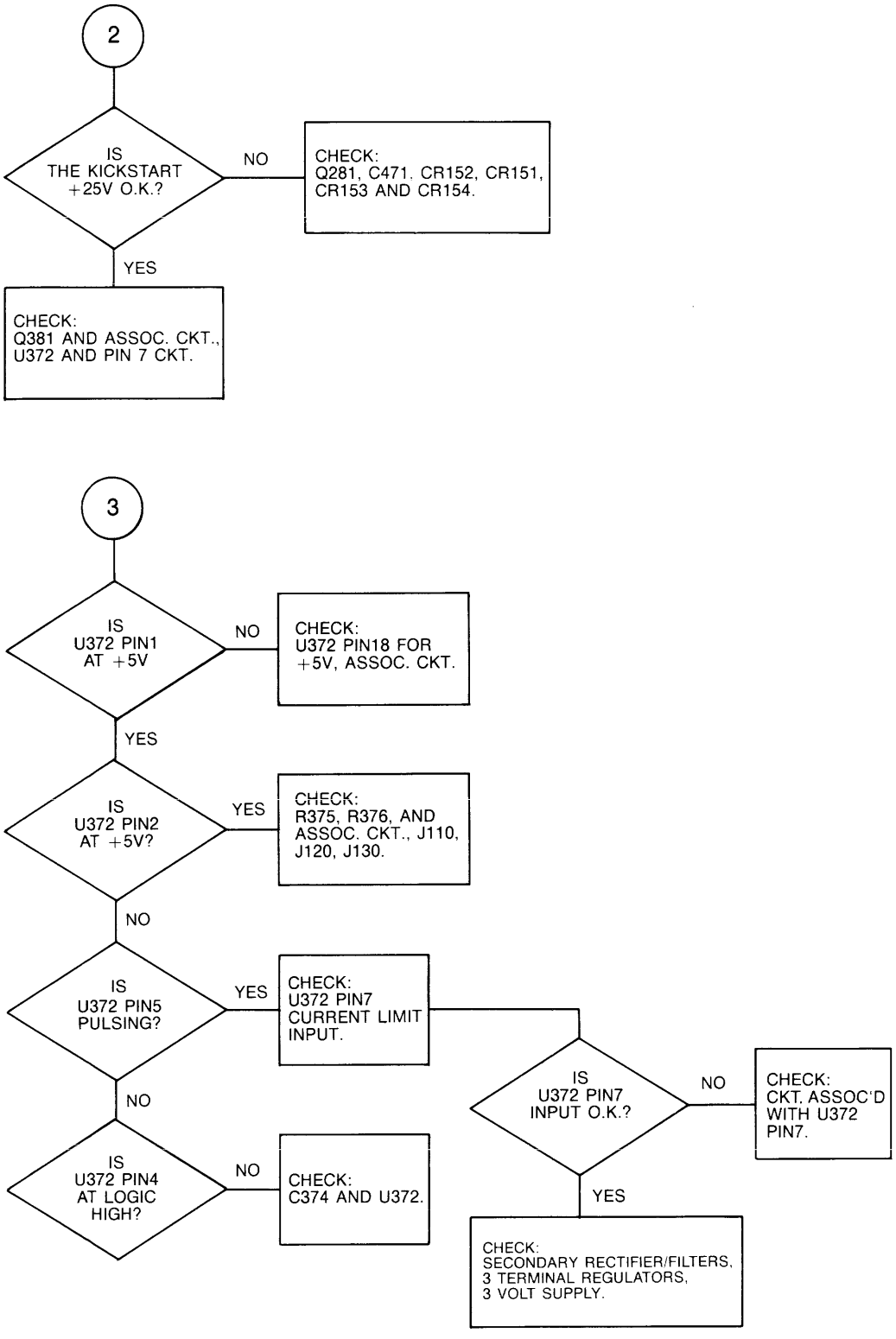


Figure 8-1B. 670-7534-05 power supply troubleshooting tree (cont.).

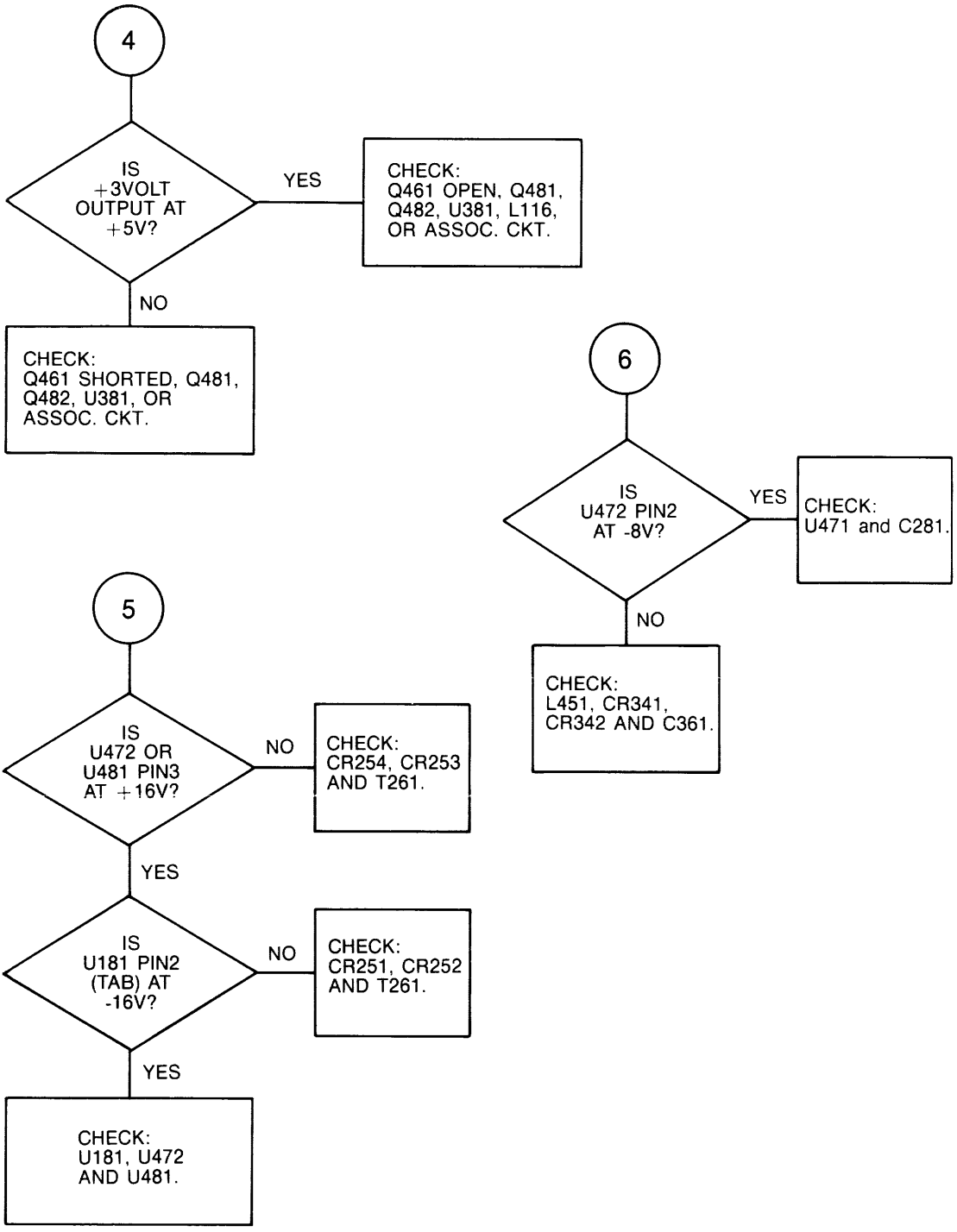


Figure 8-1B. 670-7534-05 power supply troubleshooting tree (cont.).

CRT DRIVE BOARD TROUBLESHOOTING

CRT Drive Board circuit waveforms in Figures 8-2 to 8-10 should be used as reference waveforms when troubleshooting the CRT Drive Board. The top waveform in each figure shows the proper waveform for the point being observed, the bottom waveform shows the trigger source being used.

In addition to the supplied waveforms, the following voltages at specified test points may be used for troubleshooting purposes:

- A06TP331: -75 vdc to +25vdc +/- 5%
- A06TP342: +500 vdc +/- 5%

Jumper A11J155 on the Display Board, when put in the TEST position (pins 2 and 3 shorted), applies a .6 MHz square wave video signal to the CRT's Z-Axis amplifier. The resulting pattern (jailbars) is useful when troubleshooting the CRT Drive Board.

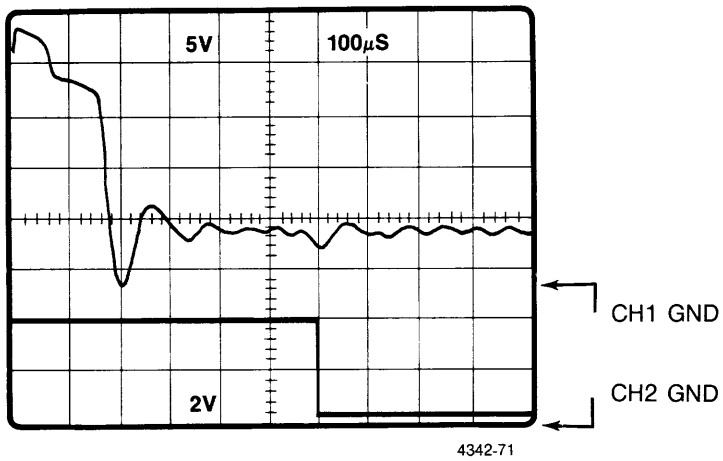


Figure 8-2. A06TP414 vertical sweep out; A06TP111 VDRIVE(H).

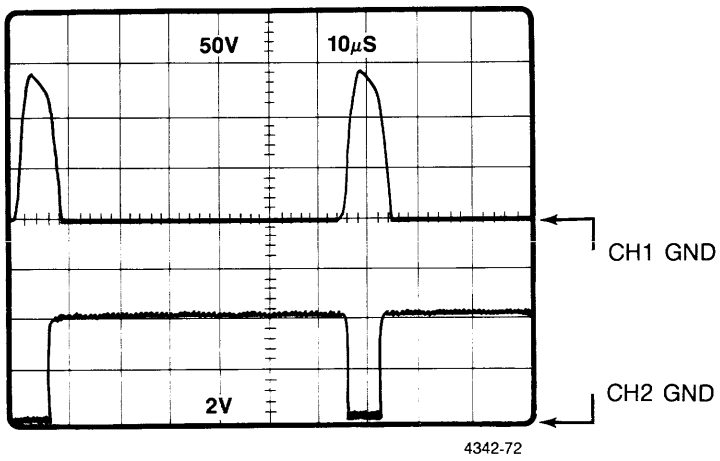


Figure 8-3. A06TP452 horizontal flyback; A06TP521 HDRIVE(L).

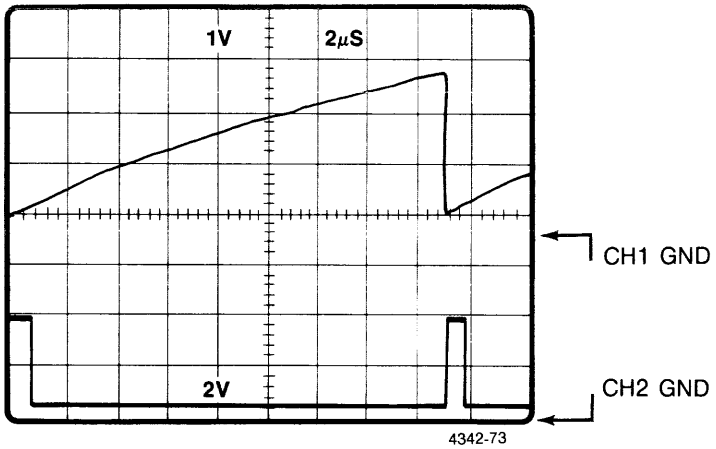


Figure 8-4. A06U311-9 vertical oscillator; A06TP111 VDRIVE(H).

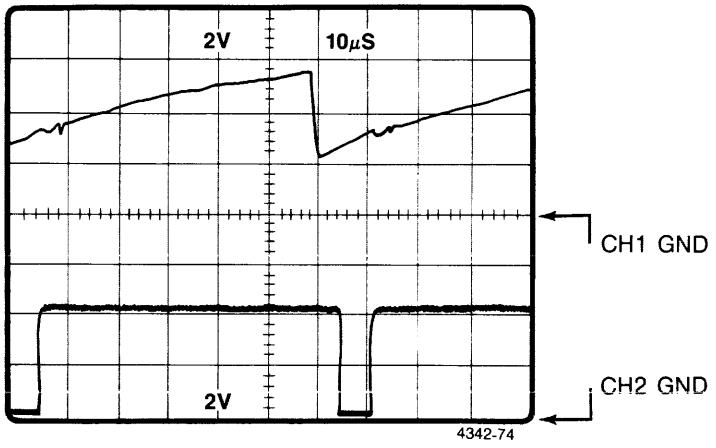


Figure 8-5. A06U534-7 horizontal oscillator; A06TP521 HDRIVE(L).

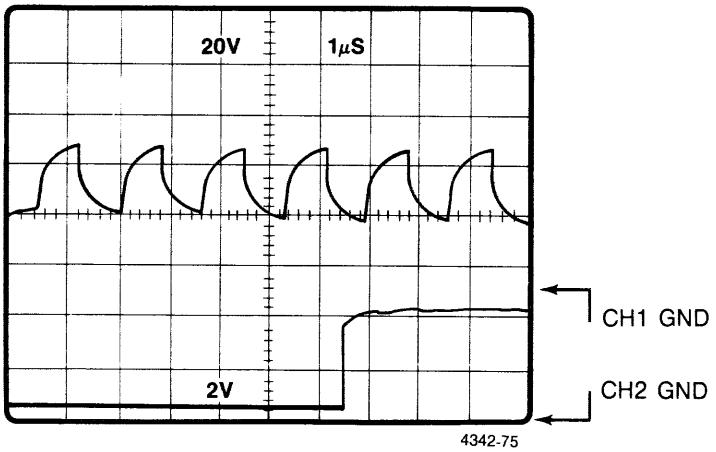


Figure 8-6. A06TP210 cathode Z-axis amplifier with Display Board A11J155 in TEST position; A06TP521 HDRIVE(L).

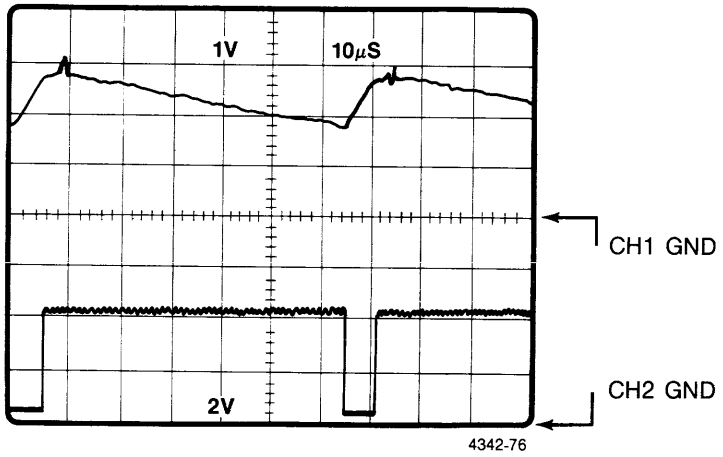


Figure 8-7. A06U534-4 sawtooth input; A06TP521 HDRIVE(L).

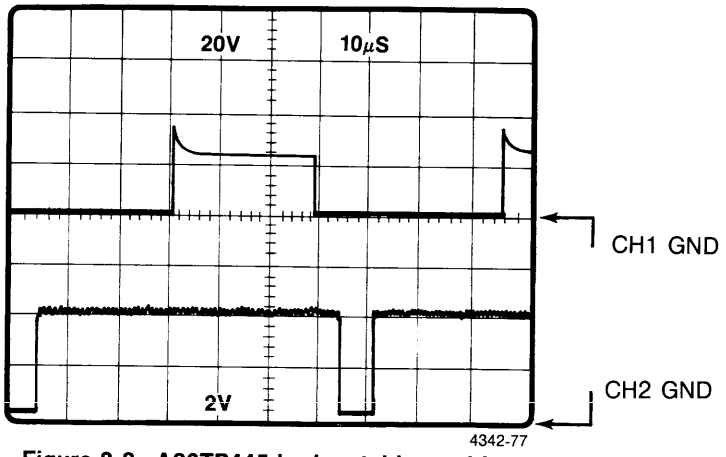


Figure 8-8. A06TP445 horizontal base drive; A06TP521 HDRIVE(L).

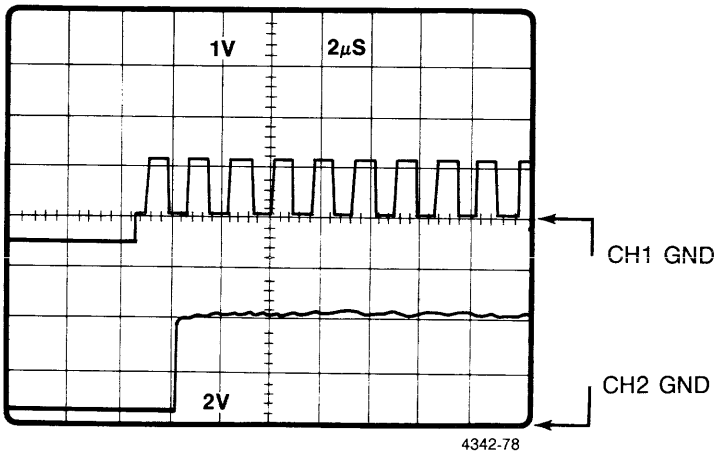


Figure 8-9. Video Out BNC with Display Board A11J155 in TEST position; A06TP521 HDRIVE(L).

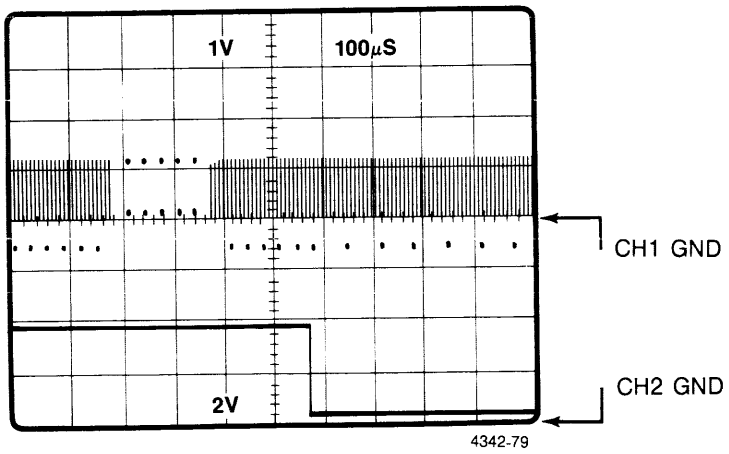


Figure 8-10. Video Out BNC with Display Board A11J155 in TEST position; A06TP111 VDRIVE(H).

SOFT KEY TROUBLESHOOTING

In the event that an on-screen soft key failure occurs, the diagnostics may appear to be inoperable. To circumvent this function failure, the diagnostics will duplicate the function of the soft keys on the front-panel keyboard when it detects a soft key failure during the power-up diagnostics. The 0 through 9 keys represent the on-screen soft keys, as shown by Figure 8-11.

If a soft key failure is detected at power-up, the ENTER NORMAL OPERATION soft key will not work until the problem is corrected. Once the diagnostics successfully pass that error during power-up, the ENTER NORMAL OPERATION soft key will operate correctly.

NOTE

Hard key number 4 allows a bypass of the inoperable ENTER NORMAL OPERATION soft key.

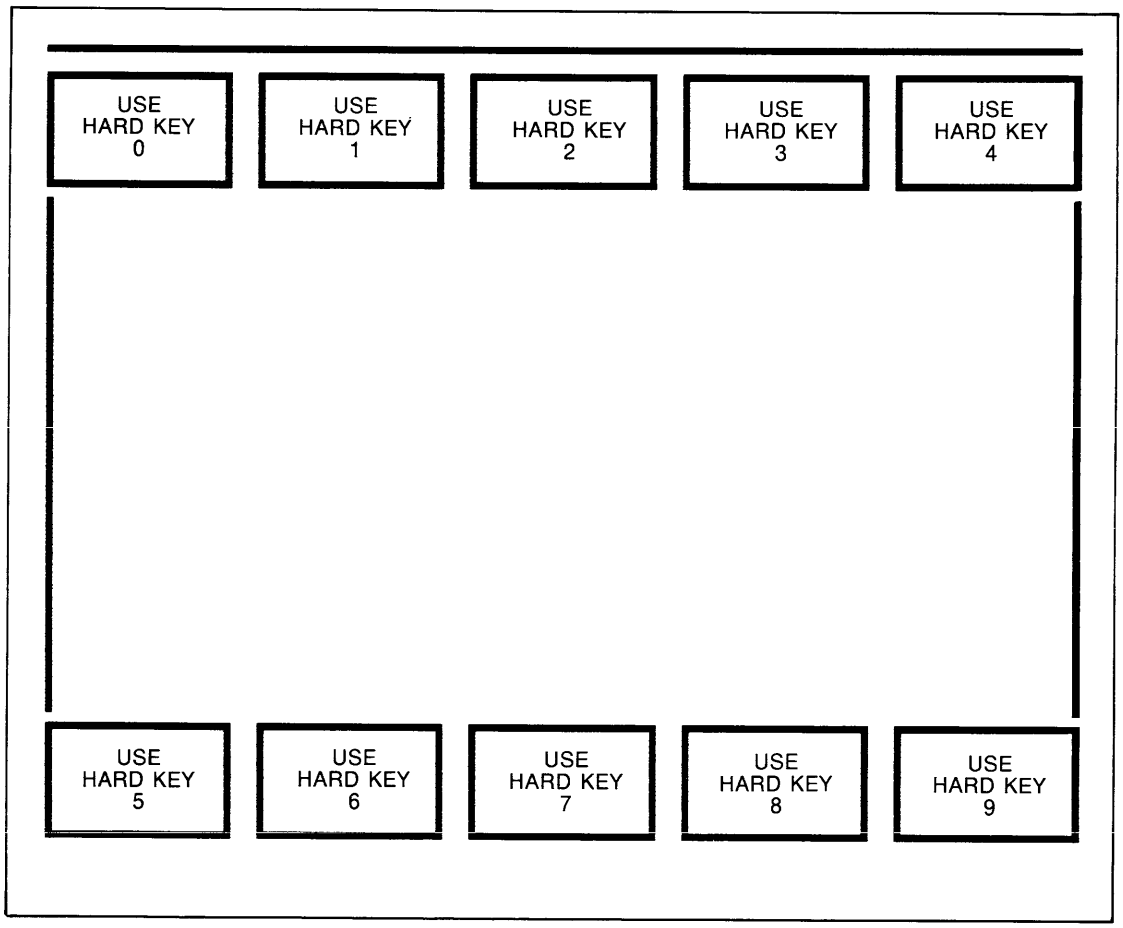


Figure 8-11. Hard key numbers corresponding to soft key boxes.

If a soft key problem still permits limited use of the soft keys, use the Soft Key Adjustment Pattern screen display (shown in Figure 5-4). This screen display shows each soft key as a box. By touching these boxes, the technician may activate any desired soft key and check the results within the circuitry. To obtain the soft key screen display, use the following steps:

1. Enter the diagnostics by simulating a keyboard failure (hold down a key during power-up).
2. Select the FRONTPANEL module and touch the MODULE DIAGNOSTIC soft key.
3. Select the FP VERIFY area and touch the AREA DIAGNOSTIC soft key.
4. Select routine 2 and press the START key.

If soft key problems do not permit the use of any soft keys, the soft key circuit waveforms in Figures 8-12 to 8-17 should be used as reference waveforms for troubleshooting the soft key circuitry. The top waveform in each figure shows the proper waveform for the point being observed, the bottom waveform shows the trigger source being used. The trigger source, A10TP320, is a strobe signal that occurs after all seven LEDs have been scanned.

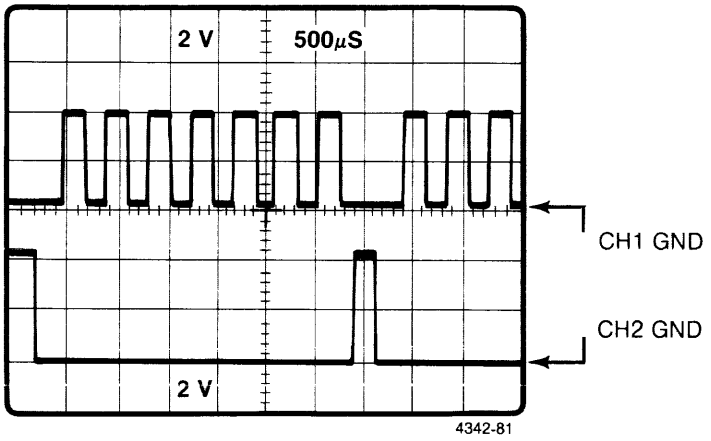


Figure 8-12. A10TP325 shows soft key pulses after processing; A10TP320 shows the trigger waveform.

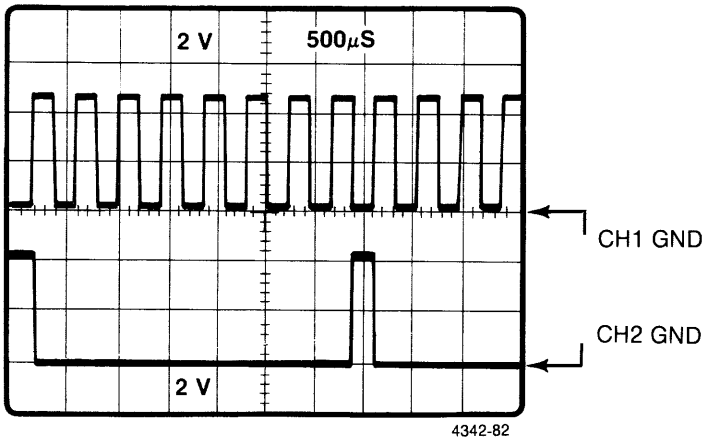


Figure 8-13. A10TP226 shows the timing signal that splits each soft key sample into two halves (i.e., sample/hold); A10TP320 shows the trigger waveform.

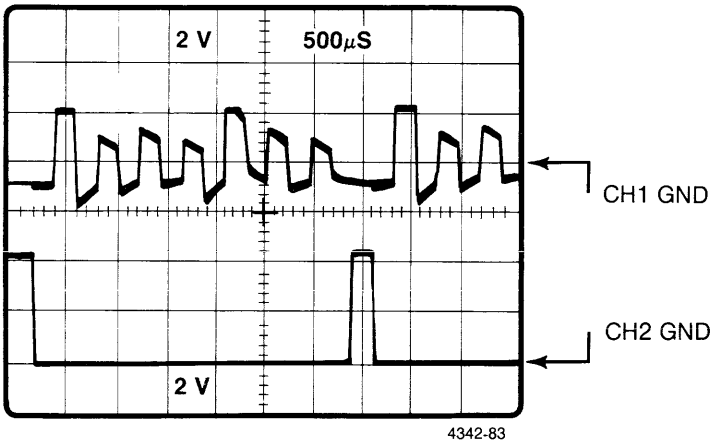


Figure 8-14. A10TP322 shows the output of the subtractor amplifier; A10TP320 shows the trigger waveform.

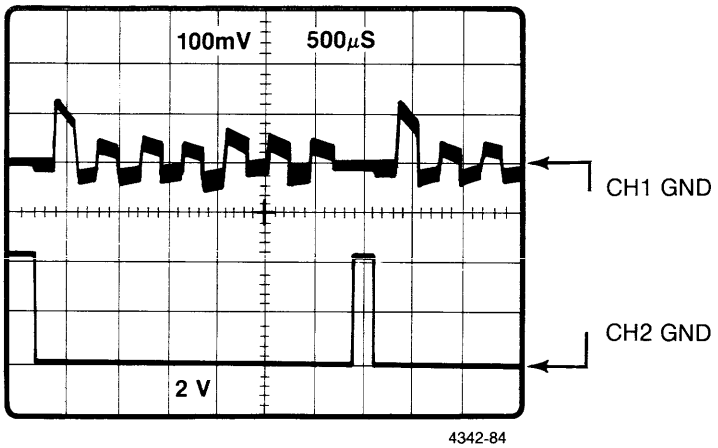


Figure 8-15. A10TP312 shows multiplexed LED/Phototransistor pulses (from the Keyboard) before processing; A10TP320 shows the trigger waveform.

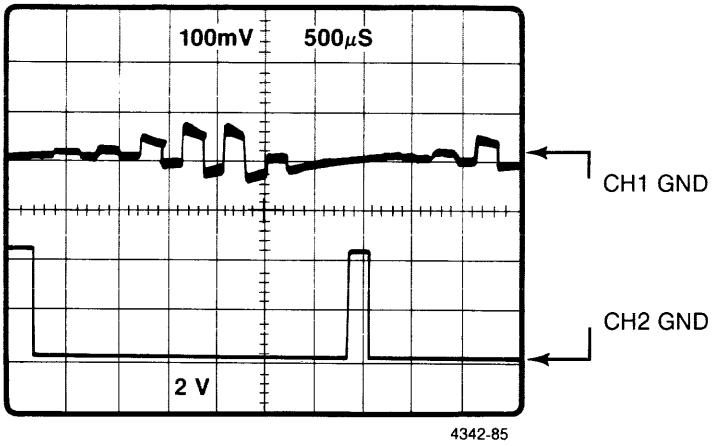


Figure 8-16. A05U205-1 shows typical LED /Phototransistor soft key pulses before multiplexing; A10TP320 shows the trigger waveform.

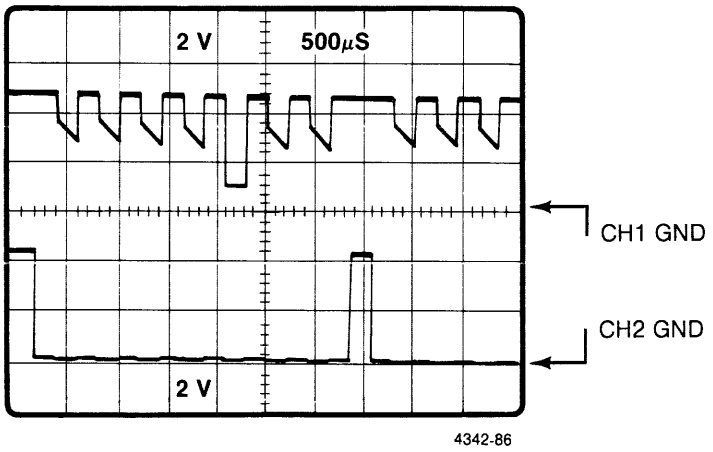


Figure 8-17. A03DS110 of LED-1 Board (at J100 pin 5) shows the cathode of photodiode being pulled low when selected by A05U525; A10TP320 shows the trigger waveform.

KEYBOARD FAILURES

If the keyboard is suspected of being faulty or having intermittent keys, the 1240 diagnostics can be used to help troubleshoot the faulty circuitry. A manual test in the diagnostics produces a keyboard screen display. When a hard key is pressed, the corresponding screen key (and no other key on the screen) should disappear. When the key is released, the display for that key should return. By touching the keys, the technician can activate keyboard circuitry and check the results within the circuitry.

To obtain the keyboard/knob screen display, use the following steps:

1. Enter the diagnostics by simulating a keyboard failure (hold down a key during power-up).
2. Using the Select keys or the Knob, choose the FRONTPANEL module and touch the MODULE DIAGNOSTIC soft key.
3. Select the FP VERIFY area and touch the AREA DIAGNOSTIC soft key.
4. Select routine 1 and press the START key.

PROCESSOR LEDS

Four LEDs on the I/O Processor Board (board asssembly A10) and six LEDs on the Control Processor Board (board assembly A9) track the progress of the diagnostic tests. When the 1240 is powered on, the kernel circuit verification tests begin to run simultaneously on the I/O and Control Processors. As each step of the kernel verification tests successfully proceeds, the status is recorded in these LEDs. When a failure is detected, the step at which the failure occurred remains displayed on the LEDs.

For more specific troubleshooting information, refer to the appropriate processor's LED error index in this *Troubleshooting and Repair* section.

KERNEL SIGNATURE ANALYSIS

If neither the 1240 display nor the processor LEDs are operational, the technician has available an additional troubleshooting aid. By removing the hardware strap and associated resistor pack on either processor board, he may isolate the CPU (Central Processing Unit) from the ROM and RAM. This operation places the CPU in a forced NOP (no operation) loop that increments the address lines each time the CPU executes an instruction cycle. Using a signature analyzer, the technician may take signatures from the processor kernel circuitry and compare them to predetermined signature values contained in Tables 8-4 through 8-8. In this manner, the technician should be able to determine the source of the problem.

Use the appropriate processor's schematic during kernel troubleshooting to help locate the problem circuitry. Start troubleshooting the kernel circuitry by checking the clock, Vcc supply, and reset line to the microprocessor. After placing the processor in a forced NOP loop, check the microprocessor address lines to verify that the lines are incrementing (indicated by correct signatures). After checking CPU signatures, continue by verifying address buffer signatures, then decoder, and finally ROM signatures.

I/O Processor Kernel Troubleshooting

Before starting any troubleshooting procedures, ensure that the Z80 CPU on the I/O Processor Board is receiving the necessary +5 volts Vcc at A10U445-11 and 4 MHZ clock at U445-6. The following steps outline the setup procedure necessary for taking signatures on the I/O Processor kernel circuitry:

1. With the 1240 powered down, remove the I/O Processor Board and replace it on Extender Board assembly A21.
2. Remove the resistor pack A10R455, remove the jumper A10J315, and place jumper A10J450 to the TEST position. (This puts the processor into a NOP loop.) Power up the 1240.
3. Remove the P6451 and P6107 probes from the top compartment of the TEKTRONIX 308 Data Analyzer. Remove the probe tip (P/N 206-0252-00) from the top compartment and place it on the P6107 probe. Connect the clip lead to +5 V (the Vcc pin of a close by TTL I.C.).
4. Set the 308 analyzer's TTL VAR switch to TTL. Connect the probes to the signature analyzer and power it on. Select the 308's standard signature mode and connect the P6451's Clock, Start, and Stop leads as indicated by the table.
5. Tables 8-4 through 8-6 contain Clock, Start, and Stop polarity settings, and signatures for the I/O Processor kernel circuitry. The polarity settings are taken from test points located on the I/O Processor Board.

NOTE

To ensure a proper signature analyzer setup, check the +5 volt and ground signatures against the table being used.

Control Processor Kernel Troubleshooting

Before starting any troubleshooting procedures, ensure that the 8088 CPU on the Control Processor Board is receiving the necessary +5 volts Vcc at A9U347-40 and 5 MHZ clock at U347-19. The following steps outline the setup procedure necessary for taking signatures on the Control Processor kernel circuitry:

1. With the 1240 powered down, remove the Control Processor Board and replace it on Extender Board assembly A21.
2. Remove the resistor pack A9R461 and place jumper A9J467 to the TEST position. (This puts the processor into a NOP loop.) Power up the 1240.
3. Remove the P6451 and P6107 probes from the top compartment of the TEKTRONIX 308 Data Analyzer. Remove the probe tip (P/N 206-0252-00) from the top compartment and place it on the P6107 probe. Connect the clip lead to +5 V (the Vcc pin of a close by TTL I.C.).
4. Set the 308 analyzer's TTL VAR switch to TTL. Connect the probes to the signature analyzer and power it on. Select the 308's standard signature mode and connect the P6451's Clock, Start, and Stop leads as indicated by the table.
5. Tables 8-7 and 8-8 contain Clock, Start, and Stop polarity settings, and signatures for the Control Processor kernel circuitry. The polarity settings are taken from test points located on the Control Processor Board.

NOTE

To ensure a proper signature analyzer setup, check +5 volt and ground signatures against the table being used.

Table 8-4
I/O P SIGNATURES: CPU, BUFFERS, AND DECODERS

Clock	⌐	J280-1	+5 Volts	0001
Start	⌐	J280-9	GND	0000
Stop	⌐	J280-9	Indeterminate	----

Location	Signature	Location	Signature	Location	Signature	Location	Signature
A10U445		A10U340		11	29A6	12	4231
1	1293	2	HAP7	12	F2A6	13	4231
2	HAP7	3	3C96	13	PC01	14	0001
3	3C96	4	0000	14	0001	A10U120	
4	3827	6	3827	A10U350		1	52F8
5	755P	7	755P	1	0000	2	HC89
6	0001	A10U130		2	----	3	2H70
7	0000*	1	12U3	4	0000	4	9840
8	0000*	2	1293	6	0001	5	0000
9	0000*	3	HAP7	8	5H21	6	HPP1
10	0000*	4	8P4P	10	0000	7	4814
11	0001	5	9840	11	UUUU	8	0000
12	0000*	6	A277	13	5555	9	4869
13	0000*	7	A68C	15	CCCC	10	1P7P
14	0000*	8	0000	17	7F7F	11	A5U0
15	0000*	16	0001	19	0000	12	2H75
16	0000	A10U345		20	0001	13	3P95
17	0001	1	0000	A10U360		14	F388
18	0001	2	1293	1	HPP0	15	1603
19	0000	4	52F8	2	HPP1	16	0001
20	0001	6	UPFH	3	9840	A10U125	
21	----	8	0AFA	4	9841	1	52F8
22	0001	9	0001	5	0000	2	HC89
23	0001	10	0000	6	0001	3	2H70
24	0001	11	----	7	0000	4	9840
25	0001	13	HC89	8	0000	5	9840
26	0001	15	2H70	9	0001	6	HPP0
27	0000	17	HPP0	10	3P94	7	8A03
28	0001	19	0000	11	3P95	8	0000
29	0000	20	0001	12	----	9	A305
30	UUUU	A10U270		13	----	10	CFP2
31	5555	1	0001	14	0001	11	4FU3
32	CCCC	2	0001	A10U365		12	7C4A
33	7F7F	3	0001	4	FF7U	13	6351
34	5H21	4	29A6	5	8P4P	14	8A6F
35	0AFA	5	P5H8	6	4231	15	APC9
36	UPFH	6	FF7U	7	0000	16	0001
37	52F8	7	0000	8	P5H8		
38	HC89	8	4814	9	9841		
39	2H70	9	0001	10	HPP0		
40	HPP0	10	4814	11	4230		

** indicates the Probe Tip (206-0252-00) was not connected to the P6107 probe when the signature was taken.*

Table 8-5
I/O P SIGNATURES: DECODERS AND BUFFERS OUTPUTS

Clock	⌐	J280-1	+5Volts	0001
Start	⌐	J280-9	GND	0000
Stop	⌐	J280-9		

Location	Signature	Location	Signature
A10U380		A10U340	
1	3C96	9	755P
2	3827	10	3827
3	755P	15	3C96
4	0000	16	HAP7
5	0000	A10U345	
6	0001	3	HPP0
7	F2A6	5	2H70
8	0000	7	HC89
9	PC01	12	0AFA
10	12U3	14	UPFH
11	4P0A	16	52F8
12	P255	18	1293
13	U3H5	A10U350	
14	0996	3	7F7F
15	6H49	5	CCCC
16	0001	7	5555
		9	UUUU
		12	5H21
		14	0001
		16	0000
		18	0000

Table 8-6
I/O P SIGNATURES: ROM DATA LINES

Clock	⌐	J280-1	+5 Volts	P254
Start	⌙	UXXX-20*	GND	0000
Stop	⌐	UXXX-20*		

Location	Signature	Location	Signature	Location	Signature
A10U160		A10U170		A10U185	
11	9PA1	11	6108	11	3363
12	F4C0	12	30P7	12	664U
13	3F3F	13	9P61	13	8H60
15	65C8	15	88A5	15	06F0
16	951U	16	86P7	16	3AC7
17	F6C4	17	CA89	17	AF91
18	3316	18	7375	18	9PU0
19	9184	19	82H4	19	9PH9
A10U165		A10U180			
11	27AC	11	FA2A		
12	1HU5	12	F437		
13	3UA8	13	AUUP		
15	9F21	15	9774		
16	3212	16	UAH5		
17	7FH5	17	PH82		
18	6CC8	18	397P		
19	CHAA	19	UAP8		

** Where XXX denotes ROM under test.*

Table 8-7
CON P SIGNATURES: CPU, BUFFERS, DECODERS, AND ROM

Clock	⌞	J100-1	GND	0000
Start	⌜	J100-10	+5 Volts	000U
Stop	⌜	J100-10	Indeterminate	----

Location	Signature	Location	Signature	Location	Signature	Location	Signature
A9U347		13	PUA7	A9U451		9	9696
1	0000	14	H389	1	0000	10	UUUU
2	0005	15	H389	2	2A3U	20	258F
3	P064	16	69F8	3	9643	21	H389
4	69F8	17	69F8	4	U668	22	0009
5	7P50	18	000F	5	0P0P	23	7P50
6	H389	19	000F	6	9696	24	P962
7	P962	20	000U	7	----	25	PUA7
8	PUA7	A9U361		8	HHHA	26	P064
9	6C82	1	000U	9	UUUU	A9U233	
10	HF4A	2	000U	10	0000	1	258C
11	9643	3	000U	11	0008	2	0005
12	U668	4	000U	12	7APF	3	000F
13	5655	5	0008	13	P90H	4	FFF2
14	P90H	6	0008	14	5655	5	6669
15	----	7	0000	15	6225	6	3338
16	HHHA	8	0009	16	HPU1	7	CF17
17	0000	9	0009	17	HF4A	8	0000
18	0000	10	000U	18	6C82	9	258F
19	----	11	8953	19	----	10	000U
20	0000	12	7P50	20	000U	11	000U
21	0000	13	4601	A9U255		12	000U
22	000U	14	000U	1	0008	13	000F
23	0000	A9U354		2	9F31	14	0005
24	000U	1	C9C2	3	9F31	15	258F
25	0008	2	9F3P	4	258C	16	000U
26	000H	3	9F31	5	000U	A9U357	
27	0000	4	0008	6	000U	1	000U
28	0000	5	9F31	7	258F	2	HPU1
29	000U	6	9F3P	8	0000	3	A9H6
30	0000	7	C9C2	9	000U	4	000U
31	0000	8	0000	10	000U	5	000U
32	0009	9	C9C2	11	000U	6	000U
33	000U	10	9F3P	12	000U	7	000U
34	0000	11	9F31	13	8953	8	0000
35	C9C2	12	0008	14	892U	9	000U
36	C9C2	13	9F31	15	000U	10	000U
37	C9C5	14	9F3P	16	000U	11	000U
38	C9C2	15	C9C5	A9U257		12	000U
39	000F	16	000U	7	0000	13	2A3U
40	000U	A9U258		8	000U	14	0P0P
A9U351		1	000F	9	000H	15	000U
1	0000	2	0005	10	000U	16	000U
2	0005	3	000U	11	000U	A9U201	
3	0005	4	P064	12	000U	1	0000
4	P064	5	69F8	13	8951	2	000U
5	P064	6	4601	14	000U	3	9F31
6	7P50	7	0000	A9U135		4	000U
7	7P50	8	485H	2	69F8	5	000U
8	P962	9	H389	3	----	6	9F31
9	P962	10	4P15	4	HPU1	7	000U
10	0000	11	000U	5	2A3U	8	0000
11	0008	12	PUA7	6	0P0P	15	0000
12	PUA7	13	P962	7	6225	16	000U
		14	000U	8	7APF		

Table 8-8a
DIAGNOSTICS VERSION 7-2
CON P SIGNATURES: ROM DATA LINES

Clock	⌐	J101-11	+5 Volts UP73
Start	⌐	U233-9	GND 000U
Stop	⌐	U233-9	

Location	Signature
A9U135	
11	07UC
12	868P
13	27C9
15	8682
16	4U5C
17	8P94
18	AP84
19	PP30

Table 8-8b
DIAGNOSTICS VERSION 8-2
CON P SIGNATURES: ROM DATA LINES

Clock	⌐	J101-11	+5 Volts UP73
Start	⌐	U233-9	GND 000U
Stop	⌐	U233-9	

Location	Signature
A9U135	
11	07U7
12	868H
13	27C9
15	8683
16	4U5A
17	8P94
18	AP87
19	PP33

There are two valid sets of signatures for Diagnostics Version 9-2. The signatures should match either those in table 8-8c or 8-8d.

Table 8-8c
DIAGNOSTICS VERSION 9-2
CON P SIGNATURES: ROM DATA LINES

Clock	⌐	J101-11	+5 Volts UP73
Start	⌐	U233-9	GND 0000
Stop	⌐	U233-9	

Location	Signature
A9U135	
11	07U7
12	P678
13	671H
15	A6H0
16	2UAP
17	FP31
18	AP87
19	PP33

Table 8-8d
DIAGNOSTICS VERSION 9-2
CON P SIGNATURES: ROM DATA LINES

Clock	⌐	J101-11	+5 Volts UP73
Start	⌐	U233-9	GND 0000
Stop	⌐	U233-9	

Location	Signature
A9U135	
11	07U8
12	P676
13	6712
15	A6H0
16	2UAH
17	FP33
18	AP86
19	PP30

TROUBLESHOOTING USING DIAGNOSTICS ERROR INFORMATION

DIAGNOSTICS OVERVIEW

The 1240 diagnostic tests provide information describing the operational status of the 1240. Diagnostics performed automatically at power-up check out major 1240 circuitry and firmware functions. When power-up diagnostics are successfully completed, the 1240 defaults to the Operation Level menu. If failures are detected during power-up diagnostics, the operator may choose to continue with additional diagnostic tests or bypass the diagnostics (if failures are acceptable, e.g., failures in acquisition boards not being used). If the 1240 is not able to produce a screen display to summarize power-up failure information, the service technician must use other methods to troubleshoot the malfunction. Table 8-1, Recommended Servicing Approach, outlines the troubleshooting procedures available in this *Troubleshooting and Repair* section.

Diagnostic test results are reported using three different menu displays which, in order of their hierarchy, are: Main Diagnostic (automatically displayed at power-up if a failure is detected), Module Diagnostic, and Area Diagnostic. Refer to *Diagnostic Menu Overview* in Section 1, *General Information*, for menu details. These diagnostic test menus supply the technician with specific error indexes (and sometimes test results) that point to 1240 troubleshooting information. In the event the 1240 does not detect a failure during power-up, access the diagnostics by holding down any front panel key during power-up to induce a failure.

Some of the tests within the menus reside in the Diagnostic ROM pack, found in the 1240 Service Maintenance Kit. The Diagnostic ROM pack also contains manual diagnostic tests (described later in this section) and calibration routines. The calibration routines are discussed in the *Verification and Adjustment* section in their respective adjustment procedures.

The following Table 8-9 indicates the location of the diagnostic code for each 1240 module:

Table 8-9
DIAGNOSTIC CODE LOCATION

Module	Code Location
I/O Processor	I/O Processor
Frontpanel	I/O Processor
Display	I/O Processor
Comm pack	I/O Processor, COMM pack
Control Processor	Control Processor
Trigger	Control Processor, ROM pack
9-Channel Acq.	Control Processor, ROM pack
18-Channel Acq.	Control Processor, ROM pack
ROM pack	Control Processor
RAM pack	Control Processor

ERROR INDEX OVERVIEW

Diagnostic troubleshooting of the 1240 is based upon the use of screen-displayed four-digit error index numbers. Each number position in the four-digit sequence describes different information about the circuitry being tested. Figure 8-18 shows the error-index format and gives a description of the information indicated by each of the four digit positions.

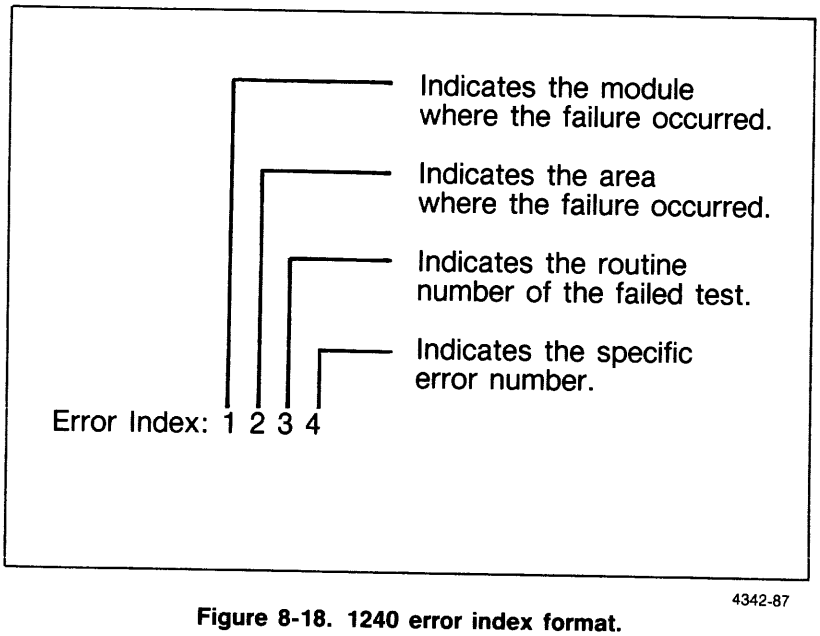


Figure 8-18. 1240 error index format.

Various troubleshooting information sources may be accessed by using the four-digit error index. The following list outlines some of these diagnostic troubleshooting aids:

- page-edge tabs for quick location of error indexes
- area block diagrams showing the involved circuit blocks
- component locators showing the board locations of involved parts
- test descriptions that state the nature of the diagnostic test
- lists of probable causes and recommended actions for repair

Since each error index in linked to many types of diagnostic information sources, it is important to understand the connection between all of these informational areas. *Troubleshooting An Example Failure* develops a procedure showing how to access all available troubleshooting information for a sample error index.

TROUBLESHOOTING AN EXAMPLE FAILURE

In this example, the technician will learn the steps necessary to troubleshoot a sample (operator induced) failure by using the screen-displayed error index number. As the steps progress, different diagnostic troubleshooting information is accessed. By following the same sequence outlined in this example, you may access all available diagnostic troubleshooting information for any LED or screen-displayed error index.

1. Induce a keyboard failure by holding down the 1 key during power-up.
2. A resulting four-digit error index is displayed: 2146.
3. The error index is decoded as module 2 (Frontpanel), area 1 (Hard Key), routine 4, error index 6.
4. To access the diagnostic troubleshooting information for module 2, find the black page-edge tab section containing 2XXX Frontpanel Error Indexes.
5. After finding the Frontpanel module section, search for the specific error index number located on the page-edge tab. The number also appears in the text, along with the associated Hard Key area failure descriptions.
6. A component location figure showing board part locations precedes the error descriptions. The component locator may be used when searching for parts suspected of being faulty.
7. A Hard Key area diagnostic block diagram also precedes the error descriptions. The pattern shading on this block diagram shows the general test path for the Hard Key area tests.

COMM PACK FAILURES

The error indexes supplied for COMM pack failures are not unique error index numbers. Some COMM pack error indexes will be repeated for different COMM packs, however the reason for error will change with each installed COMM pack. When accessing diagnostic error information for COMM packs, first locate the information for the correct type of pack, then locate the correct error index number.

ROM OR RAM PACK FAILURES

To check a ROM or RAM pack with the diagnostics, the 1240 must be powered-down before installing the untested pack. This action allows the 1240 to determine which type of pack is installed, in turn allowing it to run the proper set of diagnostic tests on that pack.

NOTE

The orientation of pin one on the ROM pack ROMs is different than that of the RAM pack RAMs (the I.C. sockets are reverse of each other). If troubleshooting procedures require the removal of a ROM or RAM from either of these packs, verify the pin one orientation before re-installing the part.

ACQUISITION PROBE FAILURES

If a diagnostics error index indicates that an acquisition probe may be the problem causing a diagnostics failure, ensure that the failure is not due to the threshold test being run on a fixed-threshold probe. Only variable threshold probes will pass the diagnostic threshold tests.

TROUBLESHOOTING INTERMITTENT FAILURES

The 1240 diagnostics provide test looping features that allow intermittent circuitry failures to be detected and failure information to be recorded. Selection of the circuitry to be tested is made in one of the diagnostic menus (Main, Module, or Area). Each of the diagnostic menus contains a row of function-selection soft keys that define how the currently displayed menu is tested. Two soft keys within each row are LOOP ON soft keys. These keys allow the user to LOOP ON SELECTED entries in the menu, or LOOP ON ALL entries in the currently displayed menu. By looping diagnostic tests on the appropriate module, area or routine menu entry, problem circuitry is more easily identified.

If a failure is detected during looping, failure information is recorded and preserved, even if the failed circuit begins to operate properly. The PASS/FAIL indication shows the current status of the test, while the ADDR, EXP, ACT, and INDEX fields indicate the most recent failure information. An example of this may be demonstrated by looping on the keyboard area tests while intermittently pressing keyboard buttons.

The 1240 produces a start signal at the beginning of each diagnostic test that may be used as a trigger signal for an oscilloscope or a logic analyzer. This signal is found on test point A10TP385 (I/O Processor Board) for Frontpanel, Display, and I/O Processor module tests. For all other module tests, the signal is found on test point A9TP117 (Control Processor Board). The signal test point is raised to a TTL high logic level at the beginning of each test, and released low at the completion of the test.

REMOTE DIAGNOSTICS

When the 1240 is operating under the real-time operating system software, a TEST command from a remote controller causes the 1240 to execute its power-up diagnostics. The error information collected during the diagnostics is available after test completion while in the normal operating software. After executing the TEST command, the 1240 returns to the default power-up state. The previous setup, if any, is available in storage memory, but not in acquisition or reference memories. The 1240 notifies the controller that the diagnostics are completed with the Test Complete SRQ. After receiving the TEST command, but before sending the SRQ, the 1240 ignores all bus activity.

To read the collected error information, the remote controller sends the DIAG? query. Data returned to the controller is in the following format:

DIAG ERRORS NNNNN NNNNN NNNNN NNNNN...

or

DIAG "ERRORS NOT FOUND"

The leftmost digit of NNNNN is the test sequence number. If more than one of any type of acquisition card is installed, two 9-channel boards for example, this digit will show which module has the error. Use the remaining four digits as error indexes to locate the troubleshooting information in this *Troubleshooting And Repair* section of the manual.

1240 MANUAL TESTS

The 1240 diagnostics provide manual tests that are not run automatically at power-up or during extended (Diagnostic ROM pack) diagnostic testing. These tests allow the user to interact with the 1240 to observe the operation of specific 1240 circuits. The following Table 8-10 lists the Module, Area, Routine number, and a brief description of the manual tests available.

Table 8-10
1240 MANUAL TESTS

Module	Area	Routine #	Description
2XXX-FRONTPANEL	FP VERIFY	1	Hard Key/Knob Verify
	FP VERIFY	2	Screen Align/Soft Key Verify
4XXX-COMMPACK	MANUAL	1	RS232 BERT Test
6XXX-TRIGGER	ATB MANUAL	1	Decade Divider Exerciser
	ATB MANUAL	2	ATB Base Rate Exerciser
7XXX-1240D1	CAL ACQ9	1	Calibrate Threshold
8XXX-1240D2	CAL ACQ18	1	Calibrate Threshold
	CAL ACQ18	2	Calibrate Gate Arrays

TROUBLESHOOTING PAGE LAYOUT

The diagnostics information is grouped according to module name and number (e.g., 2XXX - FRONTPANEL or 3XXX - DISPLAY). Page bleed tabs indicate each different module by changing vertical position on the edge of the page (as shown on the right-hand side of this page). In addition, a box containing module and area information appears at the beginning of each new area.

Below is a summary of typical information found on bleed tab pages.

BLOCK DIAGRAM: A block diagram showing circuitry associated with each diagnostic test area provides a visual representation of exercised circuitry.

COMPONENT LOCATION: An illustration of the board that diagnostics is currently testing provides component location information.

CIRCUIT OVERVIEW: A brief description of normal circuit operation.

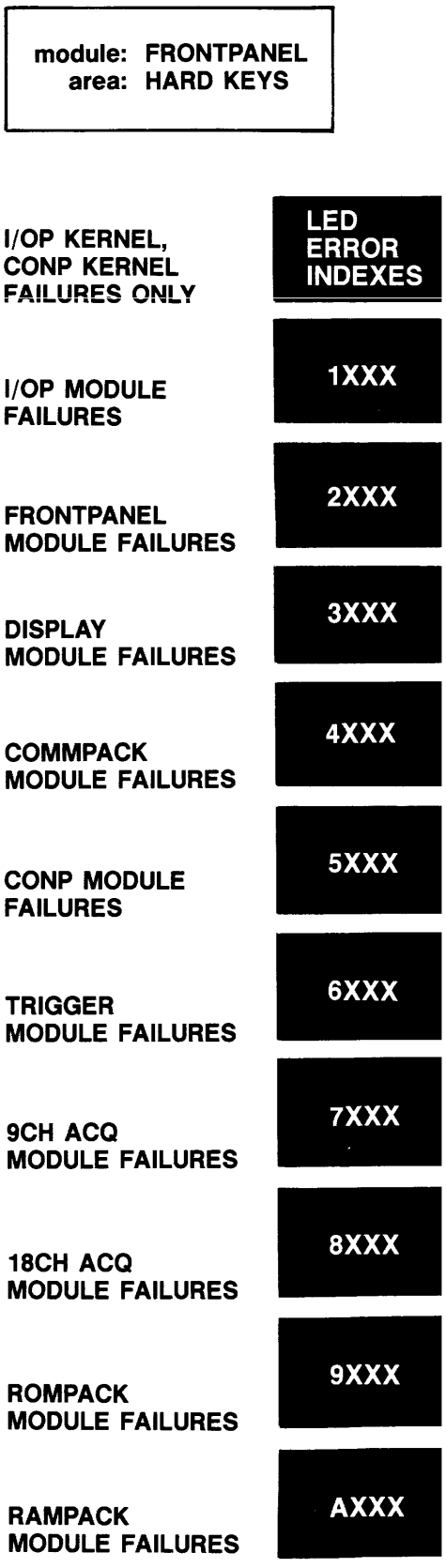
TEST DESCRIPTION: A general description of how the involved circuitry is exercised during the execution of diagnostic tests.

ROUTINE DESCRIPTION: A brief description of how a specific diagnostic routine exercises the involved circuitry.

EXPLANATION: A general description of the problem causing the given error index.

ERROR INDEX: Error indexes serve as pointers to the section of circuitry failing the diagnostic tests. LED error indexes indicate failures according to the state of the LEDs. Screen error indexes indicate failures according to the displayed numeric value. Each digit of the four-digit error index acts as an identifier describing the failed module, area, routine, and error number.

PROBABLE CAUSE/ACTION: A listing of probable reasons for the error indication and suggested actions to remedy the problem.



I/O PROCESSOR KERNEL LED ERROR INDEXES

LED Status	Test Name	Stage Number
0000 1111 1110 1011 1F11 1010 1F1F 1001 1FF1 1000 1FFF	Power-Up and ROM	Stage 0
1101 11F1 11FF	RAM	Stage 1
F000 FFFF	COMM Pack	Stage 2

(0 = OFF, 1 = ON, F = flashing)

	MSB			LSB
LED Position	o	o	o	o
LED Number	A10DS538	536	534	532

I/O PROCESSOR KERNEL BLOCK DIAGRAM
POWER-UP AND ROM – STAGE 0

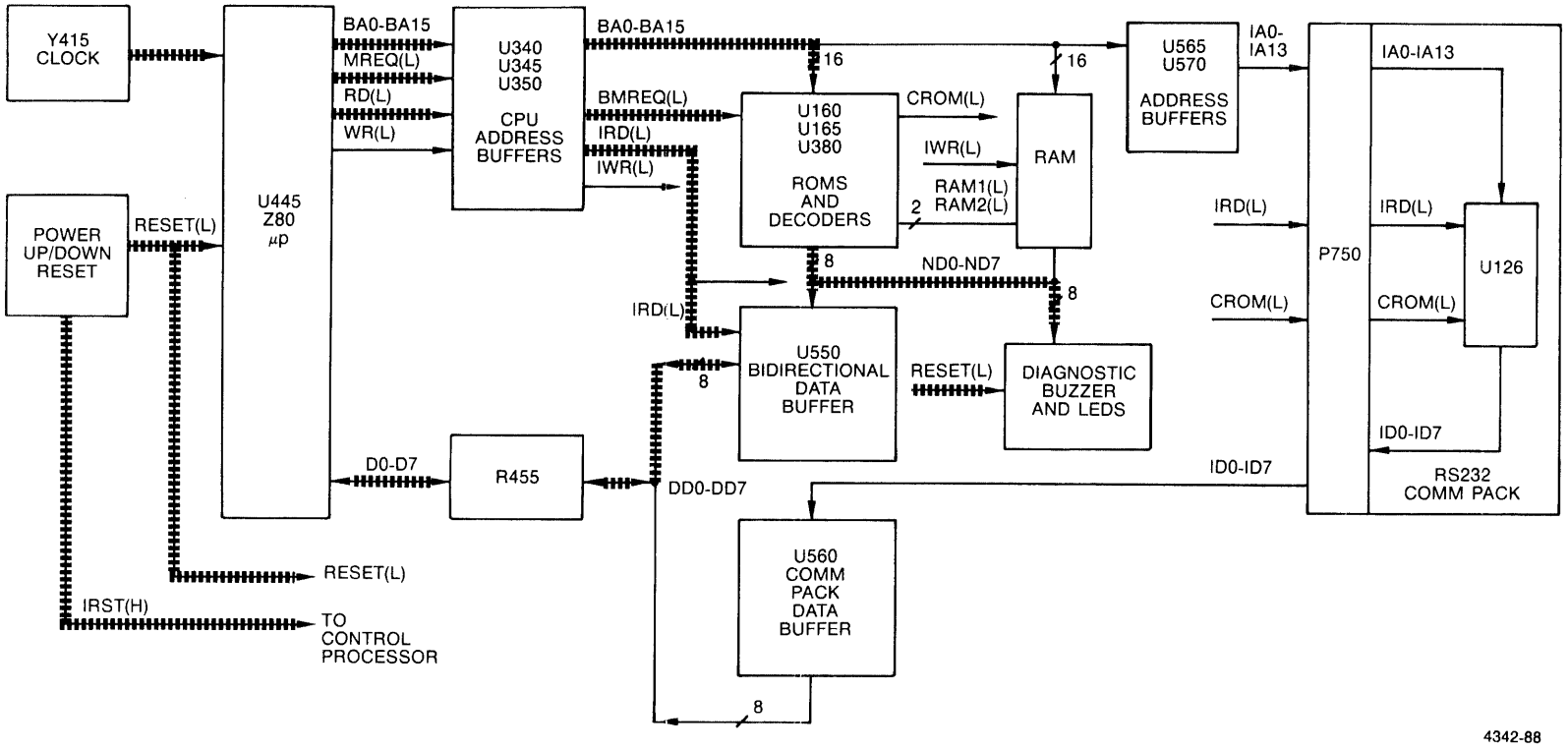


Figure 8-19. I/O Processor Kernel Stage 0 block diagram.

I/O PROCESSOR BOARD – COMPONENT LOCATION

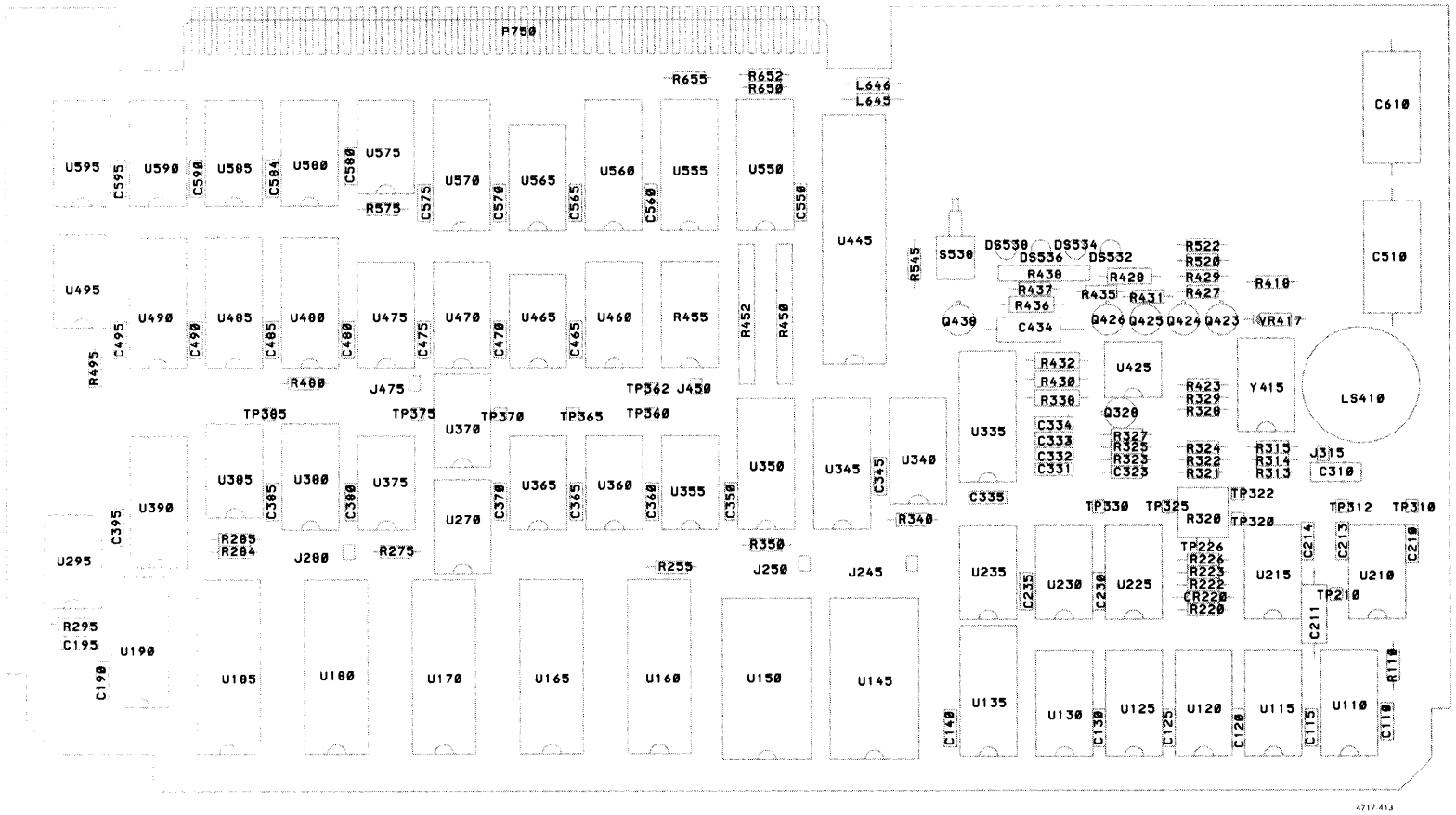


Figure 8-20. I/O Processor Board component location.

I/OP KERNEL

KERNEL AREA – CIRCUIT OVERVIEW

The I/O Processor kernel circuitry is indicated by the shaded path on the block diagram. (The shading indicates circuitry exercised for the first time during diagnostic testing.) This circuitry is comprised of a Z80 microprocessor and the associated ROM and RAM circuitry, plus the diagnostic LEDs and their latch. The microprocessor addresses the RAM through buffers A10U350, U345, and U340, and decoders A10U380 and U130. The microprocessor addresses the ROM through the same buffers and decoder A10U380. The microprocessor reads from the RAM and the ROM via bidirectional buffer A10U550.

KERNEL AREA – TEST DESCRIPTION

The I/O Processor Board has four LEDs that are used for fault analysis in the event of a kernel failure. If the kernel should fail at any point in the initial diagnostics, the LEDs will indicate at what stage the fault occurred. The following table summarizes the LED error conditions. For more specific information, refer to the error index descriptions later in this section.

I/O PROCESSOR KERNEL LED ERROR SUMMARY

LED STATUS	PROBABLE CAUSE
0000	No instrument power-up. Bad power supply. Reset circuit, LED latch A10U335, or decoder U365.
1111	Kernel failure. Unable to execute diagnostics. Bad processor A10U445, or bad ROM A10U160.
1110	Began executing diagnostics code, but could not get to RAM tests. Bad ROM A10U160.
1101	Entered RAM test, but did not finish. Bad ROM A10U160.
11F1	RAM test failed. The 1240 is looping on a bad address. Bad RAM A10U150.
11FF	RAM test failed. The 1240 is looping on a bad address. Bad RAM A10U145.
1011	Began complementary byte test on ROM A10U160, but did not finish. Bad ROM A10U160.
1F11	ROM A10U160 failed complementary byte test. Bad ROM A10U160.
1010	Began checksum test on ROM A10U160, but did not finish. Bad ROM A10U160.
1F1F	ROM A10U160 failed checksum test. Bad ROM A10U160.
1001	Began complementary byte test on ROM A10U165, but did not finish. Bad ROM A10U160.

LED STATUS	PROBABLE CAUSE
1FF1	ROM A10U165 failed complementary byte test. Bad ROM A10U165.
1000	Began checksum test on ROM A10U165, but did not finish. Bad ROM A10U160.
1FFF	ROM A10U165 failed checksum test. Bad ROM A10U165.
F000	COMM pack ROM failed checksum test. Bad COMM pack ROM.
FFFF	All LEDs are flashing in a circular (rotating) pattern. This indicates a failure in communication between the I/O Processor and the Control Processor. Suspect A10U485, U580, U585, U590, and U595.

(0 = off, 1 = on, F = flashing)

	MSB			LSB
LED Position	o	o	o	o
LED Number	A10DS538	536	534	532

Initially the instrument has no power applied (0000). When the instrument power is turned on, the LEDs are also turned on (1111). The Z80 microprocessor is vectored to ROM A10U160 (1110). The display registers A11U280 and U285 are initialized, the display screen is cleared, and the message DIAGNOSTICS IN PROGRESS is printed on the screen.

The RAM test is entered (1101). If the RAM test detects a failure, it loops on the failed address (11F1 or 11FF). If no error is detected, the ROM complementary byte test is entered (1011). If the complementary byte test detects a failure, it exits to an error routine (1F11). If the ROM complementary byte test passes, the ROM checksum test is entered (1010).

If the checksum test detects a failure, the LEDs display (1F1F). If no failure is detected, the complementary byte test for ROM A10U165 is entered (1001). If the complementary byte test detects a failure, it exits to a failure routine (1FF1). If the complementary byte check for A10U165 passes, the ROM checksum test is entered (1000). If the ROM checksum test detects a failure, it exits to an error routine (1FFF).

If the ROM checksum test passes, the I/O Processor attempts communication with the Control Processor. If a failure occurs during this attempt, the LEDs are set to a circular (rotating) pattern (FFFF). If all of the tests have been successfully completed and communication with the Control Processor is achieved, the LEDs begin indicating the operating modes of the 1240.

0000
1111

KERNEL AREA – POWER-UP ROUTINE DESCRIPTION

Power-up resets the Z80 microprocessor and the LED/Buzzer Latch A10U335 to initial conditions. The microprocessor is vectored to address 0000_{hex} of the diagnostic ROM (A10U160). The display registers A11U280 and U285 are initialized and the display is cleared. The message DIAGNOSTICS IN PROGRESS is printed on the display screen.

0000 LED Error Index (with no screen display).

Explanation: All LEDs should be reset ON at power-up, but a problem prevents the LEDs from being lighted.

Probable Cause	Action
No power to the 1240.	Check the power source and the main fuse.
Power supply failure.	Check all power supply voltages.
LED failure.	Check all LEDs with an ohmmeter.
LED latch failure.	Suspect A10U335.
Decoder failure.	Suspect A10U120 and U380.
RESET line defective.	Check RESET line by pressing the RESET switch, A10S538, and observing pin 26 of U445.

1111 LED Error Index

Explanation: All LEDs will be reset ON when the 1240 is powered up, or when the manual reset is pressed. If this test is not completed, the LEDs will remain on.

Probable Cause	Action
Kernel failure.	Move NOP jumper A10J450 to the TEST position (pin 2 to 3). Remove the resistor pack A10R455 and buzzer disable jumper A10J315. Check the Z80 microprocessor address, data, and control lines with a signature analyzer and verify values listed in *Kernel Signature Analysis*.
Wrong data in ROM or diagnostic ROM failure.	Suspect diagnostic ROM, A10U160.
Bad data buffer.	Suspect U550.
Bad address decoder.	Suspect U380.

1110 LED Error Index

Explanation: The LED DS532 will be turned off when the diagnostics ROM is entered. The code that follows this action will initialize the display registers A11U280 and U285, clear the screen, and print DIAGNOSTICS IN PROGRESS on the screen.

Probable Cause	Action
Kernel failure.	Move NOP jumper A10J450 to the TEST position (pin 2 to 3). Remove the resistor pack A10R455 and buzzer disable jumper A10J315. Check the Z80 microprocessor address, data, and control lines with a logic analyzer or signature analyzer and verify values listed in *Kernel Signature Analysis*.
Diagnostic ROM failure.	Suspect the diagnostic ROM A10U160.

I/O PROCESSOR KERNEL BLOCK DIAGRAM
RAM – STAGE 1

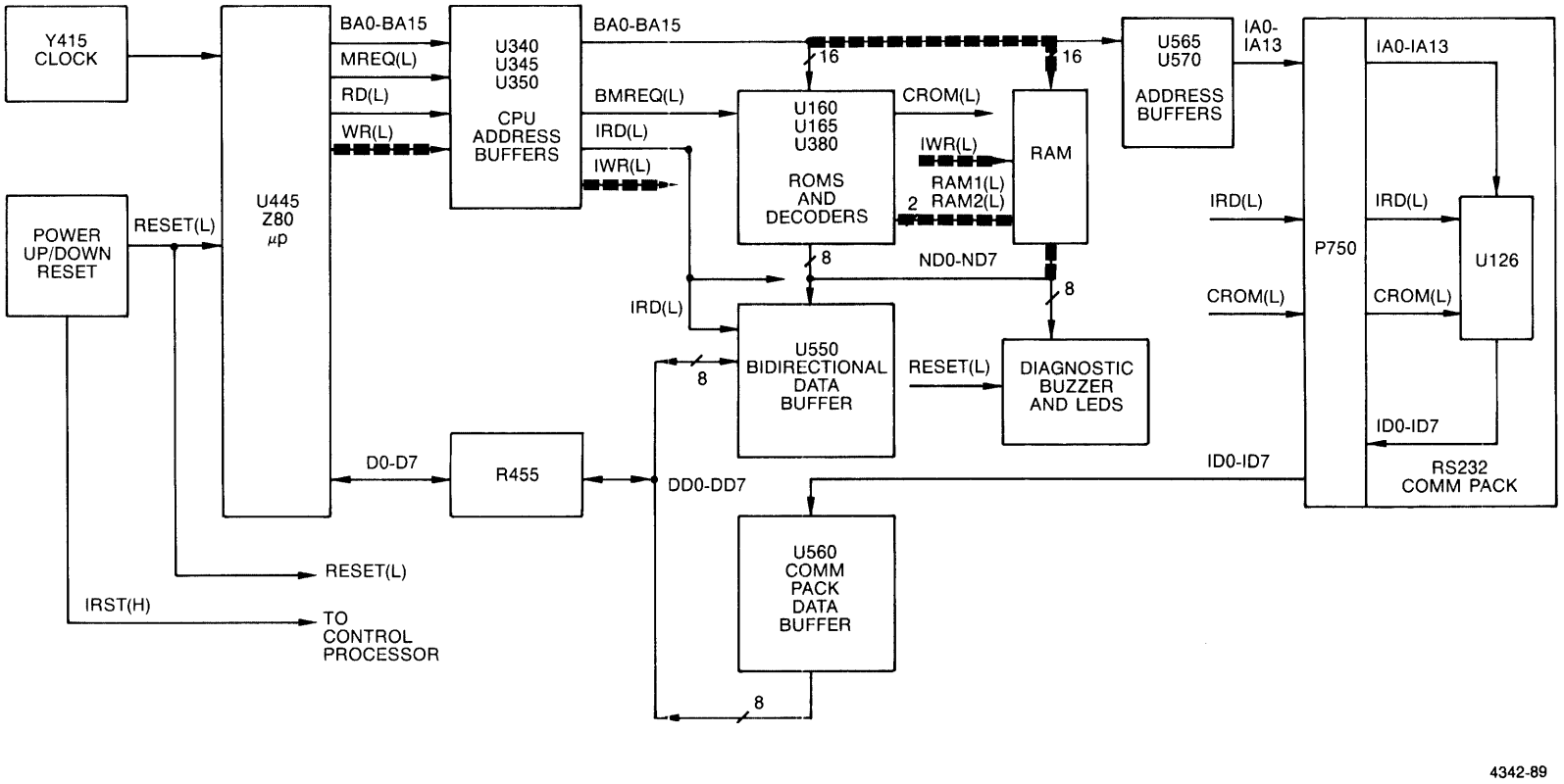


Figure 8-21. I/O Processor Kernel Stage 1 block diagram.

KERNEL AREA – RAM ROUTINE DESCRIPTION

The first RAM routine tests the 2K ($B000_{hex}$-$B7FF_{hex}$) of A10U150.

1101 LED Error Index

Explanation: The LED DS534 will be turned off after the message DIAGNOSTICS IN PROGRESS is written to the screen and the RAM test is entered.

Probable Cause	Action
RAM Test failed to run or finish.	Suspect the diagnostic ROM, A10U160.
Kernel failure.	Move NOP jumper A10J450 to the TEST position (pin 2 to 3). Remove the resistor pack A10R455 and buzzer disable jumper A10J315. Check the Z80 microprocessor address, data, and control lines with a logic analyzer or signature analyzer and verify values listed in *Kernel Signature Analysis*.
Bad address decoder.	Suspect A10U380.

11F1 LED Error Index
11FF LED Error Index

Explanation: This test checks both RAMs A10U150 and U145 for independence of all address and data lines, as well as the ability to set and clear each bit within the RAMs. The appropriate LED error index indicates the failed RAM. LED A10DS534 flashes for a failure in RAM A10U150, however both A10DS534 and DS532 flash for a failure in RAM A10U145.

First, all locations in both RAMs are filled with AA_{hex}, then the first location is checked for that AA_{hex} value. If the value is present, it is replaced with CC_{hex} and successive locations are checked and changed until the end of memory. When the RAMs are filled with the CC_{hex} value, the check and replace process is repeated using $F0_{hex}$ as the replacement value. When the check and replace process is complete, each RAM memory location is again checked for the $F0_{hex}$ value.

Probable Cause	Action
Error Index 11F1: Bad RAM A10U150.	Suspect RAM A10U150.
Error Index 11FF: Bad RAM A10U145.	Suspect RAM A10U145.

1011
1F11
1010
1F1F

KERNEL AREA – ROM ROUTINE DESCRIPTION

The kernel ROM routine tests for complementary bytes and a correct checksum in the diagnostic ROM, A10U160.

1011 LED Error Index

Explanation: The complementary byte test for ROM A10U160 began, but did not finish.

Probable Cause	Action
Diagnostic ROM failure.	Suspect the diagnostic ROM, A10U160.

1F11 LED Error Index

Explanation: ROM A10U160 failed the complementary byte test. This test checks the bytes at $1FFC_{hex}$ and $1FFD_{hex}$ to see if they are complementary.

Probable Cause	Action
Diagnostic ROM failure.	Suspect the diagnostic ROM, A10U160.

1010 LED Error Index

Explanation: The ROM checksum test for ROM A10U160 began, but did not finish.

Probable Cause	Action
Diagnostic ROM failure.	Suspect the diagnostic ROM, A10U160.

1F1F LED Error Index

Explanation: ROM A10U160 failed the ROM checksum test.

Probable Cause	Action
Diagnostic ROM failure.	Suspect diagnostic ROM, A10U160.

1001 LED Error Index

Explanation: A complementary byte test on ROM A10U165 began, but did not finish.

Probable Cause	Action
Bad ROM A10U160.	Suspect A10U160.

1FF1 LED Error Index

Explanation: ROM A10U165 failed the complementary byte test.

Probable Cause	Action
Bad ROM A10U165.	Suspect A10U165.

1000 LED Error Index

Explanation: A checksum test on ROM A10U165 began, but did not finish.

Probable Cause	Action
Bad ROM A10U160.	Suspect ROM A10U160.

1FFF LED Error Index

Explanation: ROM A10U165 failed the checksum test.

Probable Cause	Action
Bad ROM A10U165.	Suspect ROM A10U165.

I/O PROCESSOR KERNEL BLOCK DIAGRAM
COMM PACK – STAGE 2

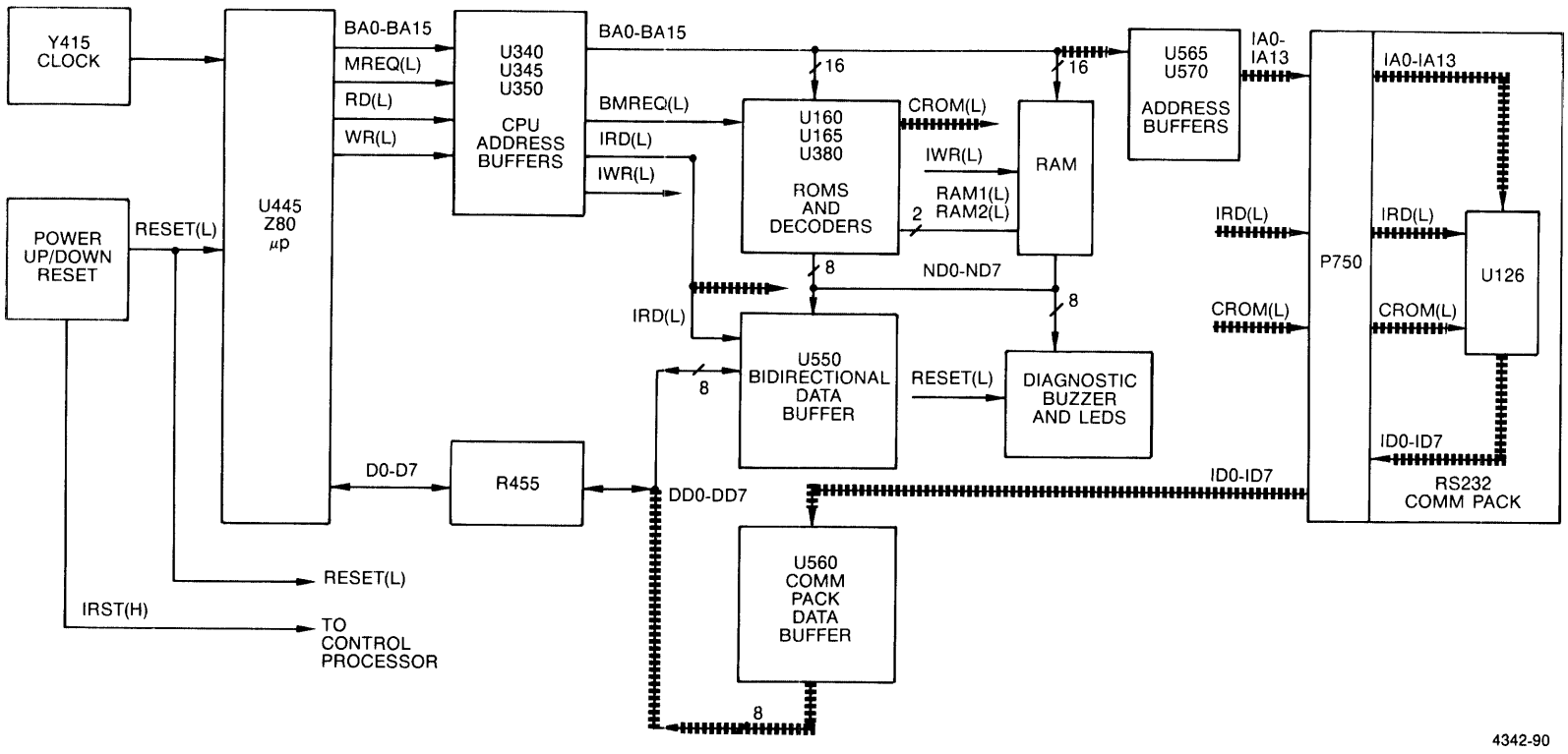


Figure 8-22. I/O Processor Kernel Stage 2 block diagram.

KERNEL AREA – COMM PACK ROUTINE DESCRIPTION

The COMM pack routine tests for a correct ROM checksum in the installed COMM pack (GPIB: A32U245, RS232: A32U126). The COMM pack is not a normal part of the normal processor kernel circuitry. However, it is checked because proper operation is necessary for diagnostic testing.

F000 LED Error Index

Explanation: A checksum test on COMM pack ROM began, but the test failed.

Probable Cause	Action
Bad COMM pack ROM.	Suspect COMM pack ROM (GPIB: A32U245, RS232: A31U126).

FFFF LED Error Index

Explanation: After completing the kernel diagnostics, the I/O Processor attempted to communicate with the Control Processor, but the attempt was unsuccessful. The LEDs are then set to a circular (rotating) pattern to indicate this failure condition.

Probable Cause	Action
Control Processor kernel failure.	Check the LEDs on the Control Processor Board for the rotating LED pattern. If LEDs indicate a problem other than the kernel, repair the problem and repeat the tests.
Inter-processor communication queue failure.	If the LEDs on the Control Processor Board are also in a rotating pattern, suspect the inter-processor communication queue consisting of A10U485, U580, U585, U590, and U595.

CONTROL PROCESSOR KERNEL LED ERROR INDEXES

LED Status	Test Name	Stage Number
000000 111111 111100 1111FF 111011 111F11	Power-Up and ROM	Stage 0
111110 10XXXX 01XXXX 111101 1111F1	RAM	Stage 1
111010 111F1F 111001 111FF1 111000 111FFF 110111 11F111 110110 11F11F 110101 11F1F1 110100 11F1FF 110011 11FF11 FFFFFF	ROM Pack	Stage 2

(0 = OFF, 1 = ON, F = flashing, X = special case)

	MSB					LSB
LED Position	o	o	o	o	o	o
LED Number	A9DS422	421	324	323	322	321

CONTROL PROCESSOR KERNEL BLOCK DIAGRAM
POWER-UP AND ROM – STAGE 0

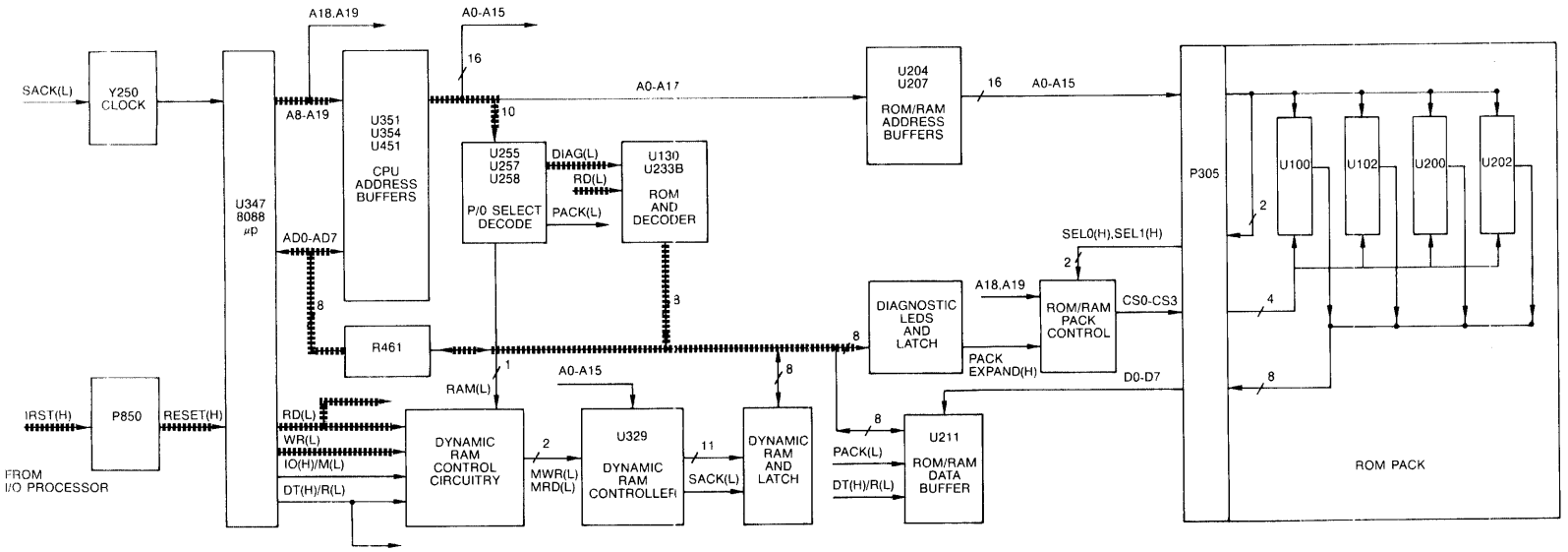


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Figure 8-23. Control Processor Kernel Stage 0 block diagram.

CONTROL PROCESSOR BOARD – COMPONENT LOCATION

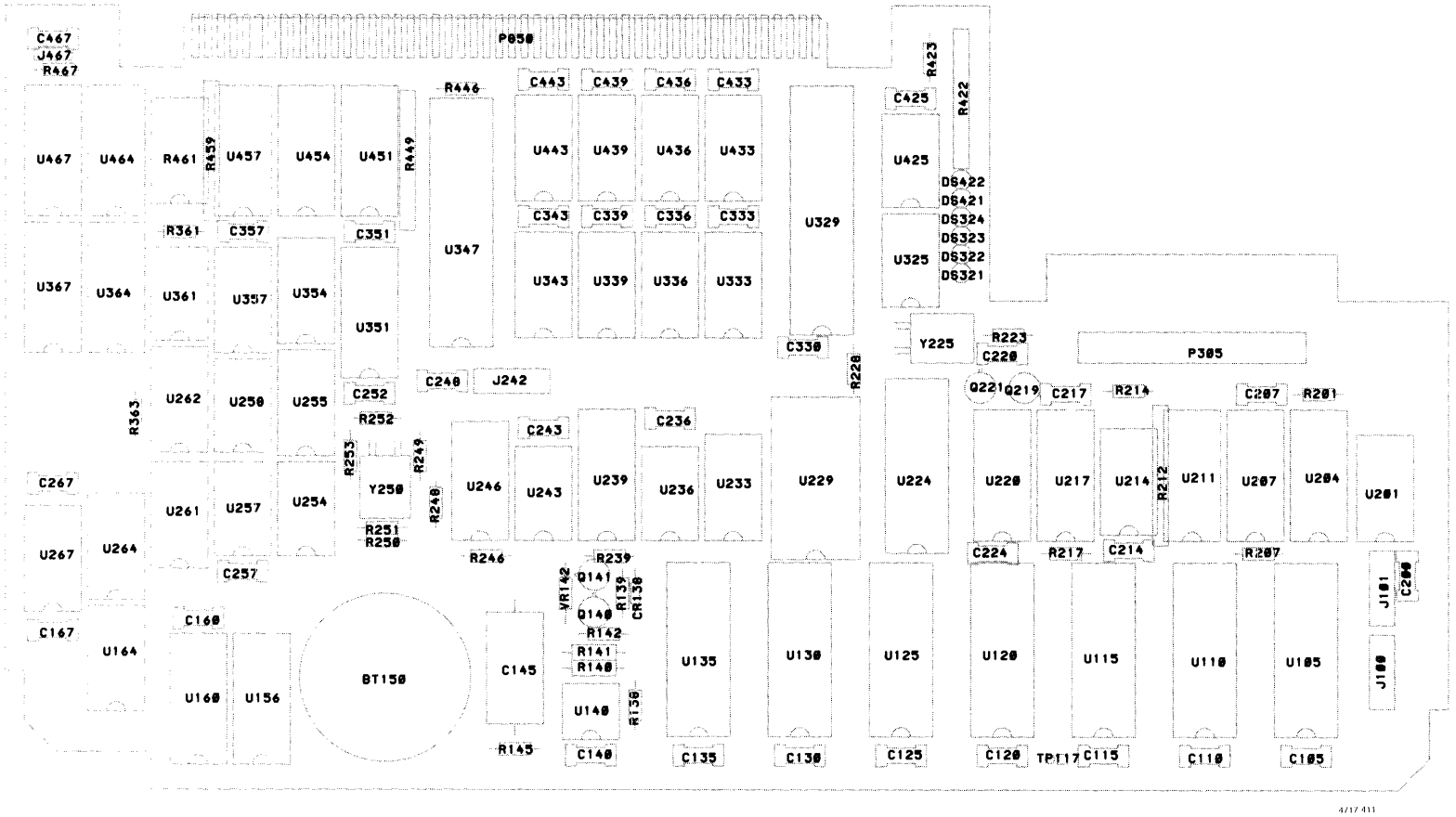

Figure 8-24. Control Processor Board component location.

CONP KERNEL

KERNEL AREA – CIRCUIT OVERVIEW

The pattern-shaded signal lines on the Control Processor kernel block diagram indicate circuitry used during diagnostic testing. Only the circuitry that is being exercised for the first time during diagnostic testing is shown. Circuitry exercised by other diagnostic tests are shown in their respective block diagrams.

The kernel circuitry is comprised of an 8088 microprocessor and associated ROM and dynamic RAM circuitry, plus the diagnostic LEDs and their latch. The microprocessor addresses the ROM and RAM through address buffers A9U351, U354, and U451. The 8088 uses some advance memory decoding circuitry and a dynamic RAM controller, A9U329, to access RAM space. Readback of RAM data is done through the latch A9U239. The diagnostic LED latch, A9U220, and associated LEDs are controlled through decoder A9U262.

KERNEL AREA – TEST DESCRIPTION

The Control Processor board has six LEDs that are used for fault analysis in the event of a kernel failure. If the kernel should fail at any point in the initial diagnostics, the LEDs indicate the stage where the fault occurred. The following table summarizes the LED error conditions. For more specific information, refer to the error index descriptions later in this section.

CONTROL PROCESSOR KERNEL LED ERROR SUMMARY

LED STATUS	PROBABLE CAUSE
000000	No instrument power-up. Suspect power supply. Check the reset circuit, the LED latch A10U220, or decoders A9U357 and U262.
111111	Kernel failure. Unable to execute diagnostics. Suspect processor A10U347 or diagnostic ROM A9U135.
111110	Began RAM data-bit-independence test, but could not finish. Suspect diagnostic ROM A9U135.
10XXXX	Suspect RAM or RAM controller A9U329. Refer to specific error index.
01XXXX	Suspect RAM or RAM controller A9U329. Refer to specific error index.
111101	Began RAM address-bit-independence test, but could not finish. Suspect diagnostic ROM A9U135.
1111F1	Suspect RAM or RAM controller failure. Refer to additional error index information.
111100	Began ROM complementary byte test, but did not finish. Suspect ROM A9U135.
1111FF	Detected failure in ROM complementary byte test. Suspect ROM A9U135.
111011	Began ROM checksum test, but did not finish. Suspect ROM A9U135.
111F11	Detected a failure in ROM checksum test. Suspect ROM A9U135.
111010	Began ROM pack tests, but did not finish. Suspect ROM A9U135.

LED STATUS	PROBABLE CAUSE
111F1F	Detected failure in ROM pack complementary byte tests at $11FFC_{hex}$ and $11FFD_{hex}$. Suspect ROM A42U100 in the diagnostic ROM pack.
111001	Began ROM pack tests, but did not finish. Suspect ROM A9U135.
111FF1	Detected failure in ROM pack complementary byte tests at $13FFC_{hex}$ and $13FFD_{hex}$. Suspect ROM A42U102 in the diagnostic ROM pack.
111000	Began ROM pack tests, but did not finish. Suspect ROM A9U135.
111FFF	Detected failure in ROM pack complementary byte tests at $15FFC_{hex}$ and $15FFD_{hex}$. Suspect ROM A42U200 in the diagnostic ROM pack.
110111	Began ROM pack test, but did not finish. Suspect ROM A9U135.
11F111	Detected failure in ROM pack complementary byte tests at $17FFC_{hex}$ and $17FFD_{hex}$. Suspect ROM A42U202 in the diagnostic ROM pack.
110110	Began ROM pack test, but did not finish. Suspect ROM A9U135.
11F11F	Detected failure in ROM pack checksum tests at $11FFE_{hex}$ and $11FFF_{hex}$. Suspect ROM A42U100 in the diagnostic ROM pack.
110101	Began ROM pack test, but did not finish. Suspect ROM A9U135.
11F1F1	Detected failure in ROM pack checksum tests at $13FFE_{hex}$ and $13FFF_{hex}$. Suspect ROM A42U102 in the diagnostic ROM pack.
110100	Began ROM pack test, but did not finish. Suspect ROM A9U135.
11F1FF	Detected failure in ROM pack checksum tests at $15FFE_{hex}$ and $15FFF_{hex}$. Suspect ROM A42U200 in the diagnostic ROM pack.
110011	Began ROM pack test, but did not finish. Suspect ROM A9U135.
11FF11	Detected failure in ROM pack checksum tests at $17FFE_{hex}$ and $17FFF_{hex}$. Suspect ROM A42U202 in the diagnostic ROM pack.
FFFFFF	All LEDs are flashing in a circular (rotating) pattern. This indicates a communication failure between the Control Processor and the I/O Processor. Suspect A10U485, U580, U585, U590, and U595.

(0 = off, 1 = on, F = flashing, X = special case)

	MSB					LSB
LED Position	o	o	o	o	o	o
LED Number	A9DS422	421	324	323	322	321

000000

Initially, the instrument has no power applied (000000). When the instrument power is turned on, all LEDs are also turned on (111111). The 8088 microprocessor is vectored to the diagnostic ROM A9U135 and the RAM data-bit-independence test is entered (111110). If a failure is detected, the error indexes (10XXXX or 01XXXX) indicate the failed bits according to a table found in the error index descriptions. If no errors are detected, the RAM address-bit-independence test is entered (111101). If a failure is detected, the LEDs display (1111F1).

If the test passes, the ROM complementary byte test is entered (111100). If a failure is detected, the LEDs display (1111FF). If the test passes, the ROM checksum test is entered (111011). If a failure is detected, the LEDs display (111F11). If the test passes, the ROM pack complementary byte test is entered (111010). If a failure is detected at addresses 11FFC$_{hex}$ and 11FFD$_{hex}$, the LEDs display (111F1F). If the test passes, complementary byte tests are run for addresses 13FFC$_{hex}$ and 13FFD$_{hex}$ (111001 when test passes or 111FFF1 for failures). When these tests are successfully completed addresses 15FFC$_{hex}$ and 15FFD$_{hex}$ are checked; producing the 111000 error index when the test passes, or 111FFF when it fails. Finally addresses 17FFC$_{hex}$ and 17FFD$_{hex}$ are checked; producing the 110111 error index when the test passes, or 11F111 when it fails.

Next, the ROM pack checksum tests are run for addresses 11FFE$_{hex}$ and 11FFF$_{hex}$; producing the 110110 error index when it passes or 11F11F when it fails. Additional ROM pack checksum tests produce LED error indexes for addresses 13FFE$_{hex}$ and 13FFF$_{hex}$ (110101 passing or 11F1F1 for failures), addresses 15FFE$_{hex}$ and 15FFF$_{hex}$ (110100 passing or 11F1FF for failures), and addresses 17FFE$_{hex}$ and 17FFF$_{hex}$ (110011 passing or 11FF11 for failures).

If the ROM pack checksum tests pass, the Control Processor attempts communication with the I/O Processor. If a failure occurs during this attempt, the LEDs are set to a rotating pattern (FFFFFF). If all of the tests have been successfully completed and communication with the I/O Processor is achieved, the LEDs begin indicating the operating modes of the 1240.

KERNEL AREA – POWER-UP ROUTINE DESCRIPTION

The kernel power-up routine resets the 8088 microprocessor and the LED Latch A9U220. The microprocessor begins executing code out of the diagnostic ROM (A9U135).

000000 LED Error Index

Explanation: All LEDs should be reset ON at power-up, but a problem prevents the LEDs from being lighted.

Probable Cause	Action
No power to the 1240.	Check the power source and the main fuse.
Power supply failure.	Check all power supply voltages.
LED failure.	Check all LEDs with an ohmmeter.
LED latch failure.	Suspect A9U220.
Address decoder failure.	Suspect A9U357 or U262.
RESET line defective.	Check RESET line by pressing the RESET switch, A10S538, and observing pin 21 of A9U347.

111111 LED Error Index

Explanation: All LEDs will be reset ON when the 1240 is powered up, or when the manual reset switch A10S538 is pressed. If this test is not completed, the LEDs will remain on.

Probable Cause	Action
Kernel failure.	Move NOP jumper A9J467 to the TEST position (pin 2 to 3). Remove the resistor pack A9R461. Check the 8088 microprocessor address, data, and control lines with a signature analyzer and verify values listed in *Kernel Signature Analysis*.
Wrong data in diagnostic ROM.	Suspect diagnostic ROM A9U135.

CONTROL PROCESSOR KERNEL BLOCK DIAGRAM
RAM – STAGE 1

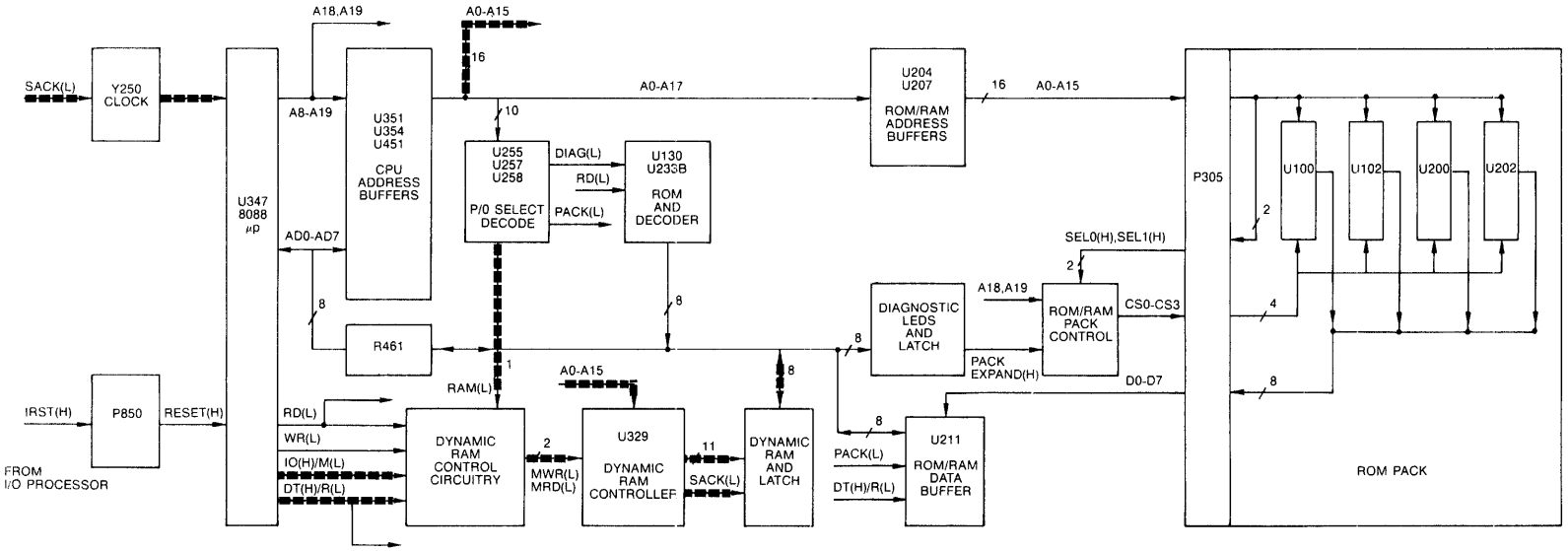

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Figure 8-25. Control Processor Kernel Stage 1 block diagram.

KERNEL AREA – RAM ROUTINE DESCRIPTION

111110
10XXXX
01XXXX

The RAM routine tests addresses 20000_{hex}-$2F7FF_{hex}$ of RAM.

111110 LED Error Index

Explanation: The LED DS321 is turned off after the RAM data-bit-independence test is entered.

Probable Cause	Action
RAM test failed to run or finish.	Suspect the diagnostic ROM A9U135.
Kernel failure.	Move NOP jumper A9J467 to the TEST position (pin 2 to 3). Remove the resistor pack A9R461. Check the 8088 microprocessor address, data, and control lines with a signature analyzer and verify values listed in *Kernel Signature Analysis.*

10XXXX LED Error Indexes
01XXXX LED Error Indexes

Explanation: These LED error indexes report failures by using the lower four LEDs A9DS324-DS321 to indicate the failed data bit position. The upper two LEDs, A9DS422 and DS421, distinguish between the upper four-bit bank (10XXXX for D4-D7) of data bits and a lower four-bit bank (01XXXX for D0-D3) of data bits. If none of the lower four LEDs are on, no failures were detected during the tests. For specific bit failure information, refer to the following table.

These tests check to see that each of the eight bits in a byte of RAM are independent of one another. First, the value 00_{hex} is written to RAM addresses 20000_{hex}-$22FFF_{hex}$, then address $22FFF_{hex}$ is checked to see that each of the eight bits can be individually set and cleared. When the first location is verified to contain 00_{hex}, then 01_{hex} is written to it. Once the 01_{hex} value is verified, 02_{hex} is written to address $22FFF_{hex}$. This verify/change sequence is repeated for the values 04_{hex}, 08_{hex}, 10_{hex}, 20_{hex}, 40_{hex}, and 80_{hex}.

Probable Cause	Action
RAM or RAM controller A9U329 failure.	Determine bad bit using the following table.

111101
1111F1

LED Status	Bit Failures
010000	No failures in the lower four bits
010001	Bit 0 (A9U433)
010010	Bit 1 (A9U333)
010100	Bit 2 (A9U436)
011000	Bit 3 (A9U343)
100000	No failures in the upper four bits
100001	Bit 4 (A9U433)
100010	Bit 5 (A9U439)
100100	Bit 6 (A9U339)
101000	Bit 7 (A9U336)

111101 LED Error Index

Explanation: The LED DS322 is turned off after the RAM address-bit-independence test is entered.

Probable Cause	Action
RAM test failed to run or finish.	Suspect the diagnostic ROM A9U135.

1111F1 LED Error Index

Explanation: LED DS322 will flash when a RAM failure is detected during the kernel RAM routine. The test checks two areas of the Control Processor RAM (that are required for diagnostic testing) to see if each of the two areas can be individually addressed. The test also checks to see if each bit in address ranges 20000_{hex} to $22FFF_{hex}$ and $2C000_{hex}$ to $2C3FF_{hex}$ can be set to a logic high and low.

First, AA_{hex} is written to all locations under test and the first location is checked for AA_{hex}. If present, 55_{hex} is written to that address. The first location is checked for 55_{hex} and, if present, the address is incremented. This location is checked for AA_{hex} and, if present, 55_{hex} is written. This sequence continues for the remaining address locations until the end of RAM is reached. If a failure is detected, the failing address is displayed on the screen (if possible), and the processor loops on the failed address.

Probable Cause	Action
Bad RAM or RAM controller A9U329.	The test is now writing to and reading from the failed location. Use the screen address information or a logic analyzer to determine the processor looping address. If the failing address value is one that requires an address line to change for the first time, then suspect that address line to be open or shorted. If the failing address value is not one that required an address line to change for the first time, then suspect a RAM failure. Verify a RAM failure by using a logic analyzer and observing the read/write loop operation. Use the following table to determine the RAM responsible for each bit.

Data Bit	Corresponding RAM
Bit 0	A9U433
Bit 1	A9U333
Bit 2	A9U436
Bit 3	A9U343
Bit 4	A9U443
Bit 5	A9U439
Bit 6	A9U339
Bit 7	A9U336

KERNEL AREA – ROM ROUTINE DESCRIPTION

The ROM routine tests for complementary bytes and a correct checksum in the diagnostic ROM, A9U135.

111100 LED Error Index

Explanation: Both LEDs DS321 and DS322 will be turned OFF when the RAM test is completed and the ROM complementary byte test is entered.

Probable Cause	Action
Diagnostic ROM failure.	Suspect the diagnostic ROM A9U135.

1111FF LED Error Index

Explanation: Both LEDs DS321 and DS322 will flash when a complementary byte failure is detected. This test checks the bytes at address locations $FFFFC_{hex}$ and $FFFFD_{hex}$ of A9U135 to see if they are complementary.

111011
111F11

Probable Cause	Action
Diagnostic ROM failure.	Suspect the diagnostic ROM A9U135.

111011 LED Error Index

Explanation: LED DS323 is turned off when the the complementary byte test is completed and the ROM checksum test is entered. This test calculates a checksum on A9U135.

Probable Cause	Action
Diagnostic ROM failure.	Suspect the diagnostic ROM A9U135.

111F11 LED Error Index

Explanation: LED DS323 will flash when a checksum error is detected in the diagnostic ROM.

Probable Cause	Action
Diagnostic ROM failure.	Suspect the diagnostic ROM A9U135.

CONTROL PROCESSOR KERNEL BLOCK DIAGRAM
ROM PACK – STAGE 2

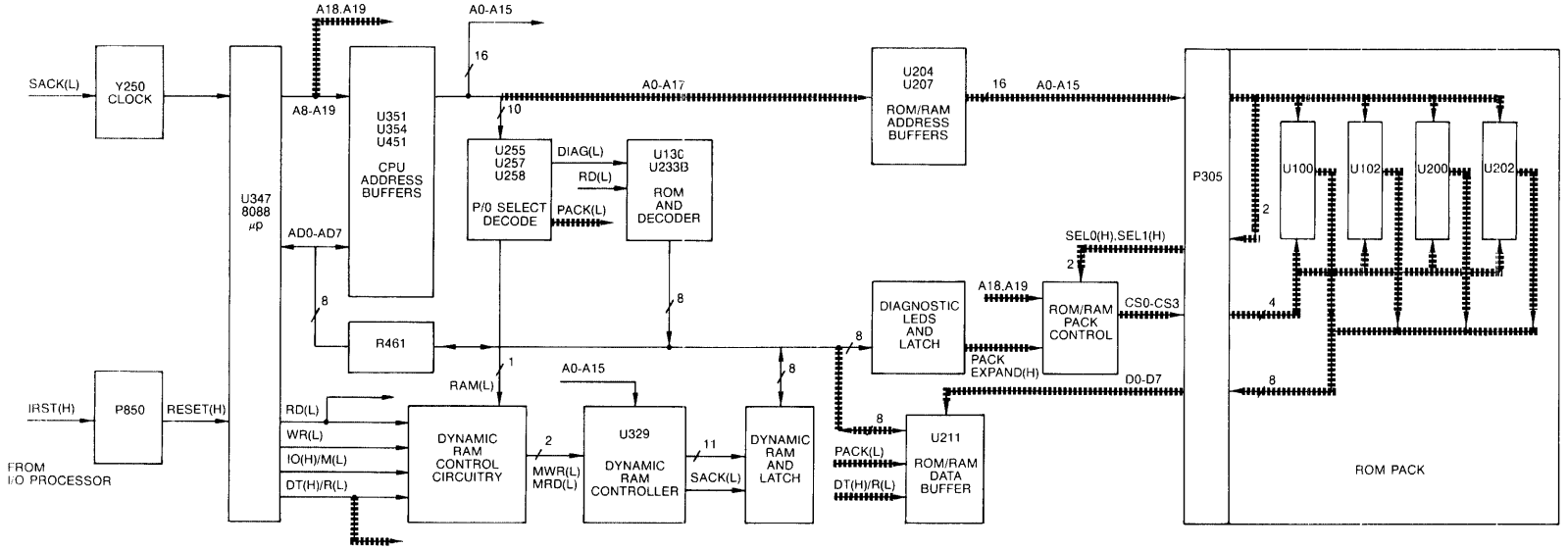

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Figure 8-26. Control Processor Kernel Stage 2 block diagram. Pages 1 through 6.

KERNEL AREA – ROM PACK ROUTINE DESCRIPTIONS

The ROM pack routines test the Diagnostic ROM pack ROMs A42U100, U102, U200, and U202 for complementary bytes and correct checksums. The Diagnostic ROM pack is not a part of the normal processor kernel circuitry, however, it is checked because proper operation is necessary for diagnostic testing.

111010 LED Error Index

Explanation: Both LEDs DS323 and DS321 are turned off when the ROM pack complementary byte test is entered.

Probable Cause	Action
Diagnostic ROM failure.	Suspect the diagnostic ROM, A9U135.

111F1F LED Error Index

Explanation: Both LEDs DS323 and DS321 will flash when a ROM pack complementary byte failure is detected. This test checks the bytes at $11FFC_{hex}$ and $11FFD_{hex}$ of A42U100 to see if they are complementary.

Probable Cause	Action
ROM pack ROM failure.	Suspect ROM A42U100.

111001 LED Error Index

Explanation: Both LEDs DS323 and DS321 are turned off as the ROM pack complementary byte test continues.

Probable Cause	Action
Diagnostic ROM failure.	Suspect the diagnostic ROM, A9U135.

111FF1 LED Error Index

Explanation: Both LEDs DS323 and DS322 will flash when a ROM pack complementary byte failure is detected. This test checks the bytes at $13FFC_{hex}$ and $13FFD_{hex}$ of A42U102 to see if they are complementary.

111000
111FFF
110111
11F111

Probable Cause	Action
ROM pack ROM failure.	Suspect ROM A42U102.

111000 LED Error Index

Explanation: LEDs DS323, DS322, and DS321 are turned off as the ROM pack complementary byte test continues.

Probable Cause	Action
Diagnostic ROM failure.	Suspect the diagnostic ROM A9U135.

111FFF LED Error Index

Explanation: LEDs DS323, DS322, and DS321 will flash when a ROM pack complementary byte failure is detected. This test checks the bytes at $15FFC_{hex}$ and $15FFD_{hex}$ of A42U200 to see if they are complementary.

Probable Cause	Action
ROM pack ROM failure.	Suspect ROM A42U200.

110111 LED Error Index

Explanation: LED DS324 is turned off as the ROM pack complementary byte test continues.

Probable Cause	Action
Diagnostic ROM failure.	Suspect the diagnostic ROM A9U135.

11F111 LED Error Index

Explanation: LED DS324 will flash when a ROM pack complementary byte failure is detected. This test checks the bytes at $17FFC_{hex}$ and $17FFD_{hex}$ of A42U202 to see if they are complementary.

Probable Cause	Action
ROM pack ROM failure.	Suspect ROM A42U202.

110110 LED Error Index

Explanation: Both LEDs DS324 and DS321 are turned off as the ROM pack checksum tests are entered.

Probable Cause	Action
Diagnostic ROM failure.	Suspect the diagnostic ROM A9U135.

11F11F LED Error Index

Explanation: Both LEDs DS324 and DS321 will flash when a ROM pack checksum failure is detected. This test calculates the checksum for ROM A42U100 and compares the result to the expected value stored at addresses $11FFE_{hex}$ and $11FFF_{hex}$ in the same ROM.

Probable Cause	Action
ROM pack ROM failure.	Suspect ROM A42U100.

110101 LED Error Index

Explanation: Both LEDs DS324 and DS322 are turned off as the ROM pack checksum tests continue.

Probable Cause	Action
Diagnostic ROM failure.	Suspect the diagnostic ROM A9U135.

11F1F1 LED Error Index

Explanation: Both LEDs DS324 and DS322 will flash when a ROM pack checksum failure is detected. This test calculates the checksum for ROM A42U102 and compares the result to the expected value stored at addresses $13FFE_{hex}$ and $13FFF_{hex}$ in the same ROM.

Probable Cause	Action
ROM pack ROM failure.	Suspect ROM A42U102.

110100
11F1FF
110011
11FF11

110100 LED Error Index

Explanation: LEDs DS324, DS322, and DS321 are turned off as the ROM pack checksum tests continue.

Probable Cause	Action
Diagnostic ROM failure.	Suspect the diagnostic ROM A9U135.

11F1FF LED Error Index

Explanation: LEDs DS324, DS322, and DS321 will flash when a ROM pack checksum failure is detected. This test calculates the checksum for ROM A42U200 and compares the result to the expected value stored at addresses $15FFE_{hex}$ and $15FFF_{hex}$ in the same ROM.

Probable Cause	Action
ROM pack ROM failure.	Suspect ROM A42U200.

110011 LED Error Index

Explanation: Both LEDs DS324 and DS323 are turned off as the ROM pack checksum tests continue.

Probable Cause	Action
Diagnostic ROM failure.	Suspect the diagnostic ROM A9U135.

11FF11 LED Error Index

Explanation: Both LEDs DS324 and DS323 will flash when a ROM pack checksum failure is detected. This test calculates the checksum for ROM A42U202 and compares the result to the expected value stored at addresses $17FFE_{hex}$ and $17FFF_{hex}$ in the same ROM.

Probable Cause	Action
ROM pack ROM failure.	Suspect ROM A42U202.

FFFFFF LED Error Index

Explanation: After completing the kernel diagnostics, the Control Processor attempted unsuccessfully to communicate with the I/O Processor. The LEDs are then set to a circular (rotating) pattern to indicate this failure condition.

Probable Cause	Action
I/O Processor kernel failure.	Check the LEDs on the I/O Processor Board for the rotating LED pattern. If LEDs indicate a problem other than the kernel, repair the problem and repeat the tests.
Inter-processor communication queue failure.	If the LEDs on the I/O Processor Board are also in a swirling pattern, suspect the inter-processor communication queue consisting of A10U485, U580, U585, U590, and U595.

1XXX I/O PROCESSOR ERROR INDEXES

Error Index	Area Name	Area Number
11XX	EPROM COMP	AREA 1
12XX	EPROM CSUM	AREA 2
13XX	EPROM PAGE	AREA 3
14XX	RAM	AREA 4
15XX	INTERRUPT	AREA 5
16XX	DWINDOW	AREA 6
17XX	SKEYREG	AREA 7

I/O PROCESSOR BLOCK DIAGRAM
EPROM COMP – AREA 1

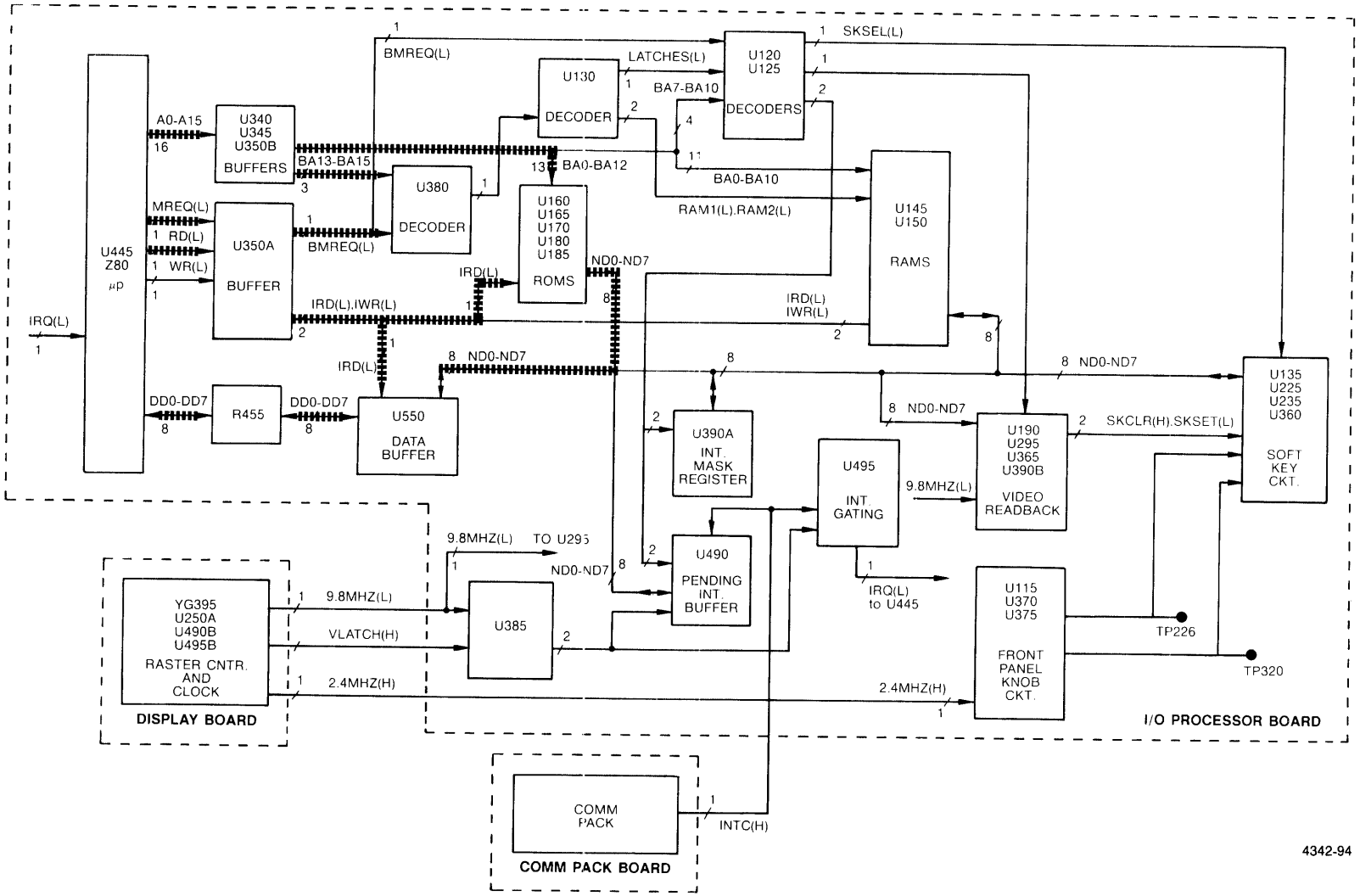


Figure 8-27. I/O Processor EPROM COMP block diagram.

I/O PROCESSOR BOARD – COMPONENT LOCATION

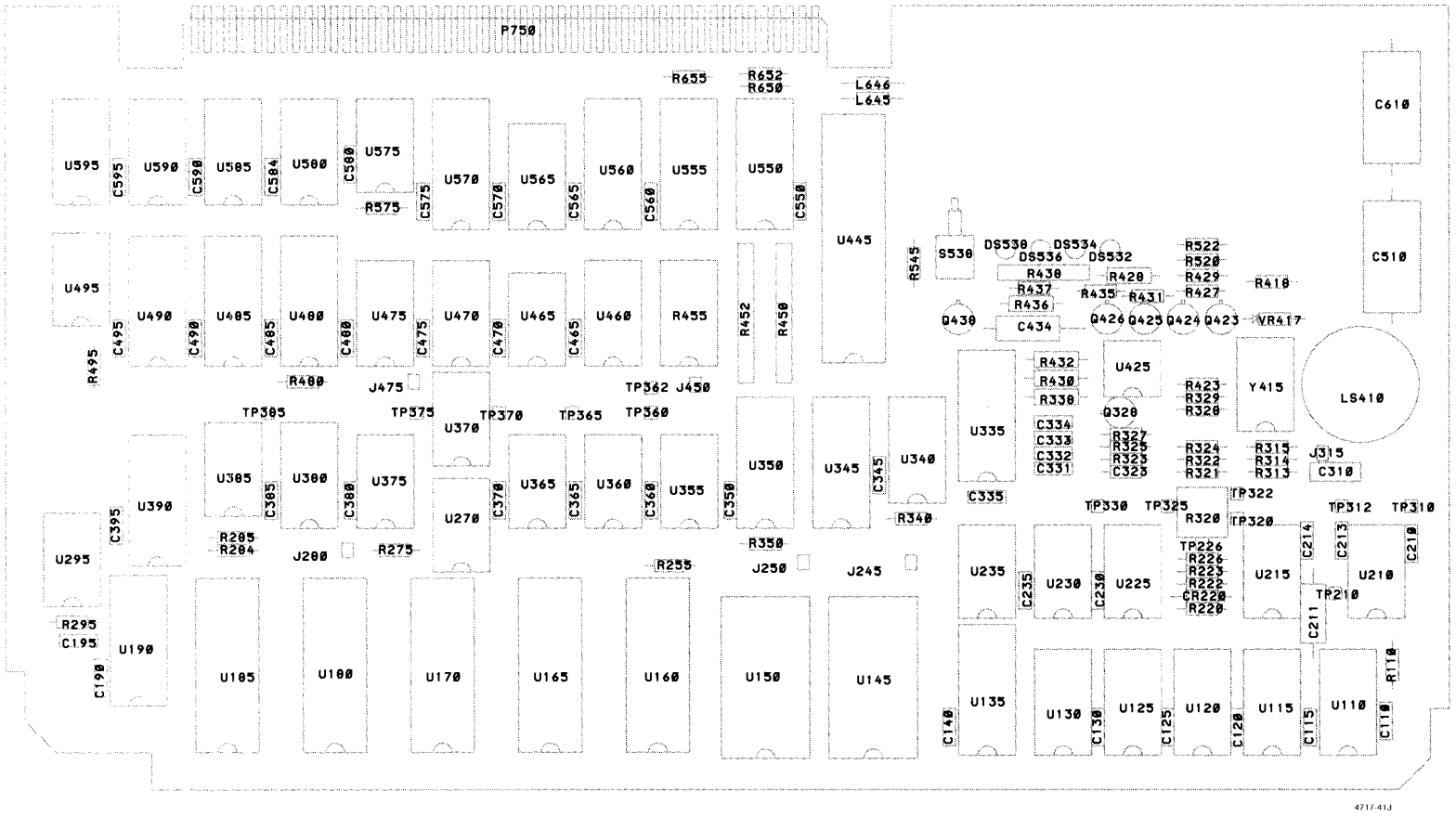


Figure 8-28. I/O Processor Board component location.

module: I/O
area: EPROM COMP

EPROM COMP AREA – CIRCUIT OVERVIEW

The circuitry that is exercised by the EPROM COMP complementary byte test is indicated by the shaded path on the block diagram. (The shading indicates circuitry exercised for the first time during diagnostic testing.) This circuitry consists of a Z80 microprocessor and the associated EPROM circuitry, including EPROM buffers A10U340, U345, U350 and decoder A10U380. The microprocessor reads the EPROMs through bi-directional buffer A10U550.

1111
1121

EPROM COMP AREA – TEST DESCRIPTION

The EPROM COMP test checks the byte at EPROM end-minus-two against end-minus-three for each EPROM to see if they are complementary. This tests the ability of the bus to be driven both logic high and low for all bits. If an error is detected, the expected and actual values are written to the 1240 display screen.

ROUTINE 1 DESCRIPTION

The bytes at $1FFC_{hex}$ and $1FFD_{hex}$ are checked to see if they are complementary.

1111 Error Index

Explanation: The bytes at $1FFC_{hex}$ and $1FFD_{hex}$ were found not to be complementary.

Probable Cause	Action
Bad EPROM	Suspect the diagnostic EPROM A10U160

ROUTINE 2 DESCRIPTION

The bytes at $3FFC_{hex}$ and $3FFD_{hex}$ are checked to see if they are complementary.

1121 Error Index

Explanation: The bytes at $3FFC_{hex}$ and $3FFD_{hex}$ were found not to be complementary.

Probable Cause	Action
Bad EPROM	Suspect the diagnostic EPROM A10U165
Bad address decoder	Suspect A10U380

ROUTINE 3 DESCRIPTION

The bytes at $5FFC_{hex}$ and $5FFD_{hex}$ are checked to see if they are complementary.

1131 Error Index

Explanation: The bytes at $5FFC_{hex}$ and $5FFD_{hex}$ were found not to be complementary.

Probable Cause	Action
Bad EPROM	Suspect the EPROM A10U170
Bad address decoder	Suspect A10U380

ROUTINE 4 DESCRIPTION

The bytes at $7FFC_{hex}$ and $7FFD_{hex}$ are checked to see if they are complementary.

1141 Error Index

Explanation: The bytes at $7FFC_{hex}$ and $7FFD_{hex}$ were found not to be complementary.

Probable Cause	Action
Bad EPROM	Suspect the EPROM A10U180
Bad address decoder	Suspect A10U380

ROUTINE 5 DESCRIPTION

The bytes at $9FFC_{hex}$ and $9FFD_{hex}$ are checked to see if they are complementary.

1151 Error Index

Explanation: The bytes at $9FFC_{hex}$ and $9FFD_{hex}$ were found not to be complementary.

Probable Cause	Action
Bad EPROM	Suspect the EPROM A10U185
Bad address decoder	Suspect A10U380

I/O PROCESSOR BLOCK DIAGRAM
EPROM CHECKSUM – AREA 2

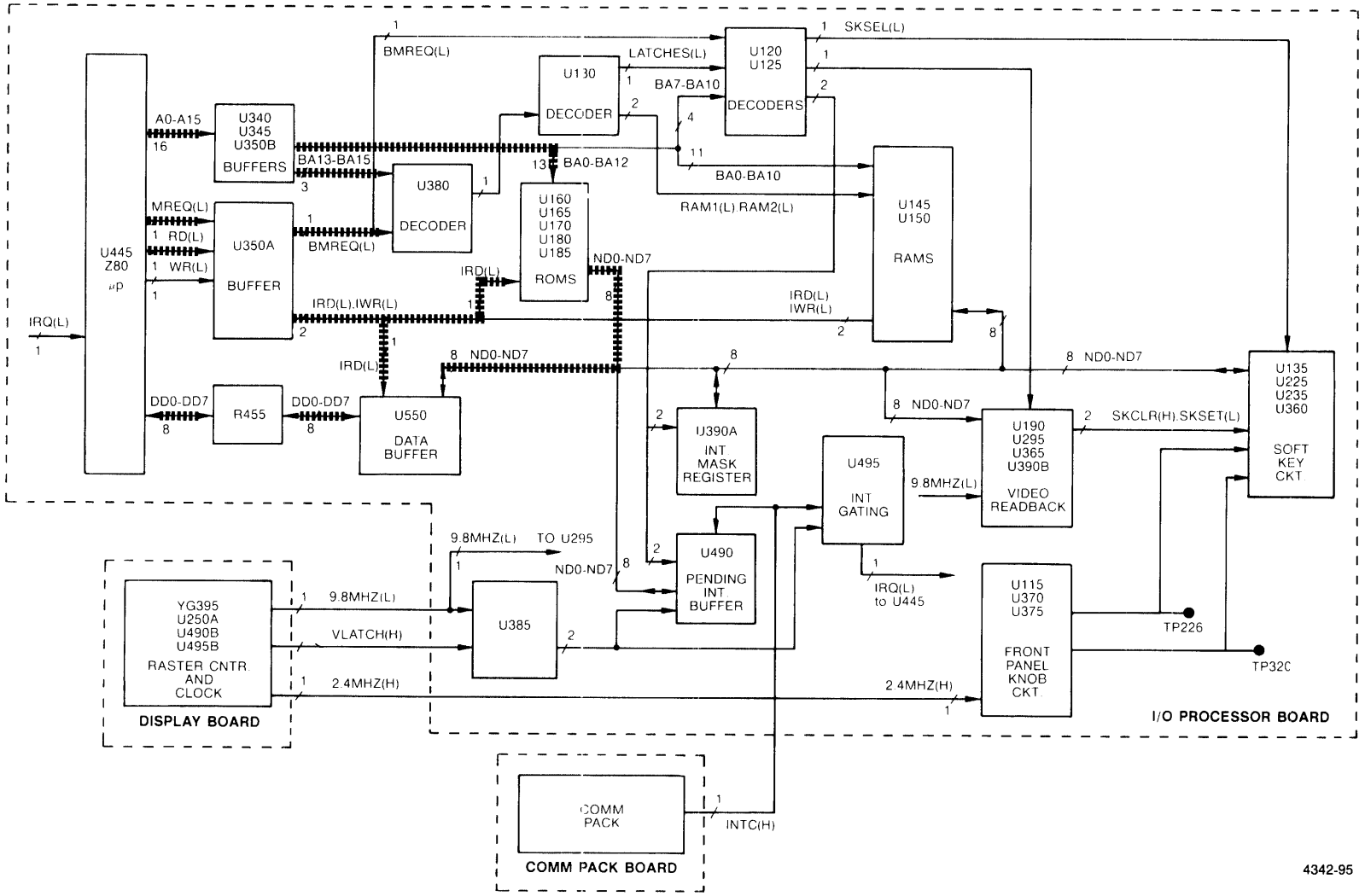


Figure 8-29. I/O Processor EPROM CSUM block diagram.

I/O PROCESSOR BOARD – COMPONENT LOCATION

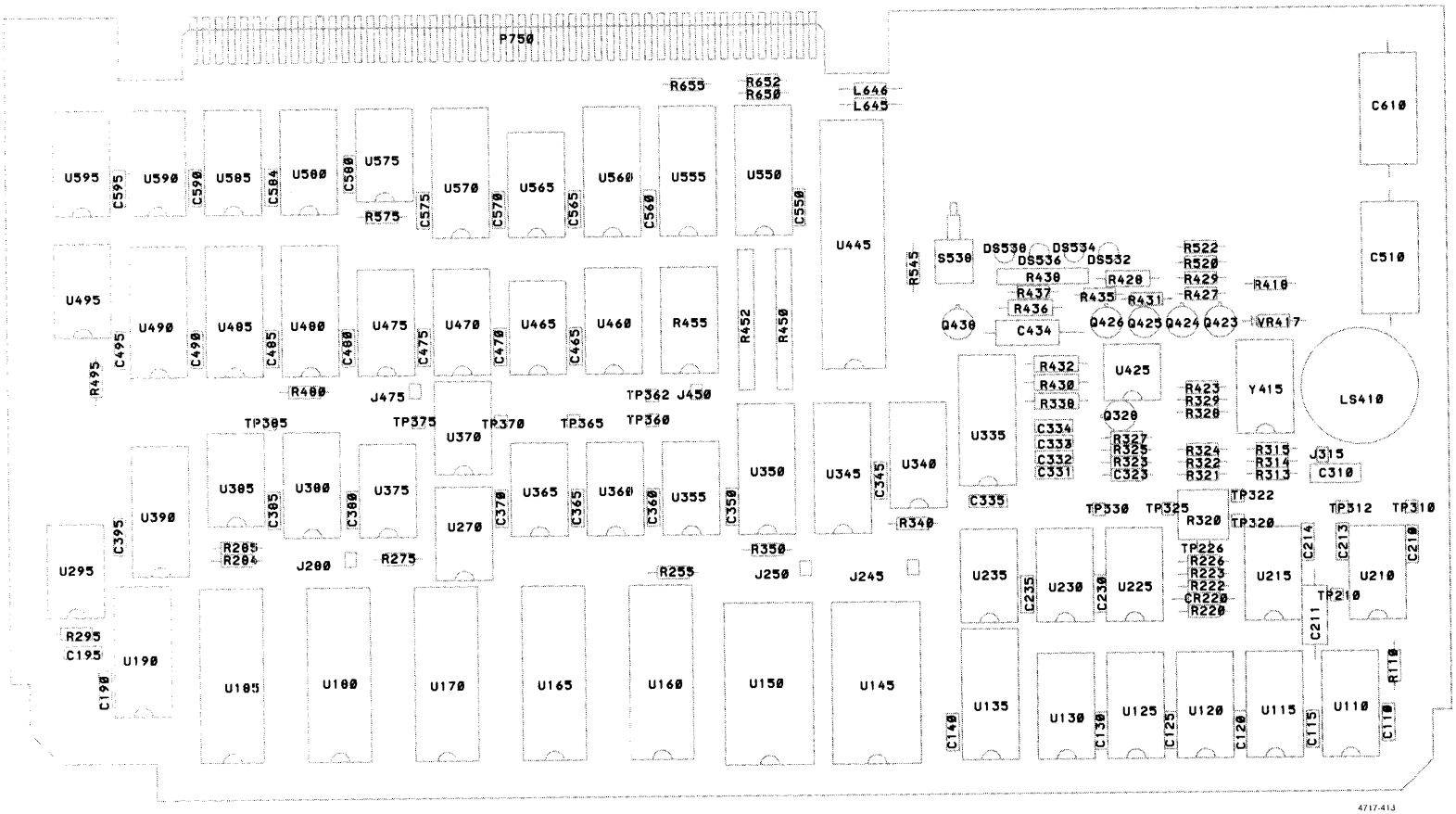


Figure 8-30. I/O Processor Board component location.

module: I/O
area: EPROM CSUM

EPROM CHECKSUM AREA – CIRCUIT OVERVIEW

The circuitry that is exercised by the EPROM CSUM checksum test is indicated by the shaded path on the block diagram. (The shading indicates circuitry exercised for the first time during diagnostic testing.) This circuitry consists of a Z80 microprocessor and the associated EPROM circuitry, including EPROM buffers A10U340, U345, U350 and decoder A10U380. The microprocessor reads the EPROMs through bi-directional buffer A10U550.

1211
1221

EPROM CHECKSUM AREA – TEST DESCRIPTION

The EPROM CSUM test performs a checksum calculation on each of the EPROMS. The calculated checksum is compared to an expected value that is stored in the last two locations of the ROM. The calculated and expected values are written to the display screen.

ROUTINE 1 DESCRIPTION

The checksum is calculated on EPROM A10U160 and the results are written to the screen.

1211 Error Index

Explanation: The calculated checksum did not agree with the expected checksum.

Probable Cause	Action
Bad EPROM	Suspect EPROM A10U160

ROUTINE 2 DESCRIPTION

The checksum is calculated on EPROM A10U165 and the results are written to the display screen.

1221 Error Index

Explanation: The calculated checksum did not agree with the expected checksum.

Probable Cause	Action
Bad EPROM	Suspect EPROM A10U165

ROUTINE 3 DESCRIPTION

The checksum is calculated on ROM A10U170 and the results are written to the display screen.

1231 Error Index

Explanation: The calculated checksum did not agree with the expected checksum.

Probable Cause	Action
Bad EPROM	Suspect EPROM A10U170

ROUTINE 4 DESCRIPTION

The checksum is calculated on EPROM A10U180 and the results are written to the display screen.

1241 Error Index

Explanation: The calculated checksum did not agree with the expected checksum.

Probable Cause	Action
Bad EPROM	Suspect EPROM A10U180

ROUTINE 5 DESCRIPTION

The checksum is calculated on ROM A10U185 and the results are written to the display screen.

1251 Error Index

Explanation: The calculated checksum did not agree with the expected checksum.

Probable Cause	Action
Bad EPROM	Suspect firmware EPROM A10U185

I/O PROCESSOR BLOCK DIAGRAM
EPROM PAGE – AREA 3

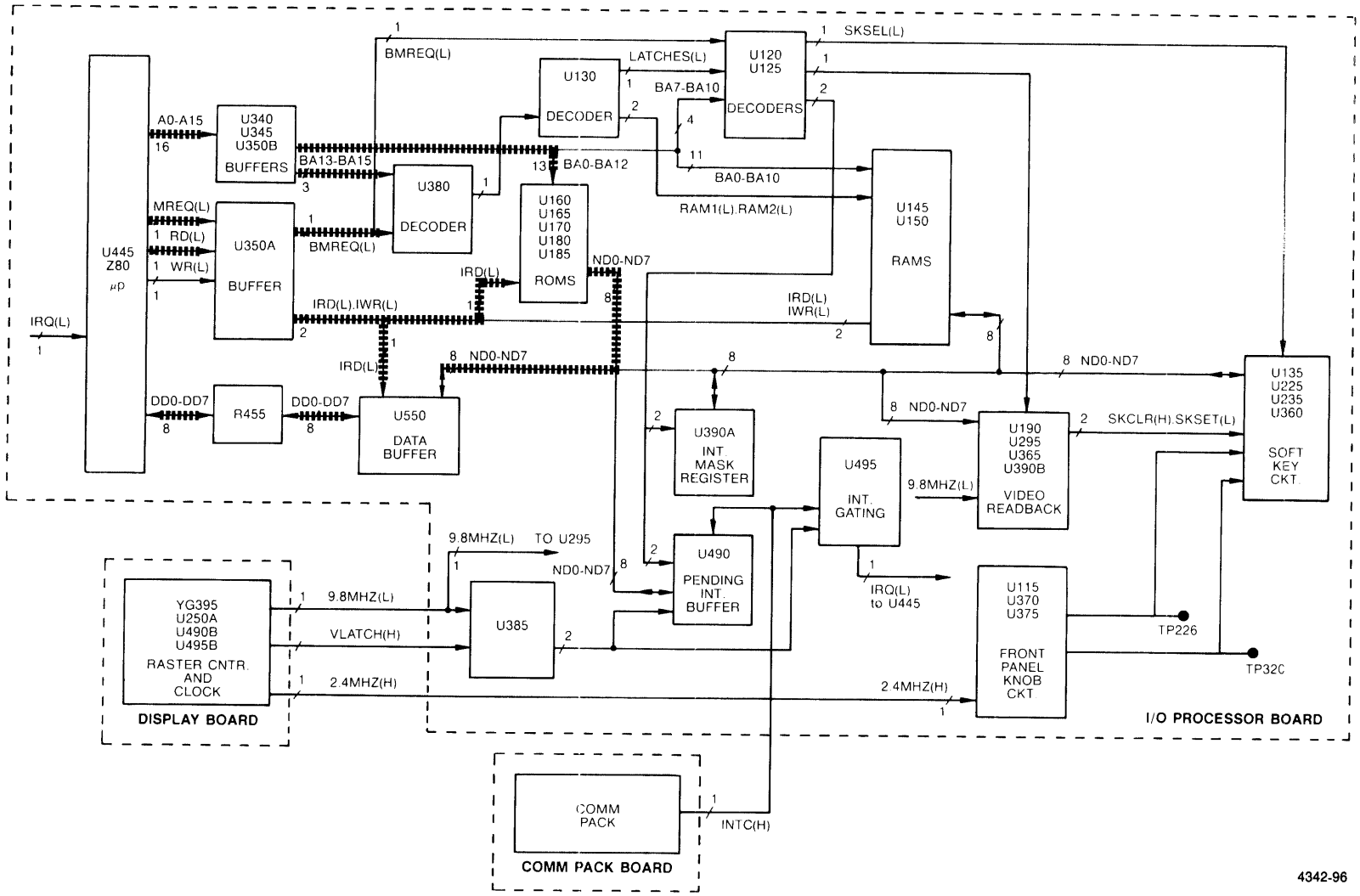


Figure 8-31. I/O Processor EPROM PAGE block diagram.

I/O PROCESSOR BOARD – COMPONENT LOCATION

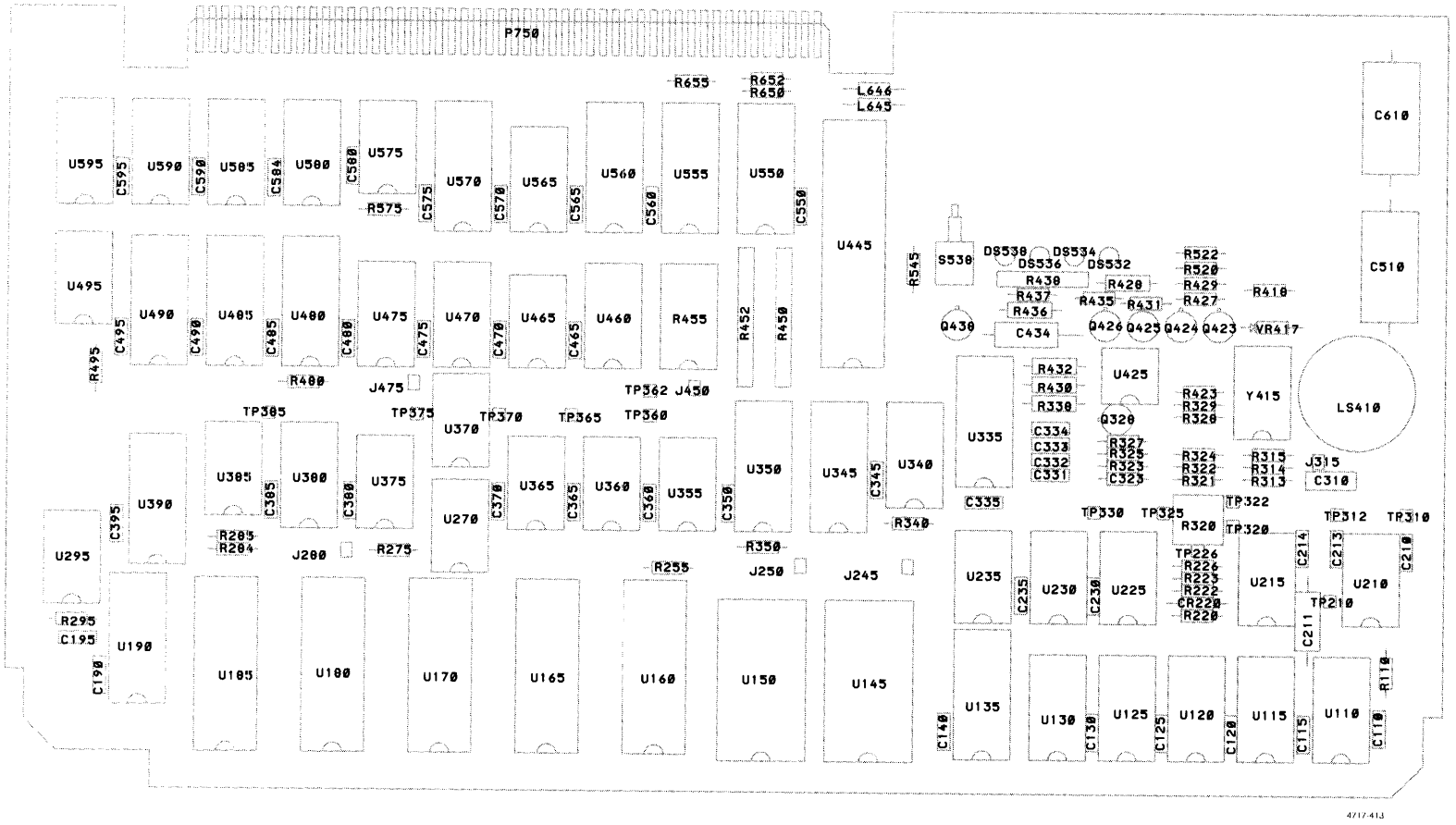


Figure 8-32. I/O Processor Board component location.

module: I/O
area: EPROM PAGE

EPROM PAGE AREA – CIRCUIT OVERVIEW

The circuitry that is exercised by the EPROM Page test is indicated by the shaded path on the block diagram. (The shading indicates circuitry exercised for the first time during diagnostic testing.) This circuitry consists of a Z80 microprocessor and the associated EPROM circuitry, including EPROM buffers A10U340, U345, U350 and decoder A10U380. The microprocessor reads the EPROM through bidirectional buffer A10U550.

1311

EPROM PAGE AREA – TEST DESCRIPTION

The routines in the EPROM Page test check that each ROM is in the correct socket. This is done by checking the byte at the last ROM-address-minus-seven. The value that is found at that address is compared with an expected value for the EPROM in that socket. An error index is generated if any other value is found.

ROUTINE 1 DESCRIPTION

This routine reads the byte at ROM end-minus-seven in socket A10U160 and compares it with the expected value of $1F_{hex}$.

1311 Error Index

Explanation: Page address value incorrect; $1F_{hex}$ was expected.

Probable Cause	Action
EPROM in A10U160 socket not in correct location	Move EPROM to correct location

If actual data is	Correct location is
$3F_{hex}$	A10U165
$5F_{hex}$	A10U170
$7F_{hex}$	A10U180
$9F_{hex}$	A10U185

Probable Cause	Action
EPROM in socket A10U160 is defective	Replace with a good EPROM of correct type. (Refer to *Replaceable Electrical Parts List* section).

ROUTINE 2 DESCRIPTION

This routine reads the byte at EPROM end-minus-seven in socket A10U165 and compares it with the expected value of $3F_{hex}$.

1321 Error Index

Explanation: Page address value incorrect; $3F_{hex}$ was expected.

Probable Cause	Action
EPROM in A10U165 socket not in correct location	Move EPROM to correct location

If actual data is	Correct location is
$1F_{hex}$	A10U160
$5F_{hex}$	A10U170
$7F_{hex}$	A10U180
$9F_{hex}$	A10U185

Probable Cause	Action
EPROM in socket A10U165 is defective	Replace with a good EPROM of correct type. (Refer to *Replaceable Electrical Parts List* section).

ROUTINE 3 DESCRIPTION

This routine reads the byte at EPROM end-minus-seven in socket A10U170 and compares it with the expected value of $5F_{hex}$.

1331 Error Index

Explanation: Page address value incorrect; $5F_{hex}$ was expected.

Probable Cause	Action
EPROM in A10U170 socket not in correct location	Move EPROM to correct location

If actual data is	Correct location is
$1F_{hex}$	A10U160
$3F_{hex}$	A10U165
$7F_{hex}$	A10U180
$9F_{hex}$	A10U185

1341

Probable Cause	Action
EPROM in socket A10U170 is defective	Replace with a good EPROM of correct type. (Refer to *Replaceable Electrical Parts List* section)

ROUTINE 4 DESCRIPTION

This routine reads the byte at EPROM end-minus-seven in socket A10U180 and compares it with the expected value of $7F_{hex}$.

1341 Error Index

Explanation: Page address value incorrect; $7F_{hex}$ was expected.

Probable Cause	Action
EPROM in A10U180 socket not in correct location	Move EPROM to correct location

If actual data is	Correct location is
$1F_{hex}$	A10U160
$3F_{hex}$	A10U165
$5F_{hex}$	A10U170
$9F_{hex}$	A10U185

Probable Cause	Action
EPROM in socket A10U180 is defective	Replace with a good EPROM of correct type. (Refer to *Replaceable Electrical Parts List* section).

ROUTINE 5 DESCRIPTION

This routine reads the byte at EPROM end-minus-seven in socket A10U185 and compares it with the expected value of $9F_{hex}$.

1351 Error Index

Explanation: Page address value incorrect; $9F_{hex}$ was expected.

Probable Cause	Action
EPROM in A10U185 socket not in correct location	Move EPROM to correct location

If actual data is	Correct location is
$1F_{hex}$	A10U160
$3F_{hex}$	A10U165
$5F_{hex}$	A10U170
$7F_{hex}$	A10U180

Probable Cause	Action
EPROM in socket A10U190 is defective	Replace with a good EPROM of correct type. (Refer to *Replaceable Electrical Parts List* section).

I/O PROCESSOR BLOCK DIAGRAM
RAM – AREA 4

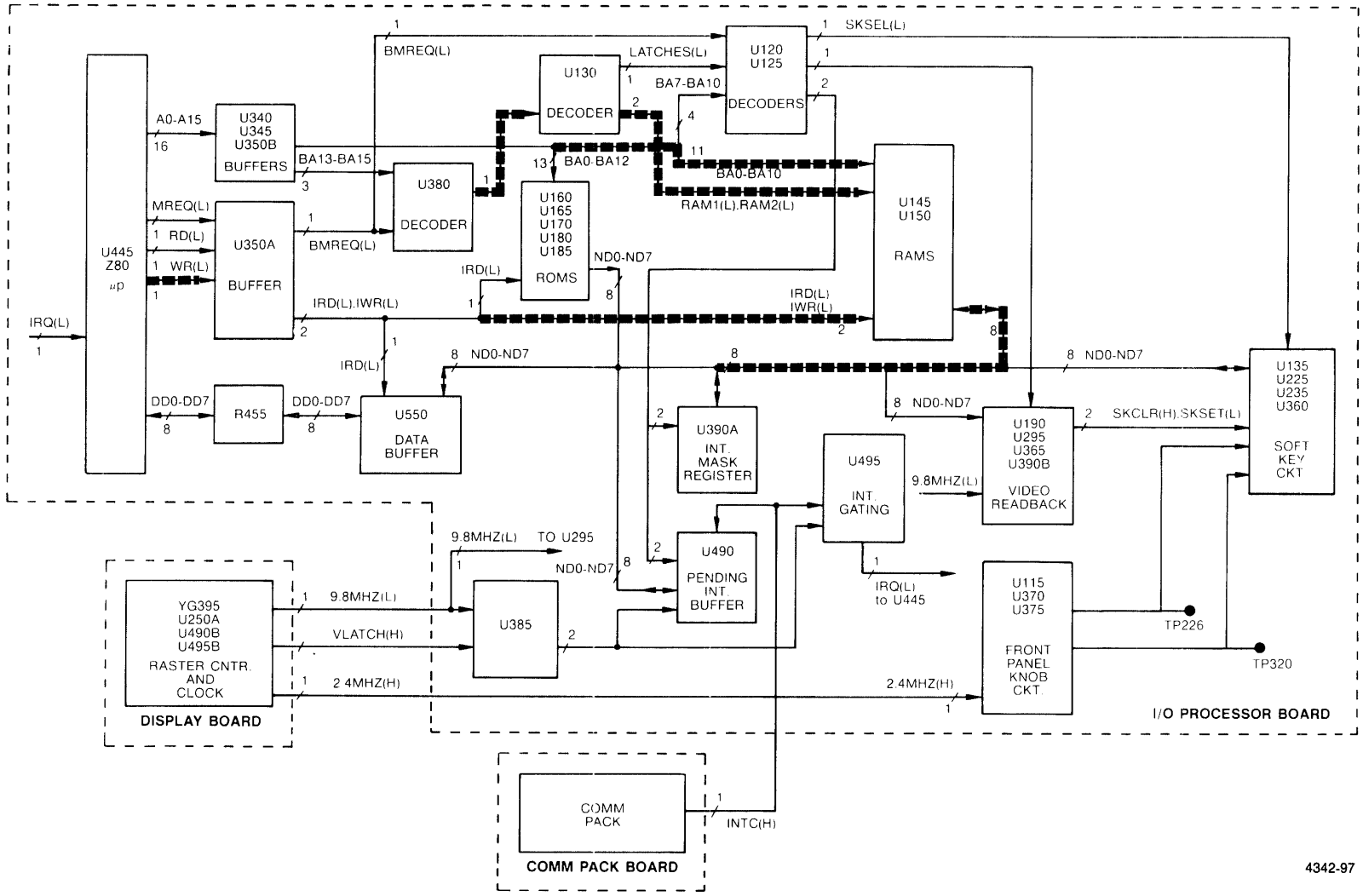


Figure 8-33. I/O Processor RAM block diagram.

I/O PROCESSOR BOARD – COMPONENT LOCATION

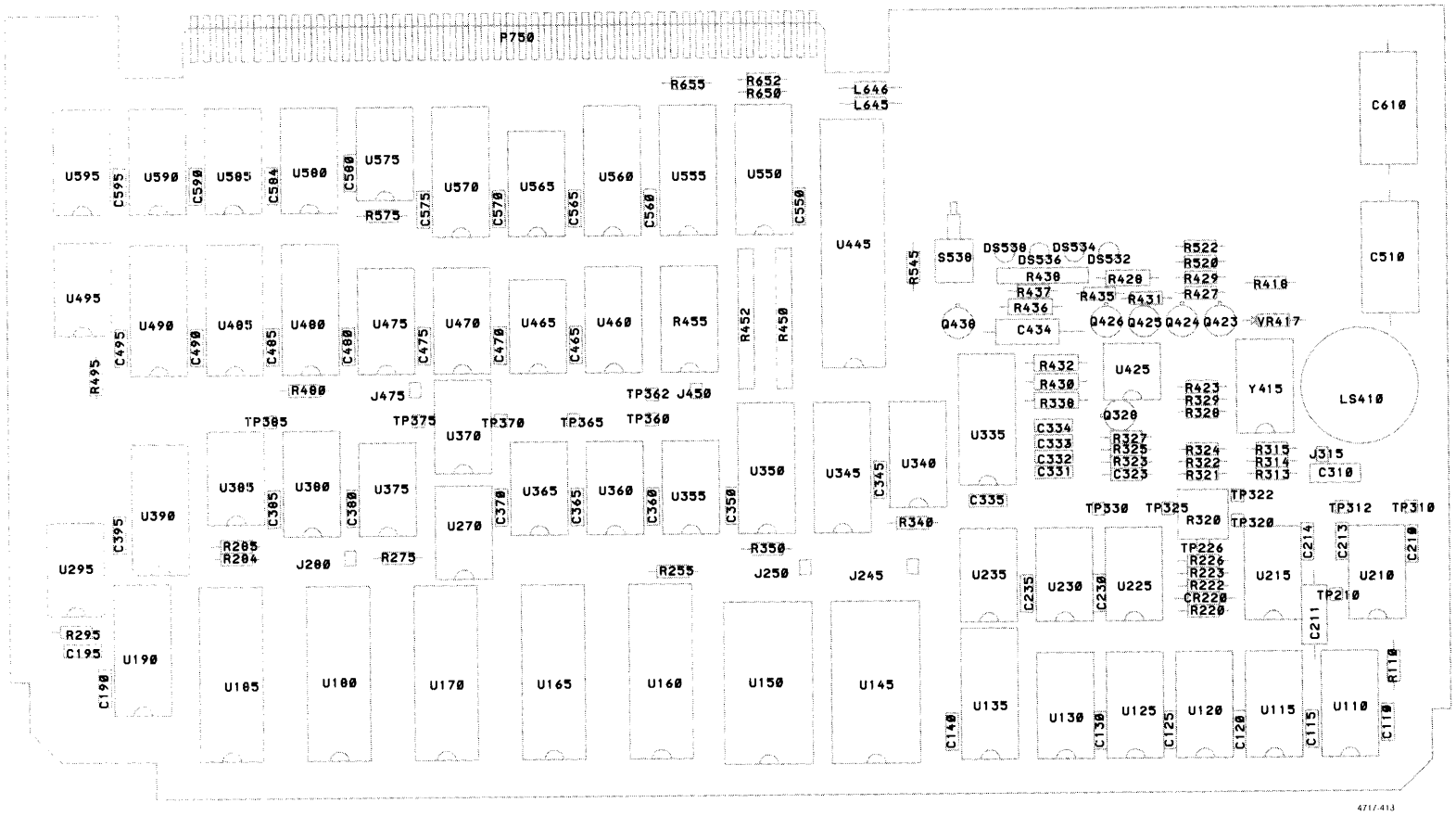


Figure 8-34. I/O Processor Board component location.

module: I/O
area: RAM

RAM AREA – CIRCUIT OVERVIEW

The RAM circuitry is indicated by the shaded path on the block diagram. (The shading indicates circuitry exercised for the first time during diagnostic testing.) This circuitry consists of the Z80 microprocessor A10U445, the RAM itself A10U145 and A10U150, address buffers A10U340, U345, U350 and decoders U130 and U380. In addition, the bidirectional buffer A10U550 is used for writing to and reading from the RAM.

1411

RAM AREA – TEST DESCRIPTION

RAM address locations $B000_{hex}$ to $BBFF_{hex}$ are tested first. If these tests pass, the values at locations $BC00_{hex}$ to $BFFF_{hex}$ are stored at $B000_{hex}$ to $B3FF_{hex}$. Then RAM address locations $BC00_{hex}$ to $BFFF_{hex}$ are tested. After completion of this test, the data is restored to locations $BC00_{hex}$ to $BFFF_{hex}$.

ROUTINE 1 DESCRIPTION

This test starts by writing the pattern AA_{hex} to all locations in A10U150 (address locations $B000_{hex}$ to $B7FF_{hex}$) and to the lower half of A10U145 (address locations $B800_{hex}$ to $BBFF_{hex}$). Then the first location is read and checked for AA_{hex}. If found, CC_{hex} is written to that location. Then the address is incremented and the next location is checked for AA_{hex}. If AA_{hex} is present, then CC_{hex} is written to that location. This procedure is repeated for each RAM address location under test, starting at the lowest address and proceeding to the highest.

Starting at the lowest address location, the RAM is checked for CC_{hex}. If present, $F0_{hex}$ is written to that address location. Then the address is incremented and this procedure is repeated until the end of RAM is reached. After the last address has been checked, the lowest address location is checked for $F0_{hex}$. Each time after $F0_{hex}$ has been found, it is replaced with $0F_{hex}$. Finally, the RAM is checked for $0F_{hex}$. But this time the check starts at the highest address and works its way down to the lowest address location in the RAM under test. If this test passes, the contents of the upper half of A10U145 is saved in the tested area, then the upper half of A10U145 is tested in an identical manner except that now the address range is from $BC00_{hex}$ to $BFFF_{hex}$.

Error Index: 1411

Explanation: RAM test failed. If the failure address (displayed on the 1240 screen) is between $B000_{hex}$ and $B7FF_{hex}$, then A10U150 was being tested when the failure occurred. If the displayed failure address is between $B800_{hex}$ and $BFFF_{hex}$, then A10U145 was being tested when the failure occurred.

Probable Cause	Action
Bad address decoder	Suspect A10U130 or U380
Bad RAM	Suspect the RAM (refer to following table)

Failure address	RAM
B000-B7FF	A10U150
B800-BFFF	A10U145

I/O PROCESSOR BLOCK DIAGRAM
INTERRUPT – AREA 5

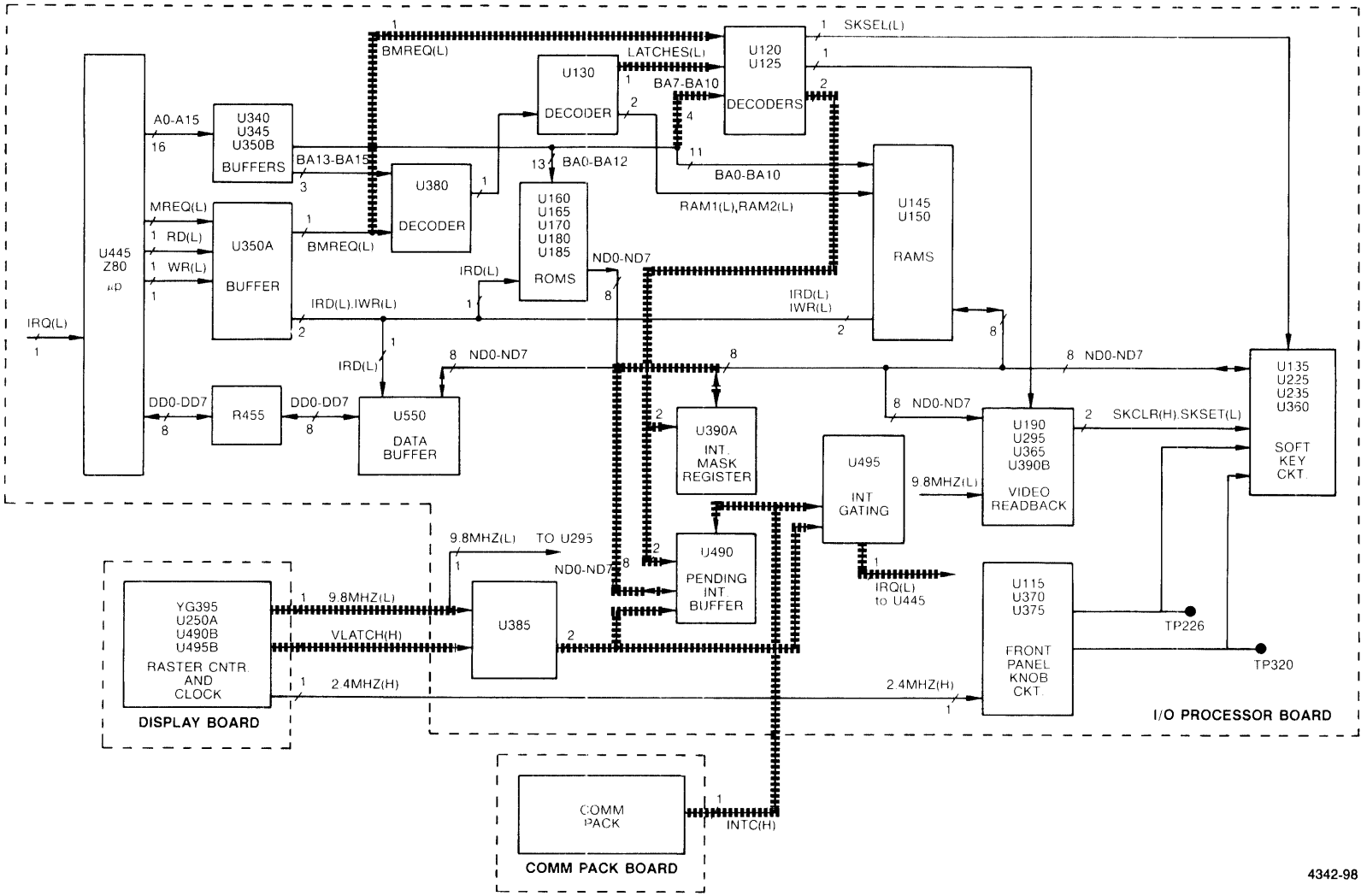


Figure 8-35. I/O Processor INTERRUPT block diagram.

I/O PROCESSOR BOARD – COMPONENT LOCATION

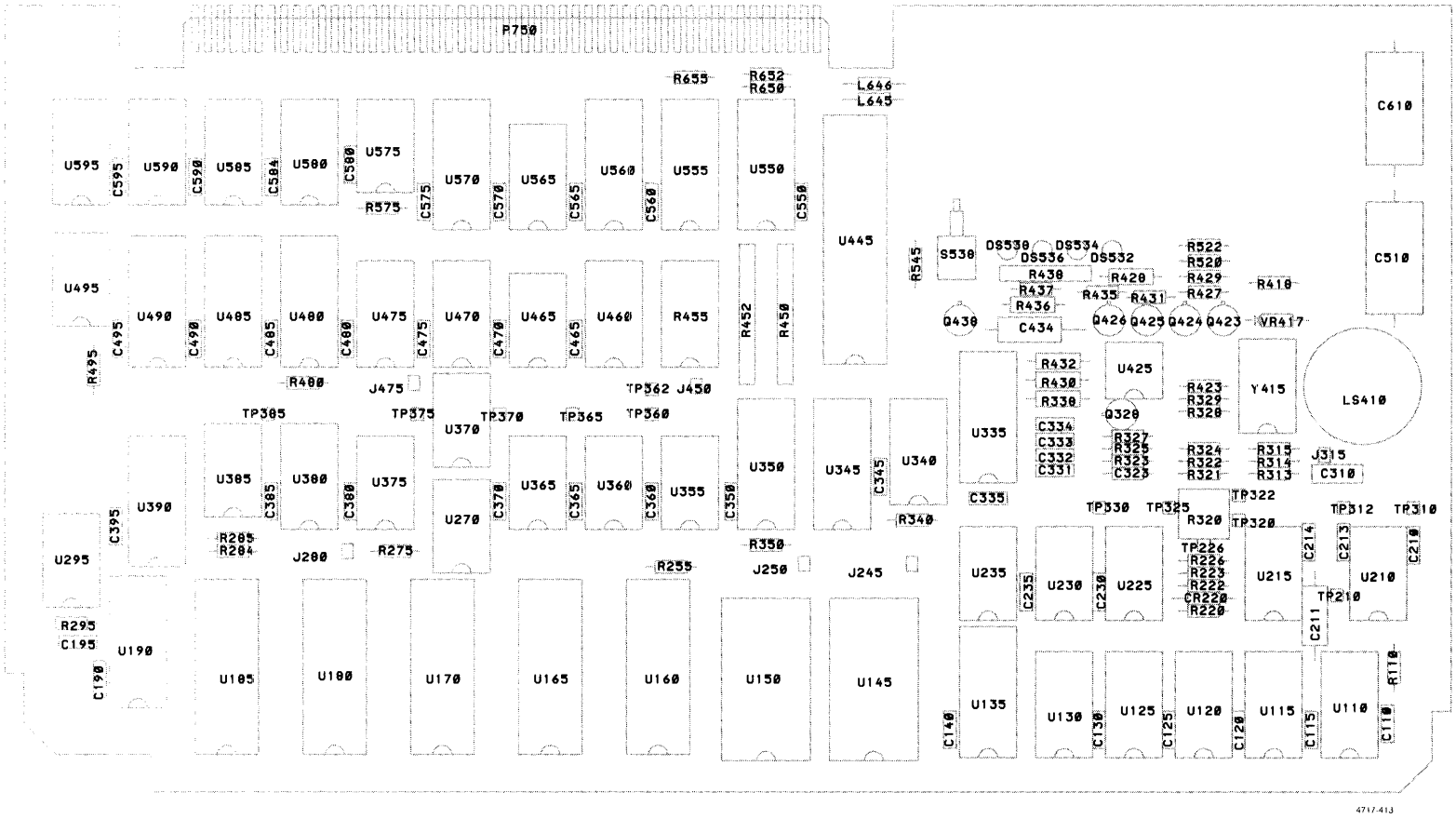


Figure 8-36. I/O Processor Board component location.

module: I/O
area: INTERRUPT

INTERRUPT AREA – CIRCUIT OVERVIEW

The I/O Processor Interrupt circuitry is indicated by the shaded path on the block diagram. (The shading indicates circuitry exercised for the first time during diagnostic testing.) The Z80 microprocessor writes an interrupt mask value to the interrupt mask register, A10U390, through data buffer A10U550. This mask value affects the gating of interrupts through the interrupt register, A10U495 (whose output is IRQ to the Z80). The Z80 may read back the status of the mask and the following interrupts: VIDEO(H) from the display, INTC(H) from COMM packs, or PINT(H) from the Control Processor. Readback is done through the pending interrupt register, A10U490, and the bi-directional data buffer, A10U550.

INTERRUPT AREA – TEST DESCRIPTION

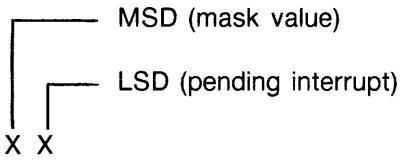
Refer to the following table as you read this discussion:

The Z80 microprocessor writes the mask value 80_{hex} to address $A800_{hex}$ (A10U390). This sets the 60 Hz interrupt mask. The mask value is read from address $A900_{hex}$ (the pending interrupt register, A10U490). Next, a mask value of 20_{hex} is written to address $A800_{hex}$, which sets the INTC interrupt mask. The mask value is read back from address $A900_{hex}$ (A10U490). If a failure occurs, only the first expected and actual mask values are written to the display screen.

INTERRUPT MASK DIGITS

MSD	Means	LSD	Means
0	All interrupts masked	0	No interrupts pending
1	Queue ready	1	60 Hz interrupt pending
2	INTC interrupt masked	2	INTC interrupt pending
4	PINT interrupt masked	4	PINT interrupt pending
8	60 Hz interrupt masked	8	60 Hz int not latched

WHERE:



ROUTINE 1 DESCRIPTION

This test clears the 60 Hz interrupt and writes 80_{hex} to address $A800_{hex}$ (A10U390). This prevents interrupts other than the 60 Hz interrupt from interrupting the I/O Processor. Interrupts are enabled, and the test goes into a wait loop until a 60 Hz interrupt occurs or the test times out. The mask and the pending interrupt are read from address $A900_{hex}$ (A10U490). If the mask or the pending interrupt was incorrect, the error index value will be 1511. If no interrupt occurred, the error index value will be 1512.

1511 Error Index

Explanation: The mask or the pending interrupt was incorrect; expected value was 80_{hex}.

Probable Cause	Action
Bad pending interrupt register.	Suspect A10U490.
Bad interrupt mask register.	Suspect A10U390.
Bad address decoder.	Suspect A10U130 or U120.

1512 Error Index

Explanation: The I/O Processor failed to be interrupted by the 60 Hz interrupt.

Probable Cause	Action
Bad interrupt mask register.	Suspect A10U390.
Bad interrupt register.	Suspect A10U495.
Bad 60 Hz interrupt source.	Suspect A10U385.

ROUTINE 2 DESCRIPTION

This test clears the INTC(H) interrupt and writes 20_{hex} to address $A800_{hex}$ (A10U390). This prevents interrupts other than INTC(H) from interrupting the I/O Processor. Interrupts are enabled, and the test goes into a wait loop until a INTC(H) interrupt occurs or the test times out. The mask and the pending interrupt are read from address $A900_{hex}$ (A10U490). If the mask or the pending interrupt was incorrect, the error index value will be 1521. If no interrupt occurred, the error index value will be 1522. If a COMM pack is installed, the INTC(H) line is checked to see if it is being held low. No interrupt should be generated under these circumstances.

1521 Error Index

Explanation: The mask or pending interrupt was incorrect; the expected value was 20_{hex}.

Probable Cause	Action
Bad pending interrupt register.	Suspect A10U490.
Bad interrupt mask register.	Suspect A10U390

1522 Error Index

Explanation: The I/O Processor failed to be interrupted by INTC(H) interrupt.

Probable Cause	Action
Bad interrupt mask register.	Suspect A10U390.
Bad interrupt register.	Suspect A10U495.
Bad INTC source.	Suspect A32U220 if using RS232 COMM pack; A32U135 or U145 if using a GPIB COMM pack.

I/O PROCESSOR BLOCK DIAGRAM
DIAGNOSTIC WINDOW – AREA 6

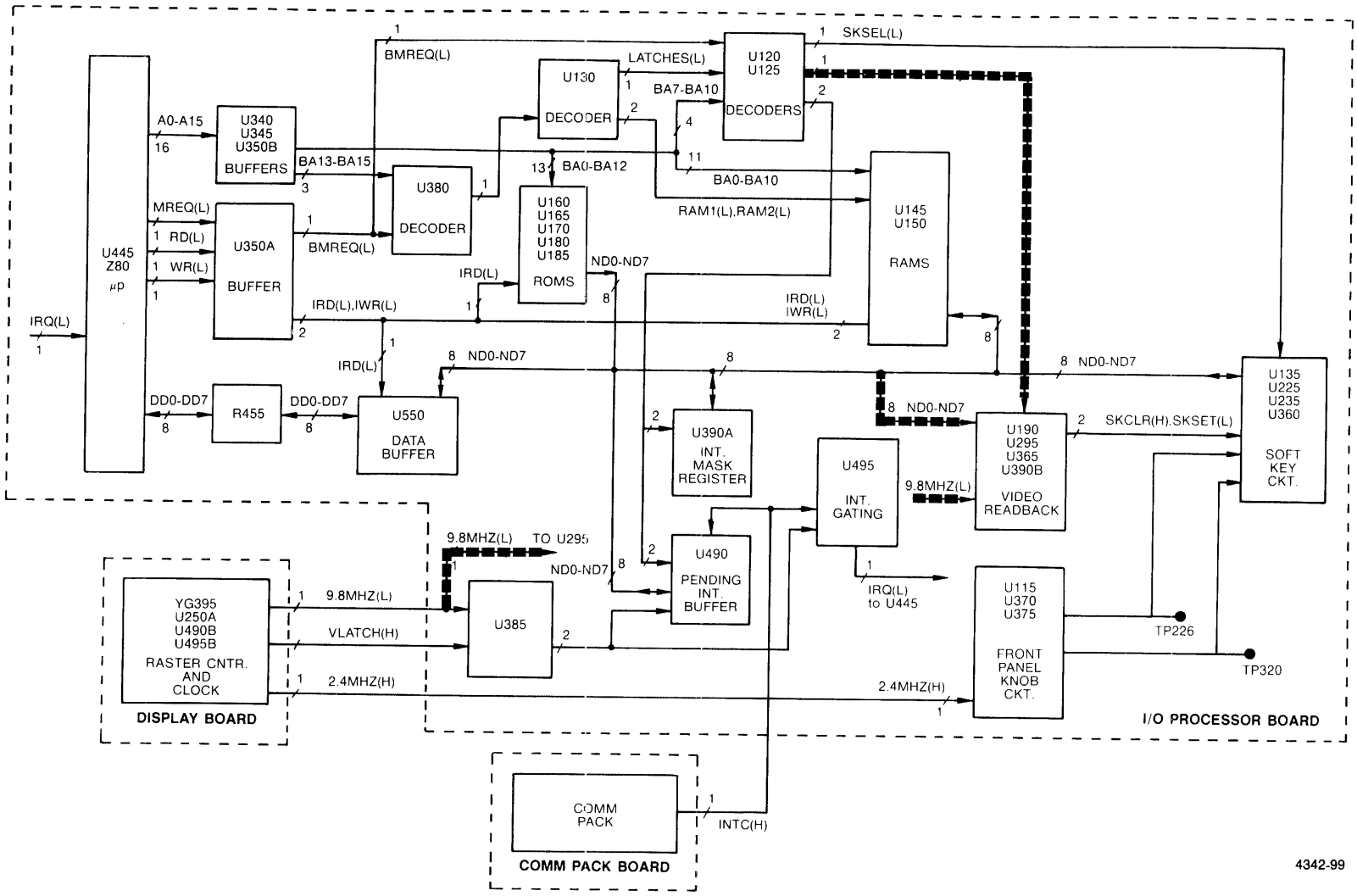


Figure 8-37. I/O Processor DWINDOW block diagram.

I/O PROCESSOR BOARD – COMPONENT LOCATION

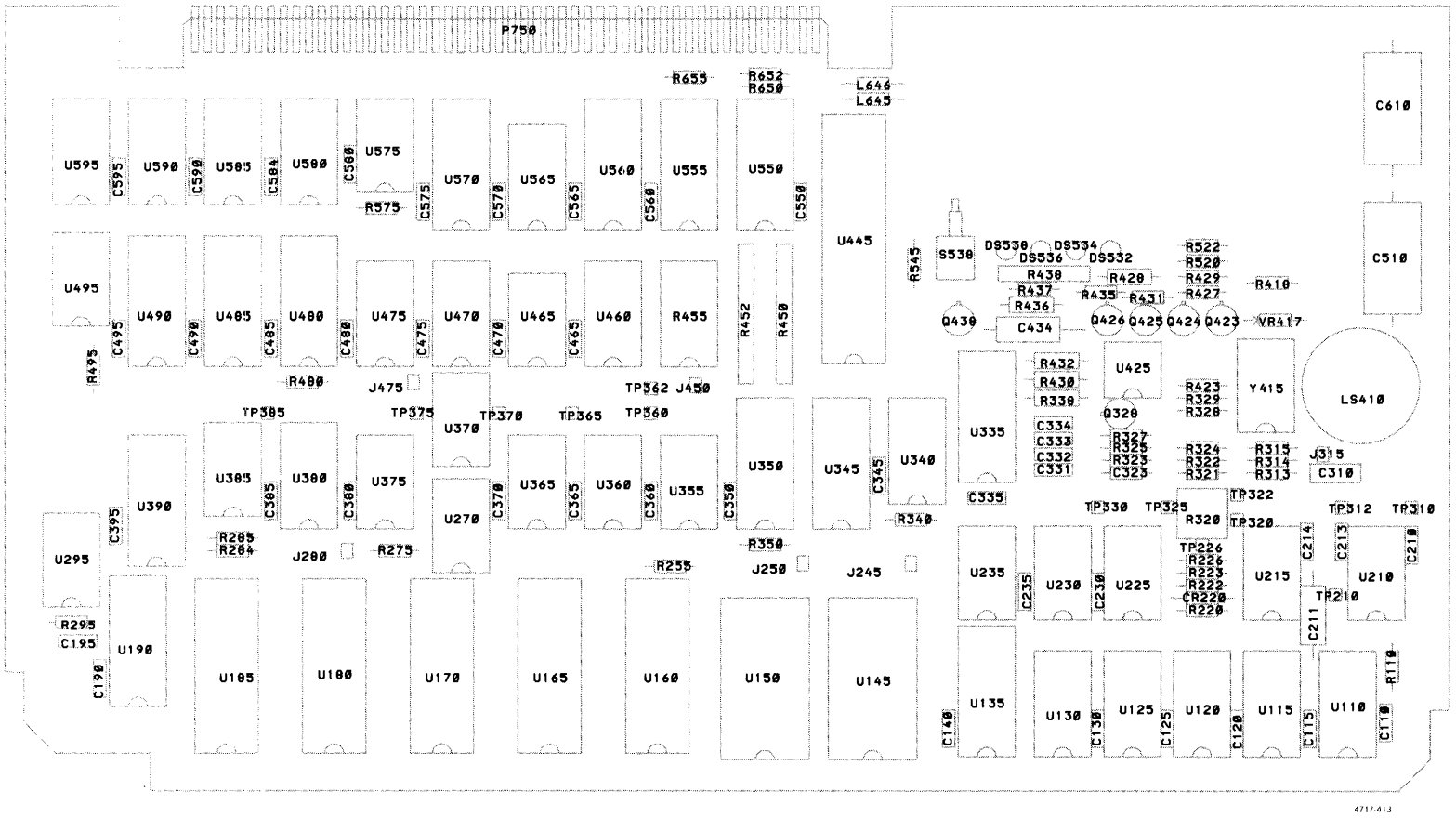


Figure 8-38. I/O Processor Board component location.

module: I/O
area: DWINDOW

DIAGNOSTIC WINDOW AREA – CIRCUIT OVERVIEW

The circuitry comprising the Diagnostic Window is indicated by the shaded path on the block diagram. The Diagnostic Window circuitry includes parts of A10U390, U120, U190, and U295 which are not used during normal 1240 operations. This circuitry is used during diagnostics to pretest other circuitry that is used during video display diagnostic tests, before the display diagnostics are run.

1610

DIAGNOSTIC WINDOW – TEST DESCRIPTION

First, a mask value is written to the interrupt mask register to clear the diagnostic window register and mask all interrupts except the 60 Hz interrupt. Two 60 Hz interrupts are expected. After they have had time to occur, the diagnostic window register is read back and checked. A new mask value is written to the interrupt mask register. Once more, two 60 Hz interrupts are expected. When they have had time to occur, the diagnostic window is again read and checked for the correct mask value.

ROUTINE 1 DESCRIPTION

The Z80 writes mask value $8C_{hex}$ to address $A800_{hex}$ (the diagnostic window register, A10U390). This clears the diagnostic window register and masks all interrupts except the 60 Hz interrupt. If two 60 Hz interrupts are not received, the test fails. The values in the interrupt gating register, A10U495, are read back through A10U490 and written to the display screen. If the two interrupts are received, the test reads address $A880_{hex}$ (A10U190) for the expected value of 00_{hex}. If that value is present, then 94_{hex} is written to address $A800_{hex}$ (A10U390). If 00_{hex} was not present, both the expected value and the actual are displayed on the screen. Now, two or more 60 Hz interrupts are expected and if they occur, address $A880_{hex}$ (A10U190) is read for the expected value of FF_{hex}. If it is present, then $9C_{hex}$ is written to $A800_{hex}$. Again, sufficient time for two 60 Hz interrupts to occur is allowed and, if they occur, address $A880_{hex}$ (A10U190) is read and checked for 00_{hex}.

1610 Error Index

Explanation: The value $8C_{hex}$ was written to $A800_{hex}$ (A10U390) and time was allowed for two 60 Hz interrupts to occur. No 60 Hz interrupts were detected within the allowed time. The interrupt register contents are read and written to the display screen.

Probable Cause	Action
Suspect A10U490, U390, U495, or U385.	Analyze these components while looping on this interrupt routine test.

1611 Error Index

Explanation: The value $8C_{hex}$ was written to address $A800_{hex}$ (A10U390). This clears the diagnostic window and masks all interrupts except for the 60 Hz interrupt. Time was allowed for two 60 Hz interrupts to occur then address $A880_{hex}$ (A10U190) was read, expecting the value 00_{hex}.

Probable Cause	Action
Suspect A10U390.	Check A10U390-19 for a low while looping on interrupt routine. Check A10U390-16 for a pulsing high while looping.
Suspect A10U295.	Turn off power and check continuity between A10U295 and A10U190.

1612 Error Index

Explanation: The value 94_{hex} was written to address $A800_{hex}$ (A10U390). Time was allowed for two 60 Hz interrupts to occur then address $A880_{hex}$ (A10U190) was read, expecting the value FF_{hex}.

Probable Cause	Action
Suspect A10U390.	Check A10U390-19 for a low while looping on interrupt routine. Check A10U390-16 for a pulsing high while looping.
Suspect A10U295.	Turn off power and check continuity between A10U295 and A10U190.

1613 Error Index

Explanation: The value $9C_{hex}$ was written to address $A800_{hex}$ (A10U390). Time was allowed for two 60 Hz interrupts to occur then address $A880_{hex}$ (A10U190) was read, expecting the value 00_{hex}.

Probable Cause	Action
Suspect A10U390.	Check A10U390-16 for a pulsing high while looping on interrupt routine. Check A10U390-19 for a pulsing low while looping.

I/O PROCESSOR BLOCK DIAGRAM
SKEYREG – AREA 7

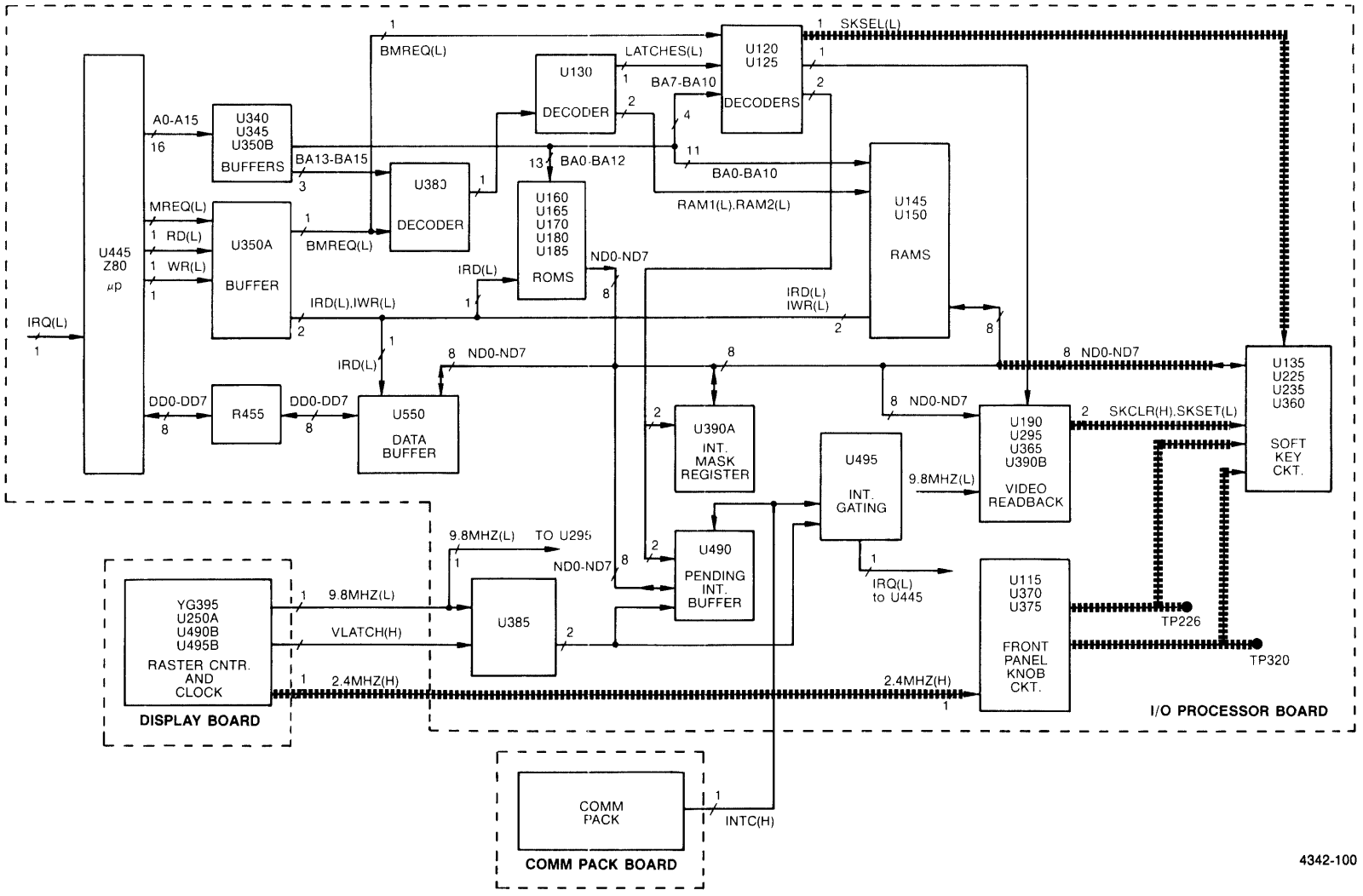


Figure 8-39. I/O Processor SKEYREG block diagram.

I/O PROCESSOR BOARD – COMPONENT LOCATION

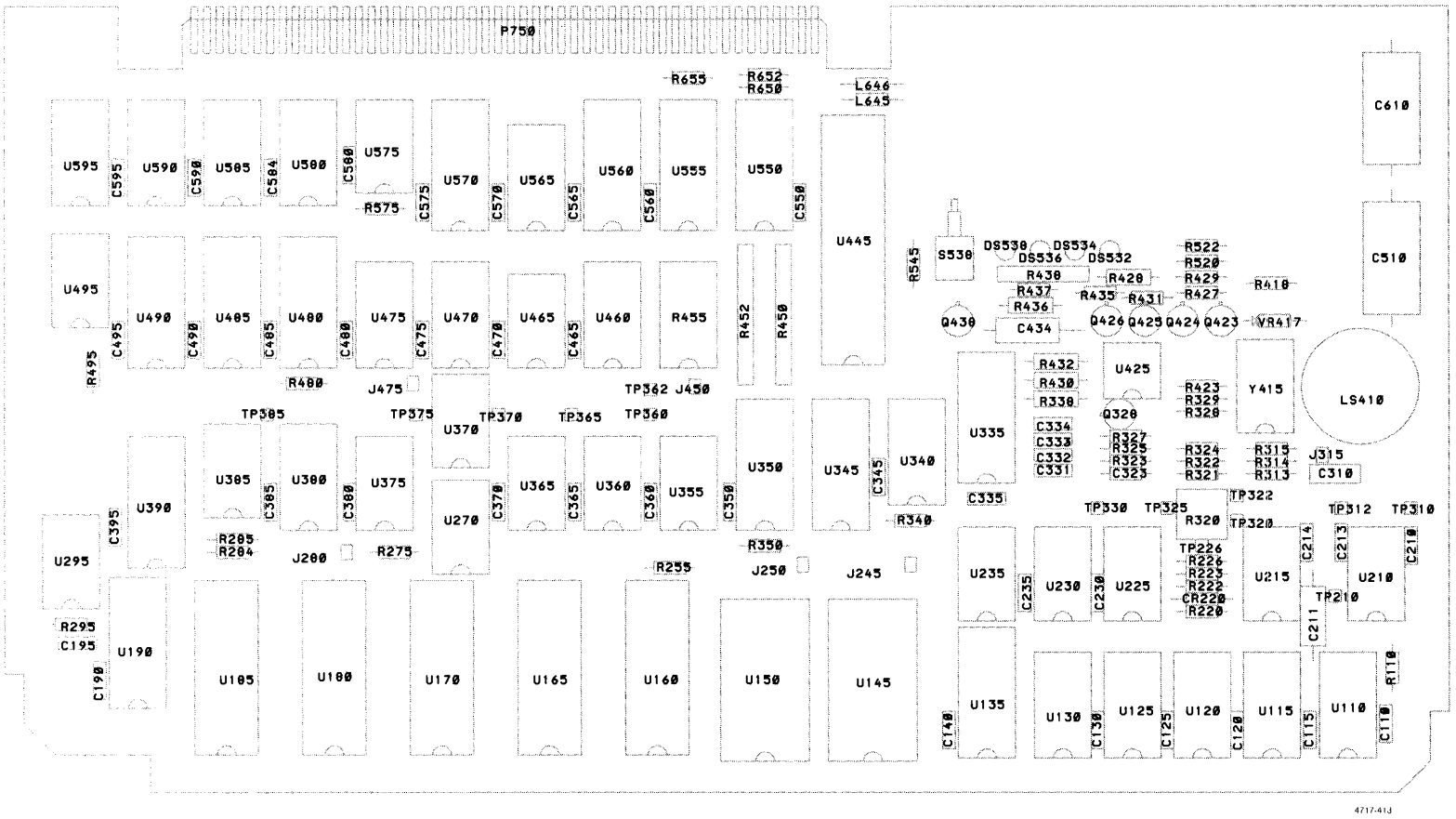


Figure 8-40. I/O Processor Board component location.

module: I/O
area: SKEYREG

SKEYREG AREA – CIRCUIT OVERVIEW

The pattern-shaded signal lines on the soft key readback register block diagram indicate circuitry used during diagnostic testing. Only the circuitry that is being exercised for the first time during diagnostic testing is shown. Circuitry exercised by other diagnostic tests are shown in their respective block diagrams.

1710

This soft key circuitry provides the I/O Processor with readback capability of processed soft key information, allowing the processor to determine when a soft key has been activated. Register A10U135 latches the soft key information from the shift register A10U235, subsequently gating it onto the ND data bus at a rate of 300Hz. The I/O Processor receives this information through the bidirectional buffer A10U550.

SKEYREG AREA – TEST DESCRIPTION

The SKSET(L) and SKCLR(H) control lines are used only during diagnostic tests. With these lines, the shift register A10U235 can be forced to output all ones or all zeros. By alternately filling and clearing the shift register with desired information, it is possible to check the operation of the readback circuitry before performing any Frontpanel Soft Key diagnostic tests.

First, $8C_{hex}$ is written to address $A800_{hex}$ (the diagnostic window register, A10U390). This action clears the soft key register A10U135 and masks all interrupts except the 60 Hz interrupt. Now, two 60 Hz interrupts are expected to occur. If no interrupts are detected, the test fails and the results are displayed.

If they occur, the test reads from address $AB00_{hex}$ (the soft key register, U135) expecting 00_{hex}. If the correct value is read, then 94_{hex} is written to address $A800_{hex}$. Once more, two 60 Hz interrupts are expected. When they have had time to occur, the test reads address $AB00_{hex}$ and checks for FF_{hex}. If correct, $9C_{hex}$ is written to address $A800_{hex}$ and two more interrupts are expected. If they occur, the register is checked one last time for a readback value of 00_{hex}.

1710 Error Index

Explanation: No interrupt occurred. The value $8C_{hex}$ was written to A10U390 and time was allowed for two 60 Hz interrupts to occur. No 60 Hz interrupts were detected within the allowed time. The contents of the interrupt register are read and displayed on the screen.

Probable Cause	Action
Suspect A10U385, U390, U490, or U495.	Analyze these components while looping on this routine test. Check A10U495-6 for low-going pulses.

1711 Error Index

Explanation: Incorrect data read from the soft key register, A10U135. The value $8C_{hex}$ was written to address $A800_{hex}$ (A10U390). This action cleared U135 and masked all interrupts except the 60 Hz interrupt. Time was allowed for two 60 Hz interrupts to occur and the test read address $AB00_{hex}$ (the soft key register) expecting to find 00_{hex}.

Probable Cause	Action
Suspect A10U390.	Check U390-16 and -19 for a low while looping on this routine test.
Suspect A10U235.	Check U235-8 for the 2.3 kHz clock while looping on this routine test.
Suspect A10U135.	Check U135-11 for a 300 Hz clock while looping. Check U135-1 for a low while looping.

1712 Error Index

Explanation: Incorrect data read from the soft key register, A10U135. The value 94_{hex} was written to address $A800_{hex}$ (the diagnostic window register). This action cleared U135 and masked all interrupts except the 60 Hz interrupt. Time was allowed for two 60 Hz interrupts to occur and the test read address $AB00_{hex}$ (the soft key register) expecting to find FF_{hex}.

Probable Cause	Action
Suspect A10U390.	Check U390-19 for a low while looping on this routine test. Check U390-16 for pulsing high while looping.
Suspect A10U235.	Power-down the 1240 and check the continuity between A10U235 and U135.

1713 Error Index

Explanation: Incorrect data read from the soft key register, A10U135. The value $9C_{hex}$ was written to address $A800_{hex}$ (the diagnostic window register). This action cleared U135 and masked all interrupts except the 60 Hz interrupt. Time was allowed for two 60 Hz interrupts to occur and the test read address $AB00_{hex}$ (the soft key register) expecting to find 00_{hex}.

Probable Cause	Action
Suspect A10U390.	Check U390-19 for a pulsing high while looping on this routine test. Check U390-16 for a pulsing low while looping.

2XXX FRONTPANEL ERROR INDEXES

Error Index	Area Name	Area Number
21XX	HARD KEYS	AREA 1
22XX	SOFT KEYS	AREA 2
23XX	KNOB	AREA 3

FRONTPANEL MANUAL TESTS

Module	Area	Routine	Description
FRONTPANEL	FP VERIFY	1	Hard Key/Knob Verify
	FP VERIFY	2	Screen Align/Soft Key Verify

FRONTPANEL BLOCK DIAGRAM
HARD KEYS – AREA 1

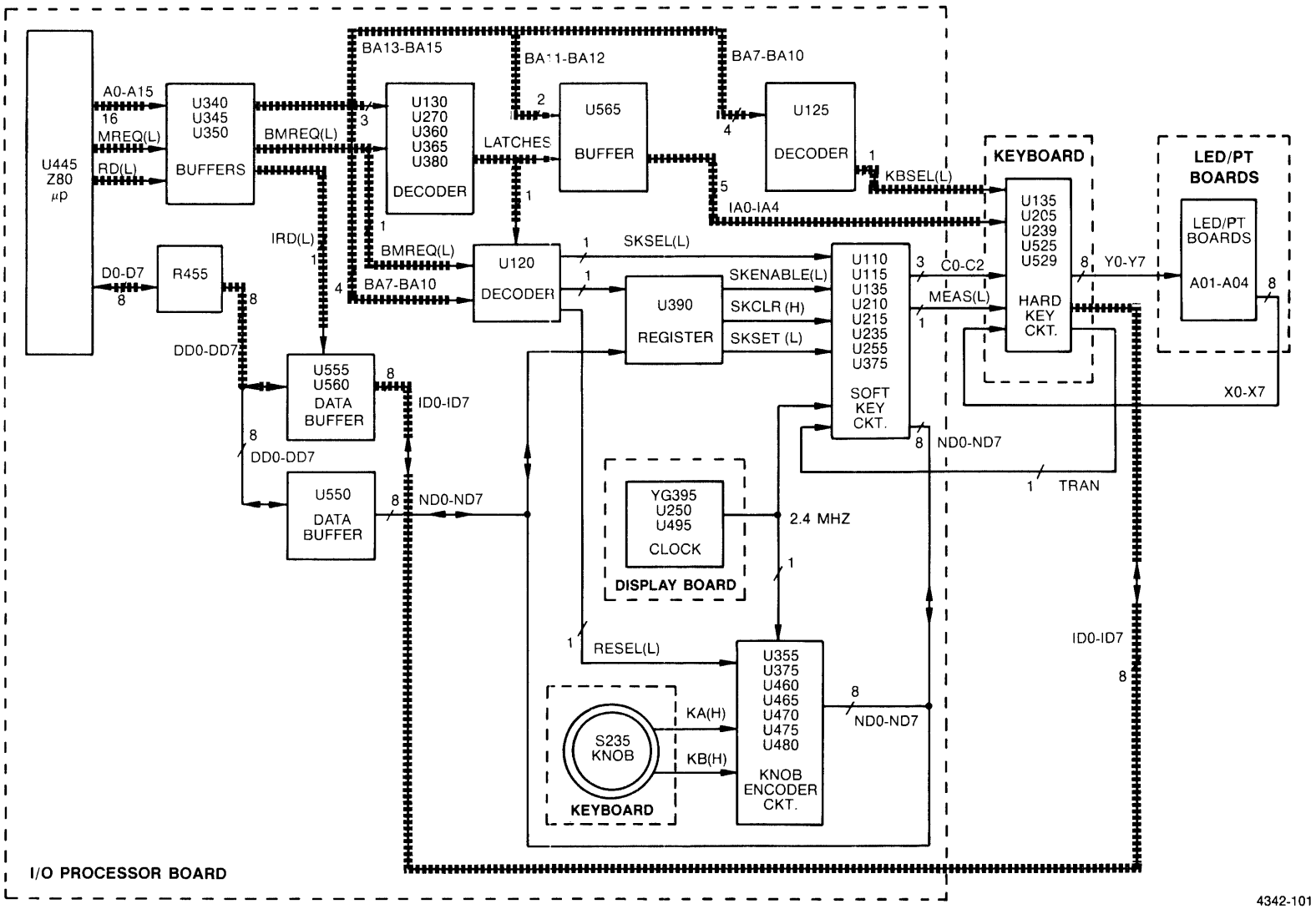


Figure 8-41. Frontpanel HARD KEYS block diagram.

KEYBOARD – COMPONENT LOCATION

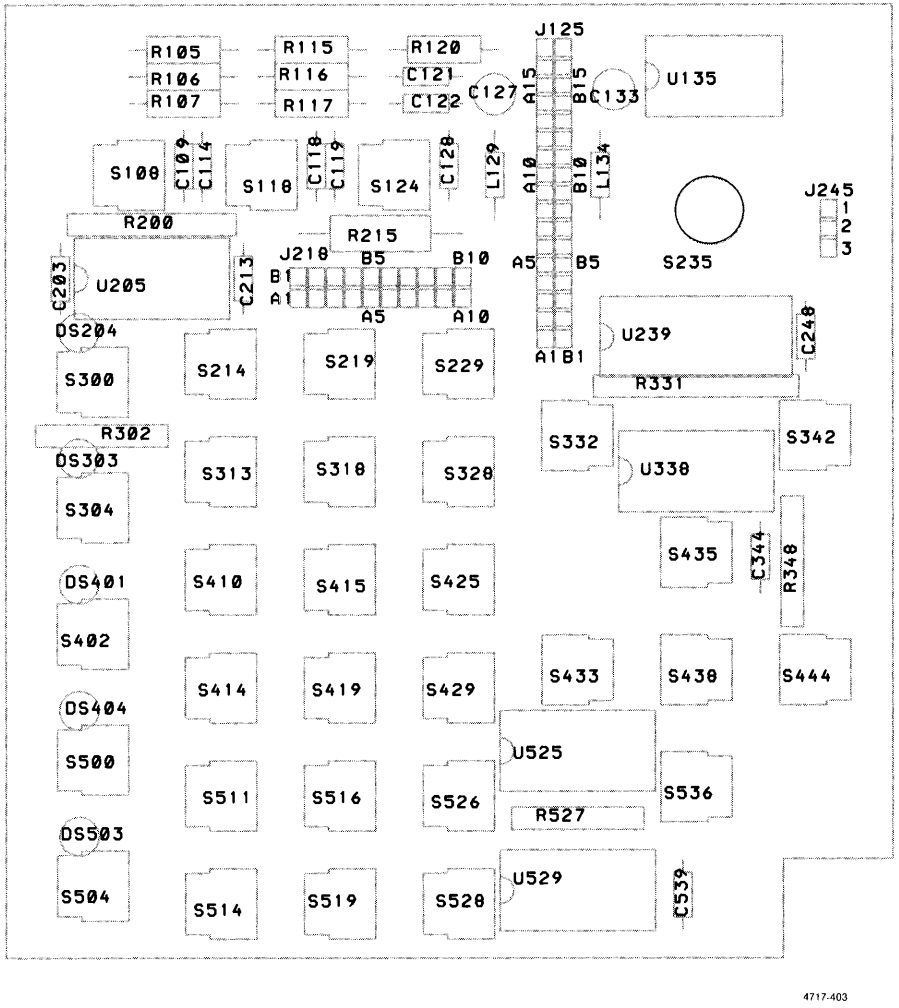


Figure 8-42. Keyboard Board component location.

module: FRONTPANEL
area: HARD KEYS

HARD KEYS AREA – CIRCUIT OVERVIEW

The hard key circuitry is indicated by the shaded path on the block diagram. (The shading indicates circuitry exercised for the first time during diagnostic testing.) The Z80 microprocessor and control circuitry located on the I/O Processor Board supplies the necessary address and control lines to scan the keyboard. The Z80 reads back data from the hard keys through the keyboard readback buffer A5U239 and data buffer A10U560.

HARD KEYS AREA – TEST DESCRIPTION

2111

The keyboard hard keys are scanned to check for any pressed or stuck front panel keys. The tests begin by checking address $ACEF_{hex}$. If anything but FF_{hex} is read back (indicating a key is pressed), an error is displayed on the 1240 screen. Next, addresses $ACF7_{hex}$, $ACFB_{hex}$, $ACFD_{hex}$, and $ACFE_{hex}$ are checked in sequence for the FF_{hex} read back values.

ROUTINE 1 DESCRIPTION

The routine checks hard key address $ACEF_{hex}$ for any pressed hard key. If anything but FF_{hex} is read back, an error is displayed.

2111 Error Index

Explanation: Data other than FF_{hex} was read back from $ACEF_{hex}$.

Probable Cause	Action
One or more keys stuck.	If actual data on screen is FE_{hex}, then the Select down-arrow key is probably stuck. Clear the stuck key.
Bad address decoders.	Suspect A10U380-10, A10U130-5, or A10U125-14.
Bad address or data buffer.	Suspect A5U135, A5U239, or A10U560.

ROUTINE 2 DESCRIPTION

The routine checks hard key address ACF7$_{hex}$ for any pressed hard keys. If anything but FF$_{hex}$ is read back, an error is displayed.

2121–2128 Error Indexes

Explanation: Data other than FF$_{hex}$ was read back from ACF7$_{hex}$.

Probable Cause	Action
One or more keys stuck.	Determine from table below if the actual data reported is a valid key. If the data is valid, check the appropriate key. If the data is not valid, then check the other possible causes.
Bad address or data buffer.	Suspect A5U135, A5U239, or A10U560.

Error Index	Actual Data	Key
2121	FE	START
2122	FD	STOP
2123	FB	AUTO
2124	F7	NEXT
2125	EF	↑ (select)
2126	DF	↑ (cursor)
2127	BF	← (cursor)
2128	7F	→ (cursor)

ROUTINE 3 DESCRIPTION

The routine checks hard key address ACFB$_{hex}$ for any pressed hard keys. If anything but FF$_{hex}$ is read back, an error is displayed.

2131–2138 Error Indexes

Explanation: Data other than FF$_{hex}$ was read back from ACFB$_{hex}$.

Probable Cause	Action
One or more keys stuck.	Determine from table below if the actual data reported is a valid key. If the data is valid, check the appropriate key. If the data is not valid, then check the other possible causes.
Bad address or data buffer.	Suspect A5U135, A5U239, or A10U560.

Error Index	Actual Data	Key
2131	FE	E
2132	FD	F
2133	FB	B
2134	F7	8
2135	EF	C
2136	DF	9
2137	BF	5
2138	7F	6

ROUTINE 4 DESCRIPTION

The routine checks hard key address $ACFD_{hex}$ for any pressed hard keys. If anything but FF_{hex} is read back, an error is displayed.

2141–2148 Error Indexes

Explanation: Data other than FF_{hex} was read back from $ACFD_{hex}$.

Probable Cause	Action
One or more keys stuck.	Determine from table below if the actual data reported is a valid key. If the data is valid, check the appropriate key. If the data is not valid, then check the other possible causes.
Bad address or data buffer.	Suspect A5U135, A5U239, or A10U560.

Error Index	Actual Data	Key
2141	FE	D
2142	FD	A
2143	FB	7
2144	F7	4
2145	EF	↓ (cursor)
2146	DF	1
2147	BF	2
2148	7F	3

ROUTINE 5 DESCRIPTION

The routine checks hard key address ACFE$_{hex}$ for any pressed hard keys. If anything but FF$_{hex}$ is read back, an error is displayed.

2151–2158 Error Indexes

Explanation: Data other than FF$_{hex}$ was read back from ACFE$_{hex}$.

Probable Cause	Action
One or more keys stuck.	Determine from table below if the actual data reported is a valid key. If the data is valid, check the appropriate key. If the data is not valid, then check the other possible causes.
Bad address or data buffer.	Suspect A5U135, A5U239, or A10U560.

Error Index	Actual Data	Key
2151	FE	CONFIG
2152	FD	TRIG
2153	FB	DATA
2154	F7	EDIT
2155	EF	UTILITY
2156	DF	GLITCH
2157	BF	0
2158	7F	DON'T CARE

FRONTPANEL BLOCK DIAGRAM
SOFT KEYS – AREA 2

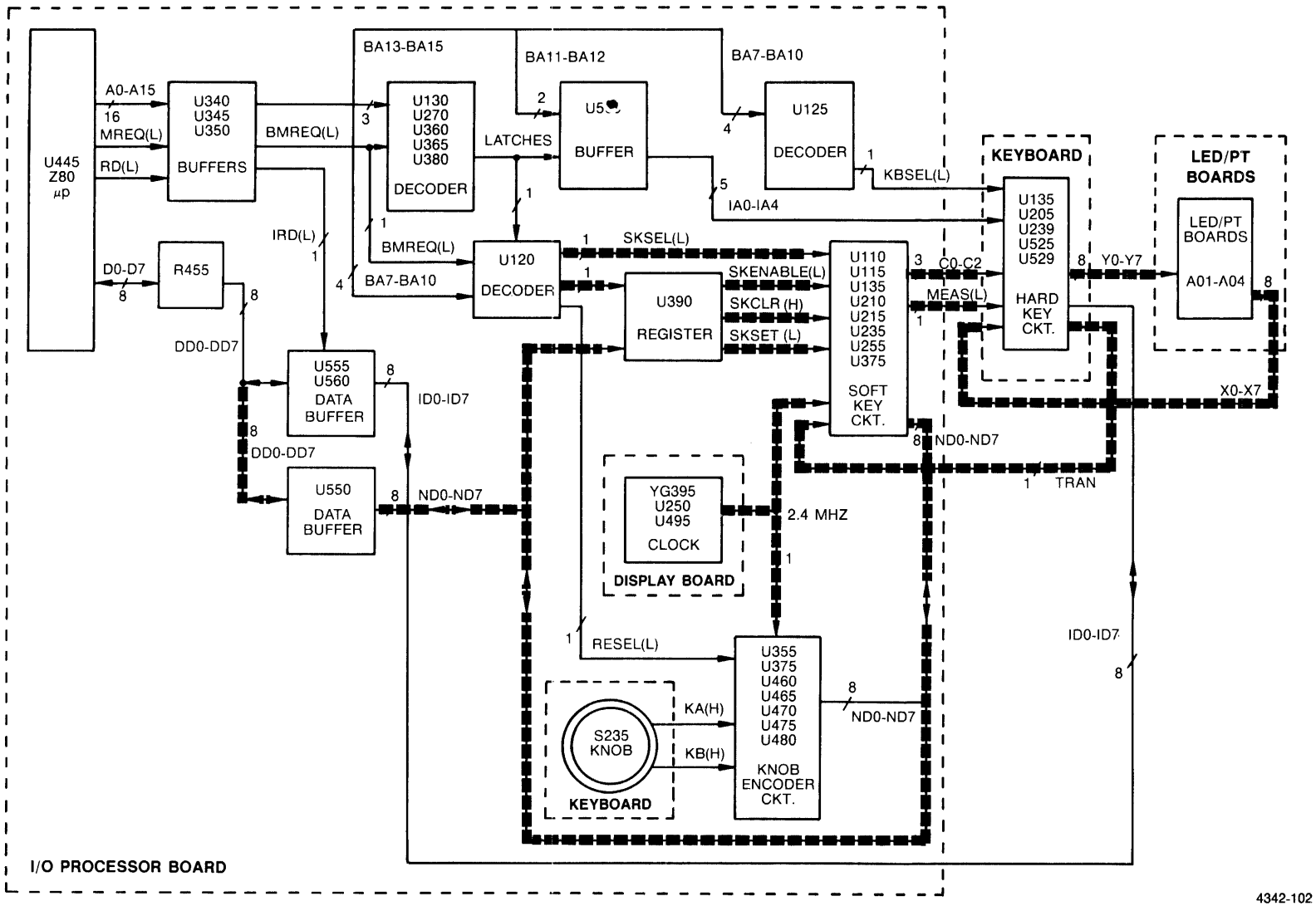


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Figure 8-43. Frontpanel SOFT KEYS block diagram.

I/O PROCESSOR BOARD – COMPONENT LOCATION

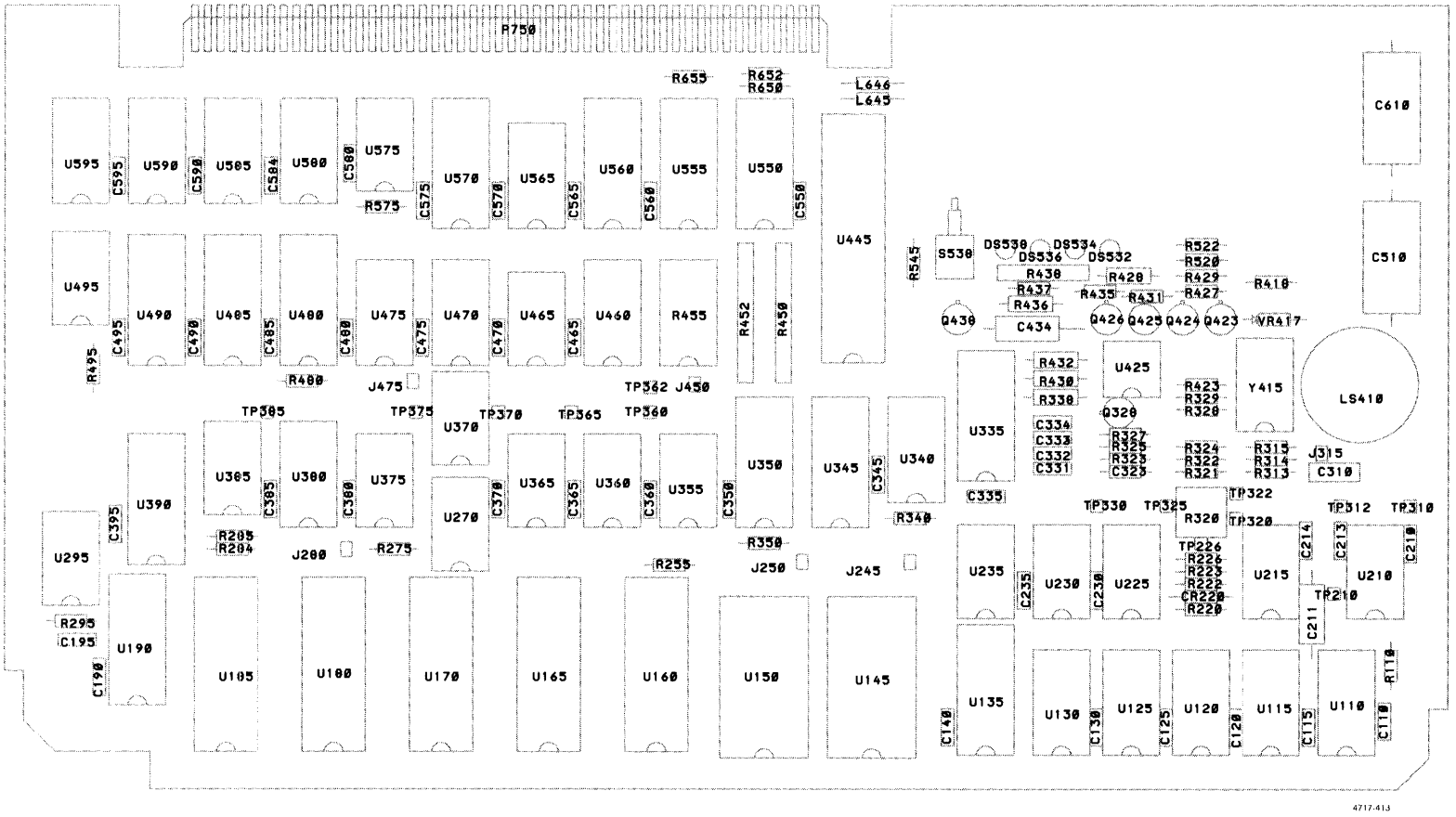

Figure 8-44. I/O Processor Board component location.

module: FRONTPANEL
area: SOFT KEYS

SOFT KEY AREA – CIRCUIT OVERVIEW

The Soft Key circuitry is indicated by the shaded path on the block diagram. (The shading indicates circuitry exercised for the first time during diagnostic testing.) This circuitry converts the soft key information (detected by the LED/Phototransistor boards) into an equivalent binary code. This code is used by the I/O Processor to determine if a soft key has been activated.

The multiplexed TRAN(H) signal at A10TP312 from the keyboard contains the status of seven phototransistors on the PT1 and PT2 phototransistor boards. This information is fed to the sample and hold circuit, A10U210. The sample and hold I.C. first samples the phototransistor ambient light output, then holds this level at its output. Next, the phototransistor is turned on (strobed). The two phototransistor readings are fed to a 50X multiplier, A10U215C. Here, the difference between the ambient light and the ambient light plus the infrared light is multiplied, producing a high-going output pulse. If one of the soft keys was being touched, only ambient light output levels would be present for both inputs to the muiltiplier. The multiplier would therefore have no output pulse, indicating the activation of that soft key.

Multiplier output pulses available at A10TP322 are integrated in A10U215B. The soft key adjustment, A10R320, controls the integrator input dc bias to set input sensitivity. An analog switch, A10U110, shorts out the integrating capacitor, A10C211, to restart the next integrating ramp at a zero-volt threshold. Comparator A10U215A shapes the ramp into a TTL-level pulse for the shift register A10U235. The seven states (plus one false state produced by the multiplexer at A05U205-4) describing the condition of each soft key box are latched by A10U135. The SKSEL(L) line enables the data onto the ND data bus.

Soft key signal lines SKCLR(L) and SKSET(L) are used only during diagnostic tests to verify the shift register and latch operation.

SOFT KEY AREA – TEST DESCRIPTION

The tests begin by scanning the soft keys to determine if any keys are being touched. The test reads address $AB00_{hex}$ (A10U135) 50 times and, if the test reads some value other than FE_{hex} ten times in a row, that key code is reported as an error. If the test does not see the same key code ten times in a row, then the displayed error index is incremented from 2211 to 2212.

Next, the test scans the soft keys after disabling them. This causes all soft keys to appear to be activated (i.e., touched). The test reads address $AB00_{hex}$ 50 times and, if anything other than 00_{hex} is read ten times in a row, then that key code is reported as an error.

In the event that an on-screen soft key failure occurs, the diagnostics may appear to be inoperable. To circumvent this function failure, the diagnostics will duplicate the function of the soft keys on the front-panel keyboard when it detects a soft key failure during the power-up diagnostics. The 0 through 9 keys represent the on-screen soft keys, as shown by Figure 8-11.

If a soft key failure is detected at power-up, the ENTER NORMAL OPERATION soft key will not work until the problem is corrected. Once the diagnostics successfully pass that error during power-up, that soft key operates normally.

NOTE

Hard key number 4 allows a bypass of the inoperable ENTER NORMAL OPERATION soft key.

ROUTINE 1 DESCRIPTION

This test reads the soft key address AB00$_{hex}$ 50 times. If the test detects any key code other than FE$_{hex}$ ten times in a row, that keycode is reported as an error.

2211 Error Index

Explanation: The data read at soft key address AB00$_{hex}$ was not FE$_{hex}$.

Probable Cause	Action
Faulty LED or phototransistor.	Refer to table below and replace as necessary.

Valid Keycodes

Top Row:	BC - BA - B6 - AE - 9E
Bottom Row:	7C - 7A - 76 - 6E - 5E
No Key Pressed:	FE

2212 Error Index

Explanation: The test could not read the same value 10 times at address AB00$_{hex}$.

Probable Cause	Action
Hardware for soft keys on front panel or I/O Processor defective.	Refer to *Soft Key Troubleshooting.*

ROUTINE 2 DESCRIPTION

This test scans the soft keys after disabling them. This causes all soft keys to appear to be activated (i.e., touched). The test reads address AB00$_{hex}$ 50 times and, if anything other than 00$_{hex}$ is read ten times in a row, that key code is reported as an error.

2221 Error Index

2221

Explanation: The data read at soft key address was not 00$_{hex}$.

Probable Cause	Action
Faulty phototransistor or associated circuitry.	Refer to table below and replace as necessary.

Valid Keycodes

Top Row:	BC - BA - B6 - AE - 9E
Bottom Row:	7C - 7A - 76 - 6E - 5E
No Key Pressed:	FE

FRONTPANEL BLOCK DIAGRAM
KNOB – AREA 3

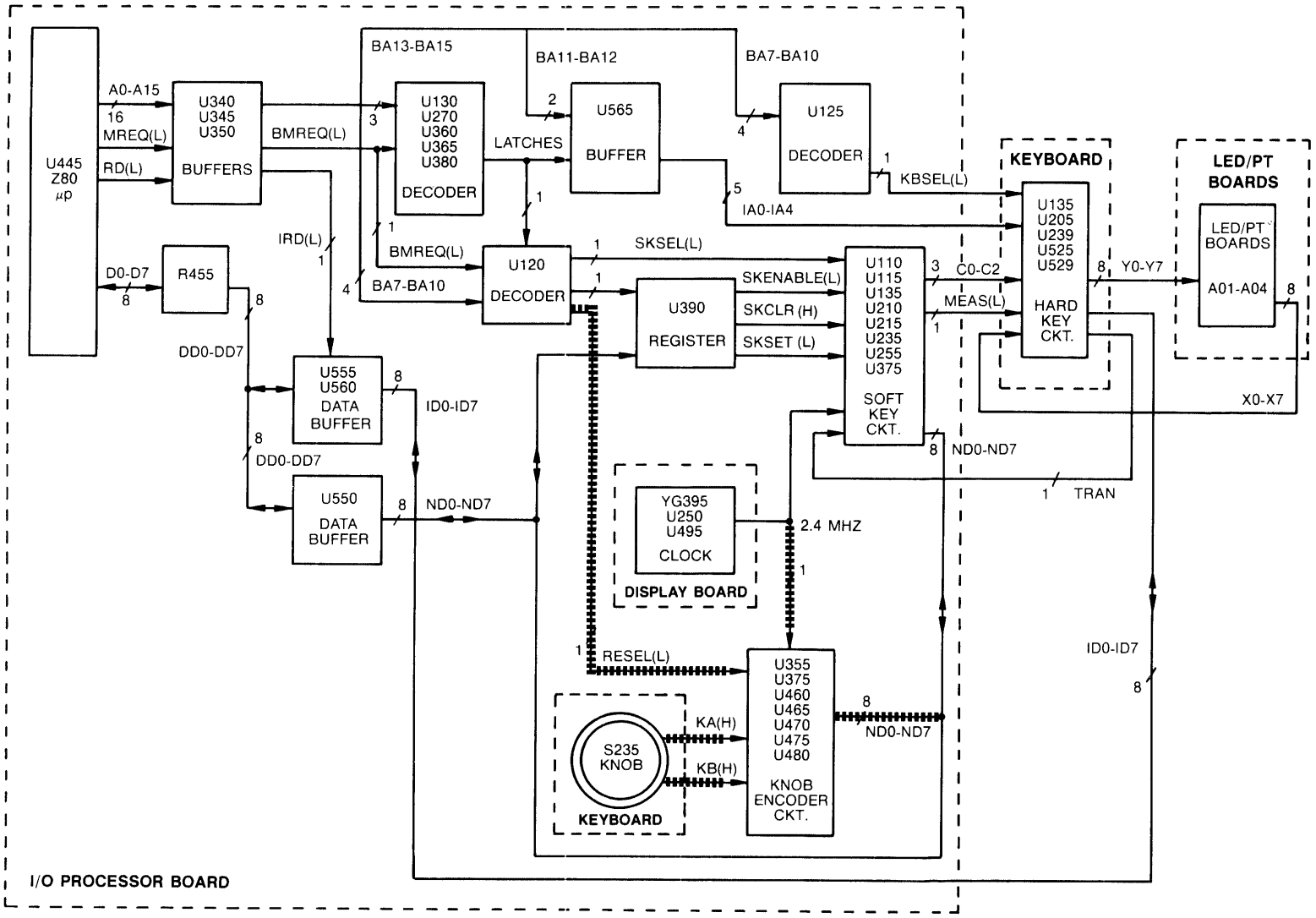

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Figure 8-45. Frontpanel KNOB block diagram.

I/O PROCESSOR BOARD – COMPONENT LOCATION

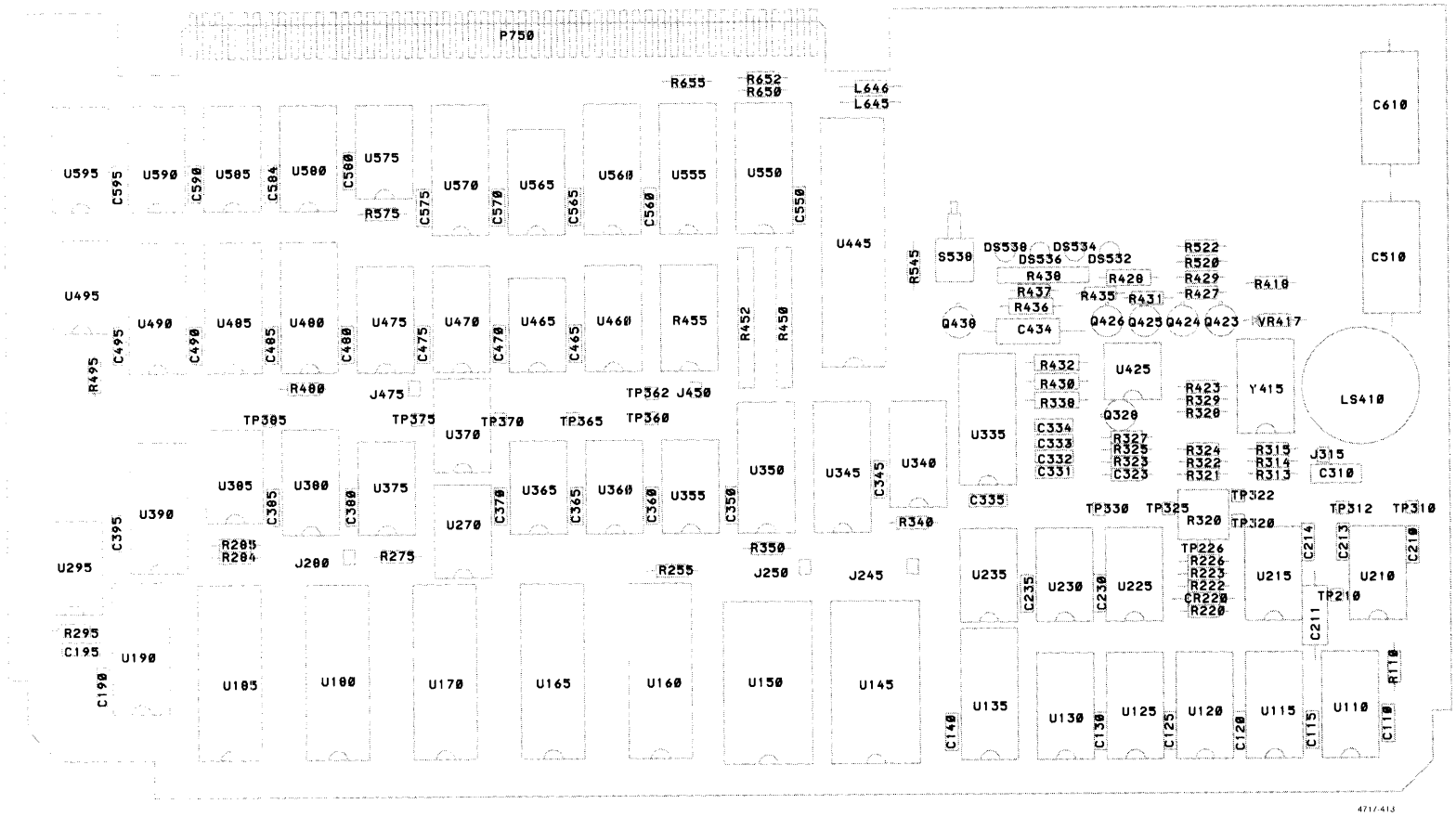

Figure 8-46. I/O Processor Board component location.

module: FRONTPANEL
area: KNOB

KNOB AREA – CIRCUIT OVERVIEW

The pattern-shaded signal lines on the knob circuitry block diagram indicate circuitry used during diagnostic testing. Only the circuitry that is being exercised for the first time during diagnostic testing is shown. Circuitry exercised by other diagnostic tests are shown in their respective block diagrams.

The knob circuitry converts the rotational movement of the front panel rotary knob into an equivalent Gray code. This code is used by the I/O Processor firmware to determine incremental value changes corresponding to knob movement.

2310
2311

The front panel knob outputs a two-bit Gray code on the KA(H) and KB(H) lines. A10U460, U465, and U375B produce the up (high signal)/down (low signal) count at A10TP375 and the clocking signal for every pulse edge at A10TP370. The four-bit up/down counters A10U470 and U475 decode the knob's clockwise movement as a count up and the counter-clockwise movement as a count down. The rotary encoder select signal line, RESEL(L), enables the data onto the ND data bus through buffer A10U480.

KNOB AREA – TEST DESCRIPTION

The knob test begins by reading the knob counter value at address $AAFF_{hex}$. The current counter value is saved, and the test waits for two 60 Hz interrupts. When the interrupts have occurred, the knob counter is read once more. The second counter value is subtracted from the first. The results should be a value of zero.

2310 Error Index

Explanation: No 60 Hz interrupts were detected.

Probable Cause	Action
The 60 Hz interrupt is defective.	Run the INTERRUPT area test in the I/O Processor module.

2311 Error Index

Explanation: The subtraction of the two counter values did not result in zero.

Probable Cause	Action
Suspect knob, A10U355, U370, U375, U460, U465, U470, U475, or U480.	Loop on this test and, while rotating the knob, check A10U480-1 and -19 for low-going pulses. Check U470-15 for carry out, check U470-2 and U475-2 for clock. Also use the manual test found in the FRONTPANEL module, FP VERIFY area, Routine 1.

module: FRONTPANEL
area: FP VERIFY

FRONTPANEL VERIFY MANUAL TEST DESCRIPTION

The FP VERIFY area manual test contains two routines that help the technician troubleshoot the 1240 front-panel circuits. Routine 1 produces a screen display that represents the 1240 hard keyboard and knob. With this display, the front-panel key and knob action can be visually verified. Routine 2 produces a screen display that represents each soft key as a box. This display allows you to verify soft key action.

ROUTINE 1 DESCRIPTION

This is a manual test for the hard keyboard and the front-panel knob to help troubleshoot their respective circuits. A screen display (shown in Figure 5-3) is a graphic representation of the front-panel keyboard. When a hard key is pressed, the corresponding screen key (and no other key on the screen) should disappear. When the key is released, the display for that key should return. By touching the keys, the technician can activate keyboard circuitry and check the results within the circuitry.

A circle of 20 dots in the upper-right corner of the keyboard screen display represents one revolution of the knob. The knob counter value is displayed in the center of the circle. One revolution of the knob is 200 counts ($C8_{hex}$) on the counter. The counter's total range is 0 to 256 (00_{hex} to FF_{hex}).

To obtain the keyboard/knob screen display, use the following steps:

1. Enter the diagnostics by simulating a keyboard failure (hold down a key during power-up).
2. Using the Select keys or the Knob, choose the FRONTPANEL module and touch the MODULE DIAGNOSTIC soft key.
3. Select the FP VERIFY area and touch the AREA DIAGNOSTIC soft key.
4. Select routine 1 and press the START key.

Keyboard Error Description: The front-panel screen display did not show the proper response when a key was pressed.

Probable Cause	Action
Bad address or data buffer.	Suspect A5U135, A5U239, or A10U560.

Knob Error Description: The asterisk on the knob display did not move as the knob was being turned, or the counter value did not change as the knob was turned.

Probable Cause	Action
Knob counter cannot be read correctly or knob does not increment/decrement counter correctly.	Suspect knob, A10U355, U370, U375, U460, U465, U470, U475, or U480. Loop on this test while rotating knob and check A10U480-1 and -19 for low-going pulses. Also check A10U470-15 for carry out, and check U470-2 and U475-2 for clock.

ROUTINE 2 DESCRIPTION

This is a manual test for the soft keys to help troubleshoot the soft key circuits. A screen display (shown in Figure 5-8) represents each soft key as a box. By touching each soft-key box, the technician may activate any desired soft key (indicated by a highlighted box) and check the results within the soft key circuitry. To obtain the soft key screen display, use the following steps:

1. Enter the diagnostics by simulating a keyboard failure (hold down a key during power-up).
2. Select the FRONTPANEL module and touch the MODULE DIAGNOSTIC soft key.
3. Select the FP VERIFY area and touch the AREA DIAGNOSTIC soft key.
4. Select routine 2 and press the START key.

Soft Key Error Description: The wrong soft key (or no soft key) is lighted when the screen-display soft key is touched.

Probable Cause	Action
Faulty phototransistors or associated circuitry.	Refer to *Soft Key Troubleshooting* for circuit waveforms.

3XXX DISPLAY ERROR INDEXES

Error Index	Area Name	Area Number
31XX	RAM	AREA 1
32XX	VSCROLL	AREA 2
33XX	HSCROLL	AREA 3
34XX	RVIDEO	AREA 4
35XX	HIGHLIGHT	AREA 5
36XX	WAVEFORM	AREA 6

DISPLAY BLOCK DIAGRAM
RAM – AREA 1

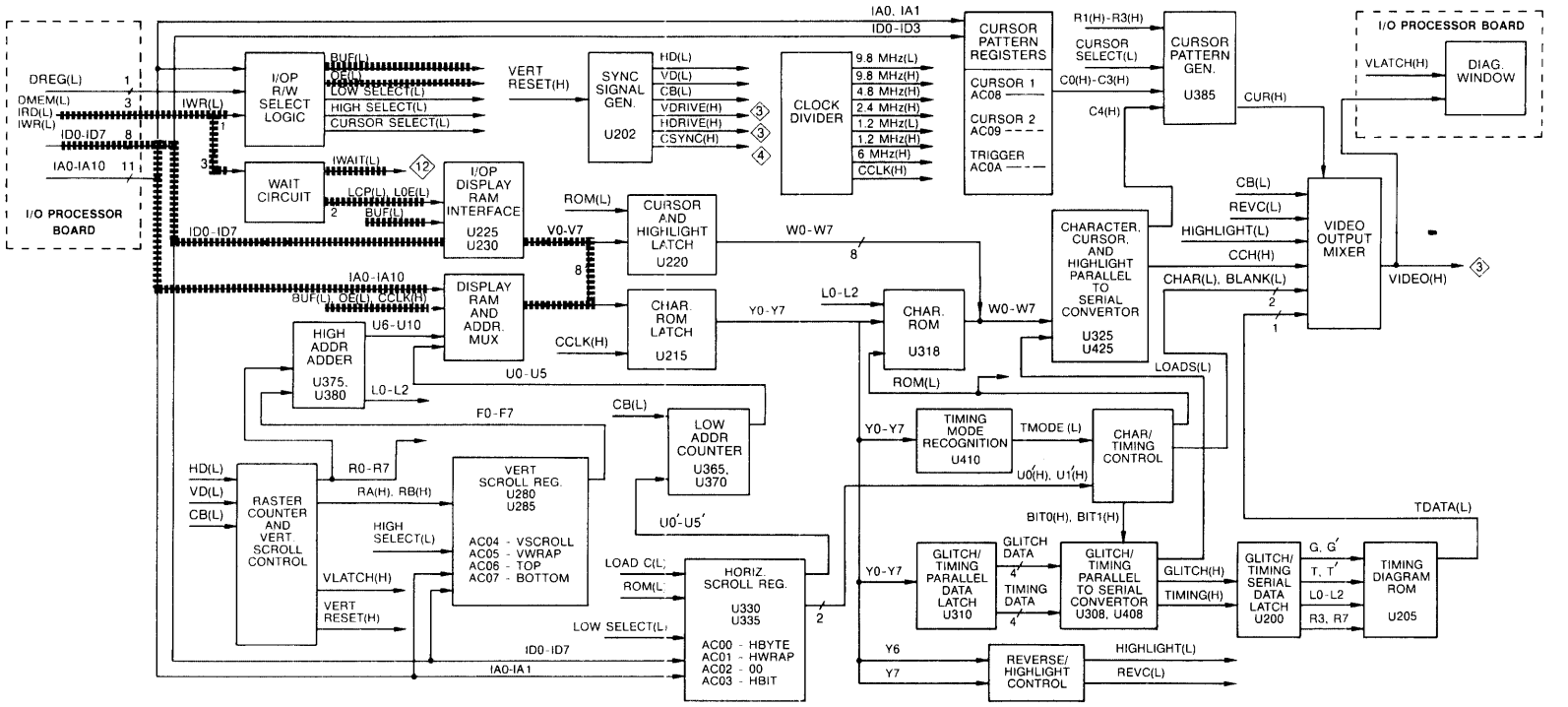

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Figure 8-47. Display RAM block diagram.

DISPLAY BOARD – COMPONENT LOCATION

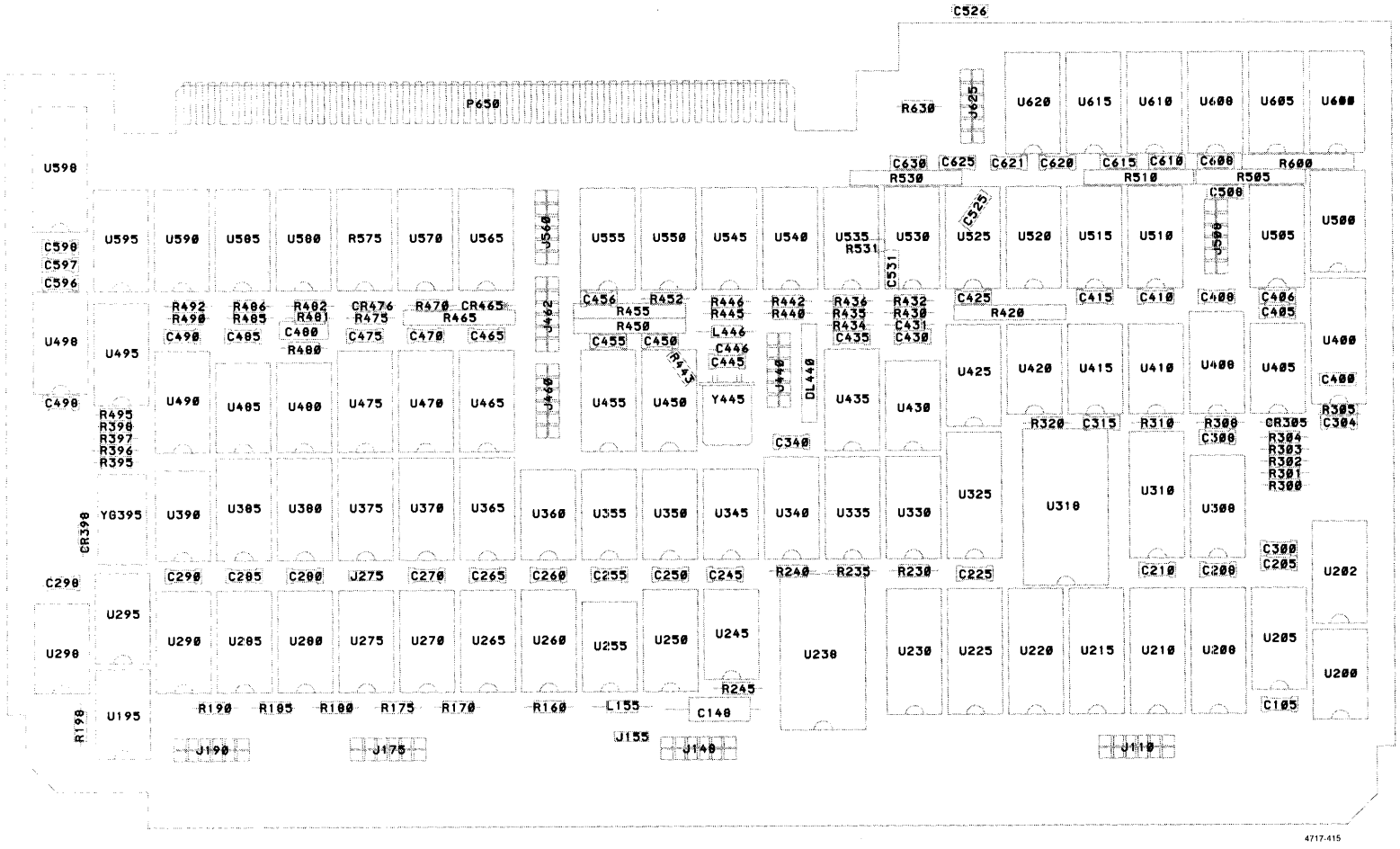

Figure 8-48. Display Board component location.

module: DISPLAY
area: RAM

DISPLAY RAM AREA – CIRCUIT OVERVIEW

The pattern-shaded signal lines on the Display RAM block diagram indicate circuitry used during diagnostic testing. Only the circuitry that is being exercised for the first time during diagnostic testing is shown. Circuitry exercised by other diagnostic tests are shown in their respective block diagrams.

The Display RAM, A11U238, provides temporary storage of four types of data: character data, timing/glitch data, timing mode highlighting data, and timing mode cursor position data. Display RAM accessing occurs according to an 800 ns-per-character cycle time. During the first 400 ns, the address multiplexers A11U265, U270, and U275 allow the I/O Processor to address the Display RAM on address lines A0-A10. The RAM then stores screen display data sent from the I/O Processor through the I/O Processor-Display RAM Interface. The remaining 400 ns of the cycle is split into two halves. During the second 400 ns of the cycle, the address multiplexers pass the addresses formed by the Low Address Counters and the High Address Adder. The first 200 ns period is used to output character or timing/glitch data sent from the Display RAM. The data is latched by A11U215 on the rising edge of CCLK(H). The second 200 ns period is used to output cursor position and highlight data and is latched by the falling edge of CCLK(H) (actually 1.2 MHZ(L)'s rising edge).

The Wait Circuit monitors the I/O Processor's IRD(L) read signal, IWR(L) write signal, and DMEM(L) display memory signals to determine when the I/O Processor should access the Display RAM. The circuit produces LCP(L) and LOE(L) that control the I/O Processor-Display RAM Interface. It also generates the IWAIT(L) signal to the I/O Processor's Z80, forcing it to wait for the appropriate access time.

The I/O P- R/W Select Logic also generates control signals used when accessing the Display RAM. BUF(L), OE(L), LOE(L), and LCP(H) control data transmission for the Display RAM A11U238 and the I/O Processor-Display RAM Interface. The interface, formed by A11U225 and U230, provides a communication link between the I/O Processor's ID data bus and the Display RAM's V data bus. The I/O Processor uses this link when transferring screen images or diagnostic data to and from the Display RAM.

DISPLAY RAM AREA – TEST DESCRIPTION

Since the Display RAM has all of the current screen data in it, its contents must be saved before the Display RAM test is run. The 2K of data in the Display RAM is moved to the system RAM at locations $B350_{hex}$ through $BB50_{hex}$.

The pattern AA_{hex} is written to all locations being tested ($A000_{hex}$-$A7FF_{hex}$). The first location is read and checked for AA_{hex}. If it contains AA_{hex}, CC_{hex} is written to that location. If it does not contain AA_{hex}, the value read is reported as an error. This sequence is repeated for each RAM location under test. After the first read/write pass has been completed, all of the RAM under test should contain CC_{hex}.

The first location is then read and checked for CC_{hex}. If it contains CC_{hex}, it is filled with $F0_{hex}$. If it does not contain CC_{hex}, the value read is reported as an error. This sequence is repeated for each RAM location under test. After this read/write pass has been completed, all of the RAM under test should contain $F0_{hex}$.

The test will run one more pass as previously described. The first location is read and checked for $F0_{hex}$. If it contains $F0_{hex}$, then $0F_{hex}$ is written to that location. If it does not contain $F0_{hex}$, the value read is reported as an error. This sequence is repeated for each RAM location under test. When this has been done, all of the RAM under test should contain $0F_{hex}$.

The last pass of the test reads each location of the RAM under test, in reverse order, starting with the last location. If any location does not contain $0F_{hex}$, the value read is reported as an error.

The final portion of the test restores to the Dynamic RAM the 2K of screen data that was saved at location $B350_{hex}$ in the system RAM.

3111 Error Index

Explanation: The data read back was not correct.

Probable Cause	Action
Bad Display RAM.	Suspect the Display RAM A11U238.
Bad I/O Processor-Display RAM Interface.	Suspect A11U225 or U230.
The Display RAM Address Multiplexer is not working correctly.	Suspect A11U265, U270, or U275.
One or more of the 8 data lines from the Display RAM to the I/O Processor--Display RAM Interface may be open or shorted together.	Power down the instrument. Using an ohm meter, check for continuity of data lines between the two points.
One or more of the 11 address lines from the Display RAM to the RAM Address Multiplexer may be open or shorted together (possibly indicated by a screen full of random characters).	Power down the instrument. Using an ohm meter, check for continuity of address lines between the two points.

DISPLAY BLOCK DIAGRAM
VERTICAL SCROLLING – AREA 2

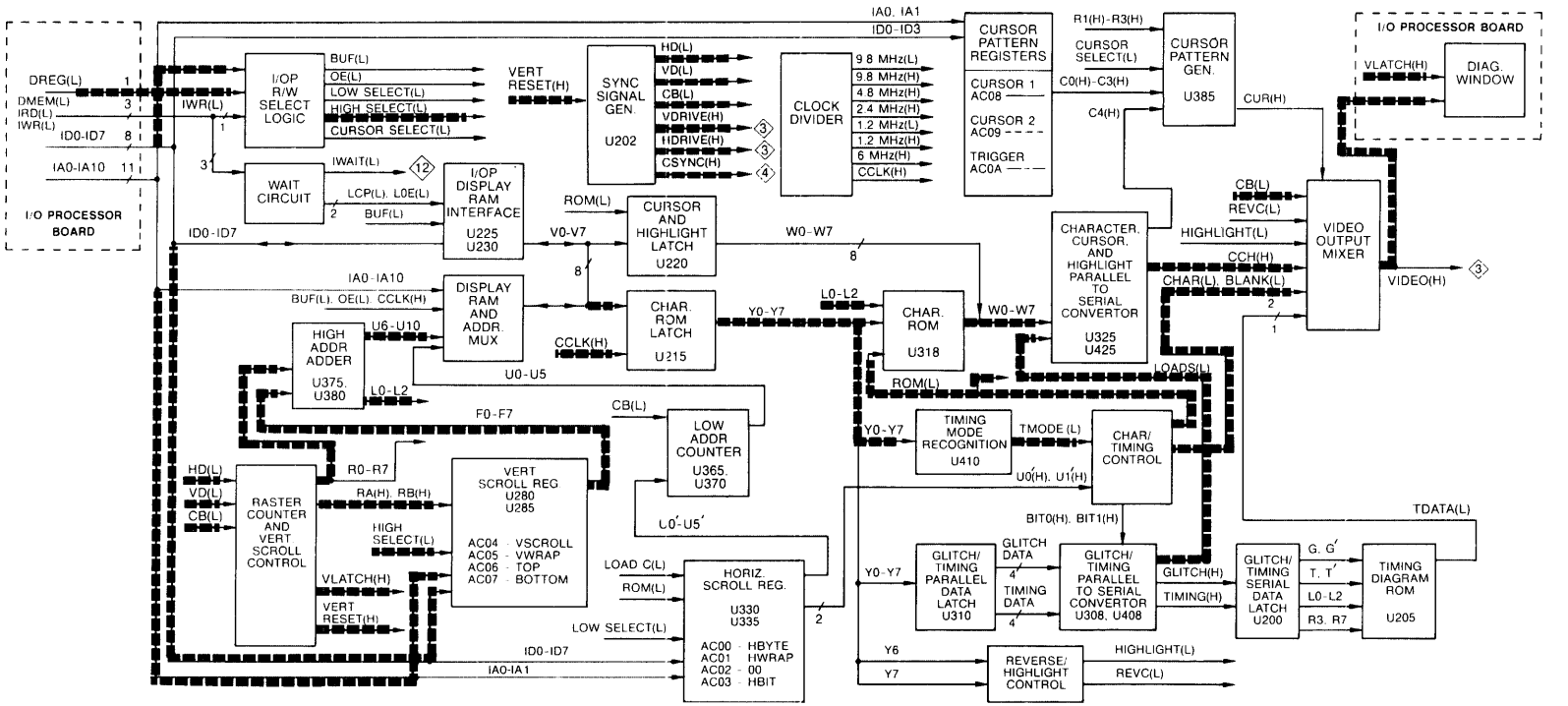

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Figure 8-49. Display VERTICAL SCROLLING block diagram.

DISPLAY BOARD – COMPONENT LOCATION

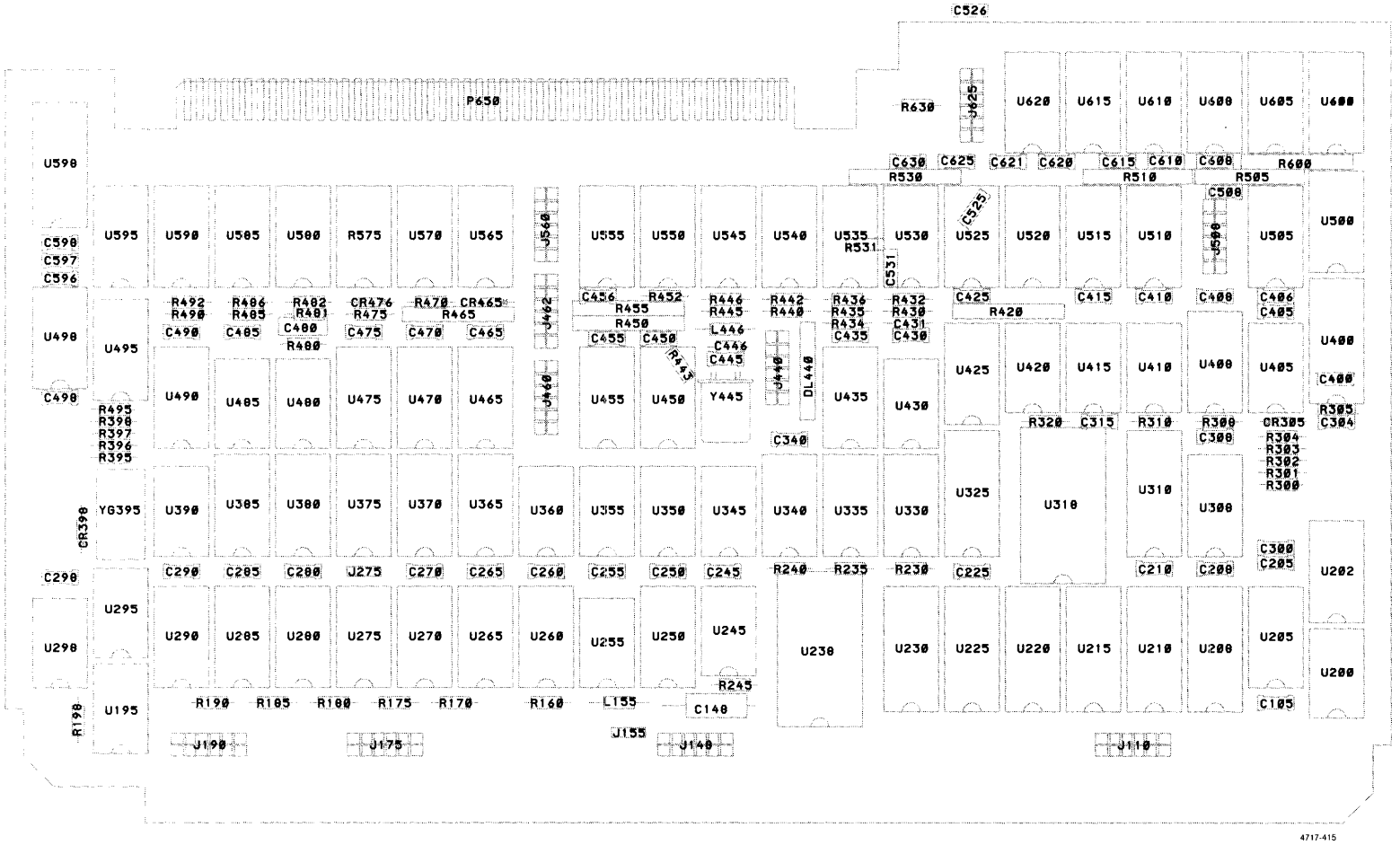


Figure 8-50. Display Board component location.

module: DISPLAY
area: VSCROLL

VERTICAL SCROLLING AREA – CIRCUIT OVERVIEW

The pattern-shaded signal lines on the vertical scrolling block diagram indicate circuitry used during diagnostic testing. Only the circuitry that is being exercised for the first time during diagnostic testing is shown. Circuitry exercised by other diagnostic tests are shown in their respective block diagrams.

The vertical scrolling circuitry is basically comprised of the vertical scrolling registers, Display RAM addressing circuitry, and Character ROM circuitry. Since vertical scrolling is only possible during text and state table displays, the Character ROM supplies any needed characters used during these operations (the Timing Diagram ROM is disabled).

The Vertical Scrolling Registers, A11U285 and U280, contain an offset value that is used to determine the portion of Display RAM to be read for vertical scrolling data. This offset value, sent by the I/O Processor on ID0(H)-ID7(H), is used by the High Address Adder to calculate the Display RAM's upper five address bits. These five address bits determine which of the 30 screen lines are being output. The information on lines 11-25 may be shifted up or down by controlling the Display RAM addresses, thereby producing the vertical scrolling action.

A Raster Counter, A11U195, tracks the output of raster lines for the display screen (240 raster lines per screen). The CB(L) composite blank signal from the Sync Signal Generator clocks this dual 4-bit counter, outputting the raster count on R0(H)-R7(H).

The High Address Adder forms the upper addresses A6(H)-A10(H) of the Display RAM from 1) the current raster line count, and 2) any offset value held in the Vertical Scrolling Register. These addresses specify the portion of Display RAM to be output. The High Address Adder also produces L0(H)-L2(H) for the Character ROM, indicating which of the eight raster rows for each character is to be output.

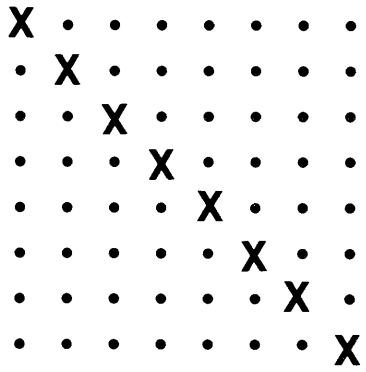
The Character ROM, A11U318, is a 2K X 8-bit, 2716-type EPROM containing two 64-character sets of text. The two character sets provide a total of 128 possible display characters. (The timing diagram characters are generated by the Timing Diagram ROM.) The output from the Character ROM is latched by A11U325 for the parallel-to-serial converter, A11U425. This shift register accepts text data from the Character ROM (or cursor/highlight data directly from the Display RAM) and converts it to serial data for the Video Output Mixer.

The Video Output Mixer combines the character, cursor, and timing diagram information with the appropriate type of video pattern. The resulting VIDEO(H) signal is sent to the CRT Drive Board and the I/O Processor's Video Readback (Diagnostic Window) circuitry. Diagnostics uses the screen readback circuitry to check a portion of the displayed video and verify that it is correct.

VERTICAL SCROLL AREA – TEST DESCRIPTION

The vertical scrolling circuitry is verified by scrolling a diagnostic character vertically through the diagnostic window, A10U295 and U190. The I/O Processor then reads back a portion of the displayed video from the diagnostic window to verify that it is correct.

The diagnostic window register is clocked by raster 200. Since it is an 8-bit shift register, it will contain the last 8 pixels that were sent to the video monitor before raster 200 occurred. (Raster 200 is the bottom pixel row of line 25.) The character scrolled through the window is a special diagnostic character. This character was selected because it supplies information that identifies which data line is bad in the character generation circuitry, or which bit is bad in the scrolling circuitry. A graphic representation of the diagnostic character being scrolled on an 8 X 8 matrix is shown in the following:



The diagnostic character is scrolled upward by writing an incrementing count to the VSCROLL and VWRAP registers in the Vertical Scrolling circuitry. As the character is scrolled, the value read back through the diagnostic window register appears to be shifted right after each pixel is scrolled up one position. The character is scrolled across the window once during power-up diagnostics, and 16 times during regular diagnostics.

3210 Error Index

Explanation: Before the diagnostic window register is read each time, a 60 Hz interrupt must occur. In this case, the 60 Hz interrupt did not occur and the diagnostic test was not run.

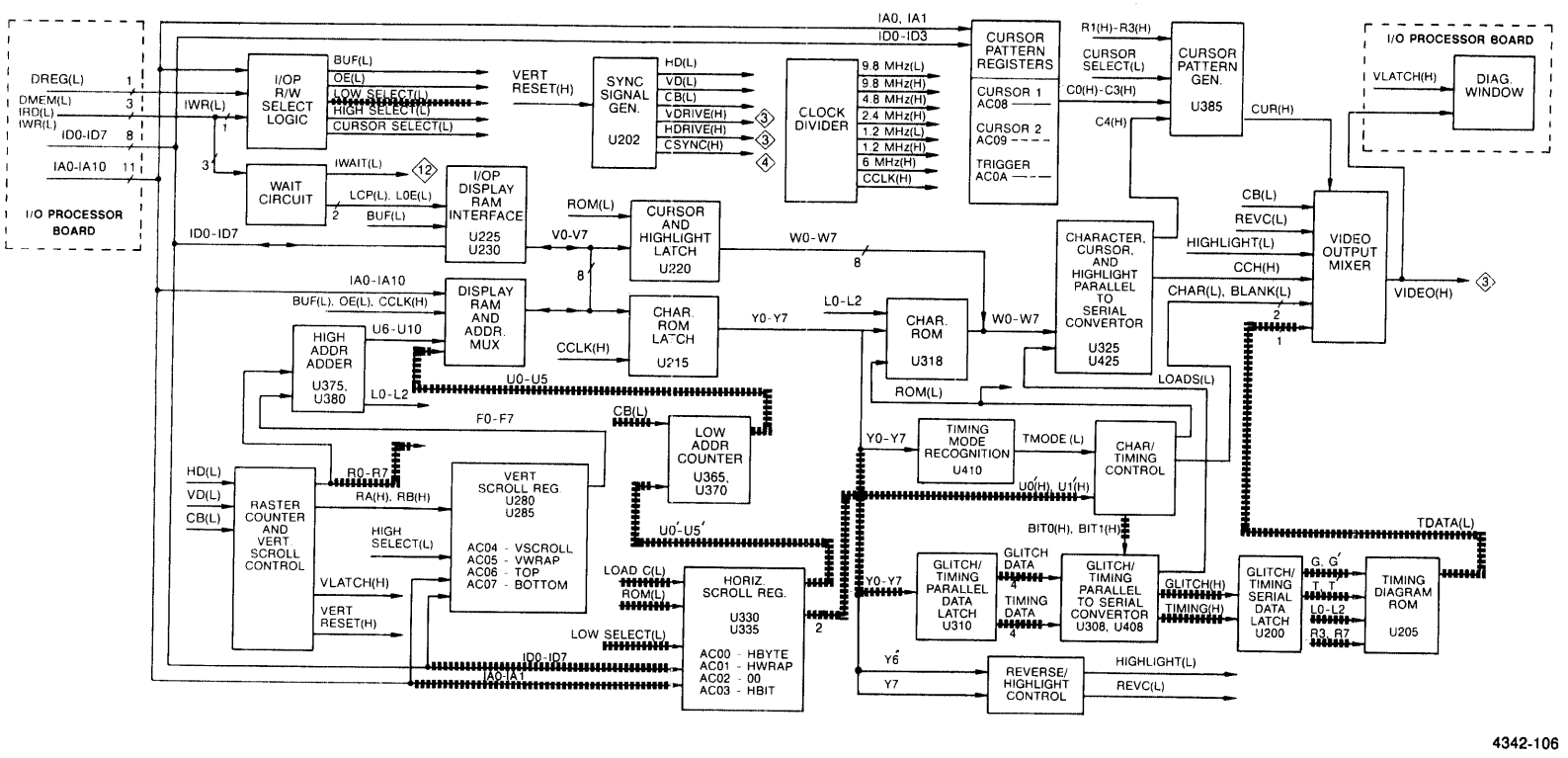
Probable Cause	Action
The 60 Hz interrupt is not working correctly.	Run the I/O Processor's INTERRUPT area diagnostic test to determine why the interrupt is not working. Since the INTERRUPT test has already been run before reaching this point, the failure is probably an intermittent one. Looping on the interrupt test may help find the error.

3211–321F Error Indexes

Explanation: While vertically scrolling the diagnostic character, an incorrect pattern was read back. The last digit of the error index (1 through F) represents the number of lines that were scrolled before the error (1 through F) was detected.

Probable Cause	Action
The Vertical Scrolling Registers are defective.	Suspect the Vertical Scrolling Registers A11U280 and U285.
The High Address Adder is defective.	Suspect the High Address Adder A11U375 and U380.
The Character ROM, the input latch, or the output latch is defective.	Suspect Character ROM A11U318, latch A11U215, or latch A11U325.
Bad Character, Cursor, and Highlight Parallel-To-Serial Convertor.	Suspect the convertor A11U425.

DISPLAY BLOCK DIAGRAM
HORIZONTAL SCROLLING – AREA 3



4342-106

Figure 8-51. Display HORIZONTAL SCROLLING block diagram.

DISPLAY BOARD – COMPONENT LOCATION

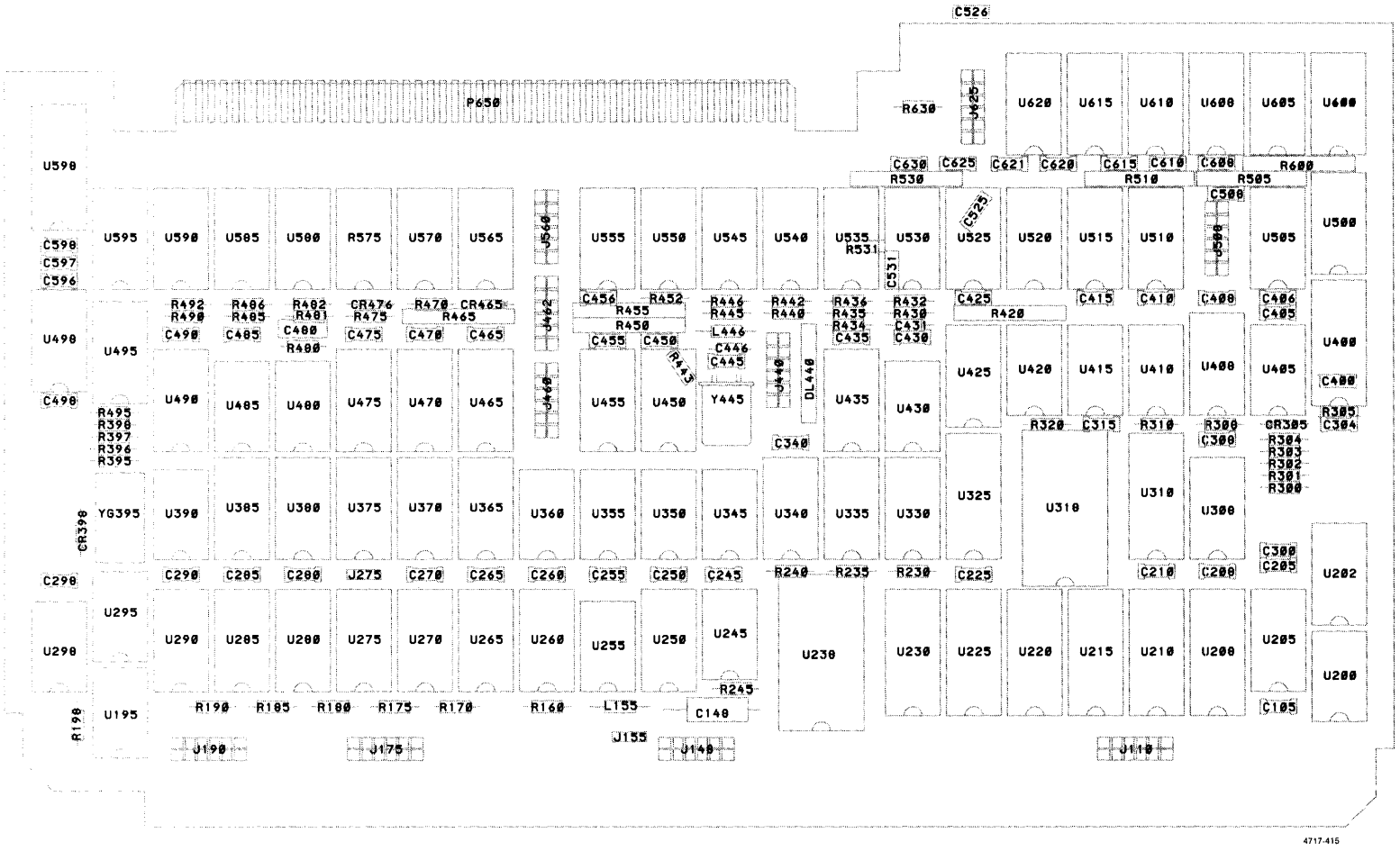


Figure 8-52. Display Board component location.

module: DISPLAY
area: HSCROLL

HORIZONTAL SCROLLING AREA – CIRCUIT OVERVIEW

The pattern-shaded signal lines on the horizontal scroll block diagram indicate circuitry used during diagnostic testing. Only the circuitry that is being exercised for the first time during diagnostic testing is shown. Circuitry exercised by other diagnostic tests are shown in their respective block diagrams.

The horizontal scrolling circuitry is basically comprised of the Horizontal Scrolling Registers, Display RAM addressing circuitry, and the Timing Diagram ROM circuitry. Since horizontal scrolling is only possible during timing diagram displays, the Timing Diagram ROM supplies any needed waveform characters used during these operations (the Character ROM is disabled).

The Horizontal Scrolling Registers, A11U330 and U335, contain an offset value that is used to determine the portion of Display RAM to be read for horizontal scrolling data. This offset value, sent by the I/O Processor on ID0(H)-ID7(H) to the Low Address Counter (A11U365 and U370), becomes the Display RAM's lower six address bits.

During basic text displays, the Display RAM's lower six bits determine which of the 64 characters in the screen line is being output. The information on lines 11-25 may be shifted left or right by controlling the time when the horizontal bit information is output, thereby producing the horizontal scrolling action. During horizontal scrolling operations, the Low Address Counter is loaded with an offset value obtained from the Horizontal Scrolling Registers. That value becomes the new address information pointing to Display RAM's horizontal scrolling data.

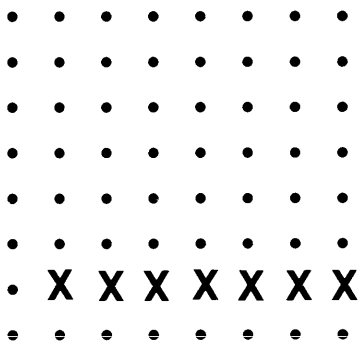
The Character ROM Latch, A11U215, latches the timing diagram cursor highlight and cursor position data from the Display RAM. The Glitch/Timing Parallel Data Latch, A11U310, latches the data on Y0-Y3 as glitch data and Y4-Y7 as timing data. The lower four bits of the data word contain highlight data, while the upper four bits contain cursor position data. This parallel data is converted into two serial data streams on the GLITCH(H) and TIMING(H) signal lines by the Glitch/Timing Parallel-To-Serial Convertor, A11U308 and U408.

A11U200 latches the serial data for the Timing Diagram ROM. The Timing Diagram ROM, A11U205, uses the Display RAM glitch and timing serial data, in conjunction with the raster row information on L0(H)-L2(H), to determine which data is to be output. The timing diagram waveforms consist of timing diagram rising and falling edges, top and bottom bars, and wide rising and falling edges (for glitches). Tick marks are generated when the GATE(L) signal blanks out the top and bottom bars, leaving only rising and falling edges.

HORIZONTAL SCROLL AREA – TEST DESCRIPTION

The horizontal scrolling circuitry is verified by scrolling a diagnostic character horizontally through the diagnostic window, A10U295 and U190. The I/O Processor then reads back a portion of the displayed video from the diagnostic window to verify that it is correct.

The diagnostic window register is clocked by raster 200. Since it is an 8-bit shift register, it will contain the last 8 pixels that were sent to the video monitor before raster 200 occurred. Raster 200 is the bottom pixel row of line 25. The character scrolled through the window is a special diagnostic character. This character was selected because it supplies information that identifies which data line is bad in the character generation circuitry, or which bit is bad in the scrolling circuitry. A graphic representation of the diagnostic character being scrolled horizontally (causing a waveform bottom-bar character to be formed) on an 8 X 8 matrix is shown in the following:



Since the test uses line 26 in the Display RAM, the contents of the Display RAM are saved in system RAM at locations $B350_{hex}$ through $BB50_{hex}$. After saving the contents of Display RAM, line 26 is filled with FF_{hex}. This causes the Display Board to select the timing character mode. The bottom-bar character (shown above) is written to the character location on line 26 so that it is directly below the character location on line 25.

Because the bottom-bar character is on character-pixel row 2, it is not positioned over raster 200 (character line 25). To position it over the correct raster row, the character is written to line 26 and vertically scrolled up by seven raster rows. The second pixel row of the horizontal bar character is then positioned over the last eight columns of raster row 200.

The diagnostic character is scrolled left by writing a sequence of values to the HBIT register (at location $A806_{hex}$) in the Horizontal Scrolling circuitry. As the character is scrolled left, the value read back in the diagnostic window will appear to be shifted left by two after each scroll operation.

To make the verification algorithm as simple as possible, the character is scrolled once horizontally before it is read the first time. The data sequence expected from the diagnostic window register is: 03_{hex}, $0F_{hex}$, $3F_{hex}$, 80_{hex}.

When the test has been completed, the contents of locations $B350_{hex}$ through $BB50_{hex}$ are restored to the Display RAM.

3310 Error Index

Explanation: Before the diagnostic window register is read each time, a 60 Hz interrupt must occur. In this case, the 60 Hz interrupt did not occur and the diagnostic test was not run.

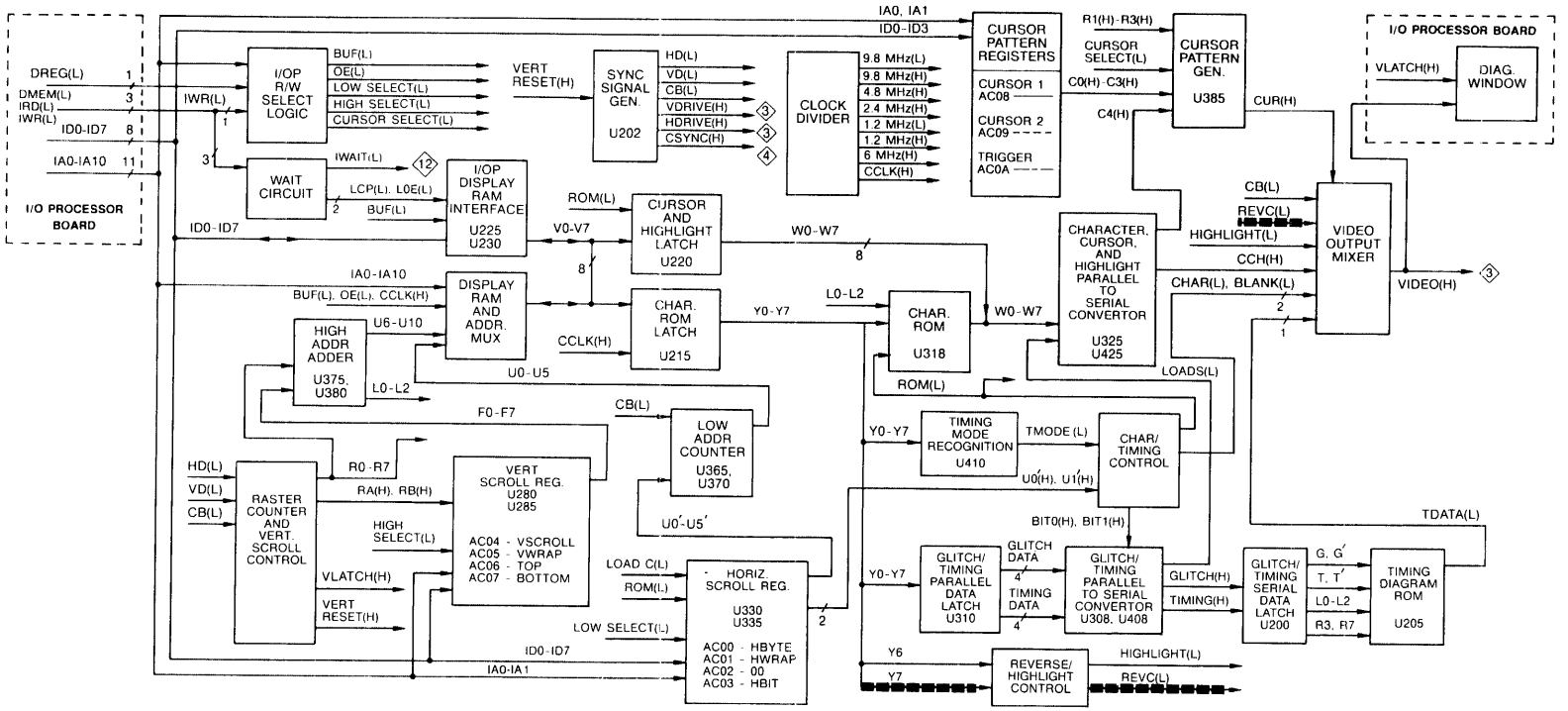
Probable Cause	Action
The 60 Hz interrupt is not working correctly.	Run the I/O Processor INTERRUPT area diagnostic test to determine why the interrupt is not working. Since the I/O INTERRUPT test has already been run before reaching this point, the failure is probably an intermittent one. Looping on the interrupt test may help find the error.

3311 Error Index

Explanation: While horizontally scrolling the diagnostic character, an incorrect pattern was read back.

Probable Cause	Action
The 19.6 MHz clock or the Clock Divider circuitry is not working.	Check the 19.6 MHz clock at A11U495B-13. Check the output frequencies of the Clock Divider A11U250A-11, 12, 13, and 14.
The Horizontal Scrolling Registers are defective.	Suspect the Horizontal Scrolling Registers A11U330 and U335.
The Low Address Counter is defective.	Suspect the Low Address Counter A11U365 and U370.
The Glitch/Timing Data Latch is defective.	Suspect the Glitch/Timing Data Latch A11U310.
The Glitch/Timing Parallel-To-Serial Convertor is defective.	Suspect the convertor A11U308 and U408.
The Timing Diagram ROM or Latch is defective.	Suspect the Timing Diagram ROM or Latch A11U200, U205, and U298.
The Video Output Mixer is defective.	Suspect the Video Mixer A11U245, U260, U405, U435, U480, U490.

DISPLAY BLOCK DIAGRAM
REVERSE VIDEO – AREA 4



4342-107

Figure 8-53. Display REVERSE VIDEO block diagram.

DISPLAY BOARD – COMPONENT LOCATION

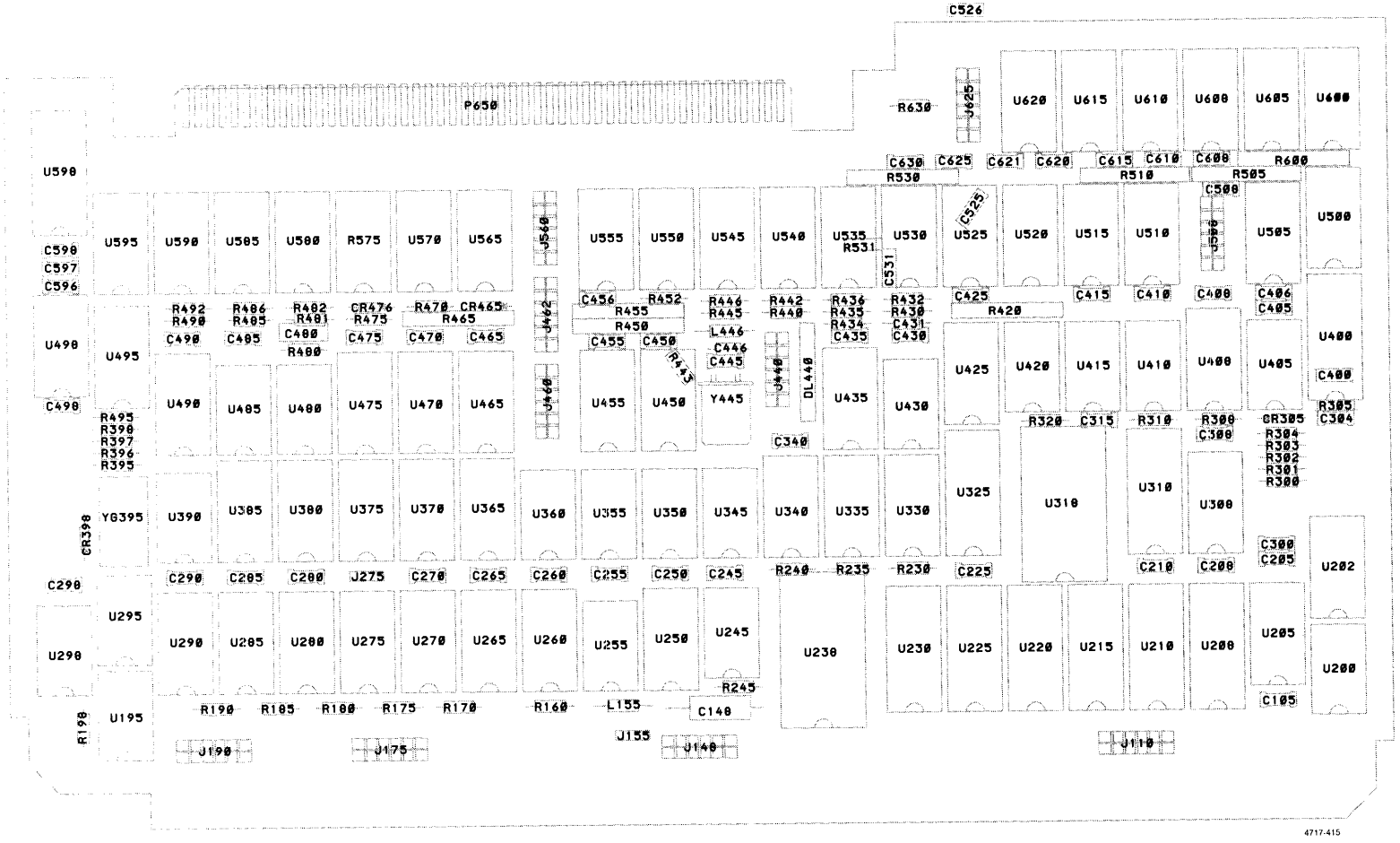


Figure 8-54. Display Board component location.

module: DISPLAY
area: RVIDEO

REVERSE VIDEO AREA – CIRCUIT OVERVIEW

The pattern-shaded signal lines on the reverse video block diagram indicate circuitry used during diagnostic testing. Only the circuitry that is being exercised for the first time during diagnostic testing is shown. Circuitry exercised by other diagnostic tests are shown in their respective block diagrams.

The Reverse/Highlight Control circuitry determines character attributes for the Video Output Mixer. Data lines Y6(H) and Y7(H) from the latched Character ROM data bus are used to determine if the output character is to be normal video, reverse video (dark characters on a light background), or highlighted video (light characters on a shaded background). The 11 (one-one) combination of data bits 6 and 7 is also used to control the A9 address line to the Character ROM.

The Character ROM, A11U318, is a 2K X 8-bit, 2716-type EPROM containing two 64-character sets of text characters. The two character sets provide a total of 128 possible display characters. The A9 address line to the Character ROM forces the character that is output to be from the second set of characters within the ROM, and to have the same attribute as the previously output character (copycat). The following table summarizes the four possible states of data lines Y6(H) and Y7(H).

BIT 7 STATE	BIT 6 STATE	CHARACTER ATTRIBUTE
0	0	standard (use set 1)
0	1	highlighted (use set 1)
1	0	reverse (use set 1)
1	1	keep previous attribute (use set 2)

REVERSE VIDEO AREA – TEST DESCRIPTION

The reverse video circuitry is verified using the diagnostic window, A10U295 and U190. When the I/O Processor reads a standard video pixel from the diagnostic window, it has a binary value of 1. A reverse video pixel is read as a binary value of 0.

First, a reverse video space character is written to the character position in Display RAM that contains raster 200 information. This is the bottom raster on character line 25. Next, the test waits for one 60 Hz interrupt prior to reading the diagnostic window. This syncronizes the processor readback of the diagnostic window register with the updating of the register by hardware. When the interrupt occurs, the diagnostic window register is read, expecting a value of 00_{hex}.

3410 Error Index

Explanation: Before the diagnostic window register is read each time, a 60 Hz interrupt must occur. In this case, the 60 Hz interrupt did not occur and the diagnostic test was not run.

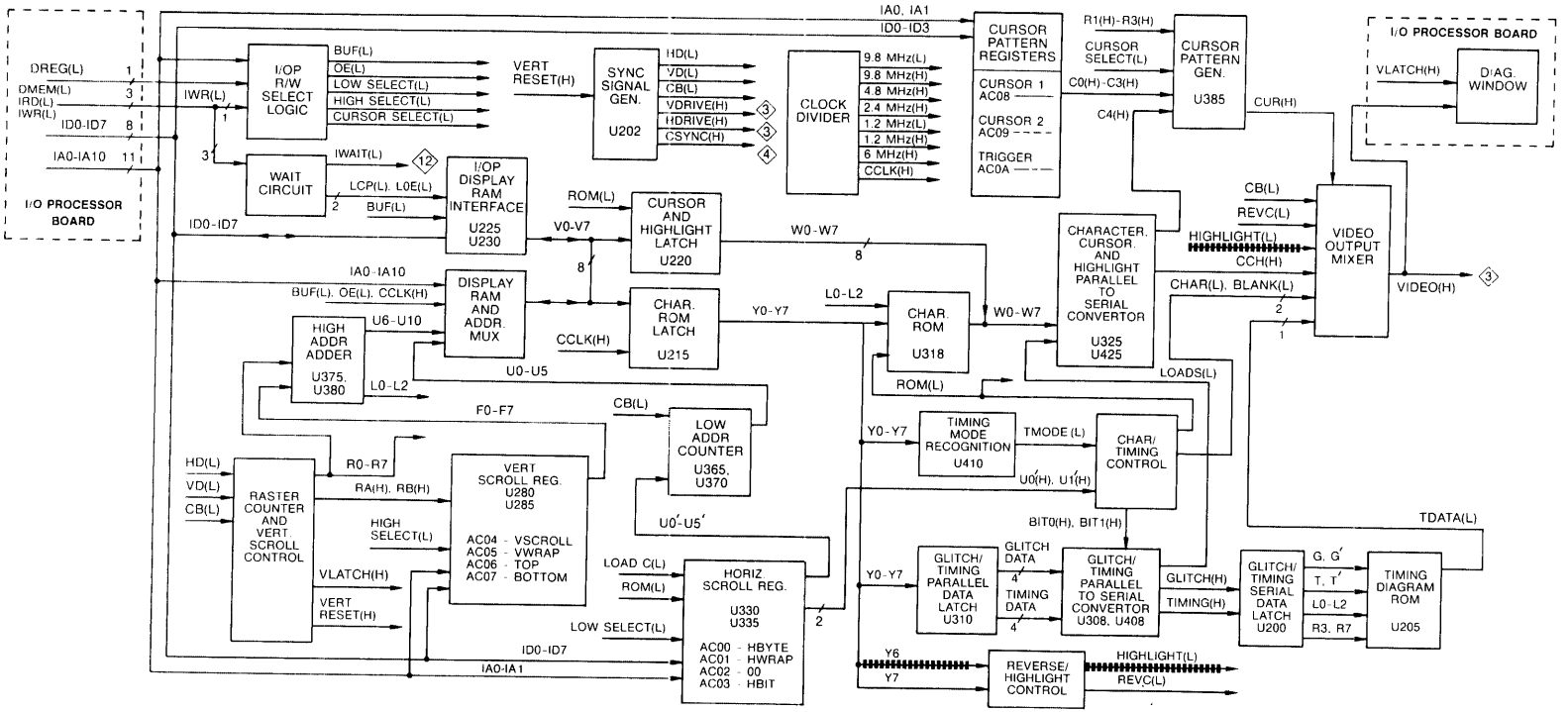
Probable Cause	Action
The 60 Hz interrupt is not working correctly.	Run the I/O Processor's INTERRUPT area diagnostic test to determine why the interrupt is not working. Since the I/O INTERRUPT test has already been run before reaching this point, the failure is probably an intermittent one. Looping on the interrupt test may help in finding the error.

3411 Error Index

Explanation: The reverse video space character could not be read back.

Probable Cause	Action
The 19.6 MHz clock, or the Clock Divider is not working.	Check the 19.6 MHz clock at A11U495-13. Check the output frequencies of the Clock Divider at A11U250A-11, 12, 13, and 14.
The generated character was not correct.	Suspect the Character ROM Latch A11U215, the Character ROM A11U318, or the Character ROM output latch A11U325.
The parallel-to-serial convertor is not working.	Suspect the Character, Cursor, and Highlight Parallel-To-Serial Convertor A11U425.
The reverse video character could not be read because the copycat control is not working.	Suspect the copycat control circuitry A11U415 and U208.
The Video Output Mixer is not working correctly.	Suspect the Video Output Mixer logic (A11U245, U260, U405, U435, U480, or U490).

DISPLAY BLOCK DIAGRAM
HIGHLIGHTING – AREA 5



4342-108

Figure 8-55. Display HIGHLIGHTING block diagram.

DISPLAY BOARD – COMPONENT LOCATION

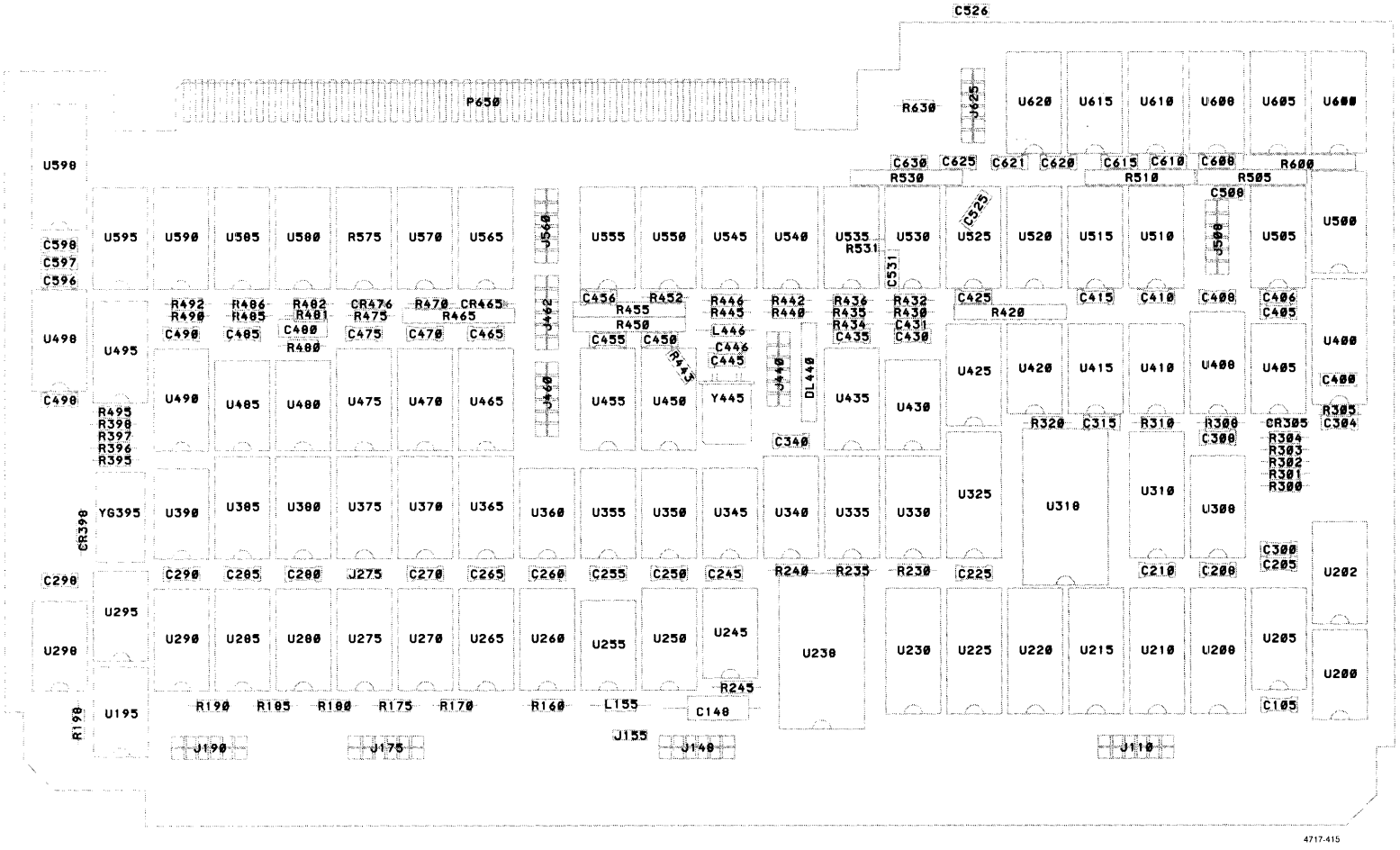


Figure 8-56. Display Board component location.

module: DISPLAY
area: HIGHLIGHT

HIGHLIGHTING AREA – CIRCUIT OVERVIEW

The pattern-shaded signal lines on the highlighting block diagram indicate circuitry used during diagnostic testing. Only the circuitry that is being exercised for the first time during diagnostic testing is shown. Circuitry exercised by other diagnostic tests are shown in their respective block diagrams.

The Reverse/Highlight Control circuitry determines character attributes for the Video Output Mixer. Data lines Y6(H) and Y7(H) from the latched Character ROM data bus are used to determine if the output character is to be normal video, reverse video (dark characters on a light background), or highlighted video (light characters on a shaded background). The 11 (one-one) combination of data bits 6 and 7 is also used to control the A9 address line to the Character ROM.

The Character ROM, A11U318, is a 2K X 8-bit, 2716-type EPROM containing two 64-character sets of text characters. The two character sets provide a total of 128 possible display characters. The A9 address line to the Character ROM forces the character that is output to be from the second set of characters within the ROM, and to have the same attribute as the previously output character (copycat). The following table summarizes the four possible states of data lines Y6(H) and Y7(H).

BIT 7 STATE	BIT 6 STATE	CHARACTER ATTRIBUTE
0	0	standard (use set 1)
0	1	highlighted (use set 1)
1	0	reverse (use set 1)
1	1	keep previous attribute (use set 2)

HIGHLIGHTING AREA – TEST DESCRIPTION

The highlighting circuitry is verified using the diagnostic window, A10U295 and U190. Two hardware addresses facilitate the verification of the highlighting area circuitry. The first address ($ACOF_{hex}$) inverts the 9.8 MHZ(H) clock by using latch U490D and EXOR gate U480C. The second address ($AC10_{hex}$) turns off the inversion. With the 9.8 MHZ(H) clock inverted, the I/O Processor is able to read highlighted pixels from the diagnostic window.

The test starts by writing a highlight space character to the diagnostic window location in the Display RAM. Next, the test waits for one 60 Hz interrupt prior to reading the diagnostic window. This synchronizes the processor readback of the diagnostic window register with the updating of the register by hardware. When the interrupt occurs, address $AC0F_{hex}$ is written to the invert 9.8 MHZ(H) clock. Now the contents of the diagnostic window register is read, expecting a value of 00_{hex}.

The test continues by writing a timing mode highlight space character to the diagnostic window location in the Display RAM. The contents of the diagnostics window register is read, expecting a value of 00_{hex}. The test now writes to address $AC10_{hex}$ to turn off the inversion of the 9.8 MHZ(H) clock. The contents of the diagnostic window is read once again, this time expecting FF_{hex}.

3510 Error Index

Explanation: Before the diagnostic window register is read each time, a 60 Hz interrupt must occur. In this case, the 60 Hz interrupt did not occur and the diagnostic test was not run.

Probable Cause	Action
The 60 Hz interrupt is not working correctly.	Run the I/O Processor's INTERRUPT area diagnostic test to determine why the interrupt is not working. Since the I/O INTERRUPT test has already been run before reaching this point, the failure is probably an intermittent one. Looping on the interrupt test may help in finding the error.

3511 Error Index

Explanation: The highlight space character could not be read back with the 9.8 MHZ(H) clock inverted.

Probable Cause	Action
The 19.6 MHz clock, or the Clock Divider circuitry is not working.	Check the 19.6 MHz clock at A11U495-13. Check the output frequencies of the Clock Divider at A11U250-11, 12, 13, and 14.
The generated character was not correct.	Suspect the Character ROM Latch A11U215, the Character ROM A11U318, or the Character ROM output latch A11U325.
The parallel-to-serial convertor is not working.	Suspect the Character, Cursor, and Highlight Parallel-To-Serial Convertor A11U425.
The highlighting latching circuitry is not working.	Suspect the highlighting latching circuitry A11U415 and U208.
The circuitry to invert the 9.8 MHZ(H) clock used by the Video Output Mixer is not working.	Suspect the 9.8 MHZ(H) inversion circuitry A11U340, U480C, or U490D.
The Video Output Mixer is not working correctly.	Suspect the Video Output Mixer logic A11U245, U260, U405, U435, U480, or U490.

3512 Error Index

Explanation: The timing mode highlight space character could not be read back with the 9.8 MHZ(H) clock inverted.

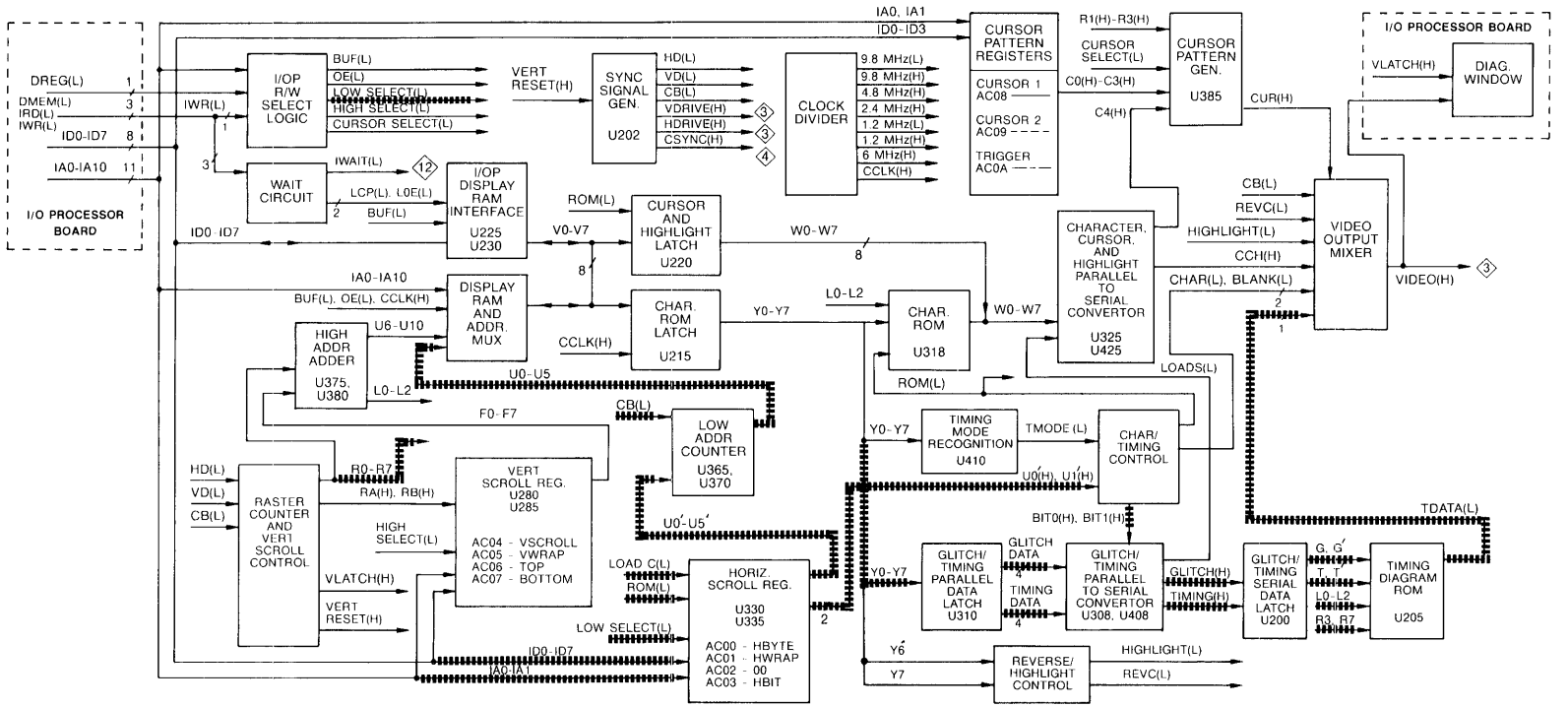
Probable Cause	Action
The 19.6 MHz clock, or the Clock Divider circuitry is not working.	Check the 19.6 MHz clock at A11U495-13. Check the output frequencies of the Clock Divider at A11U250-11, 12, 13, and 14.
The generated character was not correct.	Suspect the Character ROM Latch A11U215, the Character ROM A11U318, or the Character ROM output latch A11U325.
The parallel-to-serial convertor is not working.	Suspect the Character, Cursor, and Highlight Parallel-To-Serial Convertor A11U425.
The circuitry to invert the 9.8 MHZ(H) clock used by the Video Output Mixer is not working.	Suspect the 9.8 MHZ(H) inversion circuitry A11U340, U480C, or U490D.
The Video Output Mixer is not working correctly.	Suspect the Video Output Mixer logic A11U245, U260, U405, U435, U480, or U490.

3513 Error Index

Explanation: The timing mode highlight space character could not be read back with the normal 9.8 MHZ(H) clock.

Probable Cause	Action
The 19.6 MHz clock, or the Clock Divider circuitry is not working.	Check the 19.6 MHz clock at A11U495-13. Check the output frequencies of the Clock Divider at A11U250-11, 12, 13, and 14.
The generated character was not correct.	Suspect the Character ROM Latch A11U215, the Character ROM A11U318, or the Character ROM output latch A11U325.
The parallel-to-serial convertor is not working.	Suspect the Character, Cursor, and Highlight Parallel-To-Serial Convertor A11U425.
The circuitry to invert the 9.8 MHZ(H) clock used by the Video Output Mixer is not working.	Suspect the 9.8 MHZ(H) inversion circuitry A11U340, U480C, or U490D.
The Video Output Mixer is not working correctly.	Suspect the Video Output Mixer logic A11U245, U260, U405, U435, U480, or U490.

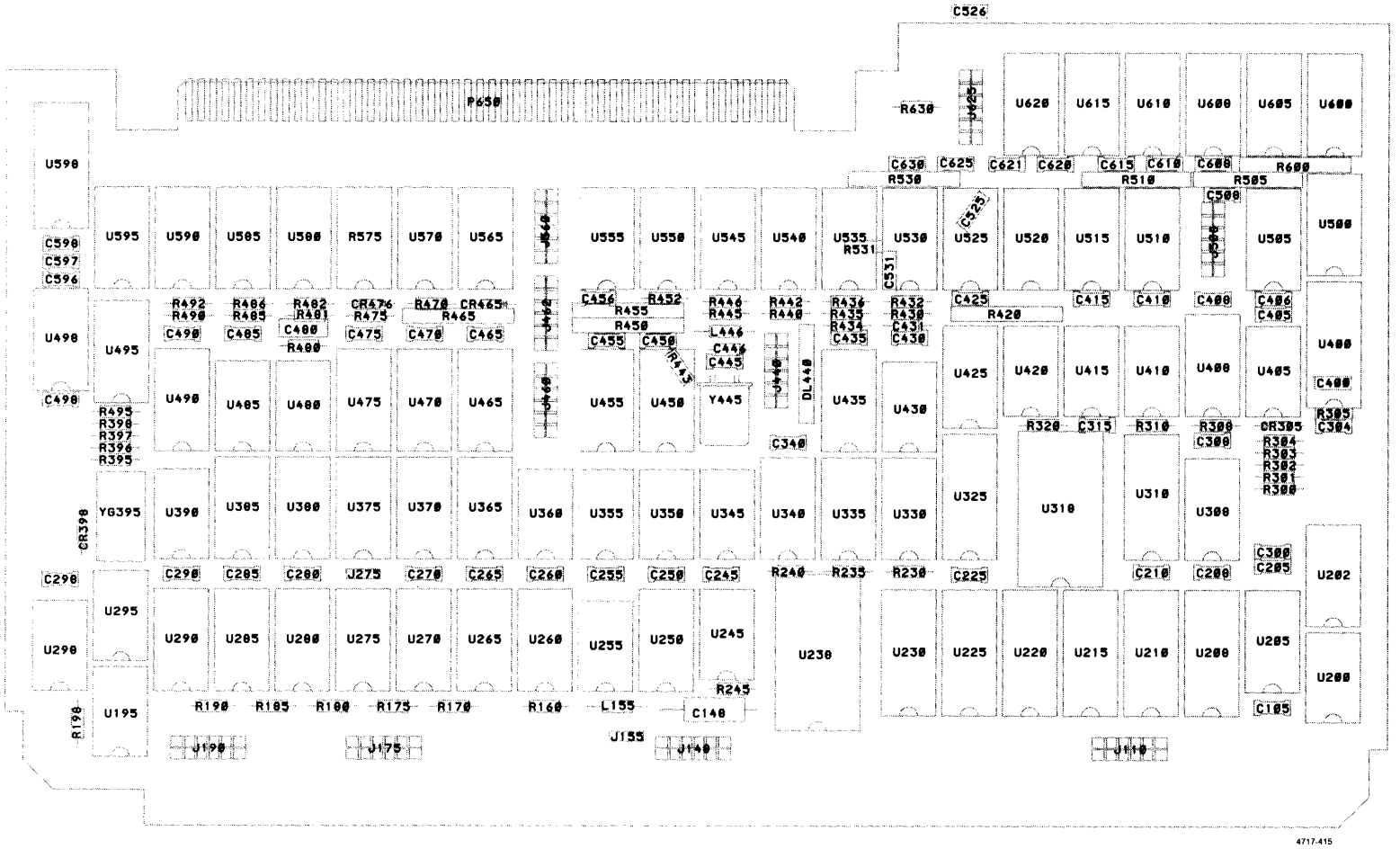
DISPLAY BLOCK DIAGRAM
WAVEFORM (GENERATION) – AREA 6



4342-109

Figure 8-57. Display WAVEFORM block diagram.

DISPLAY BOARD – COMPONENT LOCATION



10-15.

Figure 8-58. Display Board component location.

module: DISPLAY
area: WAVEFORM

WAVEFORM (GENERATION) AREA – CIRCUIT OVERVIEW

The pattern-shaded signal lines on the waveform generation block diagram indicate circuitry used during diagnostic testing. Only the circuitry that is being exercised for the first time during diagnostic testing is shown. Circuitry exercised by other diagnostic tests are shown in their respective block diagrams.

The waveform generation circuitry is basically comprised of the Horizontal Scrolling Registers, Display RAM addressing circuitry, and the Timing Diagram ROM circuitry. Since waveform character generation is only possible during timing diagram displays, the Timing Diagram ROM supplies any needed waveform characters used during these operations (the Character ROM is disabled). The circuitry used during waveform generation is the same as that used during horizontal scrolling operations, except that different portions of the Timing Diagram ROM are used. For this reason, the following circuitry discussion is a repeat of the *Horizontal Scroll Area Circuit Overview*.

The Horizontal Scrolling Registers, A11U330 and U335, contain an offset value that is used to determine the portion of Display RAM to be read for horizontal scrolling data. This offset value, sent by the I/O Processor on ID0(H)-ID7(H) to the Low Address Counter (A11U365 and U370), becomes the Display RAM's lower six address bits.

During basic text displays, the Display RAM's lower six bits determine which of the 64 characters in the screen line is being output. The information on lines 11-25 may be shifted left or right by controlling the time when the horizontal bit information is output, thereby producing the horizontal scrolling action. During horizontal scrolling operations, the Low Address Counter is loaded with an offset value obtained from the Horizontal Scrolling Registers. That value becomes the new address information pointing to Display RAM's horizontal scrolling data.

The Character ROM Latch, A11U215, latches the timing diagram cursor highlight and cursor position data from the Display RAM. The Glitch/Timing Parallel Data Latch, A11U310, latches the data on Y0-Y3 as glitch data and Y4-Y7 as timing data. The lower four bits of the data word contain highlight data, while the upper four bits contain cursor position data. This parallel data is converted into two serial data streams on the GLITCH(H) and TIMING(H) signal lines by the Glitch/Timing Parallel-To-Serial Convertor, A11U308 and U408.

A11U200 latches the serial data for the Timing Diagram ROM. The Timing Diagram ROM, A11U205, uses the Display RAM glitch and timing serial data, in conjunction with the raster row information on L0(H)-L2(H), to determine which data is to be output. The timing diagram waveforms consist of timing diagram rising and falling edges, top and bottom bars, and wide rising and falling edges (for glitches). Tick marks are generated when the GATE(L) signal blanks out the top and bottom bars, leaving only rising and falling edges.

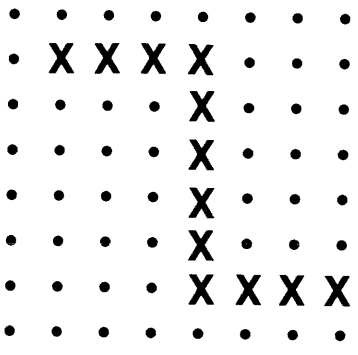
WAVEFORM (GENERATION) AREA – TEST DESCRIPTION

The timing and glitch waveform generation circuitry is verified by writing timing and glitch characters to the Display RAM. The characters are then scrolled through the diagnostic window, A10U295 and U190. The I/O Processor reads back a portion of the displayed video from the diagnostic window to verify that it is correct.

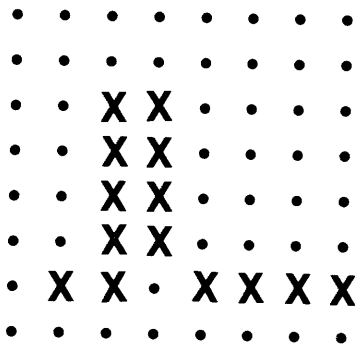
The test starts by writing a timing waveform character (graphically represented in the following) to the Display RAM. Since the test uses line 26 in the Display RAM, the contents of the Display RAM are saved in system RAM at locations $B350_{hex}$ through $BB50_{hex}$. After saving the contents of Display RAM, line 26 is filled with FF_{hex}. This causes the Display Board to select the timing character mode. The display is scrolled vertically one raster line to align the top raster row of the character with the diagnostic window (raster 200). Now, the timing waveform character is scrolled vertically eight rasters. The I/O Processor reads the diagnostic window each time the display is scrolled. If a failure is detected, the test ends and reports the failure.

When the timing waveform character has been successfully scrolled and read back, the test writes the glitch waveform character (graphically represented in the following) to the Display RAM. This time the display is scrolled vertically two rasters to align the top raster row of the character with the diagnostic window. The glitch waveform character is scrolled vertically eight rasters. The I/O Processor reads back from the diagnostic window after each scroll operation. If a failure is detected, the test ends and reports the failure.

A graphic representation of the timing and glitch waveform characters on an 8 X 8 matrix is shown in the following:



Timing Waveform Character



Glitch Waveform Character

3610 Error Index

Explanation: Before the diagnostic window register is read each time, a 60 Hz interrupt must occur. In this case, the 60 Hz interrupt did not occur and the diagnostic test was not run.

Probable Cause	Action
The 60 Hz interrupt is not working correctly.	Run the I/O Processor INTERRUPT area diagnostic test to determine why the interrupt is not working. Since the I/O INTERRUPT test has already been run before reaching this point, the failure is probably an intermittent one. Looping on the interrupt test may help in finding the error.

3611 Error Index

Explanation: While vertically scrolling the timing waveform character, an incorrect pattern was read back.

Probable Cause	Action
The Glitch/Timing Parallel Data Latch is defective.	Suspect parallel data latch A11U310.
The Timing Parallel-To-Serial Convertor is defective.	Suspect the parallel-to-serial convertor A11U408.
A latch used to hold information from the parallel-to-serial convertor is defective.	Suspect latch A11U200.
The Timing Diagram ROM is defective.	Suspect the Timing Diagram ROM A11U205.
The Video Output Mixer is defective.	Suspect the Video Mixer A11U245, U260, U405, U435, U480, U490.

3612 Error Index

Explanation: While vertically scrolling the glitch waveform character, an incorrect pattern was read back.

Probable Cause	Action
The Glitch Data Parallel-To-Serial Convertor is defective.	Suspect parallel-to-serial convertor A11U308.

4XXX COMMPACK ERROR INDEXES

Error Index	Area Name	Area Number
41XX	EPROM	AREA 1
42XX	FUNCTION	AREA 2

COMMPACK MANUAL TEST

Module	Area	Routine	Description
COMMPACK	MANUAL	1	RS232 BERT Test

RS232 COMMPACK BLOCK DIAGRAM
EPROM – AREA 1

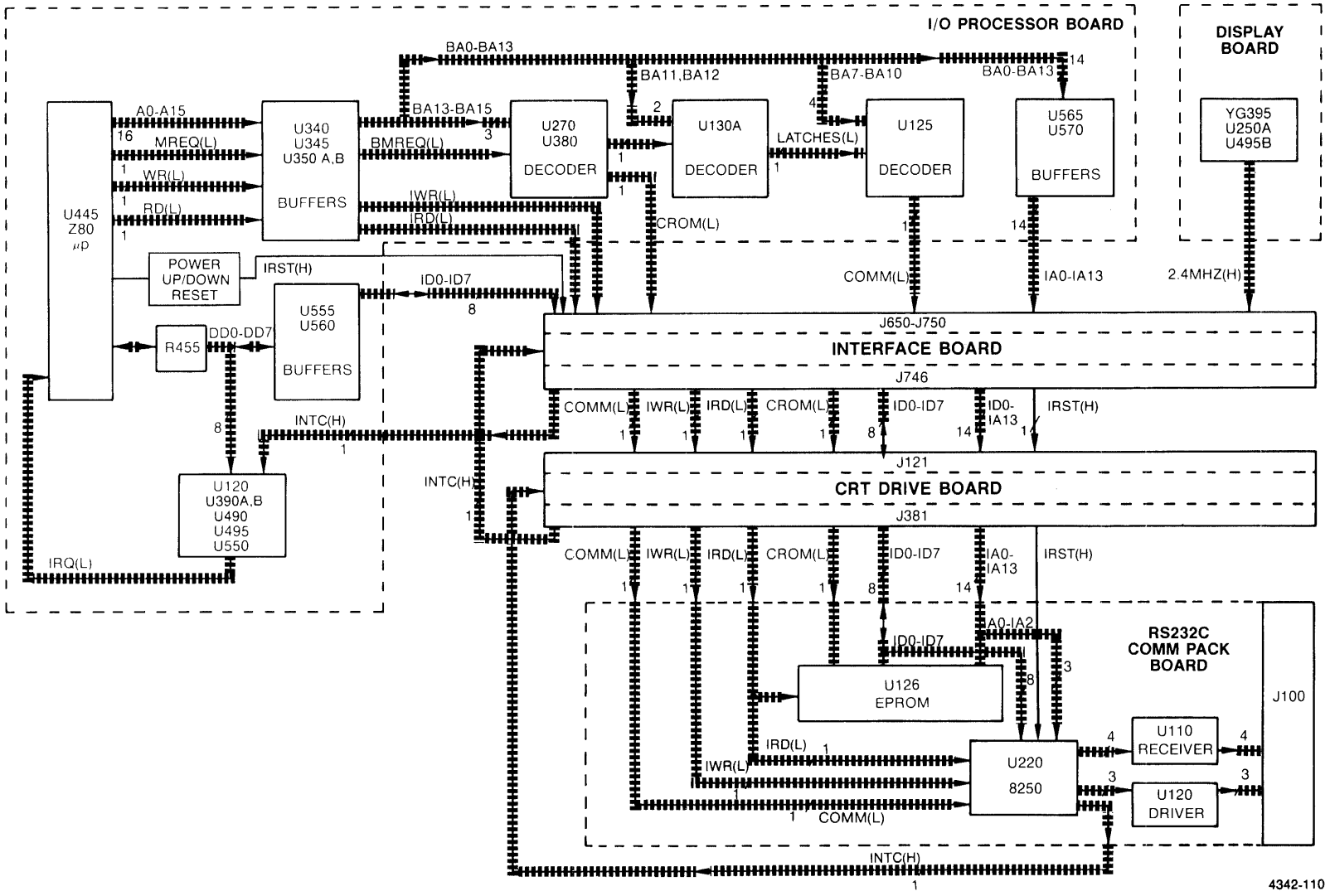


Figure 8-59. RS232 COMMPACK EPROM block diagram.

RS232 COMM PACK BOARD – COMPONENT LOCATION

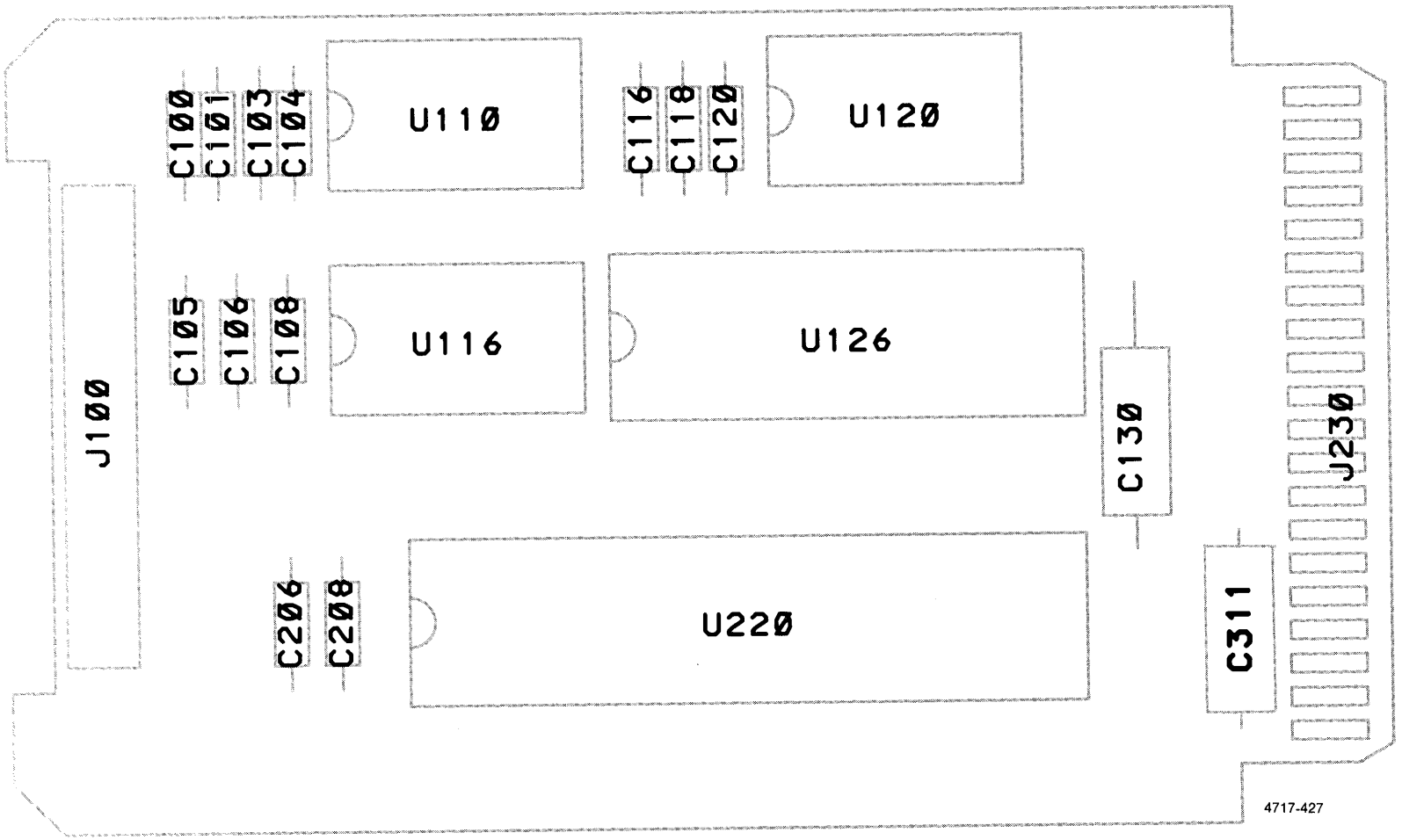


Figure 8-60. RS232 Comm Pack Board component location.

module: COMMPACK
area: EPROM

RS232 EPROM AREA – CIRCUIT OVERVIEW

The pattern-shaded signal lines on the RS232 communication pack block diagram indicate circuitry used during diagnostic testing. Only the circuitry that is being exercised for the first time during diagnostic testing is shown. Circuitry exercised by other diagnostic tests are shown in their respective block diagrams.

The Z80 microprocessor and control circuitry located on the I/O Processor Board supplies the address, control, and bidirectional data lines to the pack. When an RS232 COMM pack is installed, it indicates its presence to the Z80 microprocessor with the INTC(H) interrupt line.

RS232 EPROM AREA – TEST DESCRIPTION

The error index numbers supplied for COMM pack failures are not unique numbers. Some error index numbers are repeat indexes multiple COMM packs. The error explanations for these repeat error indexes change, however, depending on which COMM pack is installed. When accessing diagnostic error information for COMM packs, first locate the information for the correct type of pack, then locate the correct error index number.

4111

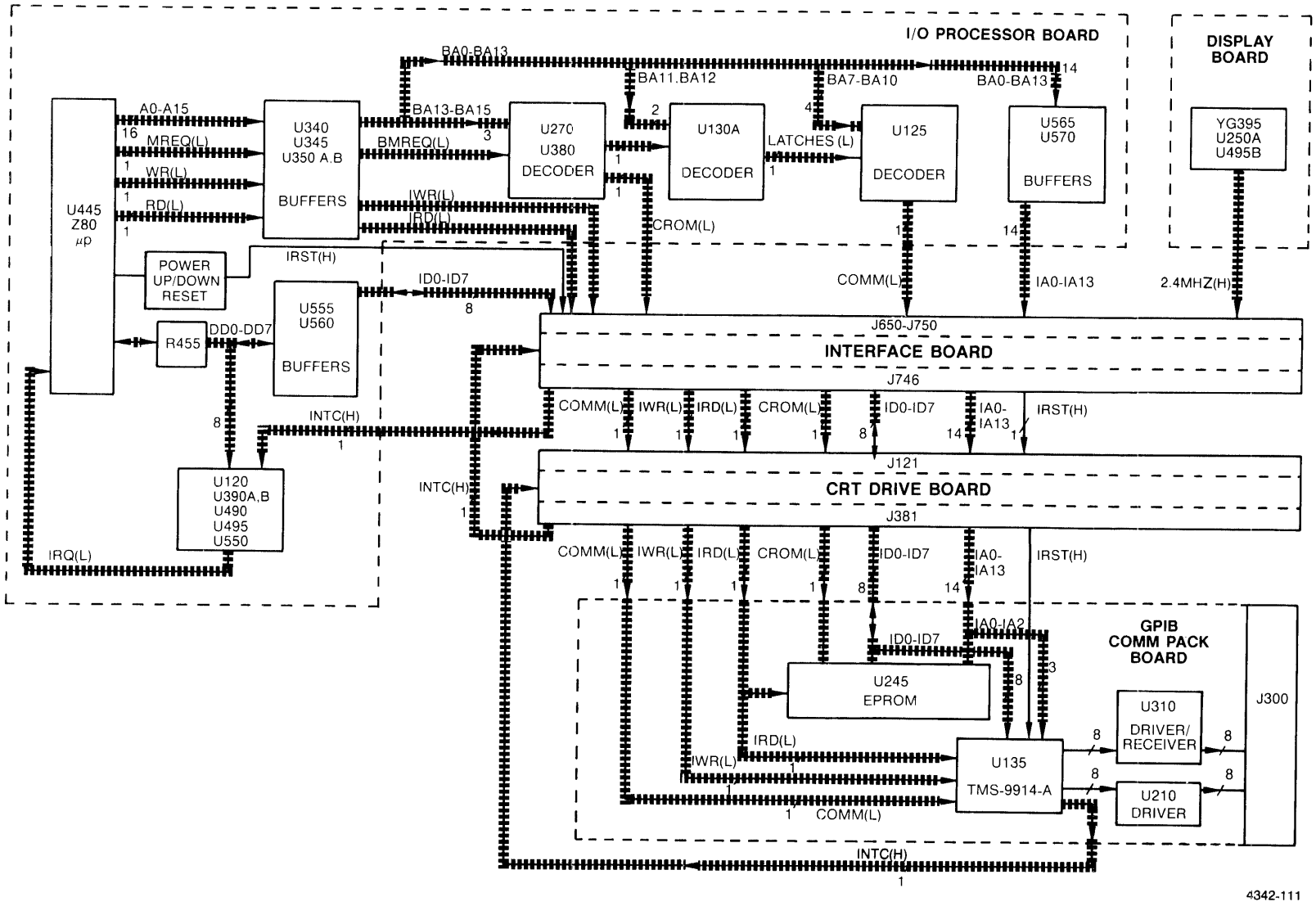
The RS232 EPROM test calculates a checksum for ROM A31U126 on the RS232 COMM Pack Board. The test then compares the calculated checksum to an expected value stored in the last two locations of the ROM. The calculated and expected checksum values are written to the 1240 display screen.

4111 Error Index

Explanation: The data read is not the same as the actual data written.

Probable Cause	Action
Bad ROM.	Suspect ROM A31U126.
Interface problem.	Examine interface signals while referring to schematic.

GPIB COMMPACK BLOCK DIAGRAM
EPROM – AREA 1



4342-111

Figure 8-61. GPIB COMMPACK EPROM block diagram.

GPIB COMM PACK BOARD – COMPONENT LOCATION

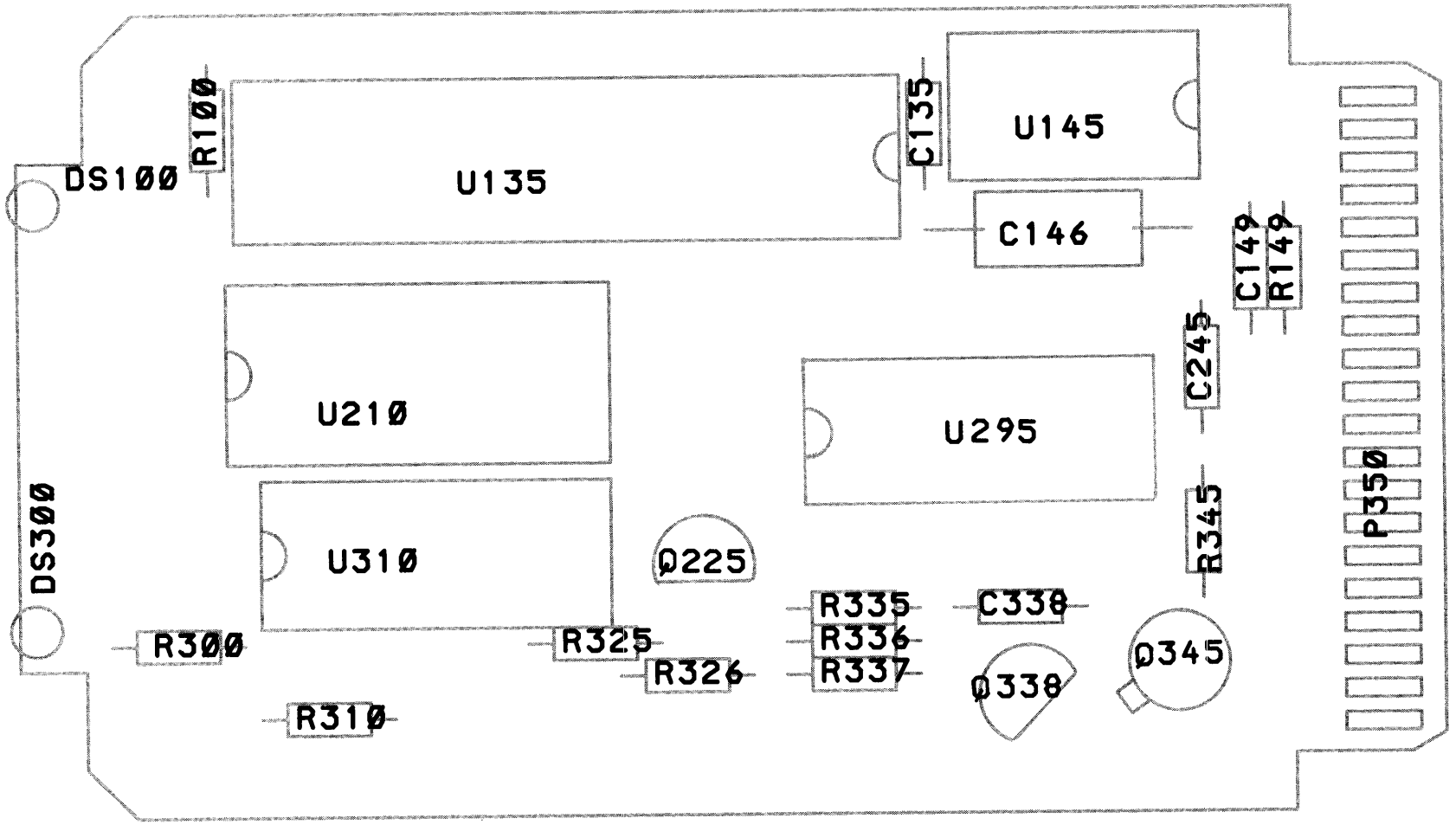


Figure 8-62. GPIB Comm Pack Board component location.

GPIB EPROM AREA – CIRCUIT OVERVIEW

The pattern-shaded signal lines on the GPIB communication pack block diagram indicate circuitry used during diagnostic testing. Only the circuitry that is being exercised for the first time during diagnostic testing is shown. Circuitry exercised by other diagnostic tests are shown in their respective block diagrams.

The Z80 microprocessor and control circuitry located on the I/O Processor Board supplies the address, control, and bidirectional data lines to the pack. When a GPIB COMM pack is installed, it indicates its presence to the Z80 microprocessor with the INTC(H) interrupt line.

GPIB EPROM AREA – TEST DESCRIPTION

The error index numbers supplied for COMM pack failures are not unique numbers. Some error index numbers are repeat indexes multiple COMM packs. The error explanations for these repeat error indexes change, however, depending on which COMM pack is installed. When accessing diagnostic error information for COMM packs, first locate the information for the correct type of pack, then locate the correct error index number.

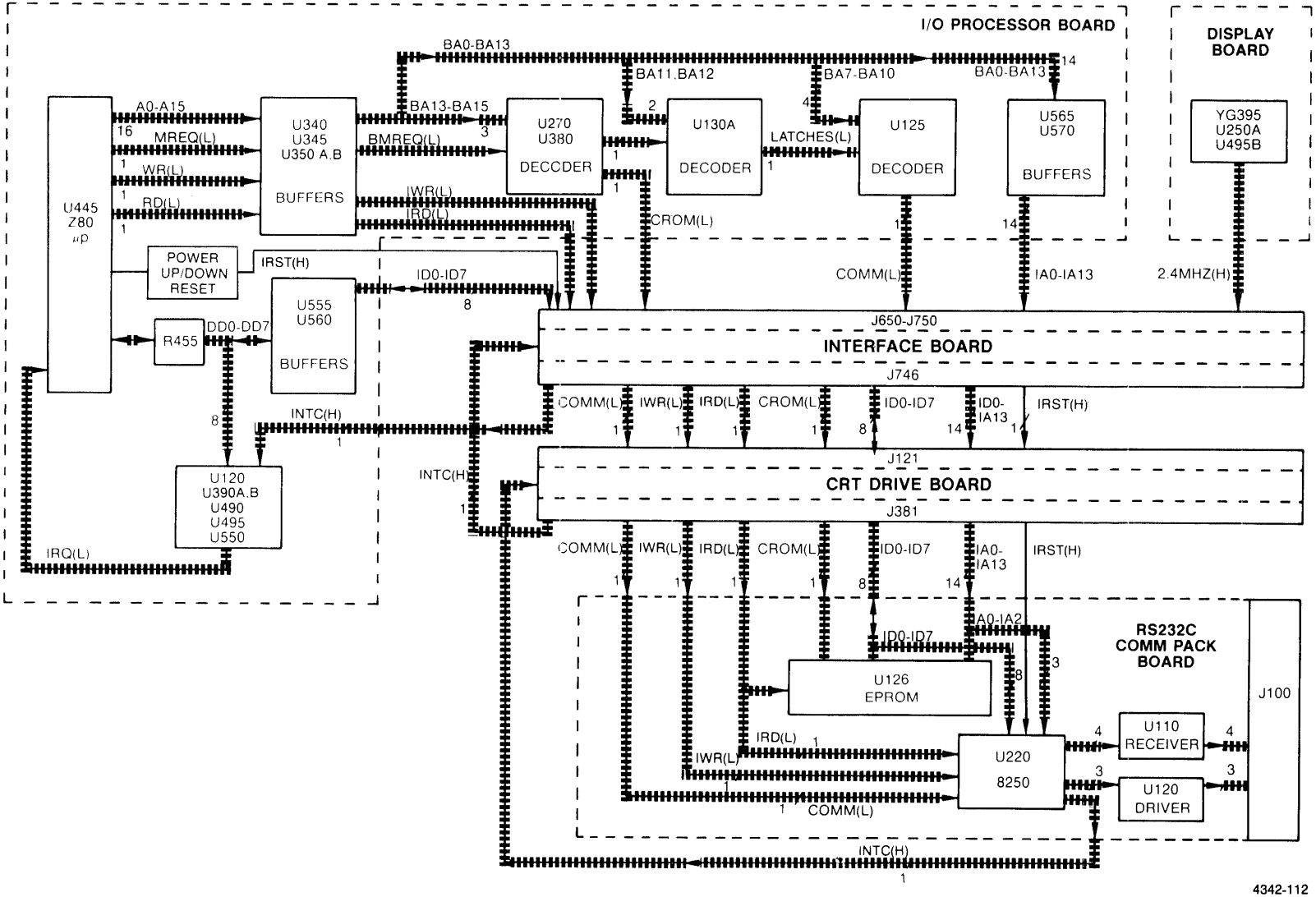
4111

4111 Error Index

Explanation: The data read is not the same as the actual data written.

Probable Cause	Action
Bad ROM.	Suspect ROM A31U245.
Interface problem.	Examine interface signals while referring to schematic.

RS232 COMMPACK BLOCK DIAGRAM FUNCTION – AREA 2



4342-112

Figure 8-63. RS232 COMMPACK FUNCTION block diagram.

RS232 COMM PACK BOARD – COMPONENT LOCATION

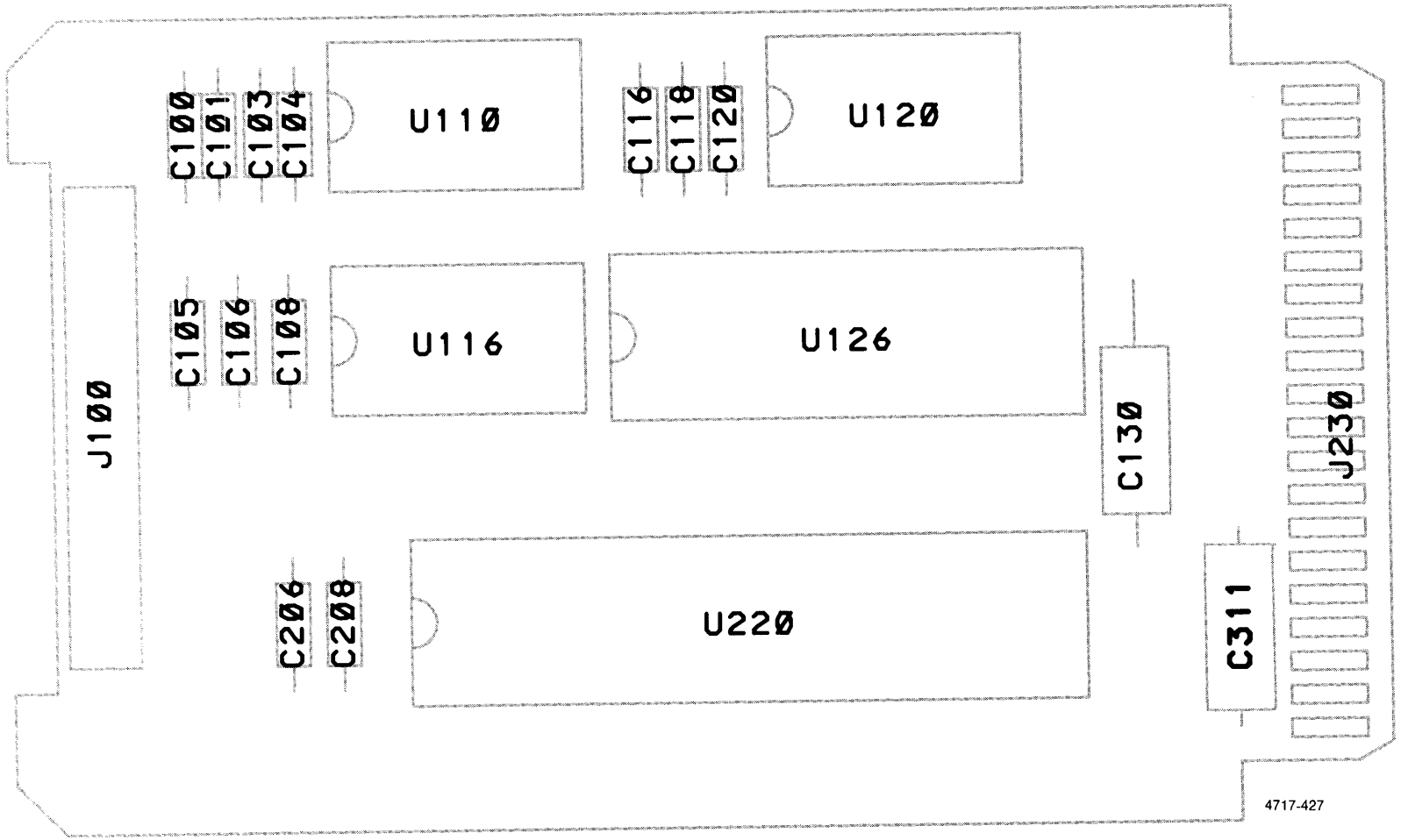


Figure 8-64. RS232 Comm Pack Board component location.

module: COMMPACK
area: FUNCTION

RS232 FUNCTION AREA – CIRCUIT OVERVIEW

The pattern-shaded signal lines on the RS232 communication pack block diagram indicate circuitry used during diagnostic testing. Only the circuitry that is being exercised for the first time during diagnostic testing is shown. Circuitry exercised by other diagnostic tests are shown in their respective block diagrams.

The Z80 microprocessor and control circuitry located on the I/O Processor Board supplies the address, control, and bidirectional data lines to the pack. When an RS232 COMM pack is installed, it indicates its presence to the Z80 microprocessor with the INTC(H) interrupt line.

RS232 FUNCTION AREA – TEST DESCRIPTION

The error index numbers supplied for COMM pack failures are not unique numbers. Some error index numbers are repeat indexes multiple COMM packs. The error explanations for these repeat error indexes change, however, depending on which COMM pack is installed. When accessing diagnostic error information for COMM packs, first locate the information for the correct type of pack, then locate the correct error index number.

4211

The RS232 COMM pack transmitter and receiver circuitry is checked in both loopback and normal (using a self-test adapter) modes. Testing begins by writing a data bit to the COMM pack, and then reading it back after the data ready bit becomes true. The testing continues by incrementing the data bit, writing another data value, and then reading it back to check for the correct value. The data bits increment as follows: 01_{hex}, 02_{hex}, 04_{hex}, 08_{hex}, 10_{hex}, 20_{hex}, 40_{hex}, 80_{hex}.

ROUTINE 1 DESCRIPTION

This routine uses the COMM pack in the loopback mode. The routine writes a 01_{hex} to address $AE80_{hex}$, then waits for the data ready bit to become true. Next, the test reads from address $AE80_{hex}$ and checks for 01_{hex}. The testing continues by writing and reading 02_{hex}, 04_{hex}, 08_{hex}, 10_{hex}, 20_{hex}, 40_{hex}, and 80_{hex}. After each write operation, the test waits for the data ready bit to become true.

4211 Error Index

Explanation: The data ready bit never became true.

Probable Cause	Action
Bad RS232 I.C.	Suspect A31U220.

4212 Error Index

Explanation: The data read is not the same as the actual data written.

Probable Cause	Action
Data line problem into A31U220.	Loop on this test and examine A31U220 data lines with a logic analyzer (trigger on A31U220-18).
Bad RS232 I.C.	Suspect A31U220.

ROUTINE 2 DESCRIPTION

This routine uses the COMM pack in the normal mode. Before testing is possible, a self-test adapter must be connected to the COMM pack. (The adapter's part number may be found in *Table 5-1, REQUIRED TEST EQUIPMENT,* of the *Verification And Adjustment* section) The routine writes 01_{hex} to address $AE80_{hex}$, then waits for the data ready bit to become true. Next, the test reads from address $AE80_{hex}$ and checks for 01_{hex}. The testing continues by writing and reading 02_{hex}, 04_{hex}, 08_{hex}, 10_{hex}, 20_{hex}, 40_{hex}, and 80_{hex}. After each write operation, the test waits for the data ready bit to become true.

4212
4221
4222

4221 Error Index

Explanation: The data ready bit never became true.

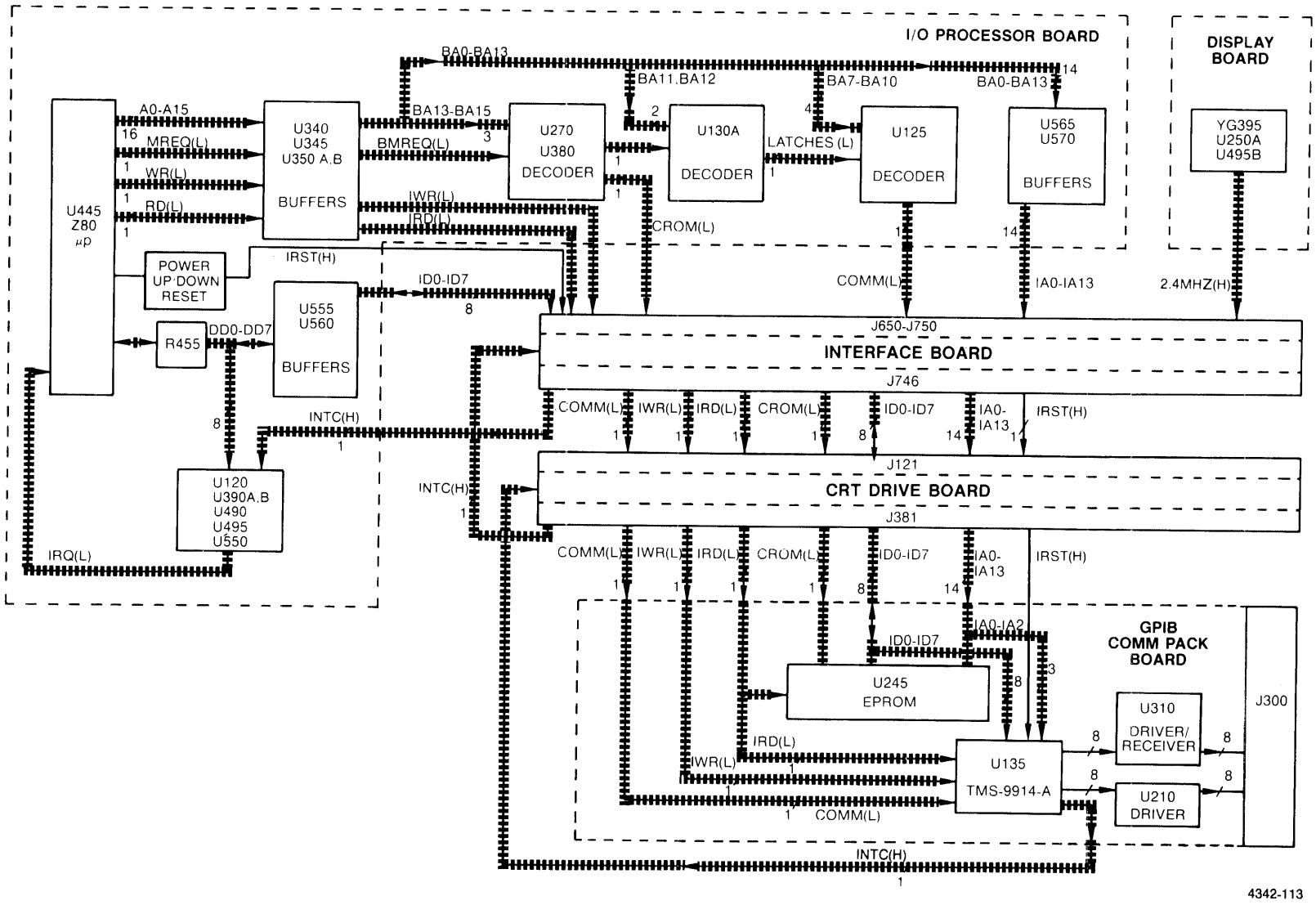
Probable Cause	Action
Bad RS232 I.C.	Suspect A31U220.

4222 Error Index

Explanation: The data read is not the same as actual data written.

Probable Cause	Action
Bad output buffer.	Suspect A31U120.
Bad input buffer.	Suspect A31U110.

GPIB COMMPACK BLOCK DIAGRAM
FUNCTION – AREA 2



4342-113

Figure 8-65. GPIB COMMPACK FUNCTION block diagram.

GPIB COMM PACK BOARD – COMPONENT LOCATION

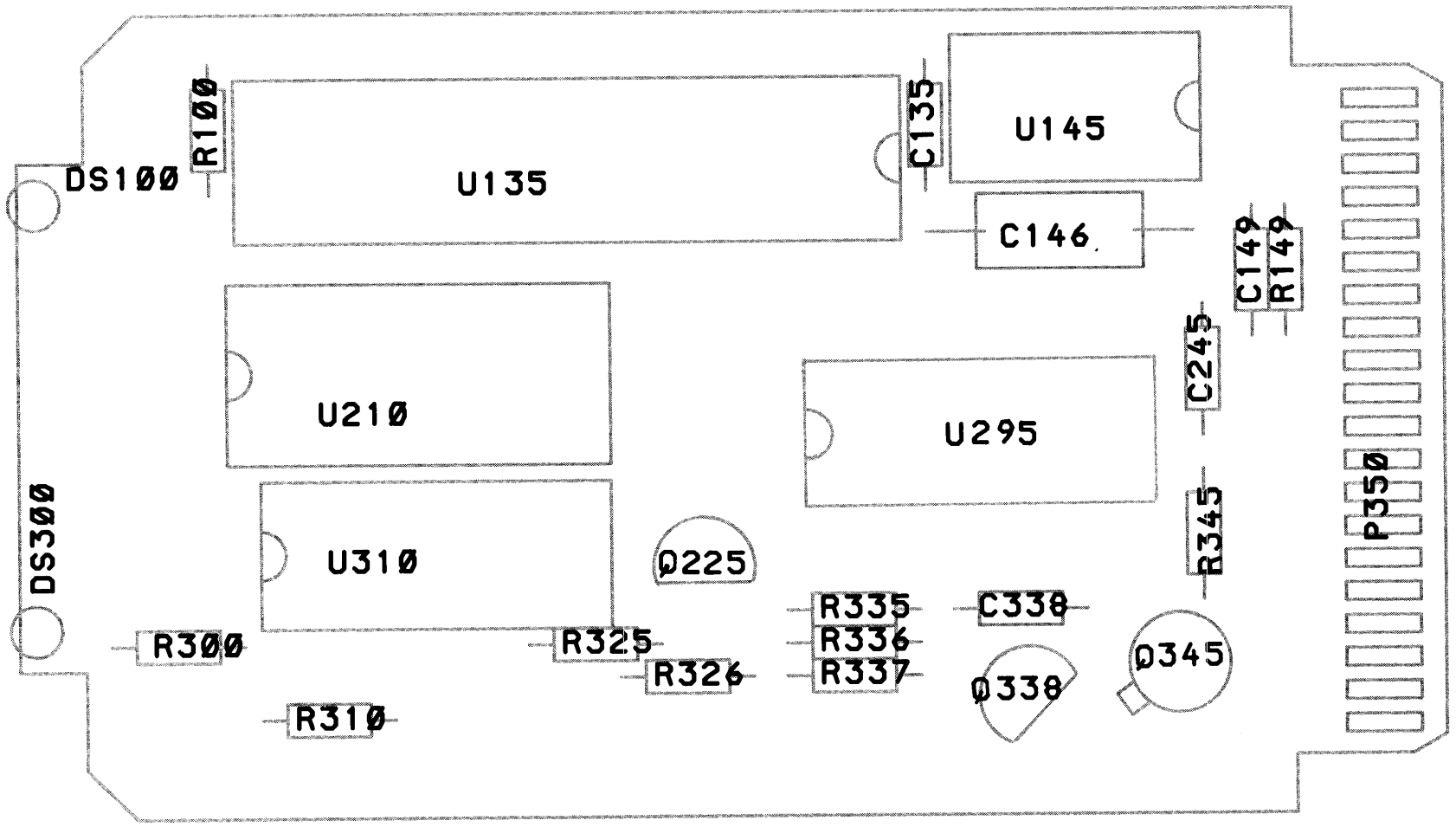


Figure 8-66. GPIB Comm Pack Board component location.

GPIB FUNCTION AREA – CIRCUIT OVERVIEW

The pattern-shaded signal lines on the GPIB communication pack block diagram indicate circuitry used during diagnostic testing. Only the circuitry that is being exercised for the first time during diagnostic testing is shown. Circuitry exercised by other diagnostic tests are shown in their respective block diagrams.

The Z80 microprocessor and control circuitry located on the I/O Processor Board supplies the address, control, and bidirectional data lines to the pack. When a GPIB COMM pack is installed, it indicates its presence to the Z80 microprocessor with the INTC(H) interrupt line.

GPIB FUNCTION AREA – TEST DESCRIPTION

The error index numbers supplied for COMM pack failures are not unique numbers. Some error index numbers are repeat indexes multiple COMM packs. The error explanations for these repeat error indexes change, however, depending on which COMM pack is installed. When accessing diagnostic error information for COMM packs, first locate the information for the correct type of pack, then locate the correct error index number.

4211

The test first resets the GPIB I.C. A32U135, then checks for correct data from the INT1 STATUS register at address AE80$_{hex}$.

4211 Error Index

Explanation: Incorrect data was read from the INT1 STATUS register.

Probable Cause	Action
Bad GPIB I.C.	Suspect A32U135.

module: COMMPACK
area: MANUAL

RS232 COMMPACK MANUAL BERT TEST DESCRIPTION

The Bit Error Rate Tests (BERT), when performed with an 834 Programmable Data Communications Tester, provide a check of the RS232 data communications link. During these tests, the 834 accumulates error information that identifies communication link failures. When the tests are complete, test results stored in the 834 may be examined to determine the operational status of the communication link.

The 1240 does not report any errors during this manual test. It is used, however, during the BERT testing. First, the 1240 reads the data ready bit from the RS232 link. If the data ready bit is active, the 1240 reads the incoming data and stores it in a processor register. Next, the 1240 reads the transmitter buffer status bit to determine if the transmitter is ready for data. When it is ready, the data stored in the processor register is written to the transmitter buffer.

1240 SETUP FOR BERT TEST

Program the 1240 menus as follows:

1. Power down the 1240 and install an RS232 COMM pack in the door-covered slot on the rear of the instrument.
2. Power up the 1240 and enter diagnostics by simulating a keyboard failure (hold down a key during power-up).
3. Using the SELECT keys or the KNOB, choose the COMMPACK module and touch the MODULE DIAGNOSTIC soft key.
4. Choose the MANUAL area and touch the AREA DIAGNOSTICS soft key.
5. Press the START key and set the desired baud rate (50 to 9600 baud).

834 SETUP FOR BERT TEST

Set up the 834 as follows:

1. Remove the interconnect cable and jumper wires from the 834 storage compartment (bottom of the 834).
2. Open switches 2 and 3 on the Interface Access panel; all other switches should be closed.
3. Using the jumper wires, connect pin 2 of the Interface Access panel to the pin labeled RXD, then connect pin 3 to TXD.
4. Connect the male end of the interconnect cable to the 834, then connect the female end of the cable to the 1240 RS232 COMM pack.
5. Power on the 834.

6. Turn the MODE switch to BERT, then press the SETUP key.
7. Using the left- or right-arrow keys, select the same baud rate (50 to 9600 baud) as previously set in the 1240 menu.
8. Press the down-arrow twice. Select the test length (in total bits received per test) with the left- or right-arrow keys according to your testing needs:
   - 10E5: 100,000 bits
   - 10E6: 1,000,000 bits
   - CONT: continuous testing for intermittent failures until STOP is pressed
9. Press the down-arrow key once, then select ASYNC (with the left- or right-arrow keys).
10. Press the down-arrow key once, then select BITS/CHR=8.
11. Press the down-arrow key once, then select PARITY=EVEN.
12. Press the down-arrow key once, then select STOPBITS=2.
13. Press the START key.

BERT TEST RESULTS

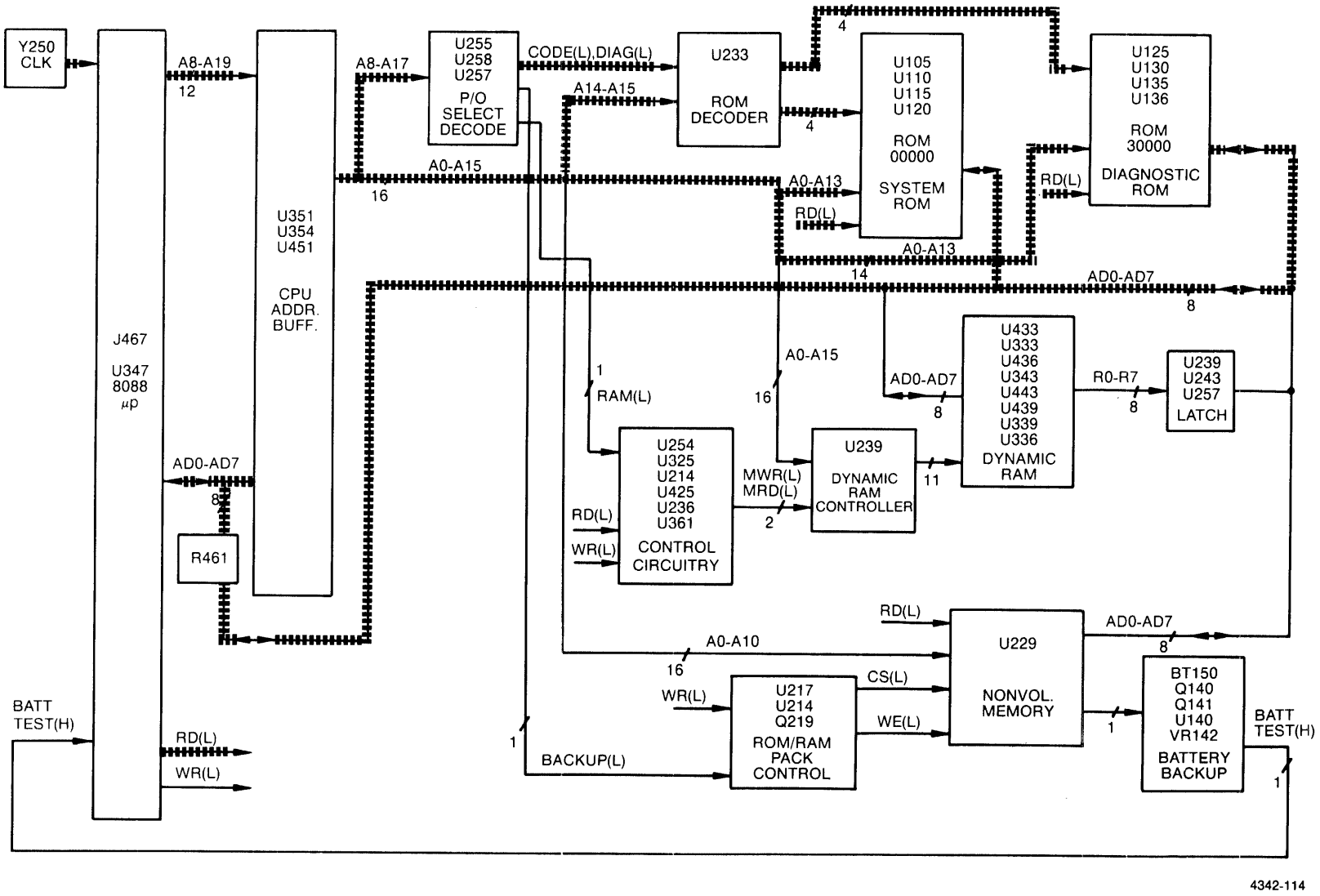
The BERT test is now running. Check that the 834's NO SYN LED is not lighted. Using the up- and down-arrow keys, you can examine bit errors, block errors, blocks, and faults. The number of tested blocks will increment while the test is running. No bit errors, block errors, or faults should occur.

When testing is complete, the 834 displays BERT TEST DONE. Note, however, that this does not indicate the tests have passed. To review the test results, press the DATA key and use the up- or down-arrow keys. There should be no errors.

5XXX CONTROL PROCESSOR ERROR INDEXES

Error Index	Area Name	Area Number
51XX	EPROM COMP	AREA 1
52XX	EPROM CSUM	AREA 2
53XX	EPROM PAGE	AREA 3
54XX	RAM	AREA 4
55XX	NVM	AREA 5

CONTROL PROCESSOR BLOCK DIAGRAM
EPROM COMP – AREA 1



4342-114

Figure 8-67. Control Processor EPROM COMP block diagram.

CONTROL PROCESSOR BOARD – COMPONENT LOCATION

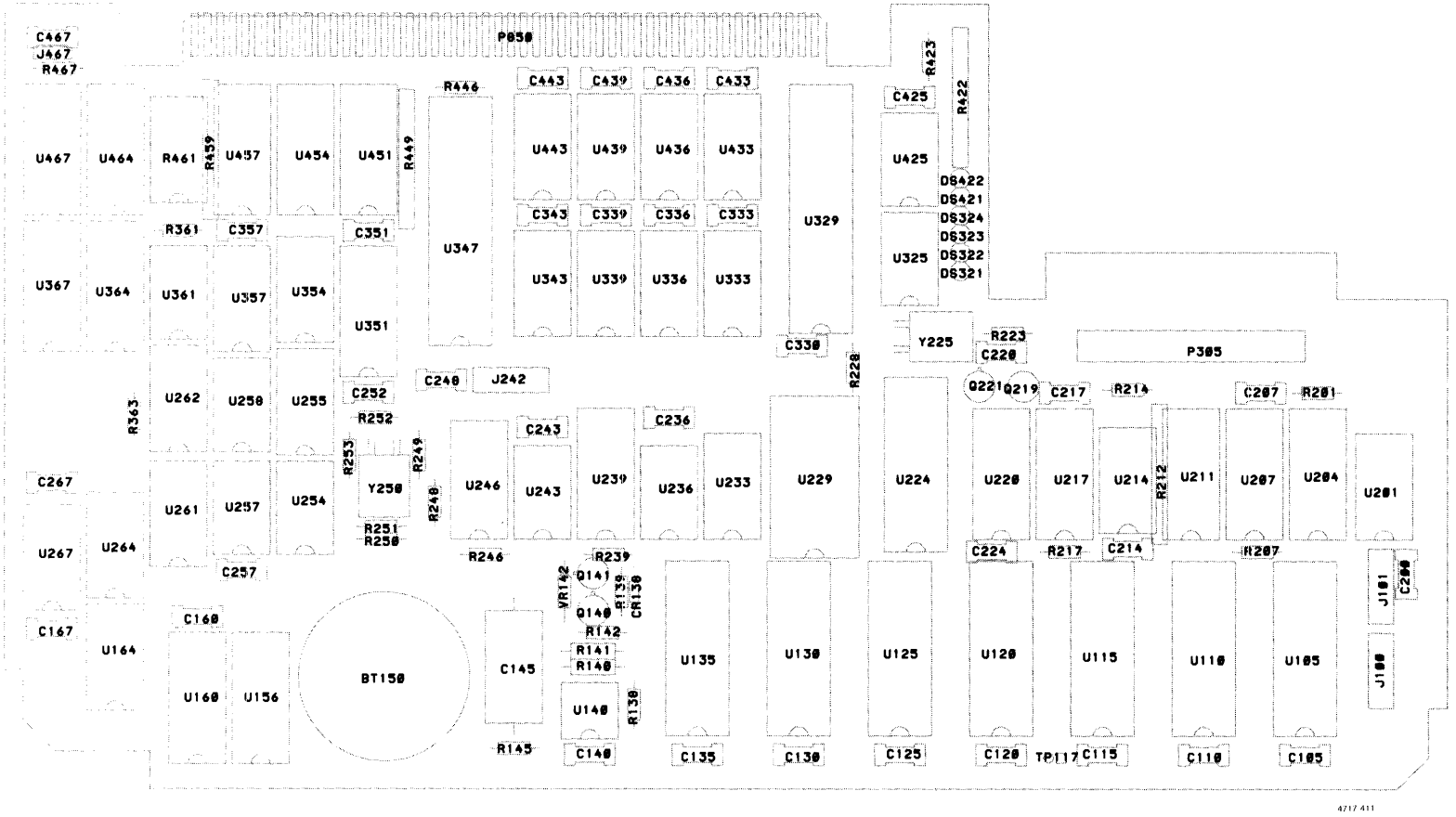


Figure 8-68. Control Processor Board component location.

module: CONTROL
area: EPROM COMP

EPROM COMP AREA – CIRCUIT OVERVIEW

The Control Processor EPROM COMP complementary byte circuitry is indicated by the shaded path on the block diagram. (The shading indicates circuitry exercised for the first time during diagnostic testing.) The 8088 microprocessor addresses the ROMs via address lines A0-A15. Select decoder A9U255 supplies two signals CODE(L) and DIAG(L) to the ROM decoder A9U233, which enables the specific ROM being read. The microprocessor reads back ROM data through the resistor pack A9R461 on the bidirectional address/data lines D0-D7.

EPROM COMP AREA – TEST DESCRIPTION

The ROM bytes at ROM-end-minus-three and ROM-end-minus-two are compared to see if they are complementary. This tests the ROM's ability to drive the address and data bus both logic high and low on all bits. Each routine tests one of the eight ROMs on the Control Processor Board. If the test detects an error, the corresponding error index is displayed on the 1240 screen and the next ROM is checked.

ROUTINE 1 DESCRIPTION

The bytes at address locations $03FFC_{hex}$ and $03FFD_{hex}$ of ROM A9U105 are compared to see if they are complementary.

5111
5121

5111 Error Index

Explanation: The bytes at address locations $03FFC_{hex}$ and $03FFD_{hex}$ were found not to be complementary.

Probable Cause	Action
Bad ROM.	Suspect ROM A9U105.

ROUTINE 2 DESCRIPTION

The bytes at address locations $07FFC_{hex}$ and $07FFD_{hex}$ of ROM A9U110 are compared to see if they are complementary.

5121 Error Index

Explanation: The bytes at address locations $07FFC_{hex}$ and $07FFD_{hex}$ were found not to be complementary.

Probable Cause	Action
Bad ROM.	Suspect ROM A9U110.

ROUTINE 3 DESCRIPTION

The bytes at address locations 0BFFC$_{hex}$ and 0BFFD$_{hex}$ of ROM A9U115 are compared to see if they are complementary.

5131 Error Index

Explanation: The bytes at address locations 0BFFC$_{hex}$ and 0BFFD$_{hex}$ were found not to be complementary.

Probable Cause	Action
Bad ROM.	Suspect ROM A9U115.

ROUTINE 4 DESCRIPTION

The bytes at address locations 0FFFC$_{hex}$ and 0FFFD$_{hex}$ of ROM A9U120 are compared to see if they are complementary.

5141 Error Index

Explanation: The bytes at address locations 0FFFC$_{hex}$ and 0FFFD$_{hex}$ were found not to be complementary.

Probable Cause	Action
Bad ROM.	Suspect ROM A9U120.

ROUTINE 5 DESCRIPTION

The bytes at address locations F3FFC$_{hex}$ and F3FFD$_{hex}$ of ROM A9U224 are compared to see if they are complementary.

5151 Error Index

Explanation: The bytes at address locations F3FFC$_{hex}$ and F3FFD$_{hex}$ were found not to be complementary.

Probable Cause	Action
Bad ROM.	Suspect ROM A9U224.

ROUTINE 6 DESCRIPTION

The bytes at address locations F7FFC$_{hex}$ and F7FFD$_{hex}$ of ROM A9U125 are compared to see if they are complementary.

5161 Error Index

Explanation: The bytes at address locations F7FFC$_{hex}$ and F7FFD$_{hex}$ were found not to be complementary.

Probable Cause	Action
Bad ROM.	Suspect ROM A9U125.

ROUTINE 7 DESCRIPTION

The bytes at address locations FBFFC$_{hex}$ and FBFFD$_{hex}$ of ROM A9U130 are compared to see if they are complementary.

5171 Error Index

Explanation: The bytes at address locations FBFFC$_{hex}$ and FBFFD$_{hex}$ were found not to be complementary.

Probable Cause	Action
Bad ROM.	Suspect ROM A9U130.

ROUTINE 8 DESCRIPTION

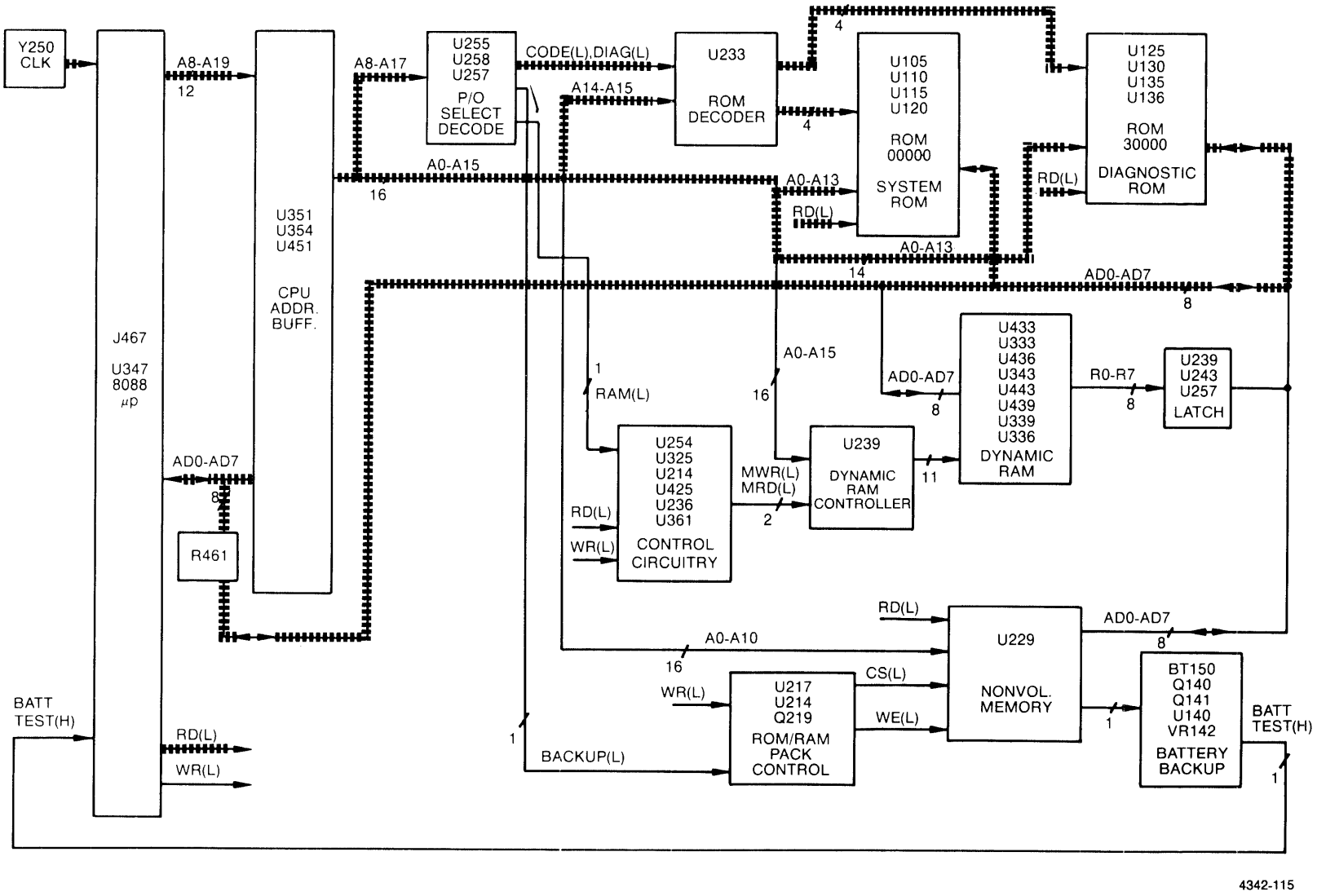
The bytes at address locations FFFFC$_{hex}$ and FFFFD$_{hex}$ of ROM A9U135 are compared to see if they are complementary.

5181 Error Index

Explanation: The bytes at address locations FFFFC$_{hex}$ and FFFFD$_{hex}$ were found not to be complementary.

Probable Cause	Action
Bad ROM.	Suspect ROM A9U135.

CONTROL PROCESSOR BLOCK DIAGRAM
EPROM CHECKSUM – AREA 2



4342-115

Figure 8-69. Control Processor EPROM CSUM block diagram.

CONTROL PROCESSOR BOARD – COMPONENT LOCATION

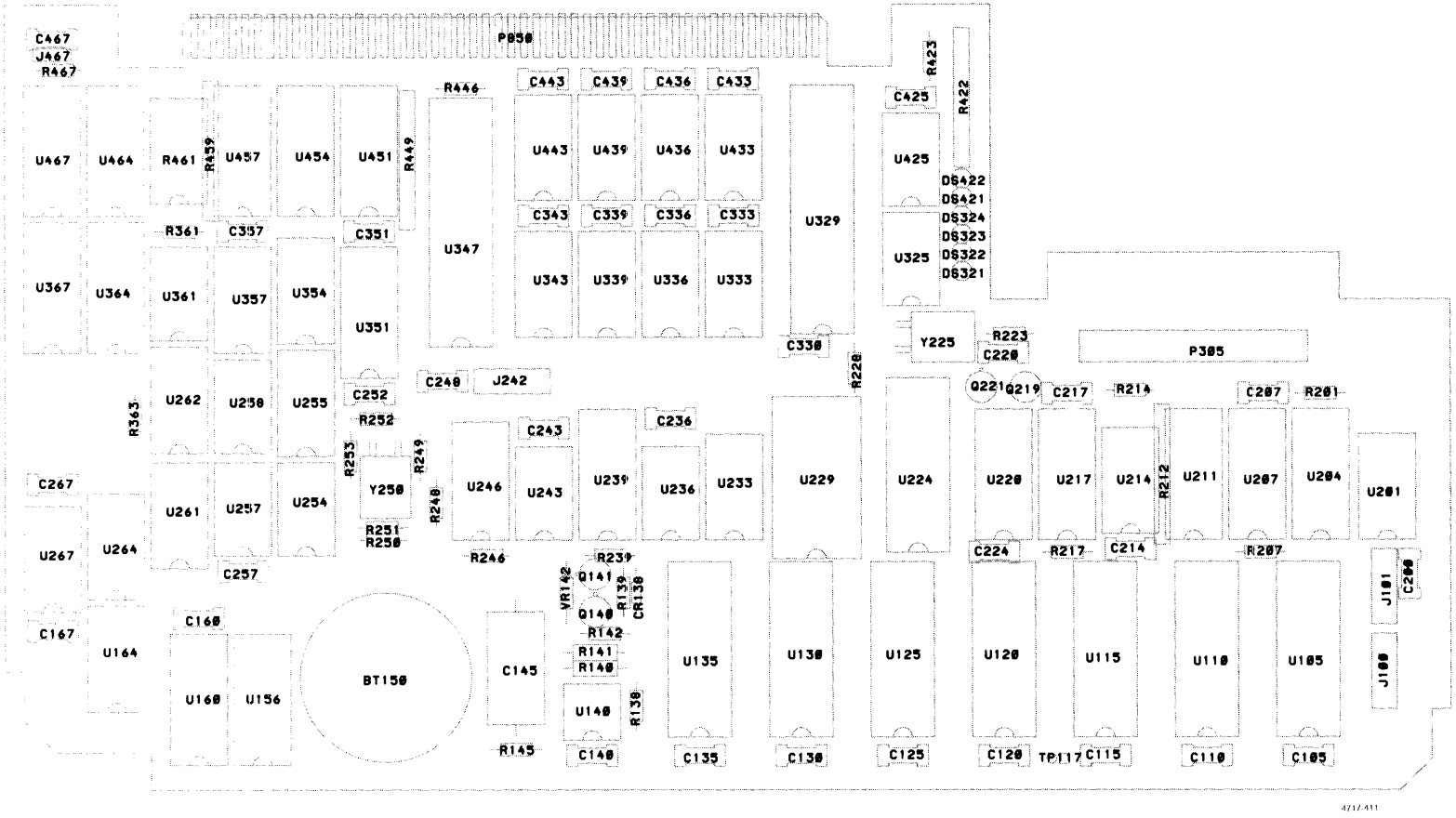


Figure 8-70. Control Processor Board component location.

module: CONTROL
area: EPROM CSUM

EPROM CHECKSUM AREA – CIRCUIT OVERVIEW

The Control Processor EPROM CSUM checksum circuitry is indicated by the shaded path on the block diagram. (The shading indicates circuitry exercised for the first time during diagnostic testing.) The 8088 microprocessor addresses the ROMs with address lines A0-A15. Select decoder A9U255 supplies two signals CODE(L) and DIAG(L)to the ROM decoder A9U233, which enables the specific ROM being read. The microprocessor reads back ROM data through the resistor pack A9R461 on the bidirectional address/data lines D0-D7.

EPROM CHECKSUM AREA – TEST DESCRIPTION

The checksum for each ROM on the Control Processor Board is calculated. The calculated checksum is compared to an expected value that is stored in the last two locations of the ROM. The calculated and expected checksum values are then written to the 1240 display screen.

ROUTINE 1 DESCRIPTION

The test calculates the checksum for ROM A9U105.

5211 Error Index

Explanation: The calculated checksum for ROM A9U105 did not match the expected checksum.

5211
5221

Probable Cause	Action
Bad ROM.	Suspect ROM A9U105.

ROUTINE 2 DESCRIPTION

The test calculates the checksum for ROM A9U110.

5221 Error Index

Explanation: The calculated checksum for ROM A9U110 did not match the expected checksum.

Probable Cause	Action
Bad ROM.	Suspect ROM A9U110.

ROUTINE 3 DESCRIPTION

The test calculates the checksum for ROM A9U115.

5231 Error Index

Explanation: The calculated checksum for ROM A9U115 did not match the expected checksum.

Probable Cause	Action
Bad ROM.	Suspect ROM A9U115.

ROUTINE 4 DESCRIPTION

The test calculates the checksum for ROM A9U120.

5241 Error Index

Explanation: The calculated checksum for ROM A9U120 did not match the expected checksum.

Probable Cause	Action
Bad ROM.	Suspect ROM A9U120.

ROUTINE 5 DESCRIPTION

The test calculates the checksum for ROM A9U224.

5251 Error Index

Explanation: The calculated checksum for ROM A9U224 did not match the expected checksum.

Probable Cause	Action
Bad ROM.	Suspect ROM A9U224.

ROUTINE 6 DESCRIPTION

The test calculates the checksum for ROM A9U125.

5261 Error Index

Explanation: The calculated checksum for ROM A9U125 did not match the expected checksum.

Probable Cause	Action
Bad ROM.	Suspect ROM A9U125.

ROUTINE 7 DESCRIPTION

The test calculates the checksum for ROM A9U130.

5271 Error Index

Explanation: The calculated checksum for ROM A9U130 did not match the expected checksum.

Probable Cause	Action
Bad ROM.	Suspect ROM A9U130.

ROUTINE 8 DESCRIPTION

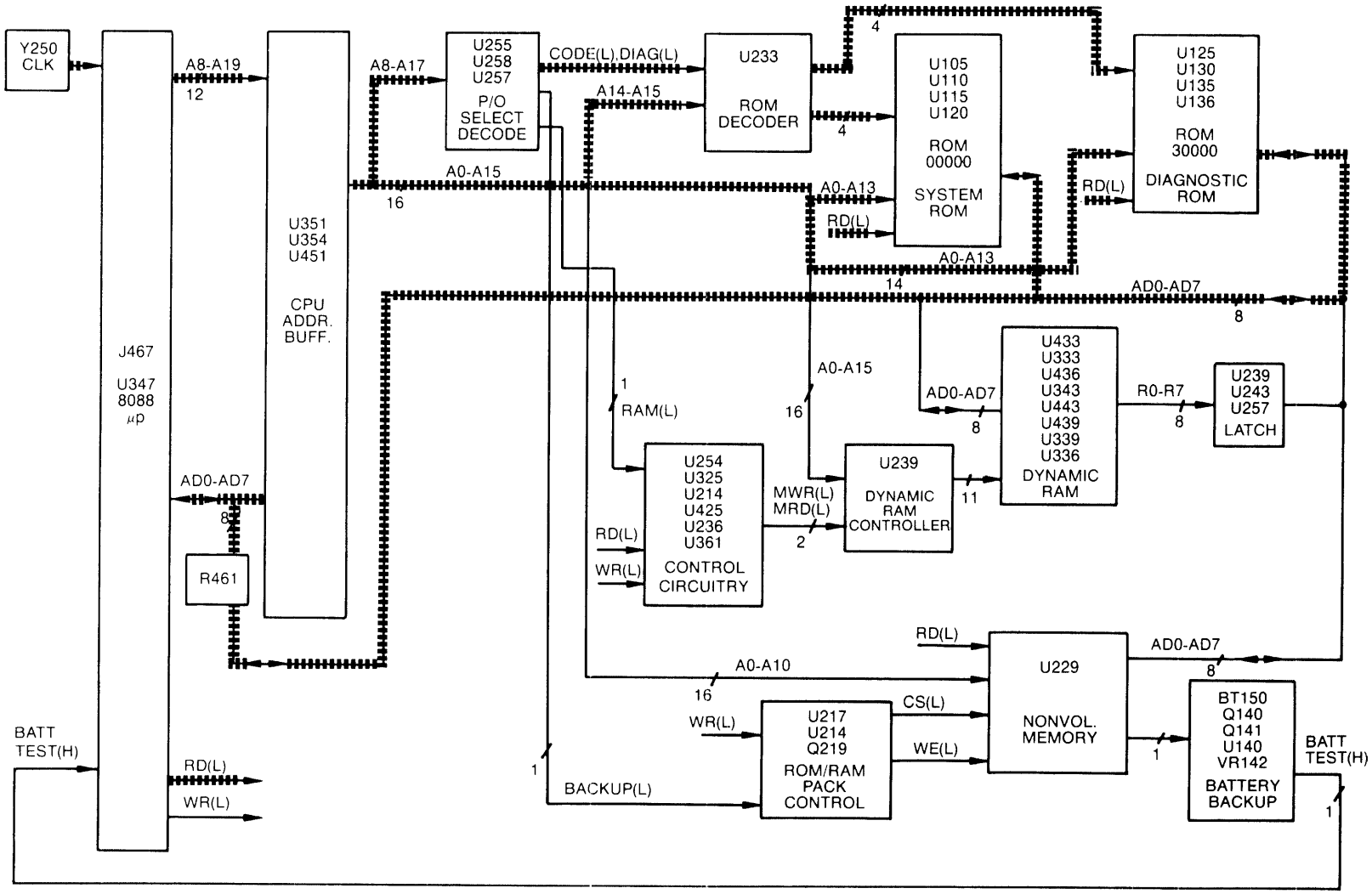
The test calculates the checksum for ROM A9U135.

5281 Error Index

Explanation: The calculated checksum for ROM A9U135 did not match the expected checksum.

Probable Cause	Action
Bad ROM.	Suspect ROM A9U135.

CONTROL PROCESSOR BLOCK DIAGRAM
EPROM PAGE – AREA 3



4342-116

Figure 8-71. Control Processor EPROM PAGE block diagram.

CONTROL PROCESSOR BOARD – COMPONENT LOCATION

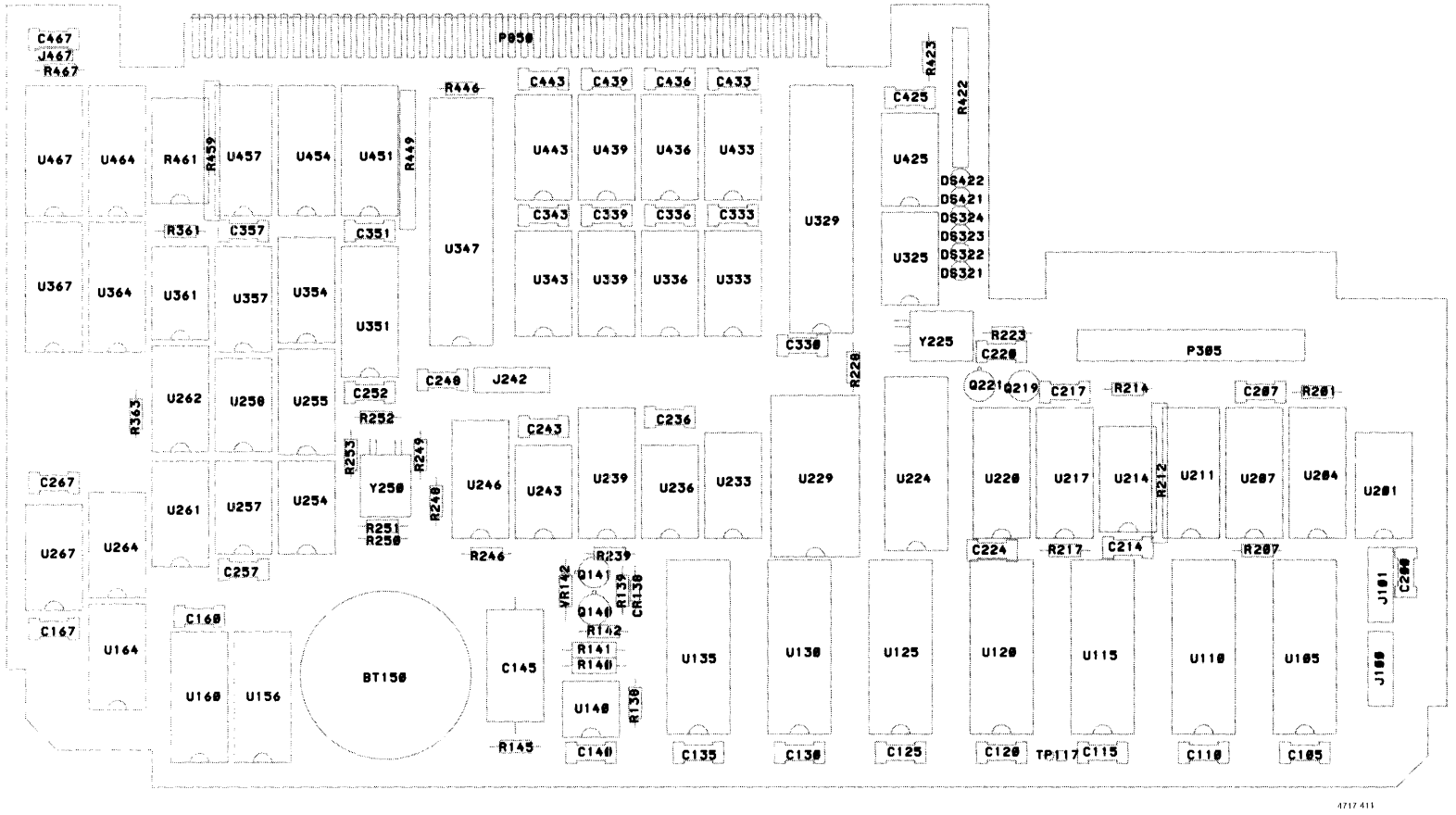


Figure 8-72. Control Processor Board component location.

module: CONTROL
area: EPROM PAGE

EPROM PAGE AREA – CIRCUIT OVERVIEW

The Control Processor EPROM PAGE circuitry is indicated by the shaded path on the block diagram. (The shading indicates circuitry exercised for the first time during diagnostic testing.) The 8088 microprocessor addresses the ROMs with address lines A0-A15. Select decoder A9U255 supplies two signals CODE(L) and DIAG(L) to the ROM decoder A9U233, which enables the specific ROM being read. The microprocessor reads back ROM data through the resistor pack A9R461 on the bidirectional address/data lines D0-D7.

EPROM PAGE AREA – TEST DESCRIPTION

The byte at ROM-end-minus-7 is checked to see if each ROM on the Control Procesor Board is in the correct socket. For example, if the ROM resides at address location 00000_{hex}-$03FFF_{hex}$, then the byte at ROM-end-minus-7 should be 03.

ROUTINE 1 DESCRIPTION

The test checks the page address value at address $03FF8_{hex}$ for ROM A9U105.

NOTE

The address value displayed on the 1240 screen indicates the middle four digits of the ROM's part number.

5311

5311 Error Index

Explanation: The page address value is incorrect, expected 03.

Probable Cause	Action
ROM A9U105 not in the correct socket.	Move ROM A9U105 to the correct socket.

If Actual Data Is	Correct Location Is
07	A9U110
0B	A9U115
0F	A9U120
F3	A9U224
F7	A9U125
FB	A9U130
FF	A9U135

ROUTINE 2 DESCRIPTION

The test checks the page address value at address 07FF8$_{hex}$ for ROM A9U110.

NOTE

The address value displayed on the 1240 screen indicates the middle four digits of the ROM's part number.

5321 Error Index

Explanation: The page address value is incorrect, expected 07.

Probable Cause	Action
ROM A9U110 not in the correct socket.	Move ROM A9U110 to the correct socket.

If Actual Data Is	Correct Location Is
03	A9U105
0B	A9U115
0F	A9U120
F3	A9U224
F7	A9U125
FB	A9U130
FF	A9U135

ROUTINE 3 DESCRIPTION

The test checks the page address value at address 0BFF8$_{hex}$ for ROM A9U115.

NOTE

The address value displayed on the 1240 screen indicates the middle four digits of the ROM's part number.

5331 Error Index

Explanation: The page address value is incorrect, expected 0B.

Probable Cause	Action
ROM A9U115 not in the correct socket.	Move ROM A9U115 to the correct socket.

If Actual Data Is	Correct Location Is
03	A9U105
07	A9U110
0F	A9U120
F3	A9U224
F7	A9U125
FB	A9U130
FF	A9U135

ROUTINE 4 DESCRIPTION

The test checks the page address value at address 0FFF8$_{hex}$ for ROM A9U120.

5341

NOTE

The address value displayed on the 1240 screen indicates the middle four digits of the ROM's part number.

5341 Error Index

Explanation: The page address value is incorrect, expected 0F.

Probable Cause	Action
ROM A9U120 not in the correct socket.	Move ROM A9U120 to the correct socket.

If Actual Data Is	Correct Location Is
03	A9U105
07	A9U110
F3	A9U224
F7	A9U125
FB	A9U130
FF	A9U135

ROUTINE 5 DESCRIPTION

The test checks the page address value at address F3FF8$_{hex}$ for ROM A9U224.

NOTE

The address value displayed on the 1240 screen indicates the middle four digits of the ROM's part number.

5351 Error Index

Explanation: The page address value is incorrect, expected F3.

Probable Cause	Action
ROM A9U224 not in the correct socket.	Move ROM A9U224 to the correct socket.

If Actual Data Is	Correct Location Is
03	A9U105
07	A9U110
0F	A9U120
F7	A9U125
FB	A9U130
FF	A9U135

ROUTINE 6 DESCRIPTION

The test checks the page address value at address F7FF8$_{hex}$ for ROM A9U125.

NOTE

The address value displayed on the 1240 screen indicates the middle four digits of the ROM's part number.

5361 Error Index

Explanation: The page address value is incorrect, expected F7.

Probable Cause	Action
ROM A9U125 not in the correct socket.	Move ROM A9U125 to the correct socket.

If Actual Data Is	Correct Location Is
03	A9U105
07	A9U110
0F	A9U120
F3	A9U224
FB	A9U130
FF	A9U135

ROUTINE 7 DESCRIPTION

The test checks the page address value at address FBFF8$_{hex}$ for ROM A9U130.

NOTE

The address value displayed on the 1240 screen indicates the middle four digits of the ROM's part number.

5371

5371 Error Index

Explanation: The page address value is incorrect, expected FB.

Probable Cause	Action
ROM A9U130 not in the correct socket.	Move ROM A9U130 to the correct socket.

If Actual Data Is	Correct Location Is
03	A9U105
07	A9U110
0F	A9U120
F3	A9U224
F7	A9U125
FF	A9U135

ROUTINE 8 DESCRIPTION

The test checks the page address value at address FFFF8$_{hex}$ for ROM A9U135.

NOTE

The address value displayed on the 1240 screen indicates the middle four digits of the ROM's part number.

5381 Error Index

Explanation: The page address value is incorrect, expected FF.

Probable Cause	Action
ROM A9U135 not in the correct socket.	Move ROM A9U135 to the correct socket.

If Actual Data Is	Correct Location Is
03	A9U105
07	A9U110
0F	A9U120
F3	A9U224
F7	A9U125
FB	A9U130

CONTROL PROCESSOR BLOCK DIAGRAM
RAM – AREA 4

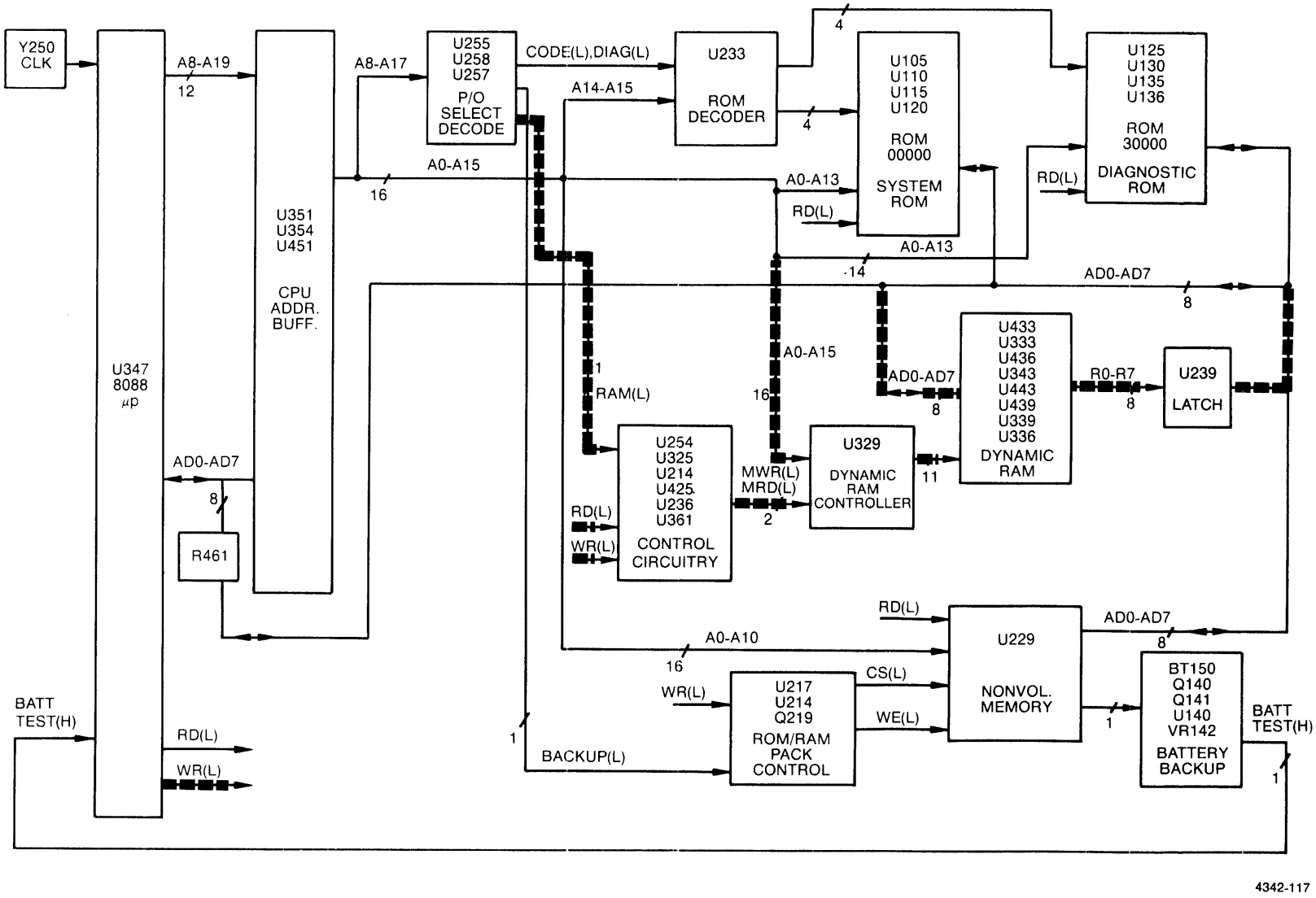


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Figure 8-73. Control Processor RAM block diagram.

CONTROL PROCESSOR BOARD – COMPONENT LOCATION

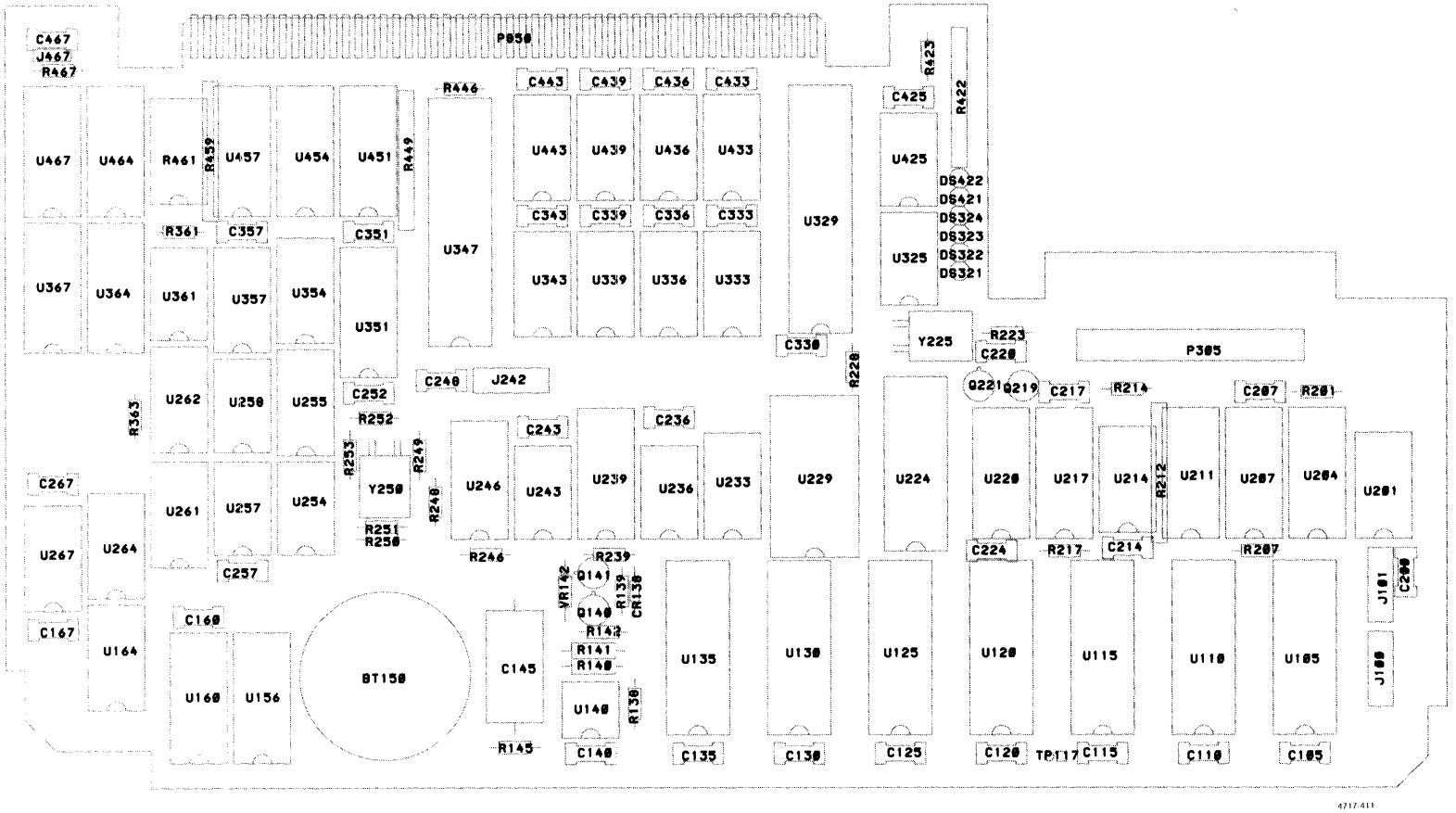

Figure 8-74. Control Processor Board component location.

module: CONTROL
area: RAM

RAM AREA – CIRCUIT OVERVIEW

The Control Processor RAM circuitry is indicated by the shaded path on the block diagram. (The shading indicates circuitry exercised for the first time during diagnostic testing.) The 8088 microprocessor addresses the dynamic RAMs with address lines A0-A15 and dynamic RAM controller A9U329. A9U325 supplies the memory read MRD(L) and write MWR(L) signals to the RAM controller, U239. The microprocessor reads back data from the RAMs through the latch A9U239 on bidirectional address/data lines D0-D7.

RAM AREA – TEST DESCRIPTION

The RAM tests check to see that all address and data lines are independent of each other. Testing of the dynamic RAM is done in two address partitions to preserve RAM data required for diagnostic testing. First tested are locations 23000_{hex} to $2F7FF_{hex}$, then 20000_{hex} to $22FFF_{hex}$. If address locations 23000_{hex} to $2F7FF_{hex}$ pass the test, the values at locations 20000_{hex} to $22FFF_{hex}$ are moved to the previously tested address locations. Now, address locations 20000_{hex} to $22FFF_{hex}$ are tested in the same manner. After testing, all data is restored to its original location. The 1240 displays expected and actual data. The bit that fails indicates the bad RAM.

ROUTINE 1 DESCRIPTION

5411

The Dynamic RAM data-bit-independence test checks to see that each of the eight data bits in a byte of RAM are independent of each other. The RAM is tested in two parts, first address locations 23000_{hex} to $2F7FF_{hex}$, then 20000_{hex} to $22FFF_{hex}$. This test begins by writing the pattern 00_{hex} to all locations within the specified address range. The last location is read and checked for 00_{hex}. If it contains the correct information, then 01_{hex} is written to that location. The last location is checked, and if 01_{hex} is present, 02_{hex} is written. Again, the last location is checked for 02_{hex}. This test sequence continues by writing and reading the values 04_{hex}, 08_{hex}, 10_{hex}, 20_{hex}, 40_{hex}, and 80_{hex}. When testing of the upper address range is complete, the contents of the lower address RAM locations is copied into upper RAM. The same write/read sequence is used to check data-bit-independence for the lower part of RAM.

5411 Error Index

Explanation: The Dynamic RAM data-bit-independence test failed. Using the following table, determine which RAM failed from the actual and expected data information on the 1240 screen. The failed bit indicates the bad RAM.

Probable Cause	Action
Bad RAM.	Compare the expected and actual screen data to determine which RAM is bad. Verify the RAM is bad by observing the RAM read/write operation with a logic analyzer. The following table shows the data bit and the RAM responsible for that bit.

Data bit	RAM
0	A9U433
1	A9U333
2	A9U436
3	A9U343
4	A9U443
5	A9U439
6	A9U339
7	A9U336

ROUTINE 2 DESCRIPTION

The Dynamic RAM address-line-independence test checks to see that each of the address lines to the RAM are independent of each other, and that each bit in each RAM can be set high and low. The RAM is tested in two parts, first addresses 23000_{hex} to $2F7FF_{hex}$, then 20000_{hex} to $22FFF_{hex}$.

The test begins by writing the pattern AA_{hex} to all locations within the specified address range. The last location is read and checked for AA_{hex}. If it contains the correct information, then 55_{hex} is written to that location. The address is decremented and the last location is read and checked for AA_{hex}. If it contains AA_{hex}, 55_{hex} is written and then checked. If 55_{hex} is present, the address under test is again decremented and the process is repeated until the end of the specified address range. When the last location is reached, the test checks for 55_{hex} and if present, the contents of the lower address RAM locations is copied into upper RAM. The same read/write sequence is used to check address-line-independence for the lower part of RAM. After all testing is complete, the saved contents of upper RAM is restored to lower RAM.

5421 Error Index

Explanation: The Dynamic RAM address-line-independence test failed. Using the the actual and expected data information on the 1240 screen, determine whether the failure was caused from an address line or a failed RAM (indicated by the following table).

Probable Cause	Action
Bad RAM or address line.	The test is now reading and writing the failed location. Use the screen address information or a logic analyzer to determine the processor looping address. If the failing address value is one that requires an address line to change for the first time, then suspect that address line to be open or shorted. If the failing address value is not one that required an address line to change for the first time, then suspect a RAM failure. Verify a RAM failure by using a logic analyzer and observing the read/write loop operation. Use the following table to determine the RAM responsible for each bit.

Data bit	RAM
0	A9U433
1	A9U333
2	A9U436
3	A9U343
4	A9U443
5	A9U439
6	A9U339
7	A9U336

ROUTINE 3 DESCRIPTION

This test checks the refresh operation of the Dynamic RAM. The RAM is tested in two parts, first addresses 23000_{hex} to $2F7FF_{hex}$, then 20000_{hex} to $22FFF_{hex}$. This test begins by writing the pattern AA_{hex} to all locations within the specified address range. The test waits for one second and all RAM locations under test are read and checked for AA_{hex}. If AA_{hex} is present, then the test writes 55_{hex} to all locations. The test waits for one second then rechecks all locations for 55_{hex}. If no problems are detected, the contents of the lower address RAM locations is copied into upper RAM. The same write/read sequence is used to check address-line-independence for the lower part of RAM. After all testing is complete, the saved contents of upper RAM is restored to lower RAM.

5431 Error Index

Explanation: The Dynamic RAM refresh test failed. Using the actual and expected data information on the 1240 screen and the following table, determine which RAM failed. The failed bit indicates the bad RAM.

Probable Cause	Action
Bad RAM	Compare the expected and actual screen data to determine which RAM is bad. Verify the RAM is bad by observing the RAM read/write operation with a logic analyzer. The follwoing table shows the data bit and the RAM responsible for that bit.

Data bit	RAM
0	A9U433
1	A9U333
2	A9U436
3	A9U343
4	A9U443
5	A9U439
6	A9U339
7	A9U336

CONTROL PROCESSOR BLOCK DIAGRAM
NONVOLATILE MEMORY – AREA 5

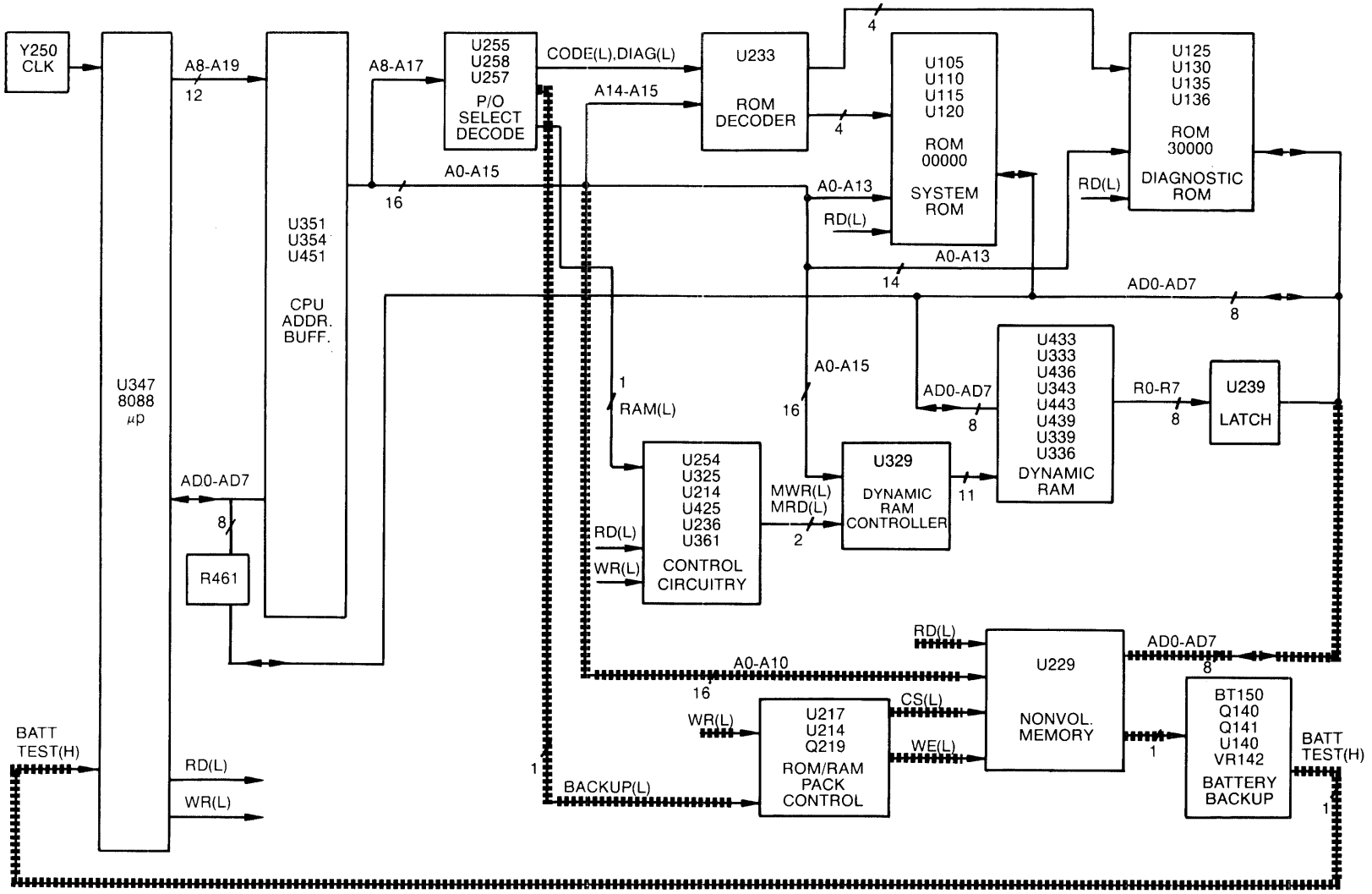

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Figure 8-75. Control Processor NVM block diagram.

CONTROL PROCESSOR BOARD – COMPONENT LOCATION

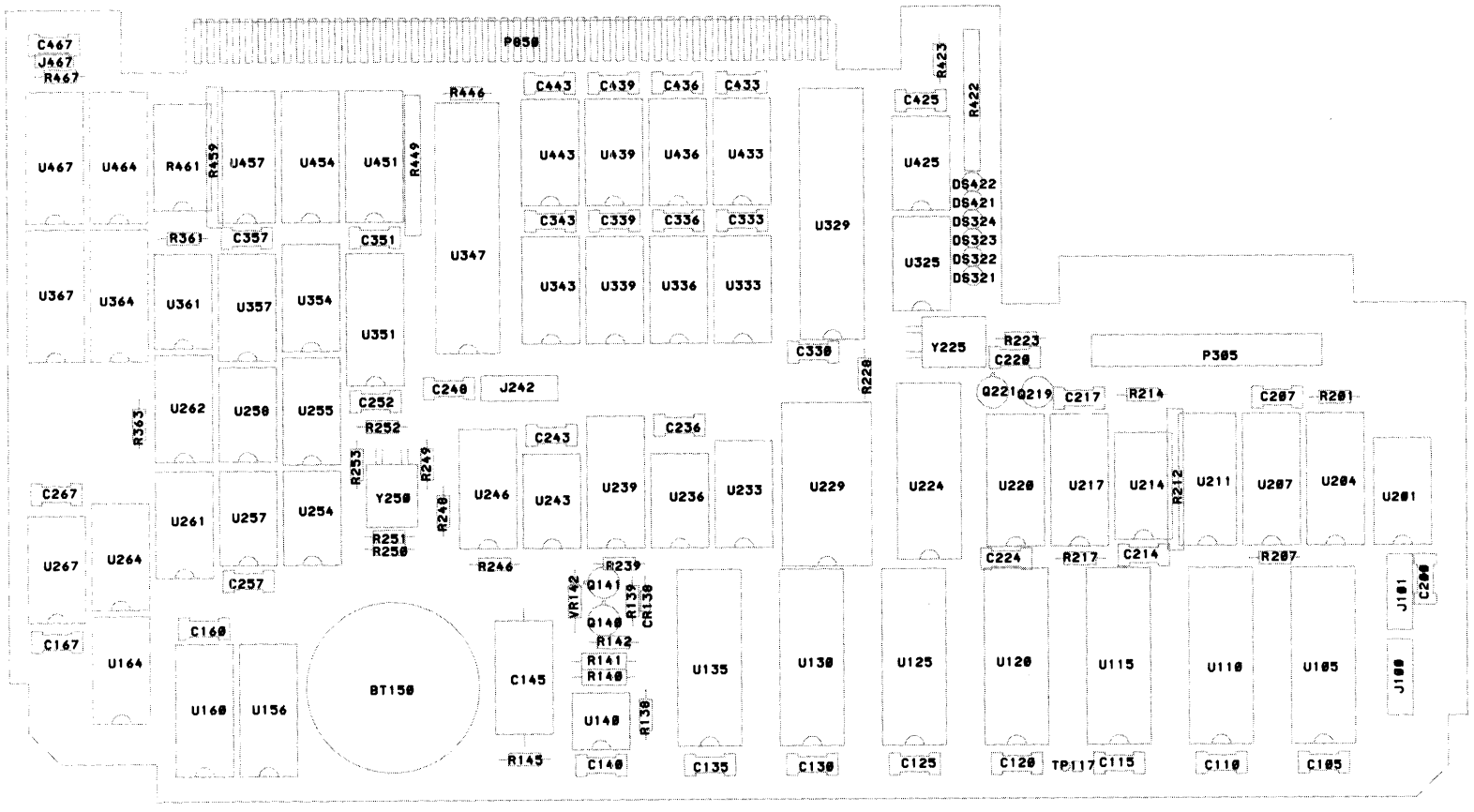

Figure 8-76. Control Processor Board component location.

module: CONTROL
area: NVM

NONVOLATILE MEMORY AREA – CIRCUIT OVERVIEW

The Control Processor nonvolatile RAM circuitry is indicated by the shaded path on the block diagram. (The shading indicates circuitry exercised for the first time during diagnostic testing.) The microprocessor addresses the nonvolatile RAM with address lines A0-A10 and latch A9U217. The BATT TEST(H) output signal from the battery level detection circuitry feeds the 8088 interrupt input. This signal indicates when the RAM's backup-battery level is below 2.44 volts. The microprocessor reads back data from the nonvolatile memory through the resistor pack A9R461 on the bidirectional address/data lines D0-D7.

NONVOLATILE MEMORY AREA – TEST DESCRIPTION

First the battery level detection circuitry is checked to see if an interrupt can be detected when the battery voltage level is low. Next, the nonvolatile memory (NVM) is tested by saving the contents of one byte of the NVM in a register. The NVM is written to and read from for data-bit-independence verification, then the saved byte is replaced. Next, a portion of the Dynamic RAM is completely checked and, when verified, all data saved in the NVM is stored in the dynamic RAM. The NVM is then written to and read from for address-line-independence verification. After testing, the data stored in the Dynamic RAM is restored to the NVM.

ROUTINE 1 DESCRIPTION

5511

The test checks to see if an interrupt was recognized from the battery level detection circuitry. If an interrupt has been generated, the test fails (indicating the battery level is low).

5511 Error Index

Explanation: The battery voltage level for the nonvolatile RAM is less than 2.44 volts.

Probable Cause	Action
Low or dead battery	Suspect battery A9BT150

ROUTINE 2 DESCRIPTION

The nonvolatile memory (NVM) data-bit-independence test starts by saving the contents of one byte from the NVM in a processor register. The now-empty byte is filled with AA_{hex} and then read back. Next CC_{hex} is written and checked. Then $F0_{hex}$ is written and checked, and finally $0F_{hex}$ is written and read back. After testing, the original data is restored to the NVM test location. A failure at any point in the testing produces an on-screen error code accompanying the failed address and data information.

At power-up, the diagnostics test only one memory location as previously described. During normal diagnostics, all NVM locations are checked as previously described.

5521 Error Index

Explanation: The nonvolatile memory data-bit-independence test failed.

Probable Cause	Action
Bad nonvolatile memory	Suspect nonvolatile RAM A9U229

ROUTINE 3 DESCRIPTION

The test starts by verifying the operation of the Dynamic RAM between address locations 23000_{hex} and $237FF_{hex}$. If a failure is detected, the test fails and the failed Dynamic RAM address and data information is displayed on the 1240 screen. If no failure is detected, the entire contents of nonvolatile memory (NVM) is moved to the now-verified Dynamic RAM. All locations of NVM are filled with zeros. The first address is checked for zero and, if present, FF_{hex} is written. The address is incremented and the next location is checked for zero and FF_{hex} is written to that location. This is repeated until the end of the NVM is reached. Finally, the entire NVM is checked for FF_{hex}. If a failure is detected, the failure information is displayed on the 1240 screen. After testing, the original data is restored to the NVM.

5531 Error Index

Explanation: An error was detected during the testing of Dynamic RAM. Using the following table, determine which RAM failed.

Probable Cause	Action
Bad RAM	Suspect the RAM

Data bit	RAM
0	A9U433
1	A9U333
2	A9U436
3	A9U343
4	A9U443
5	A9U439
6	A9U339
7	A9U336

5532 Error Index

Explanation: The nonvolatile memory address-bit-independence test failed.

Probable Cause	Action
Bad RAM	Suspect the nonvolatile memory A9U229

6XXX TRIGGER ERROR INDEXES

Error Index	Area Name	Area Number
61XX	SEQ CTRL	AREA 1
62XX	GLOBAL FILTER	AREA 2
63XX	SEQ FILTER	AREA 3
64XX	I COUNTER	AREA 4
65XX	TPI 1	AREA 5
66XX	TPI 2	AREA 6
67XX	CTR/TIMER	AREA 7
68XX	ATB	AREA 8
69XX	TIMING	AREA 9
6AXX	X SEQ CTL	AREA A

TRIGGER MANUAL TESTS

Module	Area	Routine	Description
TRIGGER	ATB MANUAL	1	Decade Divider Exerciser
	ATB MANUAL	2	ATB Base Rate Exerciser

TRIGGER BLOCK DIAGRAM
SEQUENTIAL CONTROL – AREA 1

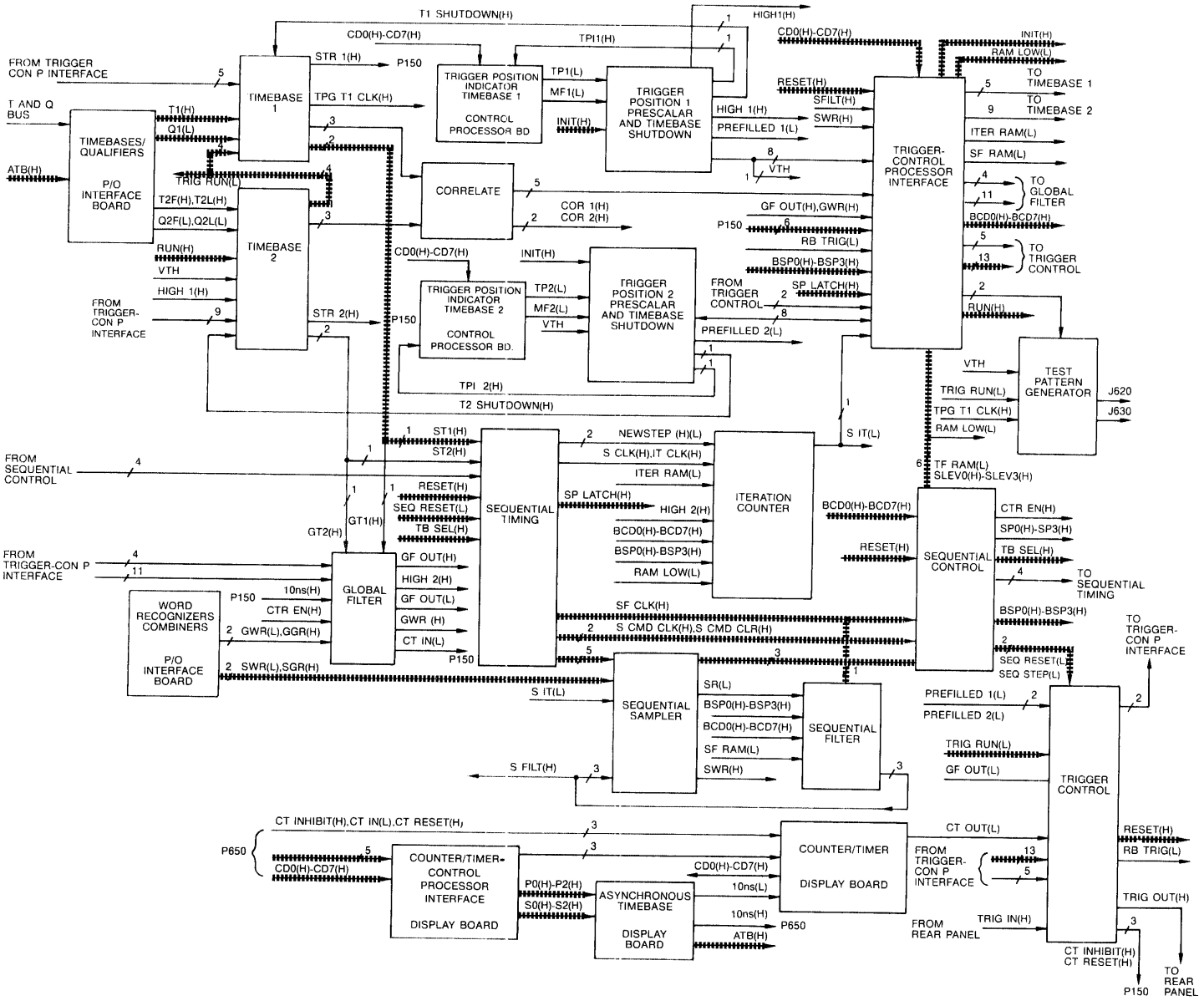

Figure 8-77. Trigger SEQ CTRL block diagram.

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TRIGGER BOARD – COMPONENT LOCATION

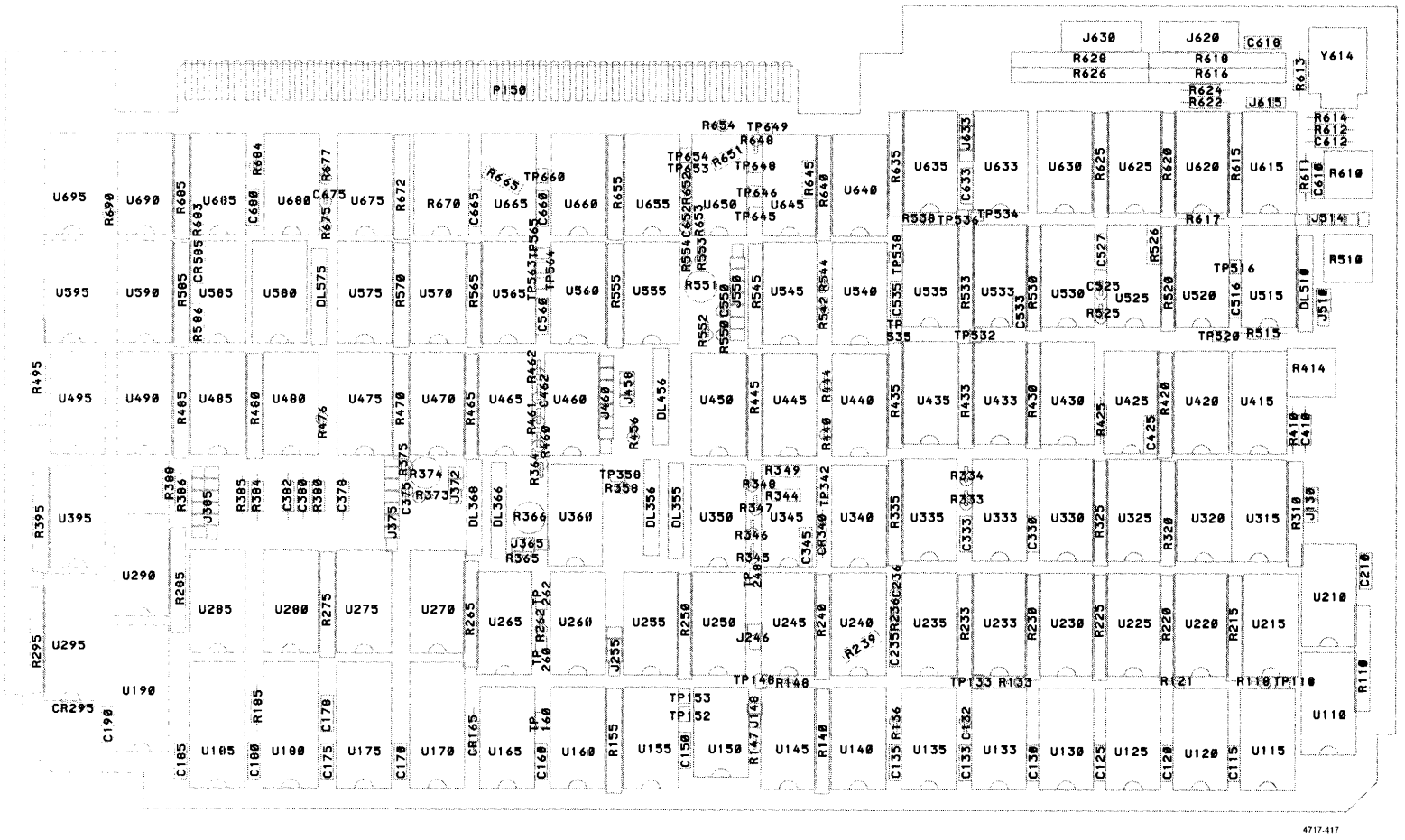

Figure 8-78. Trigger Board component location.

module: TRIGGER
area: SEQ CTRL

SEQUENTIAL CONTROL AREA – CIRCUIT OVERVIEW

The pattern-shaded signal lines on the timing block diagram indicate circuitry used during diagnostic testing. Only the circuitry that is being exercised for the first time during diagnostic testing is shown. Circuitry exercised by other diagnostic tests are shown in their respective block diagrams.

The sequence pointer tells the acquisition cards which word value to use for the sequence word and glitch recognizers.

One bit of the sequence pointer is produced by A14U630 through U640. RAM A14U135 holds the value that the sequence level will go to when a true event is found. RAM A14U235 holds the value that the sequence level goes to when a false event is found. The feedback on A14U630-U640 (pin 2 to pin 5), latches the value taken from the RAM and holds the value until a new true or false event is found.

Four different commands may be performed on each level of the sequence: do nothing, change level, reset the trigger machine, and trigger. RAM A14U330 holds the commands for all sequence levels (for both true and false events). Lines C0(H) and C2(H) are the command for a false event; C1(H) and C3(H) for a true event. A14U430 selects the command for either the true or false event and presents the command to A14U433 which latches it.

SEQ CTRL AREA – TEST DESCRIPTION

The sequential control tests check the ability of the sequence circuits to perform different tasks. First, two different test patterns, 05_{hex} and $0A_{hex}$, are written to the Sequential Control circuitry via A14U180 in the Trigger-Processor Interface. During readback, the patterns are buffered through A14U140, and sent to the Control Processor via A14U115 and U110 (in the Trigger-Processor Interface). If the patterns are read back correctly, the test proceeds to the next check.

Second, the test checks the ability of the sequence pointer to step when an event is found true and when the event is found not true. The Sequential Filter RAM, A14U333 and U335, is loaded (address $FF85_{hex}$) with DF_{hex} at all sequence pointer locations. (This means step when false, no reset, T1 sequence clock.) The TF RAM A14U135 and U235 (address $FF87_{hex}$ with RAM LOW(L) true) is loaded with EF_{hex} at all sequence pointer locations. (This means go to next step.) The TF RAM A14U330 and U540 (address $FF87_{hex}$ with RAM LOW(L) false)) is loaded with $1E_{hex}$ at all sequence pointer locations. (This means sequential filter value=1, level mode, SWR ON NOT.)

The sequence pointer is reset and 15 T1 clocks are generated by the Control Processor. The status of the sequence pointer is checked after each clock via A14U115, U110, and U140. If any errors are detected (the sequence pointer did not decrement after a clock), then the test is aborted and a failure is reported.

The SF RAM A14U333 and U335 (address $FF85_{hex}$) is loaded with DF_{hex} at all sequence pointer locations. (This means when true, no reset, T1 sequence clock.) The TF RAM A14U135 and U235 (address $FF87_{hex}$ with RAM LOW(L) true) is loaded $1D_{hex}$ at all sequence pointer locations. (This means go to next step, increment sequence pointer.) The TF RAM A14U330 and U540 is loaded with $1B_{hex}$ at all sequence pointer locations. (This means sequential filter = 1, level mode, SGR ON NOT.) The sequence pointer is reset and 15 T1 clocks are generated by the Control Processor. The status of the sequence pointer is checked after each clock via A14U115, U110, and U140. If any errors are detected (the sequence pointer did not decrement after a clock), then the test is aborted and a failure is reported.

Finally, the test verifies the ability of the sequence pointer to trigger on event true for each sequence level. The TF RAM A14U135 and U235 (address $FF87_{hex}$ with RAM LOW(L) true) is loaded with 15_{hex}. Timebase and store control (address $FF84_{hex}$) is loaded with $F2_{hex}$. (This means trig enable, asynchronous timebase enable, timebase 1 enable.) Trigger position control (address $FF83_{hex}$) is loaded with $B3_{hex}$. (This means no prefill, set RUN HIGH(H) true.)

The process previously described is performed before each pass, incrementing the sequence pointer before each pass. The Control Processor generates 16 T1 clocks. After each clock, the trigger status bit is read back via A14U285-11. The bit should be high for the first pass. The readback data should be 16 sets of the value 02_{hex}. On the second pass, the read back data is 15 sets of 02_{hex} and one set of 00_{hex}. The pattern repeats with the third pass, reading back 14 sets of 02_{hex} and two sets of 00_{hex}. For pass number 16, the readback data should be 16 sets of 00_{hex}.

6111 Error Index

Explanation: The sequence pointer does not appear to be set at 05_{hex}.

Probable Cause	Action
The data bus buffer, A14U295 in the Trigger-Processor Interface, is not working correctly.	Verify that the chip enable signal on A14U295-19 is pulsing low while the test is looping. Check that the data direction signal on pin 1 is working properly. Check the data line input pins 3, 7, 4, 6, 5, 9, 2, and 8 are changing states. If all input signals are correct and the outputs are not changing states, suspect A14U295.
The read/write decoders, A14U495 and U395 in the Trigger-Processor Interface are defective.	Verify that the address inputs to decoder pins 1, 2, and 3 are working properly. Check the CRD(L), CWR(L), and IBS0(L) lines are working properly. Check that pin 6 on both A14U395 and U495 are pulled high. If the inputs appear correct but the outputs do not, suspect the decoders U395 and U495.
The latches A14U170, U175, and U180, in the Trigger-Processor Interface, are not working properly.	Verify that the data inputs on each of the latches are changing states. If the inputs appear correct but the outputs are not, suspect the control latches.
The RESET(H) signal is not being generated. The RESET(H) signal is generated by A14U675 and U580 in the Trigger Control circuitry.	If the inputs to A14U675 and U580 appear correct and the RESET(H) line is not high, suspect the expander gates A14U675 and U580.
Defective sequence pointer circuitry A14U630, U633, U635, and U640.	Check pin 2 of these I.C.s for a value of 05_{hex}. If the value is not correct, check pin 14 for the same value. If necessary, check the remaining inputs. If the inputs appear correct, suspect A14U630, U633, U635, and U640.
The processor readback circuitry may be defective.	Check pins 7, 4, 10, and 13 of A14U140 for the value of 05_{hex}. If the inputs appear correct, check the output pins 6, 5, 11, and 9 for a value of 05_{hex}. If the inputs are correct but the outputs are not, suspect A14U140. Check pins 12, 9, 10, and 13 of A14U115 in the Trigger-Processor Interface for a value of 05_{hex}. Verify that the clock signal on pin 6 is working properly. Check the output pins 15, 3, 14, and 2 of A14U115 and verify the value of 05_{hex}. If inputs appear to be correct but outputs are not, suspect A14U115. Check pins 2, 10, 14, and 6 of A14U110 in the Trigger-Processor Interface for a value of 05_{hex}. Check that the output enable on pin 4 is going low. If the inputs appear correct but the outputs are not, suspect A14U110.

6112 Error Index

Explanation: The sequence pointer does not appear to be set at $0A_{hex}$.

Probable Cause	Action
The data bus buffer, A14U295 in the Trigger-Processor Interface, is not working correctly.	Verify that the chip enable signal on A14U295-19 is pulsing low while the test is looping. Check that the data direction signal on pin 1 is working properly. Check the data line input pins 3, 7, 4, 6, 5, 9, 2, and 8 are changing states. If all input signals are correct and the outputs are not changing states, suspect A14U295.
The read/write decoders, A14U495 and U395 in the Trigger-Processor Interface are defective.	Verify that the address inputs to decoder pins 1, 2, and 3 are working properly. Check the CRD(L), CWR(L), and IBS0(L) lines are working properly. Check that pin 6 on both A14U395 and U495 are pulled high. If the inputs appear correct but the outputs do not, suspect the decoders U395 and U495.
The latches A14U170, U175, and U180, in the Trigger-Processor Interface, are not working properly.	Verify that the data inputs on each of the latches are changing states. If the inputs appear correct but the outputs are not, suspect the control latches.
The RESET(H) signal is not being generated. The RESET(H) signal is generated by A14U675 and U580 in the Trigger Control circuitry.	If the inputs to A14U675 and U580 appear correct and the RESET(H) line is not high, suspect the expander gates A14U675 and U580.
Defective sequence pointer circuitry A14U630, U633, U635, and U640.	Check pin 2 of these I.C.s for a value of $0A_{hex}$. If the value is not correct, check pin 14 for the same value. If necessary, check the remaining inputs. If the inputs appear correct, suspect A14U630, U633, U635, and U640.
The processor readback circuitry may be defective.	Check pins 7, 4, 10, and 13 of A14U140 for the value of $0A_{hex}$. If the inputs appear correct, check the output pins 6, 5, 11, and 9 for a value of $0A_{hex}$. If the inputs are correct but the outputs are not, suspect A14U140. Check pins 12, 9, 10, and 13 of A14U115 in the Trigger-Processor Interface for a value of $0A_{hex}$. Verify that the clock signal on pin 6 is working properly. Check the output pins 15, 3, 14, and 2 of A14U115 and verify the value of $0A_{hex}$. If inputs appear to be correct but outputs are not, suspect A14U115. Check pins 2, 10, 14, and 6 of A14U110 in the Trigger-Processor Interface for a value of $0A_{hex}$. Check that the output enable on pin 4 is going low. If the inputs appear correct but the outputs are not, suspect A14U110.

6113 Error Index

Explanation: The sequence pointer did not step on event false. The Actual field on the 1240 screen indicates the current sequence pointer value.

Probable Cause	Action
If pin 2 of the sequence pointer I.C.s, A14U630, U633, U635, and U640, are $0F_{hex}$, the clock from the Asynchronous Timebase may be missing.	Loop on this routine and verify a negative-going clock on pin 11 of the sequence pointer I.C.s. If it is not present, trace the clock path back through the Sequential Timing and Timebase 1 circuits. If there is no clock on the T1 bus, refer to the tests for the ATB (Asynchronous Timebase) area 8.
If the sequence clocks appear at the sequence pointer, there may be defective true/false sequence and control RAMs.	Examine the next sequence value (for event found false) at the output of A14U235. The next sequence step should be the current sequence value pointer minus one. Verify that A14U330 pin 2 is low and that pins 1, 15, and 14 are high. Verify that SWR(L) is low at pin 9 of A14U535B (in the Sequential Sampler). If not, then the sequential word recognizers on the acquisition boards are not initialized true low. Verify that SWR POL(H) on pin 7 of A14U535B is high after the failure occurs in the test. If not, then suspect control RAM A14U333 in the Sequential Filter.

6114 Error Index

Explanation: The sequence pointer did not step on event true. The Actual field on the 1240 screen indicates the current sequence pointer value.

Probable Cause	Action
If pin 2 of the sequence pointer I.C.s, A14U630, U633, U635, and U640, are $0F_{hex}$, the clock from the Asynchronous Timebase may be missing.	Verify that A14U530A-4, -6, and -7 are low. If U530A-4 is high and U535B-7 is low, suspect control RAM A14U333. If A14U530-6 is high, the Sequential Filter output is not initialized low; refer to the error description for 631X. If A14U530-7 is high, the Iteration Counter output is not initialized low; refer to the error description for 641X. Verify a negative-going strobe on A14U530A-5.

6115 Error Index (670-7523-10)

Explanation: The sequence pointer did not trigger on event true; (the Actual data equals 2).

Probable Cause	Action
Possible defective RAM location in the sequential control RAM, A14U330.	Verify that A14U330-1 and -14 are low.
A14U433B may be defective.	Verify that A14U433B-15 and -2 are low after the test is done. Verify that S CMD CLK(H) is present on A14U433-9.
The Trigger Control circuitry may be defective.	Verify that A14U570-4 and -7 are high. If either pin is low, suspect the Trigger Control registers A14U170 and U175 in the Trigger-Processor Interface.
	Verify that the PREFILLED 1(L) and PREFILLED 2(L) are active low on A14U470-6 and -7 (in the Trigger Control circuitry). Also, verify that A14U675-12 is high. If it is low, suspect the Trigger Control register A14U170 in the Trigger-Processor Interface.

6115 Error Index (670-7523-09 and below)

Explanation: The sequence pointer did not trigger on event true; (the Actual data equals 2).

6115

Probable Cause	Action
Possible defective RAM location in the sequential control RAM, A14U330.	Verify that A14U330-1 and -14 are low.
A14U433B may be defective.	Verify that A14U433B-15 and -2 are low after the test is done. Verify that S CMD CLK(H) is present on A14U433-9.
The Trigger Control circuitry may be defective.	Verify that A14U570-4 and -7 are high. If either pin is low, suspect the Trigger Control registers A14U170 and U175 in the Trigger-Processor Interface.
	Verify that the PREFILLED 1(L) and PREFILLED 2(L) are active low on A14U680C-10 and -11 (in the Trigger Control circuitry). Also, verify that A14U675-12 is high. If it is low, suspect the Trigger Control register A14U170 in the Trigger-Processor Interface.

TRIGGER BLOCK DIAGRAM
GLOBAL FILTER – AREA 2

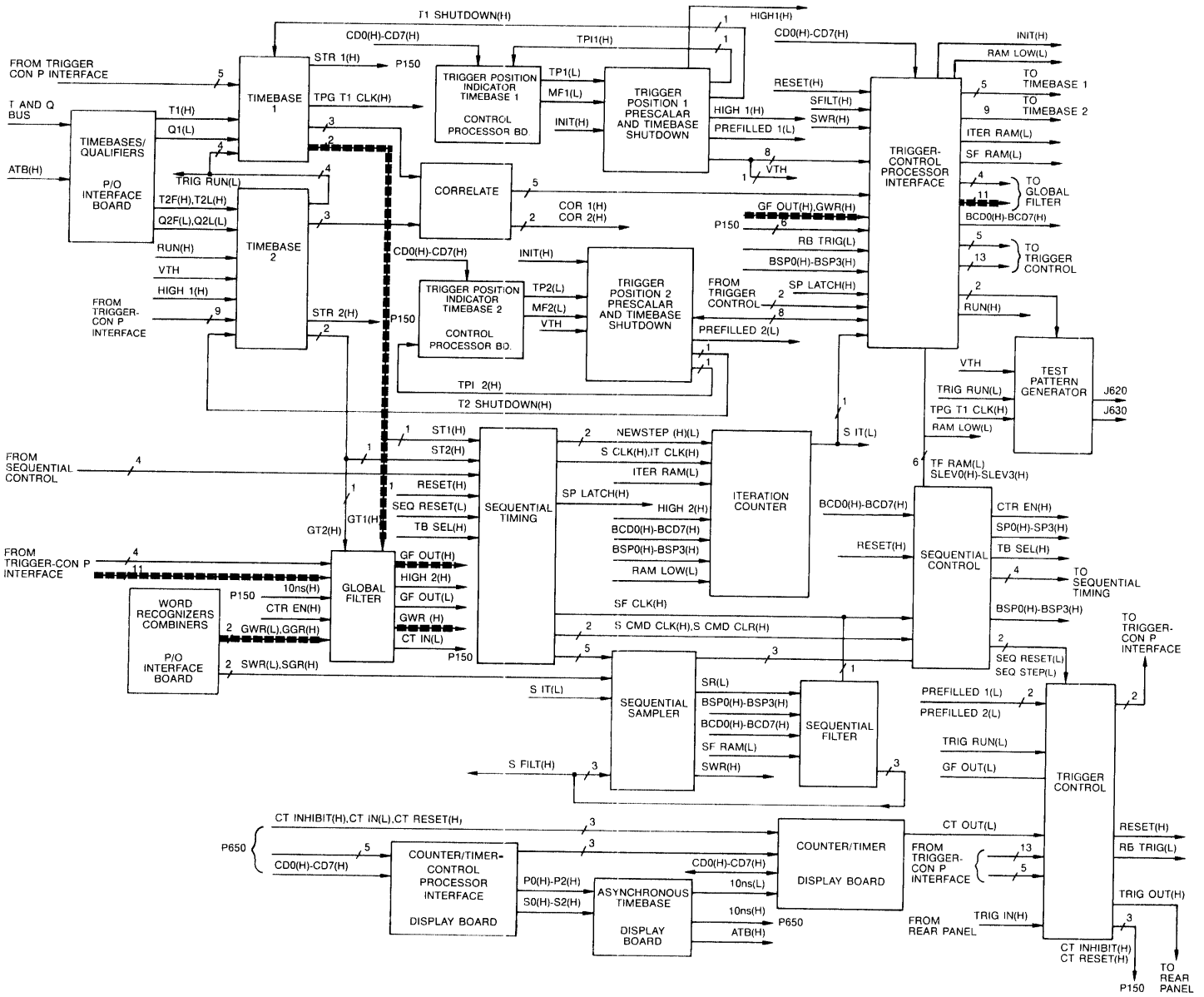

Figure 8-79. Trigger GLOBAL FILTER block diagram.

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TRIGGER BOARD – COMPONENT LOCATION

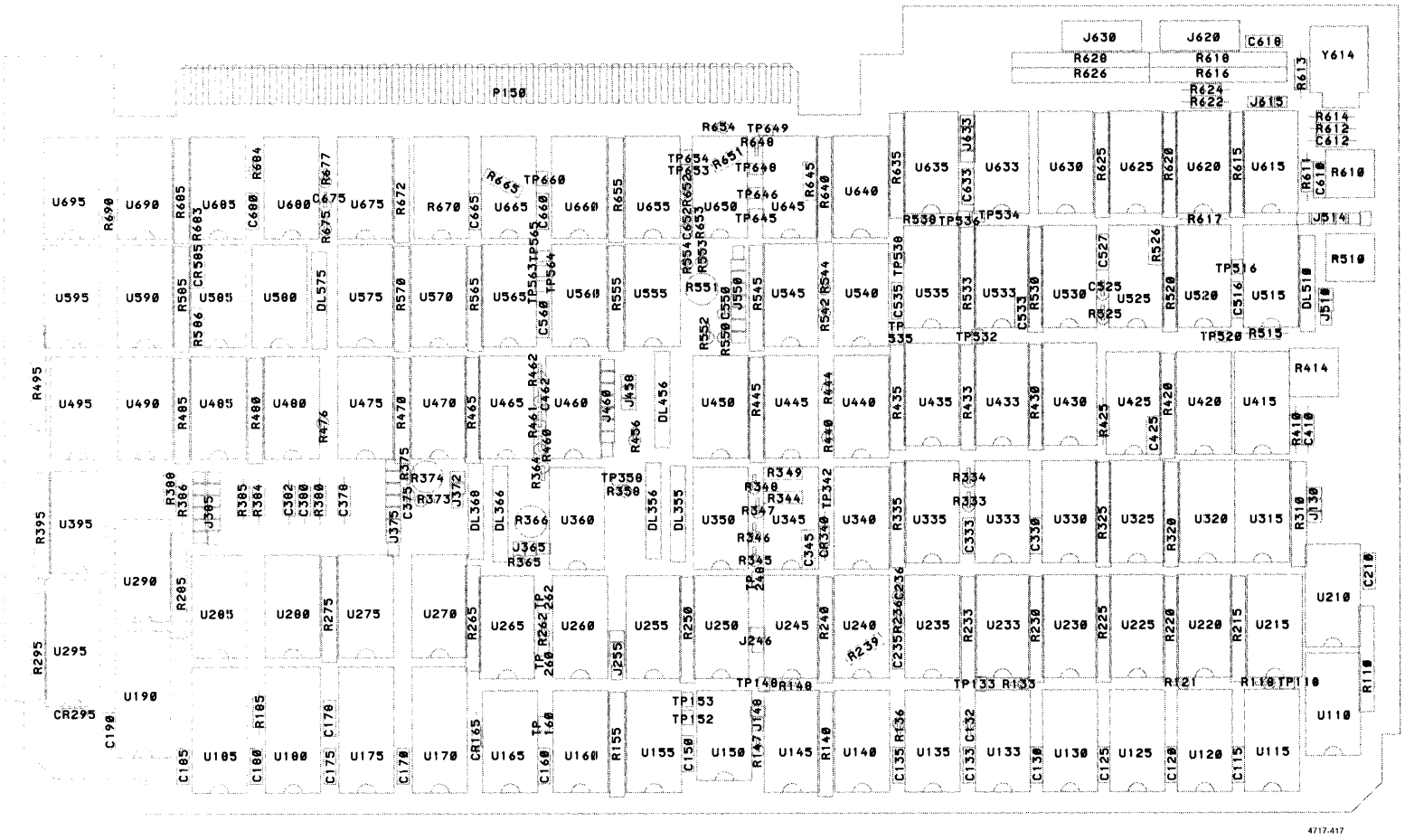

Figure 8-80. Trigger Board component location.

module: TRIGGER
area: GLOBAL FIL

GLOBAL FILTER AREA – CIRCUIT OVERVIEW

The pattern-shaded signal lines on the timing block diagram indicate circuitry used during diagnostic testing. Only the circuitry that is being exercised for the first time during diagnostic testing is shown. Circuitry exercised by other diagnostic tests are shown in their respective block diagrams.

The global filter consists of four basic sections: Event Polarity, Clock Select, Duration Count, and Edge/Level Control. The global filter, when used, forces a recognized global event to be active for a specified number of clock cycles (up to 16 cycles) before it is recognized as a true global event. A global event consists of word and glitch recognition signals derived from the inputs to 1240D1 and D2 cards. The filter can be used with either T1, T2, or 10 ns timebases, and can run from the event edge or during the event level. If the recognized global event is active for the specified duration, a global-event-valid (found) signal is generated. Otherwise, no output is produced. The global filter output goes to both the counter/timer circuitry and the trigger control circuitry.

GLOBAL FILTER AREA – TEST DESCRIPTION

The global filter test consists of two routines. Routine 1 verifies the global event counter. Routine 2 verifies the global event filter mode (edge and level).

ROUTINE 1 – TEST DESCRIPTION

This routine verifies the global event counter. First the Global Filter is loaded with 02_{hex}. It is incremented to $0F_{hex}$ using the processor-stepped T1 clock. The filter status bit GF OUT(H) from A14U485-15 is then read back via A14U275-6, expecting it to be asserted true.

Next, the filter is loaded with $0A_{hex}$ and incremented seven times. Again the status bit is checked, expecting it to be false. The filter is clocked one more time and the status bit is read, expecting it to be asserted true.

Finally, the filter is loaded with 05_{hex} and then incremented 12 times. The status bit is checked, expecting it to be false. The filter is clocked one more time and the status bit is read, expecting it to be asserted true.

6211 Error Index

Explanation: The Global Filter is not initialized.

Probable Cause	Action
Latch A14U190 in the Trigger-Processor Interface may be defective.	Check A14U190-11 for a clock. Check that U190-15 is high; if not, then suspect A14U190.
The GF OUT(H) flip-flop, A14U485B, was not reset.	Verify that A14U485-13 goes high during the test. If pin 13 is going high and output pin 15 is not going low, suspect A14U485.
The EXOR gate, A14U660A, may be defective.	Verify that A14U660-4 and -5 are high. Check the output pin 2 for a high. If the output is not correct, suspect A14U660.
Latch A14U275 in the Trigger-Processor Interface may be defective.	Check A14U275-4 for a clock. Check that U275-2 is high and pin 6 is low. If the latch is receiving a clock pulse and the inputs are correct, suspect A14U275.

6212 Error Index

Explanation: The Global Filter counter, A14U490, was loaded with 02_{hex} and clocked 14 times. The status bit is checked, expecting it to be low. The counter was clocked once more. The status bit should have been asserted high. If the EXPECT=40 and the ACTUAL=80, the filter output was high after only 14 clocks. If the EXPECT=C0 and ACTUAL=40, the filter output was not high after 15 clocks.

Probable Cause	Action
Latch A14U190 in the Trigger-Processor Interface may be defective.	Verify that the start value 02_{hex} is being latched into U190-9, -19, -12, and -2. If not, suspect the latch A14U190.
The counter, A14U490, may be defective.	Check A14U490-6 for a low chip enable signal during the test. Next, verify the 02_{hex}value is present on the parallel load inputs of U490. Check that U490-5 goes low, and then high during the test. If the inputs appear correct and pin 4 generates a carry out signal after 14 clocks (or there is no carry out after 15 clocks), then suspect A14U490.
There was no clock to the counter, A14U490.	Verify that a clock is present from A14U345-2. If no clock is output and the input pins 4, 9, 7, and 12 appear correct, suspect A14U345.

6213 Error Index

Explanation: The Global Filter counter, A14U490, was loaded with $0A_{hex}$ and clocked seven times. The status bit is checked, expecting it to be low. The counter was clocked once more. The status bit should have been asserted high. If the EXPECT=40 and the ACTUAL=80, the filter output was high after only seven clocks. If the EXPECT=C0 and ACTUAL=40, the filter output was low after eight clocks.

Probable Cause	Action
Latch A14U190 in the Trigger-Processor Interface may be defective.	Verify that the start value $0A_{hex}$ is being latched into U190-9, -19, -12, and -2. If not, suspect the latch A14U190.

6214 Error Index

Explanation: The Global Filter counter, A14U490, was loaded with 05_{hex} and clocked 12 times. The status bit is checked, expecting it to be low. The counter was clocked once more. The status bit should have been asserted high. If the EXPECT=40 and the ACTUAL=80, the filter output was high after only 12 clocks. If the EXPECT=C0 and ACTUAL=40, the filter output was low after 13 clocks.

Probable Cause	Action
Latch A14U190 in the Trigger-Processor Interface may be defective.	Verify that the start value 05_{hex} is being latched into U190-9, -19, -12, and -2. If not, suspect the latch A14U190.

ROUTINE 2 – TEST DESCRIPTION

This routine verifies global event filter mode (edge and level). First the Global Filter is placed in the level (sync) mode. The filter is loaded with $0C_{hex}$ and incremented five times using the processor-stepped T1 clock. The filter status bit GF OUT(H) from A14U485-15 is then read back via A14U275-6, expecting it to be false. The filter is clocked once more and the status bit is expected to be true. Now the filter is clocked five more times and the status bit is checked after each clock, expecting each time for the bit to be false. Finally, the filter is clocked one last time and the status bit is checked, expecting it to be true.

Next, the filter is put in the edge (async) mode. The filter is loaded with $0C_{hex}$ and incremented five times using the processor-stepped T1 clock. The GF OUT(H) filter status bit is then read back, expecting it to be false. The filter is clocked once more and the status bit is expected to be true. Now the filter is clocked 16 more times and the status bit is checked after each clock, expecting each time for the bit to be true.

6221 Error Index

Explanation: The Global Filter was placed in the level mode. The global filter event status bit on GF OUT(H) and global word status bit on GWR(H) were checked. The first should have been true; the second should have been false. If the ACTUAL = 00_{hex} or 80_{hex}, the global word status bit was low when it should have been high. If the ACTUAL = $C0_{hex}$ or 80_{hex}, the global filter event status bit was high when it should have been set low.

Probable Cause	Action
The GWR POL(H), GF DT2(L), and GF 10 ns(L) signals were not set high in the Trigger-Processor Interface latch A14U185.	Check A14U185-16, -15, and -12 to verify that they go high during the test. If not, suspect A14U185.
The expander gate, A14U345, is not generating a clock pulse for the counter A14U490.	Verify that control signals on A14U345-4, -7, and -12 are high; check for a clock on U345-9. If U345-2 has no output, suspect A14U345.

6222 Error Index

Explanation: The Global Filter was clocked once and the global filter event status bit did not go high.

6221
6222

Probable Cause	Action
The GF = 1(H) flip-flop, A14U585B, is not being reset.	Check that A14U585-13 goes high during the test. Check that the output pin 15 goes low. If not, suspect A14U585.
The GF OUT(H) flip-flop A14U485B is not being set.	Check that A14U485-13 is not being held high during the test. Verify that the input pin 10 is high, and that a clock pulse is present on pin 11 while pin 10 is high. If the inputs appear correct but the output pin 15 is not going high, suspect A14U485.

6223 Error Index

Explanation: The Global Filter was clocked five more times while watching the filter status bit GF OUT(H). The global filter event status bit was high when it should have been low.

Probable Cause	Action
The Global Filter was not in the level mode.	Verify a low on A14U190-5 while the routine is stopped on the error. Suspect A14U595, U485, and U695.

6224 Error Index

Explanation: The Global Filter was clocked once more; the global filter event status bit should have gone high but it did not.

Probable Cause	Action
The Global Filter was not in the level mode.	Verify a low on A14U190-5 while the routine is stopped on the error. Verify a high on A14U595-6. Suspect A14U595, U485, U695, and U585.

6225 Error Index

Explanation: The Global Filter was placed in the edge (async) mode and the global word status bit and global filter event status bits were not correct. If the ACTUAL=00_{hex} or 80_{hex}, the status bits were high when the should have been low. If the ACTUAL=$C0_{hex}$ or 80_{hex}, the status bits were low when the should have been high.

Probable Cause	Action
The Global Filter counter may be defective.	Verify correct operation of A14U490; it should have been loaded with C_{hex} then given five clocks with the terminal count remaining low.

6226 Error Index

Explanation: The global event filter was clocked once more and the global filter event status bit was checked. The bit should have been high, but was found to be low.

Probable Cause	Action
The Global Filter did not go into edge mode.	Verify a high on A14U190-5; suspect A14U190 and U595.

6227 Error Index

Explanation: The global event filter was clocked 16 times while watching the global filter event status bit. The bit went high, but should have remained low.

Probable Cause	Action
The Global Filter went into the level mode.	Verify a high on A15U595-11; suspect A14U595, U585, U485, and U695.

TRIGGER BLOCK DIAGRAM
SEQ FILTER – AREA 3

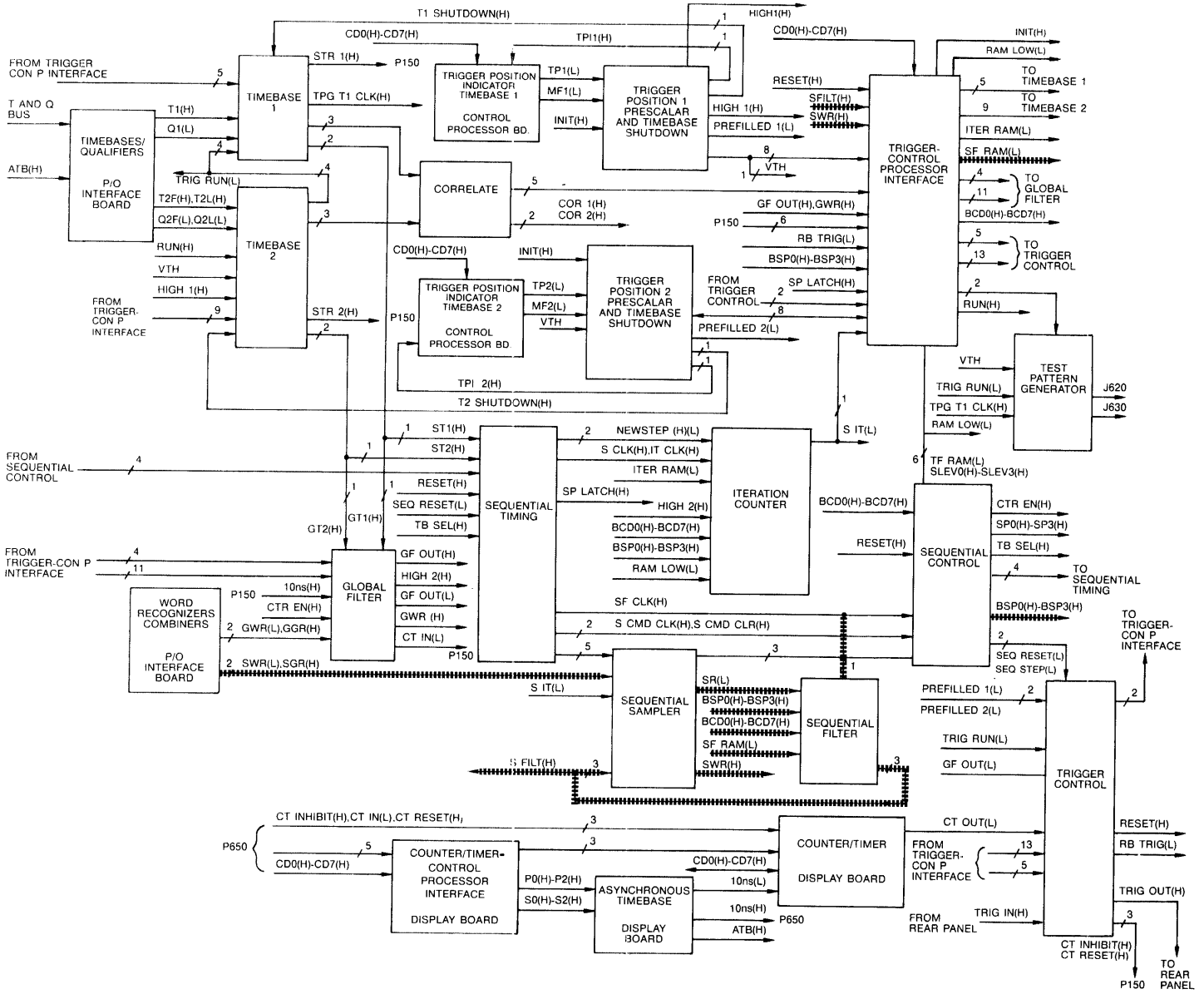

Figure 8-81. Trigger SEQ FILTER block diagram.

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TRIGGER BOARD – COMPONENT LOCATION

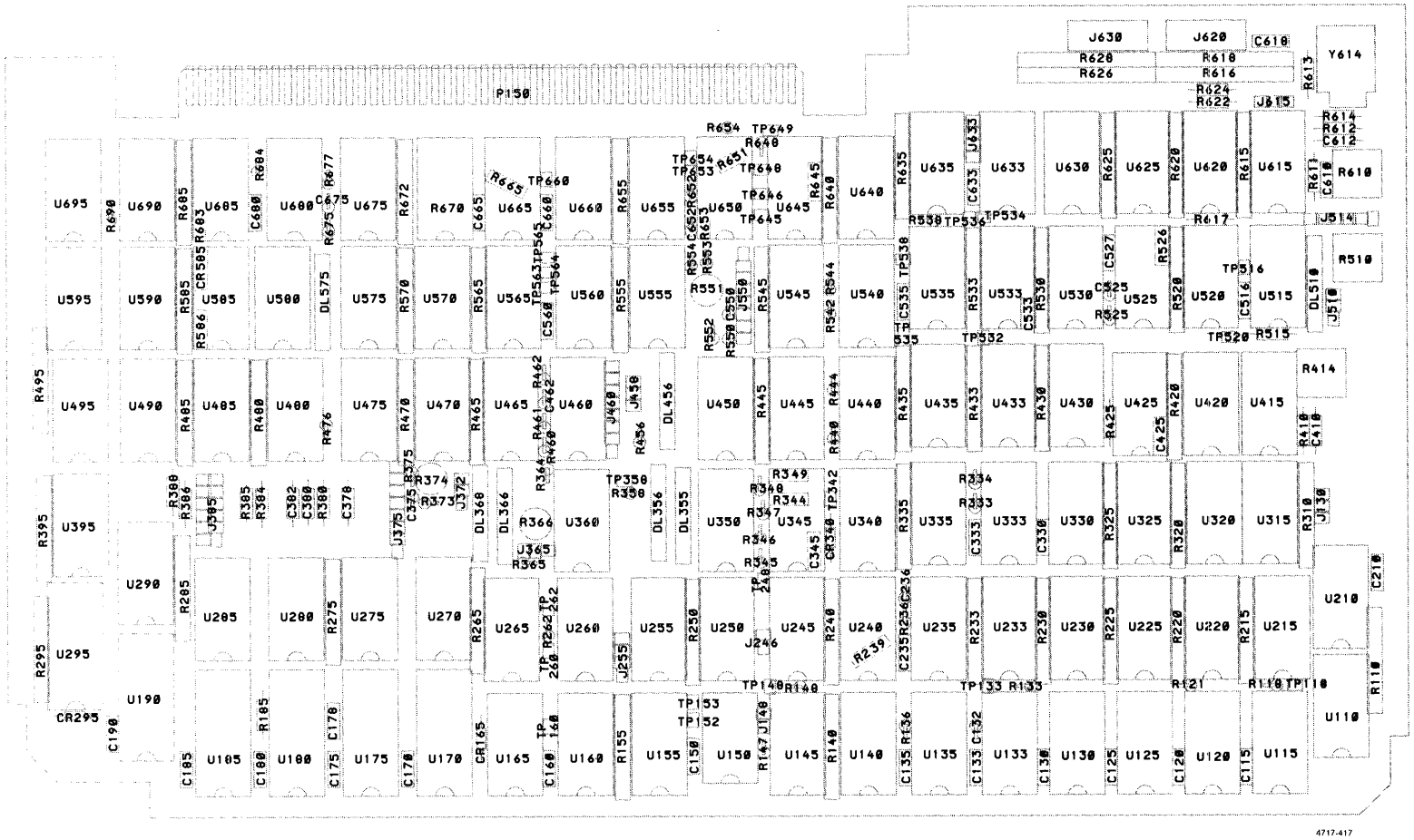

Figure 8-82. Trigger Board component location.

module: TRIGGER
area: SEQ FILTER

SEQUENTIAL FILTER AREA – CIRCUIT OVERVIEW

The pattern-shaded signal lines on the timing block diagram indicate circuitry used during diagnostic testing. Only the circuitry that is being exercised for the first time during diagnostic testing is shown. Circuitry exercised by other diagnostic tests are shown in their respective block diagrams.

The Sequential Filter, when used, requires the sequential recognizer to be true for a specified number of clock cycles (up to 16 cycles) before it is recognized as a true sequential event. When the event duration is one count less than the user-selected value, the filter outputs an enable signal, S FILT(L).

Outputs from the Sequential Filter S FILT(L), the Sequential Iteration Counter S IT(L), and the Sequence Recognizer, SR(L), are combined with timing strobes by A14U530 and A14U533 in the Sequential Sampler.

In the Sequential Sampler, EXOR gates A14U535B and C select the ON/ON NOT polarity of the word and glitch recognizers and combine the word and glitch together. This combined sequence recognizer signal is sampled by A14U525B to eliminate glitches produced when the acquisition cards are sampling data asynchronously. This sampled Sequence Recognizer signal, SR(L), is sent to the Sequential Filter and Iteration Counter.

SEQ FILTER AREA – TEST DESCRIPTION

The sequential filter test consists of two routines. Routine 1 verifies the ability of the Sequential Filter counter to count. Routine 2 verifies the ability of the Sequential Filter counter to count in the edge and level modes.

ROUTINE 1 – TEST DESCRIPTION

This routine verifies the ability of the Sequential Filter counter to count. First, the Sequential Filter is initialized and the S FILT(H) and SWR(H) signals are read back and checked for correct initialization. The Sequential Filter counter, A14U435, is loaded with 00_{hex}. The counter is then incremented to $0F_{hex}$ using the processor-stepped T1 clock. The Sequential Filter status bit S FILT(H) is read back from A14U285-5, expecting it to be asserted true when the filter count is at $0F_{hex}$. Next the filter is loaded with $0A_{hex}$ and incremented to $0F_{hex}$. The S FILT(H) status bit is read back, expecting it to be asserted true (high) when the filter count is $0F_{hex}$. The test is repeated once more using a start count of 05_{hex}.

6311 Error Index

Explanation: The Sequential Filter is not initialized.

Probable Cause	Action
The write decoder, A14U495 in the Trigger-Processor Interface, may be defective.	Check that A14U495-10 goes low during the test. If not, suspect A14U495.
The Sequential Filter control signals were not latched correctly in RAM A14U333.	Check that A14U333-15 is low. Also, check that pins -2, -1, and -14 are high. If the outputs are not correct, suspect A14U333.
EXOR gate A14U535B in the Sequential Sampler may be defective.	Check that A15U535-9 and -7 are low. Check that the output at U535-11 is high. If it is not high when the two inputs are low, suspect A14U535.
Latch A14U275 in the Trigger-Processor Interface may be defective.	Check that A14U285-6 and A14U275-10 are both high. Check that the read back enable on A14U285-4 goes low during the test. If the inputs appear correct but the outputs do not, suspect A14U275 or U285.

6312 Error Index

Explanation: The Sequential Filter counter, A14U435, was loaded with 00_{hex} and clocked 16 times. The status bit is checked, expecting it to be low. The counter was clocked once more. The status bit should have been asserted high. If the EXPECT=00 and the ACTUAL=04, the filter output was high after only 16 clocks. If the EXPECT=04 and ACTUAL=00, the filter output was not high after 17 clocks.

Probable Cause	Action
The Sequential Filter control signals were not latched correctly in control RAM A14U333.	Verify that A14U333-15 and -2 are low; verify that U333-1 and -14 are high. If the outputs are not correct, suspect A14U333.
The Sequential Filter stack RAM, A14U335, may be defective.	Verify that A14U335-13 goes low during the test. Check that U335-2, -1, -15, and -14 are low. If the write enable on pin 13 is correct and the outputs of U335 are not, suspect A14U335.
The Sequential Filter counter, A14U435, may be defective.	Verify that the parallel input enable on A14U435-5 goes low during the test. Check that U435-7, -9, -10, and -11 are low. Check for clock pulses on U435-13. If the input signals appear to be correct and there is an output on U435-4 before clock number 17 appears at pin 13 (or if there is no output on pin 4 after clock number 17), then suspect A14U435.
The S FILT(H) flip-flop A14U440B may be defective.	Verify that A14U440-10 goes low during the test. Check for a clock pulse on U440-9 while pin 10 is low. Check that the reset at U440-13 is low. If the inputs are correct and output U440-14 does not go high, then suspect A14U440.

6313 Error Index

Explanation: The Sequential Filter counter, A14U435, was loaded with $0A_{hex}$ and clocked 6 times. The S FILT(H) status bit is checked, expecting it to be low. The counter was clocked once more. The status bit should have been asserted high. If the EXPECT=20 and the ACTUAL=28, the filter output was high after only 6 clocks. If the EXPECT=28 and ACTUAL=20, the filter output was not high after 7 clocks.

Probable Cause	Action
The Sequential Filter stack RAM, A14U335, may be defective.	Verify that A14U335-13 goes low during the test. Check U335-2, -1, -15, and -14 for the value $0A_{hex}$. If the pattern is not found, suspect A14U335.
The Sequential Filter counter, A14U435, may be defective.	Check U435-7, -9, -10, and -11 for the $0A_{hex}$ pattern. If the pattern is present, then suspect A14U435.

6314 Error Index

Explanation: The Sequential Filter counter, A14U435, was loaded with 05_{hex} and clocked 11 times. The S FILT(H) status bit is checked, expecting it to be low. The counter was clocked once more. The status bit should have been asserted high. If the EXPECT=00 and the ACTUAL=04, the filter output was high after only 11 clocks. If the EXPECT=04 and ACTUAL=00, the filter output was not high after 12 clocks.

Probable Cause	Action
The Sequential Filter stack RAM, A14U335, may be defective.	Check U335-2, -1, -15, and -14 for the value 05_{hex}. If the pattern is not found, suspect A14U335.
The Sequential Filter counter, A14U435, may be defective.	Check U435-7, -9, -10, and -11 for the 05_{hex} pattern. If the pattern is present, then suspect A14U435.

ROUTINE 2 – TEST DESCRIPTION

This routine verifies the ability of the Sequential Filter counter to count in the edge and level modes. First, the Sequential Filter is placed in the level (sync) mode. The filter is set up for the special case of 1 event by asserting the SF-EN signal (A14U333-2) high, and then low. The S FILT(H) status bit is read back, expecting it to be false. The filter is clocked one time using the processor-stepped T1 clock and the Sequential Filter status bit should be set true. The filter is clocked four times and the S FILT(H) line is checked after each clock; it should remain false. The filter is clocked a fifth time and the S FILT(H) line should be set true.

Next, the filter is placed in the edge (async) mode. The sequential filter counter, A14U435, is loaded with $0C_{hex}$ and three clock pulses are generated. The S FILT(H) status bit is read back, expecting it to be set false. The filter is clocked once more and the status bit should be asserted true. Finally, the Sequential Filter is clocked 16 times and the status bit is checked after each clock; the status bit should remain high.

6321 Error Index

Explanation: The Sequential Filter was placed in the level (sync) mode. The SWR(H) line from the Sequential Sampler is checked, expecting it to be true (high); the S FILT(H) line is checked, expecting it to be false (low). If ACTUAL=00_{hex} or 08_{hex}, the SWR sequential word status bit was low when it should have been high.

Probable Cause	Action
Acquisition cards may be holding the SWR(H) readback line low.	Check A14U535B-9, SWR(L), and U535B-15, SGR(H), to verify both are low. If both are not low, remove accompanying acquisition cards and run the test again. If both are still not low, suspect A14U535.
	Check A14U535B-10 for a high. If high, check U535-11 for a low. If low, the problem is A14U275 in the Trigger-Processor Interface. If A14U535B-11 is high, suspect A14U535.
	Check A14U535B-10 for a high; if not high, suspect A14U535.
Sequential RAM A14U333 may be defective.	Check A14U535-7 for a low; if low, suspect A14U333.

Now, the Sequential Filter is placed in the level (sync) mode. The SWR(H) line from the Sequential Sampler is checked, expecting it to be true (high); the S FILT(H) line is checked, expecting it to be false (low). If ACTUAL=28_{hex} or 08_{hex}, the SWR sequential word status bit was high when it should have been low.

Probable Cause	Action
A14U440B or A14U285 may be defective.	Check A14U440B-14 for a low. If low, suspect A14U285 in the Trigger-Processor Interface. While looping on this test, check A14U440B-10 for a 10 ns pulse; refer to schematic number 24.

6322 Error Index

Explanation: The Sequential Filter was clocked once and the S FILT(H) line should have gone true, but it did not.

Probable Cause	Action
Acquisition cards may be pulling the SGR(H) readback line high.	Check A14U535B-15, SGR(H), for a low. If high, remove accompanying acquisition cards and run the test again. If still not low, recheck U535-15 for a low. If pin 15 is still not low, suspect A14U535.
Sequential RAM A14U333 may be defective.	Check A14U333-1 for a high; there are also some low-going pulses. If pin 1 is stuck low; suspect A14U333 or U535.
A14U440B or A14U285 may be defective.	Check A14U440B-14 for a high. If high, suspect A14U285 in the Trigger-Processor Interface.

6323 Error Index

Explanation: The Sequential Filter was clocked four more times and the S FILT(H) line was checked to be low after each clock.

Probable Cause	Action
A14U333 may be defective, or stack values may be incorrect.	Using a logic analyzer, check A14U440 for the four incoming clocks while monitoring the outputs.

6324 Error Index

Explanation: The Sequential Filter was clocked one more time and the S FILT(H) line should have gone true, but it did not.

Probable Cause	Action
Sequential RAM A14U333 may be defective.	Check A14U333-14 for a low with 2 ms high pulses. If high pulses are present, suspect A14U445. If pulses are not present, suspect A14U333.

6325 Error Index

Explanation: The Sequential Filter was placed in the edge (async) mode. The SWR(H) line from the Sequential Sampler is checked, expecting it to be true (high); the S FILT(H) line is checked, expecting it to be false (low).

Probable Cause	Action
RAM A14U333 may be defective.	Ensure the filter is in the edge mode by verifying that A14U333-14 is low. If not low, suspect A14U333.

6326 Error Index

Explanation: The Sequential Filter was clocked 16 times and the S FILT(H) line went high during one of the clocks.

Probable Cause	Action
A14U440 or A14U445 may be defective.	Check A14U440-4 for a low with 2 ms positive-going pulses. If pulses are present, suspect A14U440; if not, suspect A14U445.

6327 Error Index

Explanation: A false event condition was generated, indicated by the S FILT(H) line being high when it should have been low.

Probable Cause	Action
The Sequential Filter was not programmed correctly.	Suspect RAM A14U333.

6328 Error Index

Explanation: The Sequential Filter was clocked once and the S FILT(H) line was found to be low when it should have been high.

Probable Cause	Action
A14U340 may be defective.	Check A14U340-14 for a high; the signal is not a steady high. If pin 14 has no high present, check U340-12 for a low. If no low is present, suspect A14U525B in the Sequential Sampler.

TRIGGER BLOCK DIAGRAM
I COUNTER – AREA 4

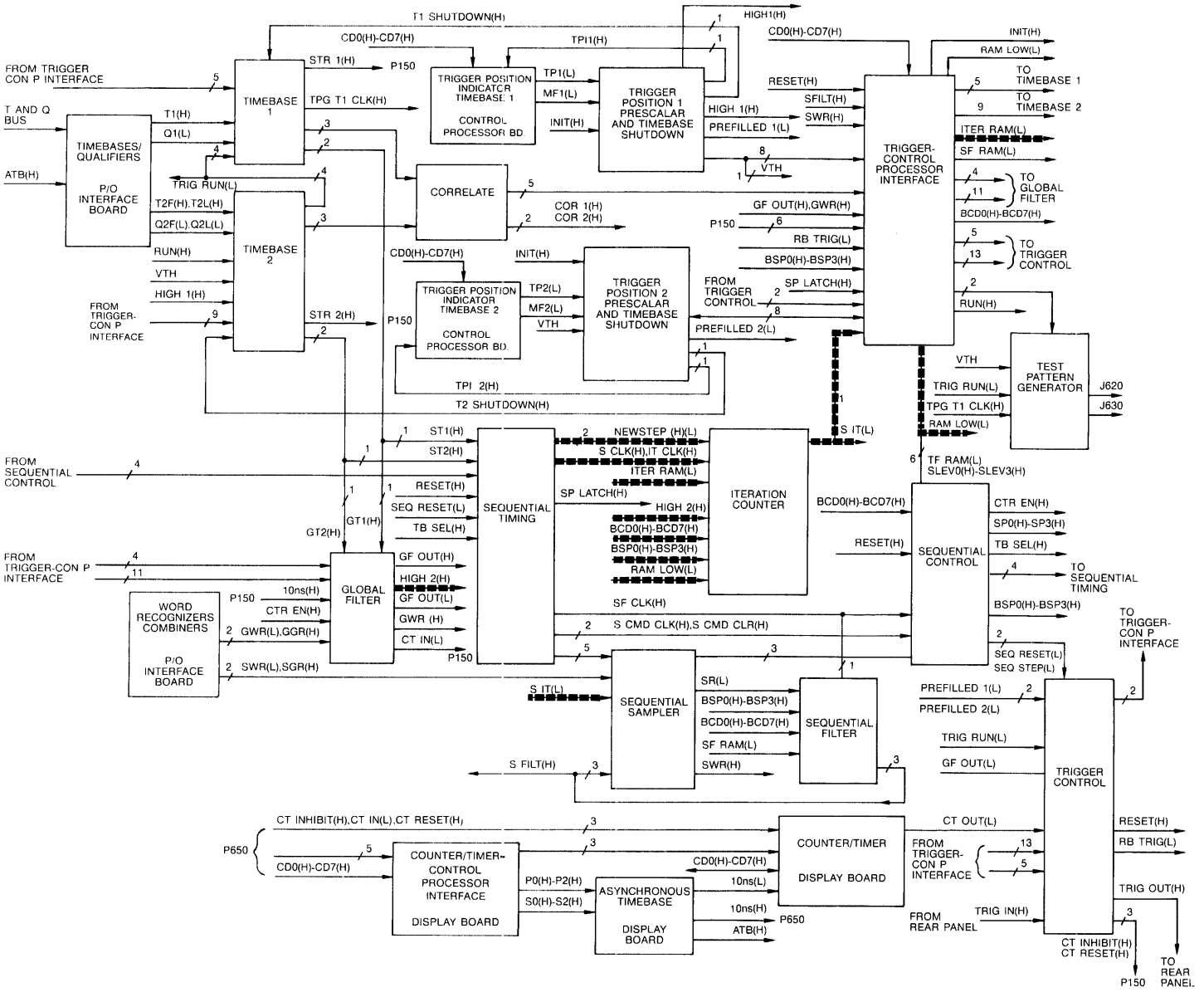

Figure 8-83. Trigger I COUNTER block diagram.

4342-122

TRIGGER BOARD – COMPONENT LOCATION

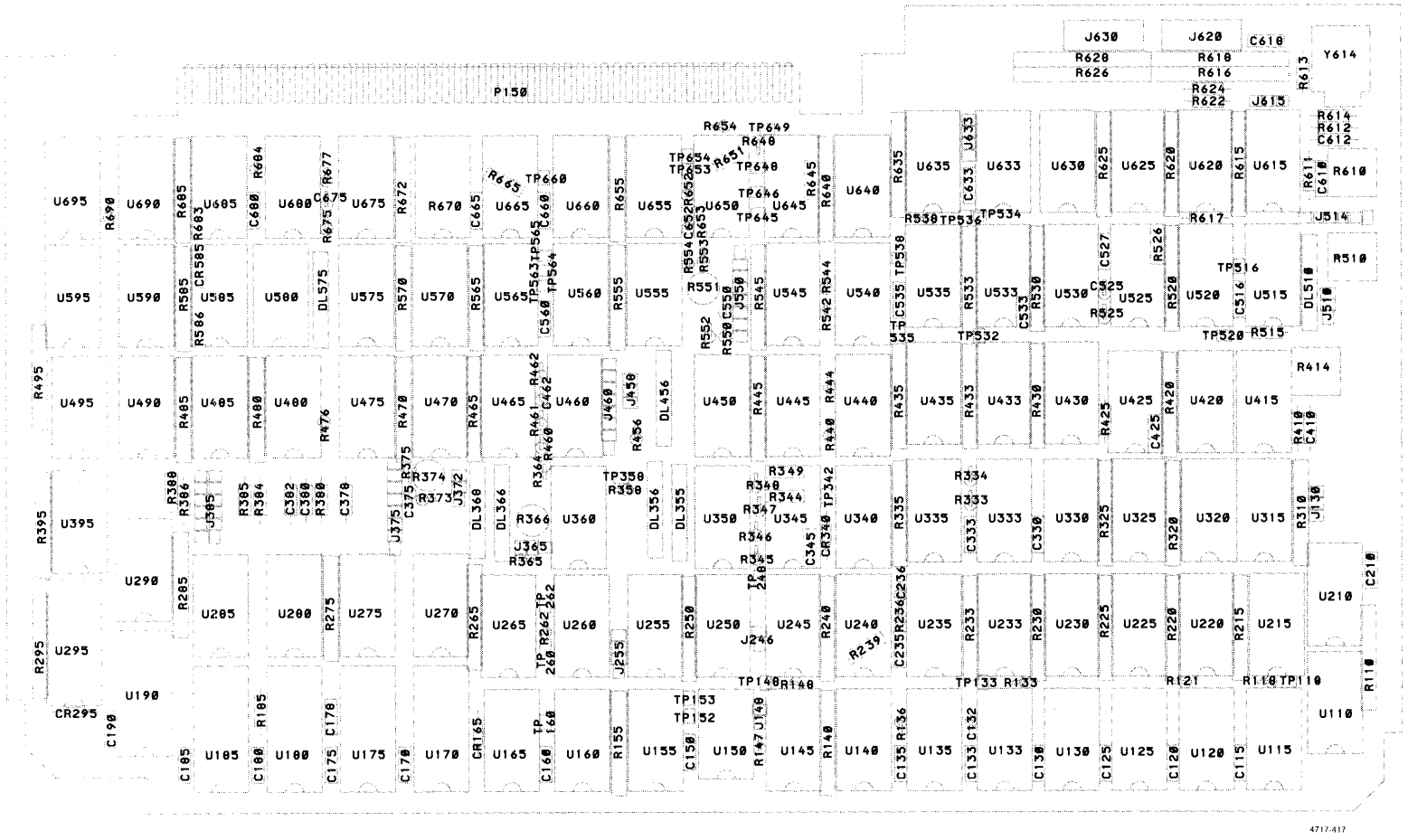

Figure 8-84. Trigger Board component location.

module: TRIGGER
area: I COUNTER

ITERATION COUNTER AREA – CIRCUIT OVERVIEW

The pattern-shaded signal lines on the timing block diagram indicate circuitry used during diagnostic testing. Only the circuitry that is being exercised for the first time during diagnostic testing is shown. Circuitry exercised by other diagnostic tests are shown in their respective block diagrams.

The iteration counter, when used, requires the filtered sequential recognizer to occur a user-specified number of times. When the count reaches a value one less than the user selected value, the counter outputs an enable signal, S IT(L).

For an iteration count of one, the iteration counter is not used. For an iteration count of two, A14U215B requires that an event be found by the filter one time before the S IT(L) signal is asserted. On the second true filter output, the command is executed.

For an iteration count of 3 to 9999, the counters A14U220 -U233 require that an event be found by the filter a number of times before asserting S IT(L).

ITERATION COUNTER AREA – TEST DESCRIPTION

The Iteration Counter test consists of two routines. Routine 1 verifies data independence for the four counters A14U220-U233. Routine 2 verifies the ability to load the Iteration Counter RAM at each sequence level.

ROUTINE 1 – TEST DESCRIPTION

This routine verifies data independence for the four counters A14U220, U225, U230, and U233. Each counter is loaded with $0A_{hex}$ or 05_{hex} and incremented to a known value with a processor-stepped T1 clock. The iteration counter bit, S IT(L), is then read to check for correct status.

6411 Error Index

Explanation: The Iteration Counter was loaded with $7FFA_{hex}$. Then the processor clocked the counter five times. When read, the iteration status line, S IT(L), should have remained high but it was low.

Probable Cause	Action
The Iteration Counter RAM may be defective.	Check the input pin 3 on the lower 8-bits of RAM A14U130 and U125 and verify that the RAM LOW(L) signal changes state during the test. Verify that pin 13 of the four counters A14U220-U233 goes low during the test. Check the data input pins 5, 4, 11, and 12 on RAMs A14U120-U133 for the $7FFA_{hex}$ pattern. Also check output pins 2, 1, 15, and 14 for the correct pattern being output. If the inputs are correct and the outputs are not, suspect the RAM with the incorrect output.
The Iteration Counter A14U220, U225, U230, or U233 may be defective.	Verify that the $7FFA_{hex}$ pattern is being loaded into the counter input pins 7, 9, 10, and 11. Check input pin 5 on each of the counters and verify that it goes low during the test. Check pin 13 of each counter to verify the IT CLK(H) iteration clock signal is present. Check pin 4, the carry out of each counter stage. The carry out from the lower counter stages are logically ORed with the carry out of the next higher stage. Verify that the carry out is being propagated through the stages.
The Iteration Counter terminal count OR gate, A14U325, may be defective.	Verify that each of the inputs to A14U325 do not go high at the same time during the test. The output of the OR gate at pin 14 should remain high. If not, suspect A14U325.
The S IT(L) flip-flop, A14U215B, is not being reset.	Check pin 13 of A14U215B and verify that it goes high during the test. Check that pin 14 of U215B is high.

6412 Error Index

Explanation: The Iteration Counter was clocked one time and the iteration status line, S IT(L), failed to go low.

Probable Cause	Action
The Iteration Counter A14U220, U225, U230, or U233 may be defective.	Verify that the $7FFA_{hex}$ pattern is being loaded into the counter input pins 7, 9, 10, and 11. Check input pin 5 on each of the counters and verify that it goes low during the test. Check pin 13 of each counter to verify the IT CLK(H) iteration clock signal is present. Check pin 4, the carry out of each counter stage. The carry out from the lower counter stages are logically ORed with the carry out of the next higher stage. Verify that the carry out is being propagated through the stages.
The Iteration Counter terminal count OR gate, A14U325, may be defective.	Verify that each of the inputs to A14U325 do not go high at the same time during the test. The output of the OR gate at pin 14 should remain high. If not, suspect A14U325.
The S IT(L) flip-flop, A14U215B, is not being reset.	Check pin 13 of A14U215B and verify that it is low. Verify that the input pin 10 goes high during the test, and that a clock pulse is present on pin 11 while pin 10 is high. Verify that the output U215B-14 is low. If not low, suspect A14U215.

6413 Error Index

Explanation: The Iteration Counter was loaded with $7FF5_{hex}$ and the counter was given 10 clocks. The iteration status line, S IT(L), should have remained high (error index 6413). The counter was clocked one more time and the status bit should have gone low (error index 6414).

Correct operation of the Iteration Counter was tested by error indexes 6411 and 6412. This portion of the routine is checking the data bit independence of the data path through the Iteration Counter RAM and into the Iteration Counter. The pattern used in tests 6411 and 6412 was 05_{hex}; the pattern used in 6413 and 6414 is the same. If a failure occurs in these tests, the probable cause is one of the RAMs or the parallel load portion of the counters.

Probable Cause	Action
The Iteration Counter RAM may be defective.	Suspect A14U130.
The Iteration Counter may be defective.	Suspect A14U230.

6414 Error Index

Explanation: The Iteration Counter was clocked one time and the iteration status line, S IT(L), should have gone low.

Probable Cause	Action
The Iteration Counter RAM may be defective.	Suspect A14U130.
The Iteration Counter may be defective.	Suspect A14U230.

6415 Error Index

Explanation: This error index is reserved for future use.

6416 Error Index

Explanation: The Iteration Counter was loaded with $7FAF_{hex}$ and the counter was clocked 80 times. The iteration status line, S IT(L), should have remained high but was found low.

Probable Cause	Action
The Iteration Counter RAM may be defective.	Suspect A14U125.
The Iteration Counter may be defective.	Suspect A14U225.

6417 Error Index

Explanation: The Iteration Counter was clocked one time and the iteration status line, S IT(L), should have gone low.

Probable Cause	Action
The Iteration Counter RAM may be defective.	Suspect A14U125.
The Iteration Counter may be defective.	Suspect A14U225.

6418 Error Index

Explanation: The Iteration Counter was loaded with $7F5F_{hex}$ and the counter was clocked 160 times. The iteration status line, S IT(L), should have remained high but was found low.

Probable Cause	Action
The Iteration Counter RAM may be defective.	Suspect A14U125.
The Iteration Counter may be defective.	Suspect A14U225.

6419 Error Index

Explanation: The Iteration Counter was clocked one time and the iteration status line, S IT(L), should have gone low.

Probable Cause	Action
The Iteration Counter RAM may be defective.	Suspect A14U125.
The Iteration Counter may be defective.	Suspect A14U225.

641A Error Index

Explanation: The Iteration Counter was loaded with $7AFF_{hex}$ and the counter was clocked 1280 times. The iteration status line, S IT(L), should have remained high but was found low.

Probable Cause	Action
The Iteration Counter RAM may be defective.	Suspect A14U120.
The Iteration Counter may be defective.	Suspect A14U220.

641B Error Index

Explanation: The Iteration Counter was clocked one time and the iteration status line, S IT(L), should have gone low.

Probable Cause	Action
The Iteration Counter RAM may be defective.	Suspect A14U120.
The Iteration Counter may be defective.	Suspect A14U220.

641C Error Index

Explanation: The Iteration Counter was loaded with $75FF_{hex}$ and the counter was clocked 2560 times. The iteration status line, S IT(L), should have remained high but was found low.

Probable Cause	Action
The Iteration Counter RAM may be defective.	Suspect A14U120.
The Iteration Counter may be defective.	Suspect A14U220.

641D Error Index

Explanation: The Iteration Counter was clocked one time and the iteration status line, S IT(L), should have gone low.

Probable Cause	Action
The Iteration Counter RAM may be defective.	Suspect A14U120.
The Iteration Counter may be defective.	Suspect A14U220.

641E Error Index

Explanation: The Iteration Counter was loaded with $2FFF_{hex}$ and the counter was clocked 20,480 times. The iteration status line, S IT(L), should have remained high but was found low.

Probable Cause	Action
The Iteration Counter RAM may be defective.	Suspect A14U133.
The Iteration Counter may be defective.	Suspect A14U233.

641F Error Index

Explanation: The Iteration Counter was clocked one time and the iteration status line, S IT(L), should have gone low.

Probable Cause	Action
The Iteration Counter RAM may be defective.	Suspect A14U133.
The Iteration Counter may be defective.	Suspect A14U233.

ROUTINE 2 – TEST DESCRIPTION

This routine verifies the ability to load the Iteration Counter RAM at each sequence level using the values 5555_{hex} and $2AAA_{hex}$. First, every sequence level in the Iteration Counter is loaded with 5555_{hex}. Starting at the first sequence level (level value = F), the Iteration Counter is loaded with the contents of the Iteration Counter RAM. The counter is then incremented to its terminal count minus one. The iteration status bit, S IT(L), should be high. The counter is clocked once more and the status bit should go low (true). This verification sequence is repeated for each of the remaining sequence levels.

Next, the value $2AAA_{hex}$ is loaded into every sequence level of the Iteration Counter RAM, then the verification sequence described earlier is repeated.

641F
6421

6421 Error Index

Explanation: The Iteration Counter was loaded with 5555_{hex} from the Iteration Counter RAM. Then the processor clocked the counter 10,922 times. When read, the iteration status line, S IT(L), should have remained high but it was low.

Probable Cause	Action
The Iteration Counter RAM, A14U130, U125, U120, and U133 may be defective.	Check the test results. These results contain the information needed to isolate the problem. The ADDR information indicates the sequence level at which the test failed. The EXPECTED information indicates if the test sequenced to the next level or not. Refer to the following example.

ADDRESS	EXPECTED	ACTUAL
0002	10	00

This example indicates that on the second sequence level, the S IT(L) status bit was expected high but it was not (after 10,922 clocks).

ADDRESS	EXPECTED	ACTUAL
0002	00	10

This example indicates that on the second sequence level, the S IT(L) status bit was expected low but it was not (after 10,923 clocks).

6422 Error Index

Explanation: The Iteration Counter was loaded with $2AAA_{hex}$ from the Iteration Counter RAM. Then the processor clocked the counter 21,845 times.

Probable Cause	Action
The Iteration Counter RAM, A14U130, U125, U120, and U133 may be defective.	Check the test results. These results contain the information needed to isolate the problem. The ADDR information indicates the sequence level at which the test failed. The EXPECTED information indicates if the test sequenced to the next level or not. Refer to the following example.

ADDRESS	EXPECTED	ACTUAL
0012	10	00

This example indicates that on sequence level number 12, the S IT(L) status bit was expected high but it was not (after 21,845 clocks).

ADDRESS	EXPECTED	ACTUAL
0002	00	10

This example indicates that on the second sequence level, the S IT(L) status bit was expected low but it was not (after 21,846 clocks).

TRIGGER BLOCK DIAGRAM
TPI 1 – AREA 5

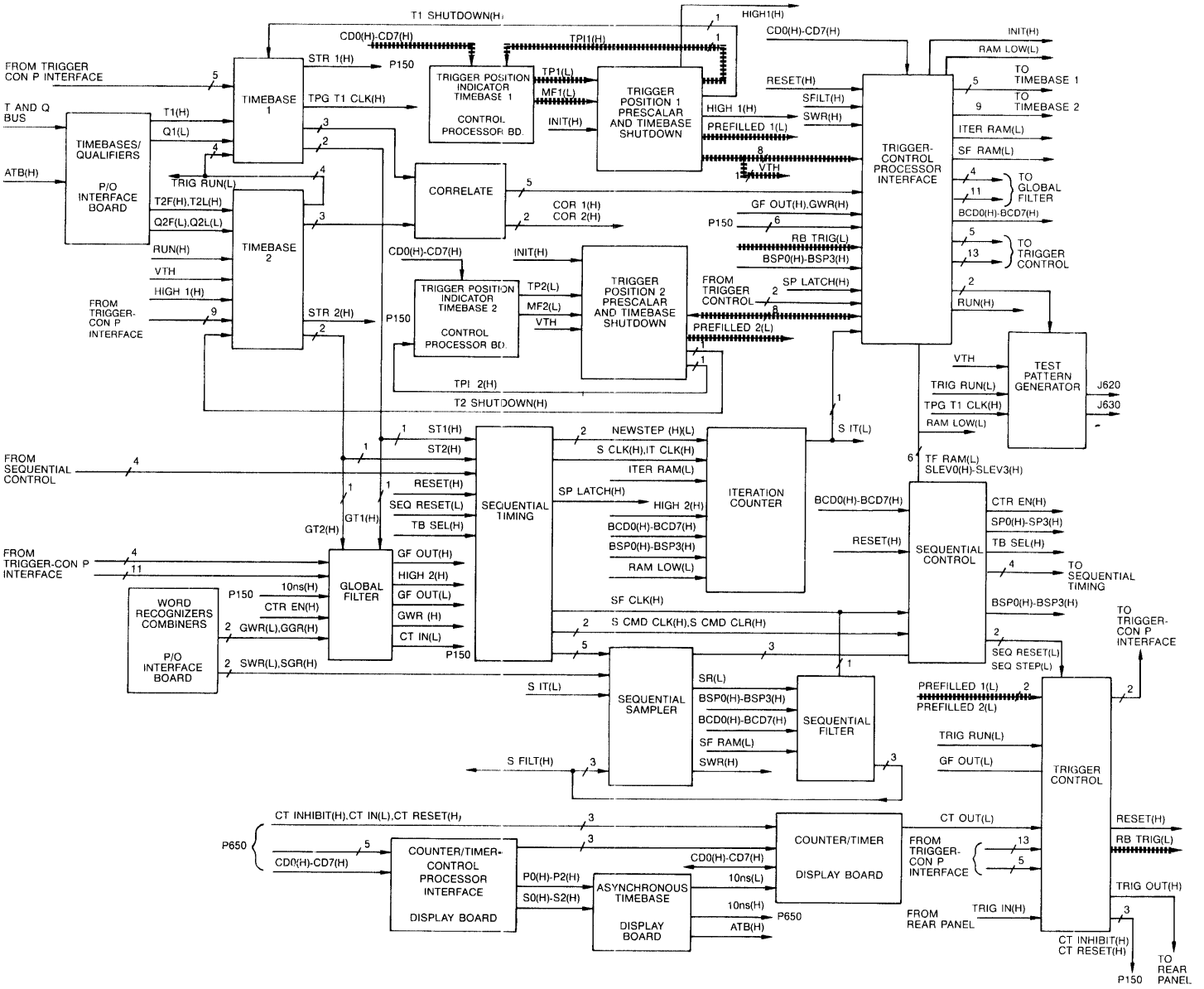

Figure 8-85. Trigger TPI 1 block diagram.

4342-123

TRIGGER BOARD – COMPONENT LOCATION

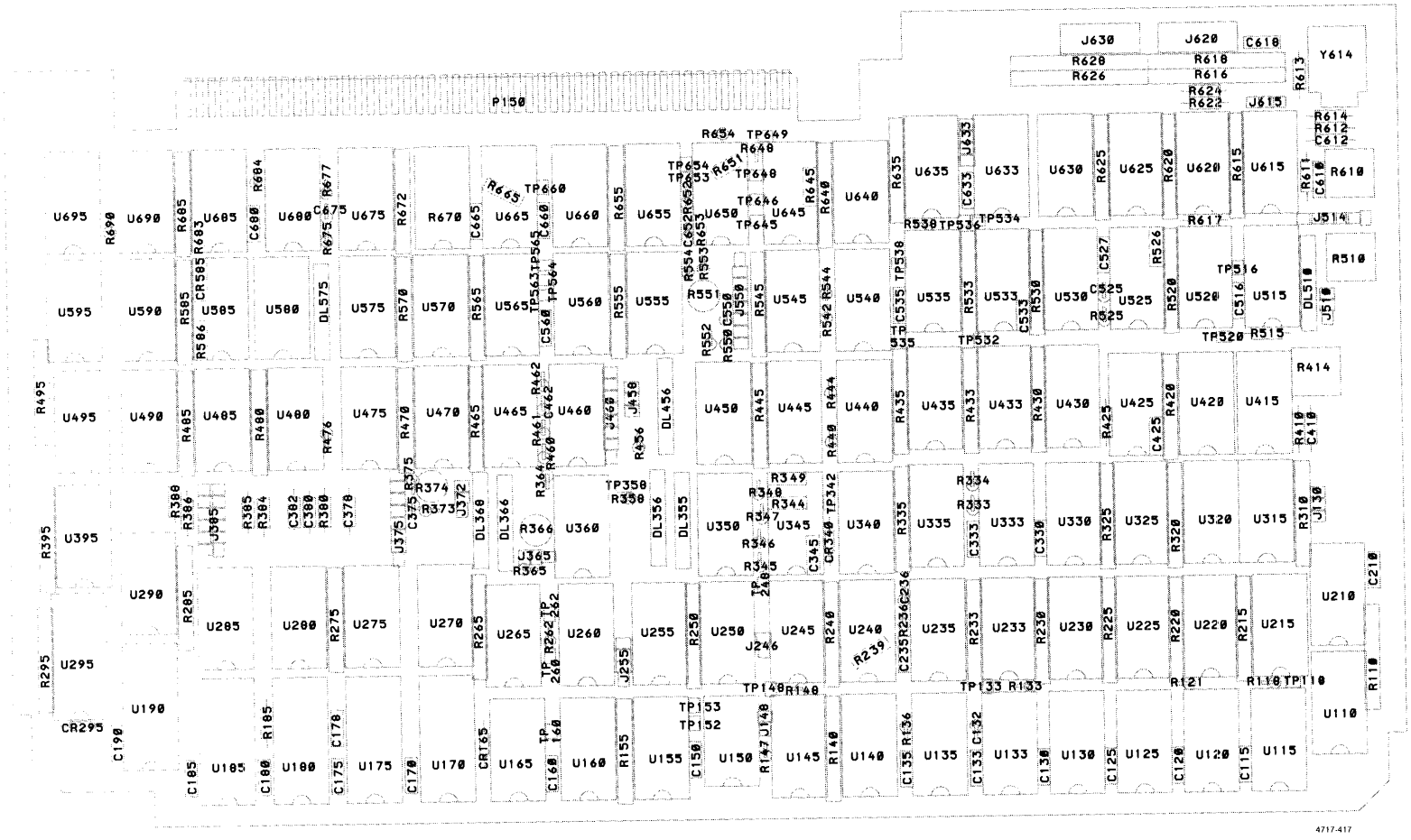

Figure 8-86. Trigger Board component location.

module: TRIGGER
area: TPI 1

TPI 1 AREA – CIRCUIT OVERVIEW

The pattern-shaded signal lines on the timing block diagram indicate circuitry used during diagnostic testing. Only the circuitry that is being exercised for the first time during diagnostic testing is shown. Circuitry exercised by other diagnostic tests are shown in their respective block diagrams.

The trigger position indicators, in conjunction with the trigger position prescalers, count the number of stored data samples. Since the 1240 can acquire data using two independent timebases (T1 and T2), a trigger position indicator exists for each. Data stored before the trigger point is called prefilled data, data stored subsequent to the trigger point is called postfilled data. The user can specify the amount of postfill data and when the specified amount has been stored, the trigger position circuitry shuts down the acquisition system. If the After Memory Full mode is selected, the trigger position circuitry also inhibits the Trigger Control circuits until the prefill section of the memory is filled.

Once prefill is complete, the Trigger Control circuit is allowed to detect a trigger. Now, A14U260B (and U260A for TPI 2) in the Trigger Position 1 and 2 Prescalers and Timebase Shutdowns circuit latches, setting the preload on A14U165 (and U160 for TPI 2). The timebase then waits for a trigger. The system requires approximately 35 ns to decide if a trigger has occurred. The Timebase T-clocks are delayed by approximately 38 ns, then they clock A14U565A and B. U565A and B sample the TRIG(L) signal from the Trigger Control block.

When a trigger is detected, A14U565B and A allow A14U165 and U160 (respectively) to begin counting the postfill. A14U165 (or U160) outputs the lower four bits of the 12-bit counter. The upper 8-bits of the counter reside on the Control Processor Board. Comparators A14U150A and B convert the ECL-level signals to TTL-levels to clock the upper 8-bit counters.

When both the Prescaler on the Trigger Board and the counters on the Control Processor Board reach their final count, then A14U265C (and U265B) goes high. On the next clock, the output of A14U255B (and U255A) goes low. On successive clocks, the flip-flop chain propagates the signal. The low-order counters A14U165 (and U160) begin their count from a non-zero value to compensate for this flip-flop chain. Eventually A14U645A (or U145B) shuts down the timebase via the timebase qualifier lines.

TPI 1 AREA – TEST DESCRIPTION

The Trigger Position Indicator 1 (TPI 1) test verifys operation of the trigger position circuits. First, the test verifys the ability to increment the TPI 1 prescaler counter, A14U165. The counter is reset, and then incremented 16 times. The output of the counter is read back through A14U290 in the Trigger-Processor Interface each time it is incremented. The count received is compared to the expected count.

Now, the prescaler counter, A14U165, is reset and the count is read back to verify it is zero. The upper eight-bit posiiton counter, A09U261 and A09U267, is loaded with the value 55_{hex} and read back via A09U160 to verify that the counter loads correctly.

Next, the prescaler counter is clocked 21 times and read back via A14U290 to verify that it contains 05_{hex} (the prescaler preload value). The clock input to the prescaler counter should have been disabled when the counter's terminal count output was asserted. The prescaler is clocked once again and the output is read back to verify that no change occurred.

The Trigger Position Indicator (TPI) is now incremented to the first trigger position by giving it 2737 processor-stepped clocks. Trigger status is checked via A14U285-11; expecting RB TRIG(L) to be true.

Finally, the upper eight-bit position counter, A09U261 and A09U267, is loaded with AA_{hex}. The output of the counter is read via A09U160 and verified to be AA_{hex}. This portion of the test verifies bit independence for the inputs and outputs of the upper eight-bit position counter. The Trigger Position Indicator (TPI) is incremented to the first trigger position by giving it 1377 processor-stepped clocks. Trigger status is checked via A14U285-11; expecting RB TRIG(L) to be true.

6511 Error Index

Explanation: The Trigger Position Indicator 1 (TPI 1) prescaler counter, A14U165, did not increment correctly.

Probable Cause	Action
The TPI 1 prescaler counter, A14U165, may be defective.	Verify that A14U165-12 goes high during the test. Pin 5, the parallel enable, should remain high while pin 13 is clocked 16 times. If pins 3, 2, 15, and 14 are not high after the counter has been clocked 16 times, suspect A14U165.
The address decoder, A14U395, for the read back buffer, A14U290, (both in the Trigger-Processor Interface) may be defective.	Verify that A14U395-15 goes low during the test. If not, suspect decoder A14U395.
The readback buffer, A14U290, may be defective.	Verify that the output of the TPI 1 prescaler counter is present on input pins 2, 10, 14, and 6 of the readback buffer A14U290. Also, verify that A14U395-15 is present on input pin 4 of A14U290. If the inputs are correct, suspect A14U290.

6512 Error Index

Explanation: The Trigger Position Indicator 1 (TPI 1) prescaler counter, A14U165, was reset and read back expecting it to be zero, but it was not.

Probable Cause	Action
Latch A14U170 in the Trigger-Processor Interface may be defective.	Verify that A14U170-9 is high during the test. If not, suspect A14U170.
The TPI 1 prescaler counter, A14U165, may be defective.	Verify that A14U165-12 goes high during the test. Verify that pins 3, 2, 15, and 14 go low when pin 12 goes high. If they do not, suspect A14U165.

6513 Error Index

Explanation: The Trigger Position Indicator 1 (TPI 1) upper eight-bit counter, A09U261 and A09U267, was loaded with 55_{hex}, but could not be read back correctly.

Probable Cause	Action
The TPI 1 address decoder, A09U262, may be defective.	Verify that A09U262-12 and -13 go low during the test. If they do not, suspect A09U262.
The TPI 1 disable signal, TPI DIS(H), is defective.	Verify that A09U220-19 goes low during the test. If not, suspect A09U220.
The TPI 1 upper eight-bit counter, A09U261 and A09U267, may be defective.	Verify that pin 11 of both counters go low while the pattern 55_{hex} is present on input pins 15, 1, 10, and 9. Verify that the chip enable input pins 4 are low. If the inputs to the counter are correct, suspect A09U261 and A09U267.
The TPI 1 read back latch, A09U160, may be defective.	Verify the 55_{hex} pattern is present on the input pins to A0U160. Also, verify that the enable on pins 1 and 19 are low while the 55_{hex} pattern is present on the inputs. If all input and control signals appear correct, suspect A09U160.

6514 Error Index

Explanation: The Trigger Position Indicator 1 (TPI 1) upper eight-bit counter, A09U261 and A09U267, was clocked 21 times. The counter output was read back expecting 05_{hex}, but it was not.

Probable Cause	Action
The TPI 1 prescaler counter, A14U165, may be defective.	Verify that pins 7 and 10 of the prescaler counter are pulled up to 5 volts through diode A14CR165. Verify that the terminal carry from pin 4 goes low during the 21 clock pulses, and that the parallel enable pin 5 goes low. If all input signals appear correct but the counter output is not 05_{hex}, suspect A14U165.
The TPI 1 prefilled flip-flop, A14U260B, may be defective.	Verify that A14U260-12 and -13 are low. Verify that pin 10 goes high during the test, and that the flip-flop is set when a clock pulse appears on pin 11 while pin 10 is held high. If not set, suspect A14U260.

6515 Error Index

Explanation: The T1 clock was not disabled and the prescaler continued to count.

Probable Cause	Action
The TPI 1 prescaler counter, A14U165, may be defective.	Verify that pin of the prescaler counter goes low during the test. Verify that the counter output pattern is 05_{hex}. If the output changes, suspect A14U165.

6516 Error Index

Explanation: The trigger status bit on RB TRIG(L) was read back high when it was expected low (after 2737 clocks). The prefilled flip-flop may not have been set.

Probable Cause	Action
The readback path may be defective.	While stopped on the error, check A14U290-10 for a low; if low, then suspect U290.
NAND gate A09U236 may be defective.	Verify highs on A09U236-4 and -5; if highs are present, suspect U236. If highs are not present, suspect A09U261 and U267.
Prefilled flip-flop not set.	Check A14U260B-14 for a low; if a low is not present, suspect U260.

6517 Error Index

Explanation: The Trigger Position Indicator 1 (TPI 1) upper eight-bit counter, A09U261 and A09U267, was loaded with AA_{hex}. The counter output was read back expecting AA_{hex}, but it was not.

Probable Cause	Action
The TPI 1 upper eight-bit counter, A09U261 and A09U267, may be defective.	Verify that pin 11 of both counters go low while the pattern AA_{hex} is present on input pins 15, 1, 10, and 9. If the inputs to the counter are correct, suspect A09U261 and A09U267.

6518 Error Index

Explanation: The trigger status bit on RB TRIG(L) was read back high when it was expected low (after 1377 clocks).

Probable Cause	Action
The TPI 1 upper eight-bit counter, A09U261 and A09U267, may be defective.	Verify that pin 12 of both counters are high while stopped on the error. Use a logic analyzer to ensure correct operation.

TRIGGER BLOCK DIAGRAM
TPI 2 – AREA 6

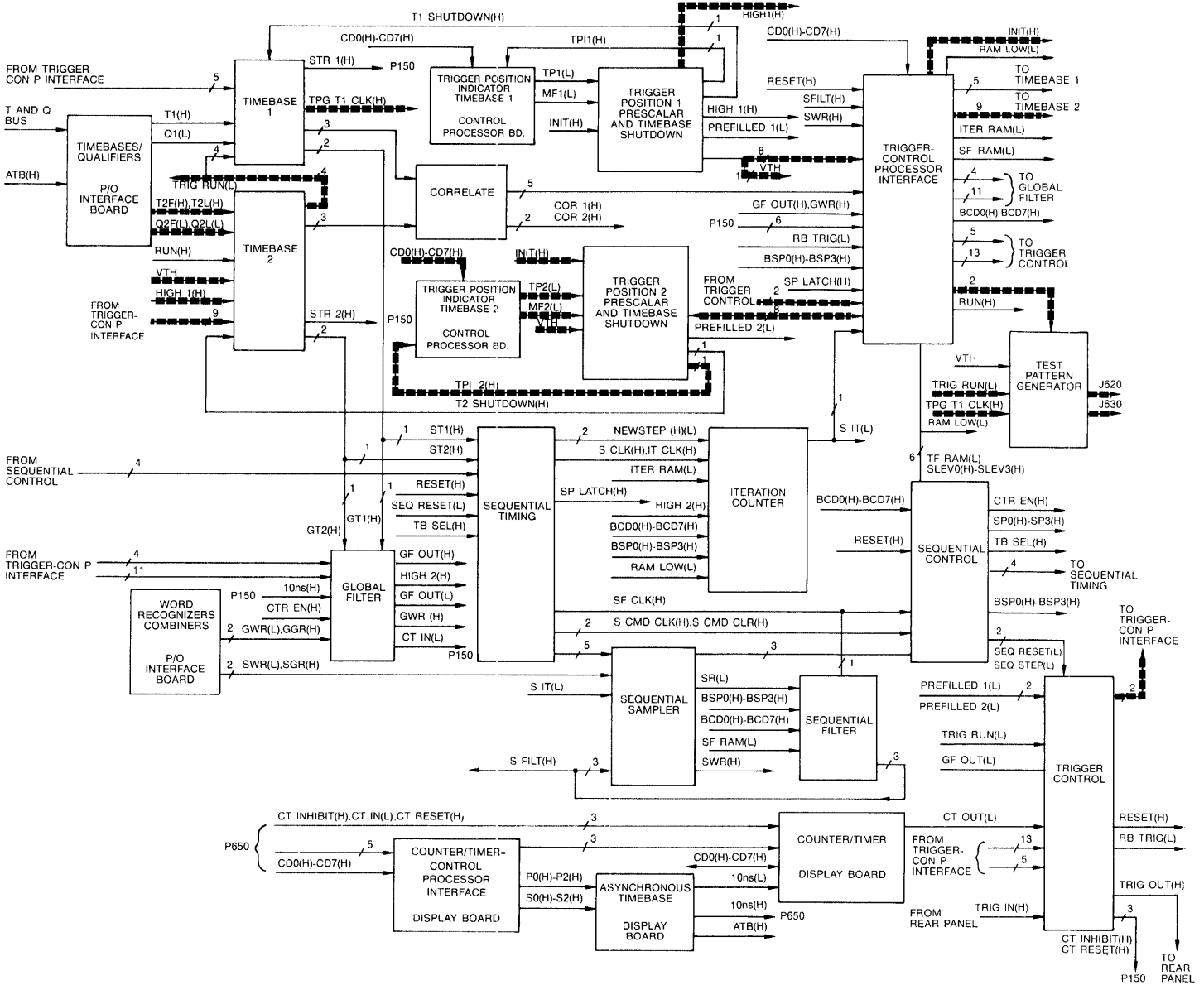

Figure 8-87. Trigger TPI 2 block diagram.

4342-124

TRIGGER BOARD – COMPONENT LOCATION

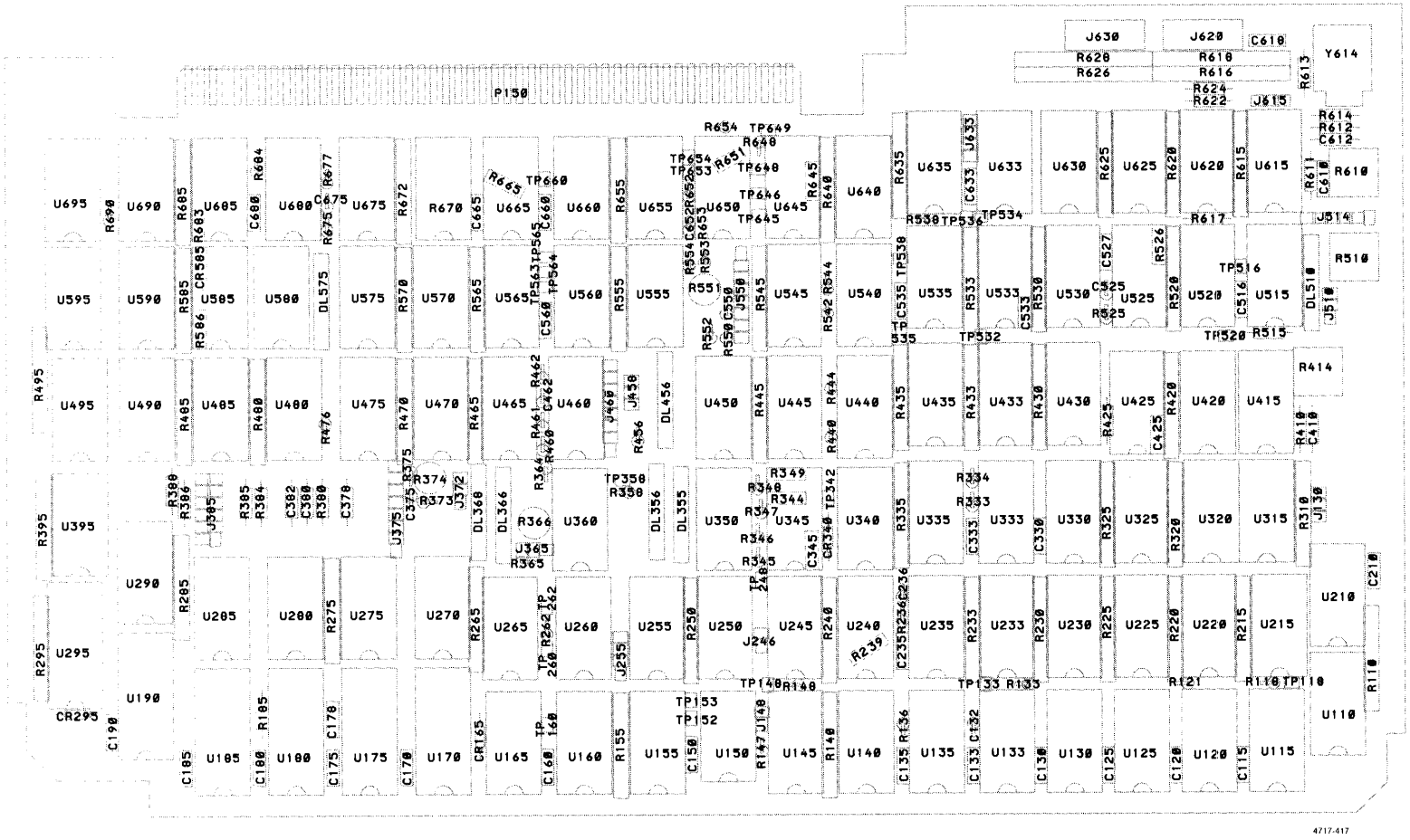

Figure 8-88. Trigger Board component location.

module: TRIGGER
area: TPI 2

TPI 2 AREA – CIRCUIT OVERVIEW

The pattern-shaded signal lines on the timing block diagram indicate circuitry used during diagnostic testing. Only the circuitry that is being exercised for the first time during diagnostic testing is shown. Circuitry exercised by other diagnostic tests are shown in their respective block diagrams.

The trigger position indicators, in conjunction with the trigger position prescalers, count the number of stored data samples. Since the 1240 can acquire data using two independent timebases (T1 and T2), a trigger position indicator exists for each. Data stored before the trigger point is called prefilled data, data stored subsequent to the trigger point is called postfilled data. The user can specify the amount of postfill data and when the specified amount has been stored, the trigger position circuitry shuts down the acquisition system. If the After Memory Full mode is selected, the trigger position circuitry also inhibits the Trigger Control circuits until the prefill section of the memory is filled.

Once prefill is complete, the Trigger Control circuit is allowed to detect a trigger. Now, A14U260A (and U260B for TPI 1) in the Trigger Position 1 and 2 Prescalers and Timebase Shutdowns circuit latches, setting the preload on A14U160 (and U165 for TPI 1). The timebase then waits for a trigger. The system requires approximately 35 ns to decide if a trigger has occurred. The Timebase T-clocks are delayed by approximately 38 ns, then they clock A14U565A and B. U565A and B sample the TRIG(L) signal from the Trigger Control block.

When a trigger is detected, A14U565A and B allow A14U160 and U165 (respectively) to begin counting the postfill. A14U165 (or U160 for TPI 1) outputs the lower four bits of the 12-bit counter. The upper 8-bits of the counter reside on the Control Processor Board. Comparators A14U150A and B convert the ECL-level signals to TTL-levels to clock the upper 8-bit counters.

When both the Prescaler on the Trigger Board and the counters on the Control Processor Board reach their final count, then A14U265B (and U265C for TPI 1) goes high. On the next clock, the output of A14U255A (and U255B for TPI 1) goes low. On successive clocks, the flip-flop chain propagates the signal. The low-order counters A14U160 (and U165) begin their count from a non-zero value to compensate for this flip-flop chain. Eventually A14U145B (or U645A) shuts down the timebase via the timebase qualifier lines.

TPI 2 AREA – TEST DESCRIPTION

This test is run only if a 9- or 18-Channel Acquisition Board is installed in slot 0 next to the Trigger Board. The test also requires that an acquisition probe be installed and connected to the Test Pattern Generator.

The Trigger Position Indicator 2 (TPI 2) test verifys operation of the trigger position circuits. First, the test verifys the ability to increment the TPI 2 prescaler counter, A14U160. The counter is reset, and then incremented 16 times. The output of the counter is read back through A14U280 in the Trigger-Processor Interface each time it is incremented. The count received is compared to the expected count.

Now, the prescaler counter, A14U160, is reset and the count is read back to verify it is zero. The upper eight-bit position counter, A09U264 and A09U164, is loaded with the value 55_{hex} and read back to verify that the counter loads correctly.

The counter is clocked 18 times and read back to verify that it contains 02_{hex} (the prescaler preload value). The clock input to the prescaler counter should have been disabled when the counter's terminal count output was asserted. The prescaler is clocked once again and the output is read back to verify that no change occurred. The prescaler counter is clocked 2736 times and the TPI 2 prefilled bit should be set.

Finally, the upper eight-bit position counter, A09U264 and A09U164, is loaded with AA_{hex}. The counter output is read and verified to be AA_{hex}. This portion of the test verifies bit independence for the inputs and outputs of the upper eight-bit position counter. The TPI 2 counter is now clocked 1376 times and the TPI 2 prefilled bit should be set.

6611 Error Index

Explanation: The acquisition probes are not connected.

Probable Cause	Action
The acquisition probes are defective or not securely plugged in.	Check all probe connections and rerun the test. If failure still exists, replace the probes.

6612 Error Index

Explanation: The Trigger Position Indicator 2 (TPI 2) prescaler counter, A14U160, did not increment correctly.

Probable Cause	Action
The TPI 2 prescaler counter, A14U160, may be defective.	Verify that A14U160-12 goes high during the test. Pin 5, the parallel enable, should remain high while pin 13 is clocked 16 times. If pins 3, 2, 15, and 14 are not high after the counter has been clocked 16 times, suspect A14U160.
The address decoder, A14U395, for the read back buffer, A14U280, (both in the Trigger-Processor Interface) may be defective.	Verify that A14U395-15 goes low during the test. If not, suspect decoder A14U395.
The readback buffer, A14U280, may be defective.	Verify that the output of the TPI 2 prescaler counter is present on input pins 14, 10, 2, and 6 of the readback buffer A14U280. Also, verify that A14U395-15 is present on input pin 4 of A14U280. If the inputs are correct, suspect A14U280.

6613 Error Index

Explanation: The Trigger Position Indicator 2 (TPI 2) prescaler counter, A14U160, was reset and read back expecting it to be zero, but it was not.

Probable Cause	Action
Latch A14U170 in the Trigger-Processor Interface may be defective.	Verify that A14U170-19 is high during the test. If not, suspect A14U170.
The TPI 2 prescaler counter, A14U160, may be defective.	Verify that A14U160-12 goes high during the test. Verify that pins 3, 2, 15, and 14 go low when pin 12 goes high. If they do not, suspect A14U160.

6614 Error Index

Explanation: The Trigger Position Indicator 2 (TPI 2) upper eight-bit counter, A09U264 and A09U164, was loaded with 55_{hex}, but could not be read back correctly.

Probable Cause	Action
The TPI 2 address decoder, A09U262, may be defective.	Verify that A09U262-7 and -11 go low during the test. If they do not, suspect A09U262.
The TPI 2 upper eight-bit counter, A09U264 and A09U164, may be defective.	Verify that pin 11 of both counters go low while the pattern 55_{hex} is present on input pins 15, 1, 10, and 9. Verify that the chip enable input pins 4 are low. If the inputs to the counter are correct, suspect A09U264 and A09U164.
The TPI 2 read back latch, A09U156, may be defective.	Verify the 55_{hex} pattern is present on the input pins to A0U156. Also, verify that the enable on pins 1 and 19 are low while the 55_{hex} pattern is present on the inputs. If all input and control signals appear correct, suspect A09U156.

6615 Error Index

Explanation: The Trigger Position Indicator 2 (TPI 2) upper eight-bit counter, A09U264 and A09U164, was clocked 18 times. The counter output was read back expecting 02_{hex}, but it was not.

Probable Cause	Action
The TPI 2 prescaler counter, A14U160, may be defective.	Verify that pin 9 of the prescaler counter are pulled up to 5 volts through diode A14CR165. Verify that the terminal carry from pin 4 goes low during the 18 clock pulses, and that the parallel enable pin 5 goes low. If all input signals appear correct but the counter output is not 02_{hex}, suspect A14U160.
The TPI 2 prefilled flip-flop, A14U260A, may be defective.	Verify that A14U260-4 and -5 are low. Verify that pin 7 goes high during the test, and that the flip-flop is set when a clock pulse appears on pin 6 while pin 7 is held high. If not set, suspect A14U260.

6616 Error Index

Explanation: The T1 clock was not disabled and the prescaler continued to count.

Probable Cause	Action
The TPI 2 prescaler counter, A14U160, may be defective.	Verify that pin 5 of the prescaler counter goes low during the test. Verify that the counter output pattern is 02_{hex}. If the output changes, suspect A14U160.

6617 Error Index

Explanation: The TPI 2 counter was clocked 2736 times and the prefilled flip-flop, A14U260A, was not set.

Probable Cause	Action
The middle four-bit counter for TPI 2 may be defective.	Verify that A09U264-13 changes state during the test; also verify that pin 12 goes high during the test. If it does not go high, suspect A09U164.
The high four-bit counter for TPI 2 may be defective.	Verify that clock input A09U164-14 has carry out signal present. Verify that A09U164-12 goes high during the test. If these signals are not correct, suspect A09U264.
The TPI 2 NAND gate, A09U236D, may be defective.	Verify that the two inputs at pins 12 and 13 go high during the test and that the output pin 11 goes low. If the inputs appear correct and the output is not, suspect A09U236.
The TPI 2 prefilled flip-flop, A14U260A, is not being set.	Verify that A14U260-5 and -4 are low. Verify that pin 7 goes high during the test, and that a clock pulse is present on pin 6 while pin 7 is high. Check that the output pin 3 goes low. If the inputs appear correct and pin 3 does not go low, suspect A14U260.
The expander gate, A14U570, in the Trigger Control block may be defective.	Verify that A14U570-14 goes high during the test. Verify that the output pin 2 goes high. If not, suspect A14U570.
The read back buffer, A14U285 in the Trigger-Processor Interface, may be defective.	Verify that A14U285-10 goes high during the test. If so, suspect a faulty read back buffer A14U285.

6618 Error Index

Explanation: The Trigger Position Indicator 2 (TPI 2) upper eight-bit counter, A09U264 and A09U164, was loaded with AA_{hex}. The counter output was read back expecting AA_{hex}, but it was not.

Probable Cause	Action
The TPI 2 upper eight-bit counter, A09U264 and A09U164, may be defective.	Verify that pin 11 of both counters go low while the pattern AA_{hex} is present on input pins 15, 1, 10, and 9. If the inputs to the counter are correct, suspect A09U264 and A09U164.

6619 Error Index

Explanation: The TPI 2 counter was clocked 1376 times and the prefilled flip-flop, A14U260A, was not set.

Probable Cause	Action
The TPI 2 upper eight-bit counter, A09U264 and A09U164, may be defective.	Suspect A09U264 and A09U164.

TRIGGER BLOCK DIAGRAM
CTR TIMER – AREA 7

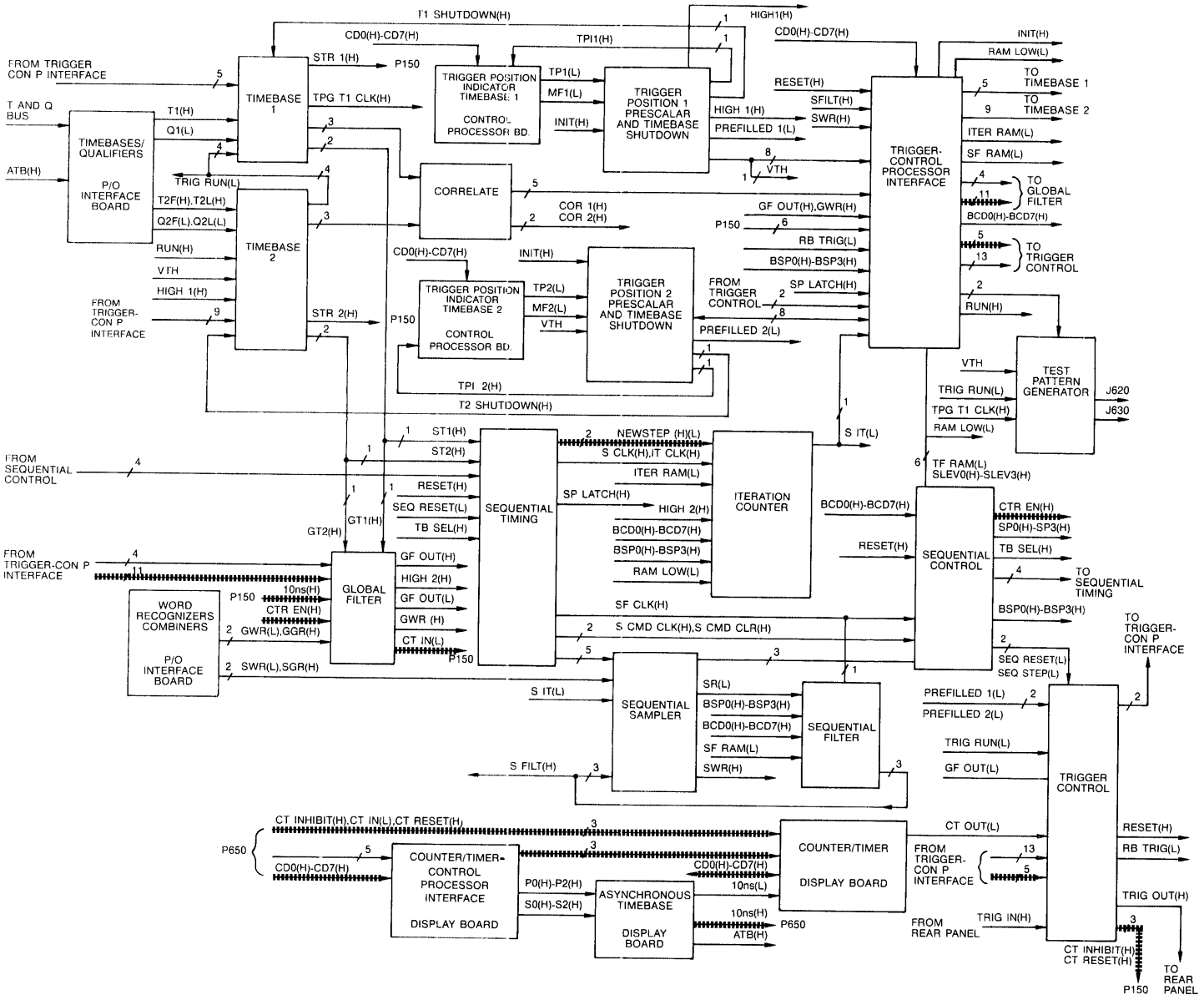

Figure 8-89. Trigger CTR/TIMER block diagram.

4342-125

TRIGGER BOARD – COMPONENT LOCATION

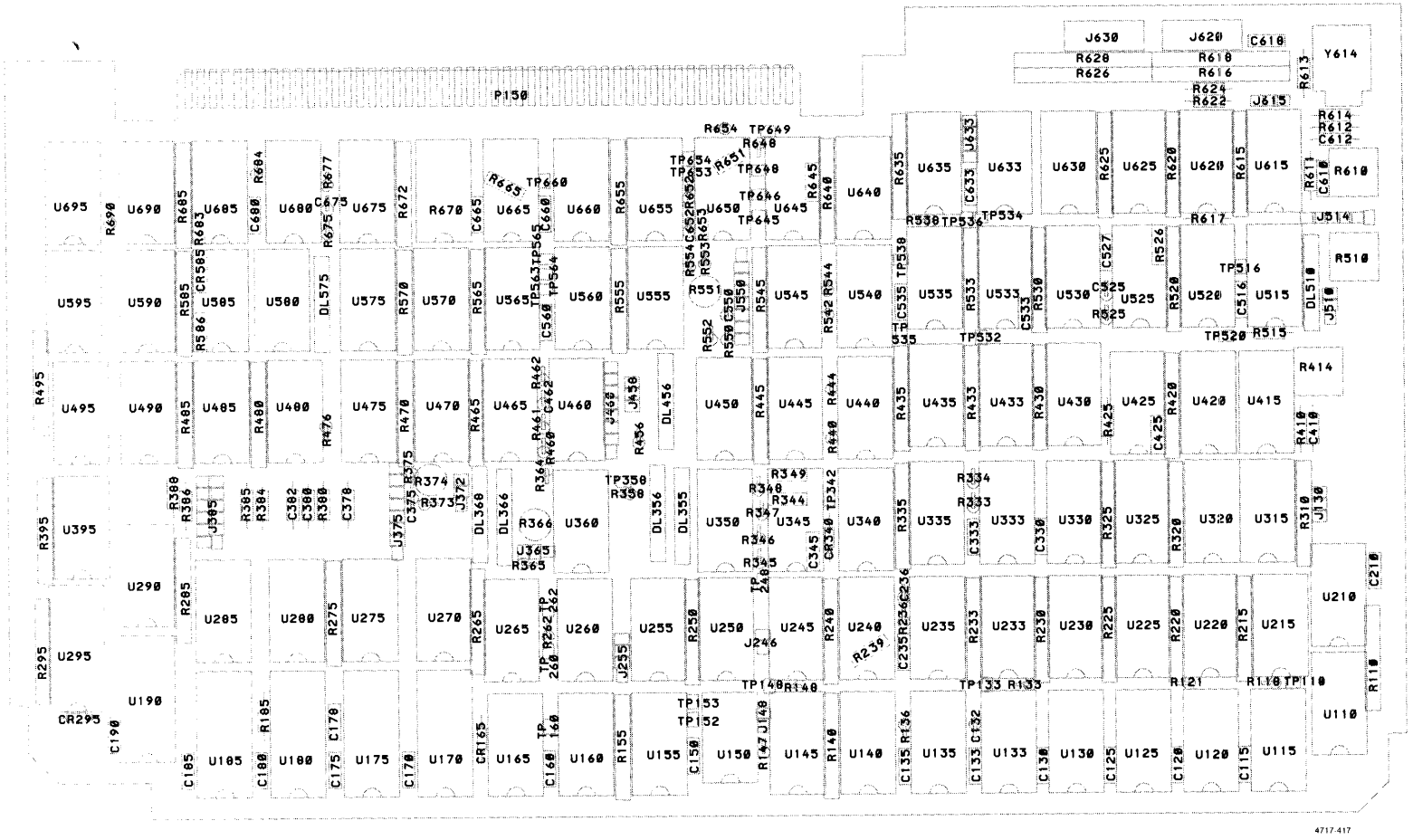

Figure 8-90. Trigger Board component location.

module: TRIGGER
area: CTR/TIMER

COUNTER/TIMER AREA – CIRCUIT OVERVIEW

The pattern-shaded signal lines on the timing block diagram indicate circuitry used during diagnostic testing. Only the circuitry that is being exercised for the first time during diagnostic testing is shown. Circuitry exercised by other diagnostic tests are shown in their respective block diagrams.

The Counter/Timer consists of four basic sections: Synchronizer, Prescaler, Accumulator, and Terminal Count. The counter/timer can be used to count occurrences of the output from the Global Filter, to start a 10 ns timer, or to time the duration of the global filter output. The programmed action is halted and any count or time values are stored when a trigger occurs. If the circuitry is preprogrammed with a value when the terminal count is reached or the timer times out, a trigger or reset command is sent to the Trigger Control block.

The counter/timer is a 37-bit, 100 MHz count-up circuit that can increment, start timing, or time while the CT IN(L) signal is active low. When used as a count-down circuit (increment to a limit), the circuit is preset to the terminal count minus the count down value. It then counts up to the terminal value.

COUNTER/TIMER AREA – TEST DESCRIPTION

The Counter/Timer test consists of three routines. Routine 1 partially verifies the Counter/Timer reset circuitry. Routine 2 verifies the operation of the counter RAM buffer, A11U505. Routine 3 verifies the operation of the stack pointer, A11U535.

ROUTINE 1 – TEST DESCRIPTION

6711

This routine partially verifies the Counter/Timer reset circuitry. When the CT RESET(H) signal goes active high, A11U450A and A11U540A are set. A11U608 and A11U610A & B are set by clocking A11U540A. Each of the flip-flops that are set by the CT RESET(H) signal can be read with address $FF42_{hex}$ via A11U600 on lines R0(H)-R3(H).

6711 Error Index

Explanation: The reset flip-flop, A11U540A, was not set by the CT RESET(H) signal.

Probable Cause	Action
The reset flip-flop, A11U540A, may be defective.	Verify that A11U540A-5 goes high during the test. Check pin 4 to ensure that it is not high. If pin 5 is high and pin 4 is low, check the output pin 2; it should be high. If not, replace A11U540.
The read back buffer, A11U600, may be defective.	Verify that A11U600-14 is high and that the buffer enable on pin 4 is also high. Verify that the gate enable signal on pin 15 is at Vbb. If the inputs appear correct, replace A11U600.

6712 Error Index

Explanation: The CT OUT(L) flip-flop, A11U470B, was not reset by the CT RESET(H) signal.

Probable Cause	Action
The CT OUT(L) flip-flop, A11U470B, may be defective.	Verify that A11U470B-13 goes high during the test. Check pin 12 to ensure that it is not high. If pin 13 is high and pin 12 is low, check the output pin 15; it should be low. If not, replace A11U470.
The read back buffer, A11U605, may be defective.	Verify that A11U605-14 is low and that the buffer enable on pin 4 is high. Verify that the gate enable signal on pin 15 is at Vbb. If the inputs appear correct, replace A11U605.

6713 Error Index

Explanation: The R3(H) flip-flop, A11U608A, was not reset by clocking A11U540A.

Probable Cause	Action
The R3(H) flip-flop, A11U608A, may be defective.	Verify that A11U608A-5 goes high during the test. Check pin 4 to ensure that it is not high. If pin 5 is high and pin 4 is low, check the output pin 3; it should be low. If not, replace A11U608.
The read back buffer, A11U600, may be defective.	Verify that A11U600-10 is low and that the buffer enable on pin 4 is high. Verify that the gate enable signal on pin 9 is at Vbb. If the inputs appear correct, replace A11U600.
The reset synchronizer A11U455A, may be defective.[1]	Verify U451A-4, 6, and 7 go high during the test. If A11U451A-2 does not pulse high, replace A11U451.[1]

[1] 670-7525-04 board only

6714 Error Index

Explanation: The preload 1 and preload 2 flip-flops, A11U610A & B, were not set by clocking A11U540A.

Probable Cause	Action
The preload 1 and 2 flip-flop, A11U610, may be defective.	Verify that A11U610B-12 goes high during the test. Check pin 13 to ensure that it is not high. If pin 12 is high and pin 13 is low, check the output pin 15; it should be high. If not, replace A11U610.
The read back buffer, A11U600, may be defective.	Verify that A11U600-2 and -6 are high and that the gate enables on pins 1 and 7 are at Vbb. If the inputs appear correct, replace A11U600.
The reset synchronizer A11U451A, may be defective.[1]	Verify U451A-4, 6, and 7 go high during the test. If A11U451A-2 does not pulse high, replace it.[1]

[1] 670-7525-04 board only

ROUTINE 2 – TEST DESCRIPTION

This routine verifies the operation of the counter RAM buffer, A11U505. The verification is accomplished by walking a value of one across the low four bits of the buffer U505. The Counter/Timer is placed in the control mode by setting bit 7 in the control latch to a one. The test pattern, 01_{hex}, 02_{hex}, 04_{hex}, and 08_{hex} is written to the latch. After each write, the contents of the buffer is read back and verified.

6714
6721

6721 Error Index

Explanation: The data read back from the buffer A11U505 is not correct.

Probable Cause	Action
The control latch, A11U400, may be defective.	Check for the expected data pattern on the inputs of A11U400-2, -5, -6, and -9. Verify that pin 19 is high. If the latch output pins are not correct, and if there is a clock present on pin 11, suspect A11U400.
The counter RAM buffer, A11U505, may be defective.	Check for the expected data pattern on the inputs of A11U505-5, -6, -7, and -10. Verify that pin 9 is low while the inputs are in the correct state. If the inputs are correct and the outputs are not, suspect A11U505.
The read back buffer, A11U500, may be defective.	Verify that the input pins A11U500-2, -6, -14, and -10 are pulsing high. Verify that pin 4 is high. Verify that the gate enable pins A11U500-1, -7, -15, and -9 are at Vbb. If the input signals appear correct, suspect A11U500.

ROUTINE 3 – TEST DESCRIPTION

Routine 3 verifies the operation of the stack pointer, A11U535, and its associated circuitry. To verify stack pointer operation, a value of one is walked across the four parallel load inputs of the counter A11U535. First, the CT RESET(H) line is asserted true and the R4(H) flip-flop, A11U540B, is set low. The reset flip-flop, A11U540A, was set when the CT RESET(H) line was asserted. The output of U540A is inverted by gate A11U545 and the output is wire-ORed to form the pin 10 input for the R4(H) flip-flop, A11U540B. A11U400-12 is asserted true for the input of A11U545B-6, holding the input to U540B-10 low. Now, the event count mode is selected for the Counter/Timer by asserting A11U400-15 true. The Counter/Timer is enabled by setting the CT INHIBIT(H) line low. When clock pulses are generated on the CT IN(L) line, the R4(H) flip-flop is reset and the chip enable at A11U535-6, the stack pointer, is held low to enable it.

The test pattern 01_{hex}, 02_{hex}, 04_{hex}, and 08_{hex} is now written to and read back from the stack pointer, A11U535.

6731 Error Index

Explanation: The R4(H) flip-flop could not be reset.

Probable Cause	Action
The NOR gate, A11U545B, may be defective.	Verify that the input pins A11U545-4 and -5 are high. Verify that the output pin 2 is low. If not, suspect A11U545.
The R4(H) flip-flop, A11U540B, may be defective.	Verify that A11U540-11 is low and that pin 9 is clocked (with a narrow pulse) each time the test is run. Verify that the output pin 15 goes low. If the inputs appear correct but the outputs are not, suspect A11U540.

6732 Error Index

Explanation: The stack pointer, A11U535, could not be loaded with the pattern from A11U400.

Probable Cause	Action
The inverter, A11U530C, may be defective.	Verify that the inputs to the inverter on A11U530-10 and -11 are high. Check that the output pin 14 is low. If it is not, suspect A11U530.
The expander gate, A11U555A, may be defective.	Verify that the input pins A11U555-7 and -6 are low. While looping on this test, verify a processor-stepped pulse on pin 9 and pin 3. If the output is not correct, suspect A11U555.
The stack pointer, A11U535, may be defective.	Verify that A11U535-5, -6, and -12 are low during the test. Verify that a 10 ns positive-going pulse is present on pin 13. Check that the 01_{hex}, 02_{hex}, 04_{hex}, and 08_{hex} pattern is being written to the inputs A11U530-7, -9, -10, and -11. If the inputs are correct, check the output pins for the pattern. If the pattern is not correct, suspect A11U535.[1]

[1] 670-7525-03 board only

6732

TRIGGER BLOCK DIAGRAM
ATB – AREA 8

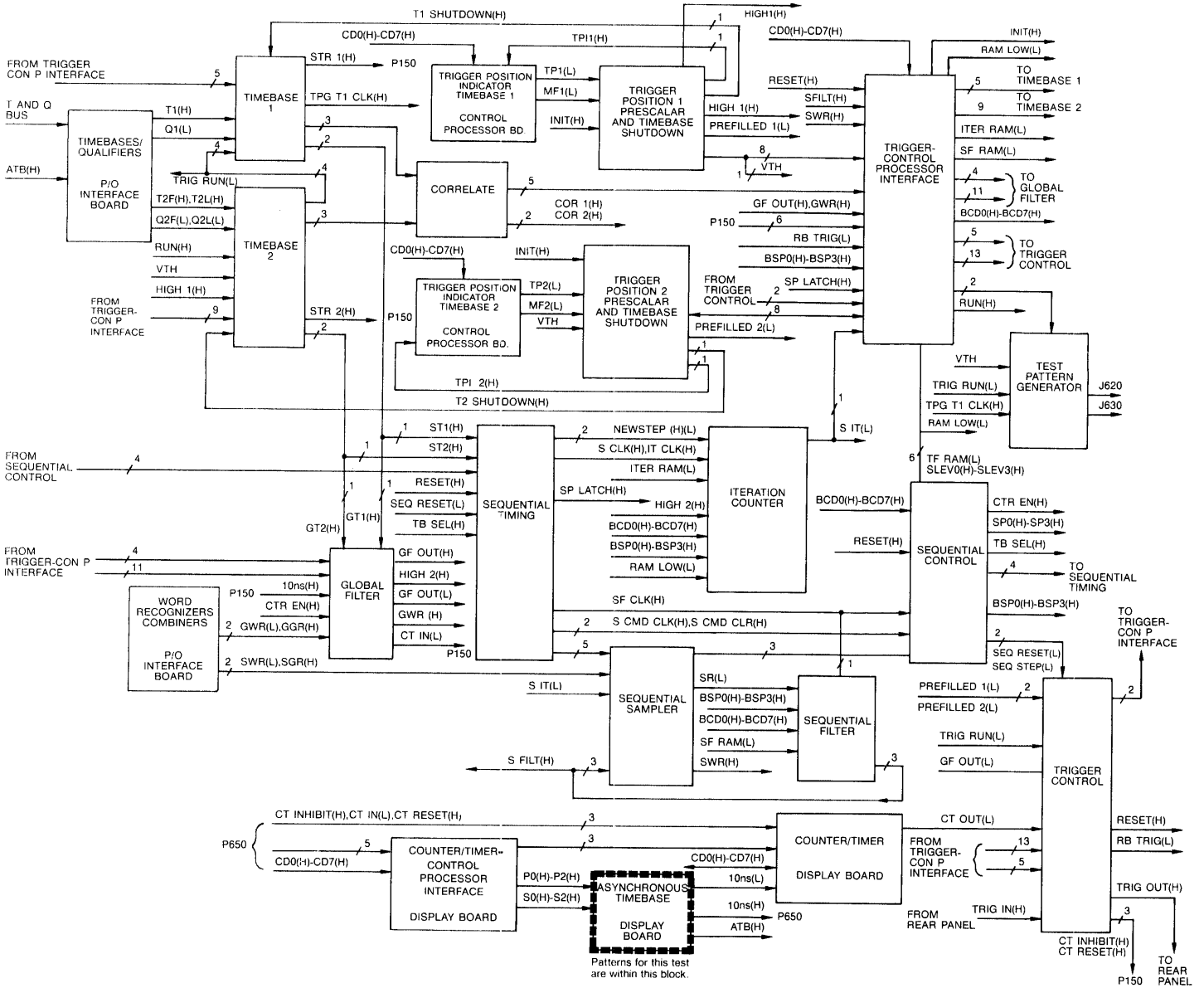

Figure 8-91. Trigger ATB block diagram.

4342-126

TRIGGER BOARD – COMPONENT LOCATION

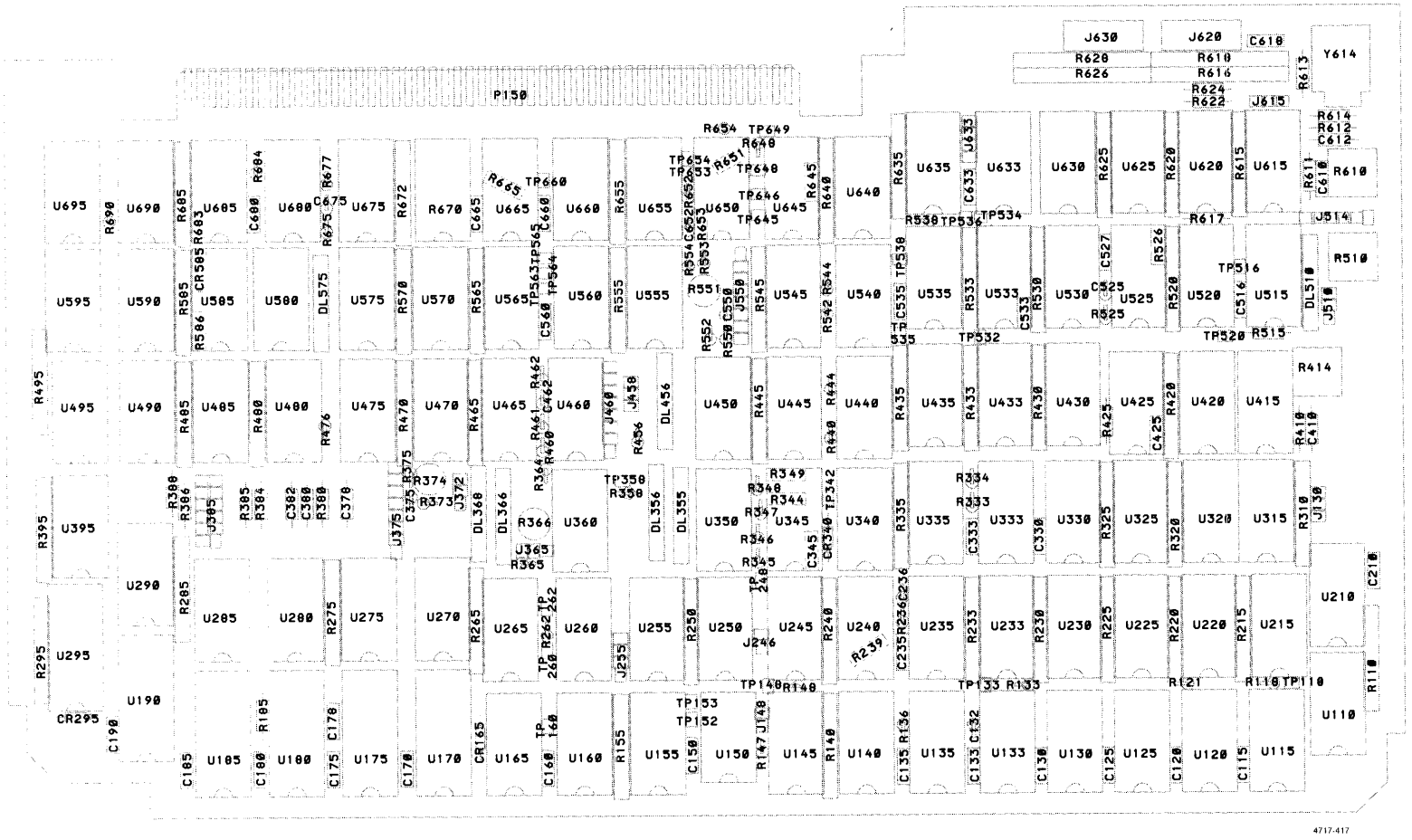

Figure 8-92. Trigger Board component location.

module: TRIGGER
area: ATB

ASYNCHRONOUS TIMEBASE AREA – CIRCUIT OVERVIEW

The pattern-shaded signal lines on the timing block diagram indicate circuitry used during diagnostic testing. Only the circuitry that is being exercised for the first time during diagnostic testing is shown. Circuitry exercised by other diagnostic tests are shown in their respective block diagrams.

The Asynchronous Timebase, located on the Display Board (assembly A11), generates acquisition clocks on timebase T1 at rates from 10 ns to 1 second in a 1-2-5 sequence. It also generates a 10 ns clock used by the global filter and counter/timer circuitry.

Components A11U545C, D and their associated passive components form a 100 MHz oscillator. This is the 10 ns asynchronous timebase sample rate. A11U450B, configured as a divide-by-two, produces a 20 ns sample rate. A11U455 is configured to produce a divide-by-five count and a divide-by-ten count. A11U465 selects the high speed clock rate to be either 10, 20, 50, or 100 ns. The firmware can select any of the four rates, or a logic high, or a logic low, through control of the P0(H)-P2(H) lines. A logic low is selected with a value of 4 or 6 on P0(H)-P2(H); a logic high is selected with a value of 5 or 7.

The output of multiplexer A11U465 is therefore a clock of period 10, 20, 50, or 100 ns, or a processor-derived rate determined by the firmware when it alternately selects a logic high and then a logic low.

A divide-by-ten prescaler, A11U565, produces output periods from 200 ns to 1 μs. A11U498B converts the ECL-level signals to TTL-level signals. The TTL counters, A11U580-590, are each configured to divide the signal frequency by a factor of ten. The final counter, A11U590B, produces a clock rate from 200 ms to 1 second. Multiplexer A11U570 selects the final output clock rate, while A11U475C, D, and the associated passive components form a pulse generator. This generator produces a 4 ns pulse width (approximately) for the output clock regardless of the rate selected. The clock pulse is ORed onto Timebase 1 by circuitry located on the Interface Board.

ASYNCHRONOUS TIMEBASE AREA – TEST DESCRIPTION

The Asynchronous Timebase test consists of eleven routines. Routines 1, 2, and 3 verify the divide-by-1, 10, and 100 sections of the multiplexer, A11U570. Routines 4 through 7 verify the divide-by-10^3, 10^4, 10^5, 10^6, and 10^7 sections, respectively, of the multiplexer A11U570. Routines 9, A, and B verify the 20 ns, 50 ns, and 100 ns base rate circuits for the Asynchronous Timebase.

ROUTINE 1 – TEST DESCRIPTION

This routine verifies the divide-by-1 section of the multiplexer, A11U570. First, the base rate input is selected on the multiplexer. The event latch, A14U485B, is reset and checked. Then the timebase is single stepped. The A14U485B event latch should be set if the multiplexer A14U345 is working correctly. The address of the latch is returned in the result address field. The expected result should always be 80_{hex}. If the latch was set, 80_{hex} is returned in the actual result field. If the latch was not set, 00_{hex} is returned.

6810 Error Index

Explanation: It is not possible to reset the event latch, A14U485B.

Probable Cause	Action
A14U485 may be defective.	Run the Global Filter tests (62XX) to check the latch.

6811 Error Index

Explanation: The latch A14U485B on the Trigger Board was not set when the Asynchronous Timebase (ATB) was stepped.

Probable Cause	Action
The ATB latch, A11U598, may be defective.	Verify the following pins: 1, 2, 5, 6, 10, 12 and 19 should be low; pins 15 and 20 should be high; pin 9 should transition from low to high; pin 11 should transition from high to low.
The base rate multiplexer, A11U465, may not be generating a single step pulse. A11U465-12 may not be pulled up to +5 volts.	Check pin U465-12 for a high. If not present, check R470 and CR465.
A11U465 may not be working correctly.	Verify a positive pulse on the output of A11U465-15 each time the test is run. If no pulse is present, suspect A11U465.
A11U570 may not be working correctly.	Verify a positive pulse on A11U570-6 and -15 each time the test is run. If no pulse is present, suspect A11U570.
A11U475D & C, the output pulse generator circuit, may be defective.	Verify a positive pulse on A11U475-12 and -13. Verify a narrow positive-going pulse on the output pin 14. If no pulse is present, check R480, R481, and C480. If no problems found, suspect A11U475.

ROUTINE 2 – TEST DESCRIPTION

This routine verfies the divide-by-10 section of the multiplexer U570. First, the base rate input is selected on the multiplexer. The event latch, A14U485B, is reset and checked. Then the timebase is single stepped 10 times. A14U485B should be set if the multiplexer A14U345 is working correctly. The address of the latch is returned in the result address field. The expected result should always be 80_{hex}. If the latch was set, 80_{hex} is returned in the actual result field. If the latch was not set, 00_{hex} is returned.

6820 Error Index

Explanation: It is not possible to reset A14U485B.

Probable Cause	Action
The latch on the Trigger Board may be defective.	Run the Global Filter tests (62XX) to check the latch.

6821 Error Index

Explanation: The A14U485B was not set when the Asynchronous Timebase (ATB) was stepped.

Probable Cause	Action
The ATB latch, A11U598, may be defective.	Verify the following pins: 1, 5, 6, 10, 12 and 19 should be low; pins 2, 15, and 20 should be high; pin 9 should transition from low to high; pin 11 should transition from high to low.
A11U565, the divide-by-10 stage of the decade divider circuit, may be defective.	Verify ten positive pulses on input pin A11U565-13 each time the test is run. Verify a positive pulse from the output A11U565-14 each time the test is run. If no pulse is present on the output, suspect A11U565.
Multiplexer A11U570 may be defective.	Verify a positive-going pulse on input pin A11U570-5 each time the test is run. Verify a positive-going pulse on the output pin A11U570-15 each time the test is run. If no pulse is present, suspect A11U570.
A11U475D & C, the output pulse generator circuit, may be defective.	Verify a positive pulse on A11U475-12 and -13. Verify a narrow positive-going pulse on the output pin 14. If no pulse is present, check R480, R481, and C480. If no problems found, suspect A11U475.

ROUTINE 3 – TEST DESCRIPTION

This routine verfies the divide-by-100 section of the multiplexer U570. First, the base rate input is selected on the multiplexer. The event latch, A14U485B, is reset and checked. Then the timebase is single stepped 100 times. A14U485B should be set if the multiplexer A14U345 is working correctly. The address of the latch is returned in the result address field. The expected result should always be 80_{hex}. If the latch was set, 80_{hex} is returned in the actual result field. If the latch was not set, 00_{hex} is returned.

6830 Error Index

Explanation: It is not possible to reset the latch A14U485B.

Probable Cause	Action
The latch on the Trigger Board may be defective.	Run the Global Filter tests (62XX) to check the latch.

6831 Error Index

Explanation: The latch A14U485B was not set when the Asynchronous Timebase (ATB) was stepped.

Probable Cause	Action
The ATB latch, A11U598, may be defective.	Verify the following pins: 1, 2, 6, 10, 12 and 19 should be low; pins 5, 15, and 20 should be high; pin 9 should transition from low to high; pin 11 should transition from high to low.
The ECL-to-TTL level shift, A11U498B, may be defective.	Verify that input A11U498-6 has ten positive-going ECL pulses each time the test is run; also, verify the output A11U498-5 has the ten pulses. If no pulses are present, check resistors A11R396 and R397; otherwise suspect A11U498.
A11U580A, the second divide-by-10 stage of the decade divider circuit, may be defective.	Verify ten positive pulses on input pin A11U580-1 each time the test is run. Verify ten positive pulses from the output U580-7 each time the test is run. If no pulses are present on the output, suspect A11U580.
Multiplexer A11U570 may be defective.	Verify a positive-going pulse on input pin A11U570-4 each time the test is run. Verify a positive-going pulse on the output pin A11U570-15 each time the test is run. If no pulse is present, suspect A11U570.

ROUTINE 4 – TEST DESCRIPTION

This routine verfies the divide-by-10^3 (ten to the third power) section of the multiplexer A11U570. First, the base rate input is selected on the multiplexer. The event latch, A14U485B, is reset and checked. Then the timebase is single stepped 10^3 times. Latch A14U485B should be set if the multiplexer A14U345 is working correctly. The address of the latch is returned in the result address field. The expected result should always be 80_{hex}. If the latch was set, 80_{hex} is returned in the actual result field. If the latch was not set, 00_{hex} is returned.

6840 Error Index

Explanation: It is not possible to reset the latch A14U485B.

Probable Cause	Action
A14U485 may be defective.	Run the Global Filter tests (62XX) to check the latch.

6841 Error Index

Explanation: Latch A14U485B was not set when the Asynchronous Timebase (ATB) was stepped 10^3 times.

Probable Cause	Action
The ATB latch, A11U598, may be defective.	Verify the following pins: 1, 6, 10, 12 and 19 should be low; pins 2, 5, 15, and 20 should be high; pin 9 should transition from low to high; pin 11 should transition from high to low.
A11U580B, the third divide-by-10 stage of the decade divider circuit, may be defective.	Verify ten positive pulses on input pin A11U580-15 each time the test is run. Verify ten positive pulses from the output U580-9 each time the test is run. If no pulses are present on the output, suspect A11U580.
Multiplexer A11U570 may be defective.	Verify a positive-going pulse on input pin A11U570-3 each time the test is run. Verify a positive-going pulse on the output pin A11U570-15 each time the test is run. If no pulse is present, suspect A11U570.

ROUTINE 5 – TEST DESCRIPTION

This routine verfies the divide-by-10^4 section of the multiplexer A11U570. First, the base rate input is selected on the multiplexer. The event latch, A14U485B, is reset and checked. Then the timebase is single stepped 10^4 times. Latch A14U485B should be set if the multiplexer A14U345 is working correctly. The address of the latch is returned in the result address field. The expected result should always be 80_{hex}. If the latch was set, 80_{hex} is returned in the actual result field. If the latch was not set, 00_{hex} is returned.

6850 Error Index

Explanation: It is not possible to reset latch A14U485B.

Probable Cause	Action
The latch on the Trigger Board may be defective.	Run the Global Filter tests (62XX) to check the latch.

6851 Error Index

Explanation: Latch A14U485B was not set when the Asynchronous Timebase (ATB) was stepped 10^4 times.

Probable Cause	Action
The ATB latch, A11U598, may be defective.	Verify the following pins: 1, 2, 5, 10, 12 and 19 should be low; pins 6, 15, and 20 should be high; pin 9 should transition from low to high; pin 11 should transition from high to low.
A11U585A, the fourth divide-by-10 stage of the decade divider circuit, may be defective.	Verify ten positive pulses on input pin A11U585-1 each time the test is run. Verify ten positive pulses from the output U585-7 each time the test is run. If no pulses are present on the output, suspect A11U585.
Multiplexer A11U570 may be defective.	Verify a positive-going pulse on input pin A11U570-11 each time the test is run. Verify a positive-going pulse on the output pin A11U570-15 each time the test is run. If no pulse is present, suspect A11U570.

ROUTINE 6 – TEST DESCRIPTION

This routine verfies the divide-by-10^5 section of the multiplexer A11U570. First, the base rate input is selected on the multiplexer. The event latch, A14U485B, is reset and checked. Then the timebase is single stepped 10^5 times. Latch A14U485B should be set if the multiplexer A14U345 is working correctly. The address of the latch is returned in the result address field. The expected result should always be 80_{hex}. If the latch was set, 80_{hex} is returned in the actual result field. If the latch was not set, 00_{hex} is returned.

6860 Error Index

Explanation: It is not possible to reset latch A14U485B.

Probable Cause	Action
A14U485 may be defective.	Run the Global Filter tests (62XX) to check the latch.

6861 Error Index

Explanation: Latch A14U485B was not set when the Asynchronous Timebase (ATB) was stepped 10^4 times.

Probable Cause	Action
The ATB latch, A11U598, may be defective.	Verify the following pins: 1, 5, 10, 12 and 19 should be low; pins 2, 6, 15, and 20 should be high; pin 9 should transition from low to high; pin 11 should transition from high to low.
A11U585B, the fifth divide-by-10 stage of the decade divider circuit, may be defective.	Verify ten positive pulses on input pin A11U585-15 each time the test is run. Verify that there are ten positive pulses from the output U585-9 each time the test is run. If no pulses are present on the output, suspect A11U585.
Multiplexer A11U570 may be defective.	Verify a positive-going pulse on input pin A11U570-12 each time the test is run. Verify a positive-going pulse on the output pin A11U570-15 each time the test is run. If no pulse is present, suspect A11U570.

ROUTINE 7 – TEST DESCRIPTION

This routine verfies the divide-by-10^6 section of the multiplexer A11U570. First, the 10 ns clock (base rate input) is selected on the multiplexer. With the 10 ns clock selected, the output cycle from the multiplexer is 10 ms. Using a processor timing loop, increment the decade divider in 1 ms bursts of 10 ns clocks until the output of the multiplexer goes low. If the output does not go low within 8 ms (1 ms longer than the negative half of the cycle divide rate of the selected decade rate), then report an error. Latch A14U485B should be set if the multiplexer A14U345 is working correctly. The address of the latch is returned in the result address field. The expected result should always be 80_{hex}. If the latch was set, 80_{hex} is returned in the actual result field. If the latch was not set, 00_{hex} is returned.

6870 Error Index

Explanation: It is not possible to reset latch A14U485B.

Probable Cause	Action
Latch A14U485B may be defective.	Run the Global Filter tests (62XX) to check the latch.

6871 Error Index

Explanation: The output of the sixth stage of the decade divider would not go low.

Probable Cause	Action
The 100 MHz oscillator may be defective.	Verify the 100 MHz clock on A11U545-12 and -9. If not present, verify the part associated with the 100 MHz ocsillator. If parts appear to be good, then suspect A11U545.
A11U590A, the sixth divide-by-10 stage of the decade divider circuit, may be defective.	Verify ten positive pulses on input pin A11U590-1 each time the test is run. Verify ten positive pulses from the output U590-7 each time the test is run. If no pulses are present on the output, suspect A11U590.

6872 Error Index

Explanation: Latch A14U485B was not set when the Asynchronous Timebase (ATB) was stepped 10^6 times.

Probable Cause	Action
The ATB latch, A11U598, may be defective.	Verify the following pins: 1, 2, 9, 10, 12, 15, and 19 should be low; pins 5, 6, and 20 should be high; pin 11 should transition from high to low.
A11U570, the multiplexer may be defective.	Verify ten positive pulses on input pin A11U570-13 each time the test is run. Verify ten positive pulses from the output U570-15 each time the test is run. If no pulses are present on the output, suspect A11U570.

ROUTINE 8 – TEST DESCRIPTION

This routine verfies the divide-by-10^7 section of the multiplexer, A11U570. First, the 10 ns clock (base rate input) is selected on the multiplexer. With the 10 ns clock selected, the output cycle from the multiplexer is 100 ms. Using a processor timing loop, increment the decade divider in 1 ms bursts of 10 ns clocks until the output of the multiplexer goes low. If the output does not go low within 80 ms (10 ms longer than the negative half of the cycle divide rate of the selected decade rate), then report an error. Latch A14U485B should be set if the multiplexer A14U345 is working correctly. The address of the latch is returned in the result address field. The expected result should always be 80_{hex}. If the latch was set, 80_{hex} is returned in the actual result field. If the latch was not set, 00_{hex} is returned.

6880 Error Index

Explanation: It is not possible to reset the latch A14U485B.

Probable Cause	Action
Latch A14U485B may be defective.	Run the Global Filter tests (62XX) to check the latch.

6881 Error Index

Explanation: The output of the seventh stage of the decade divider would not go low.

Probable Cause	Action
A11U590B, the seventh divide-by-10 stage of the decade divider circuit, may be defective.	Verify ten positive pulses on input pin A11U590-15 each time the test is run. Verify ten positive pulses from the output U590-9 each time the test is run. If no pulses are present on the output, suspect A11U590.

6882 Error Index

Explanation: Latch A14U485B was not set when the Asynchronous Timebase (ATB) was stepped 10^7 times.

Probable Cause	Action
The ATB latch, A11U598, may be defective.	Verify the following pins: 1, 2, 9, 10, 12, 15, and 19 should be low; pins 5, 6, and 20 should be high; pin 11 should transition from high to low.
A11U570, the multiplexer may be defective.	Verify ten positive pulses on input pin A11U570-14 each time the test is run. Verify ten positive pulses from the output U570-15 each time the test is run. If no pulses are present on the output, suspect A11U570.

ROUTINE 9 – TEST DESCRIPTION

This routine verfies the 20 ns base rate circuits for the Asynchronous Timebase. First, the 20 ns clock is selected from the multiplexer, A11U465. The divide-by-10^6 stage of the decade divider circuit is selected. With the 20 ns clock selected, the output cycle from the multiplexer is 20 ms. Using a processor timing loop, increment the decade divider in 1 ms bursts of 20 ns clocks until the output of the multiplexer goes low. If the output does not go low within 16 ms (1 ms longer than the negative half of the cycle divide rate of the selected decade rate), then report an error. Latch A14U485B should be set if the multiplexer A14U345 is working correctly. The address of the latch is returned in the result address field. The expected result should always be 80_{hex}. If the latch was set, 80_{hex} is returned in the actual result field. If the latch was not set, 00_{hex} is returned.

6890 Error Index

Explanation: It is not possible to reset the latch A14U485B.

Probable Cause	Action
Latch A14U485B may be defective.	Run the Global Filter tests (62XX) to check the latch.

6891 Error Index

Explanation: The output of the sixth stage of the decade divider would not go low.

Probable Cause	Action
The divide-by two stage of the base rate circuit may be defective.	Verify a 100 MHz clock on A11U450-9. If not present, check connection to A11U545-9. Also, verify a 50 MHz clock on A11U450-14. If not present, suspect A11U545.
The ATB latch, A11U598, may be defective.	Verify the following pins: 1, 2, 10, 12, 15, and 19 should be low; pins 5, 6, 9, and 20 should be high; pin 11 should transition from high to low.
The base rate multiplexer, A11U465, may be defective.	Verify a 50 MHz on the input, A11U465-5, and the output U465-15. If problems are found, suspect A11U465.

6892 Error Index

Explanation: Latch A14U485B was not set when the Asynchronous Timebase (ATB) was stepped by the 50 MHz clock.

Probable Cause	Action
The problem is in circuitry that was previously tested.	Run diagnostic routines 6810 through 6872 to isolate the problem.

ROUTINE A – TEST DESCRIPTION

This routine verfies the 50 ns base rate circuits for the Asynchronous Timebase. First, the 50 ns clock is selected from the multiplexer, A11U465. The divide-by-10^6 stage of the decade divider circuit is selected. With the 50 ns clock selected, the output cycle from the multiplexer is 50 ms. Using a processor timing loop, increment the decade divider in 1 ms bursts of 50 ns clocks until the output of the multiplexer goes low. If the output does not go low within 45 ms (5 ms longer than the negative half of the cycle divide rate of the selected decade rate), then report an error. Latch A14U485B should be set if the multiplexer A14U345 is working correctly. The address of the latch is returned in the result address field. The expected result should always be 80_{hex}. If the latch was set, 80_{hex} is returned in the actual result field. If the latch was not set, 00_{hex} is returned.

68A0 Error Index

Explanation: It is not possible to reset the latch A14U485B.

Probable Cause	Action
Latch A14U485B may be defective.	Run the Global Filter tests (62XX) to check the latch.

68A1 Error Index

Explanation: The output of the sixth stage of the decade divider would not go low.

Probable Cause	Action
The divide-by-five stage of the base rate circuit, A11U455, may be defective.	Verify a 100 MHz clock on A11U455-13. If not present, check connection to A11U545-9. Also, verify a 20 MHz clock on A11U455-2. If not present, suspect A11U545.
The ATB latch, A11U598, may be defective.	Verify the following pins: 1, 2, 9, 10, 15, and 19 should be low; pins 5, 6, 12, and 20 should be high; pin 11 should transition from high to low.
The base rate multiplexer, A11U465, may be defective.	Verify a 20 MHz on the input, A11U465-4, and the output U465-15. If problems are found, suspect A11U465.

68A2 Error Index

Explanation: Latch A14U485B was not set when the Asynchronous Timebase (ATB) was stepped by the 20 MHz clock.

Probable Cause	Action
The problem is in circuitry that was previously tested.	Run diagnostic routines 6810 through 6872 to isolate the problem.

ROUTINE B – TEST DESCRIPTION

This routine verfies the 100 ns base rate circuits for the Asynchronous Timebase. First, the 100 ns clock is selected from the multiplexer, A11U565. The divide-by-10^6 stage of the decade divider circuit is selected. With the 100 ns clock selected, the output cycle from the multiplexer is 100 ms. Using a processor timing loop, increment the decade divider in 1 ms bursts of 100 ns clocks until the output of the multiplexer goes low. If the output does not go low within 80 ms (10 ms longer than the negative half of the cycle divide rate of the selected decade rate), then report an error. Latch A14U485B should be set if the multiplexer A14U345 is working correctly. The address of the latch is returned in the result address field. The expected result should always be 80_{hex}. If the latch was set, 80_{hex} is returned in the actual result field. If the latch was not set, 00_{hex} is returned.

68B0 Error Index

Explanation: It is not possible to reset the latch A14U485B.

Probable Cause	Action
Latch A14U485B may be defective.	Run the Global Filter tests (62XX) to check the latch.

68B1 Error Index

Explanation: The output of the sixth stage of the decade divider would not go low.

Probable Cause	Action
The divide-by-10 stage of the base rate circuit, A11U455, may be defective.	Verify a 100 MHz clock on A11U455-13. If not present, check connection to A11U545-9. Also, verify a 10 MHz clock on A11U455-14. If not present, suspect A11U545.
The ATB latch, A11U598, may be defective.	Verify the following pins: 1, 2, 10, 15, and 19 should be low; pins 5, 6, 9, 12, and 20 should be high; pin 11 should transition from high to low.
The base rate multiplexer, A11U465, may be defective.	Verify a 10 MHz on the input, A11U465-3, and the output U465-15. If problems are found, suspect A11U465.

68B2 Error Index

Explanation: Latch A14U485B was not set when the Asynchronous Timebase (ATB) was stepped by the 10 MHz clock.

Probable Cause	Action
The problem is in circuitry that was previously tested.	Run diagnostic routines 6810 through 6872 to isolate the problem.

TRIGGER BLOCK DIAGRAM
TIMING – AREA 9

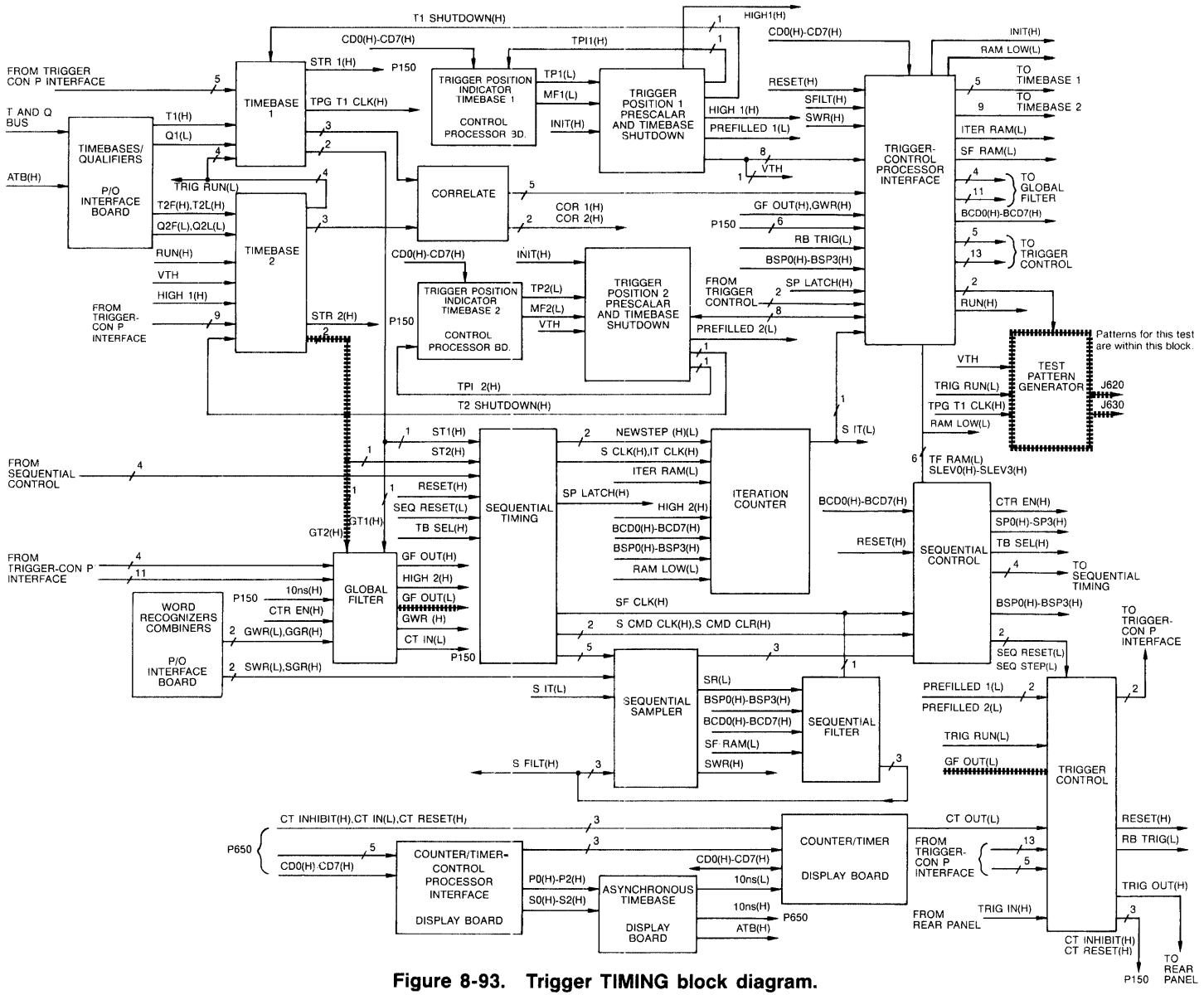

Figure 8-93. Trigger TIMING block diagram.

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TRIGGER BOARD – COMPONENT LOCATION

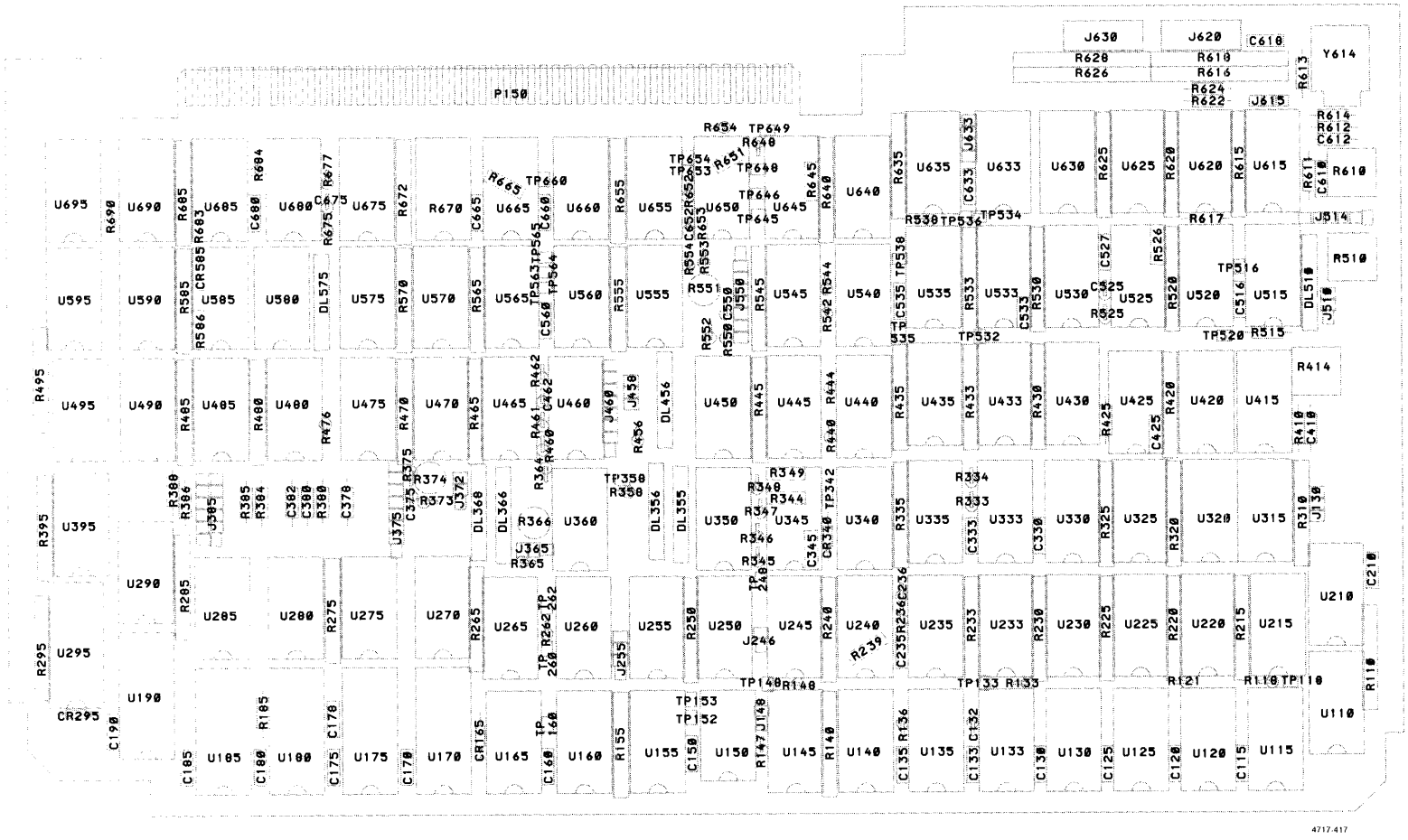

Figure 8-94. Trigger Board component location.

module: TRIGGER
area: TIMING

TIMING AREA – CIRCUIT OVERVIEW

The pattern-shaded signal lines on the timing block diagram indicate circuitry used during diagnostic testing. Only the circuitry that is being exercised for the first time during diagnostic testing is shown. Circuitry exercised by other diagnostic tests are shown in their respective block diagrams.

The timing tests use circuitry from three different areas of the trigger/acquisition system. These areas include the following:

- Global Filter timing circuits
- Sequential timing circuits
- Sequential Filter timing circuits

Since the theory overview for these areas is lengthy, the descriptions are not included here. For circuit descriptions, refer to the appropriate theory discussion in the *Theory of Operation* section.

TIMING AREA – TEST DESCRIPTION

This test is run only if a 9- or 18-Channel Acquisition Board is installed in slot 0 next to the Trigger Board. The test also requires that an acquisition probe be installed and connected to the Test Pattern Generator.

The timing test consists of three routines. Routine 1 verifies Global Filter timing. Routine 2 verifies the timing of the Sequential Stack. Routine 3 verifies Sequential Filter timing.

ROUTINE 1 – TEST DESCRIPTION

This routine verifies the timing of the Global Filter. The test is performed only if there is an acquisition card in slot 0; otherwise the test is aborted and a failure is reported.

First, the acquisition card is polled to verify that an acquisition probe is properly connected. The Global Word Recognizer is programmed to recognize the pattern, 155_{hex}. The Global Filter timebase selection is set to 10 ns and the filter is programmed to trigger on a global event. The Test Pattern Generator (TPG) is set to run from its local oscillator at 12 MHz. The Asynchronous Timebase (ATB) is programmed to generate a 20 ns clock as the T1 timebase. The memory full value is set to stop the acquisition clock after two passes. Once the machine is started, the test expects a trigger to occur. Failure to trigger is an indication that the instrument did not meet the T1 Filter Acceptance - Asynchronous specification. The test is aborted and a failure is reported.

Next, the Global Filter is set to a value of 5 and the timebase selection is T1 asynchronous (edge) mode. Once the machine is started, the test expects a trigger not to occur. Trigger indicates that the instrument did not meet the T1 Filter Rejection - Asynchronous specification. The test is aborted and a failure is reported.

The Global Word recognizer is programmed to recognize $01E_{hex}$. The T2LF clock is selected as the acquisition clock. The ATB is set to 20 ns and the Global Filter is set to a value of 3. Once the machine is started, the test expects a trigger to occur. Failure to trigger is an indication that the instrument did not meet the T2 Filter Acceptance - Synchronous specification. The test is aborted and a failure is reported.

Finally, the Global Filter is set to a value of 5 and the machine is started. This time, the test expects the machine not to trigger. If a trigger does occur, it indicates that the instrument did not meet the T2 Filter Rejection - Synchronous specification. The test is aborted and a failure is reported.

6911 Error Index

Explanation: The acquisition probes are not connected.

Probable Cause	Action
The acquisition probes are defective or not securely plugged in.	Check all probe connections and rerun the test. If failure still exists, replace the probes.

6912 Error Index

Explanation: A trigger was not detected.

Probable Cause	Action
The Global Word recognizer may be defective.	Ensure that the acquisition card in slot 0 passed all diagnostic tests. There may be a timing problem with A14U675 and A14U570.

6913 Error Index

Explanation: No trigger was expected, but a trigger did occur.

Probable Cause	Action
There may be a timing problem.	Check A14U675 and A14U570.

6914 Error Index

Explanation: A trigger was expected, but it did not occur.

Probable Cause	Action
There may be a timing problem.	Check A14U675 and A14U570.

6915 Error Index

Explanation: No trigger was expected, but a trigger did occur.

Probable Cause	Action
There may be a timing problem.	Check A14U675 and A14U570.

ROUTINE 2 – TEST DESCRIPTION

This routine verifies the timing of the sequential stack. The test is performed only if there is an acquisition card in slot 0; otherwise the test is aborted and a failure is reported.

The test checks the speed of the sequential stack timing circuits using the trigger module and the acquisition card in slot 0. The Test Pattern Generator (TPG) is incremented by the 50 ns Asynchronous Timebase (ATB) on the T1 clock line. The Sequential Word Recognizers are programmed in the following sequence:

- Level 1 (F) if sequential event $1BE_{hex}$ is true, step to Level 2 (E)
- Level 2 (E) if sequential event $17D_{hex}$ is true, step to Level 3 (D)
- Level 3 (D) if sequential event $0BA_{hex}$ is true, step to Level 4 (C)
- Level 4 (C) if sequential event $1C0_{hex}$ occurs twice, step to Level 5 (B)
- Level 5 (B) do nothing if/if not (stay here until trigger occurs).

6921 Error Index

Explanation: The acquisition probes are not connected.

Probable Cause	Action
The acquisition probes are defective or not securely plugged in.	Check all probe connections and rerun the test. If failure still exists, replace the probes.

6922 Error Index

Explanation: The sequence pointer should have gone to B_{hex} (readback via A14U115 and U110).

Probable Cause	Action
The sequence pointer did not step to the correct level.	Ensure that the acquisition card in slot 0 passed all diagnostic tests. Using the SWR programming information described earlier and the Actual data displayed on the screen, determine which level the failure occurred.

6923 Error Index

Explanation: No trigger was expected, but a trigger did occur.

Probable Cause	Action
There may be a timing problem with A14U675.	While looping on this routine, verify that the sequential step signal is toggling on A14U675-7 when the sequential pointer is not at B_{hex} (i.e., check for a sequential step when the sequential pointer is at F_{hex}, E_{hex}, D_{hex}, and C_{hex}).

6924 Error Index

Explanation: A trigger did not occur, therefore the sequence pointer did not step.

Probable Cause	Action
There may be a timing problem with RAMs A14U135, U235, or U330.	Using a logic analyzer, verify that A14U330 outputs D_{hex} when BSP0(L)-BSP3(L) = F_{hex}, E_{hex}, D_{hex}, and C_{hex}. Also verify the output is F_{hex} when BSP0(L)-BSP3(L) = B_{hex}. Check that A14U135 outputs E_{hex}, D_{hex}, C_{hex}, B_{hex}, and B_{hex} when BSP0(L)-BSP3(L) = F_{hex}, E_{hex}, D_{hex}, C_{hex}, and B_{hex}, respectively. Check that A14U235 outputs F_{hex}, E_{hex}, D_{hex}, C_{hex}, and B_{hex} when BSP0(L)-BSP3(L) = F_{hex}, E_{hex}, D_{hex}, C_{hex}, and B_{hex}, respectively.

ROUTINE 3 – TEST DESCRIPTION

This routine verifies the timing of the Sequential Filter. The test is performed only if there is an acquisition card in slot 0; otherwise the test is aborted and a failure is reported.

First, the acquisition card is polled to verify that an acquisition probe is properly connected. The Sequential Word Recognizers are programmed to recognize the pattern, 155_{hex}. The Sequential Filter is set to a value of $0D_{hex}$. The trigger is set to generate a trigger on recognition of a sequential event, edge mode. The Test Pattern Generator (TPG) is set to run from its local oscillator at 12 MHz. The Asynchronous Timebase (ATB) is programmed to generate a 20 ns clock as the T1 timebase. The memory full value is set to stop the acquisition clock after two passes. Once the machine is started, the test expects a trigger to occur. If a trigger does not occur, the test is aborted and a failure is reported.

6924
6931

Now, the Sequential Filter is set to a value of $0B_{hex}$ and the timebase selection is T1 asynchronous (edge) mode. Once the machine is started, the test expects that a trigger does not occur. If a trigger occurs, the test is aborted and a failure is reported.

6931 Error Index

Explanation: The acquisition probes are not connected.

Probable Cause	Action
The acquisition probes are defective or not securely plugged in.	Check all probe connections and rerun the test. If failure still exists, replace the probes.

6932 Error Index

Explanation: A trigger did not occur.

Probable Cause	Action
The Sequential Word recognizer may be defective.	Ensure that the acquisition card in slot 0 passed all diagnostic tests.
The Sequential Filter may be defective.	Refer to Trigger schematic number 24. Verify that A14U335 and U435 are being loaded correctly with D_{hex}; also, verify that A14U435 counts correctly.

6933 Error Index

Explanation: A trigger did occur.

Probable Cause	Action
A14U675 may be defective.	Refer to Trigger schematic number 25.
The Sequential Filter may be defective.	Refer to Trigger schematic 24. Verify that A14U335 and U435 are being loaded correctly with B_{hex}; also, verify that A14U435 counts correctly. Check that latch A14U440B is operating correctly; if U440B is not the problem, follow the signal path out until the problem is found.

TRIGGER BLOCK DIAGRAM
X SEQ CTL – AREA A

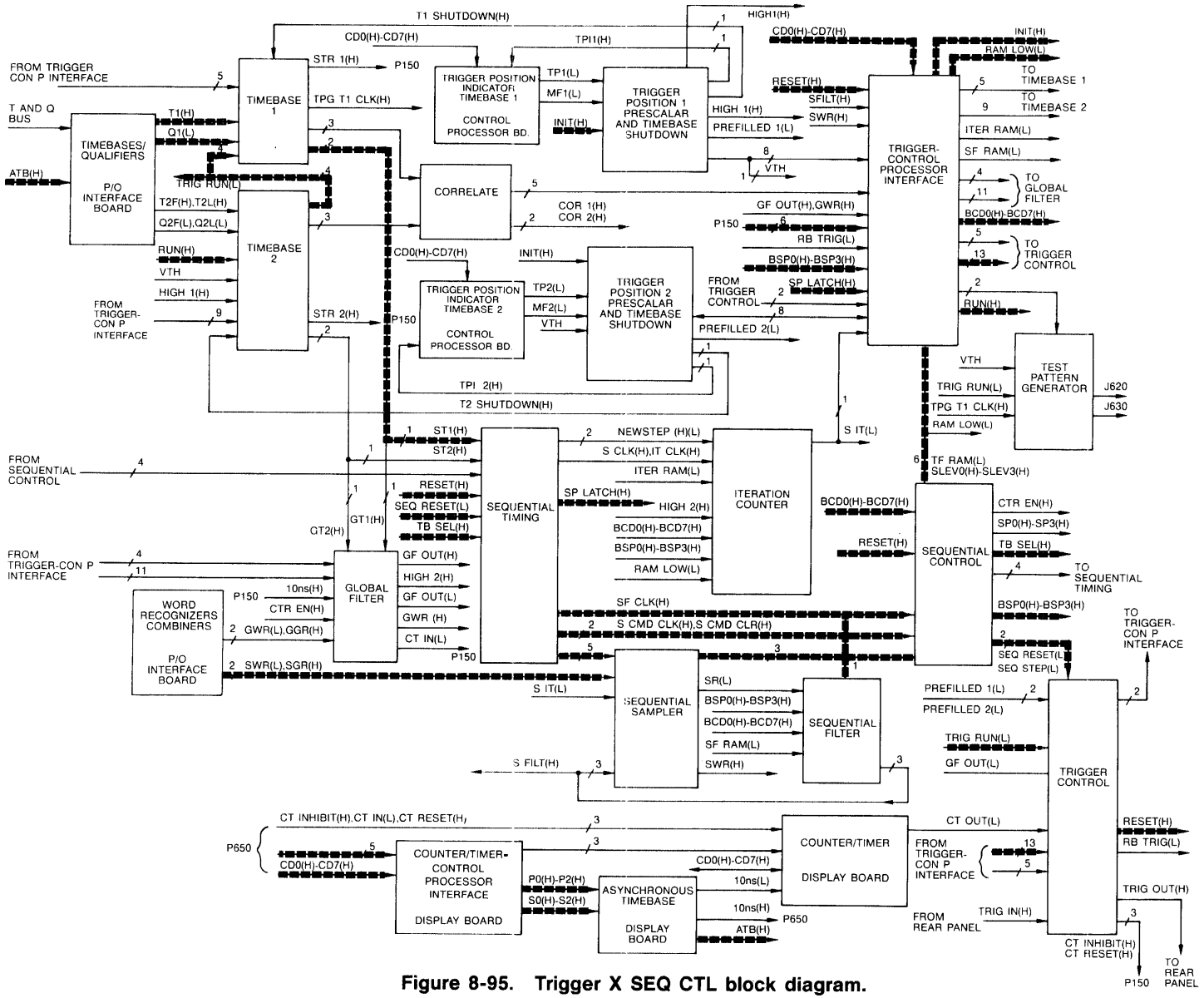

Figure 8-95. Trigger X SEQ CTL block diagram.

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TRIGGER BOARD – COMPONENT LOCATION

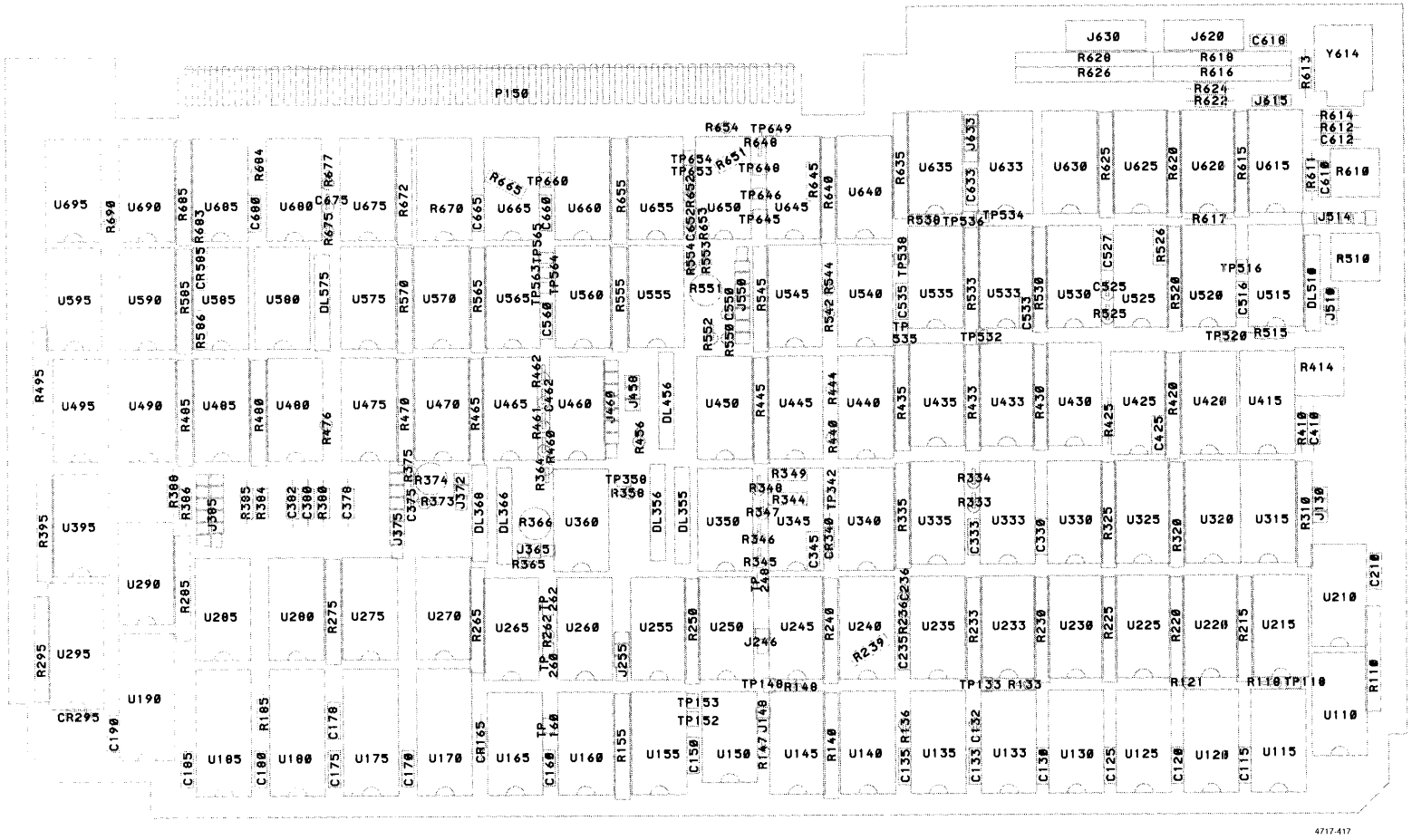

Figure 8-96. Trigger Board component location.

module: TRIGGER
area: X SEQ CTL

X SEQ CTL AREA – CIRCUIT OVERVIEW

The pattern-shaded signal lines on the timing block diagram indicate circuitry used during diagnostic testing. Only the circuitry that is being exercised for the first time during diagnostic testing is shown. Circuitry exercised by other diagnostic tests are shown in their respective block diagrams.

The circuitry tested in this extended sequential control circuitry is basically the same as that tested in the Area 1 Sequential Control tests. Since the theory overview for these areas is lengthy, the descriptions are not repeated here. For circuit descriptions, refer to either the Area 1 circuit overview or the appropriate theory discussion in the *Theory of Operation* section.

X SEQ CTL AREA – TEST DESCRIPTION

The extended sequential control test verifies the ability of the Sequential Control circuit to trigger when the event is false for each stack level. Every sequence level is programmed to step on the occurrence of an event being false. The sequence command Trigger On Event False is programmed into the last sequence level, and the sequence pointer is stepped until a trigger occurs.

The remaining sequence levels are checked using this same procedure.

6A11 Error Index

Explanation: A trigger did not occur; the Actual data is 02_{hex}.

6A11

Probable Cause	Action
The Sequential Control RAM, A14U330, may be defective.	Verify that A14U330-2 and -15 are low. Suspect A14U430 and U433.

module: TRIGGER
area: ATB MANUAL

TRIGGER ATB MANUAL TEST DESCRIPTION

The Asynchronous Timebase (ATB) manual test consists of two routines that help the technician troubleshoot the 1240 trigger circuits. Routine 1, the Decade Divider Exerciser, allows the user to select between the eight different divide rates available at the output of the Decade Divider Multiplexer, A11U570. Routine 2, the ATB Base Rate Exerciser, allows the user to select between the five different clocks available at the output of the Base Rate Multiplexer, A11U465.

ROUTINE 1 DESCRIPTION

The Decade Divider Exerciser routine allows the user to select between the eight different divide rates available at the output of the Decade Divider Multiplexer, A11U570. The selected divide rate is found on A11U570-15 or on A11J462-11. The Base Rate Multiplexer, A11U465, is programmed to select the 10 ns clock; each divide rate is a derivative of this clock.

The eight divide rates selectable through A11U570 are listed below with their respective output cycle times. Test points to verify these ATB outputs are A14J630-1, A14J620-1, and A14TP653.

- 1 (10 ns)
- 10 (100 ns)
- 10^2 (1 μs)
- 10^3 (10 μs)
- 10^4 (100 μs)
- 10^5 (1 ms)
- 10^6 (10 ms)
- 10^7 (100 ms)

ROUTINE 2 DESCRIPTION

The Asynchronous Timebase (ATB) Base Rate Exerciser, allows the user to select between the five different clocks available at the output of the Base Rate Multiplexer, A11U465. The selected clock rate is available on A11U465-15 and A11J560-2.

The five clock rates selectable through A11U465 are listed below.

- 10 ns
- 20 ns
- 50 ns
- 100 ns
- STEP

When the user selects the Base Rate Manual test (routine 2) and presses the start key, the clock rate selected is 1 (10 ns). To select any of the remaining clock rates, use the SCROLL knob or the ↑ and ↓ Select keys. To exit the test, press the STOP key.

7XXX 9-CHANNEL ACQUISITION ERROR INDEXES

Error Index	Area Name	Area Number
71XX	THRESHOLD	AREA 1
72XX	ACQ RAM	AREA 2
73XX	MAP	AREA 3
74XX	FEH	AREA 4
75XX	GWR/GGR	AREA 5
76XX	SWR/SGR	AREA 6
77XX	X ACQ RAM	AREA 7
78XX	CHAINING	AREA 8
79XX	TIMING	AREA 9

9-CHANNEL ACQUISITION MANUAL TEST

Module	Area	Routine	Description
1240D1	CAL ACQ9	1	Calibrate Threshold

1240D1 9-CHANNEL BLOCK DIAGRAM
THRESHOLD – AREA 1

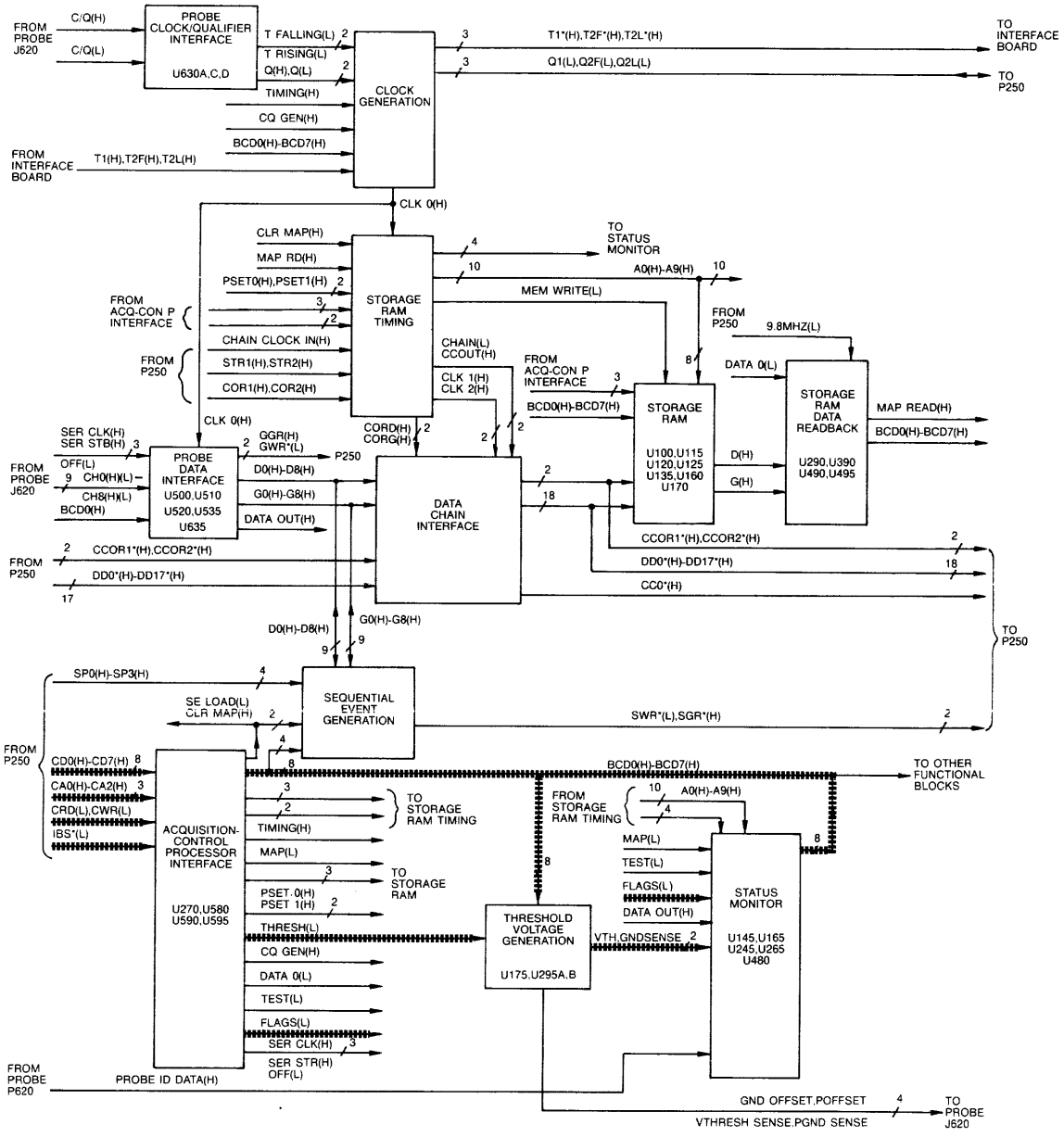

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Figure 8-97. 9-Channel THRESHOLD block diagram.

1240D1 9-CHANNEL ACQUISITION BOARD – COMPONENT LOCATION

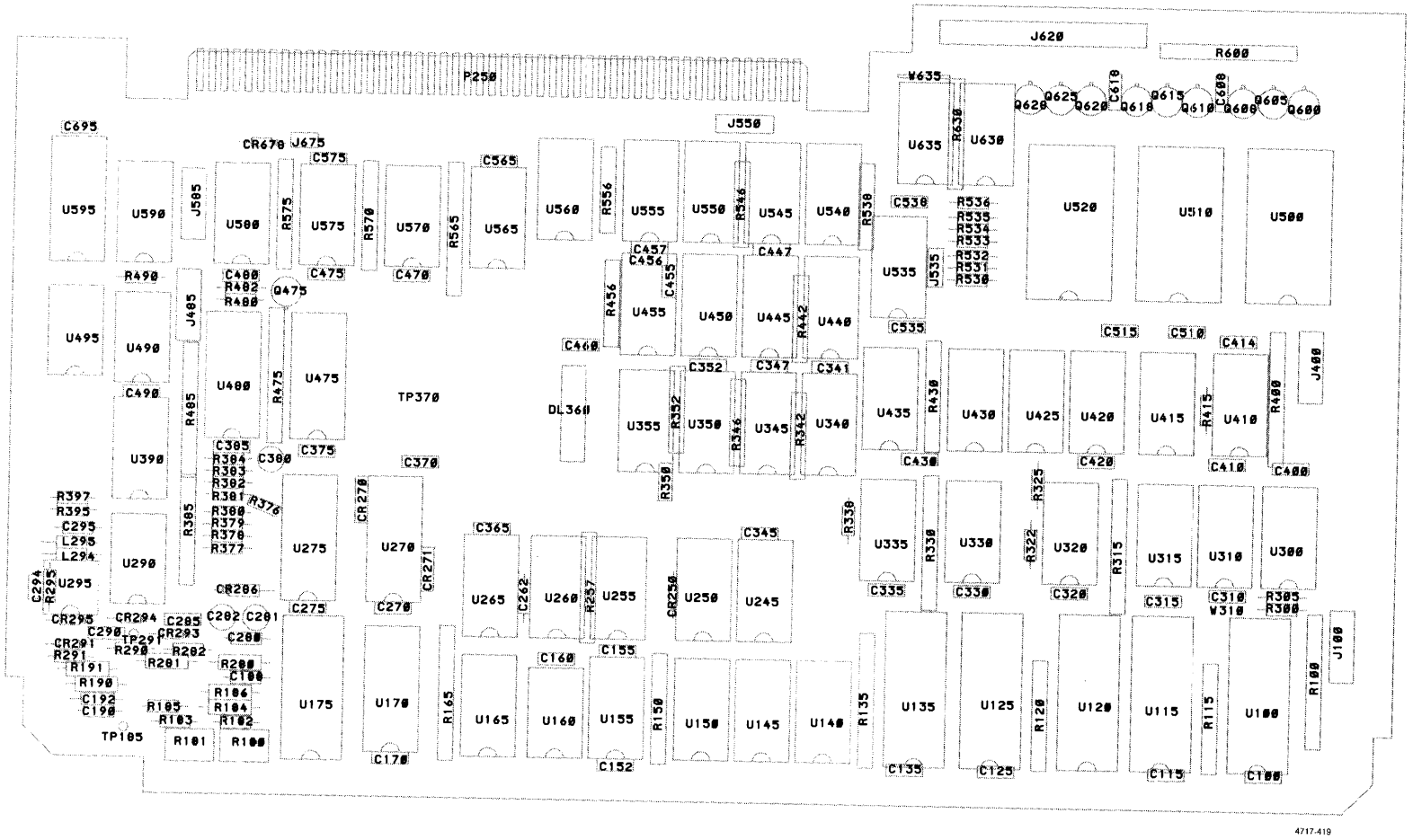


Figure 8-98. 9-Channel Acquisition Board component location.

module: 1240D1-X
area: THRESHOLD

THRESHOLD AREA – CIRCUIT OVERVIEW

The pattern-shaded signal lines on the threshold block diagram indicate circuitry used during diagnostic testing. Only the circuitry that is being exercised for the first time during diagnostic testing is shown. Circuitry exercised by other diagnostic tests are shown in their respective block diagrams.

The Control Processor links its CD data bus to the 9-Channel Acquisition's BCD data bus through the Acquisition-Control Processor Interface. The Control Processor uses this link for loading a user-specified voltage level into the Threshold Voltage Generation circuitry. Here, the voltage level information is converted into a probe threshold voltage for the acquisition probe.

A15U595 is a bidirectional buffer that gates the Control Processor's CD data onto the acquisition card's BCD data bus. A15U580 decodes the THRESH(L) signal from Control Processor address and control lines. This is the load enable signal used during write operations to the Threshold Voltage Generation circuitry.

The digital-to-analog converter (DAC), A15U175, latches and translates the data on BCD0(H)-BCD7(H). Operational amplifiers A15U295A and B produce the probe threshold voltages. Each bit change produces a 50 mV threshold voltage change, with a total range from +6.35 volts to – 6.35 volts.

Comparator A15U165, monitoring the GND SENSE and VTH lines, serves as a zero volt crossing detector. The comparator outputs a signal on the BCD0(H) line that indicates when the threshold voltage has reached a 0 volt level. This signal, read back by the Control Processor, is used during the diagnostic testing of the threshold circuitry.

THRESHOLD AREA – TEST DESCRIPTION

This test checks the digital-to-analog converter (DAC) that is used to produce the 9-channel acquisition probe's threshold voltages. The test writes values 01_{hex} through FF_{hex} to the DAC A15U175 while monitoring the BCD0(H) line from comparator A15U165. When the DAC reaches the zero crossing point, comparator U165 switches its output polarity. The BCD0(H) line reflects this polarity change, thereby indicating to the diagnostics that the DAC output can be set to both positive and negative threshold values.

7111

7111 Error Index

Explanation: The comparator, A15U165, indicated that the DAC output was above 0 volts when it should have been below 0 volts.

Probable Cause	Action
Bad DAC A15U175.	While looping on this test, connect a test oscilloscope probe to A15TP185 (ground to A15TP291). The waveform observed should be a sawtooth ramp from −6.35 V up to +6.35 V.
Bad comparator A15U165.	While looping on this test, connect a test oscilloscope probe to A15U165-3 (ground to A15TP291). The voltage output at pin 3 should change when the DAC output crosses 0 volts.

7112 Error Index

Explanation: The comparator, A15U165, indicated that the DAC output was below 0 volts when it should have been above 0 volts.

Probable Cause	Action
Bad DAC A15U175.	While looping on this test, connect a test oscilloscope probe to A15TP185 (ground to A15TP291). The waveform observed should be a sawtooth ramp from −6.35 V up to +6.35 V.
Bad comparator A15U165.	While looping on this test, connect a test oscilloscope probe to A15U165-3 (ground to A15TP291). The voltage output at pin 3 should change when the DAC output crosses 0 volts.

1240D1 9-CHANNEL BLOCK DIAGRAM
ACQ RAM – AREA 2

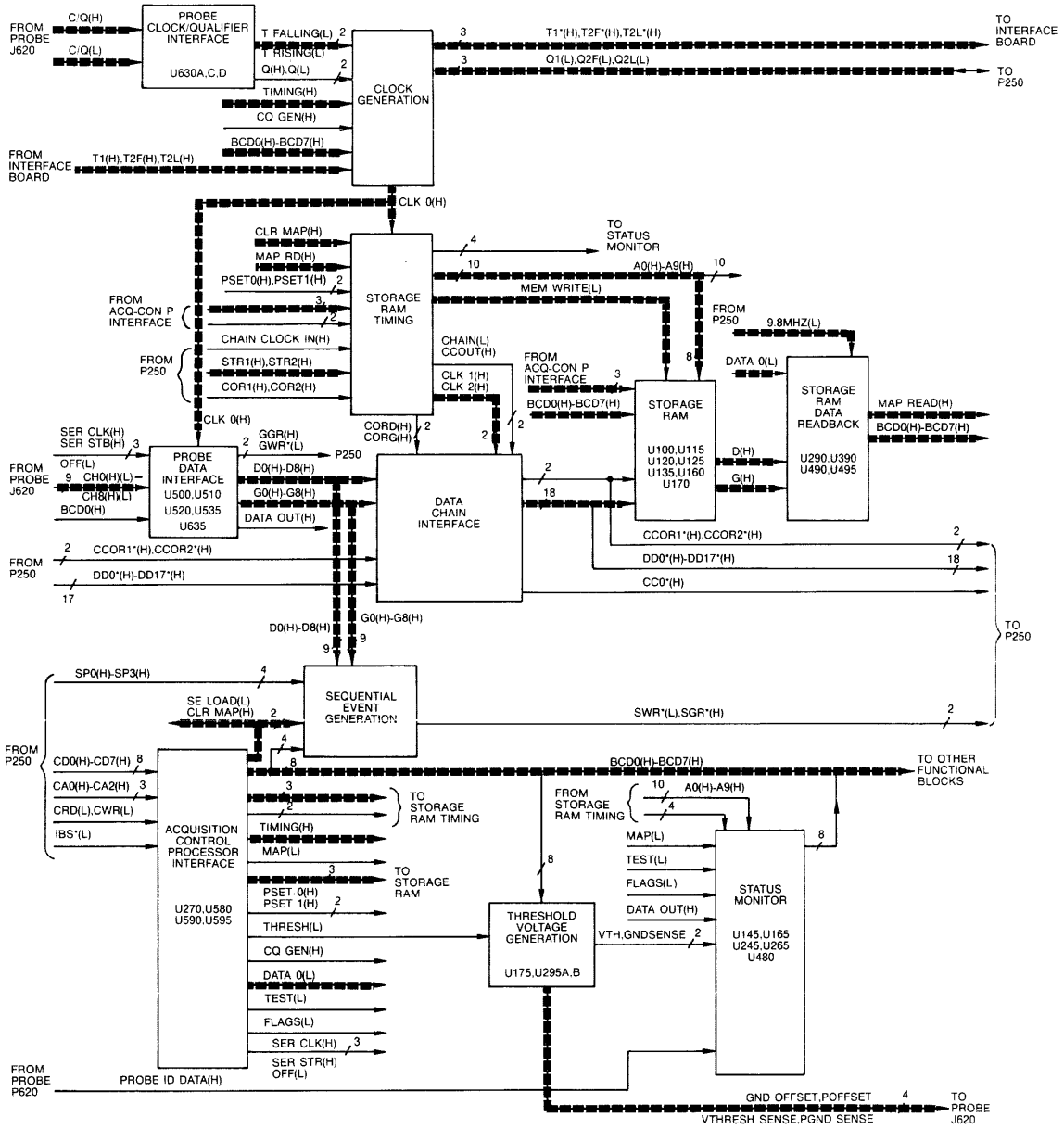


Figure 8-99. 9-Channel ACQ RAM block diagram.

1240D1 9-CHANNEL ACQUISITION BOARD – COMPONENT LOCATION

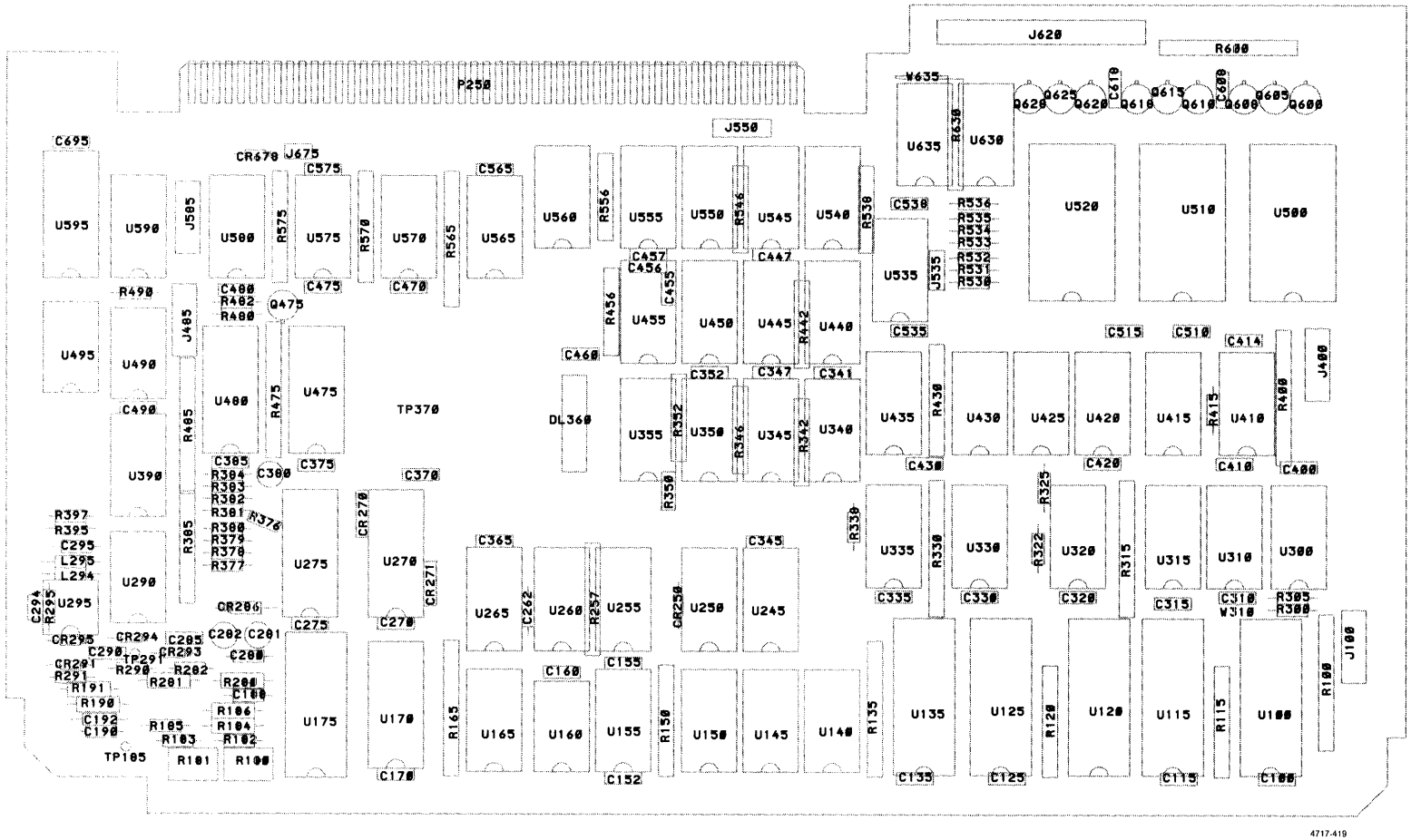


Figure 8-100. 9-Channel Acquisition Board component location.

module: 1240D1-X
area: ACQ RAM

ACQ RAM AREA – CIRCUIT OVERVIEW

The pattern-shaded signal lines on the acquisition RAM block diagram indicate circuitry used during diagnostic testing. Only the circuitry that is being exercised for the first time during diagnostic testing is shown. Circuitry exercised by other diagnostic tests are shown in their respective block diagrams. Most of the 9-channel's function blocks are required to support the storing of data into acquisition RAM.

The Probe Data Interface accepts differential ECL-level channels CH0(H)(L)-CH8(H)(L). The CLK 0(H) signal from the Clock Generation circuitry clocks the data on these lines into the Front End Hybrids (FEHs) A15U520, U510, and U500. The latched data is sent on D0(H)-D8(H) and G0(H)-G8(H) to the Sequential Event Generation circuitry and the Data Chain Interface.

The Sequential Event Generation circuitry uses sequential event RAMs for storage of up to 14 different event recognition patterns. The incoming probe data and glitch information from the Probe Data Interface is compared to the previously stored patterns and, when a match is made, the appropriate data or glitch recognizer signal is generated.

The Data Chain Interface consists of both probe and chain data latches. The probe data latches A15U320, U310, U335, and U330 accept data on the D0(H)-D8(H) and G0(H)-G8(H) signal lines from the Probe Data Interface. The chain data latches are used during chaining of data from one card to the next. The Storage RAM Timing circuitry produces the CLK 1(H) and CLK 2(H) signals that clock the data into the probe data latches. The CLK 1(H) signal latches in the data information, and CLK 2(H) latches in data or glitch information. Output data from these latches is available for either the Storage RAMs or the data chain bus, if chaining is in effect.

The Storage RAM Timing circuitry generates timing and control signals used during the storage of probe data into the storage RAMs. The circuitry comprised of A15DL360, U345B, U350B and C, and U355 A and B, generates write pulses to the storage RAMs at the wire OR on the output of U350C. The memory address pointer circuitry, consisting of counters A15U150 and U250, produce an eight-bit count on address lines A0(H)-A7(H). These address lines are used when accessing the storage RAMs and also serve as a memory address pointer (MAP) value used by the Control Processor when reconstructing data for display.

The Storage RAMs are 256 x 4-bit ECL RAMs that provide temporary buffer storage for data coming from the probe, or data being chained from a previous card. When the Control Processor reads data out of the Storage RAMs, it accesses one 256 x 2-bit block at a time. The serial ECL-level data is converted to TTL-level data by the high-speed comparators A15U160A and B. The serial data is then converted into parallel data by the Storage RAM Data Readback circuitry A15U390, U490, and U495.

ACQ RAM AREA – TEST DESCRIPTION

This test provides a functional check of the acquisition RAM circuitry. The test, run at processor speed, was not designed to isolate specific acquisition failures. Moreover, the test checks the operational status of the acquisition circuitry as a system. Other acquisition circuitry checks may be performed with the 9-Channel's X ACQ RAM (area 7) tests. The test requires that an input probe be used to connect the 9-Channel Acquisition card to the Test Pattern Generator (TPG).

Prior to testing, the Sequential Event RAM buffers are cleared to prevent unwanted bit patterns from affecting the test. First, the test determines if the acquisition probe is connected to the acquisition card. If the probe is not connected, the test reports a failure and the test is aborted. The acquisition card is programmed to acquire data synchronously and to use the AT2LF(L) signal as the source for acquisition clocks. The TPG is programmed to use the processor-stepped T1 clock. The TPG and the acquisition RAMs are clocked 512 times by the T1 clock from the asynchronous timebase. Data stored in acquisition RAM is then checked to determine if it is correct. Failures detected during the diagnostics are reported on the 1240 display screen.

7211 Error Index

Explanation: The test failed to detect the acquisition probe.

Probable Cause	Action
The acquisition probe is improperly connected or bad.	Examine the expected and actual results. If the expected data is 00 and the actual data is 40, then suspect the probe.
Defective input or output latch.	While looping on this test, use a test oscilloscope to check A15U270-6 for serial data being output. Check A15U590-11 for a clock output to the probe. Check A15U480-18 for input probe I.D. serial data.

7212 Error Index

Explanation: The acquired data did not match the expected data.

Probable Cause	Action
Defective acquisition probe.	Replace probe and run test again.
Timing malfunction; incorrect write clock to the acquisition memory.	With routine stopped on failure, check for a logic low on A15U270-16 and a logic high on U590-9. While looping on the test, check for clock pulses on A15J550-4, U540-14, U140-7, and U455-2. Check A15U540-10 for a low. If U540-10 is low and no clock clock is present on U540-14, suspect U630, U440, the probe, or the TPG. Finally, verify that the Trigger module did not fail with error index 6113. If it did, suspect the T1 clock generation circuitry.
Defective data or glitch probe data latches A15U310, U320, U330, or U335.	While looping on this routine, use a logic analyzer and the TPG output pattern (listed in the *Operating Information* section) to verify the outputs of the latches. Latches A15U320 and 310 work as a pair, as do latches U330 and U335. The data being output alternates between the two pair of latches.
The Memory Address Pointer (MAP) does not increment correctly.	While looping on this routine, Use a logic analyzer to observe the output of the MAP. Connect the analyzer to A15U150 and U250 on pins 3, 2, 15, and 14. The values on these pins should increment from 000_{hex} to $0FF_{hex}$.
Defective Front End Hybrids (FEHs).	Determine which hybrid is bad by comparing the expected and actual data. If the error is in the lower three bits, replace A15U520. If it is in the middle three bits, replace A15U510. If found in the upper three bits, replace A15U500.
Defective Test Pattern Generator (TPG).	While looping on this test, verify the TPG patterns output on J630 with a logic analyzer.

1240D1 9-CHANNEL BLOCK DIAGRAM
MAP – AREA 3

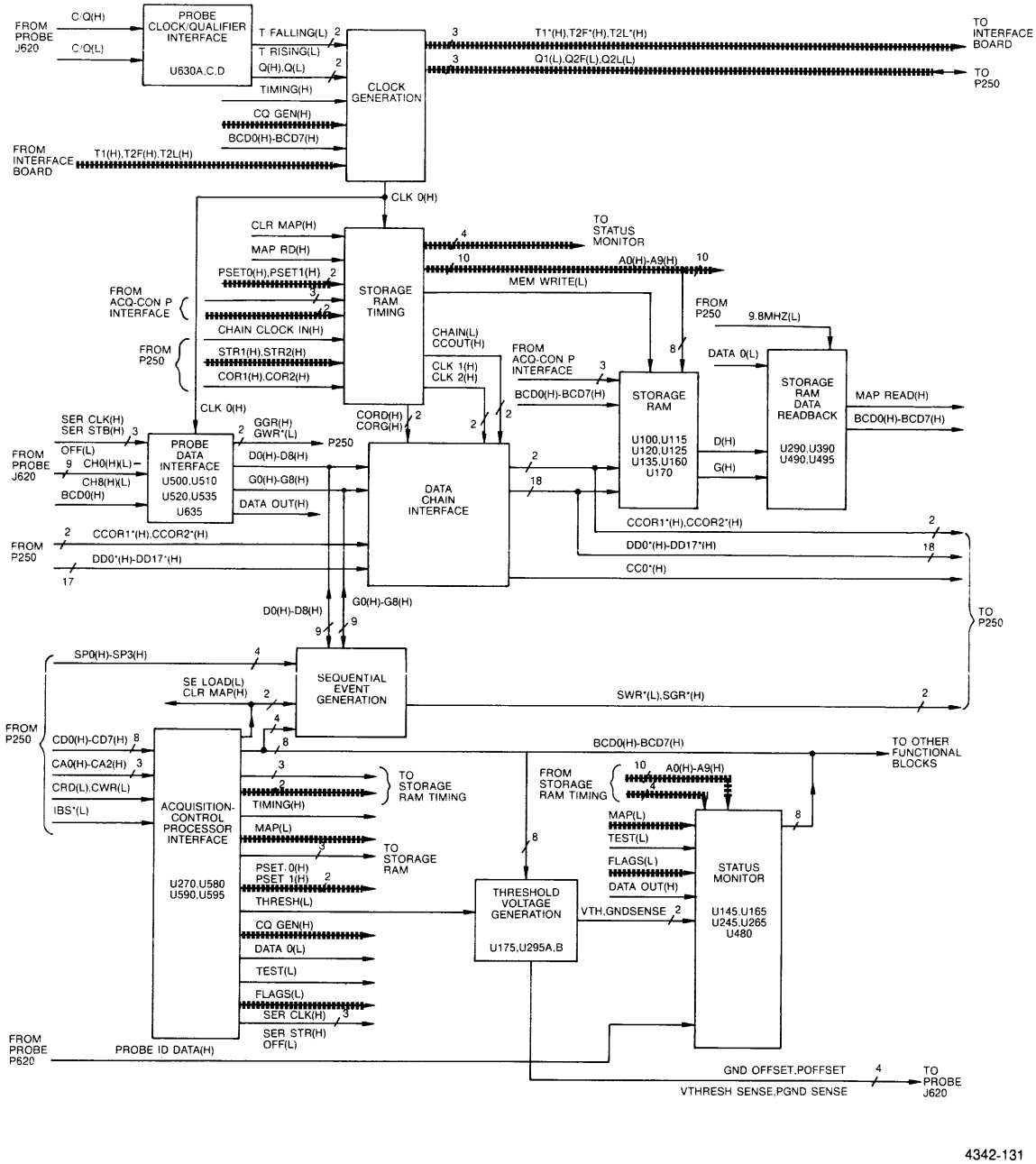


Figure 8-101. 9-Channel MAP block diagram.

1240D1 9-CHANNEL ACQUISITION BOARD – COMPONENT LOCATION

Figure 8-102. 9-Channel Acquisition Board component location.

module: 1240D1-X
area: MAP

MAP AREA – CIRCUIT OVERVIEW

The pattern-shaded signal lines on the Memory Address Pointer (MAP) block diagram indicate circuitry used during diagnostic testing. Only the circuitry that is being exercised for the first time during diagnostic testing is shown. Circuitry exercised by other diagnostic tests are shown in their respective block diagrams.

The MAP circuitry generates the addresses used to access the storage RAMs. These addresses also serve as a memory address pointer value used by the Control Processor when reconstructing data for display. The MAP circuitry, consisting of counters A15U150 and U250, is clocked by the MAP READ(H) signal (from the Storage RAM Data Readback circuitry). Counter A15U390 supplies the four count MAP READ(H) signal for the memory address pointer circuitry and the readback shift registers. Each count loads a bit into the shift register and increments the MAP counter. The MAP counters produce an eight-bit count on address lines A0(H)-A7(H). The terminal count from A15U150 and U250 enable a third counter, A15U255. As a count is produced on address lines A8(H) and A9(H), a comparison to the memory chain depth indicators PSET 0(H) and PSET 1(H) is made by A15U155A. If the depth indicators are set at 00 (no cards chained), the logic causes the counter A15U255 to output an active FO(H) Filled Once signal when the first acquisition card is filled. If the depth indicators were set at 11 (binary code indicating four cards chained), the FO(H) signal would become active on this card after all cards in the chain are filled.

The Control Processor reads the MAP count on the A0(H)-A7(H) lines through the Status Monitor.

MAP AREA – TEST DESCRIPTION

The MAP area tests consist of four routines. Routine 1 verifies correct operation of address bits 0 through 7 in the MAP circuit. Routine 2 verifies the operation of the NOT NO CLK(L) and SLOW CLK(H) signals, as well as the ability of the MAP circuit to be incremented by the T1 clock in the glitch store mode. Routine 3 verifies the ability of the MAP circuit to be incremented by the asynchronous timebase (generated on the T1 clock line) in the data store mode. Routine 4 checks MAP address bits 0 through 9 by verifying the ability of the MAP to address the maximum memory depth of 2048 words. The test requires that an input probe be used to connect the 9-Channel Acquisition card to the Test Pattern Generator (TPG).

ROUTINE 1 DESCRIPTION

This test verifies correct operation of address bits 0 through 7 in the MAP circuit. This test begins by clearing the MAP counters and reading to verify the counters are reset. A15U390 is loaded and the MAP READ(H) line increments the MAP count by four. The MAP count is read once again to verify that it was incremented. This increment/read sequence is repeated 64 times to verify address bits 0 through 7. (Since bits 0 and 1 will always contain the same value, they are not as completely tested as the other address bits). If a failure is detected, the test is aborted and the failure is reported.

7311 Error Index

Explanation: The MAP count was not 0 after being reset.

Probable Cause	Action
Defective reset path to the MAP circuit.	While looping on this routine, check for a low-going pulse on A15U150 and U250-12. If not present, check for a signal on address decoder A15U590-7 and buffer A15U290-10.
The test was unable to correctly read the MAP count.	Use a logic analyzer to verify that the count from the MAP circuit is reaching the readback buffers A15U145 and U245. Also verify the read strobe on pin 4 of the readback buffers. If not present, check for signal on address decoder A15U590-13.

7312 Error Index

Explanation: The MAP did not increment correctly.

Probable Cause	Action
No clock to the MAP circuit.	While looping on this test, check for a positive-going clock signal on pin 13 of A15U150 and U250. If not present, check for signal on A15U350-9 and U390-14. If still not present, check A15U390-2 for the 9.8 MHz clock and check U390-9 for a load strobe. If necessary, use a logic analyzer to verify the MAP circuit count operation on A15U150 and U250.

ROUTINE 2 DESCRIPTION

This routine first verifies the operation of the NOT NO CLK(L) and SLOW CLK(H) signals, then checks the ability of the MAP circuit to be incremented by the T1 clock in the glitch store mode. The processor generates the storage clock from the asynchronous timebase on the T1 clock line. In this test, all Memory Address Pointer (MAP) bits are, at minimum, functionally verified.

The test begins by clearing the MAP counters, then reading the MAP count to ensure that the count is set at 0. Next, the processor reads the condition of the slow clock monitoring circuitry, A15U260A and C, with the FLAGS(L) signal to verify that the SLOW CLK(H) line is inactive low. The NOT NO CLK(L) line is also read to verify that it is active low. Reading the status of the SLOW CLK(H) line causes the slow clock bit to be set low and the not no clock bit to be set high. The test reads both bits to ensure they are in the correct states. Now, a clock is generated on the T1 clock line, causing the SLOW CLK(H) signal to go active high and the NOT NO CLK(L) line to go active low. The processor reads the status of these bits to determine if the outputs changed. Finally, the MAP is incremented by the T1 clock to $0FF_{hex}$. The test reads the MAP count value after each increment to determine if the MAP circuit counted correctly.

7321 Error Index

Explanation: The MAP count was not 0 after being reset.

Probable Cause	Action
Defective reset path to the MAP circuit.	While looping on this routine, check for a high-going pulse on A15U150 and U250-12. If not present, check for a signal on address decoder A15U590-7 and buffer A15U290-10.
The test was unable to correctly read the MAP count.	Use a logic analyzer to verify that the count from the MAP circuit is reaching the readback buffers A15U145 and U245. Also, verify the read strobe on pin 4 of the readback buffers. If not present, check for signal on address decoder A15U590-13.

7321
7322

7322 Error Index

Explanation: The not no clock and slow clock status bits were not at the correct logic levels when read back.

Probable Cause	Action
If the actual data was 40_{hex} or $C0_{hex}$, the no clock bit may not have been reset.	While looping on this test, check for a reset pulse on A15U340-4 and 13. When the routine stops on the failure, verify a logic high on A15U270-2.
If the actual data was 80_{hex} or $C0_{hex}$, the slow clock bit may not have been reset.	While looping on this test, check for a reset pulse on A15U260-10. If not present, check A15U590-12. Also check A15C262 and R257.

7323 Error Index

Explanation: The not no clock and slow clock status bits were not at the correct logic levels when read back.

Probable Cause	Action
If the actual data was 00_{hex} or 80_{hex}, the no clock bit may not have been set.	While looping on this test, check for a set pulse on A15U340-5 and 12. If not present, check A15U290-12 and U590-9. With the routine stopped on the failure, check A15U340-4 and 13 for logic lows. If not, check A15U260-2 for a low and U590-10 for a high.
If the actual data was $C0_{hex}$ or 80_{hex}, the slow clock bit may not have been reset.	While looping on this test, check for a reset pulse on A15U260-10. If not present, check A15U590-12. Also, check A15C262 and R257.

7324 Error Index

Explanation: The not no clock and slow clock status bits were not at the correct logic levels after the T1 clock was generated.

Probable Cause	Action
If the actual data was 00_{hex} or 40_{hex}, the slow clock bit may not have been set.	While looping on this test, check A15U260-7 for a T1 clock. If not present, check A15U450-11 and U545-6. With the routine stopped on the failure, verify that the T1 clock bus is selected; A15U450-13 should be at a logic low. Also, verify that the Q1 qualifier at A15U545-7 is low.
If the actual data was $C0_{hex}$ or 40_{hex}, the not no clock bit may not have been reset.	While looping on this test, check A15U340-9 for a T1 clock. If not present, check A15U450-11 and U545-6. With the routine stooped on the failure, verify that the T1 clock bus is selected; A15U450-13 should be low. Also verify that the Q1 qualifier at A15U545-7 is low.

7325 Error Index

Explanation: The Memory Address Pointer (MAP) circuitry does not increment correctly in the glitch store mode.

Probable Cause	Action
Defective glitch mode control circuitry.	While looping on this test, examine the clock selector circuit path to A15U455-7 and 9. Check for clock pulse on A15U455-2. Check for a set pulse on A15U355-12. Also, verify that A15U350-13 is asserted low.

ROUTINE 3 DESCRIPTION

This routine verifies the ability of the MAP circuit to be incremented by the T1 clock in the data store mode. The processor generates a storage clock from the asynchronous timebase on the T1 clock line. In the data store mode, the MAP clock is generated at half the rate of the T1 clock.

The test begins by clearing the MAP counters, then reading the MAP count to ensure that the count is set at 0. Next, the processor increments the MAP circuit and reads the count value to verify the counters incremented correctly. After the MAP has been incremented to $0FF_{hex}$ (the MAP is read after each increment), another T1 clock is generated to set the HALF BYTE (H) line active high and the FO(H) filled once bit low. The processor reads the condition of the half byte bit to verify the active high logic level. Now, an additional T1 clock is generated to reset the HALF BYTE (H) line low and set the FO(H) filled once signal line active high.

7331 Error Index

7325
7331

Explanation: The MAP count was not 0 after being reset.

Probable Cause	Action
Defective reset path to the MAP circuit.	While looping on this routine, check for a high-going pulse on A15U150 and U250-12. If not present, check for a signal on address decoder A15U590-7 and buffer A15U290-10.
The test was unable to correctly read the MAP count.	Use a logic analyzer to verify that the count from the MAP circuit is reaching the readback buffers A15U145 and U245. Also, verify the read strobe on pin 4 of the readback buffers. If not present, check for signal on address decoder A15U590-13.

7332 Error Index

Explanation: The MAP did not increment correctly.

Probable Cause	Action
The data store mode was not selected.	With the routine stopped on the failure, verify a logic high on A15U350-7.

7333 Error Index

Explanation: Either the half byte bit or the filled once bit was incorrect.

Probable Cause	Action
If the actual data was 04_{hex} or 00_{hex}, the half byte bit was not high when it should have been.	While looping on this test, check for a logic-high square pulse on A15U355-14.
No clock from the Trigger module through A15U455 to A15U355.	While looping on this test, check for a clock on A15U455-5 and 2, and a clock at U355-11.
If the actual data was $0C_{hex}$ or 00_{hex}, the filled once bit was not low when it should have been.	While looping on this test, check for a logic-low square pulse on A15U255-14. Also check A15U255-13 for a clock.

7334 Error Index

Explanation: Either the half byte bit or the filled once bit was incorrect.

Probable Cause	Action
If the actual data was $0C_{hex}$ or 08_{hex}, the half byte bit was not low when it should have been.	While looping on this test, check for a logic-low square pulse on A15U355-14.
No clock from the Trigger module through A15U455 to A15U355.	While looping on this test, check for a clock on A15U455-5 and 2, and a clock at U355-11.
If the actual data was 00_{hex} or 08_{hex}, the filled once bit was not high when it should have been.	While looping on this test, check for a logic-low square pulse on A15U255-14. Also check A15U255-13 for a clock.
The carry out from the MAP circuit may be defective.	While looping on this test, check for the carry out from A15U150-4 and U250-4. Check the output from A15U140-15, and A15U255-5 and 6 for low-going pulses.

ROUTINE 4 DESCRIPTION

This routine checks Memory Address Pointer (MAP) bits 0 through 9 by verifying the ability of the MAP to address the maximum memory depth of 2048 words. The test acquires the TPG data and compares it to reference TPG data, therefore the test requires that an acquisition probe be connected to the Test Pattern Generator (TPG).

The test begins by interrogating the status of the probe to ensure a probe is connected. If the probe is found to be connected, the test assumes that it is also connected to the TPG. To verify the MAP circuitry, the test manipulates the PSET 0(H) and PSET1 (H) lines. These lines control memory depth (when acquisition cards are chained) to fill the acquisition memory to the maximum depth. By simulating a chained memory condition, all MAP address lines including the A8(H) and A9(H) address bits may be tested.

The T2L clock generated from the TPG clock is used to increment the MAP circuitry. The TPG output clock is sourced by the processor-stepped T1 clock.

MAP address bits A8 and A9 are examined after the MAP has been incremented to the next 256-location block of acquisition memory. As the MAP is incremented through each new block of acquisition memory, the A8(H) and A9(H) lines are checked to verify that they have changed correctly. When all 2048 memory locations have been addressed, the FO(H) filled once signal is checked to verify it is active high.

7341 Error Index

Explanation: The probe status check indicates that there is no probe connected to the acquisition board.

Probable Cause	Action
No probe connected.	Connect the probe to the board under test and to the TPG.
Probe may be defective.	Replace the probe.
The probe's input or output status registers may be defective.	While looping on this test, observe the serial data output to the probe on A15U270-6. Check for the serial data clock on A15U590-11. Check for the incoming serial data on A15U480-18.

7342 Error Index

Explanation: After incrementing the MAP 256 times, MAP address bits 8 and 9 were not correct. A8 should have been high and A9 should have been low. The actual state of bits 8 and 9 can be found as bits 4 and 5 of the Actual Data on the 1240 screen.

Probable Cause	Action
The carry out signal from the least significant 8 bits is defective.	While looping on this test, check for low-going pulses on A15U255-6.
The PSET 0(H) and PSET 1(H) lines were not correct.	While the test is stopped, verify that A15U155-4 and 9 are both high. If not, check A15U270-5 and 19.
Defective MAP counter.	Verify the operation of A15U255. Check the control inputs on pins 5, 6, 11, and 12. Also, check for a clock on pin 13.

7343 Error Index

Explanation: After incrementing the MAP 512 times, MAP address bits 8 and 9 were not correct. A8 should have been low and A9 should have been high. The actual state of bits 8 and 9 can be found as bits 4 and 5 of the Actual Data on the 1240 screen.

Probable Cause	Action
The PSET 0(H) and PSET 1(H) lines were not correct.	While the test is stopped, verify that A15U155-4 and 9 are both high. If not, check A15U270-5 and 19.
Defective MAP counter.	Verify the operation of A15U255. Check the control inputs on pins 5, 6, 11, and 12. Also, check for a clock on pin 13.

7344 Error Index

Explanation: After incrementing the MAP 768 times, MAP address bits 8 and 9 were not correct. A8 should have been high and A9 should have been high. The actual state of bits 8 and 9 can be found as bits 4 and 5 of the Actual Data on the 1240 screen.

Probable Cause	Action
The PSET 0(H) and PSET 1(H) lines were not correct.	While the test is stopped, verify that A15U155-4 and 9 are both high. If not, check A15U270-5 and 19.
Defective MAP counter.	Verify the operation of A15U255. Check the control inputs on pins 5, 6, 11, and 12. Also, check for a clock on pin 13.

7345 Error Index

Explanation: After incrementing the MAP 1023 times, MAP address bits 0 through 7 were not correct. The MAP count should have been $0FF_{hex}$. The actual state of bits 0 through 7 can be found as bits 0 through 7 of the Actual Data on the 1240 screen.

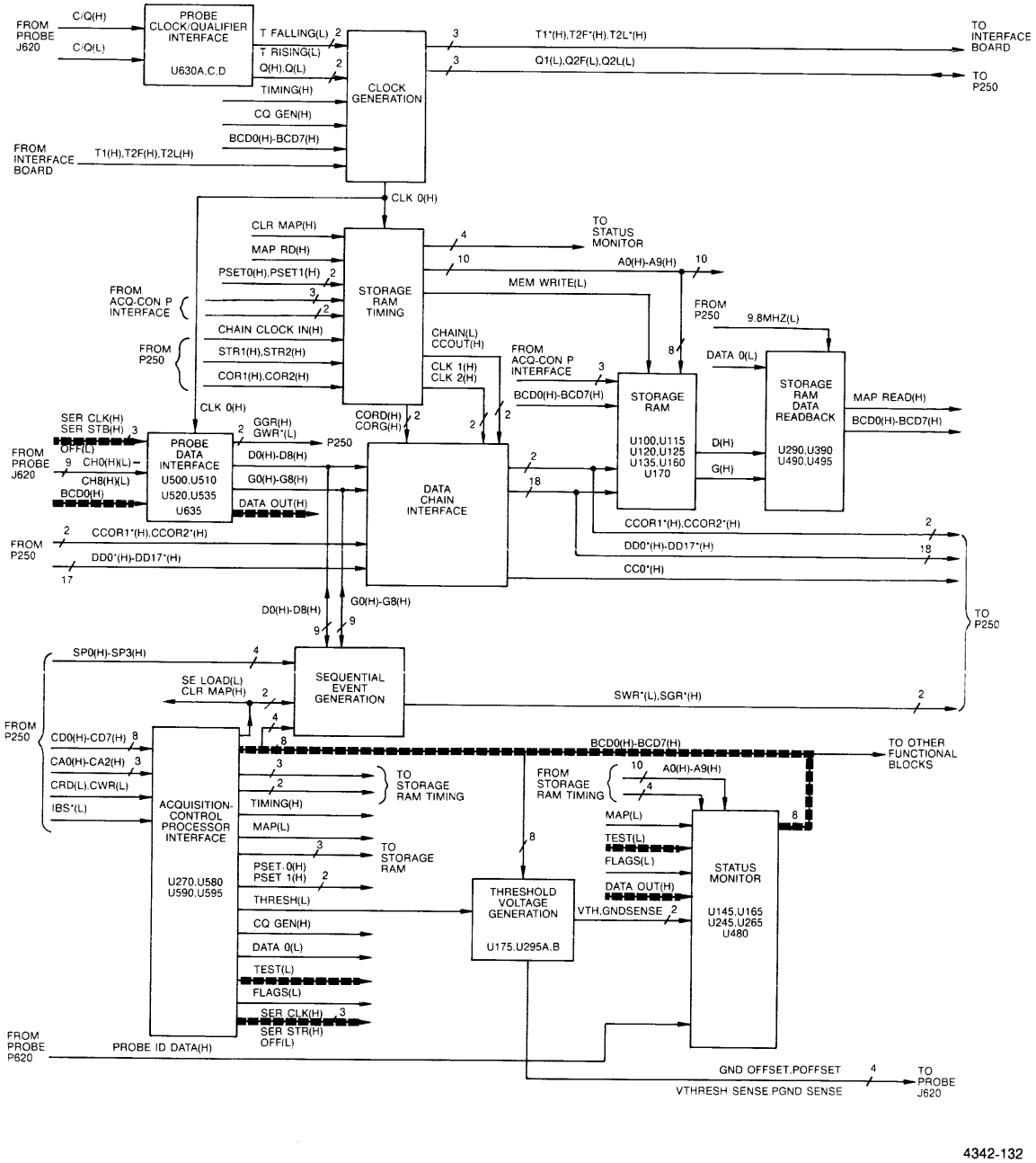
Probable Cause	Action
There is noise on the clock line to the MAP causing extra clocks.	While looping on this test, observe the MAP clock inputs at pin 13 of A15U150 and U250.
Defective MAP counter.	Verify the operation of A15U255. Check the control inputs on pins 5, 6, 11, and 12. Also, check for a clock on pin 13. While looping on this test, observe the count from the MAP circuit with a logic analyzer.

7346 Error Index

Explanation: After incrementing the MAP 1025 times, either the MAP address bits 8 and 9 or the filled once bit was not correct. A8 and A9 should have both been low, and the FO(H) filled once bit should have been high. The actual state of bits 8 and 9 can be found as bits 4 and 5 of the Actual Data on the 1240 screen. The actual state of the filled once bit is Actual Data bit 2.

Probable Cause	Action
Defective MAP counter.	Verify the operation of A15U255. Check the control inputs on pins 5, 6, 11, and 12. Also, check for a clock on pin 13. While looping on this test, observe the count from the MAP circuit with a logic analyzer.

1240D1 9-CHANNEL BLOCK DIAGRAM
FEH – AREA 4



4342-132

Figure 8-103. 9-Channel FEH block diagram.

1240D1 9-CHANNEL ACQUISITION BOARD – COMPONENT LOCATION

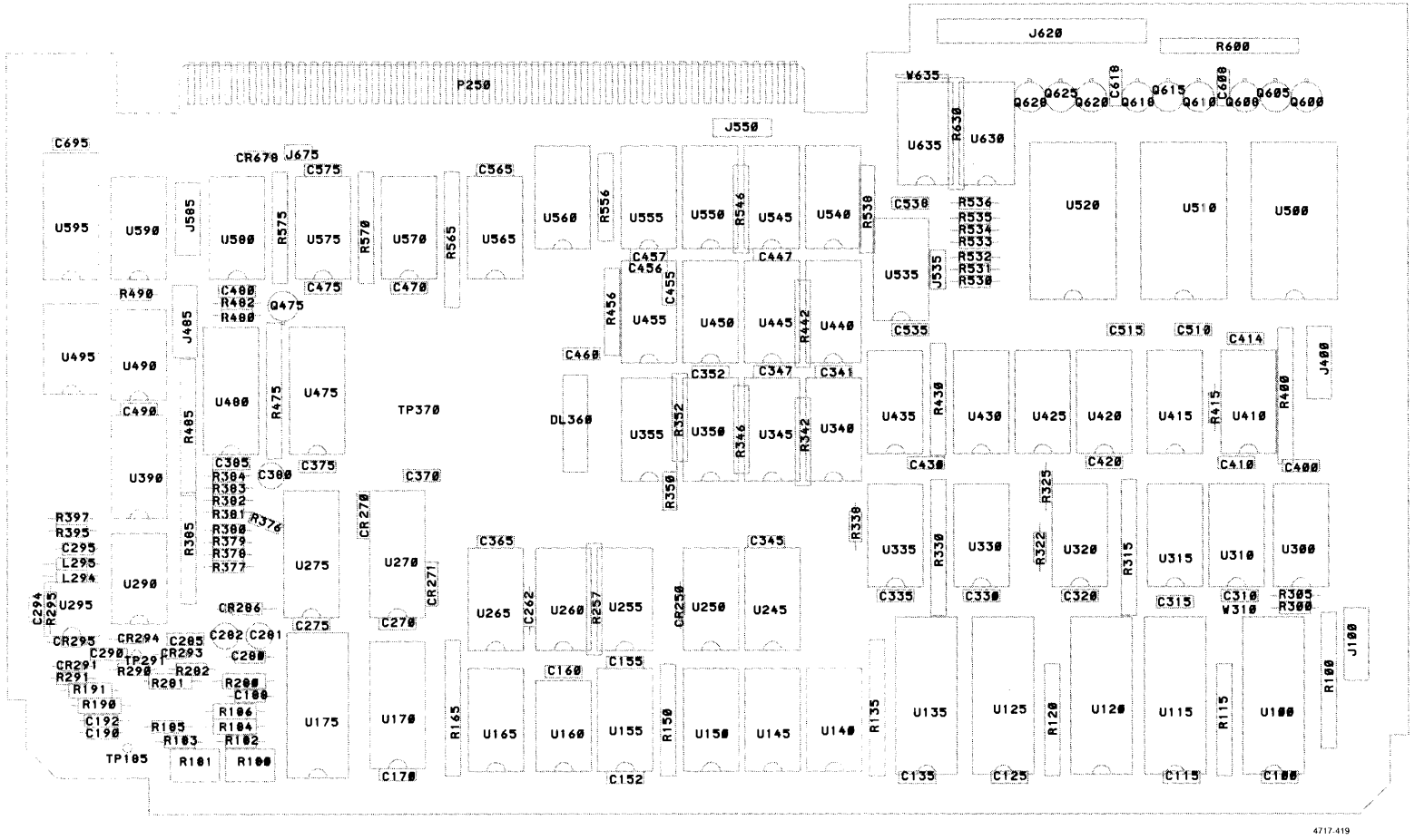


Figure 8-104. 9-Channel Acquisition Board component location.

module: 1240D1-X
area: FEH

FEH (FRONT END HYBRID) AREA – CIRCUIT OVERVIEW

The pattern-shaded signal lines on the Front End Hybrid (FEH) block diagram indicate circuitry used during diagnostic testing. Only the circuitry that is being exercised for the first time during diagnostic testing is shown. Circuitry exercised by other diagnostic tests are shown in their respective block diagrams.

The nine differential ECL-level channels CH0(H)(L)-CH8(H)(L) carry probe data to the FEHs A15U520, U510, and U500. The hybrids provide a latch for probe data, and compare incoming data and glitch information against previously selected event patterns. When a data match occurs, A15U630 outputs the active-low global word recognizer GWR*(L) signal. When a data/glitch acquisition match occurs, both the global word recognizer and global glitch recognizer, GGR(H), outputs go to their active states. The latched data is sent on the D0(H)-D8(H) and G0(H)-G8(H) lines to the Sequential Event Generation circuitry and the Data Chain Interface. Once at the chain interface, the information may be chained to the next acquisition card or sent to the Storage RAMs.

The serial global-event pattern information is loaded on BCD0(H). Each Front End Hybrid (FEH) has 16 internal shift/store control registers that hold the event patterns. After sequentially shifting the global data and glitch recognizer values into the hybrids with the SER CLK(H) signal, the SER STB(H) signal latches the data into the hybrids.

The DATA OUT(H) signal line carries the serial pattern information previously clocked in on the BCD0(H) line. Diagnostics use this read back information to verify the shift/store registers.

FEH (FRONT END HYBRID) AREA – TEST DESCRIPTION

This test verifies that event patterns may successfully be loaded into and read from the 9-channel's FEHs. The test begins by serially loading the three hybrids A15U520, U510, and U500 with a 48-bit pattern. The pattern consists of three 16-bit words $00AA_{hex}$, 0155_{hex}, and $00EB_{hex}$. After loading of the pattern is complete, the bits are serially read out and the 48-bit output pattern is compared to previously loaded input pattern. If a descrepancy between the two sets of data is found, the test is aborted and a failure is reported.

7411 Error Index

Explanation: The first 16-bit pattern was not read back as $00AA_{hex}$.

Probable Cause	Action
No serial clock to one or more of the Front End Hybrids.	While looping on this test, verify that a clock is present on pin 2 of A15U520, U510, and U500. If not present, check A15U580-13.
Defective readback buffer.	While looping on this test, use an oscilloscope to observe the serial data on A15U480-2.
Noise on the serial clock path to the Front End Hybrids.	While looping on this test, use an oscilloscope to observe the serial clock SER CLK(H) on A15J585-3.
Defective Front End Hybrid.	While looping on this test, check pin 3 of A15U500, U510, and U520 for serial data. The hybrid with no output is most likely defective. If necessary, replace each FEH until the test passes.

7412 Error Index

Explanation: The second 16-bit pattern was not read back as 0155_{hex}.

Probable Cause	Action
Noise on the serial clock path to the Front End Hybrids.	While looping on this test, use an oscilloscope to observe the serial clock SER CLK(H) on A15J585-3.
Defective Front End Hybrid.	Replace each FEH until the test passes.

7413 Error Index

Explanation: The third 16-bit pattern was not read back as $00EB_{hex}$.

Probable Cause	Action
Noise on the serial clock path to the Front End Hybrids.	While looping on this test, use an oscilloscope to observe the serial clock SER CLK(H) on A15J585-3.
Defective Front End Hybrid.	Replace each FEH until the test passes.

1240D1 9-CHANNEL BLOCK DIAGRAM
GWR/GGR – AREA 5

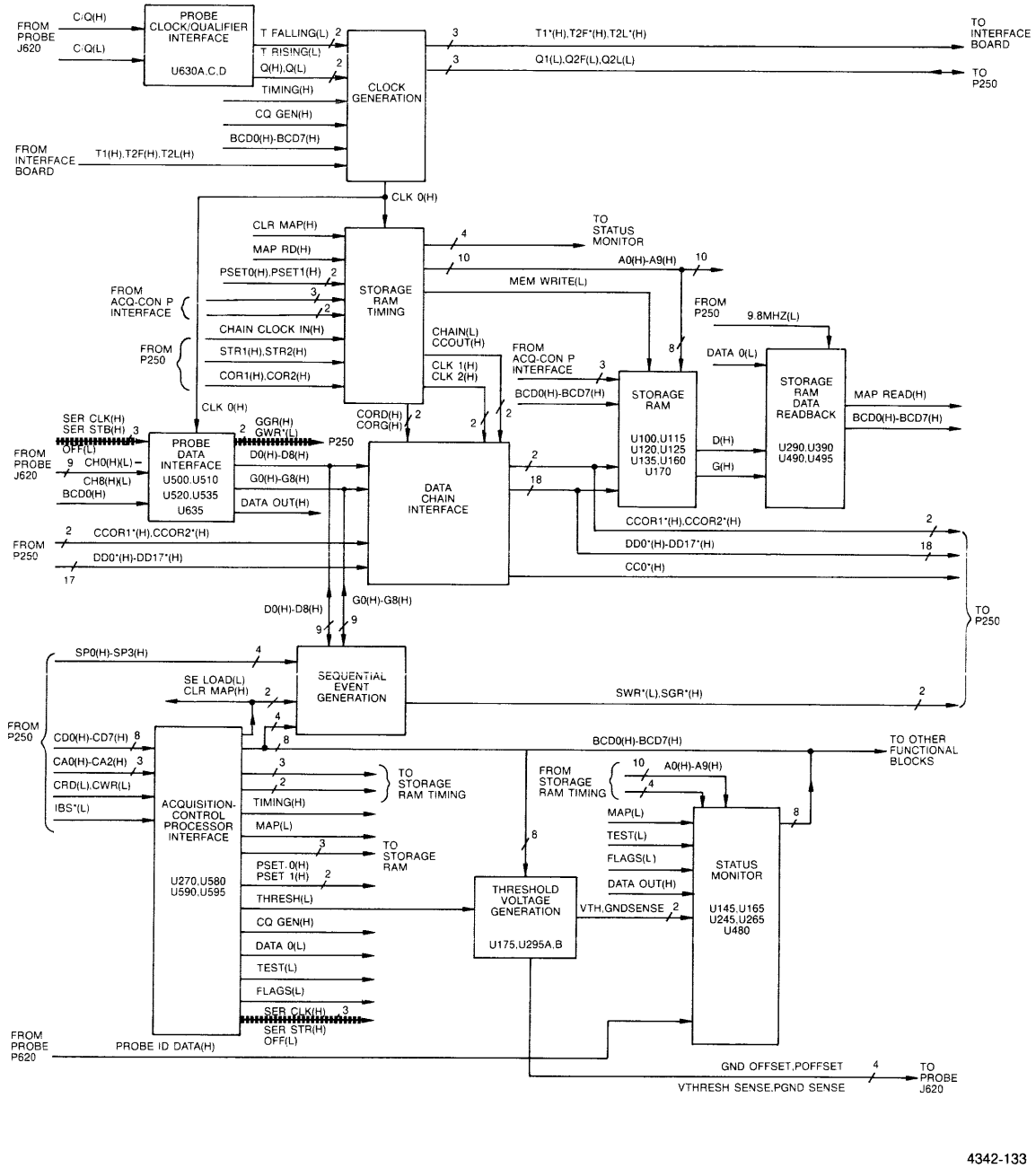


Figure 8-105. 9-Channel GWR/GGR block diagram.

1240D1 9-CHANNEL ACQUISITION BOARD – COMPONENT LOCATION

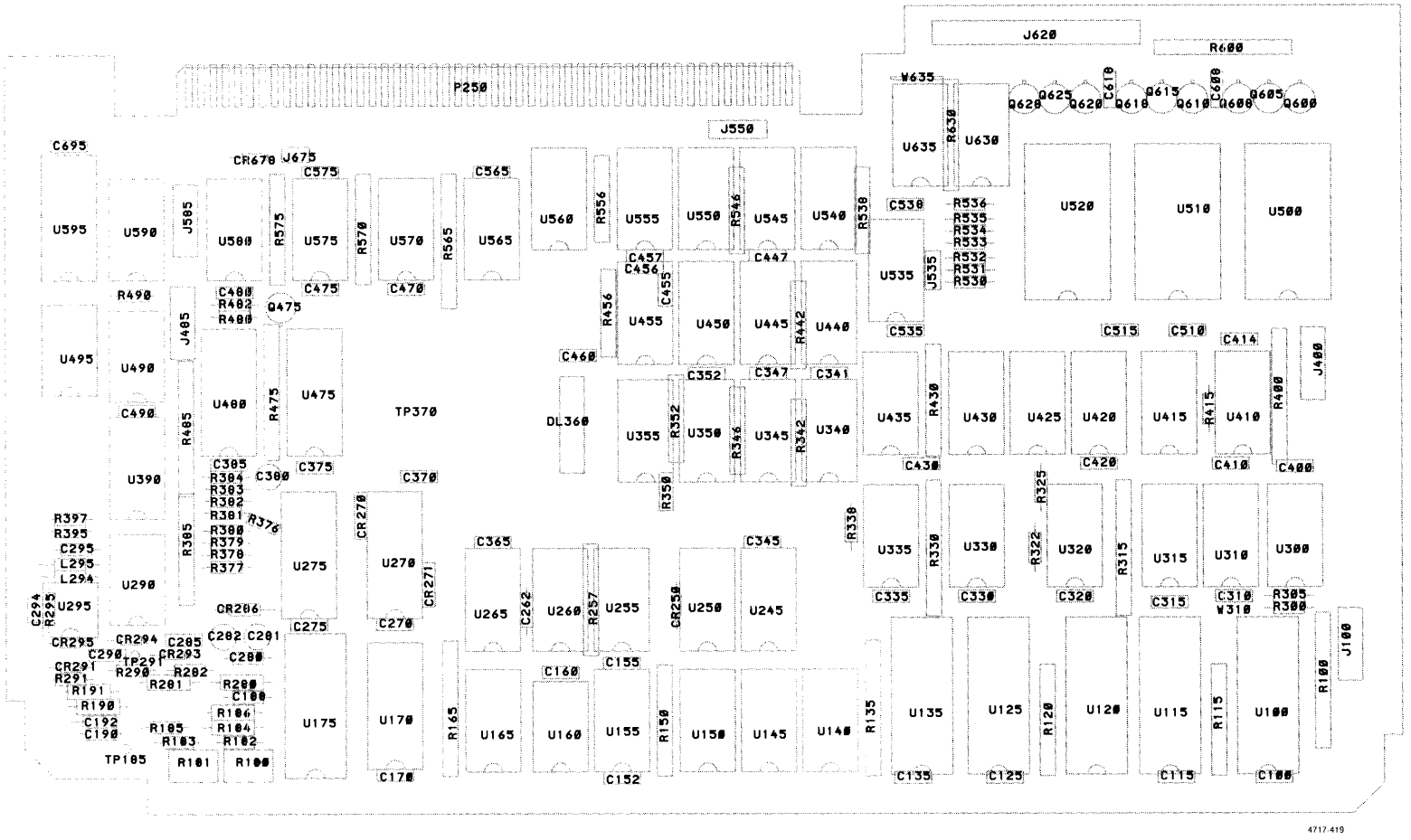


Figure 8-106. 9-Channel Acquisition Board component location.

module: 1240D1-X
area: GWR/GGR

GWR/GGR AREA – CIRCUIT OVERVIEW

The pattern-shaded signal lines on the global word and global glitch recognizer block diagram indicate circuitry used during diagnostic testing. Only the circuitry that is being exercised for the first time during diagnostic testing is shown. Circuitry exercised by other diagnostic tests are shown in their respective block diagrams.

The nine differential ECL-level channels CH0(H)(L)-CH8(H)(L) carry probe data to the Front End Hybrids (FEHs) A15U520, U510, and U500. The hybrids provide a latch for probe data, and compare incoming data and glitch information against previously selected event patterns. When a data word match occurs, A15U630 outputs the active-low global word recognizer GWR*(L) signal. When a data/glitch acquisition match occurs, both the global word recognizer and global glitch recognizer, GGR(H), outputs go to their active states. A15U630 is a dual OR-gate package that produces the GWR*(L) global word and GGR(H) global glitch recognizer signals sent to the trigger board.

Data latched by the hybrids is sent on the D0(H)-D8(H) and G0(H)-G8(H) lines to the Sequential Event Generation circuitry and the Data Chain Interface. Once at the chain interface, the information may be chained to the next acquisition card or sent to the Storage RAMs.

The serial global-event pattern information is loaded on BCD0(H). Each FEH has 16 internal shift/store control registers that hold the event patterns. After sequentially shifting the global data and glitch recognizer values into the hybrids with the SER CLK(H) signal, the SER STB(H) signal latches the data into the hybrids. An internal mode of operation for the FEHs, also programmed into the control registers, allows the global word recognizer to operate separately from the selected timebase. This allows data unrelated to the sample clock to be compared against global event patterns.

The DATA OUT(H) signal line carries the serial pattern information previously clocked in on the BCD0(H) line. Diagnostics use this read back information to verify the shift/store registers.

GWR/GGR AREA – TEST DESCRIPTION

The word recognizer test consists of two routines. Routine 1 verifies the operation of the Global Word Recognizer GWR*(L) signal. Routine 2 verifies the operation of the Global Glitch Recognizer GGR(H) signal. The test requires that the 9-Channel Acquisition card under test be connected to the Test Pattern Generator (TPG).

ROUTINE 1 – TEST DESCRIPTION

This routine verifies the operation of the Global Word Recognizer (GWR). The test first verifies that an acquisition probe is connected to the 9-channel card under test. If the probe returns a correct status, the test assumes the probe is also connected to the Test Pattern Generator (TPG). To verify the GWR circuitry, the word recognizer is loaded with a word identical to one of the TPG output words. The TPG is used as the source for input stimulus. By checking for GWR recognition of this specific word (indicated by the active GWR*(L) line), the operational status of the GWR may be determined. Refer to the *Operating Information* section for a complete listing of the A-side (J630) and B-side (J620) TPG-output words.

The test programs the global word recognizers in the 9-channel's Front End Hybrids to recognize the word $0AA_{hex}$. The acquisition card is programmed to acquire data synchronously and to use the AT2LF(L) signal as the source for acquisition clocks. The TPG is programmed to use the processor-stepped T1 clock. The TPG is then stepped to the word preceeding the event word (0AAH). The Control Processor reads the status of the GWR*(L) line through the Trigger-Control Processor Interface on the Trigger Board. (The polarity of the global word recognizer bit is inverted by the trigger circuitry before the readback occurs.) If the GWR outputs an active low signal indicating that a match to one of the TPG words was found, the test is aborted and a failure reported.

The processor then steps the output of the TPG one more time. The word generated, $0AA_{hex}$, should match the preprogrammed value in the GWR and the GWR*(L) line should go active low. If the active-low GWR signal was not generated, the test is aborted and a failure reported.

If recognition of the first word is successful, the global word recognizer is re-programmed to recognize the word 155_{hex}. The TPG is stepped to the word preceeding the event word (155_{hex}). The global event line is checked to ensure it is not asserted. The TPG is stepped once more and the event word is output. The GWR*(L) line is checked one last time to verify it is active low.

7511 Error Index

Explanation: The test failed to detect an acquisition probe.

Probable Cause	Action
The probe is not connected or the probe may be bad.	Check the probe connections and run the test again. If the test still fails, replace the probe and re-run the tests.
The probe's input or output status registers are defective.	While looping on this test, observe the serial data being output to the probe on A15U270-6. Check for a serial clock on A15U590-11. Also, check for the incoming serial probe data on A15U480-18.

7512 Error Index

Explanation: The global word recognizer output was asserted before it should have been.

Probable Cause	Action
Defective OR gate A15U630.	While looping on this test, observe the operation of A15U630-15, 12, 11, 10, and 13.
Defective polarity selector on the Trigger Board.	While looping on this test, observe the operation of A14U660-5 and 2.
Defective readback register on the Trigger Board.	While looping on this test, observe the operation of A14U275-2.
Defective 9-channel Front End Hybrid.	Check that the word reconizer outputs of the Front End Hybrids are not stuck low. If necessary, replace the FEHs one at a time and re-run the test.

7513 Error Index

Explanation: The global word recognizer output was not asserted when the TPG word $0AA_{hex}$ was output.

Probable Cause	Action
No serial strobe SER STB(H) signal was generated.	While looping on this test, verify the serial strobe signal on A15U290-3 and 4. If not present, check A15U580-12.
Defective OR gate A15U630.	While looping on this test, observe the operation of A15U630-15, 12, 11, 10, and 13.
Defective polarity selector on the Trigger Board.	While looping on this test, observe the operation of A14U660-5.
Defective readback register on the Trigger Board.	While looping on this test, observe the operation of A14U275-2.
Defective 9-channel Front End Hybrid.	Replace the FEHs one at a time and re-run the test.

7514 Error Index

Explanation: The global word recognizer output was not asserted when the TPG word 155_{hex} was output.

Probable Cause	Action
No serial strobe SER STB(H) signal was generated.	While looping on this test, verify the serial strobe signal on A15U290-3 and 4. If not present, check A15U580-12.
Defective OR gate A15U630.	While looping on this test, observe the operation of A15U630-15, 12, 11, 10, and 13.
Defective polarity selector on the Trigger Board.	While looping on this test, observe the operation of A14U660-5.
Defective readback register on the Trigger Board.	While looping on this test, observe the operation of A14U275-2.
Defective 9-channel Front End Hybrid.	Replace the FEHs one at a time and re-run the test.

ROUTINE 2 – TEST DESCRIPTION

This routine verifies the operation of the Global Glitch Recognizer (GGR). The test first verifies that an acquisition probe is connected to the 9-channel card under test. If the probe returns a correct status, the test assumes the probe is also connected to the Test Pattern Generator (TPG). To verify the GGR circuitry, the word recognizer is set to recognize glitches on all channels. The TPG is set to mode 3 (so it will generate glitches) and the TPG is programmed to use the processor-stepped T1 clock. The acquisition card is programmed to acquire data synchronously and to use the AT2LF(L) signal as the source for acquisition clocks.

The test steps the TPG three times, generating glitches on all channels. The Control Processor then reads the status of the GGR(H) line through the Trigger-Control Processor Interface on the Trigger Board. (The polarity of the global glitch recognizer bit is inverted by the trigger circuitry before readback occurs.) The readback should indicate an active-high Global Glitch Recognizer signal. If the GGR signal was not generated, the test is aborted and a failure is reported.

Next, the test disables the inputs to the Front End Hybrids (FEHs) and steps the TPG two more times. The Control Processor reads the status of the GGR to verify that it is inactive low.

7521 Error Index

Explanation: The test failed to detect an acquisition probe.

Probable Cause	Action
The probe is not connected or the probe may be bad.	Check the probe connections and run the test again. If the test still fails, replace the probe and rerun the tests.
The probe's input or output status registers are defective.	While looping on this test, observe the serial data being output to the probe on A15U270-6. Check for a serial clock on A15U590-11. Also check for the incoming serial probe data on A15U480-18.

7522 Error Index

Explanation: The global glitch recognizer output was not asserted after the glitches were generated.

Probable Cause	Action
Defective OR gate A15U630.	While looping on this test, observe the operation of A15U630-2, 4, 5, and 6.
Defective polarity selector on the Trigger Board.	While looping on this test, observe the operation of A14U660-7, 9, and 11.
Defective readback register on the Trigger Board.	While looping on this test, observe the operation of A14U275-6.
Defective 9-channel Front End Hybrid.	Check that the glitch recognizer outputs of the Front End Hybrids are not stuck low. If necessary, replace the FEHs one at a time and re-run the test.

7523 Error Index

Explanation: The global glitch recognizer output was still asserted with an acquisition containing no glitches.

Probable Cause	Action
The Front End Hybrids were not disabled.	With the test stopped, verify that A15U270-15 is at a logic low. Also verify that collectors of transistors A15Q600, Q605, Q608, Q610, Q615, Q618, Q620, Q625, and Q628 are all pulled high.
Defective OR gate A15U630.	While looping on this test, observe the operation of A15U630-2, 4, 5, and 6.
Defective polarity selector on the Trigger Board.	While looping on this test, observe the operation of A14U660-7, 9, and 11.
Defective readback register on the Trigger Board.	While looping on this test, observe the operation of A14U275-6.
Defective 9-channel Front End Hybrid.	Replace the FEHs one at a time and re-run the test.

1240D1 9-CHANNEL BLOCK DIAGRAM
SWR/SGR – AREA 6

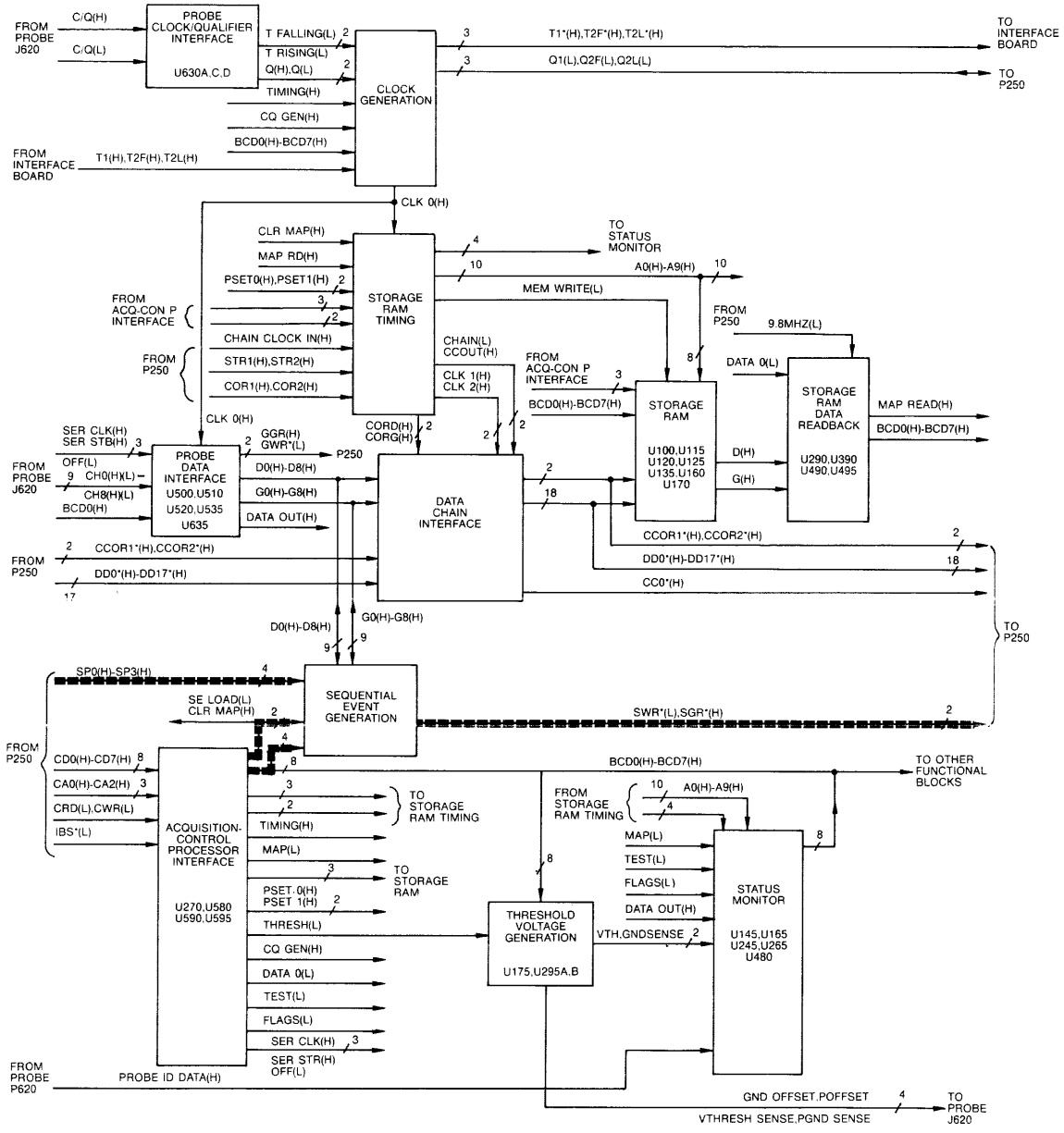


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Figure 8-107. 9-Channel SWR/SGR block diagram.

1240D1 9-CHANNEL ACQUISITION BOARD – COMPONENT LOCATION

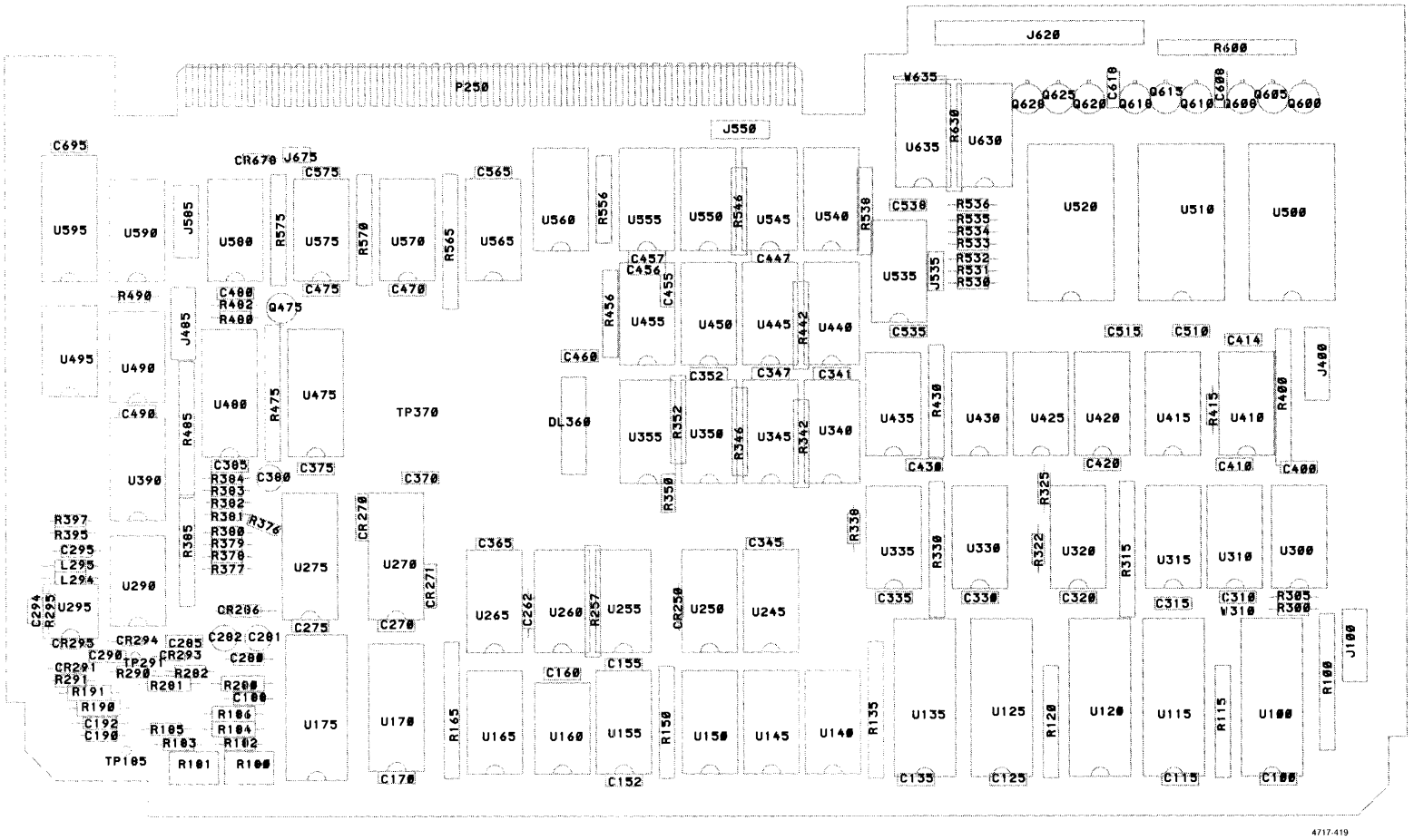

Figure 8-108. 9-Channel Acquisition Board component location.

module: 1240D1-X
area: SWR/SGR

SWR/SGR AREA – CIRCUIT OVERVIEW

The pattern-shaded signal lines on the sequential word/sequential glitch recognizer block diagram indicate circuitry used during diagnostic testing. Only the circuitry that is being exercised for the first time during diagnostic testing is shown. Circuitry exercised by other diagnostic tests are shown in their respective block diagrams.

The nine differential ECL-level channels CH0(H)(L)-CH8(H)(L) carry probe data to the Front End Hybrids (FEHs) A15U520, U510, and U500. The hybrids provide a latch for probe data, and compare incoming data and glitch information against previously selected event patterns. Data latched by the hybrids is sent on the D0(H)-D8(H) and G0(H)-G8(H) lines to the Sequential Event Generation circuitry and the Data Chain Interface.

This event generation circuitry uses sequential event RAMs for storage of up to 14 different event recognition patterns. The incoming probe data and glitch information from the Probe Data Interface is compared to the previously stored patterns and when a match is made, a sequential word recognizer, SWR*(L), or a sequential glitch recognizer, SGR*(H), control signal is generated.

The five-bit counter, A15U300, preloads the sequential event RAMs A15U415, U410, U435, and U425 with desired event patterns. The values are stored into 14 separate memory blocks per RAM (according to the user's Trigger menu setup) by controlling the BSP0(L)-BSP3(L) buffered stack pointer lines from A15U535. The Trigger Board generates these stack pointer lines to control which block is currently being accessed. When the outputs of the sequential word RAMs (A15U415 and U410) are both true, the active low SWR*(L) signal is generated. When the outputs of the sequential glitch RAMs (A15U435 and U425) are both true, the active high SGR*(H) signal is generated.

SWR/SGR AREA – TEST DESCRIPTION

The sequential word/glitch recognizer test consists of two routines. Routine 1 verifies the operation of the Sequential Word Recognizer (SWR). Routine 2 verifies the operation of the Sequential Glitch Recognizer (SGR). Both tests require that the 9-channel acquisition card under test be connected to the Test Pattern Generator (TPG).

ROUTINE 1 – TEST DESCRIPTION

This routine verifies the operation of the Sequential Word Recognizer (SWR). The test first verifies that an acquisition probe is connected to the 9-channel card under test. If the probe returns a correct status, the test assumes the probe is also connected to the Test Pattern Generator (TPG). To verify the SWR circuitry, the word recognizer is loaded with 15 TPG words. The TPG is used as the source for input stimulus. By checking for SWR recognition of this specific word (indicated by the active SWR*(L) line), the operational status of the SWR may be determined. Refer to the *Operating Information* section for a complete listing of the TPG-output words on A14J630.

The test programs the sequential word recognizer RAMs to recognize the first word of the 15-word sequence starting with the third TPG word, 17DH. The acquisition card is programmed to acquire data synchronously and to use the AT2LF(L) signal as the source for acquisition clocks. The TPG is programmed to use the processor-stepped T1 clock and is then stepped to the word preceeding the event word (17DH). The test steps the TPG output 15 times, checking the condition of the SWR*(L) line after each clock. If the SWR does not output an active low signal indicating that a match to one of the TPG words was not found, the test is aborted and a failure is reported. The SWR word that failed is displayed in the result address field, the stack value is displayed in the actual result field.

If the first part of the test was successful, the processor then steps the TPG two more times and the process begins again starting with the TPG word $1B6_{hex}$. If the SWR signal did not go active-low each time the TPG was clocked, the test is aborted and a failure is reported.

In all, this sequence is run four times, using 15 TPG words each time and skipping two words between each 15-word group. The test generates a total of 68 TPG clocks (4 $\times$ 17).

7611 Error Index

Explanation: The test failed to detect an acquisition probe.

Probable Cause	Action
The probe is not connected or the probe may be bad.	Check the probe connections and run the test again. If the test still fails, replace the probe and rerun the tests.
The probe's input or output status registers are defective.	While looping on this test, observe the serial data being output to the probe on A15U270-6. Check for a serial clock on A15U590-11. Also check for the incoming serial probe data on A15U480-18.

7612 Error Index

Explanation: The SWR output was not asserted when it should have recognized the first TPG word. Refer to the *Operating Information* section for a complete listing of the TPG-output words on A14J630.

Probable Cause	Action
The sequential word recognizer is not being programmed correctly.	While looping on this test, check pin 13 of A15U410 and U415 for write enable strobes. Also, check for activity on data inputs at pin 15 of U410 and U415. While looping on this test, use a logic analyzer to verify that the SWR RAMs are being filled correctly. Also, the stack pointer inputs on pins 2, 4, 5, and 3 of A15U410 and U415 should count down from 15 to 0 as the RAMs are loaded. The data input to the RAMs should be consecutive TPG values, one value for each stack level. Refer to the *Operating Information* section for a complete listing of the TPG-output words on A14J630.
The SWR is not receiving correct data from the TPG.	While looping on this test, use a logic analyzer to verify that data coming to the SWR RAMs (A15U415 and U410) is correct data. The data input to the RAMs should be consecutive TPG values, one value for each stack level.
Bad address or data bit in the SWR.	The value reported in the ADDR field of the diagnostic display is the TPG word that the SWR failed to recognize. If this value is one in which a single bit changed for the first time, then the RAM that holds that bit may have a bad location. If it is not possible to isolate a single bit failure, suspect both RAMs A15U415 and U410.

7613 Error Index

Explanation: This test is the same as for the 7612 error index except that the failure was not detected until the second group of 15 words was loaded into the SWR. This group started with the TPG word $1B6_{hex}$. Refer to the *Operating Information* section for a complete listing of the TPG-output words on A14J630.

Probable Cause	Action
Bad address or data bit in the SWR.	The value reported in the ADDR field of the diagnostic display is the TPG word that the SWR failed to recognize. If this value is one in which a single bit changed for the first time, then the RAM that holds that bit may have a bad location. If it is not possible to isolate a single bit failure, suspect both RAMs A15U415 and U410.

7614 Error Index

Explanation: This test is the same as for the 7612 error index except that the failure was not detected until the third group of 15 words was loaded into the SWR. This group started with the TPG word $1D7_{hex}$. Refer to the *Operating Information* section for a complete listing of the TPG-output words on A14J630.

Probable Cause	Action
Bad address or data bit in the SWR.	The value reported in the ADDR field of the diagnostic display is the TPG word that the SWR failed to recognize. If this value is one in which a single bit changed for the first time, then the RAM that holds that bit may have a bad location. If it is not possible to isolate a single bit failure, suspect both RAMs A15U415 and U410.

7615 Error Index

Explanation: This test is the same as for the 7612 error index except that the failure was not detected until the fourth group of 15 words was loaded into the SWR. This group started with the TPG word 082_{hex}. Refer to the *Operating Information* section for a complete listing of the TPG-output words on A14J630.

Probable Cause	Action
Bad address or data bit in the SWR.	The value reported in the ADDR field of the diagnostic display is the TPG word that the SWR failed to recognize. If this value is one in which a single bit changed for the first time, then the RAM that holds that bit may have a bad location. If it is not possible to isolate a single bit failure, suspect both RAMs A15U415 and U410.

ROUTINE 2 – TEST DESCRIPTION

This routine verifies the operation of the Sequential Glitch Recognizer (SGR). The test first verifies that an acquisition probe is connected to the 9-channel card under test. If the probe returns a correct status, the test assumes the probe is also connected to the Test Pattern Generator (TPG). To verify the SGR circuitry, the word recognizer is loaded with 15 TPG words. The TPG is used as the source for input stimulus. By checking for SGR recognition of this specific word (indicated by the active SGR*(H) line), the operational status of the SGR may be determined. Refer to the *Operating Information* section for a complete listing of the TPG-output words on A14J630.

The test programs the sequential glitch recognizer RAMs to recognize the first word of the 15-word sequence starting with the second TPG word, $1BE_{hex}$. The acquisition card is programmed to acquire data synchronously and to use the AT2LF(L) signal as the source for acquisition clocks. The TPG is programmed to use the processor-stepped T1 clock and is then stepped to the word preceeding the event word ($1BE_{hex}$).

The test steps the TPG output 15 times, checking the condition of SP0-SP3 stack lines (through A14U110) after each clock. If the SGR does not output an active low signal indicating that a match to one of the TPG words was not found, the test is aborted and a failure is reported. The reported address shows which word the SGR failed to recognize. The expected value field shows what the stack value should have been.

If the first part of the test was successful, the processor then steps the second group of 15 TPG words out of the TPG. The starting word for the second group is $1AE_{hex}$. If the SGR signal did not go active-low each time the TPG was clocked, the test is aborted and a failure is reported.

In all, this sequence is run four times, using 15 TPG words each time and skipping the previous word between each 15-word group. The test generates 16 TPG clocks for the first group, 31 TPG clocks on the second group, 46 clocks on the third group, and 61 clocks on the fourth group.

7621 Error Index

Explanation: The test failed to detect an acquisition probe.

Probable Cause	Action
The probe is not connected or the probe may be bad.	Check the probe connections and run the test again. If the test still fails, replace the probe and rerun the tests.
The probe's input or output status registers are defective.	While looping on this test, observe the serial data being output to the probe on A15U270-6. Check for a serial clock on A15U590-11. Also check for the incoming serial probe data on A15U480-18.

7622 Error Index

Explanation: The SGR output was not asserted when it should have recognized the first TPG word. Refer to the *Operating Information* section for a complete listing of the TPG-output words on A14J630.

Probable Cause	Action
The sequential glitch recognizer is not being programmed correctly.	While looping on this test, check pin 13 of A15U425 and U435 for write enable strobes. Also check for activity on data inputs at pin 15 of U425 and U435. While looping on this test, use a logic analyzer to verify that the SGR RAMs are being filled correctly. Also, the stack pointer inputs on pins 3, 2, 5, and 4 of A15U425 and pins 3, 2, 6, and 5 of U435 should count down from 15 to 0 as the RAMs are loaded. The data input to the RAMs should be consecutive TPG values, one value for each stack level. Refer to the *Operating Information* section for a complete listing of the TPG-output words on A14J630.
The SGR is not receiving correct data from the TPG.	While looping on this test, use a logic analyzer to verify that data coming to the SGR RAMs (A15U425 and U435) is correct data. The data input to the RAMs should be consecutive TPG values, one value for each stack level.
Bad address or data bit in the SGR.	The value reported in the ADDR field of the diagnostic display is the TPG word that the SGR failed to recognize. If this value is one in which a single bit changed for the first time, then the RAM that holds that bit may have a bad location. If it is not possible to isolate a single bit failure, suspect both RAMs A15U425 and U435.
Bad readback comparator on Trigger Board.	Suspect comparator A14U110.

7623 Error Index

Explanation: This test is the same as for the 7622 error index except that the failure was not detected until the second group of 15 words was loaded into the SGR. This group started with the TPG word $1AE_{hex}$. Refer to the *Operating Information* section for a complete listing of the TPG-output words on A14J630.

Probable Cause	Action
Bad address or data bit in the SGR.	The value reported in the ADDR field of the diagnostic display is the TPG word that the SGR failed to recognize. If this value is one in which a single bit changed for the first time, then the RAM that holds that bit may have a bad location. If it is not possible to isolate a single bit failure, suspect both RAMs A15U425 and U435.

7624 Error Index

Explanation: This test is the same as for the 7622 error index except that the failure was not detected until the third group of 15 words was loaded into the SGR. This group started with the TPG word 071_{hex}. Refer to the *Operating Information* section for a complete listing of the TPG-output words on A14J630.

Probable Cause	Action
Bad address or data bit in the SGR.	The value reported in the ADDR field of the diagnostic display is the TPG word that the SGR failed to recognize. If this value is one in which a single bit changed for the first time, then the RAM that holds that bit may have a bad location. If it is not possible to isolate a single bit failure, suspect both RAMs A15U425 and U435.

7625 Error Index

Explanation: This test is the same as for the 7622 error index except that the failure was not detected until the fourth group of 15 words was loaded into the SGR. This group started with the TPG word 186_{hex}. Refer to the *Operating Information* section for a complete listing of the TPG-output words on A14J630.

Probable Cause	Action
Bad address or data bit in the SGR.	The value reported in the ADDR field of the diagnostic display is the TPG word that the SGR failed to recognize. If this value is one in which a single bit changed for the first time, then the RAM that holds that bit may have a bad location. If it is not possible to isolate a single bit failure, suspect both RAMs A15U425 and U435.

1240D1 9-CHANNEL BLOCK DIAGRAM
X ACQ RAM – AREA 7

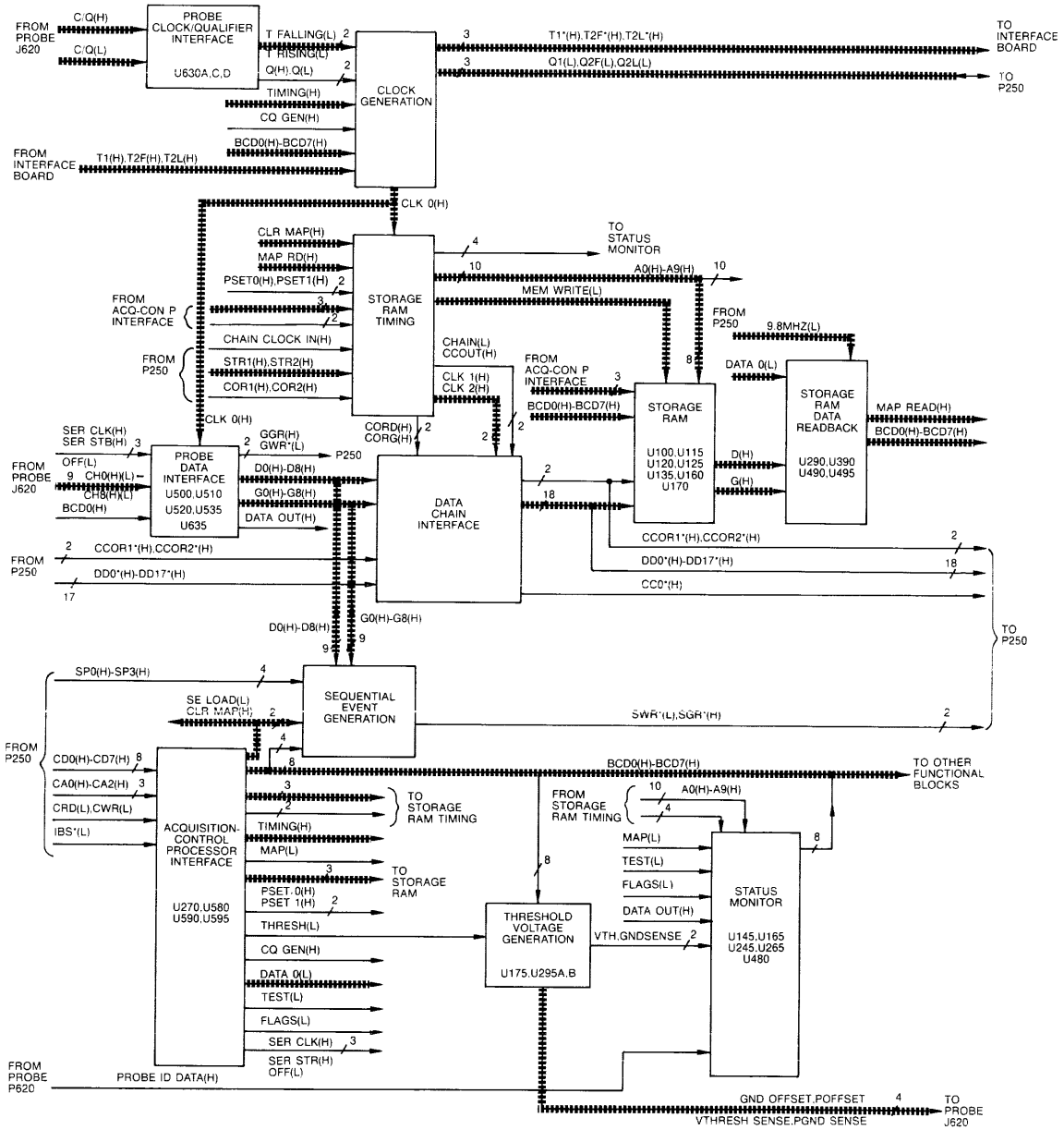

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Figure 8-109. 9-Channel X ACQ RAM block diagram.

1240D1 9-CHANNEL ACQUISITION BOARD – COMPONENT LOCATION

Figure 8-110. 9-Channel Acquisition Board component location.

module: 1240D1-X
area: X ACQ RAM

X ACQ RAM AREA – CIRCUIT OVERVIEW

The pattern-shaded signal lines on the extended acquisition RAM block diagram indicate circuity tested by test Area 2, ACQ RAM. In this case, shading does not indicate circuitry exercised for the first time during diagnostic testing, but instead shows the test path.

Since the circuitry involved during these 77XX extended acquisition RAM diagnostic tests is basically the same as that used during the 72XX Acquisition RAM diagnostic tests, circuit descriptions are not repeated here.

X ACQ RAM AREA – TEST DESCRIPTION

The extended acquisition RAM test consists of two routines. Routine 1 verifies the 9-channel's ability to correctly store five pre-determined TPG-data values. Routine 2 verifies the ability of the Global Word Recognizer to correctly store data patterns that have the three-most-significant data bits as ones (i.e., 1 11XX XXX). Routine 2 requires that an acquisition be used to connect the 9-channel and the Test Pattern Generator (TPG).

ROUTINE 1 – TEST DESCRIPTION

This test verifies the 9-channel's ability to correctly store five pre-determined data values. The data values 021_{hex}, 042_{hex}, 084_{hex}, 108_{hex}, and 010_{hex} are then read from the acquisition storage RAM and verified to be correct.

The test begins by disabling the inputs to the Front End Hybrids (FEHs) U520, U510, and U520. The five-bit counter A15U300 and buffers U315, U420, and U430 are normally used to preload the sequential event RAMs A15U415, U410, U435, and U425 with sequential word and glitch event patterns. For diagnostic purposes, this circuitry is able to generate distinct data patterns that can be stored in acquisition RAM. This counter is initially set to a value of 01_{hex}, causing the 9-bit value 021_{hex} to be generated. The acquisition RAMs are clocked 512 times by the processor-stepped T1 clock. Data stored in acquisition RAM is then checked to determine if it is correct.

7711

If the first counter value was successfully acquired in all 512 memory locations, the test is repeated using counter values 02_{hex}, 04_{hex}, 08_{hex}, and 10_{hex}. These counter values produce data words 042_{hex}, 084_{hex}, 108_{hex}, and 010_{hex}, respectively.

Failures detected during the diagnostics are reported on the 1240 display screen.

7711 Error Index

Explanation: The acquisition RAM should have contained 021_{hex}, but at least one location contained some other value.

Probable Cause	Action
Defective acquisition memory.	Using the reported expected and actual screen data, determine the failed bit. If the bit is D0, suspect A15U120. If the failed bit is D1 through D4, suspect A15U115. If the bit is D5 through D8, suspect A15U100.
No write enable to the acquisition memory.	While looping on this test, verify the WE(L) signal on pin 8 of A15U100, U115, and U120. If not present, check A15U140-7 or J100-4.
Defective counter or buffers.	While looping on this test, observe the outputs of the counter. A15U300 pins 11, 6, 5, 4, and 3 should contain 00001B. Also, check the buffer outputs at A15U315 pins 4, 3, 2, 13, 14, and 15 and buffer outputs at U420 pins 4, 3, and 2 for the value 021_{hex}.

7712 Error Index

Explanation: The acquisition RAM should have contained 042_{hex}, but at least one location contained some other value.

Probable Cause	Action
Defective acquisition memory.	Using the reported expected and actual screen data, determine the failed bit. If the bit is D0, suspect A15U120. If the failed bit is D1 through D4, suspect A15U115. If the bit is D5 through D8, suspect A15U100.
Defective counter or buffers.	While looping on this test, observe the outputs of the counter. A15U300 pins 11, 6, 5, 4, and 3 should contain 00010B. Also, check the buffer outputs at A15U315 pins 4, 3, 2, 13, 14, and 15 and buffer outputs at U420 pins 4, 3, and 2 for the value 042_{hex}.

7713 Error Index

Explanation: The acquisition RAM should have contained 084_{hex}, but at least one location contained some other value.

Probable Cause	Action
Defective acquisition memory.	Using the reported expected and actual screen data, determine the failed bit. If the bit is D0, suspect A15U120. If the failed bit is D1 through D4, suspect A15U115. If the bit is D5 through D8, suspect A15U100.
Defective counter or buffers.	While looping on this test, observe the outputs of the counter. A15U300 pins 11, 6, 5, 4, and 3 should contain 00100B. Also, check the buffer outputs at A15U315 pins 4, 3, 2, 13, 14, and 15 and buffer outputs at U420 pins 4, 3, and 2 for the value 084_{hex}.

7714 Error Index

Explanation: The acquisition RAM should have contained 108_{hex}, but at least one location contained some other value.

Probable Cause	Action
Defective acquisition memory.	Using the reported expected and actual screen data, determine the failed bit. If the bit is D0, suspect A15U120. If the failed bit is D1 through D4, suspect A15U115. If the bit is D5 through D8, suspect A15U100.
Defective counter or buffers.	While looping on this test, observe the outputs of the counter. A15U300 pins 11, 6, 5, 4, and 3 should contain 01000B. Also, check the buffer outputs at A15U315 pins 4, 3, 2, 13, 14, and 15 and buffer outputs at U420 pins 4, 3, and 2 for the value 108_{hex}.

7715 Error Index

Explanation: The acquisition RAM should have contained 010_{hex}, but at least one location contained some other value.

Probable Cause	Action
Defective acquisition memory.	Using the reported expected and actual screen data, determine the failed bit. If the bit is D0, suspect A15U120. If the failed bit is D1 through D4, suspect A15U115. If the bit is D5 through D8, suspect A15U100.
Defective counter or buffers.	While looping on this test, observe the outputs of the counter. A15U300 pins 11, 6, 5, 4, and 3 should contain 10000B. Also, check the buffer outputs at A15U315 pins 4, 3, 2, 13, 14, and 15 and buffer outputs at U420 pins 4, 3, and 2 for the value 010_{hex}.

ROUTINE 2 – TEST DESCRIPTION

This test verifies the ability of the Global Word Recognizer (GWR) to cause storage of all data patterns having the three-most-significant data bits as ones (i.e., 1 11XX XXX). The eight TPG words matching this pattern are $1FF_{hex}$, $1F7_{hex}$, $1E7_{hex}$, $1D7_{hex}$, $1EF_{hex}$, $1C7_{hex}$, $1CF_{hex}$, and $1DF_{hex}$. After storage, these values are read from the acquisition RAM and verified to be correct.

First, the test determines if the acquisition probe is connected to the acquisition card. If the probe is not connected, the test reports a failure and the test is aborted. The acquisition card is programmed to acquire data synchronously and to use the AT2LF(L) signal as the source for acquisition clocks. The TPG is programmed to use the processor-stepped T1 clock. The Global Word Recognizer is programmed to recognize all data patterns having the three-most-significant data bits as ones (i.e., 1 11XX XXX). The acquisition hardware is set to acquire only those TPG words that are qualified by the GWR.

After the test is run, the first 7 memory locations are checked for correct data. (Only the last 7 TPG-output words are actually acquired, the first $1FF_{hex}$ is not acquired.) Failures detected during the diagnostics are reported on the 1240 display screen.

7721 Error Index

Explanation: The test failed to detect the acquisition probe.

Probable Cause	Action
The acquisition probe is improperly connected or bad.	Examine the expected and actual results. If the expected data is 00 and the actual data is 40, then suspect the probe.
Defective input or output latch.	While looping on this test, use a test oscilloscope to check A15U270-6 for serial data being output. Check A15U590-11 for a clock output to the probe. Check A15U480-18 for input probe I.D. serial data.

7722 Error Index

Explanation: Defective Global Word Recognizer.

Probable Cause	Action
Defective Front End Hybrids (FEHs).	Suspect A15U500, U510, and U520.
Defective qualified data store control circuitry on the Trigger module.	Refer to the Trigger module diagnostics (error indexes 6XXX).

1240D1 9-CHANNEL BLOCK DIAGRAM
CHAINING - AREA 8

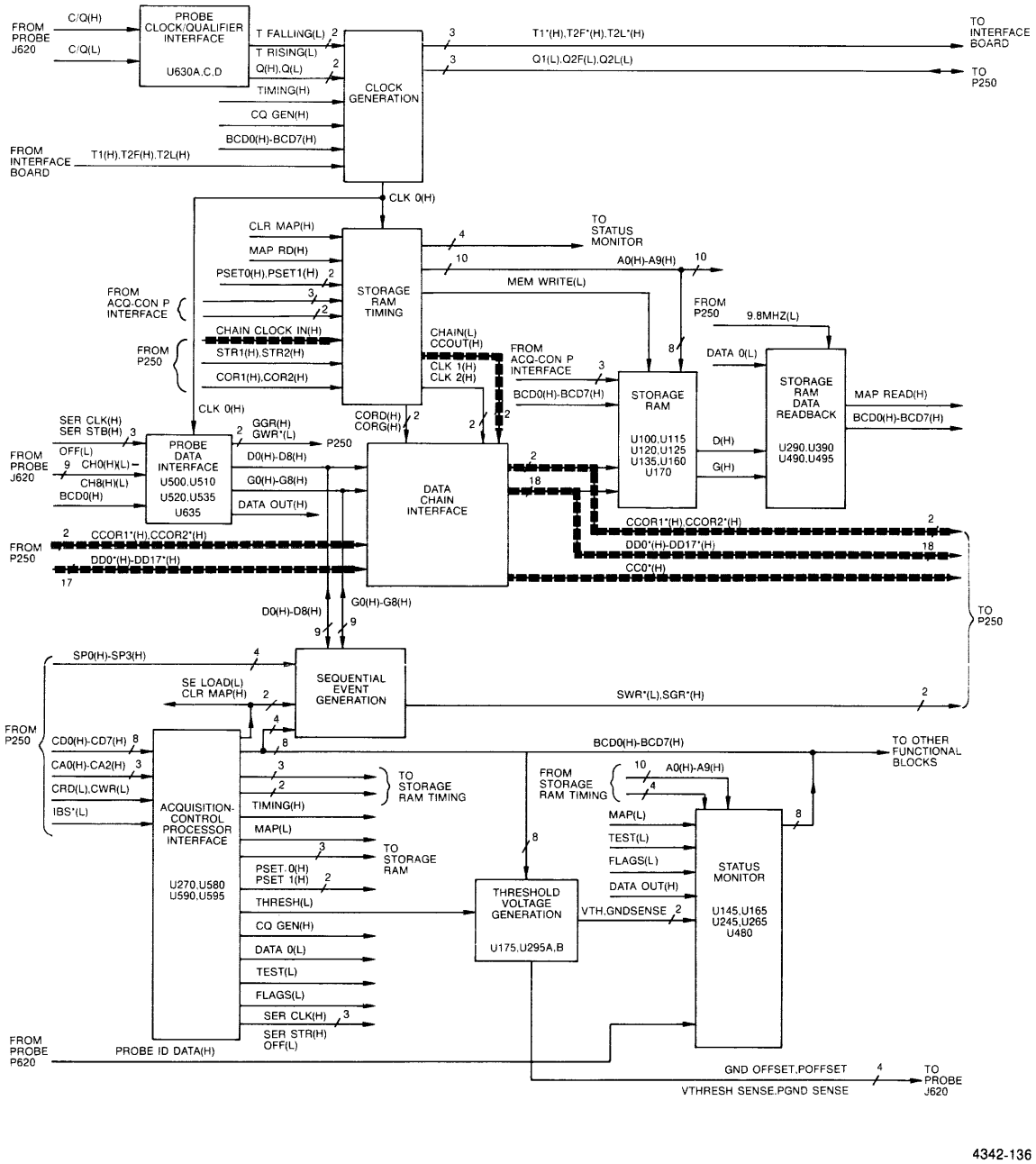


Figure 8-111. 9-Channel CHAINING block diagram.

1240D1 9-CHANNEL ACQUISITION BOARD – COMPONENT LOCATION

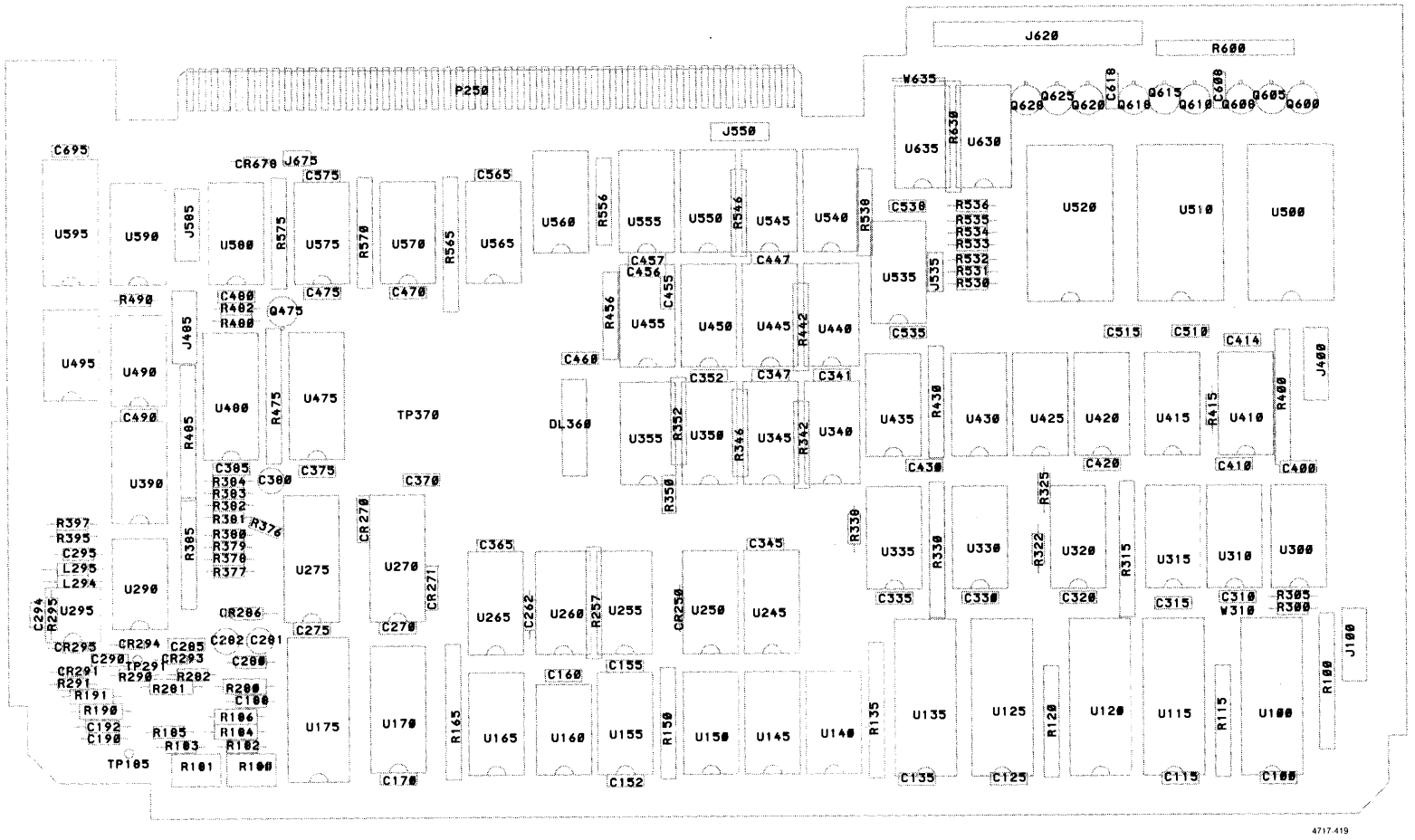


Figure 8-112. 9-Channel Acquisition Board component location.

module: 1240D1-X
area: CHAINING

CHAINING AREA – CIRCUIT OVERVIEW

The pattern-shaded signal lines on the chaining block diagram indicate circuitry used during diagnostic testing. Only the circuitry that is being exercised for the first time during diagnostic testing is shown. Circuitry exercised by other diagnostic tests are shown in their respective block diagrams.

Chaining of data from one acquisition board to the next is accomplished through the 9-Channel Acquisition Board's Data Chain Interface. The interface consists of two sets of data latches. The probe data latches A15U320, U310, U335, and U330 accept data on the D0(H)-D8(H) and G0(H)-G8(H) signal lines from the Probe Data Interface. Output data from these latches is available for either the Storage RAMs or the data chain bus, if chaining is in effect. The chain bus latches A15U575, U570, U565, and U560 transmit data to the next acquisition card in the data chain, allowing each acquisition card to pass (i.e., chain) data to the next like acquisition card.

The CCOR1*(H) and CCOR2*(H) signals are the correlation chaining signals that carry correlation information to the next acquisition card in the chain. This information, stored with the probe data, is used when reconstructing data for display if two asynchronous timebases were used during the acquisition.

NOTE

*Chaining of data from the first acquisition card to the next requires common data bus lines and control lines. To distinguish between each of the four identical acquisition board slots on the Interface Board, the * symbol in a signal name takes on a letter from A to D. For example, the signal DD0*(H) is common to four different acquisition slots, but becomes DD0A(H) when referencing acquisition slot 0 (J250). The remaining designations are: * = B for slot 1 (J350), * = C for slot 2 (J450), and * = D for slot 3 (J550).*

The 9-channel's Memory Address Pointer (MAP) circuitry generates the addresses used to access the storage RAMs. These addresses also serve as a memory address pointer value used by the Control Processor when reconstructing data for display. As a count is produced on address lines A8(H) and A9(H), a comparison to the memory chain depth indicators PSET 0(H) and PSET 1(H) is made by A15U155A. If the depth indicators are set at 00 (no cards chained), the logic causes the counter A15U255 to output an active FO(H) Filled Once signal when the first acquisition card is filled. If the depth indicators were set at 11 (binary code indicating four cards chained), the FO(H) signal would become active on this card after all cards in the chain are filled.

CHAINING AREA – TEST DESCRIPTION

This test verifies the ability of the 9-Channel Acquisition cards to chain data from one card to another. Up to four boards may be tested, provided that they are installed into consecutive slots in the Interface Board. The acquisition board closest to the Trigger Board must have an acquisition probe connecting it to the Test Pattern Generator (TPG).

NOTE

The chaining tests do not thoroughly check chain in on the first board, and chain out on the last board in the chain. For a complete check, these boards should be placed in the middle of the chain.

The test programs the acquisition card to acquire data synchronously and to use the AT2LF(L) signal as the source for acquisition clocks. The TPG is programmed to use the processor-stepped T1 clock. Next, the processor reads the I.D. status from each acquisition board slot in the interface to determine the number of 9-channel cards in the chain. This also allows the test to determine the total chained memory length (1025 for 2 boards, 1537 for 3 boards, and 2049 for 4 boards). The processor clocks the TPG (memory depth +2) times, filling the 9-channel memory chain until all boards have been filled once. Then the processor reads the data back from the storage RAMs and compares the results to correct TPG output patterns. If a problem is detected, the test is aborted and the failure is reported.

7811 Error Index

Explanation: The probe status indicates that no probe is connected to the acquisition card.

Probable Cause	Action
The acquisition probe is improperly connected or bad.	Connect the probe if it is not connected; otherwise suspect the probe.
Defective input or output latch.	While looping on this test, use a test oscilloscope to check A15U270-6 for serial data being output. Check A15U590-11 for a clock output to the probe. Check A15U480-18 for input probe I.D. serial data.

7812 Error Index

Explanation: The actual data read from the board nearest the Trigger Board did not match the expected data.

Probable Cause	Action
Defective probe.	Replace the probe and run the test again.
Timing malfunction causing and incorrect write clock to the acquisition memory.	With the routine stopped on the failure, check for a logic low on both A15U270-16 and U590-9. While looping on the test, check for a clock signal on A15U140-7 and a strobe pulse on U455-2. Also verify that Trigger module failure 6113 did not occur. If it did, the problem is probably in the generation of the T1 clock.
Defective probe data latch A15U320 or A15U310.	While looping on this test, use a logic analyzer to verify the TPG data on the outputs of the probe data latches A15U320 and U310. (Refer to the *Operating Information* section for TPG output patterns.)
The Memory Address Pointer (MAP) circuitry did not increment correctly.	While looping on this test, use a logic analyzer to observe the output of the MAP count on pins 2, 3, 14, and 15 of A15U150 and U250. The count should increment from 000_{hex} to $0FF_{hex}$.
Defective Front End Hybrid (FEH).	Determine which of the 3 hybrids is defective by comparing the expected and actual data. If the error is in the lower 3 bits, replace A15U520. The middle 3 bits are associated with U510 errors, and U500 is responsible for the upper 3 error bits.
The Test Pattern Generator (TPG) is defective.	While looping on this test, use a logic analyzer to verify the TPG output at A14J630.

7813 Error Index

Explanation: The actual data read from the second board nearest the Trigger Board did not match the expected data.

Probable Cause	Action
Defective chain bus latches on the previous acquisition board.	While looping on this test, use a logic analyzer to observe the operation of latches A15U560, U565, U570, and U575 on the first board in the chain. Check for a clock signal on pin 9 of these latches. Check for the CHAIN(L) signal on A15U560-4 and 13 and pin 1 of A15U565, U570, and U575. While looping on this test, use a logic analyzer to verify the TPG data on the outputs of the chain data latches A15U565, U570, and U575. (Refer to the *Operating Information* section for TPG output patterns.) If the acquisition RAM is suspected of being faulty, run the acquisition RAM tests on the suspect board.

7814 Error Index

Explanation: The actual data read from the third board nearest the Trigger Board did not match the expected data.

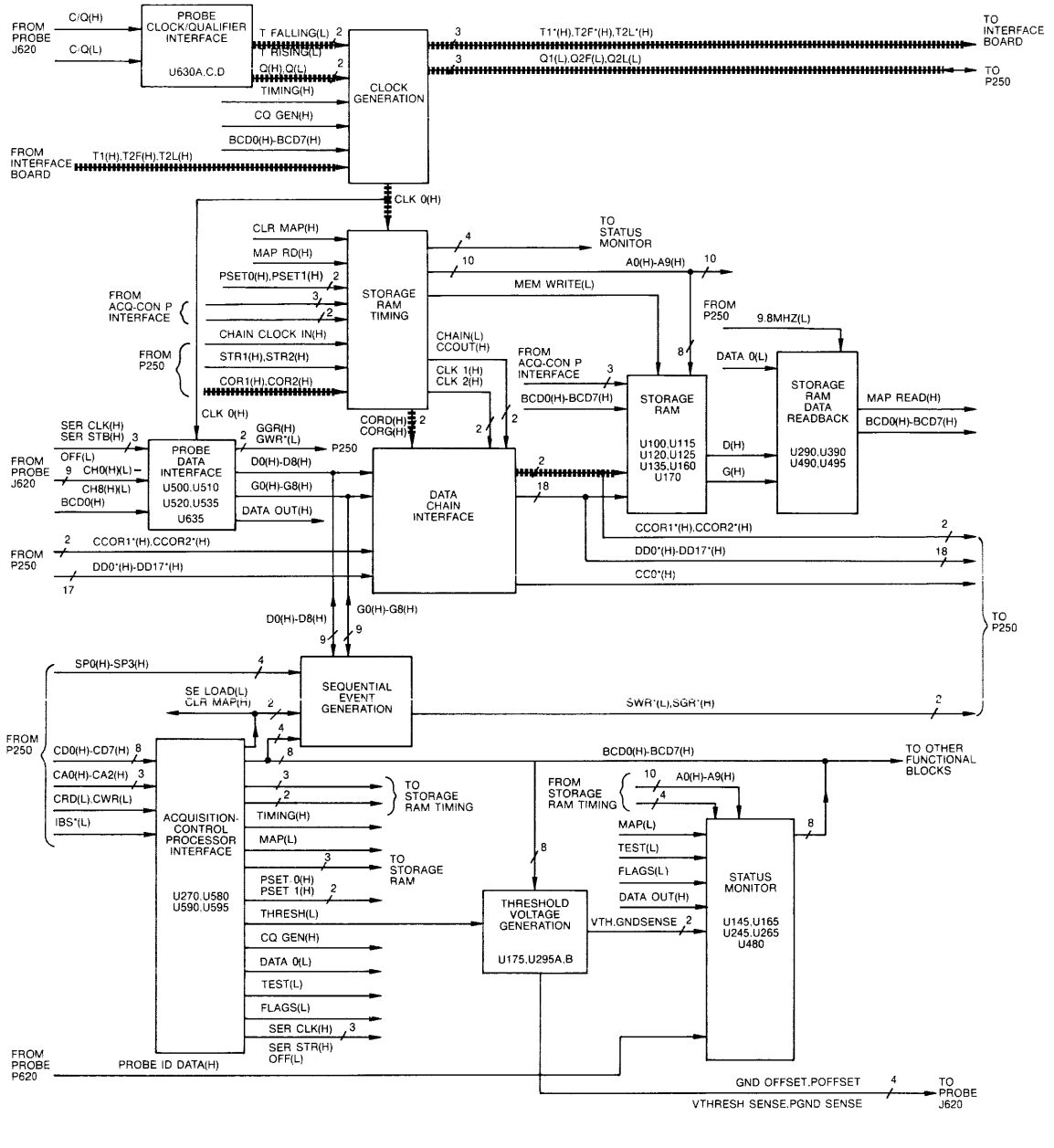
Probable Cause	Action
Defective chain bus latches on the previous acquisition board.	While looping on this test, use a logic analyzer to observe the operation of latches A15U560, U565, U570, and U575 on the second board in the chain. Check for a clock signal on pin 9 of these latches. Check for the CHAIN(L) signal on A15U560-4 and 13 and pin 1 of A15U565, U570, and U575. While looping on this test, use a logic analyzer to verify the TPG data on the outputs of the chain data latches A15U565, U570, and U575. (Refer to the *Operating Information* section for TPG output patterns.) If the acquisition RAM is suspected of being faulty, run the acquisition RAM tests on the suspect board.

7815 Error Index

Explanation: The actual data read from the fourth board nearest the Trigger Board did not match the expected data.

Probable Cause	Action
Defective chain bus latches on the previous acquisition board.	While looping on this test, use a logic analyzer to observe the operation of latches A15U560, U565, U570, and U575 on the third board in the chain. Check for a clock signal on pin 9 of these latches. Check for the CHAIN(L) signal on A15U560-4 and 13 and pin 1 of A15U565, U570, and U575. While looping on this test, use a logic analyzer to verify the TPG data on the outputs of the chain data latches A15U565, U570, and U575. (Refer to the *Operating Information* section for TPG output patterns.) If the acquisition RAM is suspected of being faulty, run the acquisition RAM tests on the suspect board.

1240D1 9-CHANNEL BLOCK DIAGRAM
TIMING – AREA 9



4342-137

Figure 8-113. 9-Channel TIMING block diagram.

1240D1 9-CHANNEL ACQUISITION BOARD – COMPONENT LOCATION

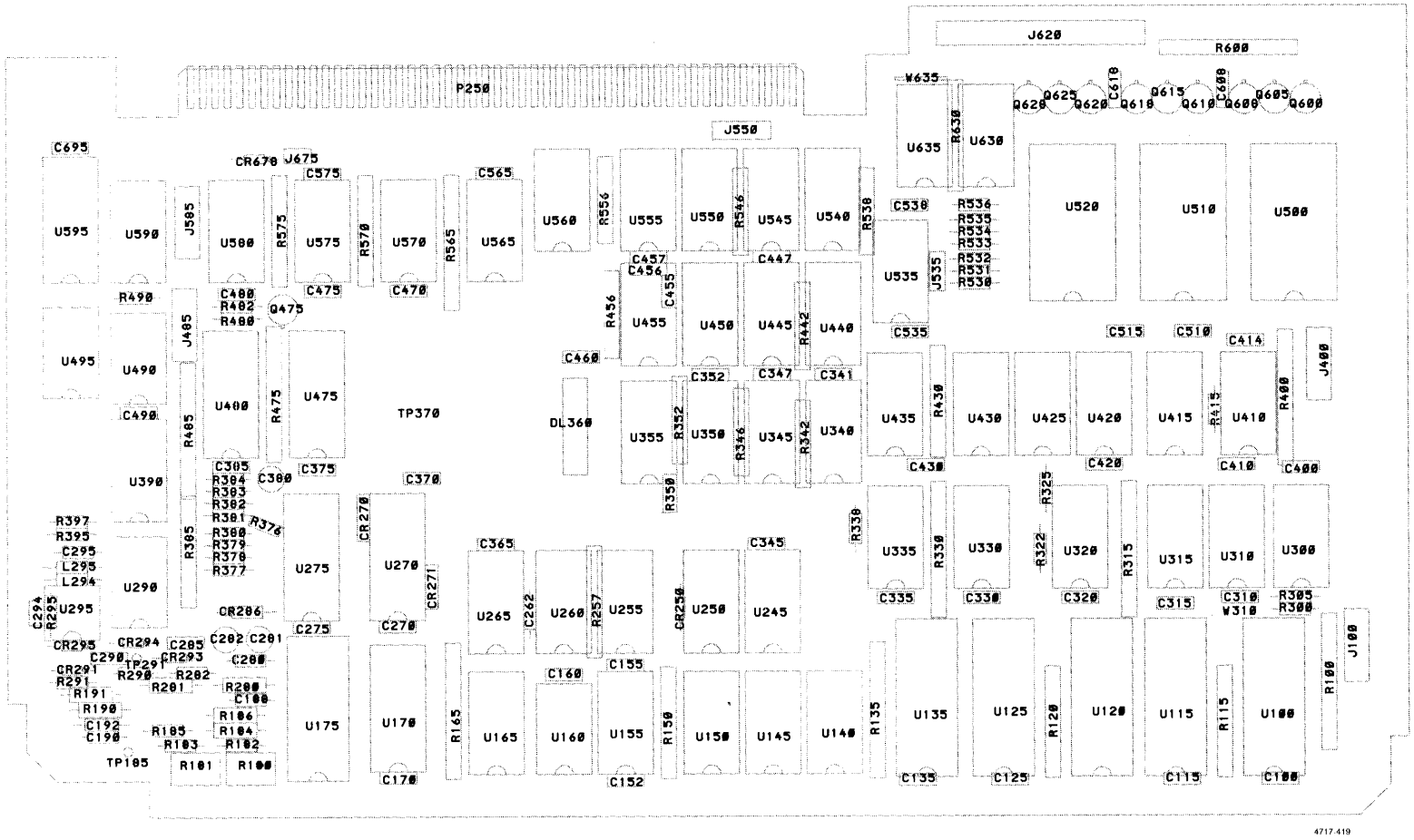


Figure 8-114. 9-Channel Acquisition Board component location.

module: 1240D1-X
area: TIMING

TIMING AREA – CIRCUIT OVERVIEW

The pattern-shaded signal lines on the timing block diagram indicate circuitry used during diagnostic testing. Only the circuitry that is being exercised for the first time during diagnostic testing is shown. Circuitry exercised by other diagnostic tests are shown in their respective block diagrams.

Differential line receivers A15U635A and C in the Probe Clock/Qualifier Interface accept the ECL-level clock/qualifier lines C/Q(L) and C/Q(H) from the installed acquisition probe. The resulting signals are used for the generation of T clocks and Q qualifiers in the Clock Generation circuitry.

Transitions on the differential C/Q lines pass through U635C. A falling edge on the C/Q probe line causes U635C pin 7 to go low (the active T FALLING (L) signal). The delay-invert path through U635A, U635D, and U440B pulls the active low line high again. The same process occurs for a rising edge on the C/Q probe input line, causing the active low T RISING(L) signal. The T-pulse rising and falling edge output signals serve as clock pulses for the Clock Generation circuitry. The clock pulses may be gated onto the specified timebase (T) bus by the Clock Generation circuitry. Outputs from U440B are the Q-bus qualifiers that qualify the timebase selections.

Latches A15U275 and U475 in the Clock Generation circuitry output signals that are sent, along with the T and Q signals, to the OR-AND-INVERT gates A15U445, U540, and U550. These gates produce a total of six outputs. Three of these are T-signal edge indicators T1*OUT(H), T2L*OUT(H), and T2F*OUT(H). These T signals are ORed on the Interface Board with T signals from other installed acquisition cards, allowing T-bus clocks from any installed acquisition cards to contribute to the generation of the master sample clock. (When the asynchronous timebase is selected, it generates transitions onto the T1 signal line only.) The three remaining outputs are the Q-signal level indicators Q1(L), Q2F(L), and Q2L(L). The Q signals are ANDed on the Interface Board with Q signals from other installed acquisition cards.

The circuitry consisting of A15U545A and B, and U550A is used to select the current sample clock timebase, T1(H), T2F(H), or T2L(H) from the ORed T signals. When a T signal edge selected by the user in the Timebase menu occurs with its corresponding true Q signal (active low), the master sample clock CLK0(H) is generated. The CLK 0(H) signal, controlling the sampling of data in the Front End Hybrids (FEHs), latches data present on the probe CH0(H)(L)-CH8(H)(L) lines into the FEHs A15U500, U510, and U520 located in the Probe Data Interface.

TIMING AREA – TEST DESCRIPTION

The timing test consists of three routines. Routine 1 verifies setup times for T-clocks T1 and T2L and hold times for T-clocks T1, T2F, and T2L. Routine 2 verifies setup times for Q-qualifiers Q1 and Q2L and hold times for Q-qualifers Q1, Q2F, and Q2L. Routine 3 provides a functional timing test of the correlate memory circuitry. All routines require that input probes be used to connect the 9-Channel Acquisition card to the Test Pattern Generator (TPG).

NOTE

The TPG must be calibrated in order for the timing tests to pass. TPG calibration procedures are outlined as a part of the Trigger Board adjustments, in the Verification And Adjustment Procedures *section of this manual. If the TPG is suspected of being out of calibration (due to test failures), refer to these calibration procedures.*

ROUTINE 1 – TEST DESCRIPTION

This routine verifies setup times for T-clocks T1 and T2L and hold times for T-clocks T1, T2F, and T2L. First, the test determines if the acquisition probe is connected to the acquisition card. If the probe is not connected, the test reports a failure and the test is aborted. If the probe's status is returned correctly, it is assumed that the probe is also connected to the Test Pattern Generator (TPG). The 9-channel card under test is set up to acquire data from the TPG which is clocked by its local oscillator at 12 MHz. The TPG clock and data is sent via the probe to the acquisition FEH circuits. The clock is applied to a selector that uses rising or falling edges to generate T1, T2L, or T2F clocks. One of those 3 clocks will ultimately be used to generate the master sample clock, CLK 0(H). The data acquired using these clocks is compared to expected TPG data values and if a problem is detected, the failure is reported and the test is aborted.

The test begins by checking the T1 clock hold time. First, the test selects the T1 clock to be generated on the rising edge of the TPG clock. Now, the TPG data is acquired using this T1 clock. The acquired data is compared to the correct TPG pattern and if a problem is found, the test is aborted and the failure is reported.

The T1 clock setup time is tested by generating T1 on the falling edge of the TPG clock. Again, the TPG data is acquired using this T1 clock. The acquired data is compared to the correct TPG pattern and, if a problem is found, the test is aborted and the failure is reported.

Testing of the T2F clock hold time is done in the same manner by generating T2F on the rising edge of the TPG clock. The T2F setup time is not tested. Just as the others are checked, the T2L clock hold time is verified by generating T2L on the rising edge of the TPG clock. The T2L clock setup time is tested by generating T2L on the falling edge of the TPG clock. If a failure is detected during any part of the test, the test is aborted and the failure is reported.

7911 Error Index

Explanation: The probe status indicates that no probe is connected to the acquisition card.

Probable Cause	Action
The acquisition probe is improperly connected or bad.	Connect the probe if it is not connected; otherwise suspect the probe.
Defective input or output latch.	While looping on this test, use a test oscilloscope to check A15U270-6 for serial data being output. Check A15U590-11 for a clock output to the probe. Check A15U480-18 for input probe I.D. serial data.

7912 Error Index

Explanation: The acquisition circuitry failed the T1 clock hold time test.

Probable Cause	Action
The TPG is out of calibration.	Use the calibration procedure in the *Verification and Adjustment Procedures* section of this manual.
There was no T1 clock generated or the wrong clock was generated.	Check for T1 clock on pin 18 of any Front End Hybrid (A15U520, U510, or U500). Check A15U545-6 for a clock signal. Check for a clock on A15U540-3 and 5, and check A15U540-4 for a low.
Defective Front End Hybrid.	Suspect the hybrids A15U520, U510, and U500. Check the expected and actual results displayed on the screen. If the failed bit was 0, 1, or 2, then suspect A15U520. If the failed bit was 3, 4, or 5, suspect U510 and if the bit was 6, 7, or 8, then suspect hybrid U500.

7913 Error Index

Explanation: The acquisition circuitry failed the T1 clock setup time test.

Probable Cause	Action
The TPG is out of calibration.	Use the calibration procedure in the *Verification and Adjustment Procedures* section of this manual.
There was no T1 clock generated or the wrong clock was generated.	Check for T1 clock on pin 18 of any Front End Hybrid (A15U520, U510, or U500). Check A15U545-6 for a clock signal. Check for a clock on A15U540-3 and 7, and check A15U540-6 for a low.
Defective Front End Hybrid.	Suspect the hybrids A15U520, U510, and U500. Check the expected and actual results displayed on the screen. If the failed bit was 0, 1, or 2, then suspect A15U520. If the failed bit was 3, 4, or 5, suspect U510 and if the bit was 6, 7, or 8, then suspect hybrid U500.

7914 Error Index

Explanation: The acquisition circuitry failed the T2F clock hold time test.

Probable Cause	Action
The TPG is out of calibration.	Use the calibration procedure in the *Verification and Adjustment Procedures* section of this manual.
There was no T1 clock generated or the wrong clock was generated.	Check for T1 clock on pin 18 of any Front End Hybrid (A15U520, U510, or U500). Check A15U550-6 for a clock signal. Check for a clock on A15U555-3 and 5, and check A15U555-4 for a low.
Defective Front End Hybrid.	Suspect the hybrids A15U520, U510, and U500. Check the expected and actual results displayed on the screen. If the failed bit was 0, 1, or 2, then suspect A15U520. If the failed bit was 3, 4, or 5, suspect U510 and if the bit was 6, 7, or 8, then suspect hybrid U500.

7915 Error Index

Explanation: The acquisition circuitry failed the T2L clock hold time test.

Probable Cause	Action
The TPG is out of calibration.	Use the calibration procedure in the *Verification and Adjustment Procedures* section of this manual.
There was no T1 clock generated or the wrong clock was generated.	Check for T1 clock on pin 18 of any Front End Hybrid (A15U520, U510, or U500). Check A15U545-11 for a clock signal. Check for a clock on A15U540-14 and 12, and check A15U540-13 for a low.
Defective Front End Hybrid.	Suspect the hybrids A15U520, U510, and U500. Check the expected and actual results displayed on the screen. If the failed bit was 0, 1, or 2, then suspect A15U520. If the failed bit was 3, 4, or 5, suspect U510 and if the bit was 6, 7, or 8, then suspect hybrid U500.

7916 Error Index

Explanation: The acquisition circuitry failed the T2L clock setup time test.

Probable Cause	Action
The TPG is out of calibration.	Use the calibration procedure in the *Verification and Adjustment Procedures* section of this manual.
There was no T1 clock generated or the wrong clock was generated.	Check for T1 clock on pin 18 of any Front End Hybrid (A15U520, U510, or U500). Check A15U545-11 for a clock signal. Check for a clock on A15U540-14 and 10, and check A15U540-11 for a low.
Defective Front End Hybrid.	Suspect the hybrids A15U520, U510, and U500. Check the expected and actual results displayed on the screen. If the failed bit was 0, 1, or 2, then suspect A15U520. If the failed bit was 3, 4, or 5, suspect U510 and if the bit was 6, 7, or 8, then suspect hybrid U500.

ROUTINE 2 – TEST DESCRIPTION

This routine verifies setup times for Q-qualifiers Q1 and Q2L and hold times for Q-qualifiers Q1, Q2F, and Q2L. These are the Q bus signals that qualify the timebase selections. This routine requires that an input probe be used to connect the 9-Channel Acquisition card to the Test Pattern Generator (TPG).

NOTE

The TPG must be calibrated in order for the timing tests to pass. TPG calibration procedures are outlined as a part of the Trigger Board adjustments, in the Verification And Adjustment Procedures *section of this manual. If the TPG is suspected of being out of calibration (due to test failures), refer to these calibration procedures.*

First, the test determines if the acquisition probe is connected to the acquisition card. If the probe is not connected, the test reports a failure and the test is aborted. If the probe's status is returned correctly, it is assumed that the probe is also connected to the Test Pattern Generator (TPG). The 9-channel card under test is set up to acquire data from the TPG which is clocked by its local oscillator at 12 MHz. The TPG clock and data is sent via the probe to the acquisition Front End Hybrid (FEH) circuits. The clock is applied to a selector that uses rising or falling edge Q signals (Q1, Q2L, and Q2F) to qualify the generated T clocks T1, T2L, or T2F. One of the T clocks will ultimately be used to generate the master sample clock, CLK 0(H). The data acquired using these clocks is compared to expected TPG data values and if a problem is detected, the failure is reported and the test is aborted.

The test begins by checking the Q1 qualifier hold times. First, the test selects the Q1L qualifier and the T1R clock to be generated on the rising edge of the TPG clock. Now, the TPG data is acquired using this T1R clock. The acquired data is compared to the correct TPG pattern and, if a problem is found, the test is aborted and the failure is reported.

The Q1 qualifier setup time is tested by generating the Q1H qualifier and the T1F clock on the falling edge of the TPG clock. Again, the TPG data is acquired using this T1F clock. The acquired data is compared to the correct TPG pattern and, if a problem is found, the test is aborted and the failure is reported.

Testing of the Q2F qualifier hold times is done in the same manner by generating the Q2FL qualifier and the T2FR clock on the rising edge of the TPG clock. The Q2F qualifier setup time is not tested. Just as the others are checked, the Q2L clock hold times are verified by generating the Q2LH qualifier and T2LR clock on the rising edge of the TPG clock. The Q2L qualifier setup times are tested by generating the Q2LL qualifier and the T2LF clock on the falling edge of the TPG clock. If a failure is detected during any part of the test, the test is aborted and the failure is reported.

7921 Error Index

Explanation: The probe status indicates that no probe is connected to the acquisition card.

Probable Cause	Action
The acquisition probe is improperly connected or bad.	Connect the probe if it is not connected; otherwise suspect the probe.
Defective input or output latch.	While looping on this test, use a test oscilloscope to check A15U270-6 for serial data being output. Check A15U590-11 for a clock output to the probe. Check A15U480-18 for input probe I.D. serial data.

7922 Error Index

Explanation: The acquisition circuitry failed the Q1 qualifier hold time test.

Probable Cause	Action
The TPG is out of calibration.	Use the calibration procedure in the *Verification and Adjustment Procedures* section of this manual.
There was no clock generated or the wrong clock was generated.	Check for clock on pin 18 of any Front End Hybrid (A15U520, U510, or U500). Check A15U545-6 and 7 for a clock signal. Check for a clock on A15U445-3 and 5, and check A15U445-4 for a low.
Defective Front End Hybrid.	Suspect the hybrids A15U520, U510, and U500. Check the expected and actual results displayed on the screen. If the failed bit was 0, 1, or 2, then suspect A15U520. If the failed bit was 3, 4, or 5, suspect U510 and if the bit was 6, 7, or 8, then suspect hybrid U500.

7923 Error Index

Explanation: The acquisition circuitry failed the Q1 qualifier setup time test.

Probable Cause	Action
The TPG is out of calibration.	Use the calibration procedure in the *Verification and Adjustment Procedures* section of this manual.
There was no clock generated or the wrong clock was generated.	Check for clock on pin 18 of any Front End Hybrid (A15U520, U510, or U500). Check A15U545-6 and 7 for a clock signal. Check for a clock on A15U445-3 and 7, and check A15U445-6 for a low.
Defective Front End Hybrid.	Suspect the hybrids A15U520, U510, and U500. Check the expected and actual results displayed on the screen. If the failed bit was 0, 1, or 2, then suspect A15U520. If the failed bit was 3, 4, or 5, suspect U510 and if the bit was 6, 7, or 8, then suspect hybrid U500.

7924 Error Index

Explanation: The acquisition circuitry failed the Q2F qualifier hold time test.

Probable Cause	Action
The TPG is out of calibration.	Use the calibration procedure in the *Verification and Adjustment Procedures* section of this manual.
There was no clock generated or the wrong clock was generated.	Check for clock on pin 18 of any Front End Hybrid (A15U520, U510, or U500). Check A15U550-6 and 7 for a clock signal. Check for a clock on A15U555-12 and 14, and check A15U555-13 for a low.
Defective Front End Hybrid.	Suspect the hybrids A15U520, U510, and U500. Check the expected and actual results displayed on the screen. If the failed bit was 0, 1, or 2, then suspect A15U520. If the failed bit was 3, 4, or 5, suspect U510 and if the bit was 6, 7, or 8, then suspect hybrid U500.

7925 Error Index

Explanation: The acquisition circuitry failed the Q2L clock hold time test.

Probable Cause	Action
The TPG is out of calibration.	Use the calibration procedure in the *Verification and Adjustment Procedures* section of this manual.
There was no clock generated or the wrong clock was generated.	Check for clock on pin 18 of any Front End Hybrid (A15U520, U510, or U500). Check A15U545-10 and 11 for a clock signal. Check for a clock on A15U445-14 and 12, and check A15U445-13 for a low.
Defective Front End Hybrid.	Suspect the hybrids A15U520, U510, and U500. Check the expected and actual results displayed on the screen. If the failed bit was 0, 1, or 2, then suspect A15U520. If the failed bit was 3, 4, or 5, suspect U510 and if the bit was 6, 7, or 8, then suspect hybrid U500.

7926 Error Index

Explanation: The acquisition circuitry failed the Q2L qualifer setup time test.

Probable Cause	Action
The TPG is out of calibration.	Use the calibration procedure in the *Verification and Adjustment Procedures* section of this manual.
There was no clock generated or the wrong clock was generated.	Check for clock on pin 18 of any Front End Hybrid (A15U520, U510, or U500). Check A15U545-10 and 11 for a clock signal. Check for a clock on A15U445-14 and 10, and check A15U445-11 for a low.
Defective Front End Hybrid.	Suspect the hybrids A15U520, U510, and U500. Check the expected and actual results displayed on the screen. If the failed bit was 0, 1, or 2, then suspect A15U520. If the failed bit was 3, 4, or 5, suspect U510 and if the bit was 6, 7, or 8, then suspect hybrid U500.

ROUTINE 3 – TEST DESCRIPTION

This routine provides a functional test of the correlate memory circuitry and the T-bus clocks at 12 MHz. The test requires that an input probe be used to connect the 9-Channel Acquisition card to the Test Pattern Generator (TPG).

NOTE

The TPG must be calibrated in order for the timing tests to pass. TPG calibration procedures are outlined as a part of the Trigger Board adjustments, in the Verification And Adjustment Procedures *section of this manual. If the TPG is suspected of being out of calibration (due to test failures), refer to these calibration procedures.*

The Storage RAM Timing circuitry contains a dual one-of-four selector, A15U455, that produces two outputs based on the pin 7 (active when using timebase T2) and pin 9 (active when using timebase T1) select lines. One output at U445-15 is correlation data from the Trigger Board's COR1(H) or COR2(H) inputs. These signals, changed to COR D(H) and COR G(H), carry the data and glitch correlation information that is stored with the incoming probe data in the Storage RAMs. (The correlation information is used when reconstructing data for display if two asynchronous timebases were used during the acquisition.) The correlation information is stored in Storage RAM memory as CCOR1*(H) and CCOR2*(H) after passing through the Data Chain Interface. These signals are also the correlation chaining signals that carry correlation information to the next acquisition card in the chain.

The Storage RAM Data Readback circuitry converts the serial data from the Storage RAMs into parallel information. The Control Processor may then read the data via the Acquisition-Control Processor Interface.

This test begins by checking that an acquisition probe is connected to the acquisition board. The test assumes that the probes are connected to the Test Pattern Generator (TPG). The TPG is run by its local oscillator, operating at a frequency of 12 MHz. The acquisition memory is clocked by the T1 clock and T2 clock in demux clock mode.

The acquisition card is programmed to generate a T1 clock on the falling edge of the TPG clock, T2F on the rising edge of the TPG clock, and T2L on the falling edge of the TPG clock. The correlation bit is stored by the T2L clock. After the acquisition is complete, the 512 locations of correlation data are compared to expected data. If problems are detected, the test is aborted and the failure is reported.

The next part of the test requires that the acquisition card be re-programmed to generate the T1 clock on the rising edge of the TPG clock, T2F on the falling edge of the TPG clock, and T2L on the rising edge of the TPG clock. The correlation bit is stored by the T1 clock. After the acquisition is complete, the 512 locations of correlation data are compared to expected data. If problems are detected, the test is aborted and the failure is reported.

7931 Error Index

Explanation: The probe status indicates that no probe is connected to the acquisition card.

Probable Cause	Action
The acquisition probe is improperly connected or bad.	Connect the probe if it is not connected; otherwise suspect the probe.
Defective input or output latch.	While looping on this test, use a test oscilloscope to check A15U270-6 for serial data being output. Check A15U590-11 for a clock output to the probe. Check A15U480-18 for input probe I.D. serial data.

7932 Error Index

Explanation: The acquired data did not match the expected data.

Probable Cause	Action
Defective acquisition probe.	Replace the probe and run this test again.
Defective acquisition memory or data path.	While looping on this test, check for toggling signal on A15U335-10 and 13. If these points are not toggling, suspect U335, U455, and U550B. Also while looping, check for toggling signal on A15U135-18. If this point is not toggling, suspect U135. (It may be necessary to use a logic analyzer to check for the toggling signals.)
Timing malfunction; incorrect write clock to the acquisition memory.	With the test stopped on the failure, check A15U455 for a high on pin 9 and a low on pin 7. While looping on this test, check for a signal on A15U455-4.

7933 Error Index

Explanation: The acquired data did not match the expected data.

Probable Cause	Action
Defective acquisition memory or data path.	While looping on this test, check for toggling signal on A15U320-10 and 13. If these points are not toggling, suspect U320 or U455. Also while looping, check for toggling signal on A15U120-7. If this point is not toggling, suspect U120. (It may be necessary to use a logic analyzer to check for the toggling signals.)
Timing malfunction; incorrect write clock to the acquisition memory.	With the test stopped on the failure, check A15U455 for a low on pin 9 and a high on pin 7. While looping on this test, check for a signal on A15U455-5.

module: 1240D1-X
area: CAL ACQ9

1240D1 CAL ACQ9 TEST DESCRIPTION

The 9-channel acquisition calibrate test (routine 1) helps in the testing and calibration of the 9-channel's threshold circuitry. This circuitry produces the variable threshold voltages for the acquisition probe. The digital-to-analog convertor (DAC), A15U175, latches and translates data sent by the Control Processor as threshold voltage changes (50 mV change per bit). The total voltage range is from +6.35 volts to −6.35 volts.

NOTE

This routine requires that the operator observe test results with external equipment to determine if the threshold circuitry is properly calibrated. The procedure described in the following should only be used for verifying circuit operation. If precise calibration of the threshold circuitry is required, refer to the 1240D1 calibration procedures in the Verification and Adjustment Procedures *section of this manual.*

1240 SETUP FOR THRESHOLD CALIBRATION TEST

1. With the 1240 powered-down, access the 1240D1 acquisition board according to the instructions provided in the *Disassembly and Installation Procedures* section of this manual.
2. Set a multimeter to the 10 or 20 volt dc range and connect the high (+) lead to A15TP185, low (−) lead to A15TP291.
3. Power up the 1240 and enter diagnostics by simulating a keyboard failure (hold down a key during power-up).
4. Using the SELECT keys or the KNOB, choose the 1240D1-X module and touch the MODULE DIAGNOSTIC soft key. (The X designation indicates one of four possible 9-channel acquisition boards under test.)
5. Choose the CAL ACQ9 area and touch the AREA DIAGNOSTICS soft key.
6. Choose the Routine 1 test and press the START key.
7. With the threshold setting at 0.00 volts, verify that the multimeter reading is 0.00 volts ± 24 mV.
8. Using the SELECT keys or the KNOB, choose +6.35 volts for the probe threshold voltage and verify the reading on the multimeter is +6.35 volts ± 24 mV.
9. Now, choose −6.35 volts for the probe threshold voltage and verify the reading on the multimeter is −6.35 volts ± 24 mV.

CAL ACQ9 - ROUTINE 1 TEST RESULTS

Explanation: One of the measured voltages was incorrect by more than 24 mV.

Probable Cause	Action
Defective threshold circuit.	Suspect the DAC A15U175 if the measured voltage was more than 24 mV.

8XXX 18-CHANNEL ACQUISITION ERROR INDEXES

Error Index	Area Name	Area Number
81XX	THRESHOLD	AREA 1
82XX	ACQ RAM	AREA 2
83XX	MAP	AREA 3
84XX	X ACQ RAM	AREA 4
85XX	WORD REC	AREA 5
86XX	CHAINING	AREA 6
87XX	CALIBRATE	AREA 7
88XX	TIMING	AREA 8

18-CHANNEL ACQUISITION MANUAL TESTS

Module	Area	Routine	Description
1240D2	CAL ACQ18	1	Calibrate Threshold
	CAL ACQ18	2	Calibrate Gate Arrays

1240D2 18-CHANNEL BLOCK DIAGRAM
THRESHOLD – AREA 1

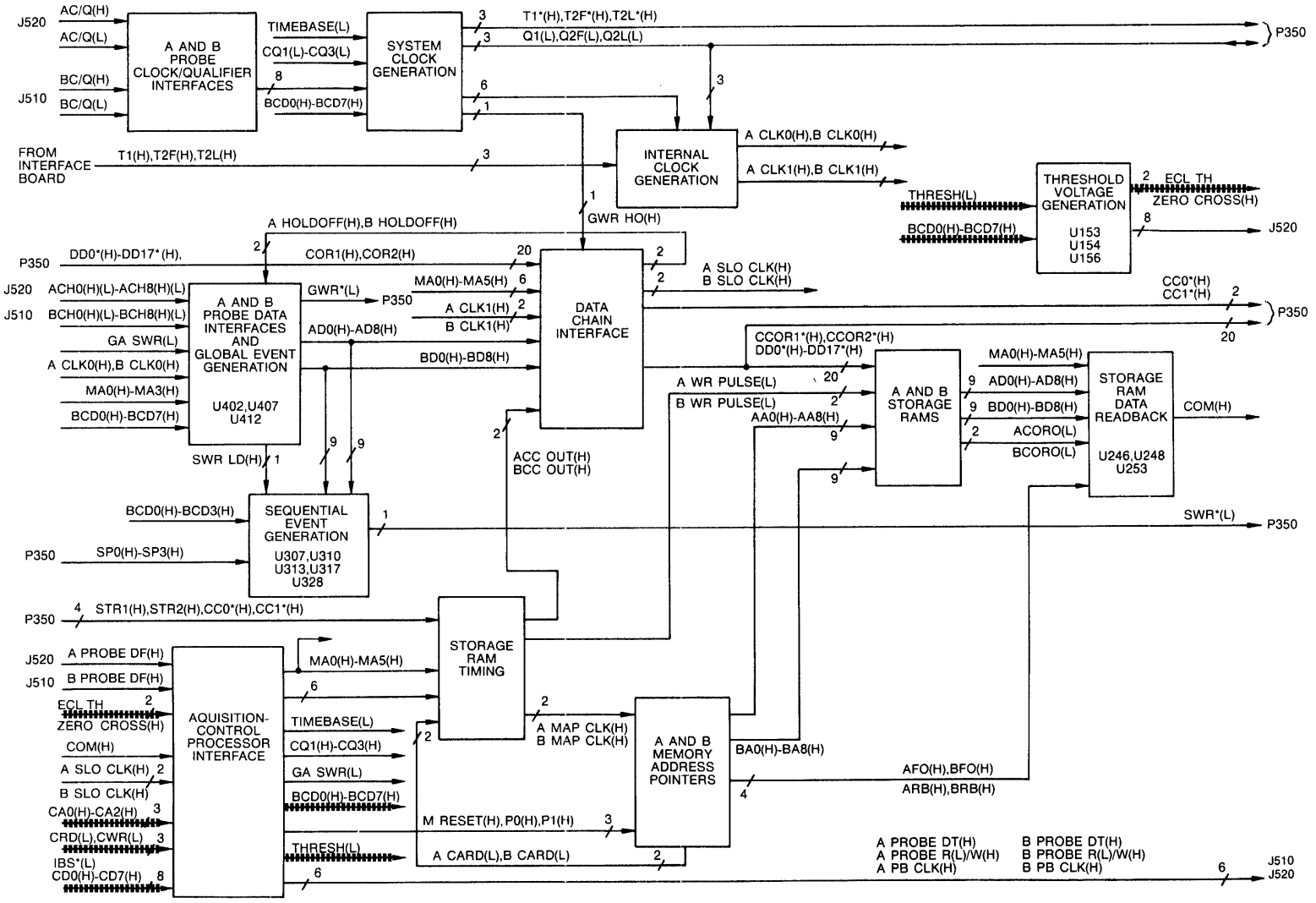


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Figure 8-115. 18-Channel THRESHOLD block diagram.

1240D2 18-CHANNEL ACQUISITION BOARD – COMPONENT LOCATION

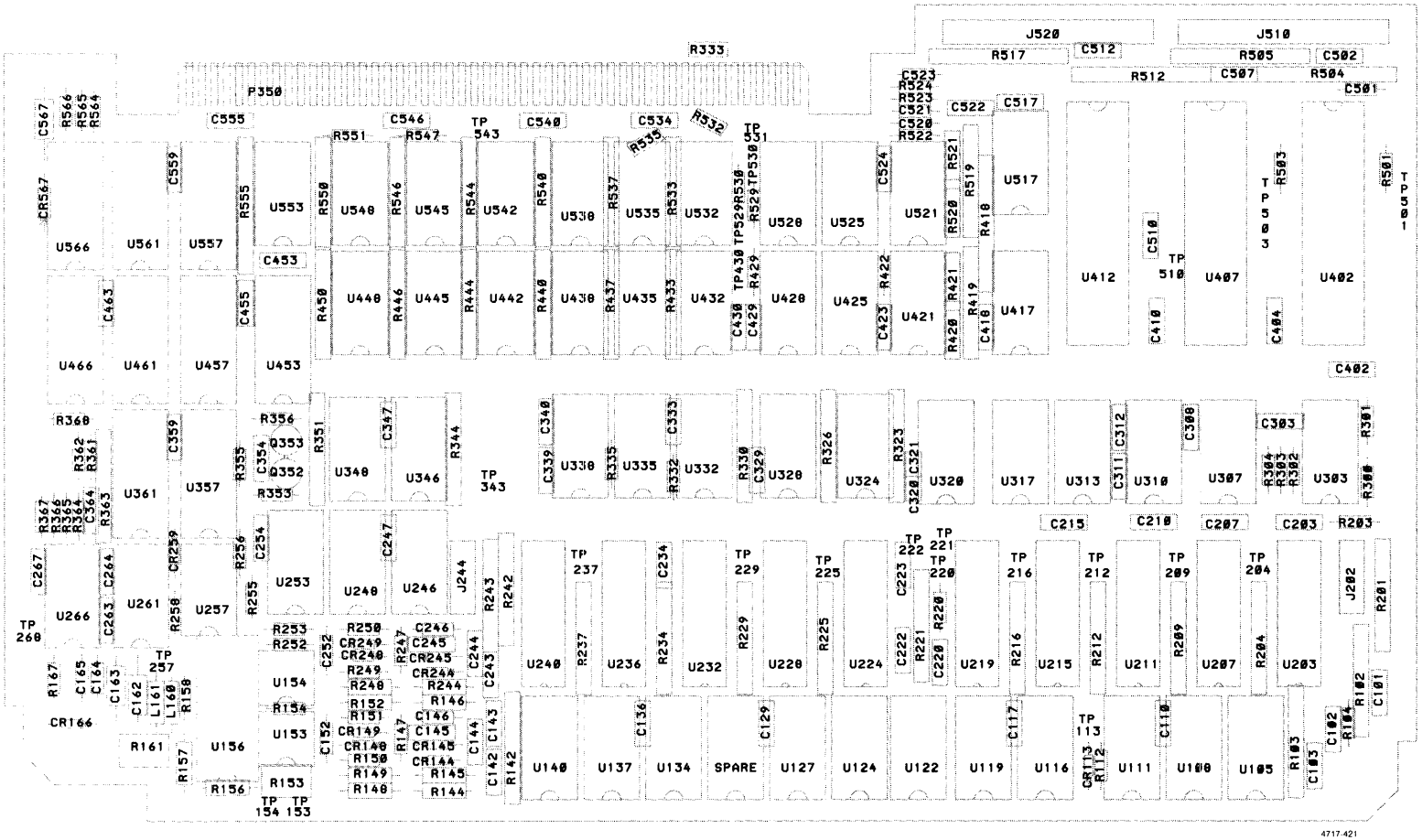

Figure 8-116. 18-Channel Acquisition Board component location.

module: 1240D2-X
area: THRESHOLD

THRESHOLD AREA – CIRCUIT OVERVIEW

The pattern-shaded signal lines on the threshold block diagram indicate circuitry used during diagnostic testing. Only the circuitry that is being exercised for the first time during diagnostic testing is shown. Circuitry exercised by other diagnostic tests are shown in their respective block diagrams.

The Control Processor links its CD data bus to the 18-Channel Acquisition's BCD data bus through the Acquisition-Control Processor Interface. The Control Processor uses this link for loading a user-specified voltage level into the Threshold Voltage Generation circuitry. Here, the voltage-level information is converted into a probe threshold voltage for both A- and B-side probes.

A16U557 is a bidirectional buffer that gates the Control Processor's CD data onto the acquisition card's BCD data bus. A16U553 decodes the THRESH(L) signal from Control Processor address and control lines. This is the load enable signal used during write operations to the Threshold Voltage Generation circuitry.

The digital-to-analog convertor, A16U156, latches and translates the data on BCD0(H)-BCD7(H). Operational amplifiers A16U153A and B produce the A-side threshold voltages, while A16U154A and B produce the B-side threshold voltages. Each bit change produces a 50 mV threshold voltage change, with a total range from +6.35 volts to – 6.35 volts.

A16U226A is a zero crossing detector that produces the ZERO CROSS(H) signal. This signal, when activated, indicates that the threshold voltage has reached a 0 volt level. The ZERO CROSS(H) signal is used during the diagnostic testing of the threshold circuitry. The Control Processor reads back the state of the zero crossing indicator through register A16U561 in the Acquisition-Control Processor Interface.

THRESHOLD AREA – TEST DESCRIPTION

This test checks the digital-to-analog convertor (DAC) that is used to produce probe threshold voltages for both A- and B-side probes. The test writes values 01_{hex} through FF_{hex} to the DAC A16U156 while monitoring the ZERO CROSS(H) signal from comparator A16U266A. When the DAC reaches the zero crossing point, comparator U266A switches its output polarity. The ZERO CROSS(H) signal reflects this polarity change, thereby indicating to the diagnostics that the DAC output can be set to both positive and negative threshold values.

8111 Error Index

Explanation: The comparator, A16U266A, indicated that the DAC output was above 0 volts when it should have been below 0 volts.

Probable Cause	Action
Bad DAC A16U156.	While looping on this test, connect a test oscilloscope probe to A16TP268 (ground to A16TP257). The waveform observed should be a sawtooth ramp from −6.35 V up to +6.35 V.
Bad comparator A16U266A.	While looping on this test, connect a test oscilloscope probe to A16U266-3 (ground to A16TP257). The voltage output at pin 3 should change when the DAC output crosses 0 volts.

8112 Error Index

Explanation: The comparator, A16U266A, indicated that the DAC output was below 0 volts when it should have been above 0 volts.

Probable Cause	Action
Bad DAC A16U156.	While looping on this test, connect a test oscilloscope probe to A16TP268 (ground to A16TP257). The waveform observed should be a sawtooth ramp from −6.35 V up to +6.35 V.
Bad comparator A16U266A.	While looping on this test, connect a test oscilloscope probe to A16U266-3 (ground to A16TP257). The voltage output at pin 3 should change when the DAC output crosses 0 volts.

1240D2 18-CHANNEL BLOCK DIAGRAM
ACQ RAM – AREA 2

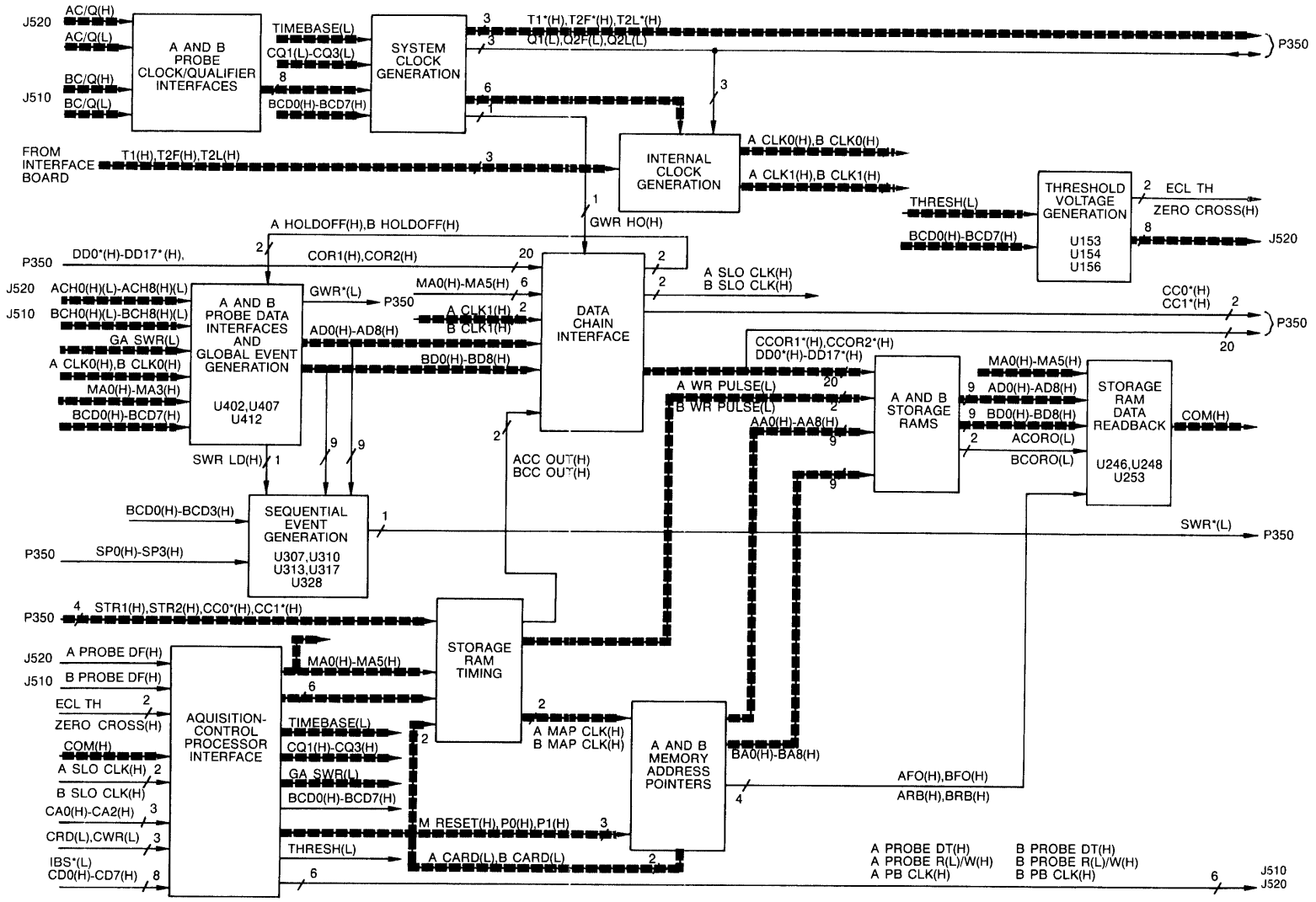

Figure 8-117. 18-Channel ACQ RAM block diagram.

4342-139

1240D2 18-CHANNEL ACQUISITION BOARD – COMPONENT LOCATION

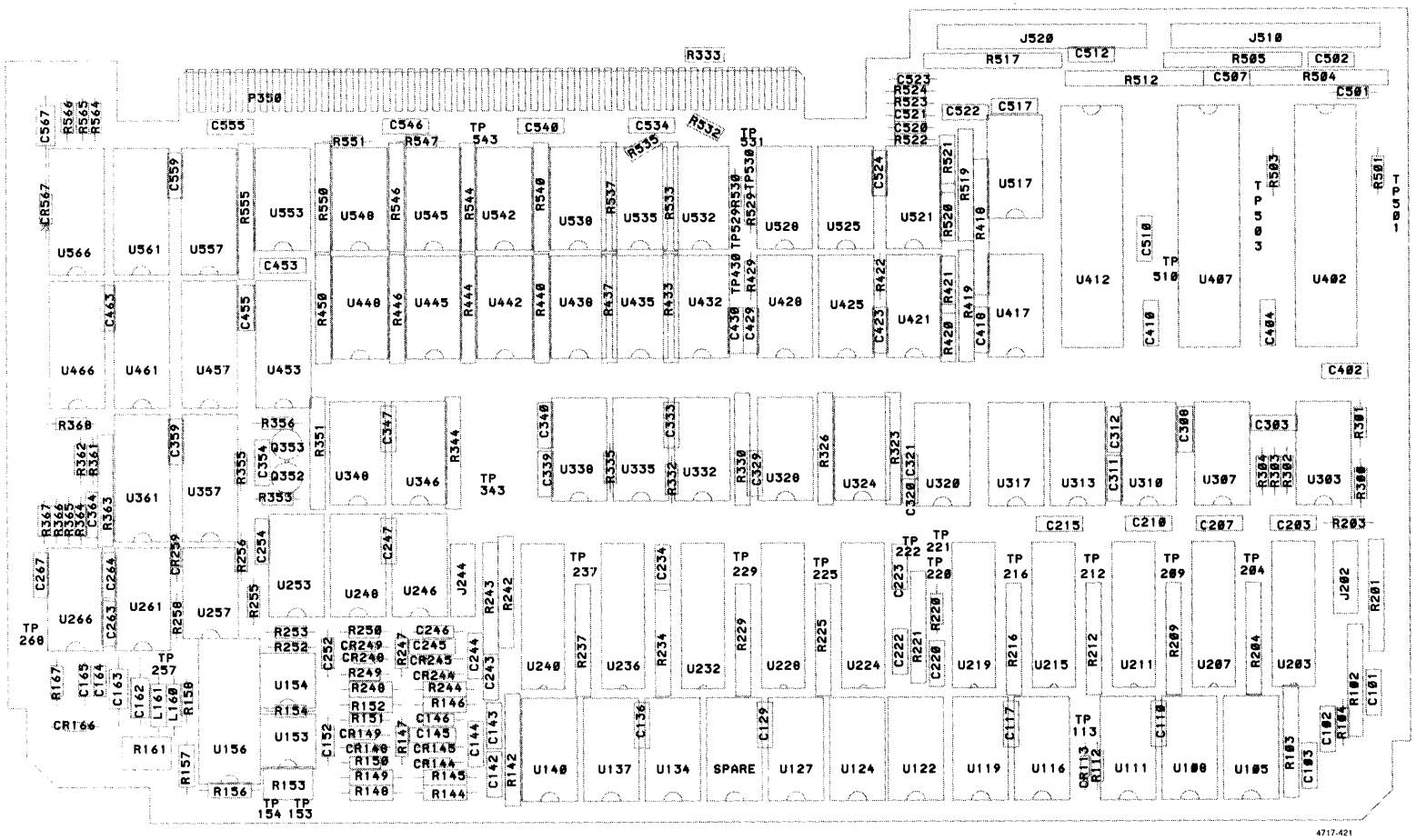

Figure 8-118. 18-Channel Acquisition Board component location.

module: 1240D2-X
area: ACQ RAM

ACQ RAM AREA – CIRCUIT OVERVIEW

The pattern-shaded signal lines on the acquisition RAM block diagram indicate circuitry used during diagnostic testing. Only the circuitry that is being exercised for the first time during diagnostic testing is shown. Circuitry exercised by other diagnostic tests are shown in their respective block diagrams. Most of the 18-channel's function blocks are required to support the storing of data into acquisition RAM. The A- and B-side circuits are duplicates of each other; therefore, circuitry discussion may exclude references to the B side.

The A and B Probe Data Interfaces accept 18 differential ECL-level channels from both A and B probes. These channels carry probe data to the gate arrays A16U412, U407, and U402. The gate arrays provide a sample latch for probe data. The latched data is sent through the Data Chain Interface and into the A and B Storage RAMs.

The Internal Clock Generation circuitry is used to produce the AT2LF clock signals for both A- and B-sides of the Probe Data Interface. The A CLK0(H) master sample clock latches data into the gate arrays A16U412, U407, and U402. The A CLK1(H) signal clocks the A-side probe data into the Data Chain Interface.

The Data Chain Interface consists of two sets of data latches. The probe data latches A16U438, U442, U445, and U448 accept data from the Probe Data Interface for both A and B probes. Output from these latches is available for either the storage RAMs or the data chain bus if chaining is in progress.

The Storage RAM Timing circuitry generates timing and control signals used during the storage and retrieval of data in the Storage RAM. Trigger Board master-storage signal STR2(H) is used with timebase 2. The OR-AND-INVERT package A16U332 produces the timing signals used to generate the A storage RAM write signal A WR PULSE(L). A16U346C produces a clock signal A MAP CLK(H) used to increment circuitry in the Memory Address Pointer.

The Memory Address Pointer creates addresses for the Storage RAM during storage and retrieval of data. These values also serve as memory address pointer (MAP) values used by the control processor when reconstructing data.

The Storage RAMs consist of two sections with five ECL static RAMs per section. Five RAMs (each 2 bits x 512 locations) hold A-probe data and the remaining five RAMs hold the B-probe data.

The Storage RAM Data Readback circuitry multiplexes the ECL-level data from the storage RAMs for serial output to the Acquisition-Control Processor Interface. Multiplexers A16U246, U253, and U248 select outputs from the A-and B-side storage RAMs, as well as memory address pointer outputs and correlation data. The ECL-level serial information is converted to TTL-level parallel information in the Acquisition-Control Processor Interface.

ACQ RAM AREA – TEST DESCRIPTION

This test provides a functional check of the acquisition RAM circuitry. The test, run at processor speed, was not designed to isolate specific acquisition failures. Moreover, the test checks the operational status of the acquisition circuitry as a system. Other acquisition circuitry checks may be performed with the 18-Channel's X ACQ RAM (area 4) tests.

The test first determines if the A- and B-side probes are connected to the acquisition card. If the probes are not connected, the test reports a failure and the test is aborted. Next, the test acquires data from the Test Pattern Generator (TPG). Data is stored in both A- and B-sides of acquisition RAM. The A-side of RAM is checked to determine if it contains the correct data. If the A-side data is correct, then the B-side of RAM is checked for correct data. Failures detected during the diagnostics are reported on the 1240 display screen.

8211 Error Index

Explanation: The test failed to detect both A- and B-side acquisition probes.

Probable Cause	Action
One or both of the acquisition probes is improperly connected or bad.	Examine the expected and actual results. If the expected data is 00 and the actual data is 40, then suspect the A-side probe. If the expected data is 00 and the actual data is 80, then suspect the B-side probe.
Bad latch A16U457.	While looping on this test, use a test oscilloscope to check A16U457-9 for low-going pulses.
Bad buffer A16U561.	While looping on this test, use a test oscilloscope to check A16U561-1 for low-going pulses and pins 8 and 12 for high-going pulses. If necesary, check A16U348 for correct operation.

8212 Error Index

Explanation: The A side of the acquisition memory failed.

Probable Cause	Action
Defective data lines in the acquisition probe.	Verify the A-side probe's operational status by swapping it with the B-side probe and running the test again. If the failure shows up on the B side, suspect the probe under test.
No Front End Hybrid clock.	Check the expected and actual results. If the expected result is $01FF_{hex}$ or $01BE_{hex}$, suspect a clock failure. (Refer to the *Operating Information* section for TPG output patterns.) While looping on this test, use a test oscilloscope to check A16U412-32 and A16U438-9 for a clock signal. If the clock is not present, check A16TP530 for a clock and A16U525-6 for a logic low.
No storage clock.	While looping on this test, use a test oscilloscope to check A16U108-2 for a logic high with a low-going 10 ns clock pulse. If no clock pulse is present, check A16U332-5 for a low. If a low is present, verify that U332-6 is a logic high with a low-going 10 ns clock.
A problem exists between the gate arrays (the front end hybrids) and the acquisition memory.	Check the expected and actual data to determine the word that was incorrectly acquired.

8213 Error Index

Explanation: The B side of the acquisition memory failed.

Probable Cause	Action
Defective data lines in the acquisition probe.	Verify the probe's operational status by substituting this probe with a known good probe or by moving this probe to the A side and running the test again. If the failure shows up on the A side, suspect the probe.
No Front End Hybrid clock.	Check the expected and actual results. If the expected result is $01FF_{hex}$ or $01F7_{hex}$, suspect a clock failure. (Refer to the *Operating Information* section for TPG output patterns.) While looping on this test, use a test oscilloscope to check A16U412-9 and A16U445-9 for a clock signal. If the clock is not present, check A16TP530 for a clock and A16U525-11 for a logic low.
No storage clock.	While looping on this test, use a test oscilloscope to check A16U137-2 for a logic high with a low-going 10 ns clock pulse. If no clock pulse is present, check A16U335-5 for a low. If a low is present, verify that U335-6 is a logic high with a low-going 10 ns clock.
A problem exists between the gate arrays (the front end hybrids) and the acquisition memory.	Check the expected and actual data to determine the word that was incorrectly acquired.

1240D2 18-CHANNEL BLOCK DIAGRAM
MAP – AREA 3

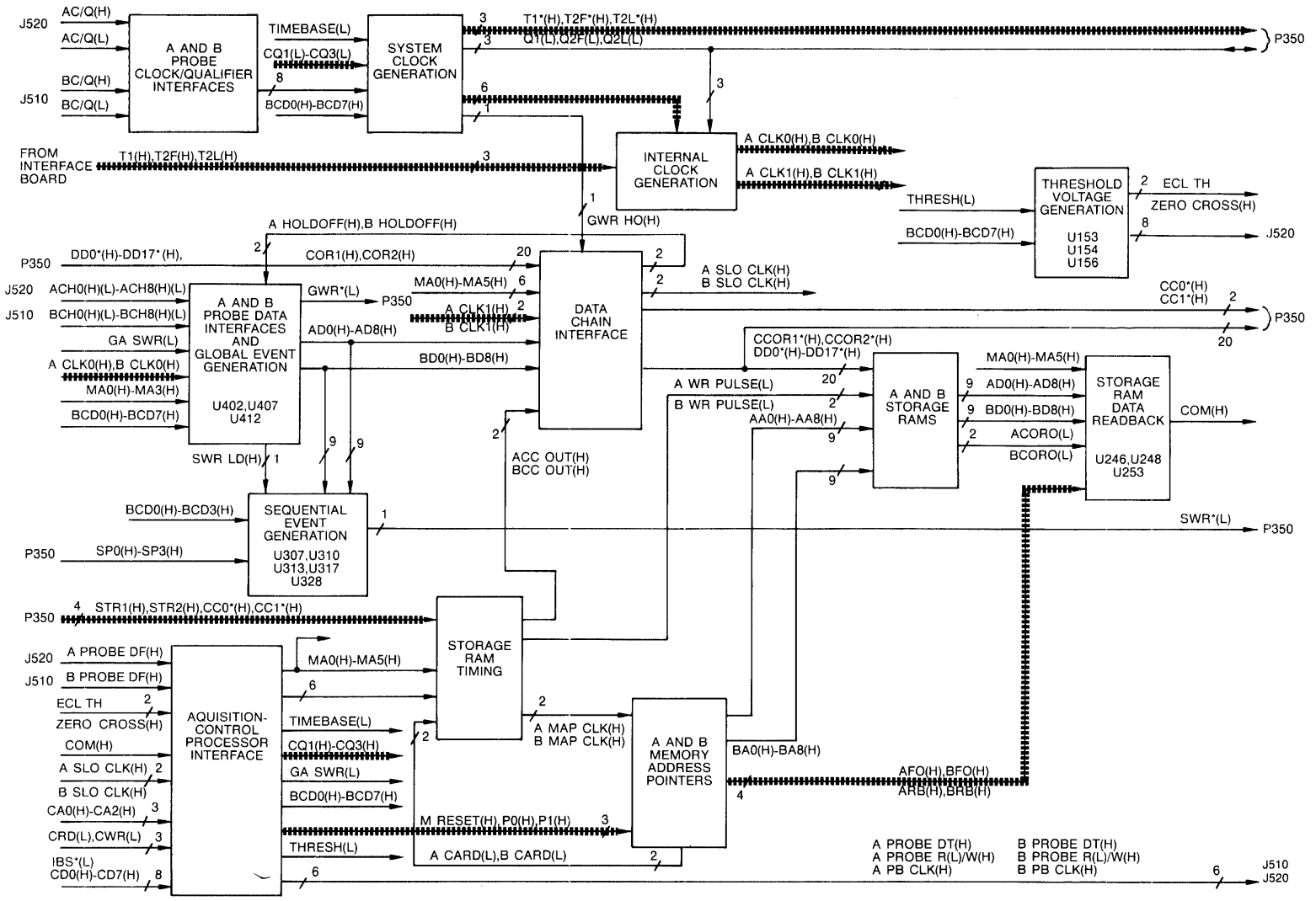

Figure 8-119. 18-Channel MAP block diagram.

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1240D2 18-CHANNEL ACQUISITION BOARD – COMPONENT LOCATION

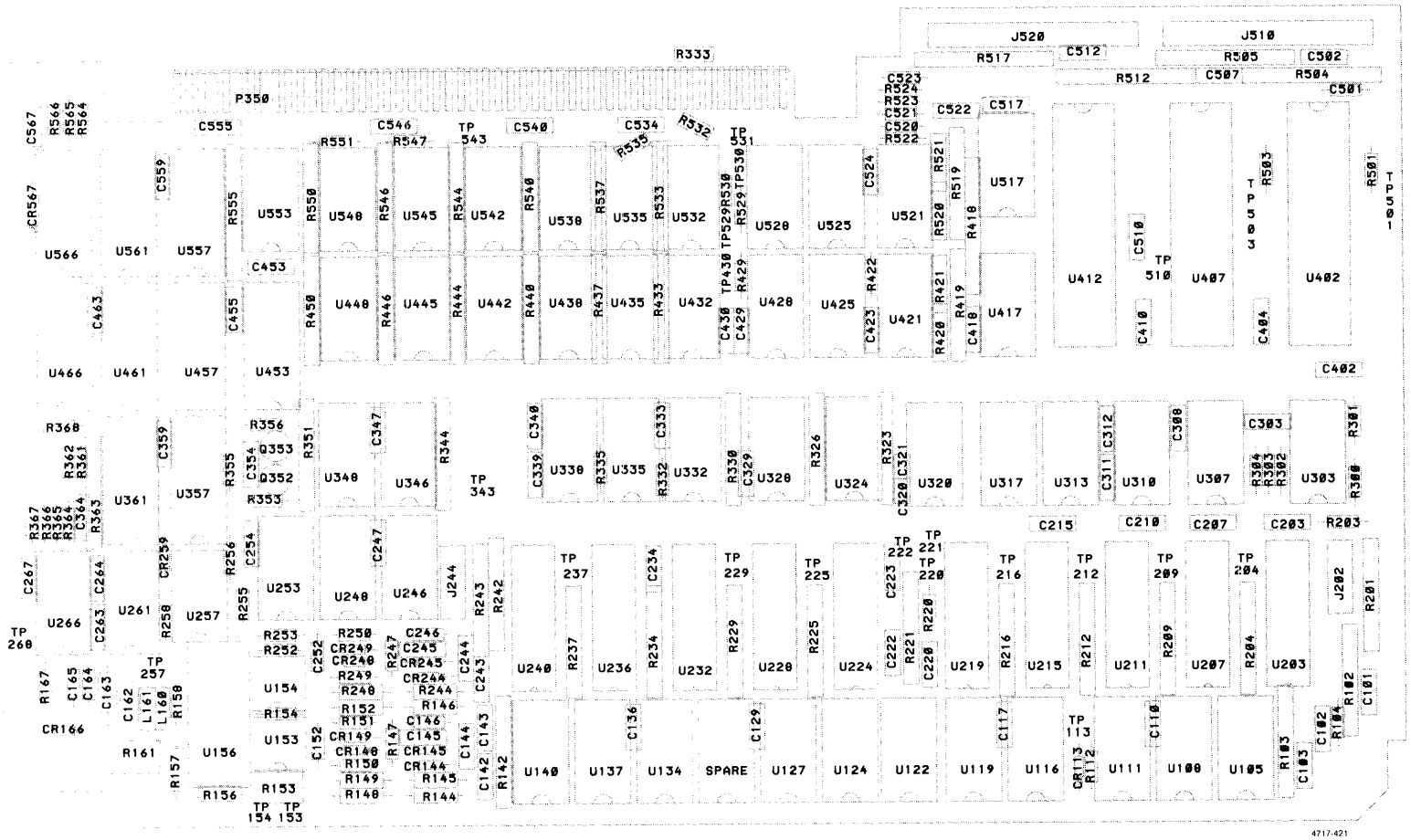


Figure 8-120. 18-Channel Acquisition Board component location.

module: 1240D2-X
area: MAP

MAP AREA – CIRCUIT OVERVIEW

The pattern-shaded signal lines on the Memory Address Pointer (MAP) block diagram indicate circuitry used during diagnostic testing. Only the circuitry that is being exercised for the first time during diagnostic testing is shown. Circuitry exercised by other diagnostic tests are shown in their respective block diagrams. The A- and B-side circuits are duplicates of each other; therefore, circuitry discussion may exclude references to the B side.

The MAP circuitry creates addresses for the Storage RAM during storage and retrieval of data. These addresses also serve as memory address pointers for the Control Processor when it reconstructs data for display.

Three 4-bit counters A16U119, U116, and U111 form the addresses for the A-side Storage RAM. Counters A16U119 and U116 form a ripple count on address lines AA0(H)-AA7(H). The terminal count from A16U116 enables the third counter, A16U111. As the count is produced on the remaining address lines, a comparison to the chain depth indicators P0(H) and P1(H) is made by A16U124A and D. If the indicators are set to 00 (no cards chained), the logic causes the counter to output an active AFO(H) signal (A-side filled once) when the first acquisition card is filled with data. If the chain depth indicators were set to 11 (binary code indicating four cards chained), the filled once signal would become active on this card after all four cards in the acquisition chain were filled. The ARB(H) signal (A-side MAP readback bit) is used in determining the oldest/newest data boundary in memory.

The Storage RAM Data Readback circuitry multiplexes the ECL-level data from the storage RAMs for serial output to the Acquisition-Control Processor Interface. Multiplexers A16U246, U253, and U248 select outputs from the A-and B-side storage RAMs, as well as memory address pointer outputs and correlation data. The COM(H) signal line carries the ECL-level serial information to the the ECL-to-TTL convertor A16U266B in the Acquisition-Control Processor Interface. A16U361 converts the serial data to parallel data for readback by the Control Processor.

MAP AREA – TEST DESCRIPTION

The MAP area tests are divided into three routines. Routine 1 and 2 tests verify the A- and B-side MAP circuits, respectively, through their entire address range. These routines also verify the portions of MAP circuitry responsible for data storage and retrieval on the second, third, and fourth acquisition cards. (These cards need not be installed for the test to run.) Routine 3 verifies the operation of both A- and B-sides while being driven by the T1 clock.

ROUTINE 1 DESCRIPTION

This test verifies the operation of the A-side Memory Address Pointer (MAP) circuitry. The ARB(H) A MAP readback bit is initially reset to return a 00_{hex} readback value. During the test, the A MAP readback status information is read $3F_{hex}$ times from A16U253. Each read increments the MAP counter by eight. Each time the information is read back, the test expects the A MAP readback bit to return a value of 00_{hex}. If the bit is not reset during any of these read operations, the test is aborted and a failure is reported. When the bit has been read back $3F_{hex}$ times, the final MAP count should be $1FF_{hex}$. The test reads the serial information on the the ARB(H) signal line once again, this time expecting a bit to be set. If the information read back does not indicate a bit was set, the test is aborted and a failure is reported.

Now, the A- and B-side MAP clocks are disabled and the AFO(H) signal (A-side MAP filled once) is selected to be read from A16U253. The test performs two more reads. The first read clears the unwanted data from A16U361. The second read returns status information on the AFO(H) signal line. The test expects to read FF_{hex} since both MAP clocks have been disabled and the MAP was not incremented.

Next, the A-side MAP circuitry is programmed to address two acquisition cards. The A MAP readback status information is read $7F_{hex}$ times from A16U253. The final MAP count should be $3F7_{hex}$. The test sequence is the same as previously described.

If no failures are detected, the MAP circuitry is programmed to address three acquisition cards. The A MAP readback status information is read BF_{hex} times from A16U253. The final MAP count should be $5F7_{hex}$. The test sequence is the same as previously described.

Finally, if no failures are detected the MAP circuitry is programmed to address four acquisition cards. The A MAP readback status information is read FF_{hex} times from A16U253. The final MAP count should be $7F7_{hex}$. The test sequence is the same as previously described.

8311 Error Index

Explanation: The ARB(H) A MAP readback bit was set before the MAP counter reached $1FF_{hex}$.

Probable Cause	Action
Suspect A16U253, U461, U119, U116, U111, U108B, U105C and D, U124A and D. The value in the result address field is the value the MAP counter reached before the set bit was read from the ARB(H) line.	Refer to the appropriate schematic and analyze these components while looping on this routine test. Check for a clock on pin 13 of A16U111, U116, and U119. Check for stuck logic high or low on U108. Also, check for low on U461-2,19.

8312 Error Index

Explanation: The ARB(H) A MAP readback bit should have been set high, but it was not read back as being set.

Probable Cause	Action
Suspect A16U253, U461, U119, U116, U111, U108B, U105C and D, U124A and D.	Refer to the appropriate schematic and analyze these components while looping on this routine test. Check for a clock on pin 13 of A16U111, U116, and U119. Check for stuck logic high or low on U108. Also, check for low on U461-2,19.

8313 Error Index

Explanation: The AFO(H) A MAP filled once readback bit should have been set high, but it was not read back as being set.

Probable Cause	Action
Suspect A16U253, U461, U119, U116, U111, U108B, U105C and D, U124A and D.	Refer to the appropriate schematic and analyze these components while looping on this routine test. Check for a clock on pin 13 of A16U111, U116, and U119. Check for stuck logic high or low on U108. Also, check for low on U461-2,19.

8314 Error Index

Explanation: The ARB(H) A MAP readback bit was set before the MAP counter reached $3F7_{hex}$. If a problem exists but the first three error indexes pass, the problem is most likely in the counters or the P0(H) and P1(H) lines.

8312
8313
8314

Probable Cause	Action
Suspect A16U253, U461, U111, U108B, U105C and D, U124A and D. The value in the result address field is the value the MAP counter reached before the set bit was read from the ARB(H) line.	Refer to the appropriate schematic and analyze these components while looping on this routine test. Check for a clock on pin 13 of A16U111, U116, and U119. Check for stuck logic high or low on U108. Also, check for low on U461-19 and high on U461-2.

8315 Error Index

Explanation: The ARB(H) A MAP readback bit should have been set high, but it was not read back as being set.

Probable Cause	Action
Suspect A16U253, U461, U111, U108B, U105C and D, U124A and D. The value in the result address field is the value the MAP counter reached before the set bit was read from the ARB(H) line.	Refer to the appropriate schematic and analyze these components while looping on this routine test. Check for a clock on pin 13 of A16U111, U116, and U119. Check for stuck logic high or low on U108. Also, check for low on U461-19 and high on U461-2.

8316 Error Index

Explanation: The AFO(H) A MAP filled once readback bit should have been set high, but it was not read back as being set.

Probable Cause	Action
Suspect A16U253, U111, U108B, U105C and D, U124A and D.	Refer to the appropriate schematic and analyze these components while looping on this routine test. Check for a clock on pin 13 of A16U111, U116, and U119. Check for stuck logic high or low on U108. Also, check for low on U461-19 and high on U461-2.

8317 Error Index

Explanation: The ARB(H) A MAP readback bit was set before the MAP counter reached 5F7$_{hex}$.

Probable Cause	Action
Suspect A16U253, U461, U111, U108B, U105C and D, U124A and D. The value in the result address field is the value the MAP counter reached before the set bit was read from the ARB(H) line.	Refer to the appropriate schematic and analyze these components while looping on this routine test. Check for a clock on pin 13 of A16U111, U116, and U119. Check for stuck logic high or low on U108. Also, check for low on U461-2 and high on U461-19.

8318 Error Index

Explanation: The ARB(H) A MAP readback bit should have been set high, but it was not read back as being set.

Probable Cause	Action
Suspect A16U253, U461, U111, U108B, U105C and D, U124A and D.	Refer to the appropriate schematic and analyze these components while looping on this routine test. Check for a clock on pin 13 of A16U111, U116, and U119. Check for stuck logic high or low on U108. Also, check for low on U461-2 and high on U461-19.

8319 Error Index

Explanation: The AFO(H) A MAP filled once readback bit should have been set high, but it was not read back as being set.

Probable Cause	Action
Suspect A16U253, U111, U108B, U105C and D, U124A and D.	Refer to the appropriate schematic and analyze these components while looping on this routine test. Check for a clock on pin 13 of A16U111, U116, and U119. Check for stuck logic high or low on U108. Also, check for low on U461-2 and high on U461-19.

831A Error Index

Explanation: The ARB(H) A MAP readback bit was set before the MAP counter reached $7F7_{hex}$.

8318
8319
831A

Probable Cause	Action
Suspect A16U253, U461, U111, U108B, U105C and D, U124A and D. The value in the result address field is the value the MAP counter reached before the set bit was read from the ARB(H) line.	Refer to the appropriate schematic and analyze these components while looping on this routine test. Check for a clock on pin 13 of A16U111, U116, and U119. Check for stuck logic high or low on U108. Also, check for high on U461-2,19.

831B Error Index

Explanation: The ARB(H) A MAP readback bit should have been set high, but it was not read back as being set.

Probable Cause	Action
Suspect A16U253, U461, U111, U108B, U105C and D, U124A and D.	Refer to the appropriate schematic and analyze these components while looping on this routine test. Check for a clock on pin 13 of A16U111, U116, and U119. Check for stuck logic high or low on U108. Also, check for high on U461-2,19.

831C Error Index

Explanation: The AFO(H) A MAP filled once readback bit should have been set high, but it was not read back as being set.

Probable Cause	Action
Suspect A16U253, U111, U108B, U105C and D, U124A and D.	Refer to the appropriate schematic and analyze these components while looping on this routine test. Check for a clock on pin 13 of A16U111, U116, and U119. Check for stuck logic high or low on U108. Also, check for high on U461-2,19.

ROUTINE 2 DESCRIPTION

This test verifies the operation of the B-side Memory Address Pointer (MAP) circuitry. The BRB(H) B MAP readback bit is initially reset to return a 00_{hex} readback value. During the test, the B MAP readback status information is read $3F_{hex}$ times from A16U253. Each read increments the MAP counter by eight. Each time the information is read back, the test expects the B MAP readback bit to be reset and return a value of 00_{hex}. If the bit is not reset during any of these read operations, the test is aborted and a failure is reported. When the bit has been read back $3F_{hex}$ times, the final MAP count should be $1FF_{hex}$. The test reads the serial information on the the BRB(H) signal line once again, this time expecting a bit to be set. If the information read back does not indicate a bit was set, the test is aborted and a failure is reported.

Now, the A- and B-side MAP clocks are disabled and the BFO(H) B MAP filled once bit is selected to be read from A16U253. The test performs two more reads. The first read clears the unwanted data from A16U361. The second read returns status information on the BFO(H) signal line. The test expects to read FF_{hex} since both MAP clocks have been disabled and the MAP was not incremented.

Next, the B-side MAP circuitry is programmed to address two acquisition cards. The B MAP readback status information is read $7F_{hex}$ times from A16U253. The final MAP count should be $3F7_{hex}$. The test sequence is the same as previously described.

If no failures are detected, the MAP circuitry is programmed to address three acquisition cards. The B MAP readback status information is read BF_{hex} times from A16U253. The final MAP count should be $5F7_{hex}$. The test sequence is the same as previously described.

Finally, if no failures are detected, the MAP circuitry is programmed to address four acquisition cards. The B MAP readback status information is read FF_{hex} times from A16U253. The final MAP count should be $7F7_{hex}$. The test sequence is the same as previously described.

8321 Error Index

Explanation: The BRB(H) B MAP readback bit was set before the MAP counter reached $1FF_{hex}$.

8321

Probable Cause	Action
Suspect A16U253, U127, U122, U134, U140, U124, and U137. The value in the result address field is the value the MAP counter reached before the set bit was read from the BRB(H) line.	Refer to the appropriate schematic and analyze these components while looping on this routine test. Check for a clock pulse on pin 13 of U122, U127, and U134. Check for stuck logic high or low on U137.

8322 Error Index

Explanation: The BRB(H) B MAP readback bit should have been set high, but it was not read back as being set.

Probable Cause	Action
Suspect A16U253, U127, U122, U134, U140, U124, and U137.	Refer to the appropriate schematic and analyze these components while looping on this routine test. Check for a clock pulse on pin 13 of U122, U127, and U134. Check for stuck logic high or low on U137.

8323 Error Index

Explanation: The BFO(H) B MAP filled once readback bit should have been set high, but it was not read back as being set.

Probable Cause	Action
Suspect A16U253, U127, U122, U134, U140, U124, and U137.	Refer to the appropriate schematic and analyze these components while looping on this routine test. Check for a clock pulse on pin 13 of U122, U127, and U134. Check for stuck logic high or low on U137.

8324 Error Index

Explanation: The BRB(H) B MAP readback bit was set before the MAP counter reached $3F7_{hex}$.

Probable Cause	Action
Suspect A16U253, U134, U140, U124, and U137. The value in the result address field is the value the MAP counter reached before the set bit was read from the BRB(H) line.	Refer to the appropriate schematic and analyze these components while looping on this routine test. Check for a clock pulse on pin 13 of U122, U127, and U134. Check for stuck logic high or low on U137.

8325 Error Index

Explanation: The BRB(H) B MAP readback bit should have been set high, but it was not read back as being set.

Probable Cause	Action
Suspect A16U253, U134, U140, U124, and U137.	Refer to the appropriate schematic and analyze these components while looping on this routine test. Check for a clock pulse on pin 13 of U122, U127, and U134. Check for stuck logic high or low on U137.

8326 Error Index

Explanation: The BFO(H) B MAP filled once readback bit should have been set high, but it was not read back as being set.

Probable Cause	Action
Suspect A16U253, U134, U140, U124, and U137.	Refer to the appropriate schematic and analyze these components while looping on this routine test. Check for a clock pulse on pin 13 of U122, U127, and U134. Check for stuck logic high or low on U137.

8327 Error Index

Explanation: The BRB(H) B MAP readback bit was set before the MAP counter reached $5F7_{hex}$.

Probable Cause	Action
Suspect A16U253, U134, U140, U124, and U137. The value in the result address field is the value the MAP counter reached before the set bit was read from the BRB(H) line.	Refer to the appropriate schematic and analyze these components while looping on this routine test. Check for a clock pulse on pin 13 of U122, U127, and U134. Check for stuck logic high or low on U137.

8328 Error Index

Explanation: The BRB(H) B MAP readback bit should have been set high, but it was not read back as being set.

Probable Cause	Action
Suspect A16U253, U134, U140, U124, and U137.	Refer to the appropriate schematic and analyze these components while looping on this routine test. Check for a clock pulse on pin 13 of U122, U127, and U134. Check for stuck logic high or low on U137.

8329 Error Index

Explanation: The BFO(H) B MAP filled once readback bit should have been set high, but it was not read back as being set.

Probable Cause	Action
Suspect A16U253, U134, U140, U124, and U137.	Refer to the appropriate schematic and analyze these components while looping on this routine test. Check for a clock pulse on pin 13 of U122, U127, and U134. Check for stuck logic high or low on U137.

832A Error Index

Explanation: The BRB(H) B MAP readback bit was set before the MAP counter reached $7F7_{hex}$.

Probable Cause	Action
Suspect A16U253, U134, U140, U124, and U137. The value in the result address field is the value the MAP counter reached before the set bit was read from the BRB(H) line.	Refer to the appropriate schematic and analyze these components while looping on this routine test. Check for a clock pulse on pin 13 of U122, U127, and U134. Check for stuck logic high or low on U137.

832B Error Index

Explanation: The BRB(H) B MAP readback bit should have been set high, but it was not read back as being set.

Probable Cause	Action
Suspect A16U253, U134, U140, U124, and U137.	Refer to the appropriate schematic and analyze these components while looping on this routine test. Check for a clock pulse on pin 13 of U122, U127, and U134. Check for stuck logic high or low on U137.

832C Error Index

Explanation: The BFO(H) B MAP filled once readback bit should have been set high, but it was not read back as being set.

Probable Cause	Action
Suspect A16U253, U134, U140, U124, and U137.	Refer to the appropriate schematic and analyze these components while looping on this routine test. Check for a clock pulse on pin 13 of U122, U127, and U134. Check for stuck logic high or low on U137.

ROUTINE 3 DESCRIPTION

This test verifies the operation of both A- and B-side Memory Address Pointer (MAP) circuits while being driven by the STR 1(H) signal line (T1 clock). During the first part of this test, the processor generates a clock on the STR 1(H) signal line. This clock signal is selected by A16U332 to be the A MAP CLK(H) signal. During the test, the A-side readback clock through A16U275 is disabled. When testing of the A side is complete, the B-side MAP circuitry is checked using the same procedure.

Testing of the A-side MAP circuitry begins by incrementing the A-side MAP counters to $1FE_{hex}$. The Control Processor reads back the condition of the ARB (H) signal line, expecting it to be inactive low. If the readback bit is set high, the test is aborted and a failure is reported. The A MAP CLK(H) line is pulsed once more and the counter should be at $1FF_{hex}$. The processor reads the ARB(H) line once again, this time expecting it to be active high. Finally, the processor increments the A-side MAP circuitry one last time and reads the condition of the AFO(H) filled once signal. It should be set active high. If either of the readback bits are not set correctly, the test is aborted and a failure is reported.

After the A-side MAP circuitry is checked, testing begins on the B-side MAP circuitry. The test sequence is the same as for the A-side circuitry.

8331 Error Index

Explanation: The ARB(H) A MAP readback bit should have been reset low after the MAP counter reached $1FE_{hex}$, but it was not read back as being set low.

Probable Cause	Action
No MAP clock.	Refer to the appropriate schematic and analyze these components while looping on this routine test. Check A16U346-11 and -14 for a high signal with a low-going 10 ns pulse.
Suspect A16U332 or A16U346.	While looping on this routine test, check A16U332-5 for a logic low.

8332 Error Index

Explanation: The ARB(H) A MAP readback bit should have been set high after the MAP count reached $1FE_{hex}$, but it was not read back as being set high.

Probable Cause	Action
No MAP clock.	Refer to the appropriate schematic and analyze these components while looping on this routine test. Check A16U346-11 and -14 for a high signal with a low-going 10 ns pulse.
Suspect A16U332 or A16U346.	While looping on this routine test, check A16U332-5 for a logic low. Also check A16U346-10 for a logic high.

8333 Error Index

Explanation: The AFO(H) A MAP filled once readback bit should have been set high after the MAP count reached 200_{hex}, but it was not read back as being set high.

Probable Cause	Action
The MAP clock signal amplitude is marginal.	Refer to the appropriate schematic and analyze these components while looping on this routine test. Check A16U346-11 and -14 for a high signal with a low-going 10 ns pulse.

8334 Error Index

Explanation: The BRB(H) B MAP readback bit should have been reset low after the MAP counter reached $1FE_{hex}$, but it was not read back as being set low.

Probable Cause	Action
No MAP clock.	Refer to the appropriate schematic and analyze these components while looping on this routine test. Check A16U346-7 for a high signal with a low-going 10 ns pulse.
Suspect A16U335 or A16U346.	While looping on this routine test, check A16U335-5 for a logic low.

8335 Error Index

Explanation: The BRB(H) B MAP readback bit should have been set high after the MAP count reached $1FE_{hex}$, but it was not read back as being set high.

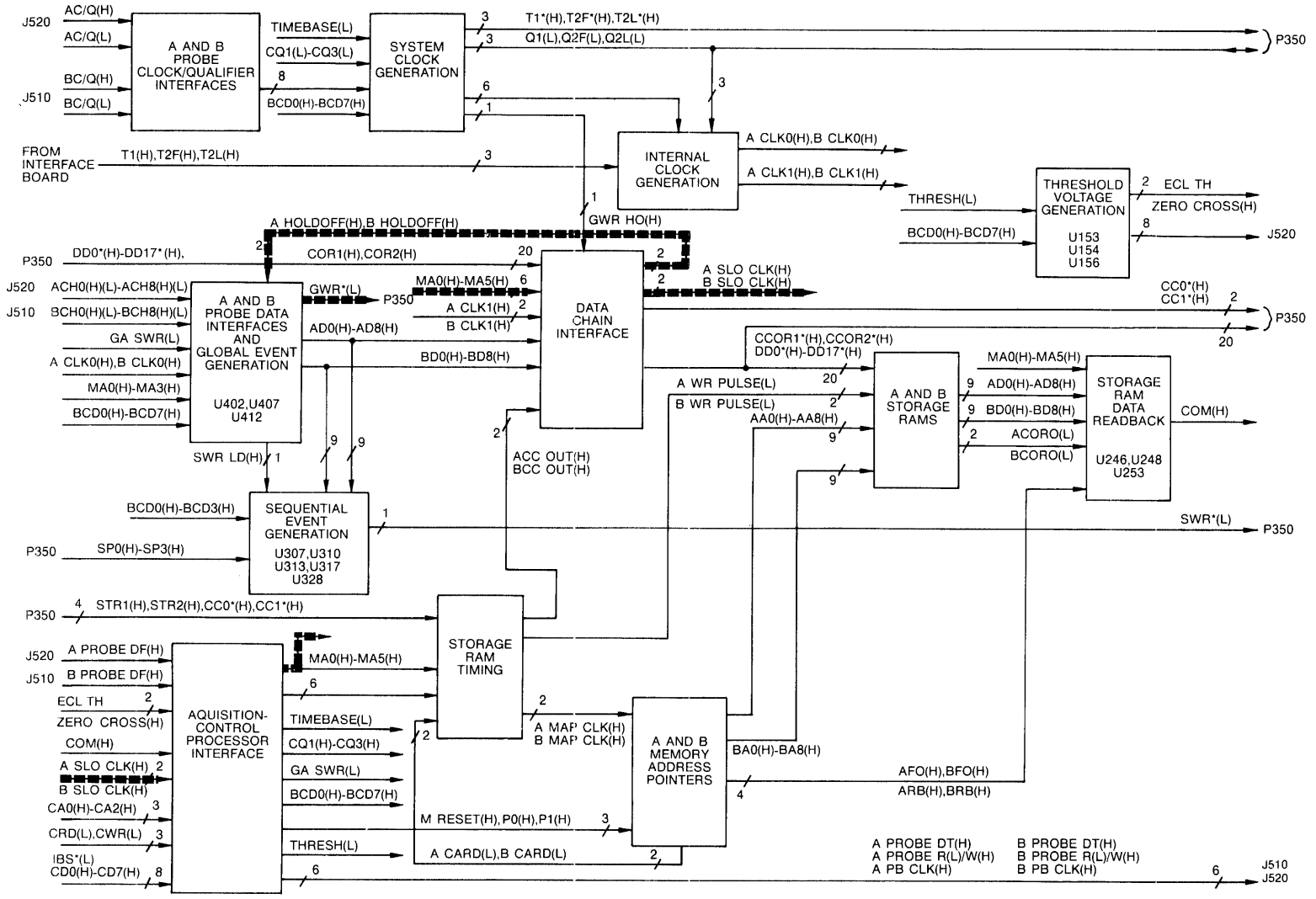
Probable Cause	Action
No MAP clock.	Refer to the appropriate schematic and analyze these components while looping on this routine test. Check A16U346-7 for a high signal with a low-going 10 ns pulse.
Suspect A16U335 or A16U346.	While looping on this routine test, check A16U335-5 for a logic low. Also, check A16U346-6 for a logic high.

8336 Error Index

Explanation: The BFO(H) B MAP filled once readback bit should have been set high after the MAP count reached 200_{hex}, but it was not read back as being set high.

Probable Cause	Action
The MAP clock signal amplitude is marginal.	Refer to the appropriate schematic and analyze these components while looping on this routine test. Check A16U346-7 for a high signal with a low-going 10 ns pulse.

1240D2 18-CHANNEL BLOCK DIAGRAM
X ACQ RAM – AREA 4



4342-141

Figure 8-121. 18-Channel X ACQ RAM block diagram.

1240D2 18-CHANNEL ACQUISITION BOARD – COMPONENT LOCATION

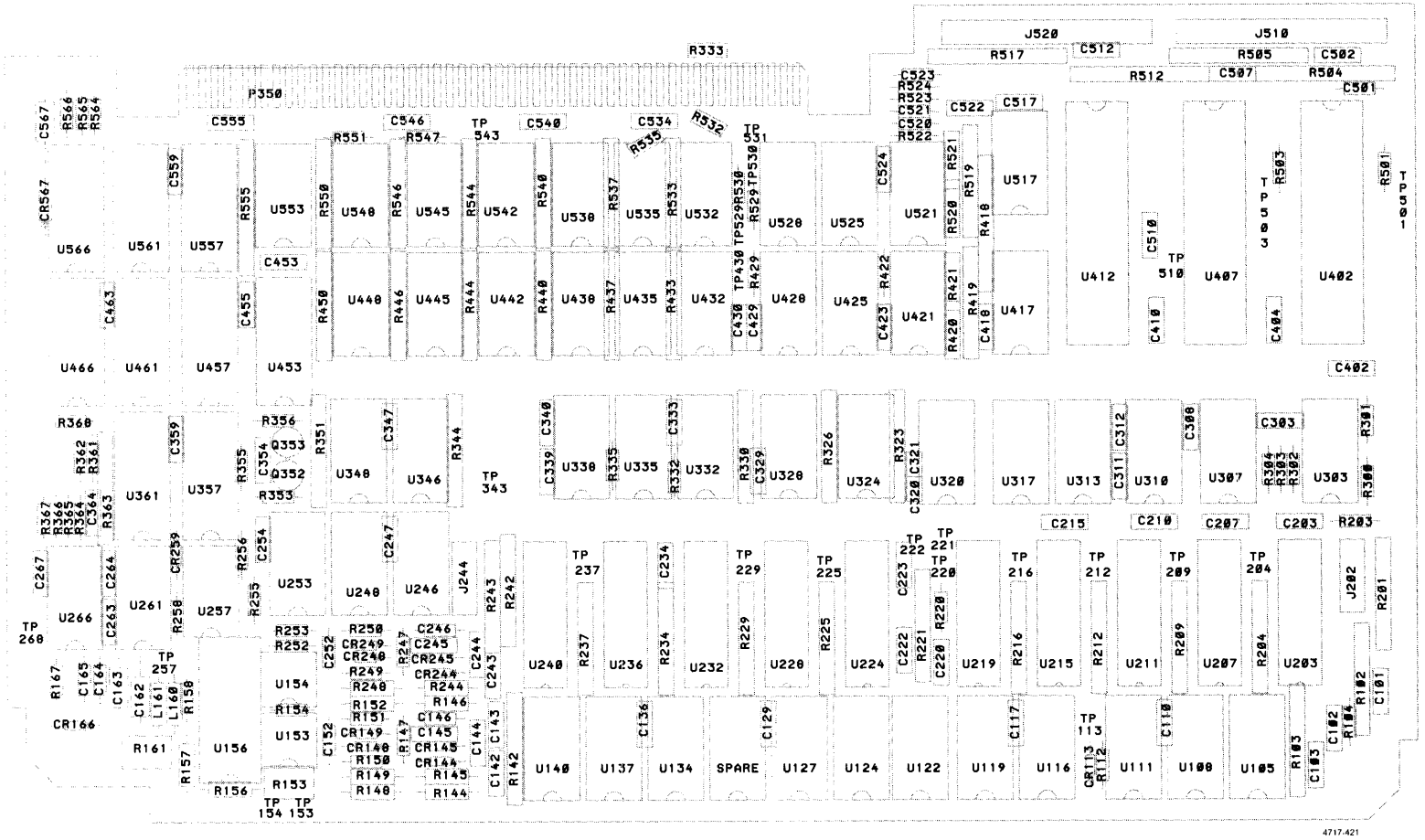


Figure 8-122. 18-Channel Acquisition Board component location.

module: 1240D2-X
area: X ACQ RAM

X ACQ RAM AREA – CIRCUIT OVERVIEW

The pattern-shaded signal lines on the extended acquisition RAM block diagram indicate circuitry used during diagnostic testing. Only the circuitry that is being exercised for the first time during diagnostic testing is shown. Circuitry exercised by other diagnostic tests are shown in their respective block diagrams.

Since the circuitry involved during these 84XX diagnostic tests is basically the same as that used during the 82XX Acquisition RAM diagnostic tests, circuit descriptions are not repeated here.

X ACQ RAM AREA – TEST DESCRIPTION

The extended acquisition RAM test consists of four routines. Routine 1 verifies the operation of both A- and B-side slow clock detection circuits. Routine 2 verifies the data-line independence for both A- and B-sides of the acquisition RAM. Routine 3 verifies the ability of the 18-Channel Acquisition card to store qualified data. Routine 4 verifies that A-side acquisition RAM data can be stored in the B-side of acquisition RAM. Both routines 3 and 4 require that two acquisition probes be connected to the Test Pattern Generator (TPG).

ROUTINE 1 – TEST DESCRIPTION

This test verifies the operation of both A- and B-side slow clock detection circuits. These circuits are responsible for determining when the A- or B-side master sample clock is occurring infrequently. During normal operation, the 1240 firmware detects when a slow clock condition exists by checking the frequency of the master sample clocks. If the firmware reads that no master sample clocks had occurred since the last time checked, it may decide that the sample clock is too slow. If so, a SLOW CLOCK message is flashed on the 1240 screen to indicate that sample clocks are infrequent.

The test begins by writing a logic high on the MA0(H) miscellaneous address line to A16U442-7. A16U442-9 is clocked by the processor with the A CLK1(H) line, causing the logic high to be latched by U442. Now, the processor reads the output of the latch on the A SLO CLK(H) line. If the read operation indicates the A SLO CLK(H) line is active high, the test passes and the B-side circuitry is then checked. Testing of the B side is performed in the same manner as for the A side.

8411

8411 Error Index

Explanation: There was a problem in the readback of the A- or B-side slow clock bit. The test may have read the A-side slow clock bit as being a logic low, but expected the bit to be a logic high. For example, if the expected screen result is 01_{hex}, and the actual result is 00_{hex}, the A-side slow clock readback bit was low. It is also possible that the test read the B-side slow clock bit as being a logic high, but expected the bit to be a logic low. For example, if the expected screen result is 01_{hex}, and the actual result is 03_{hex}, the B-side slow clock readback bit was high.

Probable Cause	Action
If the A-side circuit is suspected, check A16U442, U266, or U457.	Using the appropriate schematic, analyze these components while looping on this routine test. Check for a pulsing high signal on U442-4.
If the B-side circuit is suspected of being faulty, check A16U448.	Using the appropriate schematic, analyze these components while looping on this routine test. Check for a pulsing low signal on U448-4.

8412 Error Index

Explanation: There was a problem in the readback of the A- or B-side slow clock bit. The test may have read the A-side slow clock bit as being a logic high, but expected the bit to be a logic low. For example, if the expected screen result is 02_{hex}, and the actual result is 03_{hex}, the A-side slow clock readback bit was high. It is also possible that the test read the B-side slow clock bit as being a logic low, but expected the bit to be a logic high. For example, if the expected screen result is 02_{hex}, and the actual result is 00_{hex}, the B-side slow clock readback bit was low.

Probable Cause	Action
If the A-side circuit is suspected, check A16U442.	Using the appropriate schematic, analyze these components while looping on this routine test. Check for a pulsing high signal on U442-4.
If the B-side circuit is suspected of being faulty, check A16U448, U266, or U457.	Using the appropriate schematic, analyze these components while looping on this routine test. Check for a pulsing low on U448-4.

ROUTINE 2 – TEST DESCRIPTION

This test verifies data-line independence for both A- and B-sides of the acquisition RAM. Data-line independence is checked by shifting one bit across the inputs of gate arrays, A16U402, U407, and U412, and reading back the correct pattern.

Gate array loading is done through the Acquisition-Control Processor Interface on the BCD data lines. Data lines BCD0(H)-BCD2(H) are the A-side inputs to the gate arrays. Data lines BCD3(H)-BCD5(H) are the B-side inputs to the gate arrays. Each gate array outputs three data bits for the A-side of memory and three data bits for the B-side of memory. (The polarity of the output data is the inverse of the input data.)

Tests begin for both A and B sides by writing a high to the least significant bit of each gate array (i.e., A- and B-side bits 0, 3, and 6). The processor uses the ASELT1(L) and BSELT1(L) lines from A16U466 to select clocks for latching gate array data into the Data Chain Interface. Data in the interface is clocked into the first location of acquisition RAM by manipulating the A and B FORCE STR lines from A16U461-6 and -15.

Next, the input data pattern is shifted one bit and a logic high is written to to the second-least significant bit of each gate array (i.e., A- and B-side bits 1, 4, and 7). The output of the gate arrays is stored in the second location of both A- and B-side acquisition RAMs. A final shift of the input bit pattern and the third read of gate array data is stored in the third location of both A- and B-side acquisition RAMs. The processor reads the contents of the acquisition RAMs and compares the data to the expected patterns 049_{hex}, 092_{hex}, and 124_{hex}.

8421 Error Index

Explanation: The A-side acquisition circuitry failed the test.

Probable Cause	Action
Suspect A16U412, U407, U402, U438, U442, or the A side of Acquisition memory.	Convert the expected and actual hexidecimal values displayed on the screen to binary values. By examining the bit patterns, you can determine the data channel causing the failure.

8422 Error Index

Explanation: The B-side acquisition circuitry failed the test.

Probable Cause	Action
Suspect A16U412, U407, U402, U445, U448, or the B side of Acquisition memory.	Convert the expected and actual hexidecimal values displayed on the screen to binary values. By examining the bit patterns, you can determine the data channel causing the failure.

ROUTINE 3 – TEST DESCRIPTION

This test verifies the ability of the 18-Channel Acquisition card to store qualified data. The test requires that two input probes be used to connect the 18-Channel Acquisition card to the Test Pattern Generator (TPG).

The test checks the A side first and then the B side. First, the acquisition card is programmed to acquire data synchronously. The A- and B-side C/Q lines to the Probe Clock/Qualifier Interface are used as clock and qualifier inputs. The acquisition card is programmed to use the BT2LF(L) signal from A16U521 as the source for acquisition clocks. The TPG is programmed to use the processor-stepped T1 clock. The Global Word Recognizer is programmed to recognize a logic high on bits 6, 7, and 8; all other bits are set to the Don't Care (X) state. The trigger card is programmed to generate a store pulse on the STR2(H) line only when a global event occurs (i.e., when bits 6, 7, and 8 are high). The STR2(H) line causes the Storage RAM Timing circuitry to generate storage signals for the acquisition memory.

A 64-word-long pattern is acquired from the TPG. The data is stored in the A-side of acquisition RAM. The Control Processor reads back the A-side data through the Aquisition-Control Processor Interface. Next the TPG pattern is acquired and stored in the B-side of acquisition RAM. This time the Control Processor reads the B-side data and if an error is found, the test reports the failure. The following shows the data that should have been acquired:

A-Side Memory	B-Side Memory
$1F7_{hex}$	$1F7_{hex}$
$1E7_{hex}$	$1EF_{hex}$
$1D7_{hex}$	$1D7_{hex}$
$1EF_{hex}$	$1DF_{hex}$
$1C7_{hex}$	$1C7_{hex}$
$1CF_{hex}$	$1E7_{hex}$
$1DF_{hex}$	$1CF_{hex}$

8431 Error Index

Explanation: The test failed to detect both acquisition probes.

Probable Cause	Action
One or both of the probes is not connected, or a probe may be bad.	Examine the expected and actual screen data. If the expected result is 00_{hex} and the actual result is 40_{hex}, suspect the A-side probe. If the expected result is 00_{hex} and the actual result is 80_{hex}, suspect the B-side probe.
Suspect A16U457.	While looping on this test, check A16U457-9 for low-going pulses.
Suspect A16U561.	While looping on this test, check A16U561-1 for low-going pulses. If none are found, check A16U348 for correct operation. Also, check A16U561-8 and -12 for high-going pulses.

8432 Error Index

Explanation: The A-side acquisition circuitry failed the test.

Probable Cause	Action
No clock.	Check A16U521-3 and 11 for a clock. Check U521-15 for a logic low. If pin 15 is low and there is no clock on pin 3, suspect U521. If there is no clock on pin 14, suspect A16U517, or the B-side probe, or the TPG output.
Trigger module failure.	Run the diagnostic tests for the Trigger module.
Faulty global word recognizer (gate array).	Suspect A16U412, U407, U402, and U324.

8433 Error Index

Explanation: The B-side acquisition circuitry failed the test.

Probable Cause	Action
Faulty global word recognizer (gate array).	Suspect A16U412, U407, U402, and U324. 670-7703-07 board suspect U320.

ROUTINE 4 – TEST DESCRIPTION

This test verifies that A-side acquisition-RAM data can be stored in the B-side of acquisition RAM. This test requires that two input probes be used to connect the 18-Channel Acquisition card to the Test Pattern Generator (TPG). The test programs the gate arrays to accept data from the A probe only, causing data input on the A-side of the gate array to be output on both A- and B-side data lines.

First, the acquisition card is programmed to acquire data synchronously. The A- and B-side C/Q lines to the Probe Clock/Qualifier Interface are used as clock and qualifier inputs. The acquisition card is programmed to use the AT2LF(L) signal from A16U521 as the source for acquisition clocks. The TPG is programmed to use the processor-stepped T1 clock. All word recognizers are programmed to the Don't Care (X) state.

To fill the A- and B-side memories with TPG data, the processor generates 512 storage clocks. The Control Processor reads back the A-side memory first to verify that the data is correct. If the A-side data is correct, the B-side data is read and compared to the A-side reference data.

8441 Error Index

Explanation: The test failed to detect both acquisition probes.

Probable Cause	Action
One or both of the probes is not connected, or a probe may be bad.	Examine the expected and actual screen data. If the expected result is 00_{hex} and the actual result is 40_{hex}, suspect the A-side probe. If the expected result is 00_{hex} and the actual result is 80_{hex}, suspect the B-side probe.
Suspect A16U457.	While looping on this test, check A16U457-9 for low-going pulses.
Suspect A16U561.	While looping on this test, check A16U561-1 for low-going pulses. If none are found, check A16U348 for correct operation. Also, check A16U561-8 and -12 for high-going pulses.

8442 Error Index

Explanation: The A-side acquisition circuitry failed the test. The expected and actual results displayed indicate the first TPG word to be acquired incorrectly. Refer to the *Operating Information* section for a table showing the correct TPG output pattern. When using this table, remember that only the A-side TPG data (from J630) was stored in the A and B memories.

Probable Cause	Action
Defective gate array or A-side of memory.	Suspect A16U412, U407, and U402. If no defective I.C.'s are found, loop on this test and examine the A-side memory circuits.

8443 Error Index

Explanation: The B-side acquisition circuitry failed the test. The expected and actual results displayed indicate the first TPG word to be acquired incorrectly. Refer to the *Operating Information* section for a table showing the correct TPG output pattern. When using this table, remember that only the A-side TPG data (from J630) was stored in the A and B memories.

Probable Cause	Action
Defective gate array or B-side of memory.	Suspect A16U412, U407, and U402. If no defective I.C.'s are found, loop on this test and examine the B-side memory circuits.

1240D2 18-CHANNEL BLOCK DIAGRAM
WORD REC – AREA 5

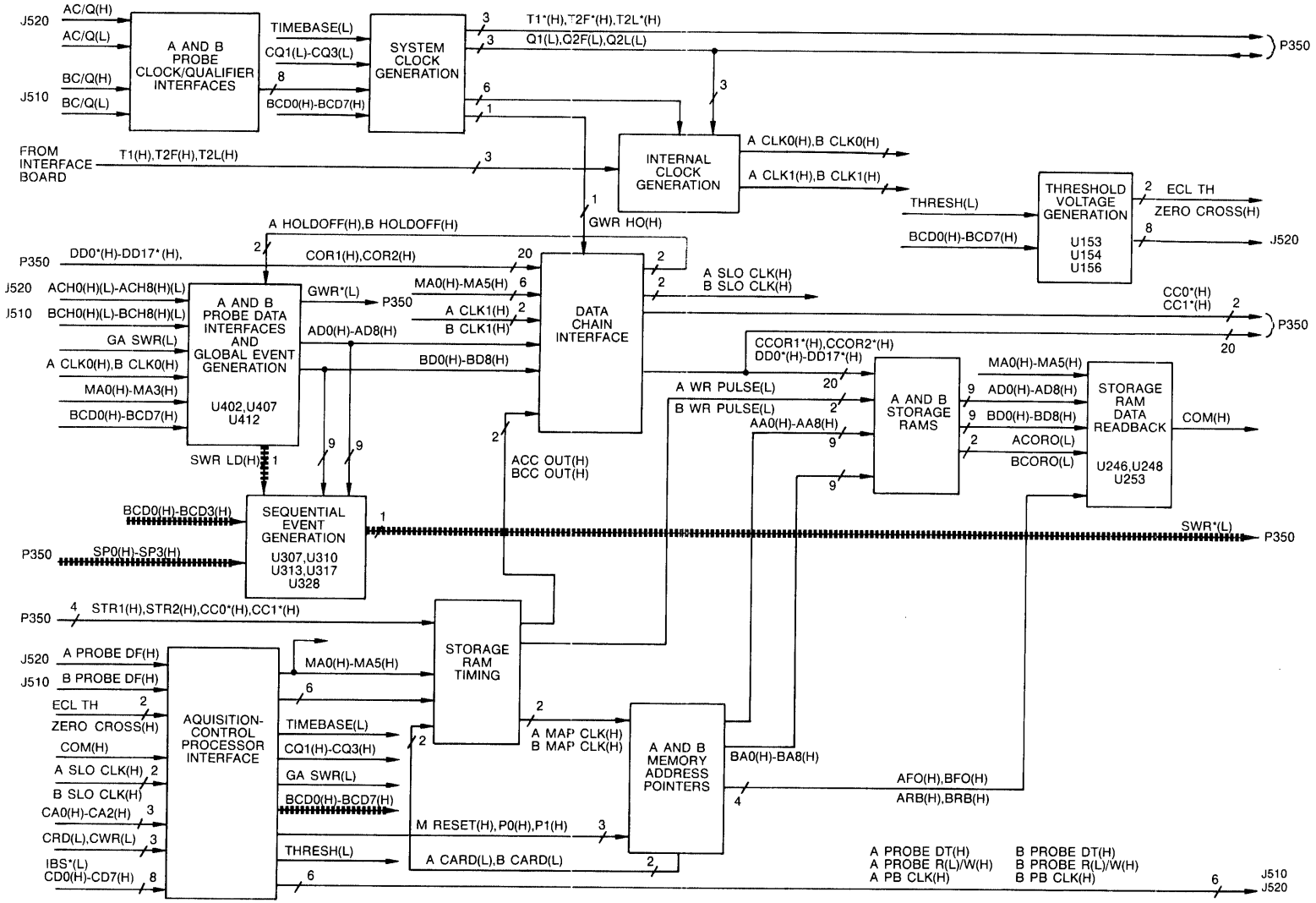


Figure 8-123. 18-Channel WORD REC block diagram.

4342-142

1240D2 18-CHANNEL ACQUISITION BOARD – COMPONENT LOCATION

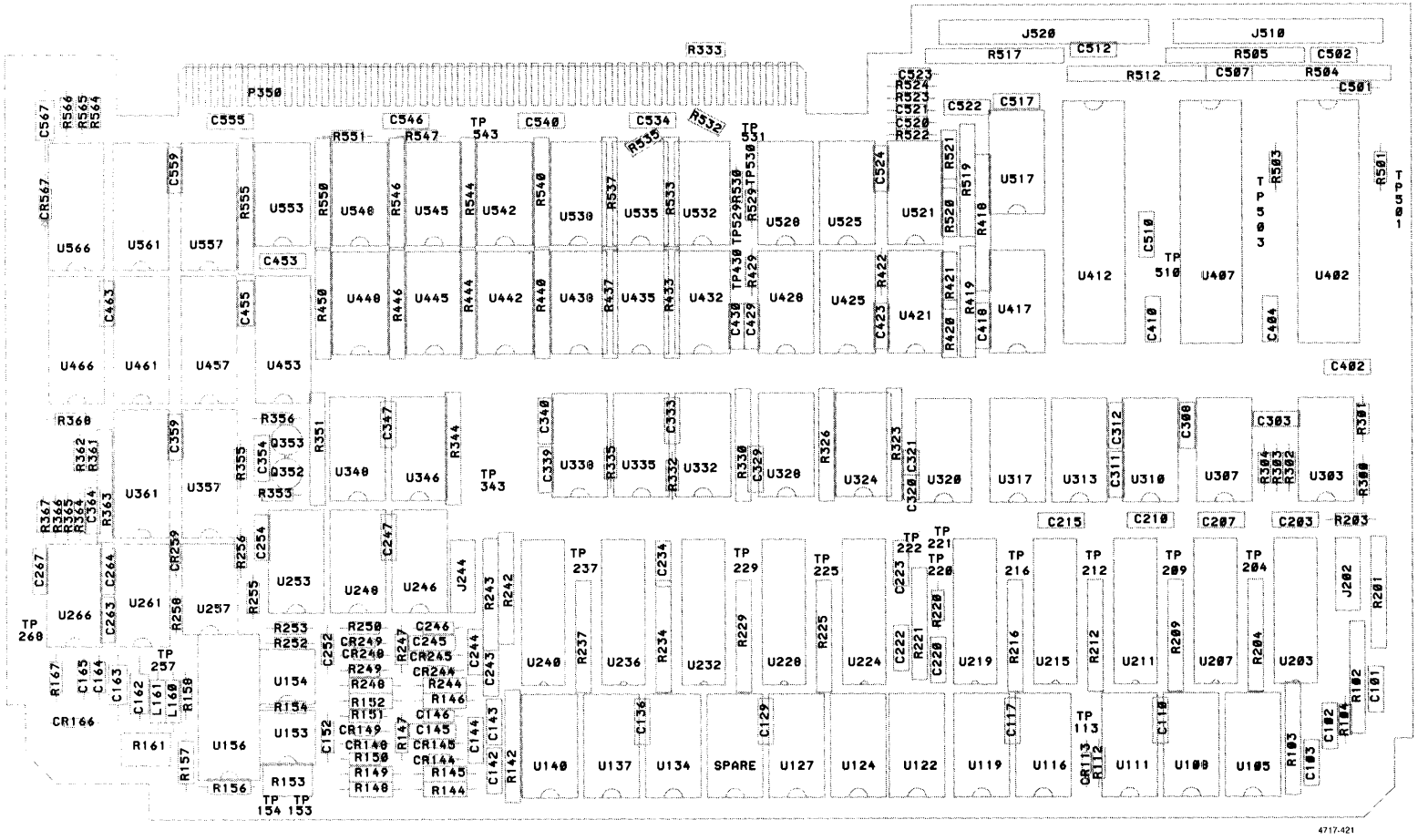


Figure 8-124. 18-Channel Acquisition Board component location.

module: 1240D2-X
area: WORD REC

WORD REC AREA – CIRCUIT OVERVIEW

The pattern-shaded signal lines on the word recognizer block diagram indicate circuitry used during diagnostic testing. Only the circuitry that is being exercised for the first time during diagnostic testing is shown. Circuitry exercised by other diagnostic tests are shown in their respective block diagrams.

The 18 differential ECL-level channels from both A and B probes carry probe data to the gate arrays A16U412, U407, and U402. The gate arrays provide a sample latch for probe data, and compare incoming data against previously selected event patterns (for global word recognition). The global event pattern information is loaded in parallel to the gate arrays on BCD0(H)-BCD6(H). Each gate array has four internal registers. Two of these hold the global event patterns for the A and B sides. One register controls the delay of data through the gate array, and the other latches data used during the programming of the sequential word recognizer.

When a GWR match occurs, the gate arrays output an active low Global Word Recognizer GWR*(L) signal from U324B pin 15. The latched data is sent to the Data Chain Interface and the Sequential Event Generation circuitry, and into storage RAM. The active low GWR*(L) line is read by the Control Processor through the Trigger Board's Trigger-Control Processor Interface circuitry. (The polarity of the global word recognizer bit is inverted by the trigger circuitry before readback occurs.)

The Sequential Event Generation RAMs, A16U307, U310, U313, and U317, are loaded with the data patterns specified by the user in the Timebase menu. Data is stored by control of the SP0(H)-SP3(H) stack pointer lines from the Trigger Board. The RAMs, acting as word recognizers, output the recognized bit pattern to A16U324A when an SWR match occurs. If all inputs to U324A are active low, the Sequential Word Recognizer SWR*(L) signal goes active low.

WORD REC AREA – TEST DESCRIPTION

The word recognizer test consists of three routines. Routine 1 verifies the Global Word Recognizer (GWR) for the clocked mode of operation. Routine 2 verifies the GWR for the unclocked mode of operation. Routine 3 verifies the operation of the Sequential Word Recognizer (SWR). All routines require that two input probes be used to connect the 18-Channel Acquisition card to the Test Pattern Generator (TPG).

ROUTINE 1 – TEST DESCRIPTION

This routine verifies the Global Word Recognizer (GWR) for the clocked mode of operation. To verify the GWR circuitry, the word recognizer is loaded with a word identical to one of the Test Pattern Generator (TPG) output words. The TPG is used as the source for input stimulus. By checking for GWR recognition of this specific word (indicated by the active GWR*(L) line), the operational status of the GWR may be determined. Refer to the *Operating Information* section for a complete listing of the A-side (J630) and B-side (J620) TPG-output words.

The test is run in two passes, checking the A side first and then the B side. The test programs the acquisition card to acquire data synchronously and to use the AT2LF(L) signal from A16U521 as the source for acquisition clocks. The TPG is programmed to use the processor-stepped T1 clock. The A-side word recognizer, consisting of gate arrays A16U412, U407, and U402, is programmed to recognize the fifth TPG output word, $0AA_{hex}$. (The first TPG word, $1FF_{hex}$, is the reset word and therefore is not counted.) The TPG is reset and the processor single-steps the TPG four times. The Control Processor reads the status of the GWR*(L) line through the Trigger-Control Processor Interface on the Trigger Board. (The polarity of the global word recognizer bit is inverted by the trigger circuitry before readback occurs.) If the GWR outputs an active low signal indicating that a match to one of the TPG words was found, the test is aborted and a failure is reported. The processor then steps the output of the TPG one more time. The word generated, $0AA_{hex}$, should match the preprogrammed value in the GWR and the GWR*(L) line should go active low. If the active-low GWR signal was not generated, the test is aborted and a failure is reported.

Testing of the B-side word recognizer (gate arrays A16U412, U407, and U402) is done in the same manner with 155_{hex} as the TPG output word. If any failures are detected, the test is aborted and the failure is reported.

The test then re-checks the A-side word recognizer with the sixth TPG-output word, 155_{hex}. If no problems are detected, the B-side word recognizer is checked with its sixth TPG-output word, $0AA_{hex}$.

8511 Error Index

Explanation: The test failed to detect both acquisition probes.

Probable Cause	Action
One or both of the probes is not connected, or a probe may be bad.	Examine the expected and actual screen data. If the expected result is 00_{hex} and the actual result is 40_{hex}, suspect the A-side probe. If the expected result is 00_{hex} and the actual result is 80_{hex}, suspect the B-side probe.
Suspect A16U457.	While looping on this test, check A16U457-9 for low-going pulses.
Suspect A16U561.	While looping on this test, check A16U561-1 for low-going pulses. If none are found, check A16U348 for correct operation. Also, check A16U561-8 and -12 for high-going pulses.

8512 Error Index

Explanation: The A-side circuitry failed the test. The GWR*(L) line (at A16U324-15) should have been high after four clocks.

Probable Cause	Action
Faulty A-side global word recognizer circuitry.	Suspect A16U412, U407, U402, and U324B. Also suspect the readback register A14U275.

8513 Error Index

Explanation: The A-side circuitry failed to recognize the TPG word $0AA_{hex}$. The GWR*(L) line (at A16U324-15) should have been low after five clocks.

Probable Cause	Action
Faulty A-side global word recognizer circuitry.	Suspect A16U412, U407, U402, and U324B. Also suspect the readback register A14U275.

8514 Error Index

Explanation: The B-side circuitry failed the test. The GWR*(L) line (at A16U324-15) should have been high after four clocks.

Probable Cause	Action
Faulty B-side global word recognizer circuitry.	Suspect A16U412, U407, U402, and U324B.

8515 Error Index

Explanation: The B-side circuitry failed to recognize the TPG word 155_{hex}. The GWR*(L) line (at A16U324-15) should have been low after five clocks.

Probable Cause	Action
Faulty B-side global word recognizer circuitry.	Suspect A16U412, U407, U402, and U324B.

8516 Error Index

Explanation: The A-side circuitry failed the test. The GWR*(L) line (at A16U324-15) should have been high after five clocks.

Probable Cause	Action
Faulty A-side global word recognizer circuitry.	Suspect A16U412, U407, U402, and U324B.

8517 Error Index

Explanation: The A-side circuitry failed to recognize the TPG word 155_{hex}. The GWR*(L) line (at A16U324-15) should have been low after six clocks.

Probable Cause	Action
Faulty A-side global word recognizer circuitry.	Suspect A16U412, U407, U402, and U324B.

8518 Error Index

Explanation: The B-side circuitry failed the test. The GWR*(L) line (at A16U324-15) should have been high after five clocks.

Probable Cause	Action
Faulty B-side global word recognizer circuitry.	Suspect A16U412, U407, U402, and U324B.

8519 Error Index

Explanation: The B-side circuitry failed to recognize the TPG word $0AA_{hex}$. The GWR*(L) line (at A16U324-15) should have been low after six clocks.

Probable Cause	Action
Faulty B-side global word recognizer circuitry.	Suspect A16U412, U407, U402, and U324B.

ROUTINE 2 – TEST DESCRIPTION

This routine verifies the Global Word Recognizer (GWR) for the unclocked mode of operation. To verify the GWR circuitry, the word recognizer is loaded with a word identical to one of the Test Pattern Generator (TPG) output words. The TPG is used as the source for input stimulus. By checking for GWR recognition of this specific word (indicated by the active GWR*(L) line), the operational status of the GWR may be determined. Refer to the *Operating Information* section for a complete listing of the A-side (J630) and B-side (J620) TPG-output words.

The test is run in two passes, checking the A side first and then the B side. The test programs the acquisition card to acquire data synchronously and to use the AT2LF(L) signal from A16U521 as the source for acquisition clocks. The TPG is programmed to use the processor-stepped T1 clock. The A-side word recognizer, consisting of gate arrays A16U412, U407, and U402, is programmed to recognize the fifth TPG output word, $0AA_{hex}$. (The first TPG word, $1FF_{hex}$, is the reset word and therefore is not counted.) The TPG is reset and the processor single-steps the TPG four times. The Control Processor reads the status of the GWR*(L) line through the Trigger-Control Processor Interface on the Trigger Board. (The polarity of the global word recognizer bit is inverted by the trigger circuitry before readback occurs.) If the GWR outputs an active low signal indicating that a match to one of the TPG words was found, the test is aborted and a failure is reported. The processor then steps the output of the TPG one more time. The word generated, $0AA_{hex}$, should match the preprogrammed value in the GWR and the GWR*(L) line should go active low. If the active-low GWR signal was not generated, the test is aborted and a failure is reported.

Testing of the B-side word recognizer (gate arrays A16U412, U407, and U402) is done in the same manner with 155_{hex} as the TPG output word. If any failures are detected, the test is aborted and the failure is reported.

The test then re-checks the A-side word recognizer with the sixth TPG-output word, 155_{hex}. If no problems are detected, the B-side word recognizer is checked with its sixth TPG-output word, $0AA_{hex}$.

8521 Error Index

Explanation: The test failed to detect both acquisition probes.

Probable Cause	Action
One or both of the probes is not connected, or a probe may be bad.	Examine the expected and actual screen data. If the expected result is 00_{hex} and the actual result is 40_{hex}, suspect the A-side probe. If the expected result is 00_{hex} and the actual result is 80_{hex}, suspect the B-side probe.
Defective A16U457.	While looping on this test, check A16U457-9 for low-going pulses.
Defective A16U561.	While looping on this test, check A16U561-1 for low-going pulses. If none are found, check A16U348 for correct operation. Also, check A16U561-8 and -12 for high-going pulses.

8522 Error Index

Explanation: The A-side circuitry failed the test. The GWR*(L) line (at A16U324-15) should have been high after four clocks.

Probable Cause	Action
Faulty A-side global word recognizer circuitry.	Suspect A16U412, U407, U402, and U324B. Also suspect the readback register A14U275.

8523 Error Index

Explanation: The A-side circuitry failed to recognize TPG word $0AA_{hex}$. The GWR*(L) line (at A16U324-15) should have been low after five clocks.

Probable Cause	Action
Faulty A-side global word recognizer circuitry.	Suspect A16U412, U407, U402, and U324B. Also suspect the readback register A14U275.

8524 Error Index

Explanation: The B-side circuitry failed the test. The GWR*(L) line (at A16U324-15) should have been high after four clocks.

Probable Cause	Action
Faulty B-side global word recognizer circuitry.	Suspect A16U412, U407, U402, and U324B.

8525 Error Index

Explanation: The B-side circuitry to recognize the TPG word 155_{hex}. The GWR*(L) line (at A16U324-15) should have been low after five clocks.

Probable Cause	Action
Faulty B-side global word recognizer circuitry.	Suspect A16U412, U407, U402, and U324B.

8526 Error Index

Explanation: The A-side circuitry failed the test. The GWR*(L) line (at A16U324-15) should have been high after five clocks.

Probable Cause	Action
Faulty A-side global word recognizer circuitry.	Suspect A16U412, U407, U402, and U324B.

8527 Error Index

Explanation: The A-side circuitry failed to recognize the TPG word 155_{hex}. The GWR*(L) line (at A16U324-15) should have been low after six clocks.

Probable Cause	Action
Faulty A-side global word recognizer circuitry.	Suspect A16U412, U407, U402, and U324B.

8528 Error Index

Explanation: The B-side circuitry failed the test. The GWR*(L) line (at A16U324-15) should have been high after five clocks.

Probable Cause	Action
Faulty B-side global word recognizer circuitry.	Suspect A16U412, U407, U402, and U324B.

8529 Error Index

Explanation: The B-side circuitry failed to recognize the TPG word $0AA_{hex}$. The GWR*(L) line (at A16U324-15) should have been low after six clocks.

Probable Cause	Action
Faulty B-side global word recognizer circuitry.	Suspect A16U412, U407, U402, and U324B.

ROUTINE 3 – TEST DESCRIPTION

This routine verifies the operation of the Sequential Word Recognizer (SWR). The TPG is used as the source for input stimulus. Refer to the *Operating Information* section for a complete listing of the A-side (J630) and B-side (J620) TPG-output words.

The A-side sequential event RAMs, A16U307 and U310, are loaded with the data patterns on the BCD0(H) and BCD1(H) lines. The B-side sequential event RAMs, A16U313 and U317, are loaded with the data patterns on the BCD2(H) and BCD3(H) lines. Data loading is done by control of the SP0(H)-SP3(H) stack pointer lines. The RAMs, acting as word recognizers, output the recognized logic-low bit when they are correctly addressed. If all four RAM outputs to U324A are active low (indicating the input patterns matched the stored patterns), the Sequential Word Recognizer SWR*(L) signal goes active low.

The test is run in two passes, checking the A side first and then the B side. The test programs the acquisition card to acquire data synchronously and to use the AT2LF(L) signal from A16U521 as the source for acquisition clocks. The TPG is programmed to use the processor-stepped T1 clock.

First, the A-side SWR is tested to verify that both RAM outputs may be driven to a logic high. The sequential word recognizer is initialized by writing zeros to both A- and B-side SWR RAMs. The Control Processor reads the status of the SWR*(L) line through the Trigger Board's Trigger-Control Processor Interface to verify that it is active low. (The polarity of the sequential word recognizer bit is inverted by the trigger circuitry before readback occurs.) Now, the A-side RAMs are tested by writing to address $1BE_{hex}$ in conjunction with the BCD0(H) and BCD1(H) lines. Bit 0 is set high and bit 1 is set low. The TPG is reset and after one clock the high bit on A16U307-15 should appear on the pin 1 output. This logic high forces the SWR*(L) signal inactive high. The Control Processor reads the condition of the SWR*(H) line and if a low is detected, the test is aborted and a failure is reported. Again, address $1BE_{hex}$ is written to, this time with bit 0 set low and bit 1 set high. The SWR*(L) line should remain inactive high. If a failure is detected, the test is aborted and a failure is reported.

Next, the A-side SWR RAMs are tested to verify that the 64-word-long TPG pattern can be recognized. The A-side RAMs are initially loaded with ones; the B-side RAMs are loaded with zeros. The A-side SWR RAMs are programmed with the first 16 words of the TPG output pattern. The TPG is reset and an active low SWR*(L) signal should be generated as each TPG pattern is acquired. If the active SWR bit is not generated each time the TPG is stepped, the 1240 displays the TPG word that failed to cause an output. Recognition of the second, third, and fourth sets of 16 TPG words is checked in the same manner. If testing is successfully completed, the A-side RAMs are loaded with zeros and testing of the B-side begins.

Testing of the B side is done in the same manner as the A side. First, the B-side SWR, consisting of RAMs A16U313 and U317, is tested to verify that both RAM outputs may be driven to a logic high. The B-side RAMs are tested by writing to address $1F7_{hex}$ in conjunction with the BCD2(H) and BCD3(H) lines. Next, the B-side SWR RAMs are tested to verify that the 64-word-long TPG pattern can be recognized. If any failures are found during these tests, the test is aborted and a failure is reported.

8531 Error Index

Explanation: The test failed to detect both acquisition probes.

Probable Cause	Action
One or both of the probes is not connected, or a probe may be bad.	Examine the expected and actual screen data. If the expected result is 00_{hex} and the actual result is 40_{hex}, suspect the A-side probe. If the expected result is 00_{hex} and the actual result is 80_{hex}, suspect the B-side probe.
Suspect A16U457.	While looping on this test, check A16U457-9 for low-going pulses.
Suspect A16U561.	While looping on this test, check A16U561-1 for low-going pulses. If none are found, check A16U348 for correct operation. Also, check A16U561-8 and -12 for high-going pulses.

8532 Error Index

Explanation: The A-side circuitry failed the test. RAM A16U307 should have forced the SWR*(L) line inactive high.

Probable Cause	Action
Faulty A-side sequential word recognizer circuitry.	Suspect A16U307 and U324A. Also suspect the read-back register A14U275.

8533 Error Index

Explanation: The A-side circuitry failed the test. RAM A16U310 should have forced the SWR*(L) line inactive high.

Probable Cause	Action
Faulty A-side sequential word recognizer circuitry.	Suspect A16U310 and U324A. Also suspect the read-back register A14U275.

8534 Error Index

Explanation: The A-side circuitry failed to recognize all of the first set of 16 TPG words.

Probable Cause	Action
Faulty A-side sequential word recognizer circuitry.	Check the result address to determine the word causing the failure. While referring to the appropriate schematic, connect a logic analyzer to AD0(H)-AD8(H), A16U307-1, A16U310-1, and SP0(L)-SP3(L) on both U307 and U310. Set the logic analyzer timebase to a 20 μs sample rate and set it to trigger on the failed word and stack level. (The failed stack level may be determined from the following table.) When the logic analyzer has triggered, examine the status of A16U307-1 and U310-1. Both outputs should be low. If an output is high, suspect a defective RAM.

AD0(H)-AD8(H)	SP0(L)-SP3(L)
$1BE_{hex}$	F
$17D_{hex}$	E
$0BA_{hex}$	D
175_{hex}	C
$0AA_{hex}$	B
155_{hex}	A
$0EB_{hex}$	9
196_{hex}	8
$12C_{hex}$	7
059_{hex}	6
$0F3_{hex}$	5
$1A6_{hex}$	4
$14D_{hex}$	3
$0DB_{hex}$	2
$1F7_{hex}$	1
$1AE_{hex}$	0

8535 Error Index

Explanation: The A-side circuitry failed to recognize all of the second set of 16 TPG words.

Probable Cause	Action
Faulty A-side sequential word recognizer circuitry.	Check the result address to determine the word causing the failure. While referring to the appropriate schematic, connect a logic analyzer to AD0(H)-AD8(H), A16U307-1, A16U310-1, and SP0(L)-SP3(L) on both U307 and U310. Set the logic analyzer timebase to a 20 μs sample rate and set it to trigger on the failed word and stack level. (The failed stack level may be determined from the following table.) When the logic analyzer has triggered, examine the status of A16U307-1 and U310-1. Both outputs should be low. If an output is high, suspect a defective RAM.

AD0(H)-AD8(H)	SP0(L)-SP3(L)
$15D_{hex}$	F
$0FB_{hex}$	E
$1B6_{hex}$	D
$16D_{hex}$	C
$09A_{hex}$	B
134_{hex}	A
069_{hex}	9
092_{hex}	8
124_{hex}	7
049_{hex}	6
$0D3_{hex}$	5
$1E7_{hex}$	4
$18E_{hex}$	3
$11C_{hex}$	2
038_{hex}	1
071_{hex}	0

8536 Error Index

Explanation: The A-side circuitry failed to recognize all of the third set of 16 TPG words.

Probable Cause	Action
Faulty A-side sequential word recognizer circuitry.	Check the result address to determine the word causing the failure. While referring to the appropriate schematic, connect a logic analyzer to AD0(H)-AD8(H), A16U307-1, A16U310-1, and SP0(L)-SP3(L) on both U307 and U310. Set the logic analyzer timebase to a 20 μs sample rate and set it to trigger on the failed word and stack level. (The failed stack level may be determined from the following table.) When the logic analyzer has triggered, examine the status of A16U307-1 and U310-1. Both outputs should be low. If an output is high, suspect a defective RAM.

AD0(H)-AD8(H)	SP0(L)-SP3(L)
$0A2_{hex}$	F
145_{hex}	E
$0CB_{hex}$	D
$1D7_{hex}$	C
$1EF_{hex}$	B
$19E_{hex}$	A
$13C_{hex}$	9
079_{hex}	8
$0B2_{hex}$	7
165_{hex}	6
$08A_{hex}$	5
114_{hex}	4
028_{hex}	3
051_{hex}	2
$0E3_{hex}$	1
186_{hex}	0

8537 Error Index

Explanation: The A-side circuitry failed to recognize all of the fourth set of 16 TPG words.

Probable Cause	Action
Faulty A-side sequential word recognizer circuitry.	Check the result address to determine the word causing the failure. While referring to the appropriate schematic, connect a logic analyzer to AD0(H)-AD8(H), A16U307-1, A16U310-1, and SP0(L)-SP3(L) on both U307 and U310. Set the logic analyzer timebase to a 20 μs sample rate and set it to trigger on the failed word and stack level. (The failed stack level may be determined from the following table.) When the logic analyzer has triggered, examine the status of A16U307-1 and U310-1. Both outputs should be low. If an output is high, suspect a defective RAM.

AD0(H)-AD8(H)	SP0(L)-SP3(L)
$10C_{hex}$	F
018_{hex}	E
030_{hex}	D
061_{hex}	C
082_{hex}	B
104_{hex}	A
008_{hex}	9
010_{hex}	8
020_{hex}	7
041_{hex}	6
$0C3_{hex}$	5
$1C7_{hex}$	4
$1CF_{hex}$	3
$1DF_{hex}$	2
$1FF_{hex}$	1
$1BE_{hex}$	0

8538 Error Index

Explanation: The B-side circuitry failed the test. RAM A16U313 should have forced the SWR*(L) line inactive high.

Probable Cause	Action
Faulty B-side sequential word recognizer circuitry.	Suspect A16U313 and U324A.

8539 Error Index

Explanation: The B-side circuitry failed the test. RAM A16U317 should have forced the SWR*(L) line inactive high.

Probable Cause	Action
Faulty B-side sequential word recognizer circuitry.	Suspect A16U317 and U324A.

853A Error Index

Explanation: The B-side circuitry failed to recognize all of the first set of 16 TPG words.

Probable Cause	Action
Faulty B-side sequential word recognizer circuitry.	Check the result address to determine the word causing the failure. While referring to the appropriate schematic, connect a logic analyzer to AD0(H)-AD8(H), A16U313-1, A16U317-1, and SP0(L)-SP3(L) on both U313 and U317. Set the logic analyzer timebase to a 20 μs sample rate and set it to trigger on the failed word and stack level. (The failed stack level may be determined from the following table.) When the logic analyzer has triggered, examine the status of A16U313-1 and U317-1. Both outputs should be low. If an output is high, suspect a defective RAM.

AD0(H)-AD8(H)	SP0(H)-SP3(H)
$1F7_{hex}$	F
$1EF_{hex}$	E
$1D7_{hex}$	D
$1AE_{hex}$	C
155_{hex}	B
$0AA_{hex}$	A
$15D_{hex}$	9
$0B2_{hex}$	8
165_{hex}	7
$0CB_{hex}$	6
$19E_{hex}$	5
134_{hex}	4
069_{hex}	3
$0DB_{hex}$	2
$1BE_{hex}$	1
175_{hex}	0

853B Error Index

Explanation: The B-side circuitry failed to recognize all of the second set of 16 TPG words.

Probable Cause	Action
Faulty B-side sequential word recognizer circuitry.	Check the result address to determine the word causing the failure. While referring to the appropriate schematic, connect a logic analyzer to AD0(H)-AD8(H), A16U313-1, A16U317-1, and SP0(H)-SP3(H) on both U313 and U317. Set the logic analyzer timebase to a 20 μs sample rate and set it to trigger on the failed word and stack level. (The failed stack level may be determined from the following table.) When the logic analyzer has triggered, examine the status of A16U313-1 and U317-1. Both outputs should be low. If an output is high, suspect a defective RAM.

AD0(H)-AD8(H)	SP0(H)-SP3(H)
$0EB_{hex}$	F
$1DF_{hex}$	E
$1B6_{hex}$	D
$16D_{hex}$	C
$0D3_{hex}$	B
$1A6_{hex}$	A
$14D_{hex}$	9
092_{hex}	8
124_{hex}	7
049_{hex}	6
$09A_{hex}$	5
$13C_{hex}$	4
071_{hex}	3
$0E3_{hex}$	2
$1C7_{hex}$	1
$18E_{hex}$	0

853C Error Index

Explanation: The B-side circuitry failed to recognize all of the third set of 16 TPG words.

Probable Cause	Action
Faulty B-side sequential word recognizer circuitry.	Check the result address to determine the word causing the failure. While referring to the appropriate schematic, connect a logic analyzer to AD0(H)-AD8(H), A16U313-1, A16U317-1, and SP0(H)-SP3(H) on both U313 and U317. Set the logic analyzer timebase to a 20 μs sample rate and set it to trigger on the failed word and stack level. (The failed stack level may be determined from the following table.) When the logic analyzer has triggered, examine the status of A16U313-1 and U317-1. Both outputs should be low. If an output is high, suspect a defective RAM.

AD0(H)-AD8(H)	SP0(H)-SP3(H)
114_{hex}	F
028_{hex}	E
059_{hex}	D
$0BA_{hex}$	C
$17D_{hex}$	B
$0F3_{hex}$	A
$1E7_{hex}$	9
$1CF_{hex}$	8
196_{hex}	7
$12C_{hex}$	6
051_{hex}	5
$0A2_{hex}$	4
145_{hex}	3
$08A_{hex}$	2
$11C_{hex}$	1
030_{hex}	0

853D Error Index

Explanation: The B-side circuitry failed to recognize all of the fourth set of 16 TPG words.

Probable Cause	Action
Faulty B-side sequential word recognizer circuitry.	Check the result address to determine the word causing the failure. While referring to the appropriate schematic, connect a logic analyzer to AD0(H)-AD8(H), A16U313-1, A16U317-1, and SP0(H)-SP3(H) on both U313 and U317. Set the logic analyzer timebase to a 20 μs sample rate and set it to trigger on the failed word and stack level. (The failed stack level may be determined from the following table.) When the logic analyzer has triggered, examine the status of A16U313-1 and U317-1. Both outputs should be low. If an output is high, suspect a defective RAM.

AD0(H)-AD8(H)	SP0(H)-SP3(H)
061_{hex}	F
$0C3_{hex}$	E
186_{hex}	D
$10C_{hex}$	C
010_{hex}	B
020_{hex}	A
041_{hex}	9
082_{hex}	8
104_{hex}	7
008_{hex}	6
018_{hex}	5
038_{hex}	4
079_{hex}	3
$0FB_{hex}$	2
$1FF_{hex}$	1
$1F7_{hex}$	0

1240D2 18-CHANNEL BLOCK DIAGRAM
CHAINING – AREA 6

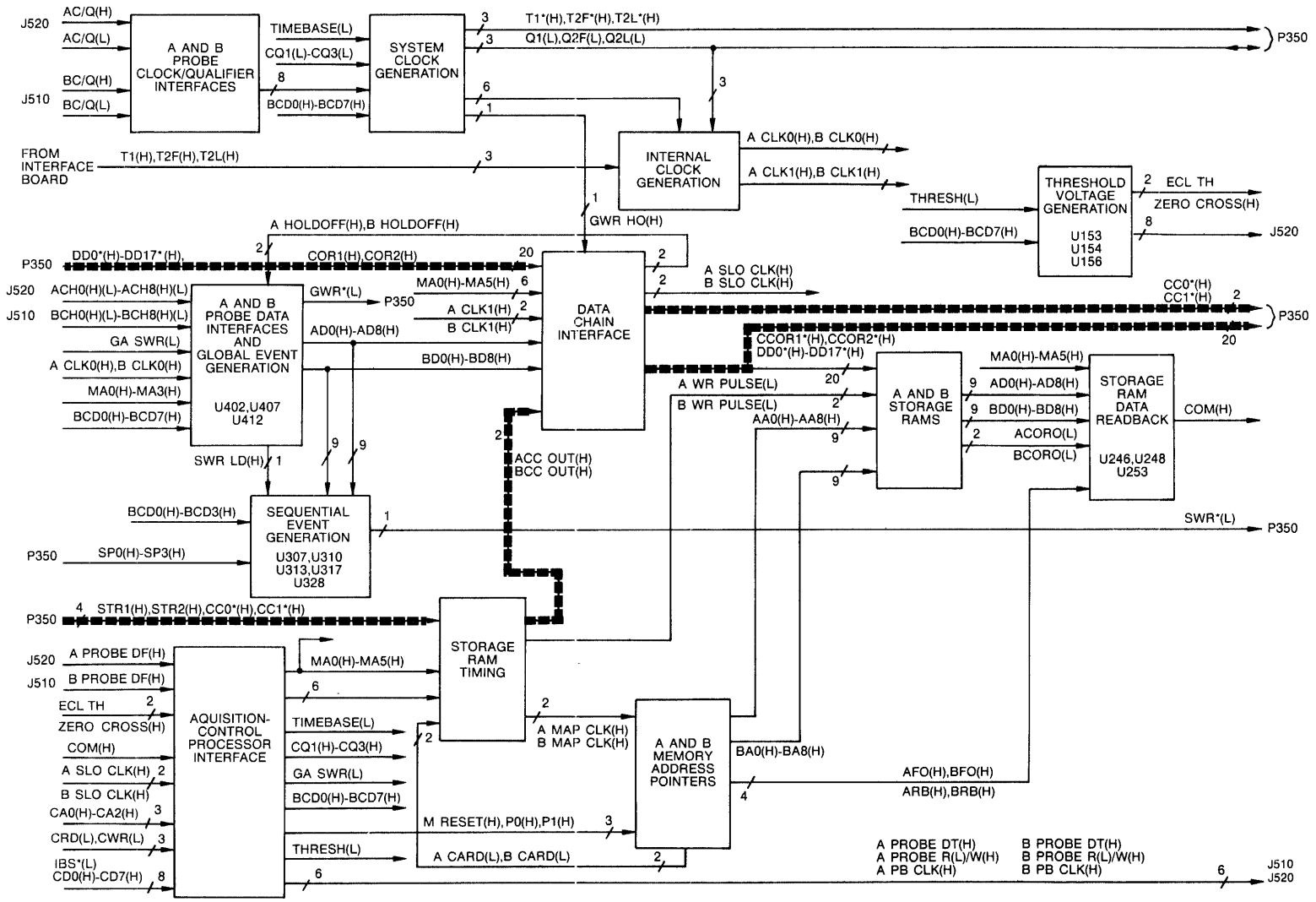


Figure 8-125. 18-Channel CHAINING block diagram.

4342-143

1240D2 18-CHANNEL ACQUISITION BOARD – COMPONENT LOCATION

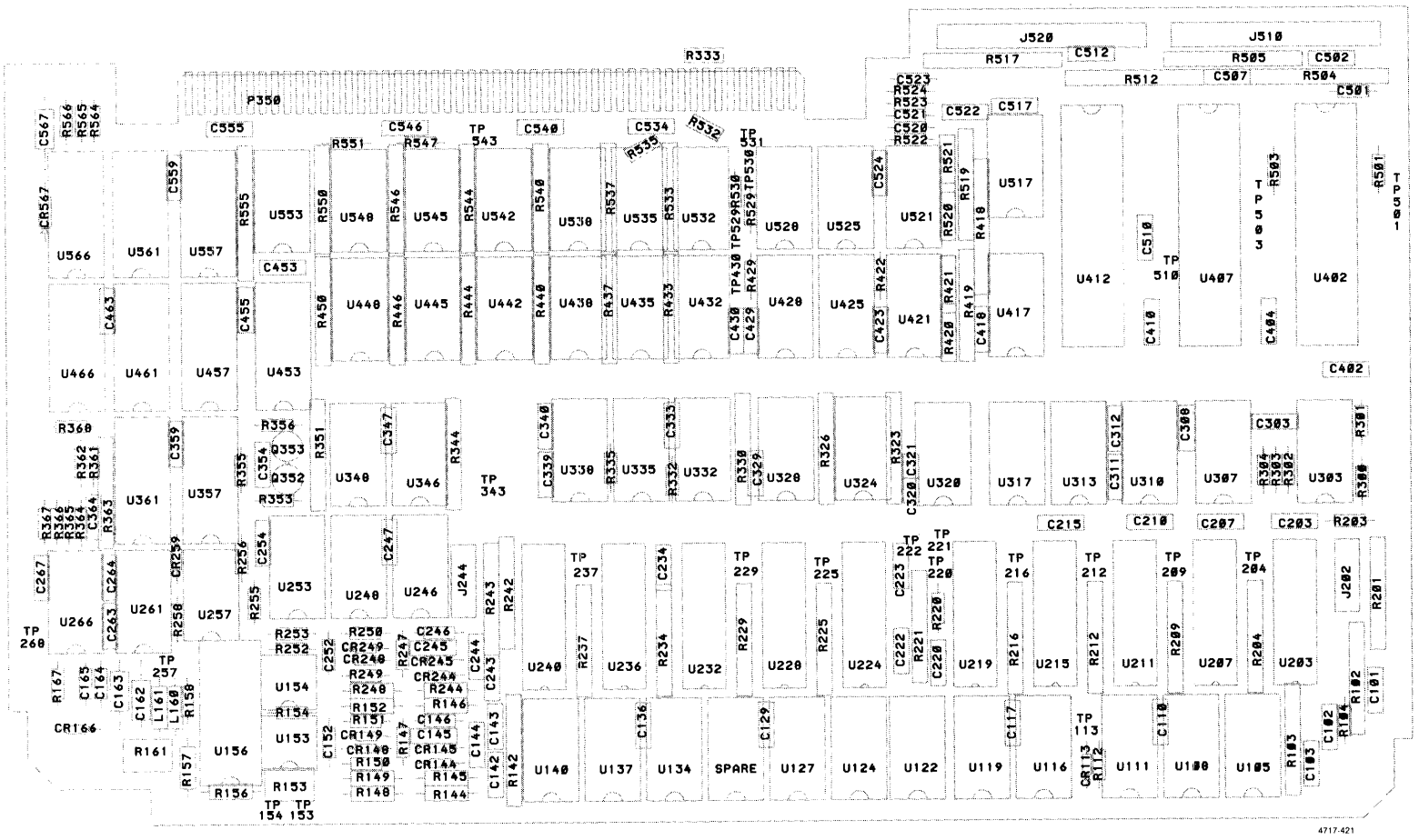


Figure 8-126. 18-Channel Acquisition Board component location.

module: 1240D2-X
area: CHAINING

CHAINING AREA – CIRCUIT OVERVIEW

The pattern-shaded signal lines on the chaining block diagram indicate circuitry used during diagnostic testing. Only the circuitry that is being exercised for the first time during diagnostic testing is shown. Circuitry exercised by other diagnostic tests are shown in their respective block diagrams.

Chaining of data from one acquisition board to the next is accomplished through the 18-Channel Acquisition Board's Data Chain Interface. The interface consists of two sets of data latches. The probe data latches A16U438, U442, U445, and U448 accept data from the Probe Data Interface for both A and B probes. Output from these latches is available for either the storage RAMs or the data chain bus if chaining is in progress. The chain bus latches A16U538, U542, U545, and U548 pass data to the next acquisition card in the data chain, allowing each acquisition card to chain data to the next like (18-channel) acquisition card.

NOTE

*Chaining of data from the first acquisition card to the next requires connecting data bus lines and control lines. To distinguish between each of the four identical acquisition board slots in the mainframe, the * symbol in a signal name takes on a letter from A to D. For example, the signal TEST*(H) is common to four different acquisition slots, but becomes TESTA(H) when referencing acquisition slot 0 (J250). The remaining designations are: * = B for slot 1 (J350), * = C for slot 2 (J450), and * = D for slot 3 (J550).*

The 18-channel's A- and B-side Memory Address Pointer (MAP) circuits are controlled by the P0(H) and P1(H) lines. The A- and B-side MAP circuits use the P0(H) and P1(H) lines to determine the number of chained acquisition cards. If both lines are set low (00 indicating no cards chained), the logic causes the counter to output an active AFO(H) Filled Once signal when the first acquisition card is filled with data. If the chain depth indicators were set to 11 (binary code indicating four cards chained), the filled-once signal would become active on this card after all cards in the acquisition chain were filled. As the storage RAM memory becomes full on each card, the MAP circuitry generates an active low signal on the ACARD(L) or BCARD(L) lines. These lines inhibit the acquisition memory storage clocks, preventing any further storage on that card.

CHAINING AREA – TEST DESCRIPTION

This test verifies the ability of the 18-Channel Acquisition cards to chain data from one card to another. Up to four boards may be tested, provided that they are installed into consecutive slots in the Interface Board. The acquisition board closest to the Trigger Board must have acquisition probes connecting it to the Test Pattern Generator (TPG).

NOTE

Due to the nature of the test, the error indexes generated for the Chaining area test are not unique. Error indexes generated for two chained acquisition cards are the same as for three and four chained cards. To properly access the correct error information, first locate the information pertaining to the number of acquisition cards in the chain. Once found, then locate the specific error index number and the corresponding error information.

The test checks the A side first and then the B side. The test programs the acquisition card to acquire data synchronously and to use the AT2LF(L) signal from A16U521 as the source for acquisition clocks. The TPG is programmed to use the processor-stepped T1 clock. Next, the processor reads the I.D. status from each acquisition board slot in the interface to determine the number of 18-channel cards in the chain. This also allows the test to determine the total chained memory length (1025 for 2 boards, 1537 for 3 boards, and 2049 for 4 boards). The processor clocks the TPG (memory depth +2) times, filling the A-side memory chain until all boards have been filled once. Then the processor reads the data back from the A-side storage RAMs and compares the results to correct TPG output patterns. If a problem is detected, the test is aborted and the failure is reported.

8611 Error Index

Explanation: The probe status indicates that no probes are connected to the acquisition card.

Probable Cause	Action
One or both of the probes is not connected, or a probe may be bad.	Examine the expected and actual screen data. If the expected result is 00_{hex} and the actual result is 40_{hex}, suspect the A-side probe. If the expected result is 00_{hex} and the actual result is 80_{hex}, suspect the B-side probe.
Suspect A16U457.	While looping on this test, check A16U457-9 for low-going pulses.
Suspect A16U561.	While looping on this test, check A16U561-1 for low-going pulses. If none are found, check A16U348 for correct operation. Also, check A16U561-8 and -12 for high-going pulses.

ERROR INDEXES FOR TWO 18-CHANNEL CARDS

8612 Error Index For Two 18-Channel Cards

Explanation: The A-side circuitry on the first acquisition board failed the test.

Probable Cause	Action
Faulty Data Chain Interface.	Suspect latches A16U438 and U442.

8613 Error Index For Two 18-Channel Cards

Explanation: The A-side circuitry on the second acquisition board failed the test.

Probable Cause	Action
Faulty Data Chain Interface.	Suspect latches A16U538 and U542 on the first 18-channel board in the chain. Also check that A16U346-2 outputs a 10 ns logic high pulse.

8614 Error Index For Two 18-Channel Cards

Explanation: The B-side circuitry on the first acquisition board failed the test.

Probable Cause	Action
Faulty Data Chain Interface.	Suspect latches A16U445 and U448.

8615 Error Index For Two 18-Channel Cards

Explanation: The B-side circuitry on the second acquisition board failed the test.

Probable Cause	Action
Faulty Data Chain Interface.	Suspect latches A16U545 and U548 on the first 18-channel board in the chain. Also check that A16U346-15 outputs a 10 ns logic high pulse.

ERROR INDEXES FOR THREE 18-CHANNEL CARDS

8612 Error Index For Three 18-Channel Cards

Explanation: The A-side circuitry on the first acquisition board failed the test.

Probable Cause	Action
Faulty Data Chain Interface.	Suspect latches A16U438 and U442.

8613 Error Index For Three 18-Channel Cards

Explanation: The A-side circuitry on the second acquisition board failed the test.

Probable Cause	Action
Faulty Data Chain Interface.	Suspect latches A16U538 and U542 on the first chained 18-channel board. Also check that A16U346-2 outputs a 10 ns logic high pulse.

8614 Error Index For Three 18-Channel Cards

Explanation: The A-side circuitry on the third acquisition board failed the test.

Probable Cause	Action
Faulty Data Chain Interface.	Suspect latches A16U538 and U542 on the second 18-channel board in the chain.

8615 Error Index For Three 18-Channel Cards

Explanation: The B-side circuitry on the first acquisition board failed the test.

Probable Cause	Action
Faulty Data Chain Interface.	Suspect latches A16U445 and U448.

8616 Error Index For Three 18-Channel Cards

Explanation: The B-side circuitry on the second acquisition board failed the test.

Probable Cause	Action
Faulty Data Chain Interface.	Suspect latches A16U545 and U548 on the first chained 18-channel board. Also check that A16U346-15 outputs a 10 ns logic high pulse.

8617 Error Index For Three 18-Channel Cards

Explanation: The B-side circuitry on the third acquisition board failed the test.

Probable Cause	Action
Faulty Data Chain Interface.	Suspect latches A16U545 and U548 on the second 18-channel board in the chain.

ERROR INDEXES FOR FOUR 18-CHANNEL CARDS

8612 Error Index For Four 18-Channel Cards

Explanation: The A-side circuitry on the first acquisition board failed the test.

Probable Cause	Action
Faulty Data Chain Interface.	Suspect latches A16U438 and U442.

8613 Error Index For Four 18-Channel Cards

Explanation: The A-side circuitry on the second acquisition board failed the test.

Probable Cause	Action
Faulty Data Chain Interface.	Suspect latches A16U538 and U542 on the first 18-channel board. Also check that A16U346-2 outputs a 10 ns logic high pulse. Also, run the acquisition RAM test for the second board in the chain to ensure correct operation in the unchained mode.

8614 Error Index For Four 18-Channel Cards

Explanation: The A-side circuitry on the third acquisition board failed the test.

Probable Cause	Action
Faulty Data Chain Interface.	Suspect latches A16U538 and U542 on the second 18-channel board in the chain. Also, run the acquisition RAM test for the third board in the chain to ensure correct operation in the unchained mode.

8615 Error Index For Four 18-Channel Cards

Explanation: The A-side circuitry on the fourth acquisition board failed the test.

Probable Cause	Action
Faulty Data Chain Interface.	Suspect latches A16U538 and U542 on the third 18-channel board in the chain. Also, run the acquisition RAM test for the fourth board in the chain to ensure correct operation in the unchained mode.

8616 Error Index For Four 18-Channel Cards

Explanation: The B-side circuitry on the first acquisition board failed the test.

Probable Cause	Action
Faulty Data Chain Interface.	Suspect latches A16U445 and U448.

8617 Error Index For Four 18-Channel Cards

Explanation: The B-side circuitry on the second acquisition board failed the test.

Probable Cause	Action
Faulty Data Chain Interface.	Suspect latches A16U545 and U548 on the first 18-channel board in the chain. Also check that A16U346-2 outputs a 10 ns logic high pulse. Also, run the acquisition RAM test for the second board in the chain to ensure correct operation in the unchained mode.

8618 Error Index For Four 18-Channel Cards

Explanation: The B-side circuitry on the third acquisition board failed the test.

Probable Cause	Action
Faulty Data Chain Interface.	Suspect latches A16U545 and U548 on the second 18-channel board in the chain. Also, run the acquisition RAM test for the third board in the chain to ensure correct operation in the unchained mode.

8619 Error Index For Four 18-Channel Cards

Explanation: The B-side circuitry on the fourth acquisition board failed the test.

Probable Cause	Action
Faulty Data Chain Interface.	Suspect latches A16U545 and U548 on the third 18-channel board in the chain. Also, run the acquisition RAM test for the fourth board in the chain to ensure correct operation in the unchained mode.

1240D2 18-CHANNEL BLOCK DIAGRAM
CALIBRATE – AREA 7

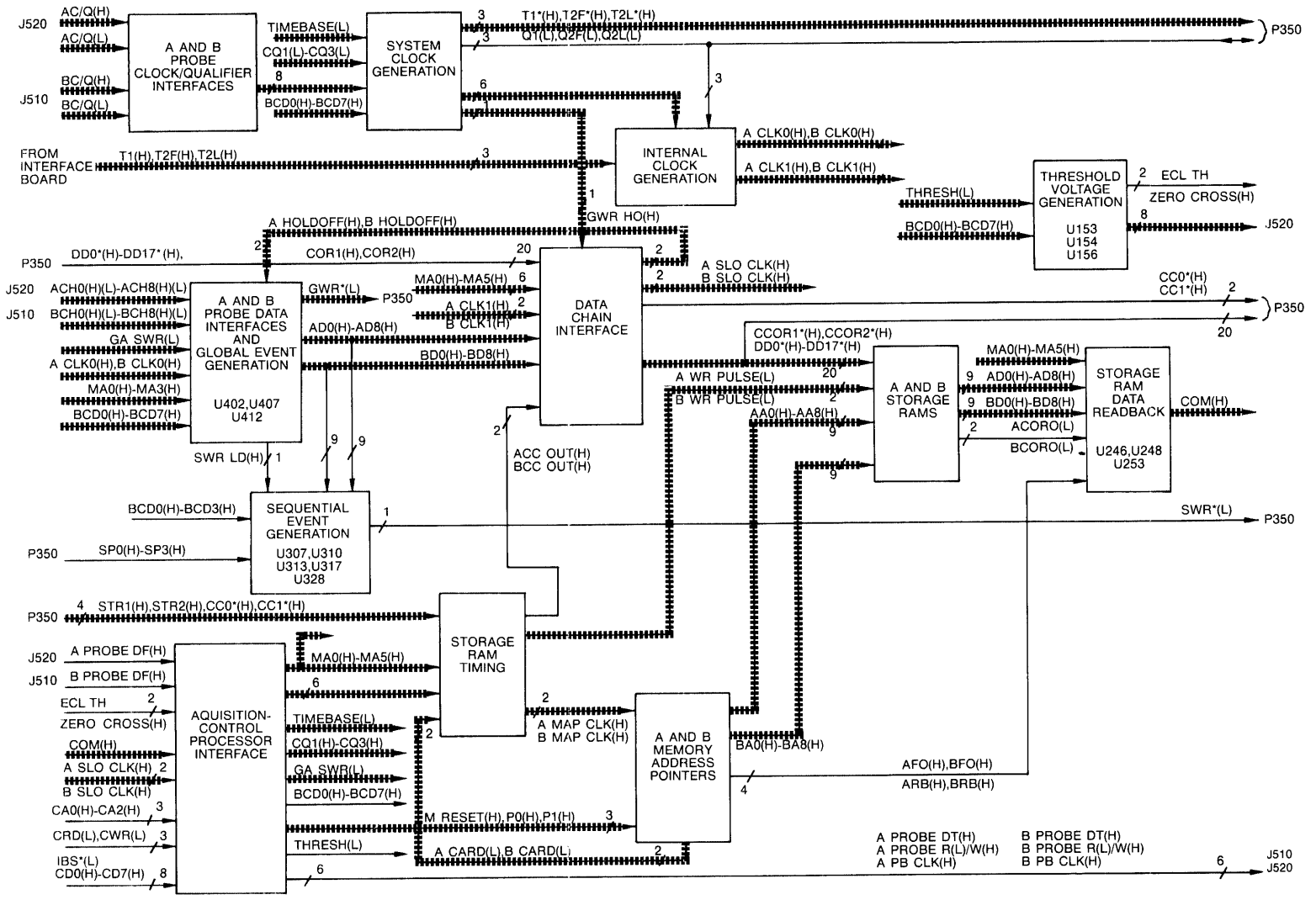


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Figure 8-127. 18-Channel CALIBRATE block diagram.

1240D2 18-CHANNEL ACQUISITION BOARD – COMPONENT LOCATION

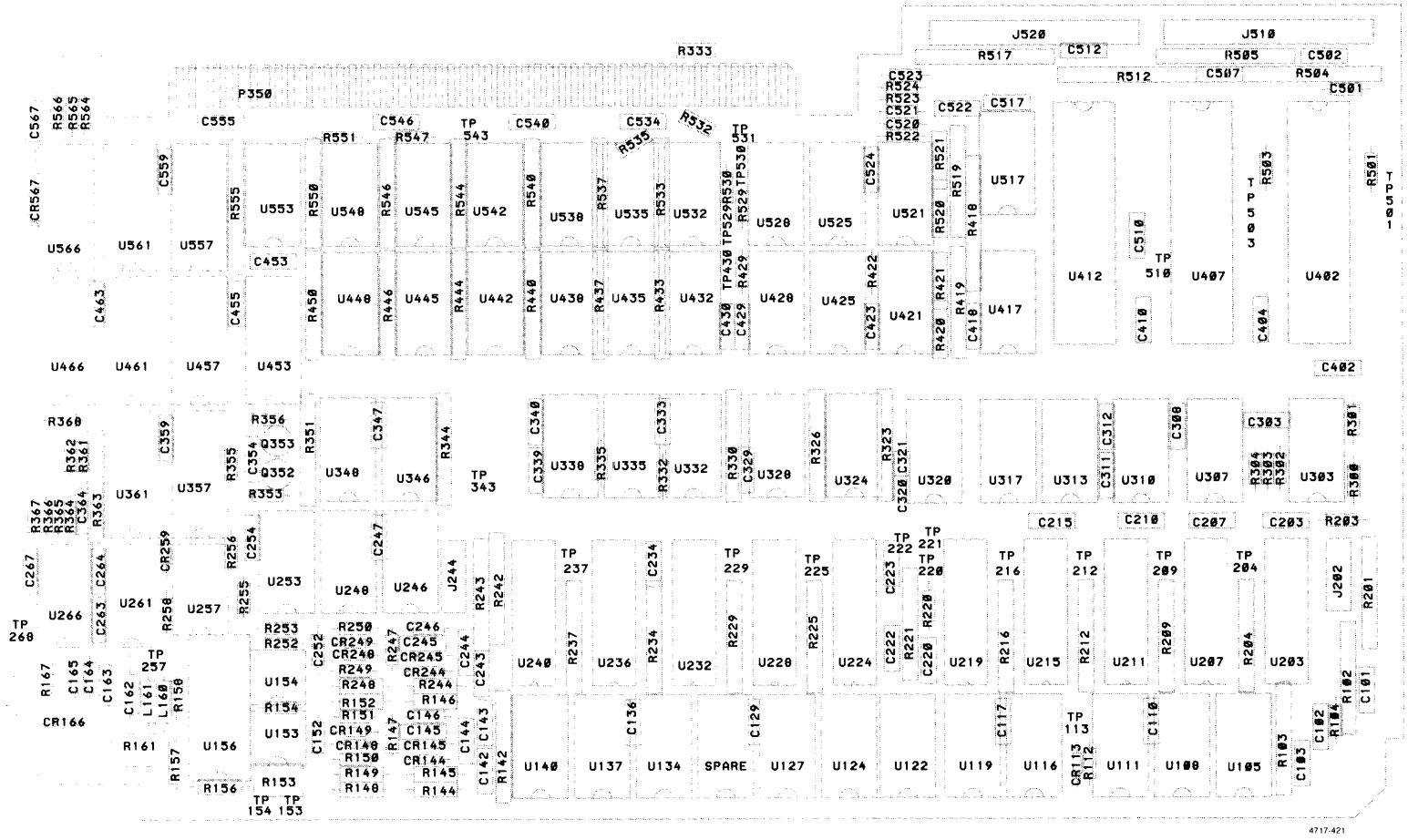


Figure 8-128. 18-Channel Acquisition Board component location.

module: 1240D2-X
area: CALIBRATE

CALIBRATE AREA – CIRCUIT OVERVIEW

The pattern-shaded signal lines on the calibrate block diagram indicate circuitry previously tested by test Area 2, ACQ RAM, and Area 4, X ACQ RAM. In this case, shading does not indicate circuitry exercised for the first time during diagnostic testing, but instead shows the test path.

Since the circuitry involved during these 87XX diagnostic tests is basically the same as that used during the 82XX and 84XX diagnostic tests, circuit descriptions are not repeated here.

CALIBRATE AREA – TEST DESCRIPTION

The calibrate area test is used to calibrate signal delay through 18-channel gate arrays A16U402, U407, and U412. Once calibrated, the delay through all three gate arrays is equal. To observe the calibrated gate-array delay value, run the CAL ACQ18 area test (routine 2). The CAL ACQ18 area test provides information describing the results of the calibration procedure. The gate arrays are automatically calibrated by the operating firmware prior to each acquisition.

NOTE

Failures found during this test are reported differently than in other diagnostic tests. This test reports only the last failure found, instead of the first failure found. This keeps a bad gate array found early in the test from preventing calibration of the remaining gate arrays.

The test checks one gate array at a time. First, the test programs the gate array under test for a pre-determined amount of delay time. (The delay time is the time it takes a signal to pass through the gate array.) This delay value is actually the mid-point value of the total possible range of values. The acquisition card is set up to allow the gate array to oscillate internally. The oscillations produce logic-low pulses on the A-side Global Word Recognizer (GWR) outputs (pin 23 on each of the gate arrays). The GWR is programmed to all Xs (don't cares) except for one input channel on each gate array (channel 0 for U412, channel 3 for U407, and channel 6 for U402). The trigger circuitry is programmed to trigger after recognizing 90 global events on the GWR*(L) line. If no trigger occurs, an error is generated. If an error is found during the calibration of the first gate array, the error is recorded and the next gate array is calibrated. If there are multiple errors, only the last error found is reported.

When a trigger occurs, the Control Processor counts the number of reads it must perform to reach the maximum MAP count. With this information, the test calculates the number of times the MAP was incremented during the test. From this, the trigger position is calculated. The test then verifies that the MAP count (or essentially the trigger position) was within an allowable count range (199_{hex} maximum count to 177_{hex} minimum count). If the MAP count was higher than the allowable limit, then the test is run again with less delay time programmed into the gate arrays. If the MAP count was lower than the minimum value, the routine is run again with more delay programmed into the gate arrays. If the MAP count was too low (less than 20_{hex}), the test is aborted and the failure is reported.

The test will continue to try different gate-array delay values until the correct delay is found. If the gate array delay value found is found to be at the minimum or maximum value and the MAP is not within the allowable limit, an error is recorded and the delay value is left at its limit (00 or 0F). If the proper delay value cannot be found, the delay programmed into the gate arrays is set to the mid-point of the possible range of delay values: 08 - 0000 (as displayed by the CAL ACQ18 diagnostic test).

8711 Error Index

Explanation: No trigger occurred within the time limit.

Probable Cause	Action
Defective the Counter/Timer circuit in the Trigger module.	Run the diagnostic tests for the Trigger module.
Defective gate array.	Run routine 2 of the CAL ACQ18 area test. Resulting information should point to defective gate array.

8712 Error Index

Explanation: The AFO(H) A-side filled once signal is stuck at a logic high.

Probable Cause	Action
Defective Memory Address Pointer (MAP) circuit.	Run the diagnostic tests for the MAP circuits.

8713 Error Index

Explanation: The ARB(H) A-side readback signal is stuck at a logic high.

Probable Cause	Action
Defective Memory Address Pointer (MAP) circuit.	Run the diagnostic tests for the MAP circuits.

8714 Error Index

Explanation: The ARB(H) A-side readback signal never became high true during the entire range of the MAP count.

Probable Cause	Action
Defective Memory Address Pointer (MAP) circuit.	Run the diagnostic tests for the MAP circuits.

8715 Error Index

Explanation: The MAP value read was too low (less than 20_{hex}).

Probable Cause	Action
Defective gate array.	Run routine 2 of the CAL ACQ18 area test. Resulting information should point to defective gate array.
Defective the Counter/Timer circuit in the Trigger module.	Run the diagnostic tests for the Trigger module.

8716 Error Index

Explanation: The MAP value read was too high (199_{hex} maximum).

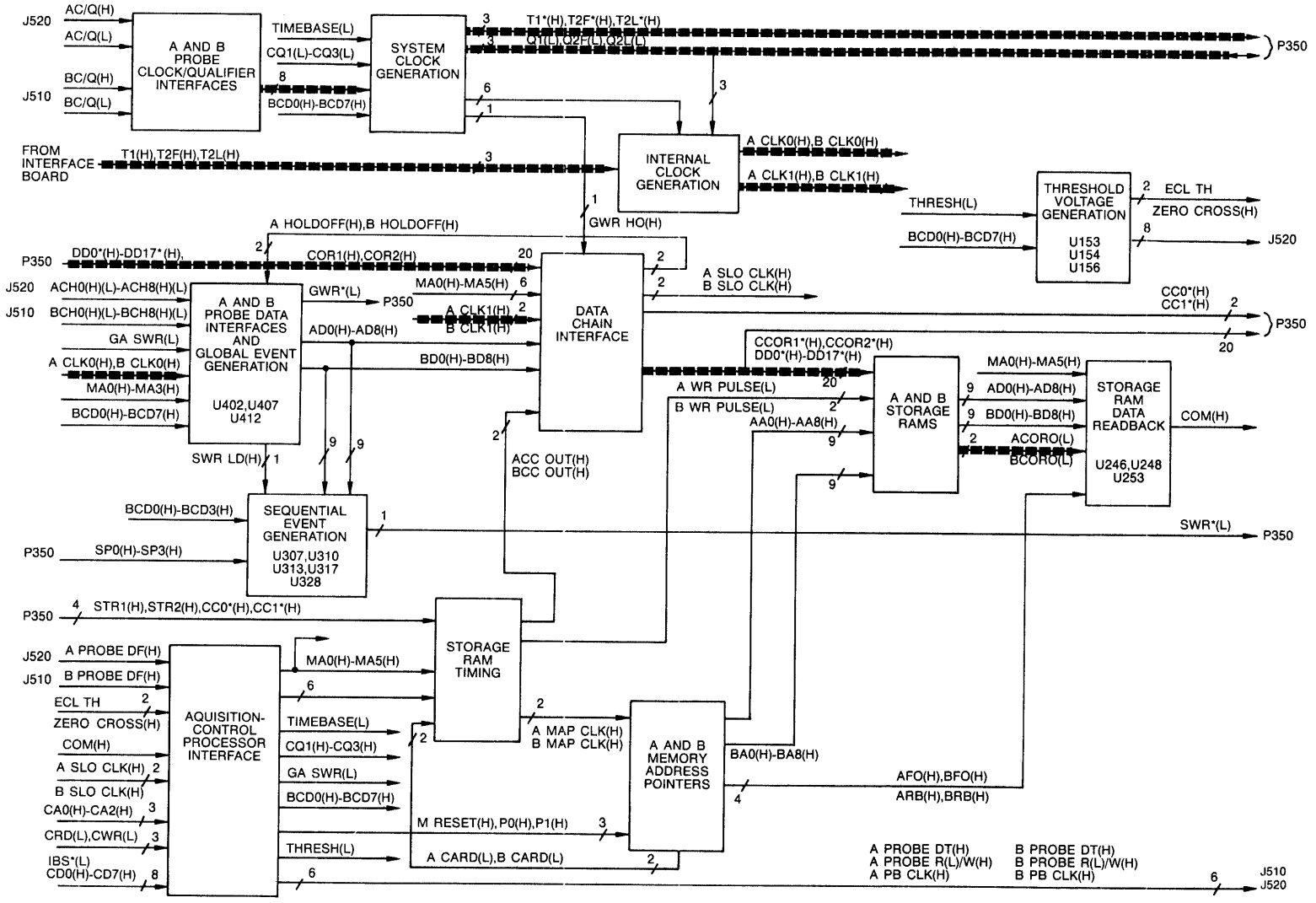
Probable Cause	Action
Defective gate array.	Run routine 2 of the CAL ACQ18 area test. Resulting information should point to defective gate array.

8717 Error Index

Explanation: The MAP value read was too low (177_{hex} minimum).

Probable Cause	Action
Defective gate array.	Run routine 2 of the CAL ACQ18 area test. Resulting information should point to defective gate array.

1240D2 18-CHANNEL BLOCK DIAGRAM
TIMING – AREA 8



4342-145

Figure 8-129. 18-Channel TIMING block diagram.

1240D2 18-CHANNEL ACQUISITION BOARD – COMPONENT LOCATION

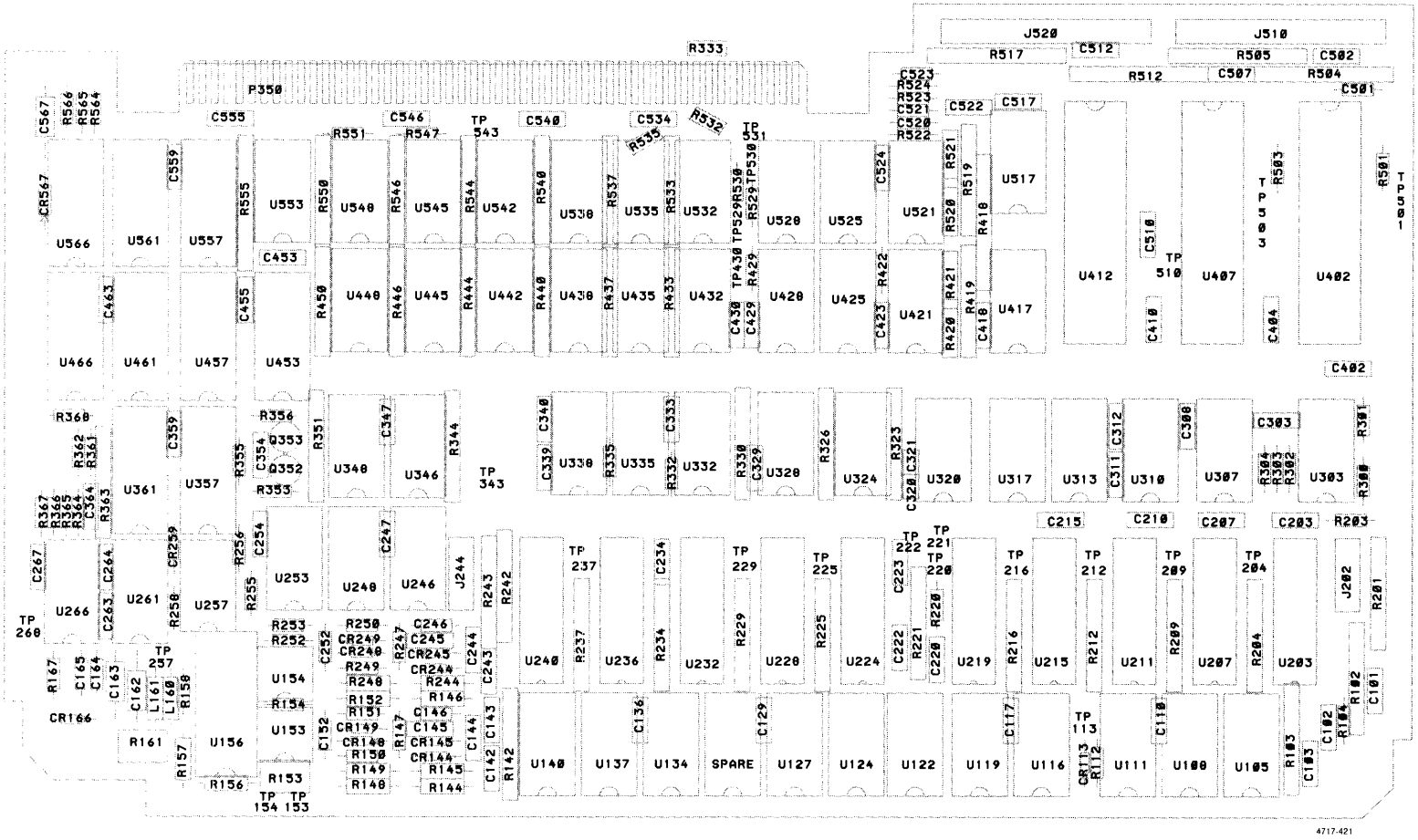


Figure 8-130. 18-Channel Acquisition Board component location.

module: 1240D2-X
area: TIMING

TIMING AREA – CIRCUIT OVERVIEW

The pattern-shaded signal lines on the timing block diagram indicate circuitry used during diagnostic testing. Only the circuitry that is being exercised for the first time during diagnostic testing is shown. Circuitry exercised by other diagnostic tests are shown in their respective block diagrams. A- and B-side circuits are duplicates of each other; therefore, circuitry discussion may exclude references to the B side.

Line receivers in the Probe Clock/Qualifier Interface accept clock/qualifier signals from the connected A-side probe. The resulting signals are used for the generation of T clocks and Q qualifiers in the System Clock Generation circuitry. The falling edge of a signal on the C/Q line causes U417B pin 7 to go low. The delay-invert path through U417C and U417A pulls the active low signal line high again. The T-pulse rising and falling edge output signals serve as clock pulses for the System Clock Generation circuitry. The clock pulses may be gated onto the specified timebase (T) bus by the System Clock Generation circuitry. Outputs from U417C are also the Q-bus qualifiers that qualify the timebase selections.

The System Clock Generation circuitry accepts the Timebase menu setup-selections. These selections are sent by the Control Processor to latches A16U566, U357, and U453. The latch outputs are sent, along with T-clock and Q-qualifier signals from the Probe Clock/Qualifier Interface, to the OR-AND-INVERT gates A16U532, U428, U521, U435, U432, and U425. These gates produce a total of six outputs that allow chosen T clocks and Q qualifiers (none, any, or all) to be gated onto their respective buses. All active high T-bus signals are ORed together on the Interface Board, allowing T-bus clocks from any installed acquisition cards to contribute to the generation of the master sample clock (for the gate arrays in the Probe Data Interface). In addition, all active low Q-bus signals are ANDed together on the Interface Board.

TIMING AREA – TEST DESCRIPTION

The timing test consists of three routines. Routine 1 verifies setup times for T-clocks T1 and T2L and hold times for T-clocks T1, T2F, and T2L. Routine 2 verifies setup times for Q-qualifiers Q1 and Q2L and hold times for Q-qualifers Q1, Q2F, and Q2L. Routine 3 provides a functional timing test of the correlate memory circuitry. All routines require that input probes be used to connect the 18-Channel Acquisition card to the Test Pattern Generator (TPG).

NOTE

The TPG must be calibrated in order for the timing tests to pass. TPG calibration procedures are outlined as a part of the Trigger Board adjustments, in the Verification And Adjustment Procedures *section of this manual. If the TPG is suspected of being out of calibration (due to test failures), refer to these calibration procedures.*

ROUTINE 1 – TEST DESCRIPTION

This routine verifies setup times for T-clocks T1 and T2L and hold times for T-clocks T1, T2F, and T2L. The test checks the A side of acquisition memory first and then the B side.

The test begins by checking the A-side T1 clock hold times. First, the test selects the A-side T1 clock to be generated on the rising edge of the TPG clock. Now, the TPG data is acquired using this T1 clock. The acquired data is compared to the correct TPG pattern and if a problem is found, the test is aborted and the failure is reported.

The A-side T1 clock setup time is tested by generating T1 on the falling edge of the TPG clock. Again, the TPG data is acquired using this T1 clock. The acquired data is compared to the correct TPG pattern and, if a problem is found, the test is aborted and the failure is reported.

Testing of the A-side T2F clock hold time is done in the same manner by generating T2F on the rising edge of the TPG clock. The T2F setup time is not tested. Just as the others are checked, the A-side T2L clock hold time is verified by generating T2L on the rising edge of the TPG clock. The A-side T2L clock setup time is tested by generating T2L on the falling edge of the TPG clock.

If a failure is detected during any part of the test, the test is aborted and the failure is reported.

8811 Error Index

Explanation: The test failed to detect both acquisition probes.

Probable Cause	Action
One or both of the probes is not connected, or a probe may be bad.	Examine the expected and actual screen data. If the expected result is 00_{hex} and the actual result is 40_{hex}, suspect the A-side probe. If the expected result is 00_{hex} and the actual result is 80_{hex}, suspect the B-side probe.
Suspect A16U457.	While looping on this test, check A16U457-9 for low-going pulses.
Suspect A16U561.	While looping on this test, check A16U561-1 for low-going pulses. If none are found, check A16U348 for correct operation. Also, check A16U561-8 and -12 for high-going pulses.

8812 Error Index

Explanation: The A-side acquisition circuitry failed the T1 clock hold time test.

Probable Cause	Action
There was no T1 clock generated or the wrong clock was generated.	Check for T1 clock on pin 32 of any gate array (A16U402, U407, or U412). Check A16U532-3 for a clock signal. Check A16U532-7 for a low when the test stops due to a failure.
Suspect the gate arrays A16U412, U407, and U402. Also suspect A16U438, U442, U532, or the A-side of acquisition memory.	Check the expected and actual results. Convert the failed bit information, displayed as a hexadecimal number, to a binary number. By examining the bit pattern, the failed channel may be identified.

8813 Error Index

Explanation: The B-side acquisition circuitry failed the T1 clock hold time test.

Probable Cause	Action
There was no T1 clock generated or the wrong clock was generated.	Suspect the gate arrays A16U412, U407, and U402. Also suspect A16U445, U448, U532, or the B-side of acquisition memory. Check the expected and actual results. Convert the failed bit information, displayed as a hexadecimal number, to a binary number. By examining the bit pattern, the failed channel may be identified.

8814 Error Index

Explanation: The A-side acquisition circuitry failed the T1 clock setup time test.

Probable Cause	Action
There was no T1 clock generated or the wrong clock was generated.	Check for T1 clock on pin 32 of any gate array (A16U402, U407, or U412). Check A16U532-3 for a clock signal. Check A16U532-4 for a low when the test stops due to a failure.
Suspect the gate arrays A16U412, U407, and U402. Also suspect A16U445, U448, U532, or the A-side of acquisition memory.	Check the expected and actual results. Convert the failed bit information, displayed as a hexadecimal number, to a binary number. By examining the bit pattern, the failed channel may be identified.

8815 Error Index

Explanation: The B-side acquisition circuitry failed the T1 clock setup time test.

Probable Cause	Action
There was no T1 clock generated or the wrong clock was generated.	Suspect the gate arrays A16U412, U407, and U402. Also suspect A16U445, U448, U532, or the B-side of acquisition memory. Check the expected and actual results. Convert the failed bit information, displayed as a hexadecimal number, to a binary number. By examining the bit pattern, the failed channel may be identified.

8816 Error Index

Explanation: The A-side acquisition circuitry failed the T2F clock hold time test.

Probable Cause	Action
There was no T2F clock generated or the wrong clock was generated.	Check for T2F clock on pin 32 of any gate array (A16U402, U407, or U412). Check A16U428-3 for a clock signal. Check A16U428-9 for a low when the test stops due to a failure.
Suspect the gate arrays A16U412, U407, and U402. Also suspect A16U438, U442, U428, or the A-side of acquisition memory.	Check the expected and actual results. Convert the failed bit information, displayed as a hexadecimal number, to a binary number. By examining the bit pattern, the failed channel may be identified.

8817 Error Index

Explanation: The B-side acquisition circuitry failed the T2F clock hold time test.

Probable Cause	Action
There was no T2F clock generated or the wrong clock was generated.	Suspect the gate arrays A16U412, U407, and U402. Also suspect A16U445, U448, U428, or the B-side of acquisition memory. Check the expected and actual results. Convert the failed bit information, displayed as a hexadecimal number, to a binary number. By examining the bit pattern, the failed channel may be identified.

8818 Error Index

Explanation: The A-side acquisition circuitry failed the T2L clock hold time test.

Probable Cause	Action
There was no T2L clock generated or the wrong clock was generated.	Check for T2L clock on pin 32 of any gate array (A16U402, U407, or U412). Check A16U521-3 for a clock signal. Check A16U521-14 for a low when the test stops due to a failure.
Suspect the gate arrays A16U412, U407, and U402. Also suspect A16U438, U442, U521, or the A-side of acquisition memory.	Check the expected and actual results. Convert the failed bit information, displayed as a hexadecimal number, to a binary number. By examining the bit pattern, the failed channel may be identified.

8819 Error Index

Explanation: The B-side acquisition circuitry failed the T2L clock hold time test.

Probable Cause	Action
There was no T2L clock generated or the wrong clock was generated.	Suspect the gate arrays A16U412, U407, and U402. Also suspect A16U445, U448, U521, or the B-side of acquisition memory. Check the expected and actual results. Convert the failed bit information, displayed as a hexadecimal number, to a binary number. By examining the bit pattern, the failed channel may be identified.

881A Error Index

Explanation: The A-side acquisition circuitry failed the T2L clock setup time test.

Probable Cause	Action
There was no T2L clock generated or the wrong clock was generated.	Check for T2L clock on pin 32 of any gate array (A16U402, U407, or U412). Check A16U521-3 for a clock signal. Check A16U521-4 for a low when the test stops due to a failure.
Suspect the gate arrays A16U412, U407, and U402. Also suspect A16U438, U442, U521, or the A-side of acquisition memory.	Check the expected and actual results. Convert the failed bit information, displayed as a hexadecimal number, to a binary number. By examining the bit pattern, the failed channel may be identified.

881B Error Index

Explanation: The B-side acquisition circuitry failed the T2L clock setup time test.

Probable Cause	Action
There was no T2L clock generated or the wrong clock was generated.	Suspect the gate arrays A16U412, U407, and U402. Also suspect A16U445, U448, U521, or the B-side of acquisition memory. Check the expected and actual results. Convert the failed bit information, displayed as a hexadecimal number, to a binary number. By examining the bit pattern, the failed channel may be identified.

ROUTINE 2 – TEST DESCRIPTION

This routine verifies setup times for Q-qualifiers Q1 and Q2L and hold times for Q-qualifiers Q1, Q2F, and Q2L. These are the Q bus signals that qualify the timebase selections. This routine requires that input probes be used to connect the 18-Channel Acquisition card to the Test Pattern Generator (TPG).

NOTE

The TPG must be calibrated in order for the timing tests to pass. TPG calibration procedures are outlined as a part of the Trigger Board adjustments, in the Verification And Adjustment Procedures *section of this manual. If the TPG is suspected of being out of calibration (due to test failures), refer to these calibration procedures.*

The test begins by checking the A- and B-side Q1 qualifier hold times. First, the test selects the A-side Q1L qualifier and the T1R clock to be generated on the rising edge of the TPG clock. Now, the TPG data is acquired using this T1R clock. The acquired data in both A and B memories is compared to the correct TPG pattern and, if a problem is found, the test is aborted and the failure is reported.

The Q1 qualifier setup time is tested by generating the Q1H qualifier and the T1F clock on the falling edge of the TPG clock. Again, the TPG data is acquired using this T1F clock. The acquired data in both A and B memories is compared to the correct TPG pattern and, if a problem is found, the test is aborted and the failure is reported.

Testing of the Q2F qualifier hold times is done in the same manner by generating the Q2FL qualifier and the T2FR clock on the rising edge of the TPG clock. The Q2F qualifier setup time is not tested.

Just as the others are checked, the Q2L clock hold times are verified by generating the Q2LH qualifier and T2LR clock on the rising edge of the TPG clock. The Q2L qualifier setup times are tested by generating the Q2LL qualifier and the T2LF clock on the falling edge of the TPG clock.

If a failure is detected during any part of the test, the test is aborted and the failure is reported.

8821 Error Index

Explanation: The test failed to detect both acquisition probes.

Probable Cause	Action
One or both of the probes is not connected, or a probe may be bad.	Examine the expected and actual screen data. If the expected result is 00_{hex} and the actual result is 40_{hex}, suspect the A-side probe. If the expected result is 00_{hex} and the actual result is 80_{hex}, suspect the B-side probe.
Suspect A16U457.	While looping on this test, check A16U457-9 for low-going pulses.
Suspect A16U561.	While looping on this test, check A16U561-1 for low-going pulses. If none are found, check A16U348 for correct operation. Also, check A16U561-8 and -12 for high-going pulses.

8822 Error Index

Explanation: The A-side acquisition circuitry failed the Q1 qualifier hold time test.

Probable Cause	Action
There was no clock generated or the wrong clock was generated.	Check for clock on pin 32 of any gate array (A16U402, U407, or U412). Check A16U435-3 for a clock signal. Check A16U435-7 for a low when the test stops due to a failure.
Suspect the gate arrays A16U412, U407, and U402. Also suspect A16U438, U442, U435, or the A-side of acquisition memory.	Check the expected and actual results. Convert the failed bit information, displayed as a hexadecimal number, to a binary number. By examining the bit pattern, the failed channel may be identified.

8823 Error Index

Explanation: The B-side acquisition circuitry failed the Q1 qualifier hold time test.

Probable Cause	Action
There was no clock generated or the wrong clock was generated.	Suspect the gate arrays A16U412, U407, and U402. Also suspect A16U445, U448, U435, or the B-side of acquisition memory. Check the expected and actual results. Convert the failed bit information, displayed as a hexadecimal number, to a binary number. By examining the bit pattern, the failed channel may be identified.

8824 Error Index

Explanation: The A-side acquisition circuitry failed the Q1 qualifier setup time test.

Probable Cause	Action
There was no clock generated or the wrong clock was generated.	Check for clock on pin 32 of any gate array (A16U402, U407, or U412). Check A16U435-3 for a clock signal. Check A16U435-4 for a low when the test stops due to a failure.
Suspect the gate arrays A16U412, U407, and U402. Also suspect A16U438, U442, U435, or the A-side of acquisition memory.	Check the expected and actual results. Convert the failed bit information, displayed as a hexadecimal number, to a binary number. By examining the bit pattern, the failed channel may be identified.

8825 Error Index

Explanation: The B-side acquisition circuitry failed the Q1 qualifier setup time test.

Probable Cause	Action
There was no clock generated or the wrong clock was generated.	Suspect the gate arrays A16U412, U407, and U402. Also suspect A16U445, U448, U435, or the B-side of acquisition memory. Check the expected and actual results. Convert the failed bit information, displayed as a hexadecimal number, to a binary number. By examining the bit pattern, the failed channel may be identified.

8826 Error Index

Explanation: The A-side acquisition circuitry failed the Q2F qualifier hold time test.

Probable Cause	Action
There was no clock generated or the wrong clock was generated.	Check for T2F clock on pin 32 of any gate array (A16U402, U407, or U412). Check A16U432-3 for a clock signal. Check A16U432-7 for a low when the test stops due to a failure.
Suspect the gate arrays A16U412, U407, and U402. Also suspect A16U438, U442, U432, or the A-side of acquisition memory.	Check the expected and actual results. Convert the failed bit information, displayed as a hexadecimal number, to a binary number. By examining the bit pattern, the failed channel may be identified.

8827 Error Index

Explanation: The B-side acquisition circuitry failed the Q2F qualifier hold time test.

Probable Cause	Action
There was no clock generated or the wrong clock was generated.	Suspect the gate arrays A16U412, U407, and U402. Also suspect A16U445, U448, U432, or the B-side of acquisition memory. Check the expected and actual results. Convert the failed bit information, displayed as a hexadecimal number, to a binary number. By examining the bit pattern, the failed channel may be identified.

8828 Error Index

Explanation: The A-side acquisition circuitry failed the Q2L qualifier hold time test.

Probable Cause	Action
There was no clock generated or the wrong clock was generated.	Check for clock on pin 32 of any gate array (A16U402, U407, or U412). Check A16U425-3 for a clock signal. Check A16U425-12 for a low when the test stops due to a failure.
Suspect the gate arrays A16U412, U407, and U402. Also suspect A16U438, U442, U425, or the A-side of acquisition memory.	Check the expected and actual results. Convert the failed bit information, displayed as a hexadecimal number, to a binary number. By examining the bit pattern, the failed channel may be identified.

8829 Error Index

Explanation: The B-side acquisition circuitry failed the Q2L qualifier hold time test.

Probable Cause	Action
There was no clock generated or the wrong clock was generated.	Suspect the gate arrays A16U412, U407, and U402. Also suspect A16U445, U448, U425, or the B-side of acquisition memory. Check the expected and actual results. Convert the failed bit information, displayed as a hexadecimal number, to a binary number. By examining the bit pattern, the failed channel may be identified.

882A Error Index

Explanation: The A-side acquisition circuitry failed the Q2L qualifier setup time test.

Probable Cause	Action
There was no clock generated or the wrong clock was generated.	Check for clock on pin 32 of any gate array (A16U402, U407, or U412). Check A16U425-3 for a clock signal. Check A16U425-13 for a low when the test stops due to a failure.
Suspect the gate arrays A16U412, U407, and U402. Also suspect A16U438, U442, U425, or the A-side of acquisition memory.	Check the expected and actual results. Convert the failed bit information, displayed as a hexadecimal number, to a binary number. By examining the bit pattern, the failed channel may be identified.

882B Error Index

Explanation: The B-side acquisition circuitry failed the Q2L qualifier setup time test.

Probable Cause	Action
There was no clock generated or the wrong clock was generated.	Suspect the gate arrays A16U412, U407, and U402. Also suspect A16U445, U448, U425, or the B-side of acquisition memory. Check the expected and actual results. Convert the failed bit information, displayed as a hexadecimal number, to a binary number. By examining the bit pattern, the failed channel may be identified.

ROUTINE 3 - TEST DESCRIPTION

This routine provides a functional test of the correlate memory circuitry and the T-bus clocks at 12 MHz. The test requires that input probes be used to connect the 18-Channel Acquisition card to the Test Pattern Generator (TPG).

NOTE

The TPG must be calibrated in order for the timing tests to pass. TPG calibration procedures are outlined as a part of the Trigger Board adjustments, in the Verification And Adjustment Procedures *section of this manual. If the TPG is suspected of being out of calibration (due to test failures), refer to these calibration procedures.*

CCOR1*(H) and CCOR2*(H) are correlation chaining signals that carry correlation information from the Data Chain Interface to the next acquisition card (which is not tested) in the chain. The correlation information, stored in the storage RAMs, is used when reconstructing data for display if two timebases were used during the acquisition. The Storage RAM Data Readback circuitry multiplexes the ECL-level correlation data from the storage RAMs on the ACORO(L) and BCORO(L) signal lines. This multiplexed data is output serially to the Acquisition-Control Processor Interface for readback by the Control Processor. The ECL-level serial information is converted to TTL-level parallel information in the Acquisition-Control Processor Interface.

Testing begins by checking that two probes are connected to the acquisition board. The test assumes that the probes are connected to the Test Pattern Generator (TPG). The TPG is run by its local oscillator, operating at a frequency of 12 MHz. The acquisition memory is clocked by the T1 and T2 clocks in demux clock mode.

The acquisition card is programmed to generate a T1 clock on the rising edge of the TPG clock, T2F on the falling edge of the TPG clock, and T2L on the falling edge of the TPG clock. The correlation bit is stored by the T1 clock. After the acquisition is complete, the 512 locations of correlation data are compared to expected data. If problems are detected, the test is aborted and the failure is reported.

The next part of the test requires that the acquisition card be re-programmed to generate the T2L clock on the rising edge (instead of falling edge) of the TPG clock. The correlation bit is stored by the T2L clock. After the acquisition is complete, the 512 locations of correlation data are compared to expected data. If problems are detected, the test is aborted and the failure is reported.

8831 Error Index

Explanation: The test failed to detect both acquisition probes.

Probable Cause	Action
One or both of the probes is not connected, or a probe may be bad.	Examine the expected and actual screen data. If the expected result is 00_{hex} and the actual result is 40_{hex}, suspect the A-side probe. If the expected result is 00_{hex} and the actual result is 80_{hex}, suspect the B-side probe.
Suspect A16U457.	While looping on this test, check A16U457-9 for low-going pulses.
Suspect A16U561.	While looping on this test, check A16U561-1 for low-going pulses. If none are found, check A16U348 for correct operation. Also, check A16U561-8 and -12 for high-going pulses.

8832 Error Index

Explanation: The A-side acquisition data was incorrect; expected 55_{hex}.

Probable Cause	Action
Bad correlate signal.	While looping on this routine, check that A16U338-7 is toggling high and low. If there is no signal present, refer to the appropriate trigger schematics. If present, check A16U338-3 for toggling high and low signal.
Bad memory or data chain.	While looping on this routine, check that A16U442-14 is toggling high and low. If no signal is present, suspect U442 and U219.
Bad storage RAM readback circuitry.	While looping on this test, check that A16U253-1 is toggling high and low. If no signal is present, suspect U253 and U219.

8833 Error Index

Explanation: The B-side acquisition data was incorrect; expected 55_{hex}.

Probable Cause	Action
Bad memory or data chain.	While looping on this routine, check that A16U448-14 is toggling high and low. If no signal is present, suspect U448 and U240.
Bad storage RAM readback circuitry.	While looping on this test, check that A16U253-5 is toggling high and low. If no signal is present, suspect U253 and U240.

8834 Error Index

Explanation: The A-side acquisition data was incorrect; expected AA_{hex}.

Probable Cause	Action
Bad correlate signal.	While looping on this routine, check that A16U338-5 is toggling high and low. If there is no signal present, refer to the appropriate trigger schematics.
Bad memory.	While looping on this routine, check that A16U219-21 is toggling high and low. If no signal is present, suspect U219.

8835 Error Index

Explanation: The B-side acquisition data was incorrect; expected AA_{hex}.

Probable Cause	Action
Bad memory.	While looping on this routine, check that A16U240-21 is toggling high and low. If no signal is present, suspect U240.

module: 1240D2-X
area: CAL ACQ18

1240D2 CAL ACQ18 TEST DESCRIPTION

The 18-channel acquisition calibrate test consists of two routines. Routine 1 helps in the testing and calibration of the 18-channel's threshold circuitry. Routine 2 provides a display of calibration values found for the 18-channel's gate arrays (front end hybrids). Routine 2 test results indicate delay values calculated during the calibration of signal delays through the gate arrays. Testing performed by routine 2 is basically the same as performed by the CALIBRATE area (87XX) test, the difference being that routine 2 displays the actual delay values calculated. The gate arrays are automatically calibrated by the operating firmware prior to each acquisition.

ROUTINE 1 – TEST DESCRIPTION

This routine aids in testing the calibration of the 18-channel's threshold circuitry. This circuitry produces the variable threshold voltages for both A and B acquisition probes. The digital-to-analog convertor (DAC), A16U156, latches and translates data sent by the Control Processor as threshold voltage changes (50 mV change per bit). The total voltage range is from +6.35 volts to −6.35 volts.

NOTE

This routine requires that the operator observe test results with external equipment to determine if the threshold circuitry is properly calibrated. The procedure described in the following should only be used for verifying circuit operation. If precise calibration of the threshold circuitry is required, refer to the 1240D2 calibration procedures in the Verification and Adjustment Procedures *section of this manual.*

1240 SETUP FOR THRESHOLD CALIBRATION TEST

1. With the 1240 powered-down, access the 1240D2 acquisition board according to the instructions provided in the *Disassembly and Installation Procedures* section of this manual.
2. Set a multimeter to the 10 or 20 volt dc range and connect the high (+) lead to A16TP268, low (−) lead to A16TP257-2.
3. Power up the 1240 and enter diagnostics by simulating a keyboard failure (hold down a key during power-up).
4. Using the SELECT keys or the KNOB, choose the 1240D2-X module and touch the MODULE DIAGNOSTIC soft key. (The X designation indicates one of four possible 18-channel acquisition boards under test.)
5. Choose the CAL ACQ18 area and touch the AREA DIAGNOSTICS soft key.
6. Choose the Routine 1 test and press the START key.
7. With the threshold setting at 0.00 volts, verify that the multimeter reading is at 0.00 volts ± 24 mV.

8. Using the SELECT keys or the KNOB, choose +6.35 volts for the probe threshold voltage and verify the reading on the multimeter is +6.35 volts ± 24 mV.
9. Now, choose −6.35 volts for the probe threshold voltage and verify the reading on the multimeter is −6.35 volts ± 24 mV.

CAL ACQ18 - ROUTINE 1 TEST RESULTS

Explanation: One of the measured voltages was incorrect by more than 24 mV.

Probable Cause	Action
Defective threshold circuit.	Suspect the DAC A16U156 if the measured voltage was in error by more than 24 mV.

ROUTINE 2 – TEST DESCRIPTION

The calibrate test results indicate delay values calculated during the calibration of signal delay through 18-channel gate arrays A16U402, U407, and U412. Once calibrated, the delay through all three gate arrays is equal. The test programs the 1240 to trigger after receiving a certain number active global events. Next, the test calculates the number of reads it must do to reach the maximum Memory Address Pointer (MAP) count. With this information, the test calculates the number of times the MAP was incremented during the test (basically the trigger position). The test then verifies that the MAP count was within an allowable count range (199_{hex} maximum count to 177_{hex} minimum count). If the MAP count was higher than the allowable limit, then the test is run again with less delay time programmed into the gate arrays. If the MAP count was lower than the minimum value, the routine is run again with more delay programmed into the gate arrays. The test will continue to try different gate-array delay values until the correct delay is found. If the proper delay value can not be found, the delay programmed into the gate arrays is set to the mid point of the possible range of delay values.

NOTE

A delay time reading at the end of its range (00 or 0F) idicates a marginal gate array. Setup and hold times may be affected in extreme temperature conditions.

1240 SETUP FOR GATE ARRAY CALIBRATION TEST

Program the 1240 diagnostic menus as follows:

1. Using the SELECT keys or the KNOB, choose the 1240D2-X module and touch the MODULE DIAGNOSTIC soft key.
2. Choose the CAL ACQ18 area and touch the AREA DIAGNOSTICS soft key.
3. Choose routine 2 and press the START key.

CAL ACQ18 - ROUTINE 2 TEST RESULTS

The following three examples show typical screen displays resulting from the routine 2 tests.

CALIBRATE GATE ARRAYS

U412 = 0A 0178
U407 = 08 0181
U402 = 02 0177

PRESS STOP TO EXIT

Example 1. All gate arrays were calibrated correctly.

CALIBRATE GATE ARRAYS

U412 = 0A 0181
U407 = 08 0000
U402 = 05 0189

PRESS STOP TO EXIT

Example 2. Display shows that A16U407 could not be calibrated correctly, indicating a problem with that gate array. A default delay value of 8 is programmed into the gate array when the test can not find the correct delay value.

CALIBRATE GATE ARRAYS

U412 = 08 0000
U407 = 08 0000
U402 = 08 0000

PRESS STOP TO EXIT

Example 3. Display shows that none of the gate arrays could be calibrated correctly. A default delay value of 8 is programmed into the gate array when the test can not find the correct delay value.

9XXX ROMPACK ERROR INDEXES

Error Index	Area Name	Area Number
91XX	EPROM COMP	AREA 1
92XX	EPROM CSUM	AREA 2
93XX	EPROM PAGE	AREA 3

ROMPACK BLOCK DIAGRAM
EPROM COMP – AREA 1

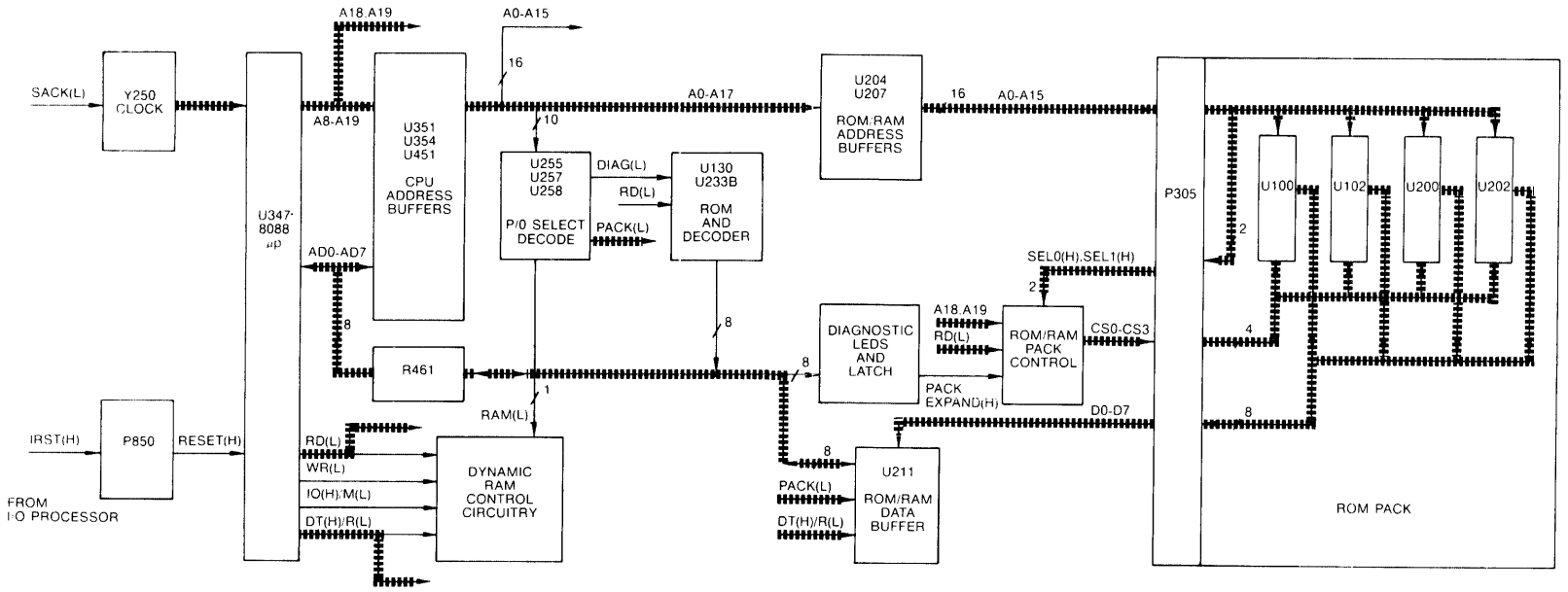


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Figure 8-131. ROM Pack EPROM COMP block diagram. Pattern shading is the same as for areas 2 and 3.

32 K ROM PACK BOARD – COMPONENT LOCATION

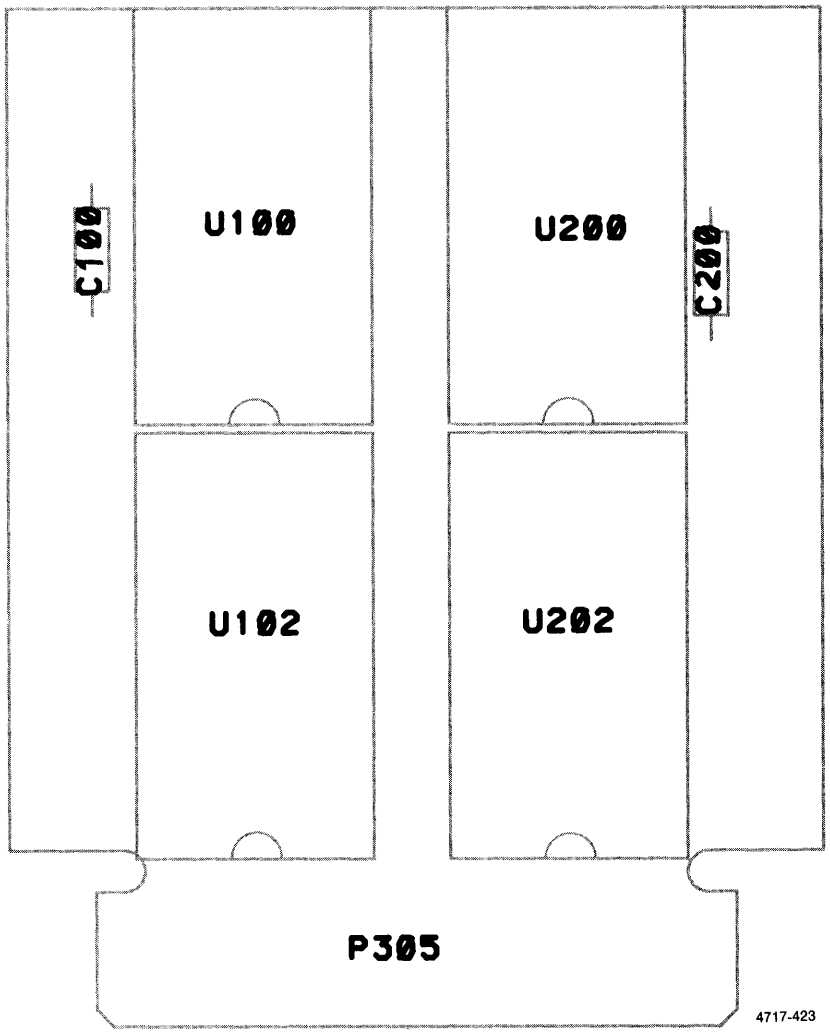

Figure 8-132. 32 K ROM Pack Board component location.

module: ROMPACK
area: EPROM COMP

EPROM COMP AREA – CIRCUIT OVERVIEW

The pattern-shaded signal lines on the ROM pack EPROM complementary byte block diagram indicate circuitry used during diagnostic testing. Only the circuitry that is being exercised for the first time during diagnostic testing is shown. Circuitry exercised by other diagnostic tests are shown in their respective block diagrams.

The 8088 microprocessor addresses the ROMs in the ROM pack with address lines A0-A15. The ROM/RAM Pack Control circuitry supplies five chip select signals, CS0(L)-CS4(L), to the ROMs. These select lines allow the Control Processor to enable the specific ROM being read. The microprocessor reads back ROM data through the ROM/RAM Data Buffer, A9U211.

EPROM COMP AREA – TEST DESCRIPTION

The ROM bytes at ROM-end-minus-three and ROM-end-minus-two are compared to determine if they are complementary. This tests the ROM's ability to drive the address and data bus both logic high and low on all bits. Each routine tests one of the four ROMs in the ROM pack. If the test detects an error, the corresponding error index is displayed on the 1240 screen and the next ROM is checked.

ROUTINE 1 DESCRIPTION

The bytes at address locations $1FFC_{hex}$ and $1FFD_{hex}$ of ROM A42U100 are compared to determine if they are complementary.

9111 Error Index

Explanation: The bytes at address locations $1FFC_{hex}$ and $1FFD_{hex}$ were found not to be complementary.

Probable Cause	Action
Bad ROM.	Suspect ROM A42U100.

9111

ROUTINE 2 DESCRIPTION

The bytes at address locations $3FFC_{hex}$ and $3FFD_{hex}$ of ROM A42U202 are compared to determine if they are complementary.

9121 Error Index

Explanation: The bytes at address locations $3FFC_{hex}$ and $3FFD_{hex}$ were found not to be complementary.

Probable Cause	Action
Bad ROM.	Suspect ROM A42U202.

ROUTINE 3 DESCRIPTION

The bytes at address locations $5FFC_{hex}$ and $5FFD_{hex}$ of ROM A43U200 are compared to determine if they are complementary.

9131 Error Index

Explanation: The bytes at address locations $5FFC_{hex}$ and $5FFD_{hex}$ were found not to be complementary.

Probable Cause	Action
Bad ROM.	Suspect ROM A42U200.

ROUTINE 4 DESCRIPTION

The bytes at address locations $7FFC_{hex}$ and $7FFD_{hex}$ of ROM A42U102 are compared to determine if they are complementary.

9141 Error Index

Explanation: The bytes at address locations $7FFC_{hex}$ and $7FFD_{hex}$ were found not to be complementary.

Probable Cause	Action
Bad ROM.	Suspect ROM A42U102.

ROMPACK BLOCK DIAGRAM
EPROM CSUM – AREA 2

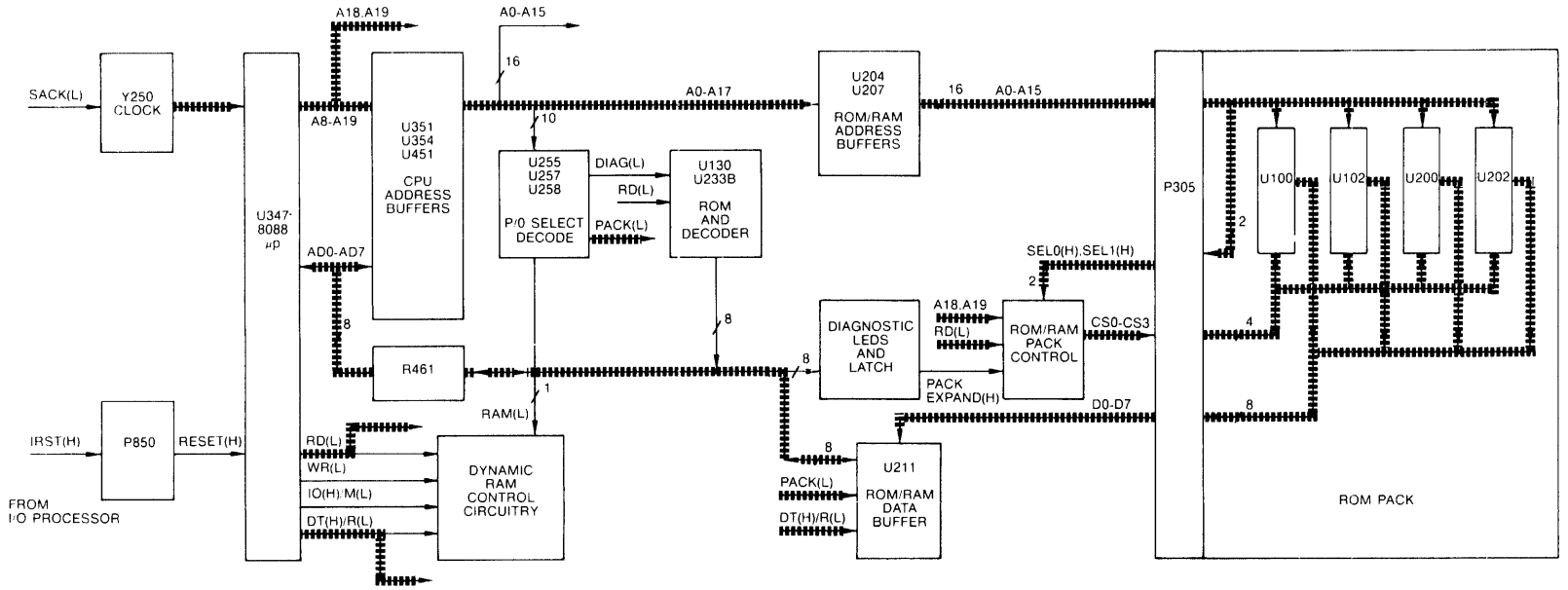

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Figure 8-133. ROM Pack EPROM CSUM block diagram. Pattern shading is the same as for areas 1 and 3.

32 K ROM PACK BOARD – COMPONENT LOCATION

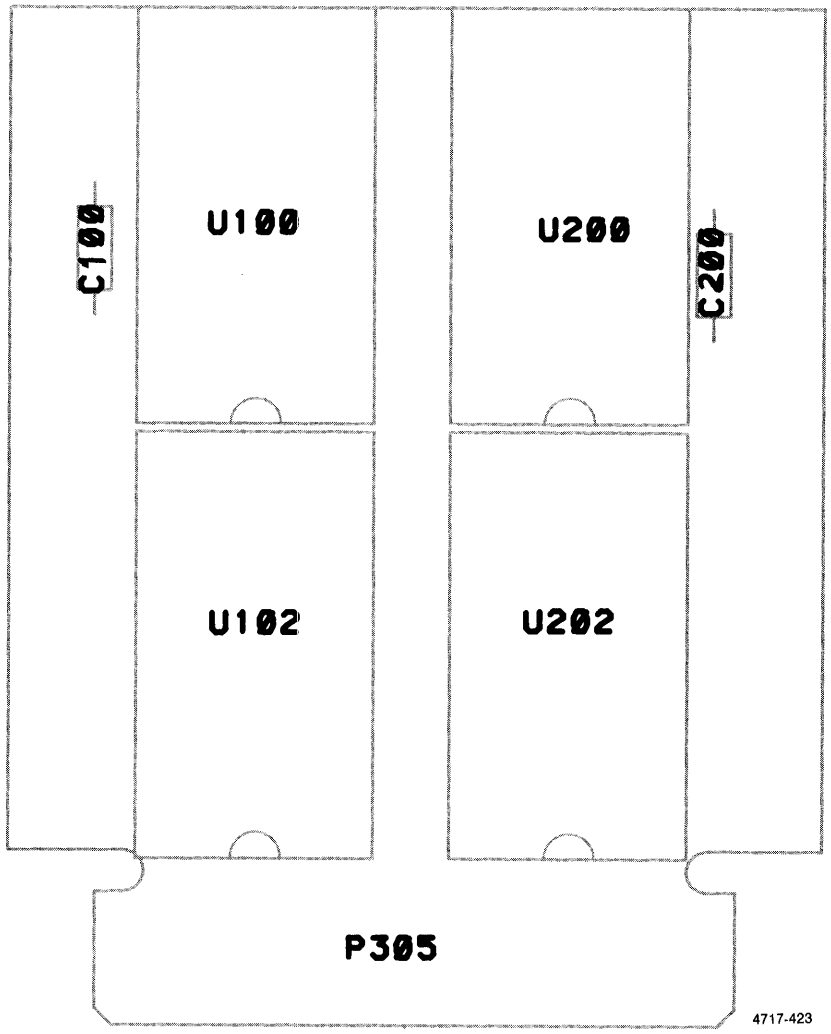

Figure 8-134. 32 K ROM Pack Board component location.

module: ROMPACK
area: CSUM

EPROM CSUM AREA – CIRCUIT OVERVIEW

The pattern-shaded signal lines on the ROM pack EPROM checksum block diagram indicate circuitry used during diagnostic testing. Only the circuitry that is being exercised for the first time during diagnostic testing is shown. Circuitry exercised by other diagnostic tests are shown in their respective block diagrams.

The 8088 microprocessor addresses the ROMs in the ROM pack with address lines A0-A15. The ROM/RAM Pack Control circuitry supplies five chip select signals, CS0(L)-CS4(L), to the ROMs. These select lines allow the Control Processor to enable the specific ROM being read. The microprocessor reads back ROM data through the ROM/RAM Data Buffer, A9U211.

EPROM CSUM AREA – TEST DESCRIPTION

The checksum for each ROM in the ROM pack is calculated. The calculated checksum is compared to an expected value that is stored in the last two locations of the ROM. The calculated and expected checksum values are then written to the 1240 display screen.

ROUTINE 1 DESCRIPTION

The test calculates the checksum for ROM A42U100.

9211 Error Index

Explanation: The calculated checksum for ROM A42U100 did not match the expected checksum.

Probable Cause	Action
Bad ROM.	Suspect ROM A42U100.

ROUTINE 2 DESCRIPTION

The test calculates the checksum for ROM A42U200.

9221 Error Index

Explanation: The calculated checksum for ROM A42U200 did not match the expected checksum.

9211
9221

Probable Cause	Action
Bad ROM.	Suspect ROM A42U200.

ROUTINE 3 DESCRIPTION

The test calculates the checksum for ROM A42U202.

9231 Error Index

Explanation: The calculated checksum for ROM A42U202 did not match the expected checksum.

Probable Cause	Action
Bad ROM.	Suspect ROM A42U202.

ROUTINE 4 DESCRIPTION

The test calculates the checksum for ROM A42U102.

9241 Error Index

Explanation: The calculated checksum for ROM A42U102 did not match the expected checksum.

Probable Cause	Action
Bad ROM.	Suspect ROM A42U102.

ROMPACK BLOCK DIAGRAM
EPROM PAGE – AREA 3

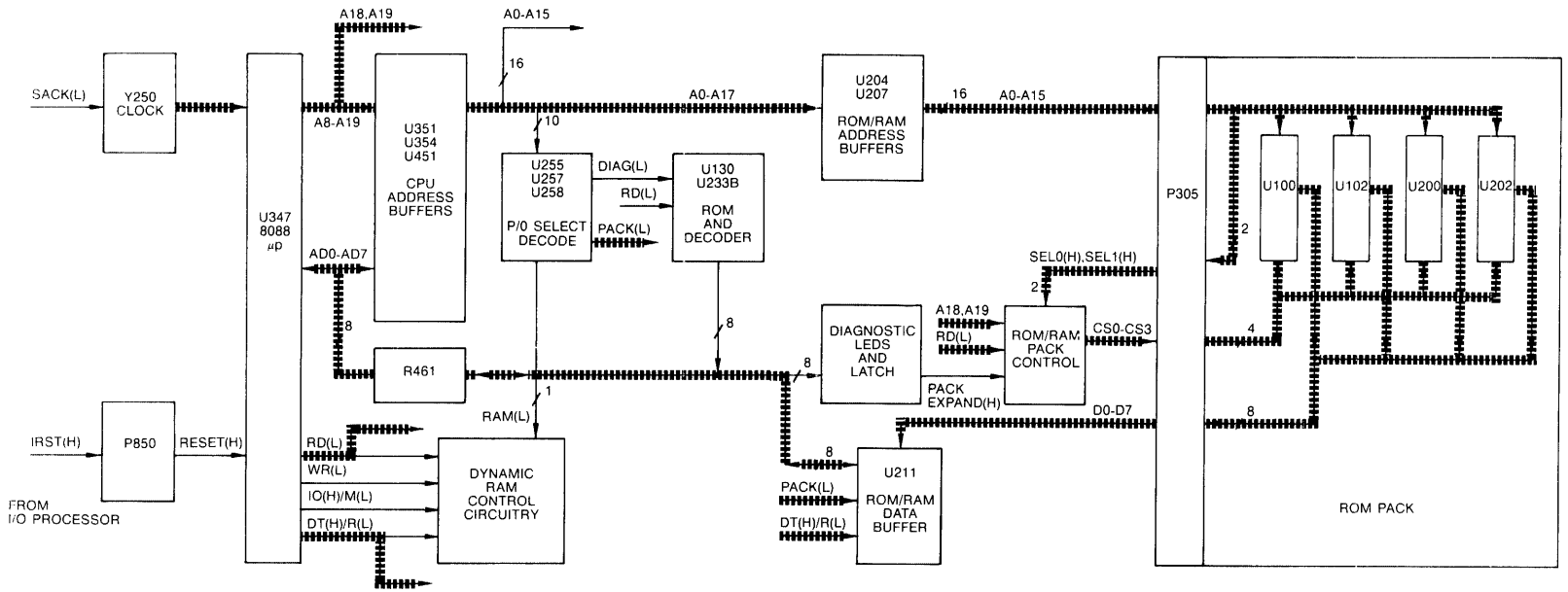

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Figure 8-135. ROM Pack EPROM PAGE block diagram. Pattern shading is the same as for areas 1 and 2.

32 K ROM PACK BOARD – COMPONENT LOCATION

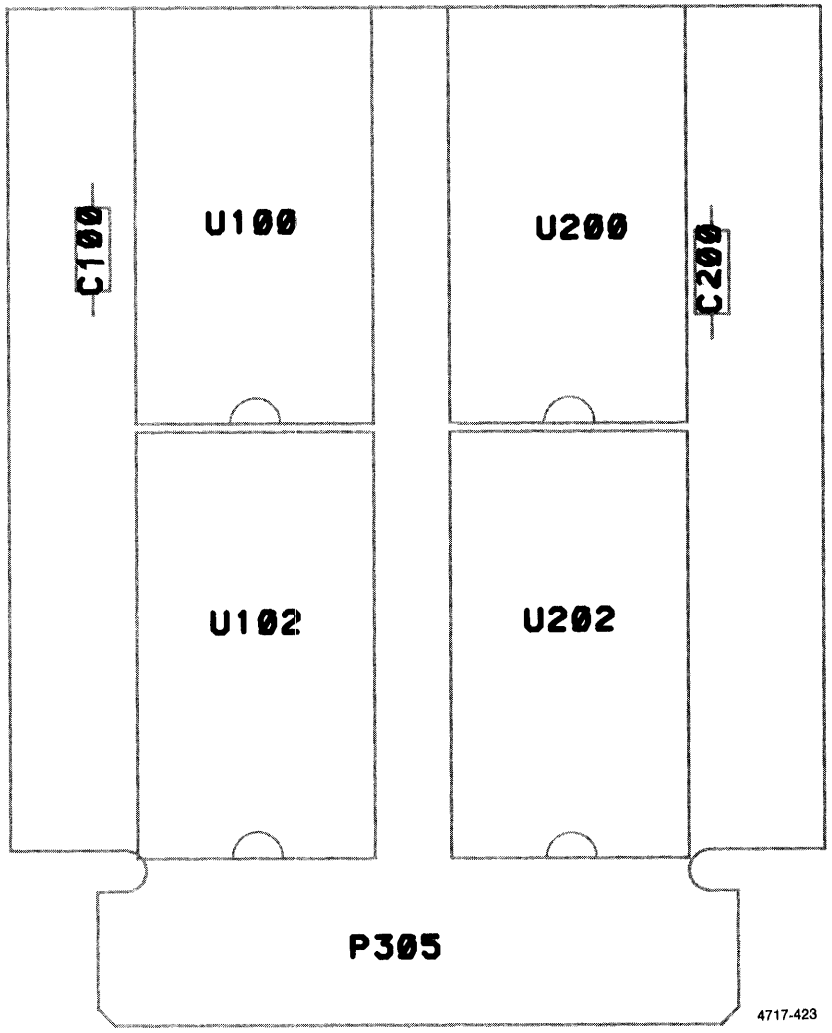


Figure 8-136. 32 K ROM Pack Board component location.

module: ROMPACK
area: EPROM PAGE

EPROM PAGE AREA – CIRCUIT OVERVIEW

The pattern-shaded signal lines on the ROM pack EPROM PAGE block diagram indicate circuitry used during diagnostic testing. Only the circuitry that is being exercised for the first time during diagnostic testing is shown. Circuitry exercised by other diagnostic tests are shown in their respective block diagrams.

The 8088 microprocessor addresses the ROMs in the ROM pack with address lines A0-A15. The ROM/RAM Pack Control circuitry supplies five chip select signals, CS0(L)-CS4(L), to the ROMs. These select lines allow the Control Processor to enable the specific ROM being read. The microprocessor reads back ROM data through the ROM/RAM Data Buffer, A9U211.

EPROM PAGE AREA – TEST DESCRIPTION

The byte at ROM-end-minus-7 is checked to determine if each ROM in the ROM pack is in the correct socket. For example, if the ROM resides at address location 10000_{hex}-$11FFF_{hex}$, then the byte at ROM-end-minus-7 should be 11_{hex}.

ROUTINE 1 DESCRIPTION

The test checks the page address value at address $11FF8_{hex}$ for ROM A42U100.

9311 Error Index

Explanation: The page address value is incorrect for this socket; expected 11_{hex}.

Probable Cause	Action
The ROM in socket A42U100 is not in the correct location.	Move ROM to the correct location.

If Actual Data Is	Correct Location Is
13_{hex}	A42U200
15_{hex}	A42U202
17_{hex}	A42U102

ROUTINE 2 DESCRIPTION

The test checks the page address value at address $13FF8_{hex}$ for ROM A42U200.

9321 Error Index

Explanation: The page address value is incorrect for this socket; expected 13_{hex}.

Probable Cause	Action
The ROM in socket A42U200 is not in the correct location.	Move ROM to the correct location.

If Actual Data Is	Correct Location Is
11_{hex}	A42U100
15_{hex}	A42U202
17_{hex}	A42U102

ROUTINE 3 DESCRIPTION

The test checks the page address value at address $15FF8_{hex}$ for ROM A42U202.

9331 Error Index

Explanation: The page address value is incorrect for this socket; expected 15_{hex}.

Probable Cause	Action
The ROM in socket A42U202 is not in the correct location.	Move ROM to the correct location.

If Actual Data Is	Correct Location Is
11_{hex}	A42U100
13_{hex}	A42U200
17_{hex}	A42U102

ROUTINE 4 DESCRIPTION

The test checks the page address value at address $17FF8_{hex}$ for ROM A42U102.

9341 Error Index

Explanation: The page address value is incorrect for this socket; expected 17_{hex}.

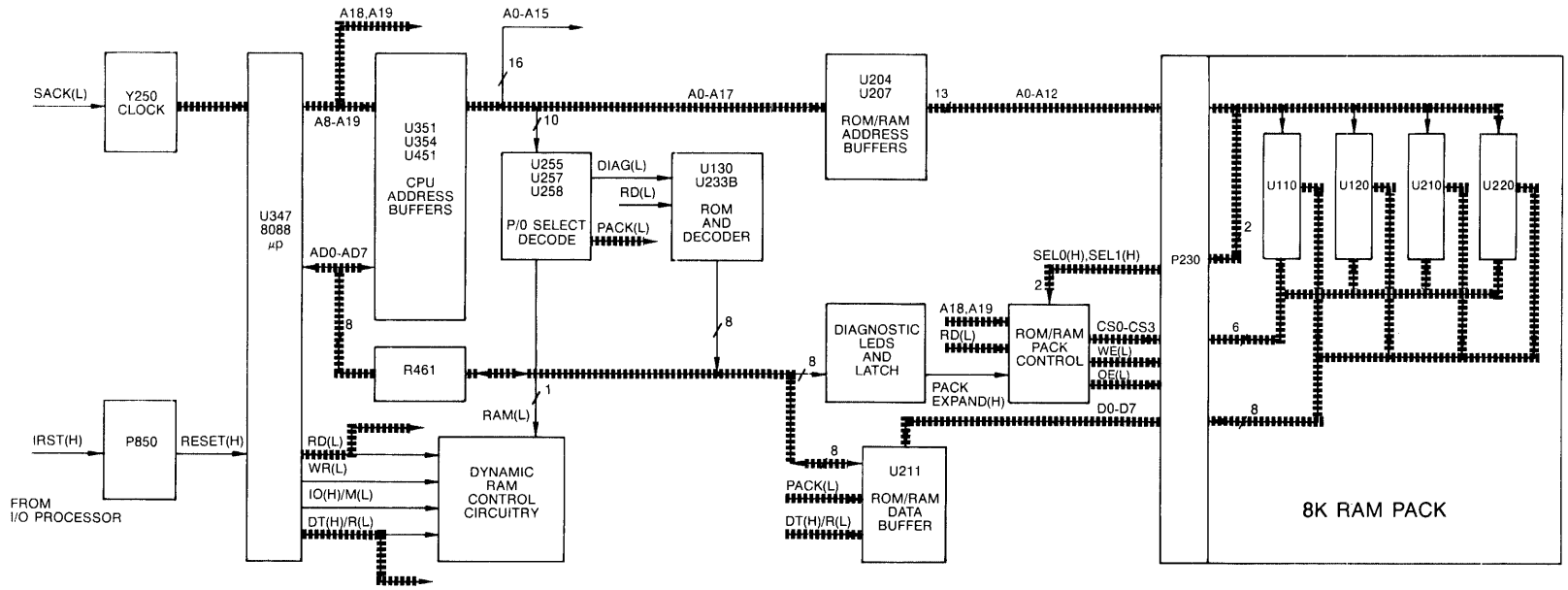
Probable Cause	Action
The ROM in socket A42U102 is not in the correct location.	Move ROM to the correct location.

If Actual Data Is	Correct Location Is
11_{hex}	A42U100
13_{hex}	A42U200
15_{hex}	A42U202

AXXX RAMPACK ERROR INDEXES
(12RS01 8K RAMPACK)

Error Index	Area Name	Area Number
A1XX	RAM	AREA 1

RAMPACK BLOCK DIAGRAM
RAM – AREA 1



4342-149

Figure 8-137. 8K RAM Pack block diagram.

8 K RAM PACK BOARD – COMPONENT LOCATION

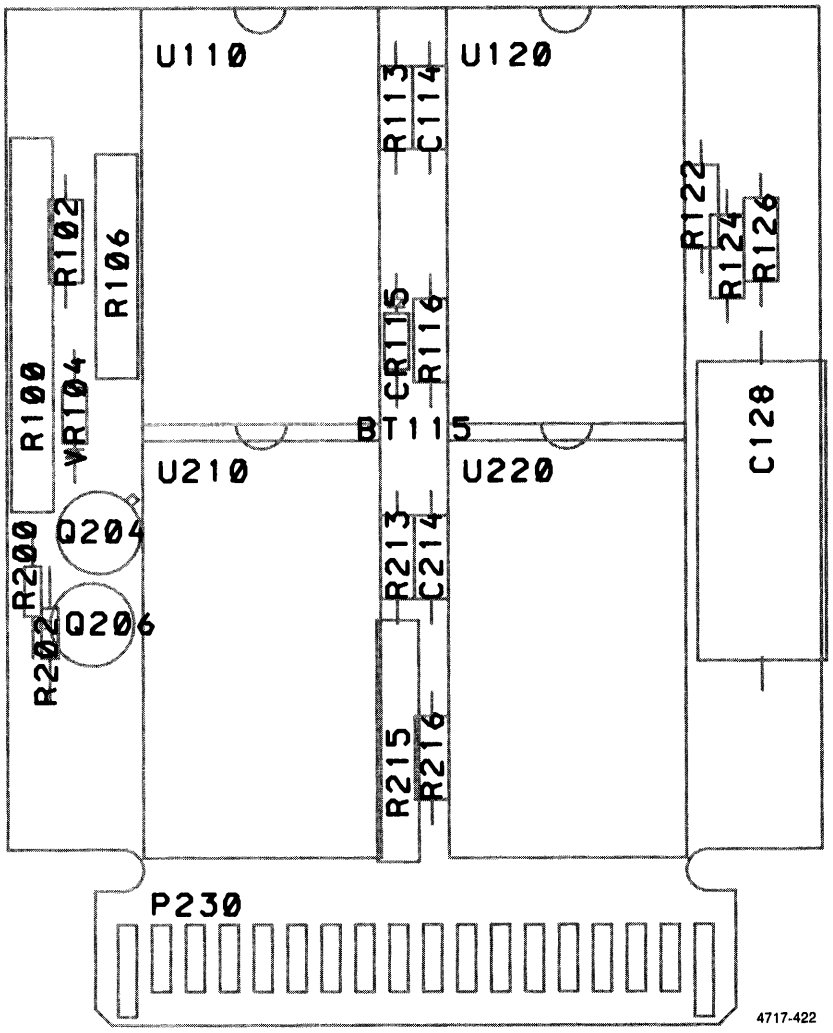


Figure 8-138. 8 K RAM Pack Board component location.

module: RAMPACK
area: RAM

RAM AREA – CIRCUIT OVERVIEW

The pattern-shaded signal lines on the RAM pack block diagram indicate circuitry used during diagnostic testing. Only the circuitry that is being exercised for the first time during diagnostic testing is shown. Circuitry exercised by other diagnostic tests are shown in their respective block diagrams.

The 8088 microprocessor addresses the RAMs in the RAM pack on address lines A0-A12. The ROM/RAM Pack Control circuitry supplies five chip select signals, CS0(L)-CS4(L), an output enable signal, OE(L), and a write enable, WE(L), to the RAMs. These select lines allow the Control Processor to enable the specific RAM being used. The microprocessor reads back RAM data through the ROM/RAM Data Buffer, A9U211.

RAM AREA – TEST DESCRIPTION

First, the checksum for the 8K RAM pack is calculated. The calculated checksum is compared to an expected value and the resulting checksum values are written to the 1240 display screen. Next, the RAM tests check to see that all address and data lines are independent of each other. The four RAMs are checked for data-bit independence by saving a byte of RAM space, testing that memory location, and then restoring the information. Now the RAMs are checked for address-line independence by storing the contents of the RAM pack in Dynamic RAM. After checking the four RAMs, the information is restored to the RAM pack.

ROUTINE 1 DESCRIPTION

This test calculates the checksum for the RAM pack.

A111 Error Index

Explanation: The calculated checksum for the RAM pack did not match the expected checksum.

Probable Cause	Action
Bad RAM or the data was changed before a new checksum was calculated.	Enter the normal operation mode and initialize the RAM pack. Now, power down the 1240 and re-enter the diagnostics by holding down a key during power-up. Check to see if the problem still exists. If problems remain, refer to the RAM pack schematic and observe the results of routines 2 and 3.

ROUTINE 2 DESCRIPTION

The RAM pack data-bit-independence test checks to see that each of the eight data bits in a RAM byte locationare independent of each other. The test begins by saving a byte of the RAM pack, then writing AA_{hex} to that location. The memory location is read and verified to contain AA_{hex}; CC_{hex} is then read and verified. The test sequence continues by writing and reading $F0_{hex}$, then $0F_{hex}$. If a failure is detected, the failed address is displayed on the 1240 screen.

At power-up, this test is performed on only one byte. During normal diagnostics, all bytes in the 8K RAM pack are tested.

A122 Error Index

Explanation: The 8K RAM pack data-bit-independence test failed. Using the following table, determine which RAM failed from the information on the 1240 screen.

Probable Cause	Action
Bad RAM.	Observe the failure address on the screen to determine which RAM has failed. Verify that the RAM is bad by observing the RAM read/write operation with a logic analyzer. The following table shows RAM pack address ranges and the RAM responsible for those addresses locations.

Addresses	RAM
0000_{hex}-$07FF_{hex}$	A41U210
0800_{hex}-$0FFF_{hex}$	A41U120
1000_{hex}-$17FF_{hex}$	A41U110
1800_{hex}-$1FFF_{hex}$	A41U220

ROUTINE 3 DESCRIPTION

The RAM pack address-line-independence test checks to see that each of the address lines in the 8K RAM pack are independent of each other. The test begins by saving the contents of the RAM pack in Dynamic RAM, then writing 00_{hex} to all memory locations. The first location is read and verified to contain 00_{hex}. If it is present and correct, then FF_{hex} is read and verified. The test sequence continues by reading the 00_{hex} value and writing the FF_{hex} value for all locations under test. If a failure is detected, the failed address is displayed on the 1240 screen.

A131 Error Index

Explanation: The Dynamic Ram on the Controll Processor Board has been tested and found to be defective.

Probable Cause	Action
Bad Dynamic RAM.	Run the Control Processor RAM test described in Section 8, *Troubleshooting and Repair.*

A133 Error Index

Explanation: Not all of the address lines in the RAM pack are independent of each other.

Probable Cause	Action
Bad RAM.	Observe the failure address on the screen to determine which RAM has failed. Verify that the RAM is bad by observing the RAM read/write operation with a logic analyzer. The following table shows RAM pack address ranges and the RAM responsible for those addresses locations.

Addresses	RAM
0000_{hex}-$07FF_{hex}$	A41U210
0800_{hex}-$0FFF_{hex}$	A41U120
1000_{hex}-$17FF_{hex}$	A41U110
1800_{hex}-$1FFF_{hex}$	A41U220

A131
A133