DR11-K interface user's guide and maintenance manual

EK-DR11K-MM-001

DR11-K interface user's guide and maintenance manual

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CHAPTER 1
INTRODUCTION

1.1 INTRODUCTION

The DR11-K is a general purpose digital input/output interface capable of the parallel transfer of up to sixteen bits of data, under program control, between a PDP-11 Unibus computer and an external device (or another DR11-K).

1.2 GENERAL DESCRIPTION

The DR11-K interface consists of three functional areas: address selection logic, interrupt control logic, and device interface logic (Figure 1-1).

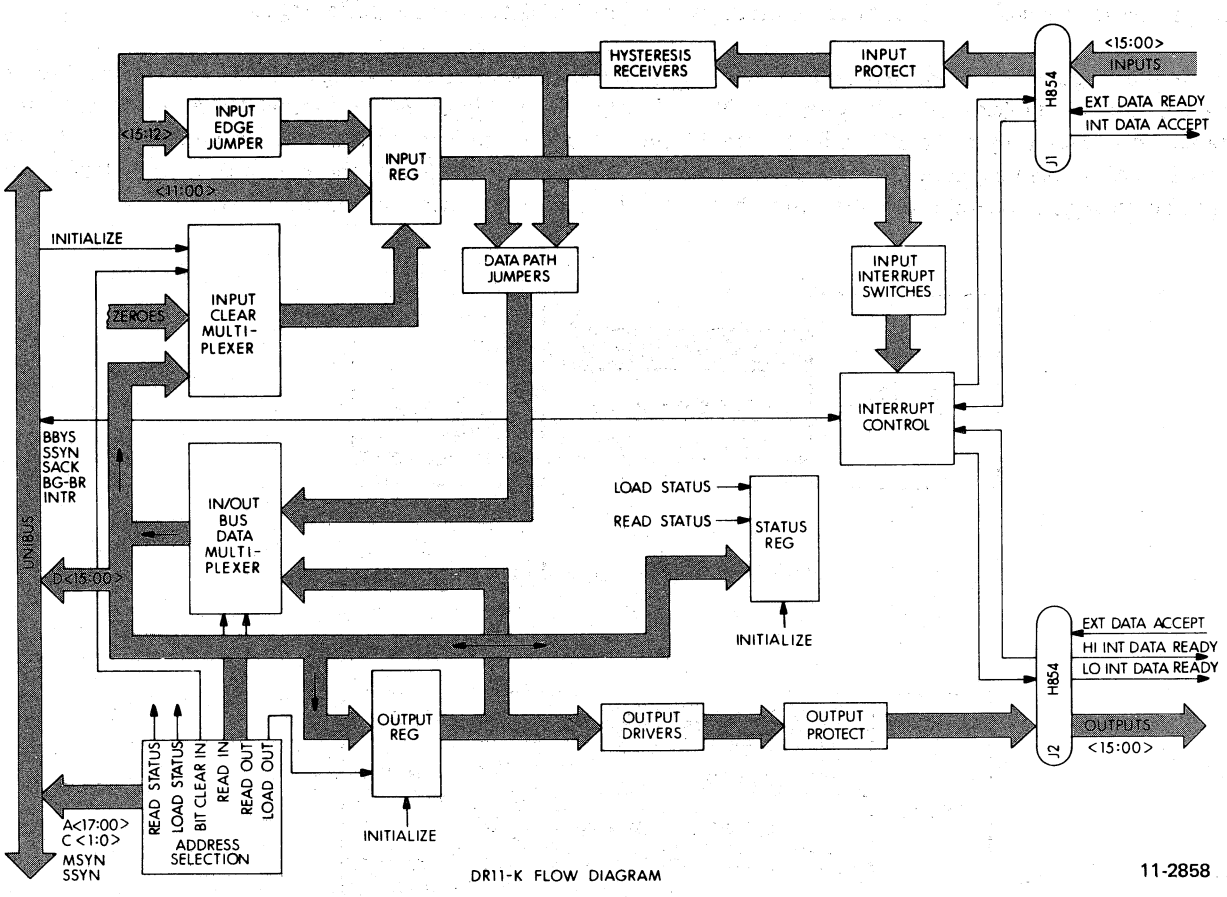

Figure 1-1 DR11-K System Block Diagram

The address selection logic determines if the interface has been selected for use, which register is to be used, whether a word or byte operation is to be performed, and what type of transfer (input or output) is to be performed.

The interrupt control logic permits the interface to gain bus control and perform program interrupts to specific vector addresses. Interrupt enable bits are under program control; interrupt bits are under control of the external device.

The DR11-K interface logic consists of three registers: status register, input register, and output register. Operation is initialized under program control by addressing the DR11-K to specify the register and the type of operation to be performed.

The status register is a 16-bit register, of which six bits are used for control and monitor functions. Two of these are flags that reflect the status of the DR11-K with respect to the external device, two are interrupt enable bits that interact with the Unibus on an interrupting condition, and two are used solely for maintenance to generate an interrupt to the Unibus.

The input register is a 16-bit buffer between an external device and the Unibus (Figure 1-2), and includes assorted option hardware selectable by solder jumpers and microswitches (described more fully in Chapter 5). Two control lines are available for full duplex control communication between the DR11-K input control logic and an external device. Each input is protected from excessive voltage and current; has hysteresis receivers for greater noise immunity; can be read either directly or from a buffer register to the Unibus; can be selected to interrupt the Unibus from its respective buffer register bit; and can be used to bit-clear data from the buffer register.

The output register is a 16-bit buffer between the Unibus and an external device (Figure 1-3). Four control lines are available for full duplex control between the DR11-K output control logic and an external device. The control lines are paired to permit byte operations. Each output is protected from excessive voltage and current (outputs gated for logical zero). A maintenance cable supplied with the DR11-K makes it possible to check internal logic by loading the input buffer register directly from the output buffer register, rather than from the external device.

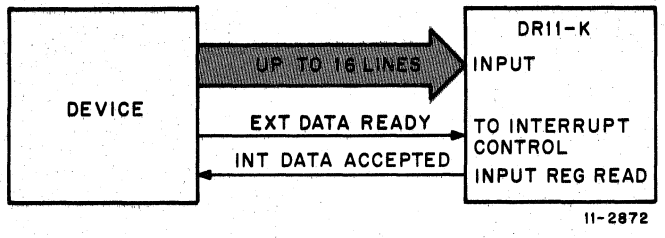

Figure 1-2 DR11-K Input Block Diagram

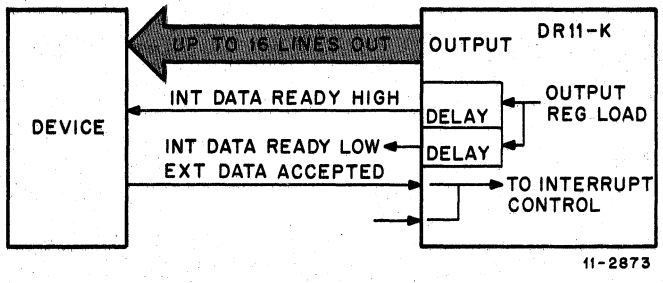

Figure 1-3 DR11-K Output Block Diagram

The DR11-K can also be used as an interprocessor buffer to allow two PDP-11 processors to transfer data between themselves. One DR11-K is connected to each processor bus, after which the two DR11-Ks are cabled together output-to-input to permit the processors to communicate. (Refer to the example in Chapter 6.)

1.3 PHYSICAL DESCRIPTION

The DR11-K is packaged on a single M7843 hex module (shown in Figure 1-4) designed for use in one of the center SPC slots of a DD11-A or DD11-B. Various user-selected options can be implemented by PC-mounted microswitches and by solder-type jumpers, both of which are marked on the module to assist in identification. These are discussed in Chapter 5 of this manual.

1.4 ELECTRICAL SPECIFICATIONS

1.4.1 Inputs

All input lines to the DR11-K are TTL-compatible. Each input has a 47-ohm fusible resistor that opens when the current exceeds 250 mA and has recoverable over-voltage protection up to +15 Vdc or −10 Vdc. A logical 1 is represented by 0 V on an input line (except for input lines 15:12, which are optionally redefined). A line must sink a minimum of 3.5 mA and maintain a voltage of less than 1.0 V at the receiver end for a logical 1. Figure 1-5 shows the basic input circuitry.

Input lines have hysteresis for both high and low thresholds, allowing the DR11-K a high degree of noise immunity. Table 1-1 shows the input voltage specifications.

1.4.2 Outputs

All output lines from the DR11-K are driven by open collector logic. Each can sink 30 mA of current to 0 V for a logical 1 output and source 5 mA of current to +4 V for a logical 0 output. Figure 1-6 shows the basic output circuitry. Each output has a fuse that opens when current exceeds 250 mA, and has overvoltage protection when in a zero state.

1.4.3 Power Requirements

The M7843 module requires +5 Vdc at 2.5 A maximum (2 A static) from the Unibus power distribution.

1.4.4 Connectors

The M7843 module contains two 40-pin H854 input/output connectors for all user input/output signals. Pin assignments for these connectors are shown in circuit schematic D-CS-M7843-0-1, sheet D8, or Figure 3-3.

1.5 SPECIFICATIONS SUMMARY

The specifications for the DR11-K interface are summarized in Table 1-2.

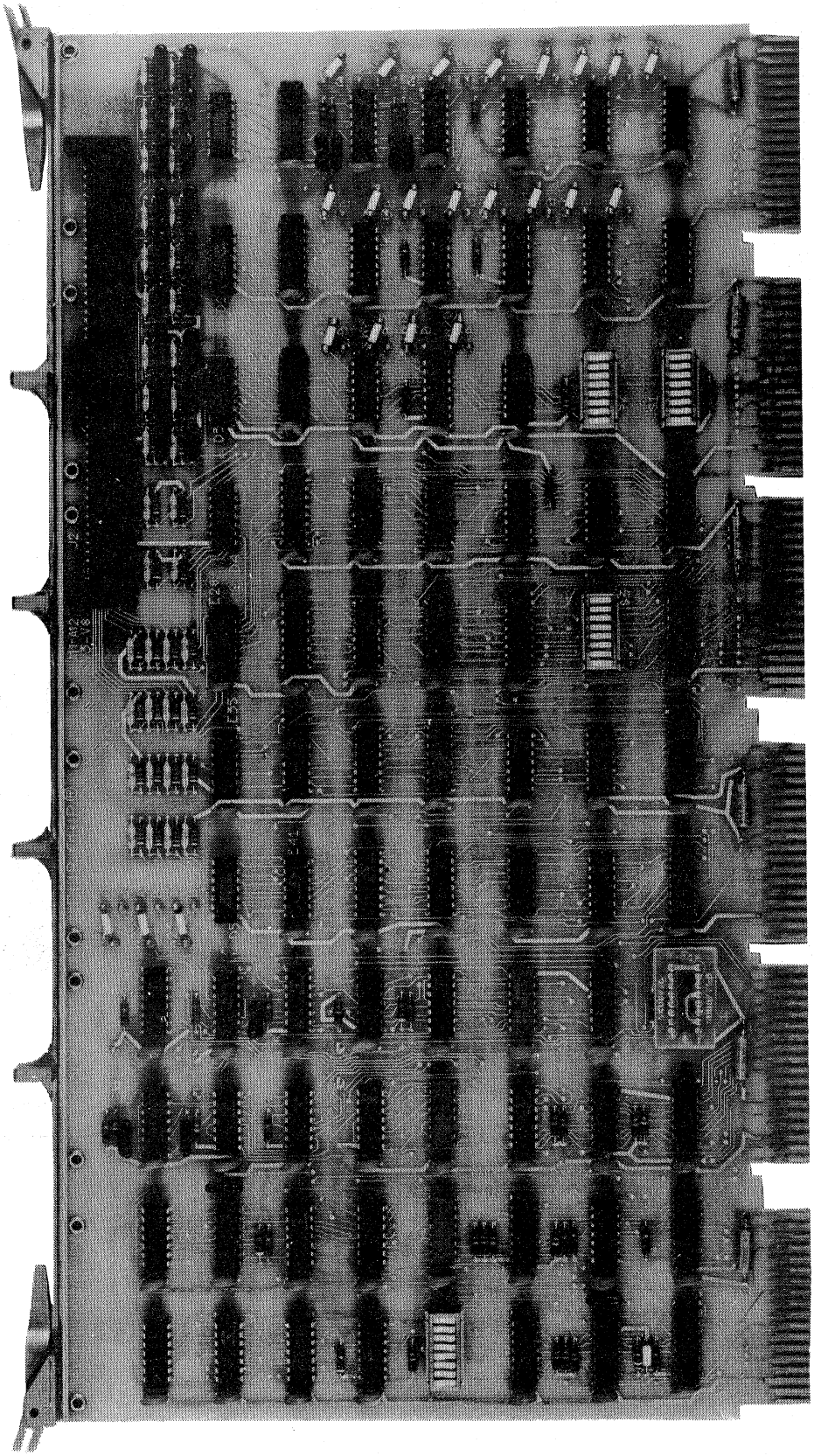

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Figure 1-4 M7843 Hex Module

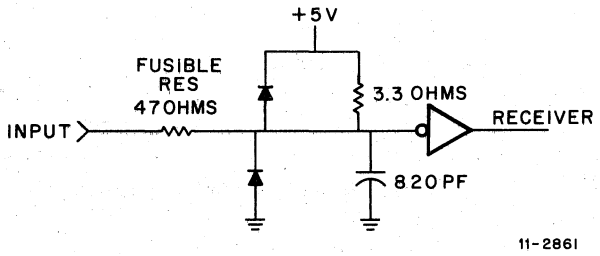


Figure 1-5 DR11-K Input Circuitry

Table 1-1
Input Hysteresis Specifications

	MIN.	MAX.	
High Threshold Input	2.0	2.4	1 0 2.0 V 2.4 V
Low Threshold Input	1.0	1.4	1 0 1.0 V 1.4 V

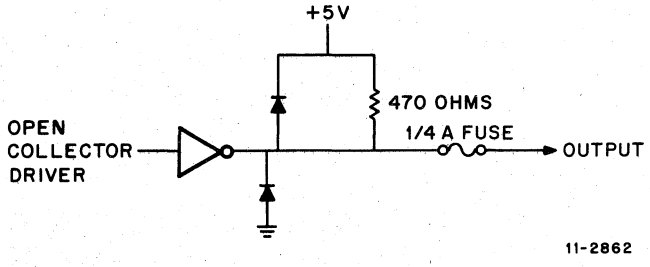


Figure 1-6 DR11-K Output Circuitry

Table 1-2
DR11-K Specifications Summary

Specification	Description
Usage	General purpose data input/output
Input/Output Levels	logic 1 = 0 V (less than 1.0 V) logic 0 = +4 V
Inputs 15:12 only	Optionally redefined
Register Addresses	
Addressing	Floating
Status Register	167 770 }
Input Register	167 772 } (Base address may be changed)
Output Register	167 774 }
Unibus Interface	
Interrupt Vector Address	Floating
Input Vector Address	300 } (Base address may be changed)
Output Vector Address	304 }
Priority Level	BR4 (May be changed)
Bus Loading	One bus load
Mechanical	
Mounting	One SPC slot
Size	Hex module
Input Current	2.5 A (2 A static) @ +5 V
Environment	
Operating Temperature	+5° C (41° F) to 43° C (110° F)
Relative Humidity	20% to 80%, noncondensing
Miscellaneous	
Inputs	TTL-compatible Overvoltage protection from -10 Vdc to +15 Vdc by 47-ohm fusible resistors that open when current exceeds 250 mA. Hysteresis for both high and low thresholds
Outputs	All driven by open collector logic. Overvoltage-protected and current-protected by fuses that open when current exceeds 250 mA when in a zero state.
Data Inputs	16-bit word from user's device
Data Outputs	16-bit word from Unibus, either as full word or 8-bit byte (either high or low)
Maintenance Mode	A maintenance cable supplied with the DR11-K jumpers the output to the input register for testing.

CHAPTER 2
SOFTWARE INTERFACE

2.1 SCOPE

This chapter presents a detailed description of the DR11-K registers (Figure 2-1). These registers are assigned bus addresses, and can be read or loaded using any instruction that refers to their addresses. The mnemonic INIT refers to the initialization signal issued by the processor. Initialization is caused by any of the following:

a. Issuance of a programmed RESET instruction.
b. Pressing of the START switch on the processor console.
c. Occurrence of a power-up or power-down condition of a system power supply.

The addresses associated with individual registers can be changed by altering the microswitches in the address selection logic. However, any programs or other software referring to those addresses must be modified to reflect the alterations. Paragraphs 2.2 through 2.4 describe the operation of the individual registers.

Unused register bits are always read as logical 0s; loading unused or read-only bits has no effect on the bit position.

2.2 INPUT REGISTER

The input register is a 16-bit register that receives data from an external device for transmission to the Unibus. The external device places the data onto the DR11-K data input lines, where it is read by a DATI sequence either directly off the input lines or from the buffer register, depending on the option selected. There are two methods of interrupting; either by the control lines or by the buffer register bits through their respective interrupt switches. If

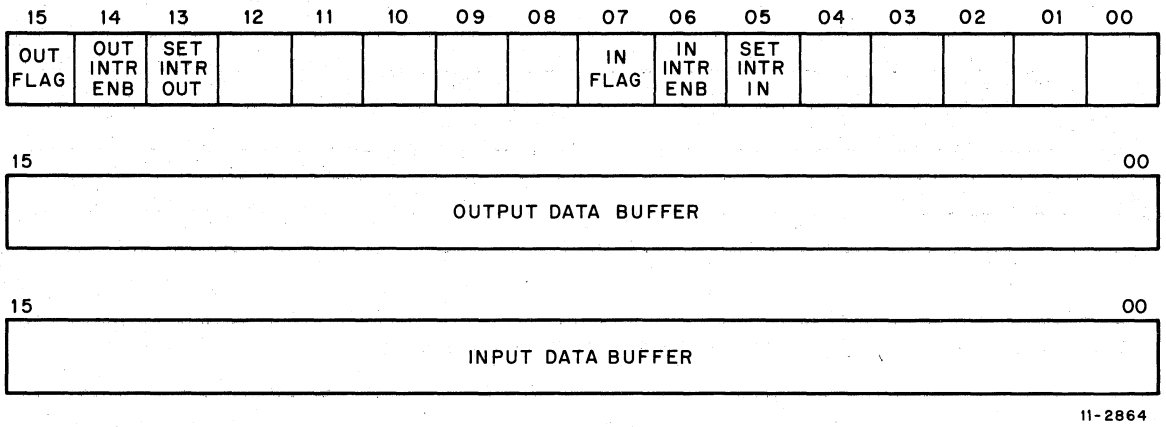


Figure 2-1 DR11-K Register Assignments

the control lines are used, the interrupt to the Unibus for a DATI sequence is produced by the EXTERNAL DATA READY line. When the data is read, the DR11-K notifies the external device on the INTERNAL DATA ACCEPTED line. If the buffer register bits are used for interrupting, the interrupt to the Unibus for a DATI sequence is produced by presenting the correct transition on the input line that corresponds to the bit selected to interrupt. The input buffer register is bit-cleared by performing a write to the register with the bits to be cleared. In order to interrupt the Unibus, the Input Enable bit of the status register must be set; the bit is cleared when the Unibus accepts the interrupt. Any unused input line will read as a logical 0.

When the maintenance cable is used, the input register receives data from the output register rather than from the external device. This permits checking of the interface logic by loading a word from the bus into the output register and verifying that the same word appears in the input register.

Examples of the way in which the input register is used in specific applications appear in Chapter 6 of this manual.

2.3 OUTPUT REGISTER

The output buffer is a 16-bit read/write register that may be read or loaded from the Unibus. Data can be loaded into this register under program control in either byte or word format. After the data is loaded, a pulsed signal (INTERNAL HIGH DATA READY or INTERNAL LOW DATA READY) permits the external transfer of data to either or both of two 8-bit devices. The output of the buffer is fed directly to the bus data lines. If 16-bit transfer is desired, either line can be used. When the external device has accepted the data, it sends back a pulsed signal (EXTERNAL DATA ACCEPTED), which causes an interrupt to the Unibus if the Output Interrupt Enable bit (status register bit 14) is set. When the interrupt is accepted by the Unibus, the bit is cleared. The contents of the output register may be read at any time by means of a DATI.

When the maintenance cable is used, the data from the output register is applied to the input buffer register, making it possible to check the operation of the interface logic.

2.4 STATUS REGISTER

The status register is used to enable interrupt logic, cause maintenance interrupts, and provide defined status functions from the external device. Input and Output flags react to signals from the external device, two Enable bits permit interrupts to occur when external signals are received, and two maintenance bits activate the interrupt logic. Figure 2-2 shows bit assignments and the status register data flow. Table 2-1 provides a brief description of each bit in the status register.

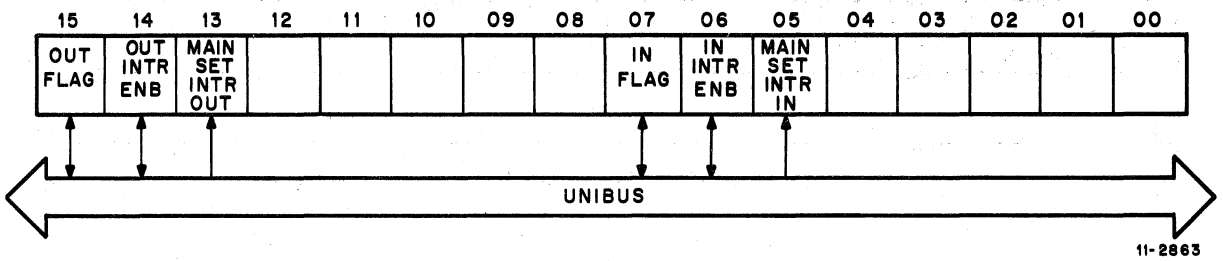


Figure 2-2 Status Register Data Flow (↑write/↓read)

Table 2-1
Status Register Bit Assignments

Bit	Title	Description
15	Output Flag	This bit sets when an EXTERNAL DATA ACCEPTED has been received from an external device.
14	Output Interrupt Enable	This bit enables an interrupt to occur when an EXTERNAL DATA ACCEPTED has been received. It is cleared when the interrupt is accepted by the Unibus.
13	Set Interrupt Out	This bit is used for maintenance only. When the DR11-K receives this bit, an output interrupt to the Unibus is generated.
07	Input Flag	This bit sets when an EXTERNAL DATA READY has been received from an external device.
06	Input Interrupt Enable	This bit enables an interrupt to occur when an EXTERNAL DATA READY has been received. It is cleared when the interrupt is accepted by the Unibus.
05	Set Interrupt In	This bit is used for maintenance only. When the DR11-K receives this bit, an input interrupt to the Unibus is generated.

2.5 REGISTER AND VECTOR ADDRESS ASSIGNMENTS

Register and vector addresses are configured prior to shipment to standard configurations, but may be changed by means of switches on the M7843 module. Chapter 5 describes the procedures in detail. Register address lines are switched on for a logical 0; vector address lines are switched on for a logical 1.

The DR11-K has floating addresses to allow the use of more than one DR11-K in a system, or to avoid any device address conflict with other options. The register address is selected by switches on the M7843 module representing address lines A12:A03. The standard register addresses selected for the DR11-K are:

167770	Status Register Address
167772	Input Address
167774	Output Address

The vector address is selected by switches on the M7843 module representing vector lines (Unibus "D" lines) D08:D03. The standard vector addresses selected for the DR11-K are:

300	Input Vector Address
304	Output Vector Address

Floating register and vector addresses are listed in Table 2-2.

Table 2-2
DR11-K Address Assignments

No. of DR11-Ks	Register Addresses	Vector Addresses
DR11-K No. 0	167774 – 167770	300, 304
DR11-K No. 1	167764 – 167760	310, 314
DR11-K No. 2	167754 – 167750	320, 324
.	.	.
.	.	.
DR11-K No. 7	167704 – 167700	370, 374
.	.	.
.	.	.
DR11-K No. 15	167604 – 167600	470, 474

The addresses in the table assume that the system contains only DR11-Ks, and no DR11-As. Addresses must be assigned for any DR11-A interfaces present in the system before DR11-K addresses are assigned. The floating vectors of the DR11-K are assigned in the following sequence:

a. Starting at 300 and proceeding upward, all DC11s.
b. Any extra KL11s called for (VT05, VT06, LC11).
c. Any DP11s.
d. Any DM11s.
e. Any DN11s.
f. Any DM11-BBs.
g. Any DR11-As.
h. Any DR11-Ks.

NOTE
Some devices use only one vector address.

The M7843 is normally shipped with a priority level configuration of BR4; this level may be changed by replacing the jumper module for another level.

2.6 INPUT PROGRAMMING

2.6.1 Input Interrupting by Control Lines

Input interrupts can be generated by the control lines, starting when the external device sends an EXTERNAL DATA READY signal to the DR11-K. That signal generates an interrupt to the Unibus if the Input Interrupt Enable is set, and sets the Input Flag of the status register. When the Unibus accepts the interrupt, the Input Interrupt

Enable bit is cleared. The program is vectored to a subroutine, where the data is read. If the input register is used for data inputting, it must be cleared before new data is sent by the external device. The program for input interrupting by control lines is as follows:

```
            MOV #00100, Status      /Set up IN INTR ENAB.
WAIT        WAIT                    /WAIT for EXT DATA READY to generate interrupt.
IN VECTOR   BR INPUT                /JMP to input subroutine.
INPUT       MOV #00100, Status      /Set up IN INTR ENAB & CLR IN FLAG.
            MOV INPUT, Memory       /Read and store the input data. This will generate an
                                    /INTERNAL DATA ACCEPT.
```

2.6.2 Input Interrupting by Buffered Input Register Bit

When the input register bits are set up to interrupt, an external device can generate interrupts by setting any of these bits. If the Input Interrupt Enable is set, an interrupt is generated to the Unibus. When the Unibus accepts the interrupt, the Input Interrupt Enable bit is cleared. The program is vectored to a subroutine, where the input data register is read. Individual register bits can be cleared by performing a Write to the input register. The program for input interrupting by register bits is as follows:

```
            MOV #177777 Input       /Clear input register.
            MOV #000100, Status     /Set up IN INTR ENAB.
WAIT,       WAIT                    /WAIT for a bit to generate an interrupt.
IN VECTOR,  BR INPUT                /Branch to input subroutine.
INPUT       MOV Input, Memory       /Read and store input register.
            MOV Memory, Input       /Clear bits that INTR.
            MOV #000100, Status     /Set up IN INTR ENAB.
            HLT or BR WAIT          /Halt or go back to WAIT for other interrupt.
```

2.7 OUTPUT PROGRAMMING

When data is loaded into the output register, a byte-oriented control signal (INTERNAL DATA READY) is sent to the external device requesting it to read the output lines of the DR11-K. The external device does so and sends a control signal (EXTERNAL DATA ACCEPTED) to the DR11-K which generates an interrupt to the Unibus, if the Output Interrupt Enable is set, and sets the Output Flag of the status register. When the Unibus accepts the interrupt, the Output Interrupt Enable bit is cleared. The program is vectored to a subroutine, where new data can be loaded into the output register.

The program for transferring data to an external device is as follows:

```
OUTPUT      MOV #040000 STATUS REG  /Set up OUT INTR ENAB.
            MOV #177777 OUTPUT REG  /Loads data into output register.
            WAIT                    /WAIT for EXT DATA ACCEPT to generate interrupt.
OUT VECTOR  HLT                     /EXT device read data.
```

CHAPTER 3
USER INPUT/OUTPUT SIGNALS

3.1 SIGNAL LIST

Tables 3-1 and 3-2 list the signals that permit the DR11-K to interact with an external device. Table 3-3 references those signals to the two H854 connectors located on the M7843 module.

Table 3-1
User Input Signals

Signal	Description
IN15 through IN00	These 16 lines are used to transfer data from an external device into the DR11-K.
EXTERNAL DATA READY	This control line is used to indicate that data from an external device is ready for transfer to the DR11-K.
INTERNAL DATA ACCEPTED	This control line is used to indicate to an external device that the data has been read off the input lines by the DR11-K, and that new data can be sent.

Table 3-2
User Output Signals

Signal	Description
OUT15 through OUT00	These 16 lines are used to transfer data from the DR11-K to an external device.
EXTERNAL DATA ACCEPTED (2 lines)	These two control lines are used to indicate to the DR11-K that data has been read off the output lines by the external device and that new data can be sent.
INTERNAL LOW DATA READY	This control line is used to indicate that data in DR11-K output register bits 07–00 is ready for transfer. This line is activated when a LOAD LOW BYTE or LOAD OUTPUT REGISTER occurs.
INTERNAL HIGH DATA READY	This control line is used to indicate that data in DR11-K output register bits 15:08 is ready for transfer. This line is activated when a LOAD HIGH BYTE or LOAD OUTPUT REGISTER occurs.
INITIALIZE	This line is used to indicate to the external device that the PDP-11 has been turned ON/OFF or the system has been initialized by the software.

3.2 CABLING

The signal distribution of the DR11-K interface is designed to minimize cross-talk. Alternate grounds are used to separate signal lines when a BC08-R flat cable is used. Up to fifty feet of BC08-R cable can be used between the DR11-K and the external device.

If longer cabling is necessary, a distribution panel, such as an H322 is recommended to distribute the lines of two BC08-R cables to 80-screw terminals, making it possible to distribute both input and output lines from this panel. Figure 3-1 shows the M7843 module plugged into a system unit and connected to an H322 distribution panel. Twisted-pair-with-shield-type cable (such as BELDON No. 8777, 8755, 8725, or equivalent) is recommended to carry the DR11-K signals from the H322 panel to an external device up to 300 feet away, as shown in Figure 3-2.

Table 3-3
Input and Output Signals

Inputs			Outputs		
Signal	**Connector**	**Pin**	**Signal**	**Connector**	**Pin**
IN00	J1	LL	OUT00	J2	K
IN01	J1	JJ	OUT01	J2	M
IN02	J1	FF	OUT02	J2	P
IN03	J1	DD	OUT03	J2	S
IN04	J1	BB	OUT04	J2	U
IN05	J1	Z	OUT05	J2	W
IN06	J1	X	OUT06	J2	Y
IN07	J1	V	OUT07	J2	AA
IN08	J1	T	OUT08	J2	CC
IN09	J1	R	OUT09	J2	EE
IN10	J1	N	OUT10	J2	HH
IN11	J1	L	OUT11	J2	KK
IN12	J1	J	OUT12	J2	MM
IN13	J1	F	OUT13	J2	PP
IN14	J1	D	OUT14	J2	SS
IN15	J1	B	OUT15	J2	UU
EXT DATA RDY	J1	NN,RR	INT HI DATA RDY	J2	E
EXT DATA ACC	J2	C	INT LO DATA RDY	J2	H
			INT DATA ACC	J1	TT
			INIT	J1	VV
			INIT	J2	A

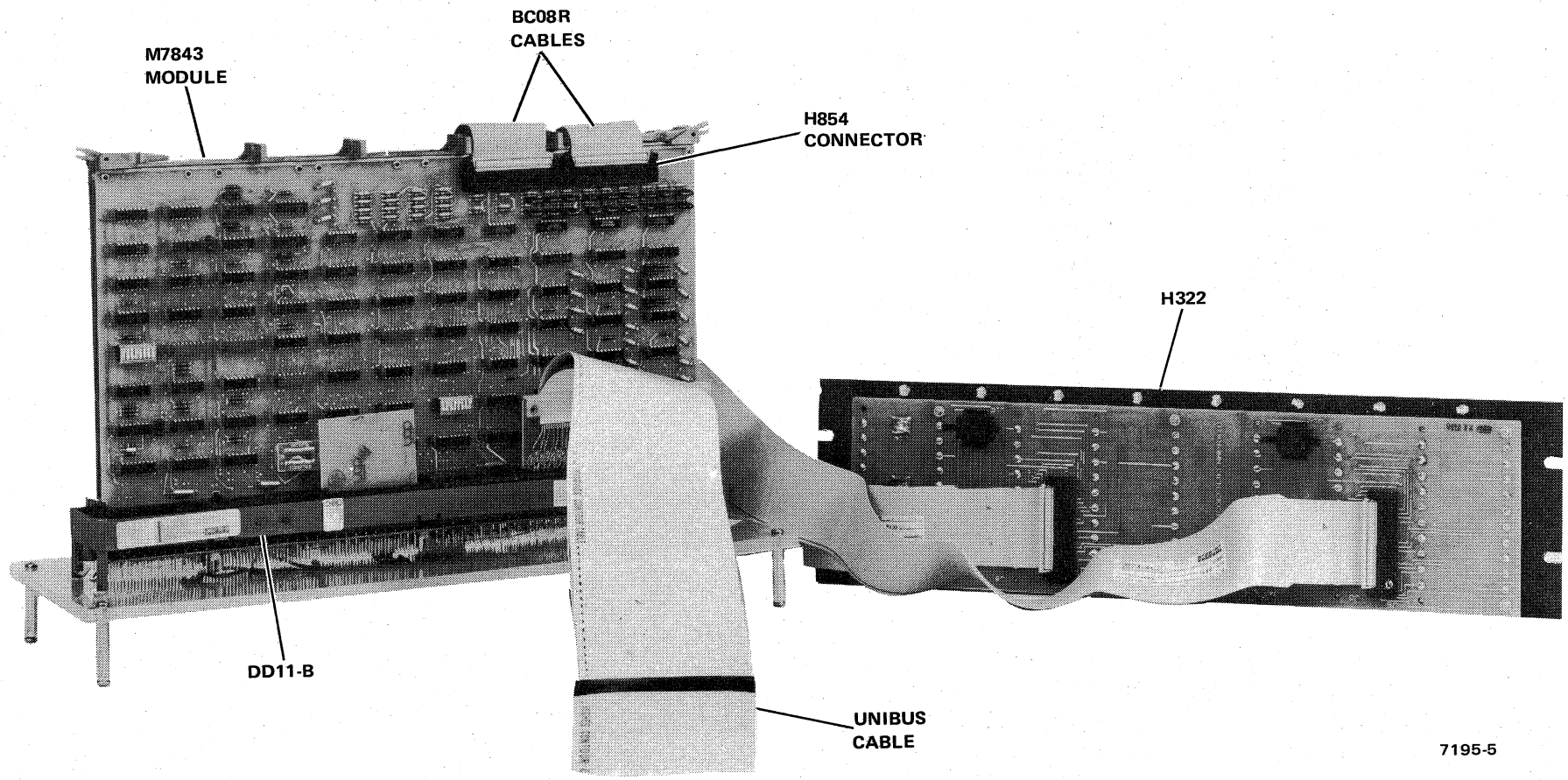


Figure 3-1 DR11-K Used With H322 Panel

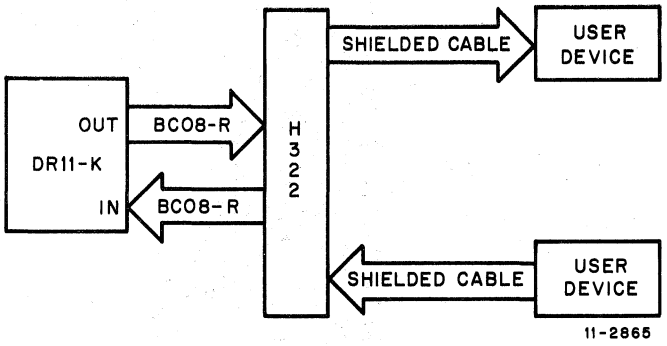


Figure 3-2 DR11-K Long Cable Arrangement

CHAPTER 4
THEORY OF OPERATION

4.1 INTRODUCTION

This chapter provides a detailed description of the DR11-K interface. The DR11-K may be divided into five major functional areas: address selection logic, interrupt logic, status register, input register, and output register. Figure 4-1 shows the interaction of these areas. The basic purpose of each area is as follows:

Address Selection Logic	Determines if the DR11-K interface has been selected for use, which register is to be used, whether a word or byte operation is required, and what type of transfer (DATI or DATO) is to be performed.
Interrupt Logic	Permits the DR11-K to gain bus control and perform a program interrupt.
Status Register	A 16-bit register that provides status of the DR11-K with respect to the external device; includes interrupt enable and generates maintenance interrupt.
Input Register	A 16-bit register that receives data from the external device for transmission to the Unibus.
Output Register	A 16-bit read/write register that can be loaded or read from the Unibus. Once the register is loaded, the data is available for transfer to the external device.

4.2 REGISTER ADDRESS SELECTION

The address selection logic (circuit schematic D-CS-M7843-0-1, sheet D3) decodes the incoming address information from the bus and provides the select lines and gating signals that determine which register has been selected and whether an input or output function is required. Switches on the logic are arranged so that the module normally responds only to device register addresses 167770, 167772, and 167774. These addresses have been selected arbitrarily by Digital Equipment as standard assignments for the DR11-K interface. The user may change the switches to any address desired; however, any MAINDEC or other software program that references the DR11-K standard address assignments must be modified correspondingly if other than standard assignments are used. Chapter 5 discusses the techniques for modification of the address assignment bits.

The first five octal digits of the address (16777–) indicate that the DR11-K has been selected as the device to be used. The final octal digit, consisting of address lines A02, A01, and A00, determines which register has been selected and whether a word or byte operation is to be performed. The two mode control lines, C1 and C0, determine whether the data in the selected register is to be the subject of a BUS DATA IN or a BUS DATA OUT function off the Unibus.

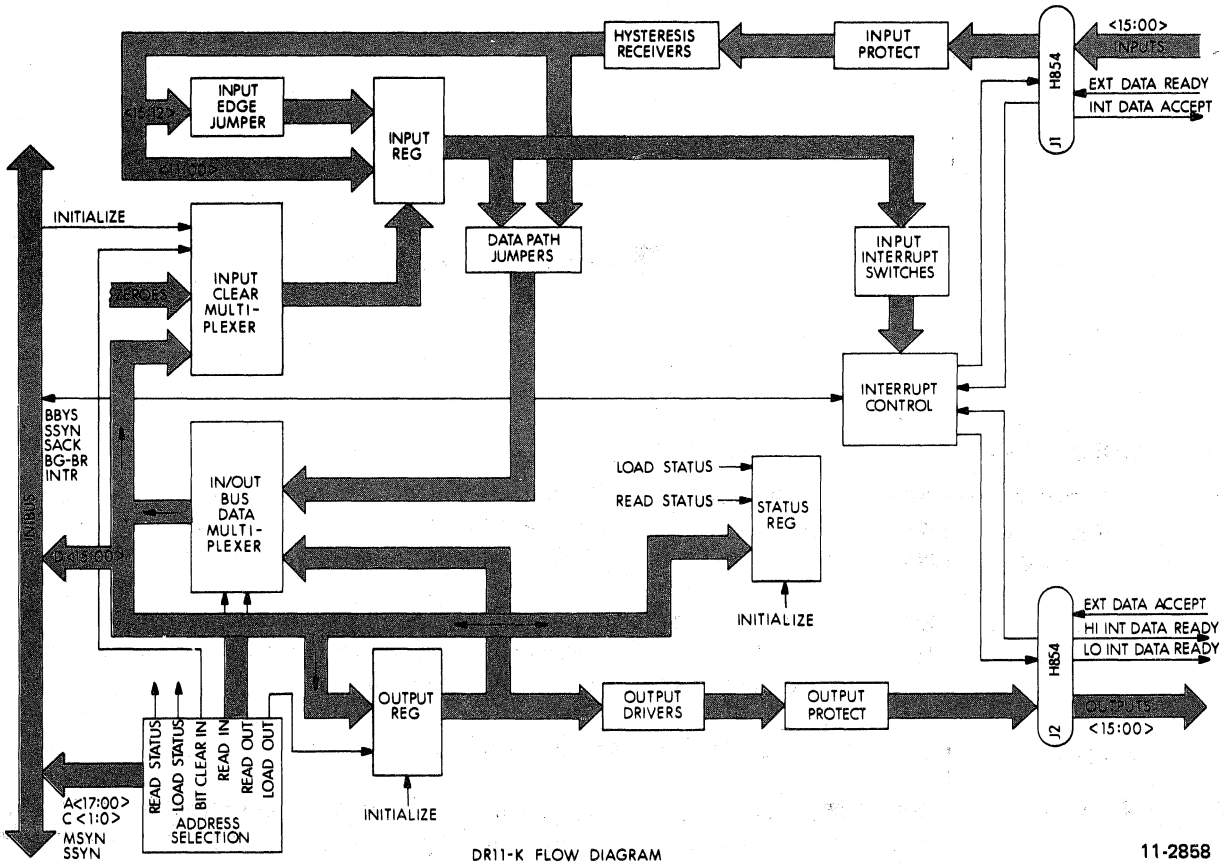


Figure 4-1 DR11-K Interface Block Diagram

Address lines A02 and A01 are decoded to produce select line signals that select the register to be used. The two mode control lines produce BUS DATA IN and BUS DATA OUT signals that determine whether the bus cycle is a DATI or DATO. A BUS DATA IN signal is provided for all three registers because all three can be read from the bus; a BUS DATA OUT signal is provided for all three registers because all three can write from the bus.

There are two BUS DATA OUT signals, OUT LO and OUT HI, that refer to the low and high bytes of a register, respectively. The basic functions of the BUS DATA IN and BUS DATA OUT signals are:

IN	The DR11-K responds by placing data from the selected register onto the Unibus data lines.
OUT LO	The DR11-K loads the low byte of the selected register from the Unibus data lines.
OUT HI	The DR11-K loads the high byte of the selected register from the Unibus data lines.

Note that both BUS DATA OUT LO and BUS DATA OUT HI are active when a full 16-bit word is being loaded into a register.

A simplified block diagram of the address selection logic appears in Figure 4-2. Note that BUS DATA IN and BUS DATA OUT are always used with reference to the master (controlling) device. Thus, BUS DATA OUT transfers represent transfers of data out of the Unibus and into the DR11-K; similarly, BUS DATA IN transfers represent data transfers from the DR11-K to the Unibus.

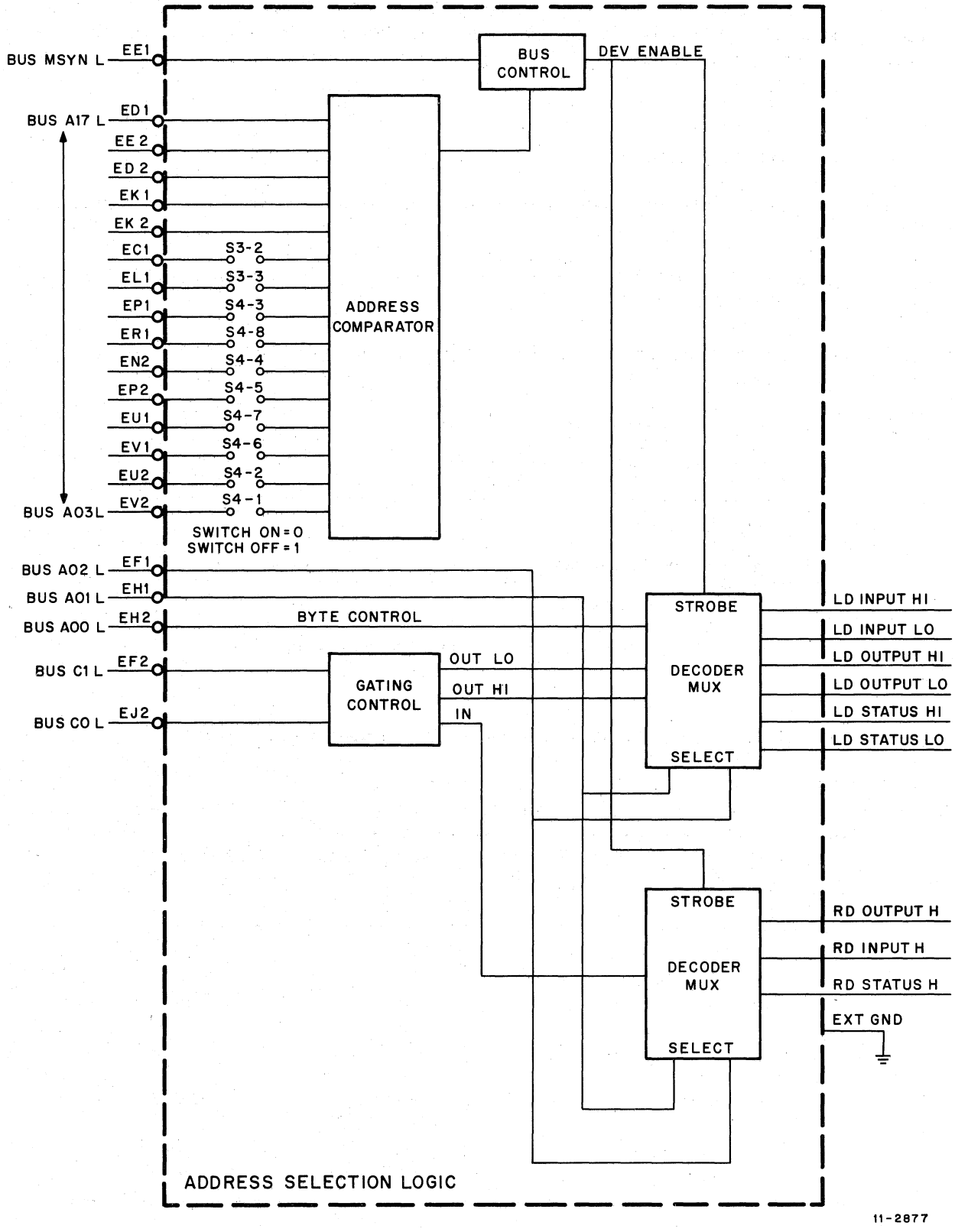


Figure 4-2 Address Selection Logic, Simplified Diagram

Input signals of the address selection logic consist of 18 address lines (A17:A00), two bus control lines (C1, C0), and a master synchronization (MSYN) line. The address selection logic decodes the incoming address as described below, according to the format shown in Figure 4-3. (All input gates are standard bus receivers.)

In Figure 4-3:

a. Line A00 is used for byte control.

b. Lines A01 and A02 are decoded to select one of the four addressable device registers (only three are used).

c. Decoding of lines A12:A03 is determined by switches. To the address logic, a switch OFF = 1, and a switch ON = 0.

d. Address lines A17:A13 must be all 1s, specifying an address within the top 8K byte address bounds for device registers.

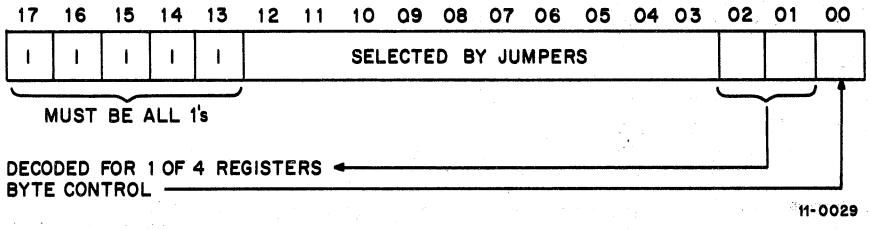


Figure 4-3 Interface Select Address Format

Table 4-1 indicates the gating control signals that determine the bus sequences to be initiated.

Table 4-1
Gating Control Signals

Mode Control C1	Mode Control C0	Byte Control A00	Gating Control Signals True (+3 V)	Bus Sequence
0	0	0	IN	DATI
0	0	1	IN	DATI
0	1	0	IN	DATIP
0	1	1	IN	DATIP
1	0	0	OUT LOW OUT HIGH	DATO
1	0	1	OUT LOW OUT HIGH	DATO
1	1	0	OUT LOW	DATOB
1	1	1	OUT HIGH	DATOB

4.3 INTERRUPT CONTROL

The interrupt control logic permits the DR11-K to gain control of the bus (become bus master) and perform an interrupt operation. The switches and jumpers on this logic can be arranged so that vector addresses can be assigned other than those configured as standard on the module for alignment. (Refer to Chapter 5 for details.) The interrupt control logic consists of a dual interrupt request and grant acknowledge circuit for establishing bus control.

One method of causing interrupts to the Unibus employs the two control lines between the DR11-K and the external device. If the Input Interrupt Enable (bit 06 of the status register) is set, a negative transition (+3 V to ground) of the EXTERNAL DATA READY pulse will generate an interrupt to the Unibus, with a vector address of 300. (Refer to circuit schematic D-CS-M7843-0-1, sheet D5.) A bus request is made on the BR level that corresponds with the level of the priority plug in the logic (sheet D2). (The standard level for the DR11-K interface is BR4; this may be changed on the priority plug if desired.) When the priority arbitration logic in the processor recognizes the request and issues a bus grant signal, the master control circuit acknowledges with a SACK signal. The control line method of interrupting is logically ORed into the DR11-K interrupt control, and is disabled by internal clamping circuitry if not desired.

The second method of interrupting is by using the individual input lines. Each input (IN15:IN00) is buffered by a flip-flop that will set on a negative transition (+3 V to ground). (Refer to circuit schematic D-CS-M7843-0-1, sheet D6.) Switches for the buffered bits on the M7843 module make it possible to wire-OR each bit onto a common interrupt line; when the Input Interrupt Enable (bit 06 of the status register) is set and a switch is on, the transition of the associated bit causes an interrupt to the Unibus. The bits are read under program control by reading the input register, and are cleared by moving data 1s to the bits to be cleared. The Input Interrupt Enable is cleared when an input interrupt is accepted by the Unibus; when reset, it will retrigger the interrupt circuit if any other input bits were set during the program service subroutine, so that new interrupting bits will not be lost.

When data is loaded into the output register in byte or word format, a pulse on INTERNAL HIGH DATA READY or INTERNAL LOW DATA READY permits the user to transfer data to two 8-bit devices or to a 16-bit device (sheet D7). Upon accepting the data, the external device sends EXTERNAL DATA ACCEPTED, causing an interrupt to the Unibus, vector address 304, if the Output Interrupt Enable (bit 14 of the status register) is set. The enable is cleared when the Unibus accepts the interrupt.

Vector addresses are determined by bits D08:D02. Bits D08:D03 are selectable by PC-mounted microswitches, as described in Chapter 5, to determine the two most significant octal digits of the addresses (sheet D2). D02 determines the least significant digit, so that all vector addresses end in either 0 (input) or 4 (output). When the bus indicates an output transfer, assertion of D02 causes a vector at location 304; for an input transfer, the unassertion of D02 causes a vector at location 300.

If the DR11-K is not issuing a request for an interrupt, the BG IN signal is allowed to pass through the logic to BG OUT (sheet D2). The ANDing of the request and the enable is necessary to request bus use. These levels must be true until the Unibus interrupt service routine clears one or the other. Bus control is maintained until the processor responds with BUS SSYN after it has strobed in the interrupt vector; the logic then inhibits further bus requests from that source until either the request or the enable is dropped and then reasserted, preventing the logic from reasserting the request line. This prevents multiple interrupts when the master control is used to generate interrupts.

4.4 STATUS REGISTER

The status register (sheet D4) is a 16-bit register used to report the status of the external control lines, enable interrupts, and generate maintenance interrupts to the Unibus. (Figure 2-2 shows the status register data flow and gating.)

Four of the bits (06, 07, 14, and 15) are read/write bits under program control, and can be read or loaded from the bus. The other two bits (05 and 13) are write-only bits used for maintenance only, and are applied directly to the interrupt control logic to initiate an interrupt sequence. The read/write capability is accomplished by the BUS DATA IN and BUS DATA OUT gating logic shown on sheet D4. A simplified version of a representative bit (bit 06) is shown in Figure 4-4. The other three read/write bits function similarly.

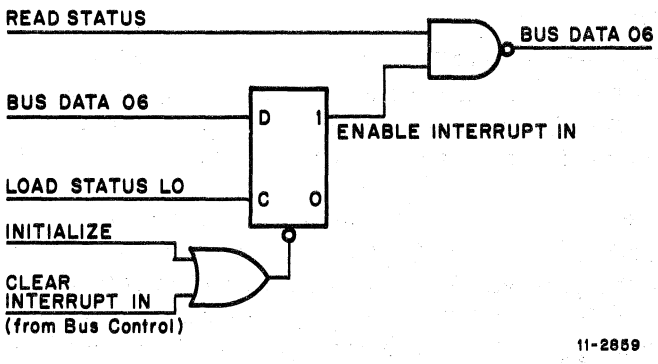


Figure 4-4 Status Register I/O Gating (Representative Bit)

When the status register is addressed for reading, READ STATUS from the address selection logic gates the ENABLE INTERRUPT IN output of the flip-flop to bus data line 06 for reading (Figure 4-4).

If it is desired to load the status register, the appropriate level is placed on bus line BUS D06 and serves as the data input to the flip-flop. The clock input becomes true when the register is addressed for loading.

The flip-flop outputs of bits 06 (ENABLE INTERRUPT IN) and 14 (ENABLE INTERRUPT OUT) are applied as an enabling level to the interrupt control logic described in Paragraph 4.3.

4.5 OUTPUT BUFFER

The output buffer is a 16-bit read/write register that can be read or loaded from the Unibus. When this buffer is addressed for loading, the LOAD OUT HIGH and LOAD OUT LOW signals are true, and applied to one-shot delays that are set up for an output of 1 μs (sheet D7). (In user applications involving long cabling, the added capacitance may require more time. By increasing the resistance factor by a value of up to 50 kilohms, as discussed in Chapter 5, it is possible to increase the one-shot delay by up to an additional 4 μs.) The resulting INTERNAL HIGH DATA READY or INTERNAL LOW DATA READY signal is transmitted to the external device to inform the user that the output buffer register has been loaded in byte or word format. These signals load the output buffer close to their leading edges; to allow for long cabling, the user's logic should sample the data lines on the trailing edges of the pulses (Figure 4-5). The output buffer can be loaded with a full 16-bit word (DATO), or with either a high-order or low-order 8-bit byte (DATOB). Selection of a DATO or DATOB depends on the incoming address and the address selection circuits described in Paragraph 4.2.

4.6 INPUT BUFFER

The 16-bit input register receives data from an external device for transmission to the Unibus. Each input has its noise immunity increased by receivers with hysteresis, and has overvoltage and current protection circuitry. The input register can be either read off the input lines or buffered by a 16-bit buffer register, which is selectable by solder jumpers (Chapter 5). When the input register is read off the input lines, each bit is represented by a logical 1 as a Low (less than 1 V) and by a logical 0 as a High (+3 V). When data is read from the input buffer register, each buffer bit is set by a negative transition on the associated register input line. Bits 15–12 can also be selected (by solder jumpers) to be set by positive transitions or by either positive or negative transitions (Chapter 5).

There are two control lines associated with the input register, EXTERNAL DATA READY and INTERNAL DATA ACCEPT. The external device places data on the input lines and, after transients have had time to settle (Figure 4-6), activates the EXTERNAL DATA READY signal line, generating an interrupt to the Unibus (Paragraph 4.3). When the data is read, the DR11-K activates the INTERNAL DATA ACCEPTED line to notify the external device that it can send new data. If these lines are not used, internal clamping will disable them. The buffer register bits can also be selected by microswitches to generate interrupts to the Unibus (Paragraph 4.3 and Chapter 5).

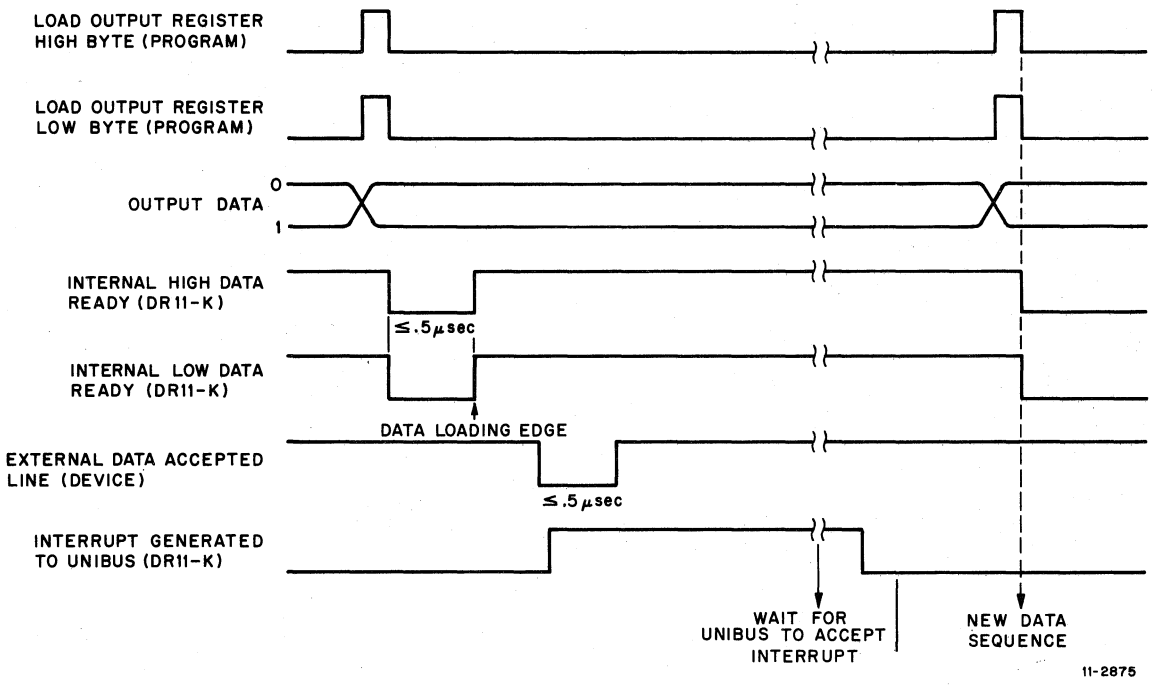


Figure 4-5 Data Outputting Timing Diagram

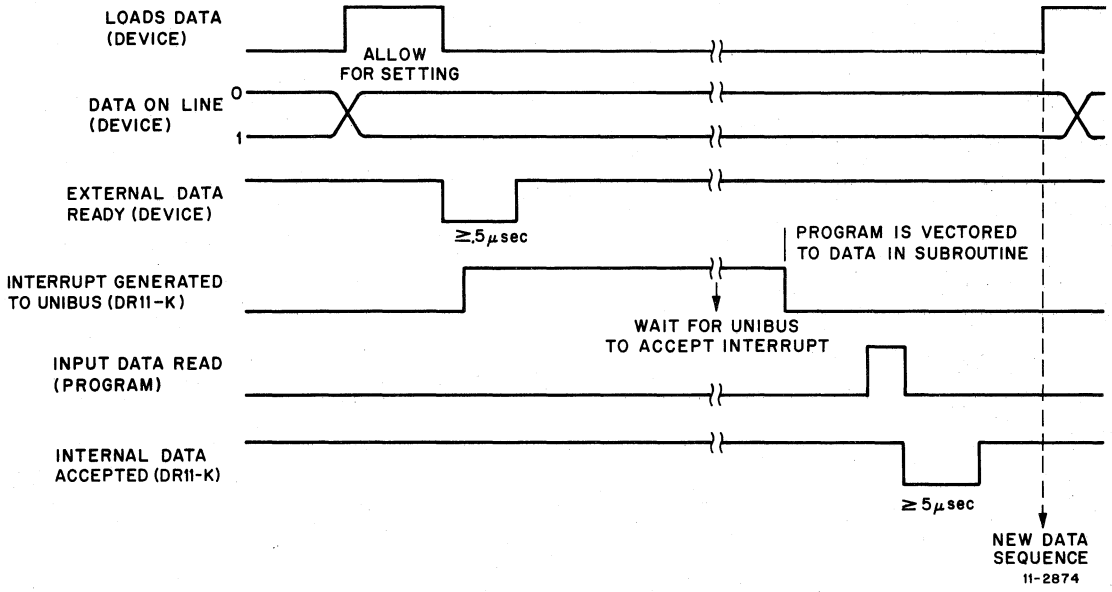


Figure 4-6 Data Input Timing Diagram

CHAPTER 5
INSTALLATION AND CHECKOUT

5.1 INSTALLATION

The DR11-K interface is designed for use in one of the center SPC slots of a DD11-A or DD11-B. Before the M7843 module is installed, all of the jumpers and microswitches should be configured to select the desired options. The switches and jumpers are marked on the module itself for easy identification. The paragraphs that follow discuss the switch and jumper configurations and the options that they control.

If other than standard configurations are selected, all MAINDEC and other software programs referencing the standard assignments must be modified to reflect the new configurations.

5.1.1 Input Data Path Selection

Each input line can be configured so that its data can be read directly off the line or from the buffer register, depending on the configuration of jumpers W5 through W20. Table 5-1 indicates the solder-type jumper configurations that will select each input data path. The module is normally shipped with the jumpers configured to select buffer register input on all lines. Figure 5-1 contains a block diagram of a representative input line, showing the data inputting and interrupting paths.

Table 5-1
Input Data Path Jumper Selection

Input Line	Jumpers for Reading	
	Direct Line Input	Buffer Register Input*
15	W5-B	W5-A
14	W6-B	W6-A
13	W7-B	W7-A
12	W8-B	W8-A
11	W9-B	W9-A
10	W10-B	W10-A
9	W11-B	W11-A
8	W12-B	W12-A
7	W13-B	W13-A
6	W14-B	W14-A
5	W15-B	W15-A
4	W16-B	W16-A
3	W17-B	W17-A
2	W18-B	W18-A
1	W19-B	W19-A
0	W20-B	W20-A

*Normal configuration for shipment.

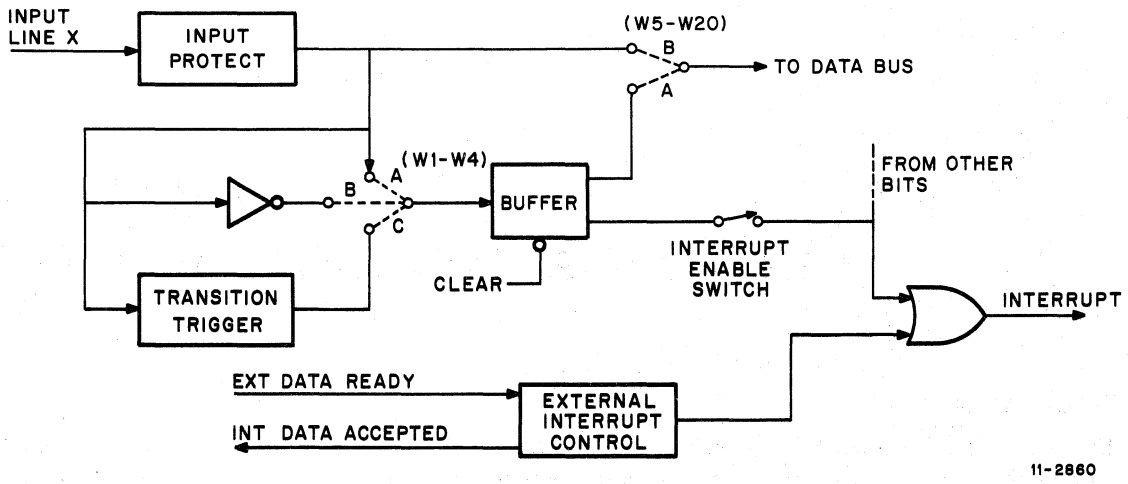


Figure 5-1 Representative Input Line Block Diagram

5.1.2 Input Definition Selection

The input definition of lines 15 through 12 can be further selected to be set by a positive transition, a negative transition, or either a positive or a negative transition. These options are controlled by jumpers W1 through W4, as Table 5-2 indicates. The module is normally shipped with these jumpers configured for a negative transition (+3 V to ground).

Table 5-2
Input Lines 15:12 Jumper Configuration

Input Line	Negative Input	Positive Input	Positive or Negative Input
15	W1-A	W1-B	W1-C
14	W2-A	W2-B	W2-C
13	W3-A	W3-B	W3-C
12	W4-A	W4-B	W4-C
	standard		

5.1.3 Interrupt Enable Selection

Each bit in the buffer register can be selected to generate an interrupt to the Unibus. This selection is controlled by microswitches on the module. Table 5-3 indicates which switch enables each bit to generate an interrupt.

5.1.4 Device Selection Addresses

The DR11-K requires three device selection addresses, for the input, output, and status registers. These addresses are selectable by microswitches marked on the M7843 module as A12 through A3. Table 5-4 indicates the selectable address bits and the associated switches. The module is normally shipped with these bits configured for an address of 16777x. The least significant octal digit is software-controlled by bits A02, A01, and A00, and is always 0 for the status register address, 2 for the input address, and 4 for the output address. A switch OFF = logical 1, and a switch ON = logical 0.

Table 5-3
Interrupt Enable Switch Chart

Input Register Bit	Switch
15	S1-4
14	S1-1
13	S1-3
12	S1-2
11	S1-6
10	S1-5
9	S2-5
8	S2-6
7	S1-7
6	S1-8
5	S2-8
4	S2-7
3	S2-1
2	S2-2
1	S2-4
0	S2-3

Table 5-4
Device Selection Address Lines

	UNIBUS ADDRESS LINES														
	A15	**A14**	**A13**	**A12**	**A11**	**A10**	**A09**	**A08**	**A07**	**A06**	**A05**	**A04**	**A03**	**A02**	**A01**	**A00**
Bits Which are Selectable				X	X	X	X	X	X	X	X	X	X			
Module Standard Configuration				ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF			
Switch ID				S3-2	S3-3	S4-3	S4-8	S4-4	S4-5	S4-7	S4-6	S4-2	S4-1			

5.1.5 Vector Address Selection

The DR11-K requires two vector addresses, one for the data input vector and the other for the data output vector. The two most significant octal digits of these addresses are controlled by microswitches marked on the module as V8 through V3, which correspond to bits D8 through D3. Table 5-5 shows the selectable bits and the standard configuration in which the module is usually shipped, which selects a vector address of 30x. (A switch ON = a logical 1, and a switch OFF = a logical 0.) The least significant octal digit of the vector address is hardware-controlled by bit D2, so that the standard input vector address is 300 and the standard output vector address is 304.

Table 5-5
Vector Address Selection Lines

	UNIBUS DATA LINES															
	D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
Bits Which are Selectable								X	X	X	X	X	X			
Module Standard Configuration								OFF	ON	ON	OFF	OFF	OFF			
Switch ID								S3-8	S3-7	S3-1	S3-5	S3-4	S3-6			

5.1.6 Control Line Polarity Selection

The DR11-K output control lines (INTERNAL DATA ACCEPTED, INTERNAL HIGH DATA READY, and INTERNAL LOW DATA READY) are generated by one-shot delays normally configured for an output of 1 μs (circuit schematic D-CS-M7843-0-1, sheet D7). By increasing the resistance for each one-shot, it is possible to increase the output time of the signal up to 5 μs (Figure 5-2) for user applications in which long cabling and the resulting capacitance necessitate added delay. It is possible to select the polarity of the control signals by solder-type jumpers, according to Table 5-6.

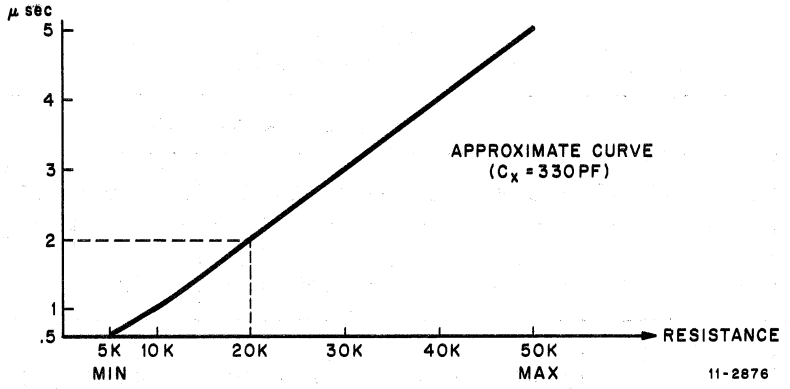


Figure 5-2 Control Line Output Time Variation (R118, R120, and R121)

Table 5-6
Control Line Polarity Selection

	Jumper Selection		
	INT DATA ACCEPT	INT HIGH DATA READY	INT LOW DATA READY
Positive Output	W23-B	W21-B	W22-B
Negative Output	W23-A Standard	W21-A Standard	W22-A Standard

5.1.7 Coulter Model "S" Selection

To use the DR11-K as an interface to the Coulter Model "S", the four most significant bits are set up for interrupting on an input change, and all lines are configured for direct line input. Table 5-7 shows this configuration.

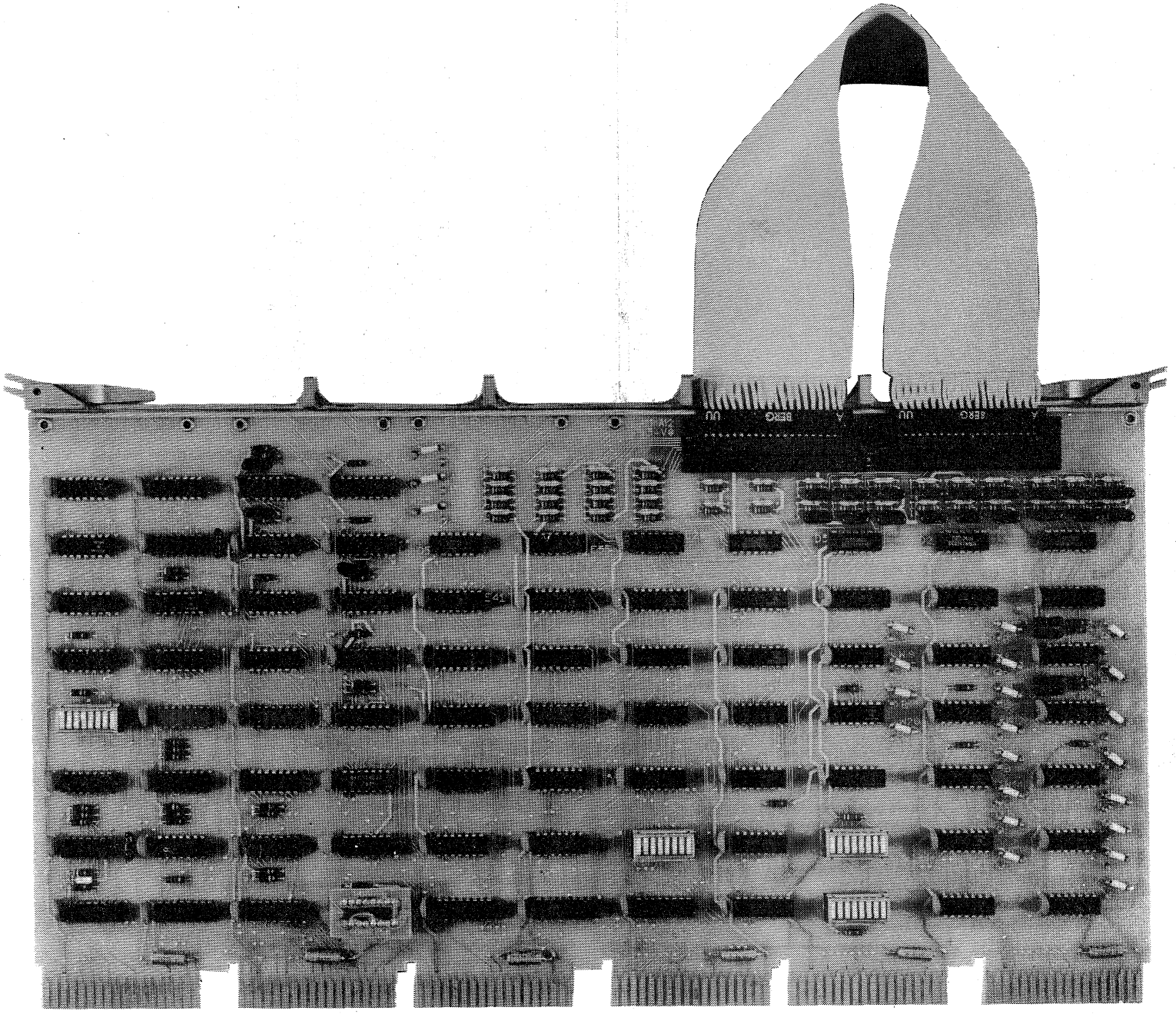
Table 5-7
Coulter Model "S" Input Configuration

Data Line	Jumpers for Data Input Paths	Interrupt Enable Switch	Jumper for Input Buffer Setting Edge
15	W5-B	S1-4 ON	W1-C
14	W6-B	S1-1 ON	W2-C
13	W7-B	S1-3 ON	W3-C
12	W8-B	S1-2 ON	W4-C
11	W9-B	S1-6 OFF	–
10	W10-B	S1-5 OFF	–
09	W11-B	S2-5 OFF	–
08	W12-B	S2-6 OFF	–
07	W13-B	S1-7 OFF	–
06	W14-B	S1-8 OFF	–
05	W15-B	S2-8 OFF	–
04	W16-B	S2-7 OFF	–
03	W17-B	S2-1 OFF	–
02	W18-B	S2-2 OFF	–
01	W19-B	S2-4 OFF	–
00	W20-B	S2-3 OFF	–

5.2 MAINTENANCE AND CHECKOUT

Checkout and testing are accomplished by using the maintenance cable supplied with each DR11-K interface. That cable (a one-foot BC08-R cable) is connected to both of the 40-pin H854 connectors as shown in Figure 5-3, so that the output lines of the DR11-K are jumpered to its input lines, and any 16-bit word loaded into the output register is fed back into the input register. If the word read is identical to that loaded, the input buffer, output buffer, and associated circuits may be presumed to be operating properly.

Installation testing may be performed by running DR11-K Digital I/O Test (MAINDEC-11-DZDRG). If performance of this test fails to disclose any errors, it may be assumed that the DR11-K is operational, and that it has been correctly installed.



7195-4

Figure 5-3 M7843 Module with Maintenance Cable

CHAPTER 6
DR11-K EXAMPLES

6.1 INTRODUCTION

This chapter contains examples of some of the applications for which the DR11-K can be adapted.

6.2 INPUT EXAMPLES

The paragraphs below include examples of possible configurations that use the DR11-K. Paragraph 6.4 discusses in more detail a specific input application.

6.2.1 Input Example 1

Application: An external device with 15-bit binary output and two control lines. When the device has placed data on the data lines, it generates a signal on one of the control lines and holds the data on the data lines until it receives a data acknowledgment on the other control line.

Solution: Because the external device has only a 15-bit output and the DR11-K has a 16-bit input, the sixteenth bit is left unconnected, and is disabled by internal clamping circuitry so that it reads as a logical 0 to the software. The data input of the DR11-K should be set for direct line input (Table 5-1), as the external device is capable of holding data on the data lines (Figure 6-1).

6.2.2 Input Example 2

Application: An external device with 16-bit binary output and two control lines; the data is strobed onto the device output lines. Because the data is strobed onto the data lines, some type of holding register is needed. When the data has been strobed onto the lines, a signal is generated on one of the control lines, after which the external device waits for a data acknowledgment on the other control line before strobing new data onto the data lines.

Solution: The bits of the DR11-K input buffer register are edge-triggered, so that the data on the data line will set each register bit on a negative transition (+3 V to ground) and will be held until the software clears the register. The data input of the DR11-K should be set up for a register input (Tables 5-1 and 5-2). Figure 6-2 shows this example graphically.

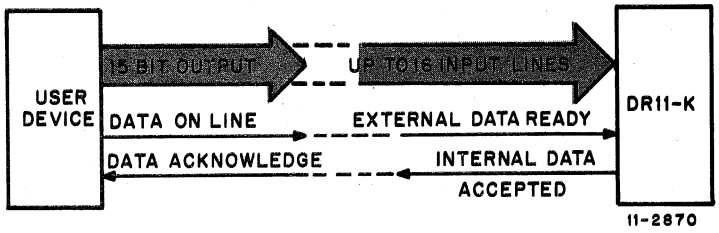


Figure 6-1 Block Diagram of Input Example 1

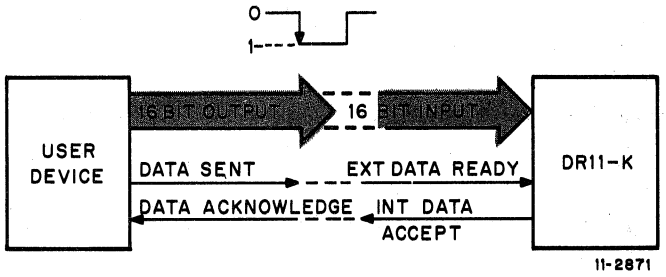


Figure 6-2 Block Diagram of Input Example 2

6.2.3 Input Example 3

Application: Three devices, each connected to a DR11-K as in Example 1, and each with three pushbutton switches, signifying:

Test Start
Test Stop
New Segment of Data Control

User software is such that it needs to be kept aware of these control functions. Signals produced by the switches are TTL-compatible, and are available off a separate connector on the back of each device.

Solution: In this example, the input lines are used to generate interrupts (Figure 6-3). The input jumpers (Table 5-1) should be set for a register input, so that the software can read the interrupting bits. Each interrupt enable switch is turned ON, allowing any input bit to generate an interrupt.

6.3 OUTPUT EXAMPLES

6.3.1 Output Example 1

Application: Transferring data between two PDP-11s via DR11-Ks.

Solution: The DR11-K is designed so that the output lines of one DR11-K can communicate to the input lines of another and vice versa (Figure 6-4).

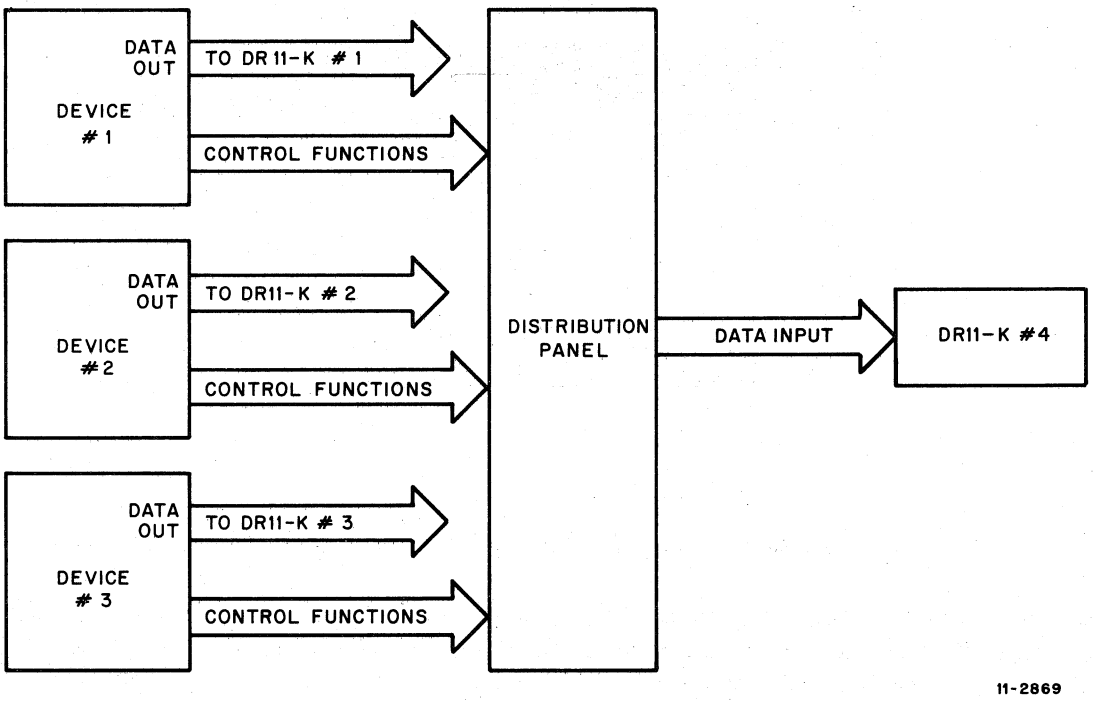


Figure 6-3 Block Diagram of Input Example 3

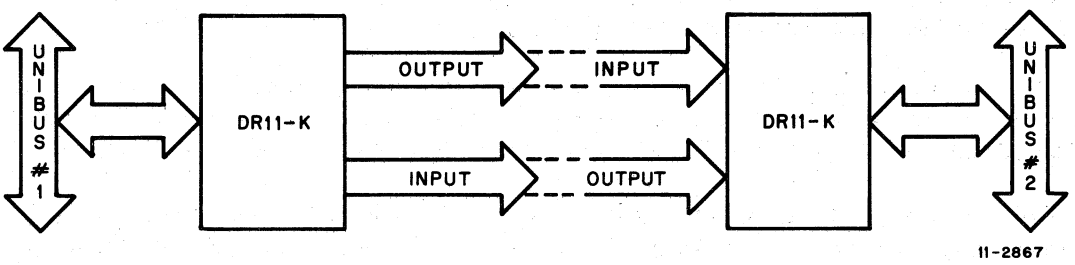


Figure 6-4 Block Diagram of Output Example 1

6.3.2 Output Example 2

Application: Transferring data to two 8-bit devices.

Solution: The output of the DR11-K can be byte-separated to transfer data to two 8-bit devices (Figure 6-5).

6.4 COULTER MODEL "S" BLOOD COUNTER INTERFACING

The dual transitional characteristic of input bits 15 through 12 was designed specifically for interfacing with a Coulter Model "S" Blood Counter. This interfacing provides a good example of the combined use of the input lines for data inputting and interrupting.

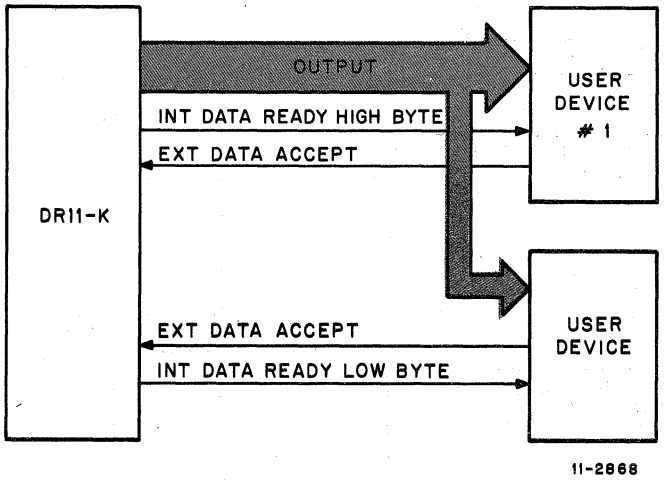


Figure 6-5 Block Diagram of Output Example 2

The Coulter Model "S" has sixteen data output lines, twelve of which are designated as S lines (S12:S01) and provide a 3-digit BCD value for reporting test data. The remaining four lines are designated as Q lines (Q4:Q1), and provide a BCD digit that indicates the test number corresponding to the data currently being reported on the S lines.

To transfer data to the PDP-11 from the Coulter Model "S" via the DR11-K, an interrupt must be generated when new data is ready on the S lines. The Model "S" does not have a signal line specifying that data is ready; because the Q lines indicate the test number and change when new data is available on the S lines, a change on the Q lines is used to generate the interrupt. There is no time difference between the change on the Q lines and the loading of data on the S lines; therefore, the software must allow sufficient delay to permit the S lines to settle.

To accomplish this, input bits 15:12 are selected for positive/negative trigger, so that any transition of the lines generates an interrupt. All sixteen data inputs are selected for direct line input (Table 5-7). Figure 6-6 shows the input characteristics for this application. The BC11-M option is a cable used to connect a DR11-K to a Coulter.

A change on any of the Q lines signifies that there is a test number change in process. The DR11-K then monitors the lines for a change and interrupts the processor when it occurs. The software must allow time for the Coulter data lines to settle. The following program example shows how the software reads data from the Coulter.

```
VECTOR ADDRESS,   BR COULTER          /Coulter interrupt has occurred.
COULTER           JSR PC DELAY        /Go to 50-ms delay subroutine and return.
                  MOV Input, Memory   /Store the data on the DR11-K input.
                  MOV #170000 Input   /Clear the interrupts (Bits 15:12).
                  MOV #040000 Status  /Set up interrupt enable for next input interrupt.
                  RTI                 /Restore program.
```

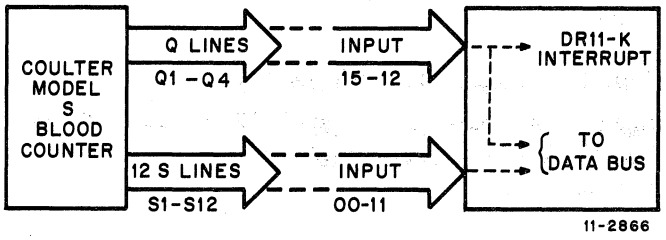


Figure 6-6 Block Diagram of DR11-K/Coulter Interface

DR11-K INTERFACE USER'S GUIDE
AND MAINTENANCE MANUAL
EK-DR11K-MM-001

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