MODEL NS23P
ADD-IN MEMORY SYSTEM
SERVICE MANUAL

National Semiconductor
Memory Systems

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PREFACE

This service manual provides information required to install and maintain the National Semiconductor Corporation (NSC) Model NS23P Add-In Memory System.

The information provided in this manual is comprised of the following:

- System Overview
- Theory of Operation
- Installation
- Maintenance
- Troubleshooting
- Reference Drawings

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Santa Clara, Ca. 95051
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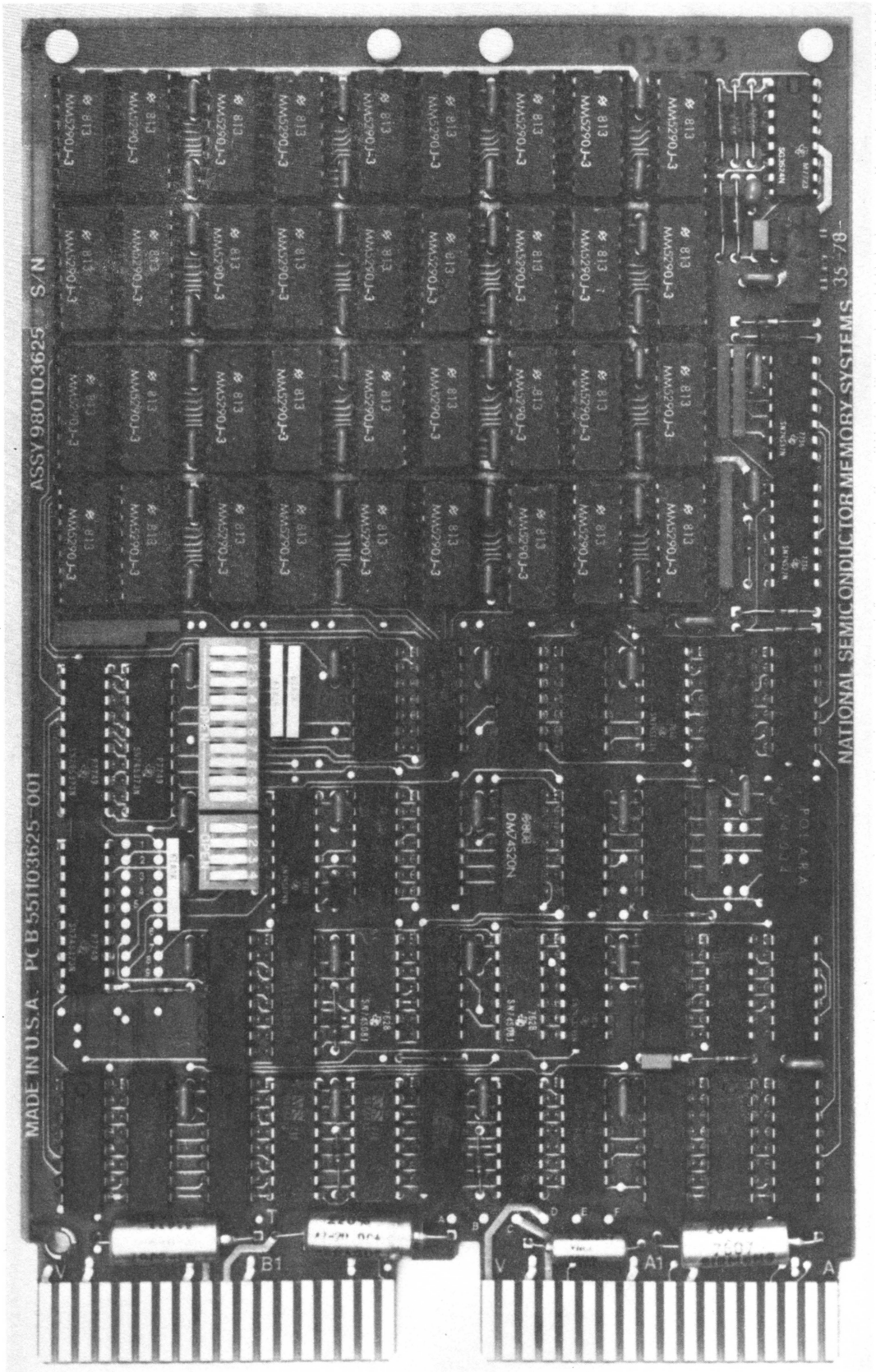


Model NS23P Add-In Memory System

SECTION 1

SYSTEM OVERVIEW

This section provides a general description of the NS23P memory card, including compatibility with other cards and systems; features and options; a mechanical description; power and environmental requirements for proper use; and other documentation.

1.1 GENERAL DESCRIPTION

The NS23P memory card is an add-in memory designed to be compatible with the DEC* (Digital Equipment Corp.) LSI-11/23, PDP-11/03, and LSI-11/2 Microcomputer Systems. The card can be installed in the H9281 or H9270 backplanes and works in conjunction with the DEC MSV11-D and MSV11-E series semiconductor memory cards.

Its standard memory capacity is 32,768 words by 18 bits (32k x 18). The 32,768 words can be assigned anywhere within the LSI-11 128k word address space in any one or multiple 4k word increments.

1.2 FEATURES AND OPTIONS

1.2.1 FEATURES

The following paragraphs discuss the user controllable features of the NS23P memory card.

*DEC, LSI 11, LSI 11/23, LSI 11/2 and PDP-11/03 are registered trademarks of the Digital Equipment Corporation.

1.2.1.1 Internal or External Refresh

The user can select whether refresh is controlled by the LSI-11 processor or by the refresh circuitry on the card itself through jumper points provided on the board.

1.2.1.2 Battery Back-up Provisions

The NS23P memory card can be used with battery back-up for LSI-11 semiconductor memory systems. The card comes with +5VB and +12VB battery back-up voltage pins, compatible with the voltage pins DEC provided on the MSV11 MOS memory card.

1.2.1.3 BRPLY External Refresh Response

The NS23P memory card can be configured for external refresh operations during installation. Jumper points are provided on the card which permit the user to allow the generation of a BRPLY signal to an external refresh command.

1.2.1.4 Expanded Address Space Operation

The standard NS23P memory card can operate anywhere within the 128k address space of the LSI-11/23 system.

1.2.2 OPTIONS

There are the following factory installable options for the NS23P memory card.

1.2.2.1 Parity Generation and Check

See paragraphs 2.1.2.1, 2.5.1, and 2.5.2 for discussions of parity generation and check.

1.2.2.2 8k or 16k RAM Operation

The standard NS23P card uses 16k RAMs as the memory elements, providing a maximum storage capacity per card of 32k words. The user can select 8k RAMs as the memory elements when ordering. This option permits maximum storage capacity per card of 16k words.

1.2.2.3 Optional Capacities

Optional capacities are available from a minimum of 4,096 words by 16 bits (4k x 16) to a maximum of 32,768 words by 18 bits (32k x 18).

1.3 MECHANICAL DESCRIPTION

The NS23P memory is completely contained on one multilayer printed circuit card. It is designed to plug directly into standard H9270 ("Quad"), H9281 ("Dual") LSI-11 backplane/card guide assemblies, and the DDV11-B ("Hex") expansion unit. Its dimensions are:

PCB	Thickness	0.056"	Nominal
	Width	5.19"	
	Length	8.93"	(Includes plastic handles)
Max. component height		0.375"	
Max. total thickness		0.490"	

1.4 POWER REQUIREMENTS

The following are power requirements for the use of the NS23P memory card.

1.4.1 PARAMETERS AND CONDITIONS

The NS23P requires both of the following voltages: +5.0 volts ± 5% and +12.0 volts ± 5%.

1.4.2 POWER CONSUMPTION

The NS23P memory card in a 32k x 18 configuration has the following current requirements:

	Standby	Operating
+5.0 volts	2.0 A max.	2.0 A max.
+12.0 volts	110 mA max.	450 mA max.

1.4.3 BATTERY BACK-UP VOLTAGE REQUIREMENTS

The battery back-up voltages must meet requirements (per card) of +12 volts $\pm$ 5% at 110 mA max. and +5 volts $\pm$ 5% at 775 mA max.

1.5 ENVIRONMENTAL REQUIREMENTS

The NS23P memory card will operate at a temperature of $5^{o}C$ to $50^{o}C$ and at a humidity of 10% to 90% (no condensation).

SECTION 2

THEORY OF OPERATION

This section provides a detailed discussion of the operation of the NS23P add-in memory. Beginning with an interface description, the discussion proceeds with a functional overview of the card, using a block diagram. Individual functional blocks, data paths, and timing considerations are then covered, with an emphasis on use of the schematics in Appendix A.

2.1 INTERFACE DESCRIPTION

Interface between the NS23P add-in memory system and the Digital Equipment Corporation LSI-11 Microcomputer System (or others) is conducted by means of eight input signals to the NS23P, two output signals to the CPU, and 18 bi-directional signal lines (address and data) on the memory card. Table 2-1 gives the connector assignments of signals, power, and other elements of the interface.

The memory card presents one standard bus load to the LSI-11 bus for each of the signals.

2.1.1 INPUT SIGNALS TO MEMORY SYSTEM

The eight input signals from the LSI-11 CPU to the NS23P are described briefly in this section. The specific purpose of each signal in the operation of the memory system will become clear as each functional module of the system is described in detail later in this section.

Table 2-1. I/O Connector Pin List

Component Side	Pin	Pin	Solder Side
A Connector			
	A1	A2	+5 Volts
	B1	B2	
BDAL16 L	C1	C2	Ground
BDAL17 L	D1	D2	+12 Volts
	E1	E2	BDOUT L
	F1	F2	BRPLY L
	H1	H2	BDIN L
Ground	J1	J2	BSYNC L
REF KILL L	K1	K2	BWTBT L
	L1	L2	
Ground	M1	M2	BIAKI L
	N1	N2	BIAKO L
	P1	P2	BBS7 L
BREF L	R1	R2	BDMGI L
+12V BATT	S1	S2	BDMGO L
Ground	T1	T2	BINIT L
	U1	U2	BDAL00 L
+5V BATT	V1	V2	BDAL01 L
B Connector			
BDCOK	A1	A2	+5 Volts
	B1	B2	
	C1	C2	Ground
	D1	D2	+12 Volts
	E1	E2	BDAL02 L
	F1	F2	BDAL03 L
	H1	H2	BDAL04 L
Ground	J1	J2	BDAL05 L
-5 Volts out	K1	K2	BDAL06 L
-5 Volts in	L1	L2	BDAL07 L
Ground	M1	M2	BDAL08 L
	N1	N2	BDAL09 L
	P1	P2	BDAL10 L
	R1	R2	BDAL11 L
	S1	S2	BDAL12 L
Ground	T1	T2	BDAL13 L
	U1	U2	BDAL14 L
+5 Volts	V1	V2	BDAL15 L

2.1.1.1 BDOUT

This signal is an indication to the memory card that a write (DATO) cycle is to be performed. It must be activated as shown in the timing diagrams in Figures 2-1 and 2-2 in the proper relationship to BSYNC.

2.1.1.2 BDIN

This signal is an indication to the memory card that the BRPLY response from the memory card is to be activated during a read cycle (DATI), the read portion of read-modify-write, or an external refresh cycle. It must be activated as shown in Figures 2-1, 2-3, and 2-4 in proper time relationship with BSYNC.

2.1.1.3 BSYNC

This signal is an indication to the memory card that either a read (DATI) or read-modify-write (DATIO-B) cycle will be initiated, a write cycle will be initiated when BDOUT is received, or an external refresh cycle should be initiated. The type of cycle initiated is a function of the state of the BDIN, BDOUT, and BREF lines when BSYNC goes to its active state as shown in Figures 2-1 through 2-4.

2.1.1.4 BWTBT

This signal, when used in conjunction with BSYNC and BDOUT, allows the board to determine whether a whole word (16 bits) or a byte (8 bits) is to be written during a write (DATO) or a read-modify-write (DATIO-B) cycle. Activating BWTBT during a write cycle as shown in Figures 2-2 and 2-3 is an indication to the card to write into the byte specified by address bit A00.

2.1.1.5 BREF

This signal, in conjunction with BSYNC (as shown in Figure 2-4), is an indication to the card to perform a refresh cycle. The card will respond to this signal only if it has been configured for external refresh operation.

2.1.1.6 REF KILL

This signal, when active, will disable the internal refresh circuitry from executing a cycle.

2.1.1.7 BDCOK

This signal is an indication to the memory card that the LSI-11 system has lost its dc power. It is used to prevent the memory card from being inadvertently selected on power up or power down.

2.1.1.8 BINIT

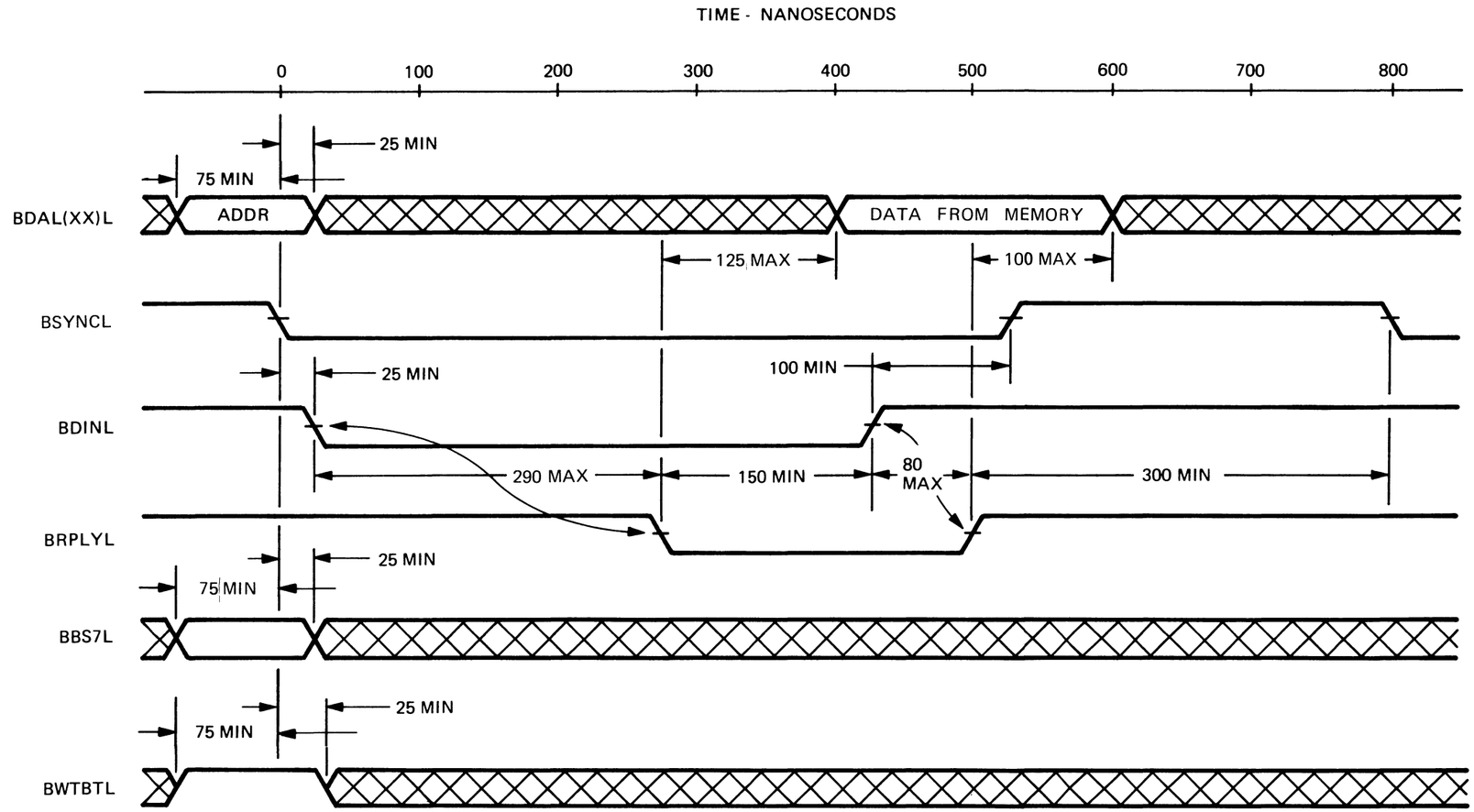
This signal is used to reset internal select registers.

2.1.1 OUTPUT SIGNALS

The two output signals from the NS23P to the LSI-11 CPU are described briefly in this section. The specific purpose of each signal in the operation of the memory system will become clear as each functional module of the system is described in detail later in this section.

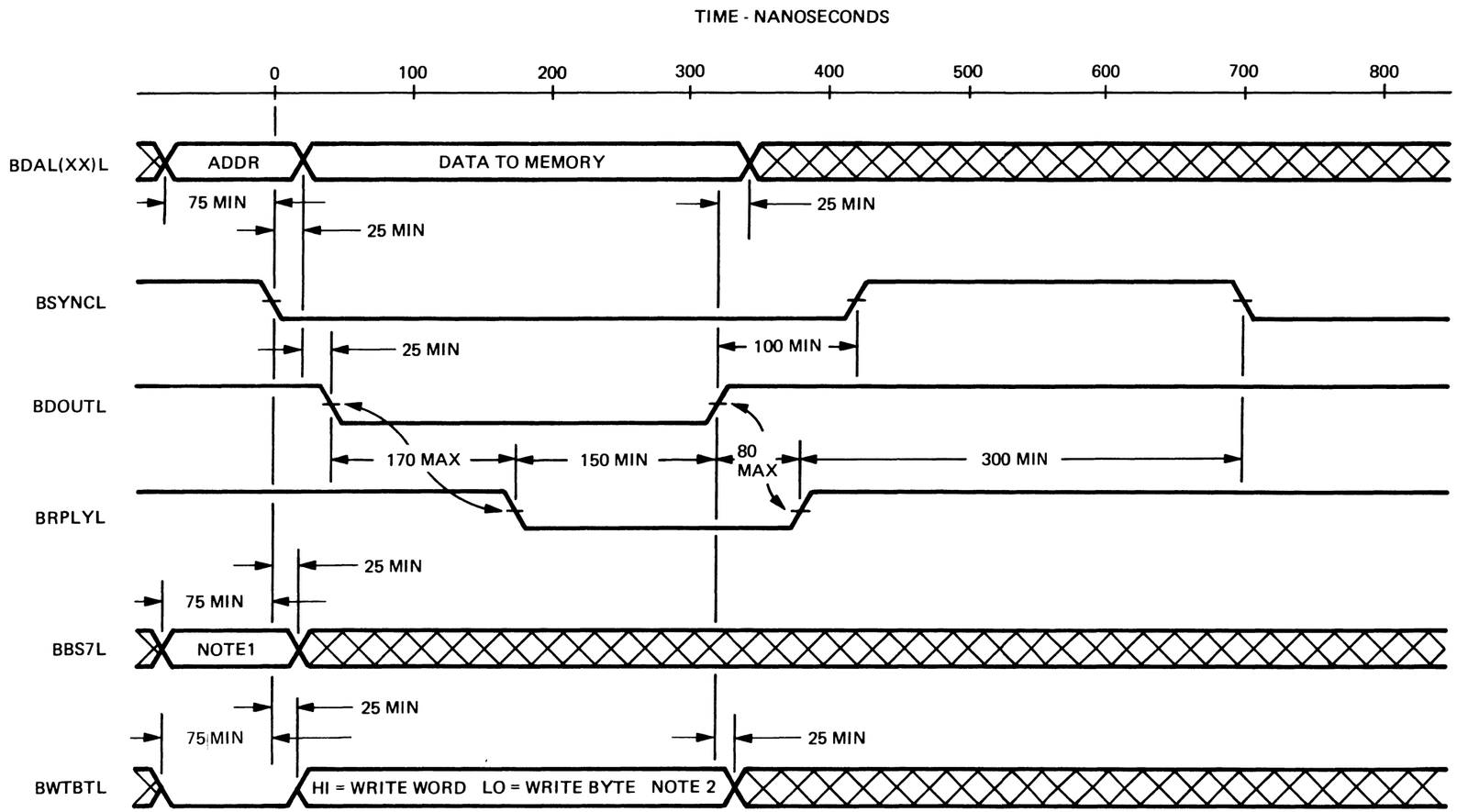
2.1.2.1 PARERR

If the parity generation and check option has been selected, PARERR indicates a parity error. Parity is generated on a byte basis on all write cycles and checked on a byte basis on all read cycles. The PARERR signal appears on the address 16 signal line (BDAL 16L).



NOTES:
1. BBS7L IS A MEMORY ADDRESS SELECT TERM. BBS7L HI, MEMORY SHALL RESPOND. BBS7L LO AND BANK SELECT SWITCHES OPEN, MEMORY SHALL NOT RESPOND.
2. FOR BWTBTL HI DURING DATA TIME, A FULL WORD IS WRITTEN, FOR BWTBTL LO DURING DATA TIME, A BYTE IS WRITTEN ACCORDING TO BDAL00L AT ADDRESS TIME,IF BDAL00L IS HI, BITS 00-07 ARE WRITTEN, IF BDAL00L IS LO, BITS 08-15 ARE WRITTEN.

Figure 2-1. Read (DATI) Timing



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2. FOR BWTBTL HI DURING DATA TIME, A FULL WORD IS WRITTEN, FOR BWTBTL LO DURING DATA TIME, A BYTE IS WRITTEN ACCORDING TO BDAL00L AT ADDRESS TIME, IF BDAL00L IS HI, BITS 00-07 ARE WRITTEN, IF BDAL00L IS LO, BITS 08-15 ARE WRITTEN.

Figure 2-2. Write (DATO-B) Timing

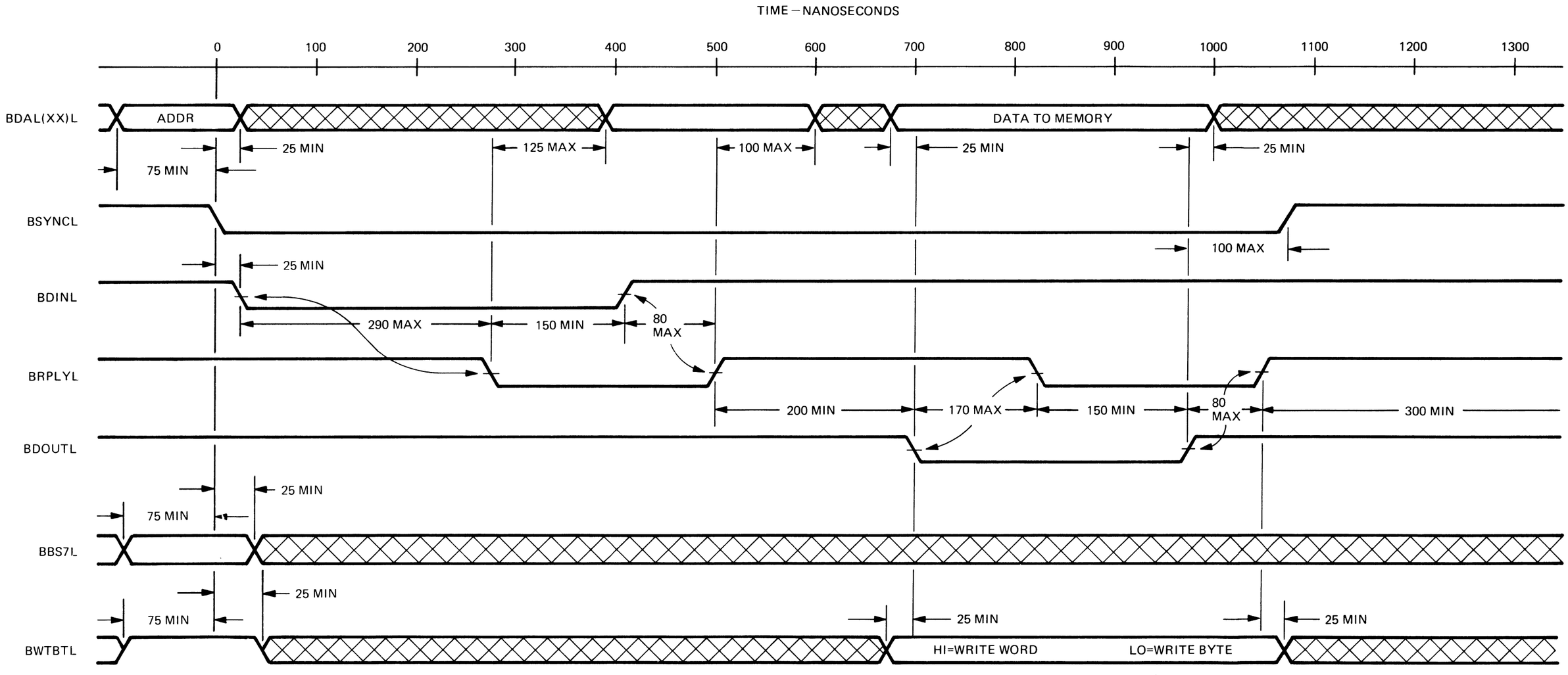


Figure 2-3. Read-Modify-Write (DATIO-B) Timing

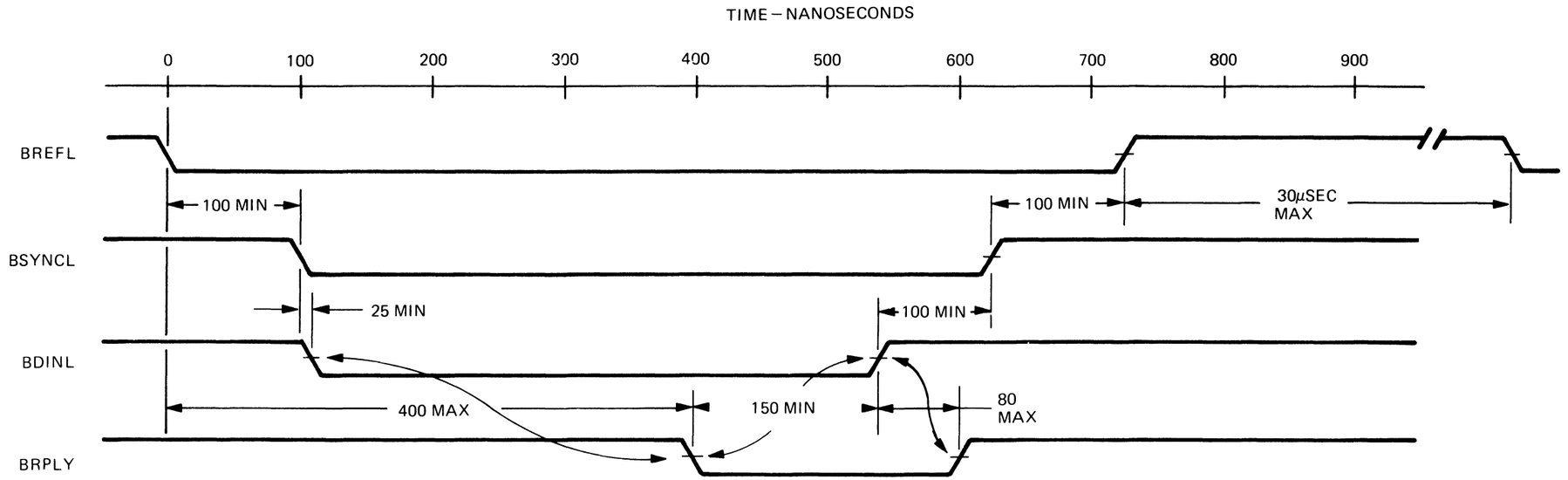


Figure 2-4. Refresh (EXTERNAL) Timing

2.1.2.2 BRPLY

This signal is an acknowledgement by the card of the receipt of a BDIN or BDOUT during a read, write, or read-modify-write mode of operation. It is also an acknowledgement of the receipt of BREF if the card has been configured for external refresh operation.

2.1.3 BI-DIRECTIONAL SIGNALS (BDAL00-BDAL17)

The 18 bi-directional signal lines provide the memory card with address and data information. These lines are time-multiplexed between the address and data in/out during any cycle externally requested of the memory card. As shown in Figures 2-1 and 2-2, the card interprets the data on these lines in relationship to BSYNC, BDIN, BDOUT, and BRPLY. At -75 to +25 nanoseconds either side of the falling edge of BSYNC, the data is interpreted as address information; at all other times, as data into or out of the card.

2.2 FUNCTIONAL OVERVIEW

This section describes the operation of the NS23P during write and read cycles from a general standpoint. Detailed discussion of the timing for each of these cycles is provided elsewhere in the manual.

Figure 2-5 is the block diagram for the NS23P. The major blocks of the memory system are the interface transmitter-receiver, the address register, the parity generation and checking unit, the refresh address, module select, timing and control, the three-to-one multiplexer, and the memory array itself. The memory array may be configured from 8k x 16 bit minimum to 32k x 18 bit maximum; the 18-bit width with parity, the 16-bit width without.

2.2.1 READ CYCLE OVERVIEW

Data coming from the interface transmitter-receiver along the BDAL lines (0-17) is asserted 75 nanoseconds (ns) before the low-going edge of the BSYNC line and held for 25 ns beyond it, thus defining address time (see Figure 2-1). Simultaneously with address time, the bank select signal (BBS7) determines if the memory module or a peripheral is to respond. The remaining time for the bus is defined as data time.

At the end of address time, the BDIN signal is taken low, and hand-shaked with a reply signal (BRPLY) from the memory card 225 ns (max.) later. In sequence, 125 ns (max.) after BRPLY goes low, data is brought from memory to the bus; 150 ns (min.) after BRPLY has gone low the processor returns BDIN to its high state; BRPLY returns to high; BSYNC returns high. Data remains on the bus for 100 ns (max.) after BRPLY goes high, and a new cycle may be initiated after 300 ns (min.).

2.2.2 WRITE CYCLE OVERVIEW

The write cycle operates on the same principle as the read cycle with a slight difference in timing. Data is available on the bus immediately after address time, then the handshaking between BDOUT and BRPLY takes place as before. The BWTBT is also brought into play during the write cycle: If BWTBT is high, a full word is written; if BWTBT is low, a byte is written in conjunction with the BDAL00 signal (BDAL00 high, bits 00-07; BDAL00 low, bits 08-15). The memory module is selected according to the address and BBS7, as in the case of a read cycle.

2.2.3 OTHER CYCLES

This concludes the overview of the two main cycles in the NS23P memory system. The read-modify-write and refresh cycles will be described in detail in Section 2.5. No overview is provided since the read-modify-write cycle is essentially a read followed by a write cycle.

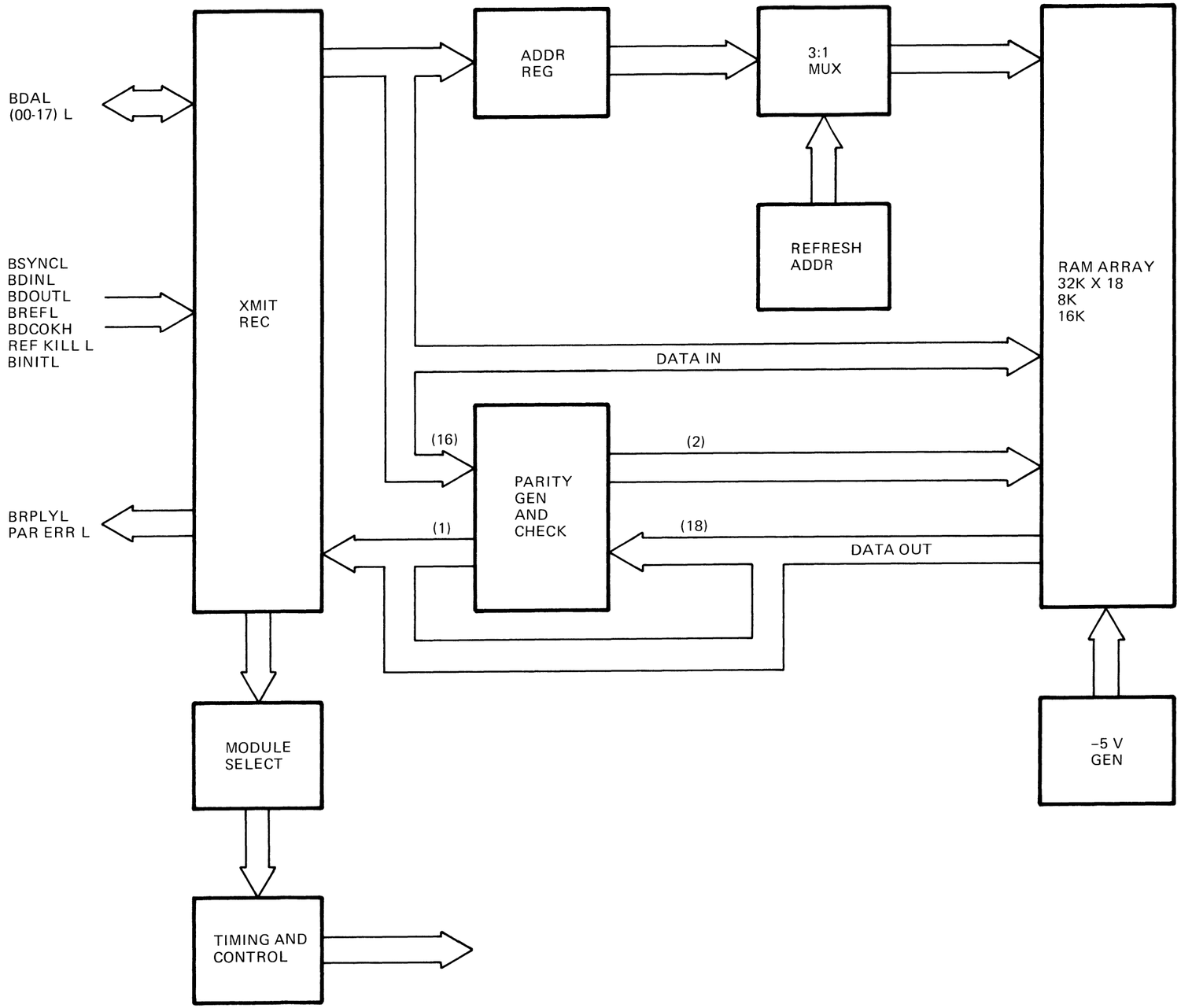


Figure 2-5. NS23P Block Diagram

2.3 DC POWER CIRCUITRY

DC voltage is brought in as +12 volts at input pin AD2 and BD2 as shown on sheet 1 of Figure A-1 (see Appendix A). Part of the +12 volt supply is run through a capacitive filter and directly to the memory array. A second part of the +12 volt supply is run through a dc to dc converter at IC location A11, where -5 volts is generated. This -5 volts is led out at pin BK1 where it is backplane-jumpered back in at pin BL1. Alternatively, a -5 volt source may be brought in directly at pin BL1 (no jumper). In either case, the -5 volts at BL1 is run directly to the memory array; it is used nowhere else.

A +5 volt source is brought in at pins AA2, BA2, and BV1, filtered, then run to both the memory array and the logic circuitry.

Provision has been made for battery backup power. If the system is so configured, the +12 volt input will be jumpered to the battery input at pin AS1, and the +5 volt jumpered to pin AV1. If battery power is used, the +5 volt battery supply is run only to that portion of the logic circuitry needed to maintain refresh (+5 volts is not required on the memory chip itself for data retention). For reference, those IC's that use the +5 volt battery source are indicated by a triangle at the IC gates on the schematic.

2.4 MEMORY ORGANIZATION

The standard memory capacity of the memory card is 32,768 words by 18 bits (32k x 18), which can be assigned in 4k increments anywhere within the LSI-11 128k word address space. Optional capacities are available from a minimum of 4,096 words by 16 bits (4k x 16) to the maximum of 32k x 18.

Also available as an option is switch-settable reserved I/O space such that 4k, 2k, 1k, or 512-word address locations in the upper portion of the address range can be reserved for device addresses.

2.5 DATA PATHS

This section consists of an expansion of the discussion of the read and write cycles in Section 2.2, as well as a detailed description of the read-modify-write cycle not described there. In this section, the schematic diagrams applicable to each operation will be used rather than the block diagram.

2.5.1 READ CYCLE/PARITY CHECK

As shown on sheet 6 of Figure A-1 in Appendix A, the data leaves the memory chips at pin 14 and is routed to two sources.

First, parity is checked (see Figure A-1, sheet 5). All of the data bits 0 through 15, including the parity bits, are brought into two 74S280 parity checkers (E7 and E8). Output pin 6 of E8, which is the parity check for the low byte on data bits 0 through 7, must always be high for the correct parity check to be performed. If an incorrect parity is developed in any of the data bits (including the parity bit), then this output will go low, signaling the parity error as a high output at pin 3 of gate F8. This high signal is the parity error signal that goes back to the driver and ultimately to the BDAL 16 line.

The data output from the memory elements also goes to IC's J4, J3, J2 and J1 (Figure A-1, sheet 4) running in the transmit mode, and to the bus via the BDAL 0 through 15 lines. If the parity error is active, it is input at (IC) J11 pin 14, and the output appears on the BDAL 16 line.

2.5.2 WRITE CYCLE/PARITY GENERATION

During a write cycle, data is brought in to the 8641 transmitter/receivers J4, J3, J2, and J1 on lines BDAL 0-17 from the bus. The receivers invert the data and distribute it to pin 2 of the memory array and to the parity generation circuits, IC's E5 and E6 (Figure A-1, sheet 4).

E5 develops the parity bit for the low-order byte and E6 the parity bit for the high-order byte. The BDAL 16 line, when set (active low), sets the input at E5-13 and E6-13 high and, in effect, writes parity opposite to that developed on each of the bytes individually for diagnositc check of the parity function.

Data may also be written as a byte. If BWTBT is issued low, the BLAL0 is interpreted as a byte select address. This signal, input at J4 pin 15, is output at pin 13 and run to F4 pin 13 (Figure A-1, sheet 3), where the output at pin 12 is latched with the leading edge of the SYNC signal. This term then runs to D11 pin 9 (Figure A-1, sheet 6), which in addition to gates D11 with output pins 3 and 11 form the write enable inputs to the memory array according to conditions established at the interface.

2.5.3 READ-MODIFY-WRITE

The read-modify-write cycle is a combination of a read cycle and a write cycle, differentiated from the individual functions only in its timing. While the memory treats the read-modify-write cycle as two internal cycles, to the processor or the external world, it is one cycle. The cycle timing will be discussed in greater detail in paragraph 2.6.1.4.

2.6 TIMING AND CONTROL

This section consists of a discussion of the timing and control involved in the external request, read, write, read-modify-write, and refresh cycles of the NS23P. Refer to the Timing and Control block diagram (Figure 2-6) for a more detailed breakdown of the timing and control section.

2.6.1 CYCLE TIMING

Except for an internal refresh cycle, timing and control are initiated through the external cycle flip-flop (Figure A-1, sheet 2, zone D4) H11 pins 8, 9, and 10, and the gates at pins 11, 12, and 13. Internal refresh control is provided by flip-flop J6

through output pins 9 and 8.

Row address select timing (TRAS) is provided by IC E10, a 74S74 D-type flip-flop with output pins 5 and 6. Column address select timing (TCAS) comes from IC E10, output pins 9 and 8.

The 74S10 IC gates F9 and H9 are the reply functions for read and write, and for refresh replay if active.

IC F11 controls a digital delay line for address timing. It is digital in that it accepts TTL signals as input and produces buffed TTL signals as output and requires no terminating resistors.

The discrete circuitry composed of a 100-ohm resistor, a 15pF capacitor and two 4.7k resistors in zone D5 smooths the output from the IC gate H9 pin 6. Its function is to allow the external flip-flop to be set and prevent fault settings of that flip-flop that may occur if a refresh request and external request are made coincidentally.

The arbitration circuitry for coincidental refresh and external requests is made up of gates H10 pins 12 and 13 and output pin 11, H10 pins 4, 5, and 6, a resistor-capacitor delay network made up of a 4.7k resistor and 10pF capacitor, and IC E9 pins 11, 12, and 13, and permits only one request to be honored at any time.

2.6.1.1 External Request

An external request is made on the external lines DIN or DOUT, run through a NOR gate at F6, and applied as an input at gate H9 pin 5. When H9 output pin 6 goes low, the external request flip-flop is set with H11 output pin 10 going low, and H10 output pin 3 going high. The H10 pin 3 output becomes input to the row address select flip-flop E10, which sets its output pin 5 high and begins the row select timing (TRAS) and the delay line at F11. At time T40, 40 ns after the row select has been initiated, output pins 11 and 6 of the row-column address multiplexer F8

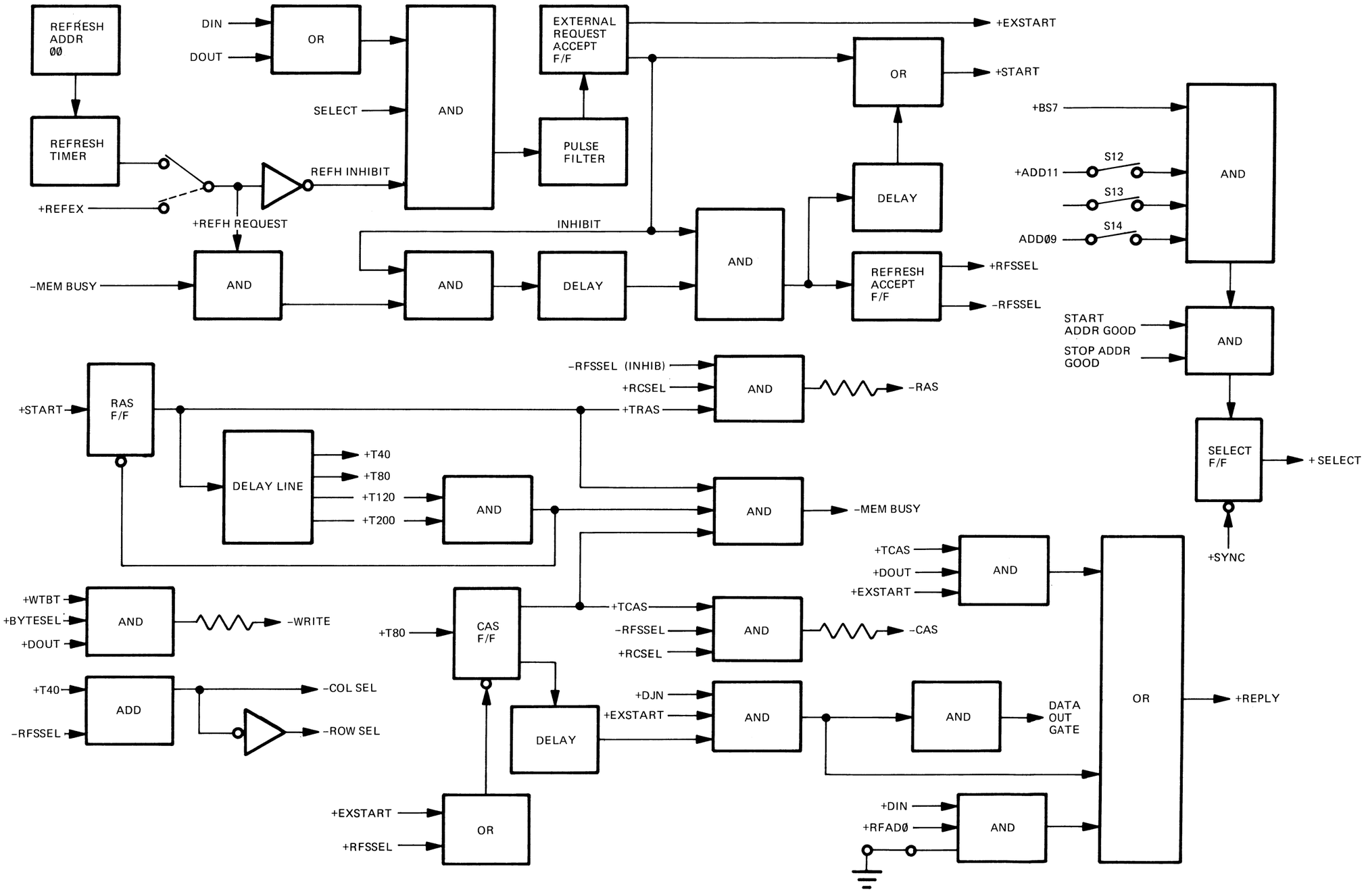


Figure 2-6. Block Diagram Timing and Control

deselect the row address and select the column address. At time T80 the clock input pin 11 of E10, the column select timing flip-flop, is set and begins the column address select term to the memory array (TCAS).

2.6.1.2 Read Cycle

In a read cycle, the output of the column address select flip-flip E10 pin 8 goes low. This sets F5 pin 5 low, output pin 6 high through a 100-ohm resistor 330pF capacitor delay, and inputs at IC F9 pin 1. This signal along with the DIN input signal at F9-2 sets the F9 output pin 12 to low which connects to F9 input pin 11. F9 output pin 8 goes high forming the reply term REPLY for the response of the memory to the DIN signal for a read cycle. Figure 2-7 shows the internal timing of these events.

2.6.1.3 Write Cycle

The timing for a write cycle is very similar to the read cycle, except that the column address select term (TCAS) is not used to produce reply. REPLY is generated by Nanding, + DOUT with + EXSTART, producing a low output at H9-12. The H9 pin 12 output is input at F9 pin 10 and output as the REPLY term for a write cycle. Figure 2-8 shows the internal timing of these events.

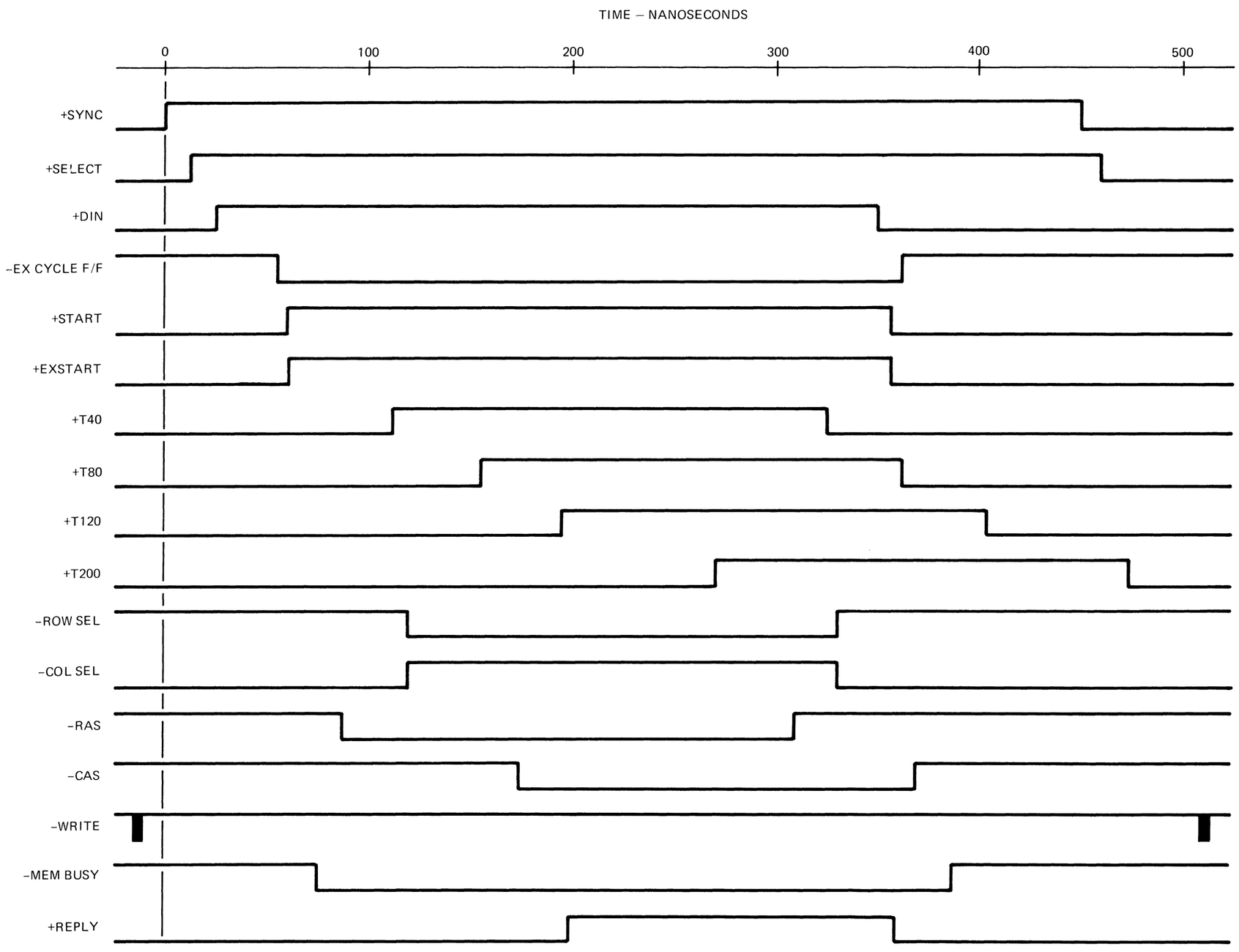
2.6.1.4 Read-Modify-Write

As mentioned in paragraph 2.5.3, the read-modify-write cycle is no more than a read cycle followed by a write cycle. Figure 2-9 shows the internal timing of this cycle.

2.6.1.5 Refresh Cycle

To begin a refresh cycle, the one-shot refresh timer J7 (Figure A-1, sheet 3, zone A7) times out with IC J7 output pin 10 set low. If the internal refresh jumper has been selected, that output runs to the input at gate J8 pin 11 and, if the refresh is not killed from the external world, J8 output pin 13 goes high, generating the refresh request signal REFRQ. Refer to figures 2-10 and 2-11 for the internal refresh and external refresh timing events, respectively.

The REFRQ signal is routed to three places (Figure A-1, sheet 2): J6 pin 13, J8 pin 2, and H8 pin 1. The incoming high signal at J6 pin 13 enables the refresh flip-flop clear input. J8 pin 2 sends J8 output pin 1 low, disabling any select inputs from the external world at gate H9 pin 3. When the high signal is presented at H8 pin 1 and the memory is not busy at pin 2, the output pin 3 goes high, which runs to input at H10 pin 12. If an external cycle is present or not being honored, as determined by H10 pin 13 being high, the H10 output pin 11 goes low, the H10 output pin 6 goes high, then is run through a 50 ns delay network composed of a 4.7k resistor and a 10pF capacitor. With a slow rising edge that forms at the delay, the signal is input at E9 pin 13 and, when the threshold is reached, E9 output pin 11 goes low and the output at F5 pin 8 goes high, clocking the refresh flip-flop J6 at its clock input pin 11. When J6 output pin 9 goes high and pin 8 goes low for the complement, indicating that a refresh cycle is being performed, the refresh select (RFSSEL) disables the row-column address multiplexer and enables the refresh address driver. An additional time delay is introduced through gate H8 pin 10 by a 4.7k resistor and 10pF capacitor network; this is then input to E9 pin 1, allowing time for those multiplexers to change state and set up the refresh address to the memory chip.



NOTE: THE MINIMUM TIMING IS SHOWN

Figure 2-7. Read Cycle (DATI) - Internal Timing Diagram

REVISIONS			
REV	DATE	ECO NO.	APPVD
B		SEE SHT 1	
C		SEE SHT 1	
D	—	ECO 2397	—
E	6-4-79	ECO 2866	RZ

A-U2 BDAL0 — 8641, J4 — BDAL0 15, I1 14, O1 13, I2 11, O2 10, I3 13, O3 3, I4 5, O4 6, DISB 7, DISA 9

A-V2 BDAL1 — 8641, J4 — BDAL1 12, I2 11, O2 10

B-E2 BDAL2 — 8641, J4 — BDAL2 1, I3 2, O3 3

B-F2 BDAL3 — 8641, J4 — BDAL3 4, I4 5, O4 6

B-H2 BDAL4 — 8641, J3 — BDAL4 12, I2 11, O2 10

B-J2 BDAL5 — 8641, J3 — BDAL5 15, I1 14, O1 13

B-K2 BDAL6 — 8641, J3 — BDAL6 1, I3 2, O3 3

B-L2 BDAL7 — 8641, J3 — BDAL7 4, I4 5, O4 6

B-M2 BDAL8 — 8641, J2 — BDAL8 12, I2 11, O2 10

B-N2 BDAL9 — 8641, J2 — BDAL9 15, I1 14, O1 13

B-P2 BDAL10 — 8641, J2 — BDAL10 1, I3 2, O3 3

B-R2 BDAL11 — 8641, J2 — BDAL11 4, I4 5, O4 6

B-S2 BDAL12 — 8641, J1 — BDAL12 12, I2 11, O2 10

B-T2 BDAL13 — 8641, J1 — BDAL13 15, I1 14, O1 13

B-U2 BDAL14 — 8641, J1 — BDAL14 1, I3 2, O3 3

B-V2 BDAL15 — 8641, J1 — BDAL15 4, I4 5, O4 6

+SELECT (3C1) 9, +DINDL (2A2) 10, F8 74S00, 8

A-C1 BDAL16 — 8641, J11 — BDAL16 15, B1 13, I1 14, C3 3, I3 2

A-D1 BDAL17 — 8641, J11 — BDAL17 1, B5, B2, B4, C2, I2, C4, I4

DISB 7, DISA 9

BYTE ADD (3D3)

+ADD0 (3D7) DTBIT0
+ADD1 (3C7) DTBIT1
+ADD2 (3C7) DTBIT2
+ADD3 (3C7) DTBIT3
+ADD4 (3C7) DTBIT4
+ADD5 (3C7) DTBIT5
+ADD6 (3C7) DTBIT6
+ADD7 (3C7) DTBIT7

(ADDRESS SHT 3) (DATA TO SHT 6)

74S280, E5: DTBIT0 4, DTBIT1 2, DTBIT2 1, DTBIT3 10, DTBIT4 11, DTBIT5 12, DTBIT6 13, DTBIT7 9, ΣEV 5, ΣOD 6, 8

DTPA0 SHT 6

DOBIT0 1, DOBIT1 2, DOBIT2 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, DOBIT14, DOBIT15

DATA OUT SHTS

(ADDRESS SHT 3) (DATA TO SHT 6)

+ADD7 (3C7) DTBIT8
+ADD8 (3C7) DTBIT9
+ADD9 (3D3) (3C7) DTBIT10
+ADD10 (3D3) (3C7) DTBIT11
+ADD11 (3D3) (3C7) DTBIT12
+ADD12 (3C3) DTBIT13
+ADD13 (3C3) DTBIT14
+ADD14 (3D3) DTBIT15
+ADD15 (3D3)
+ADD16 (3D3)
+WWP (+= WRITE WRONG PARITY) 8

74S280, E6: 1, 2, 4, 10, 11, 12, 13, 9, ΣEV 5, ΣOD 6, 8

DTPA1 SHT 6

+PARER (5C1)

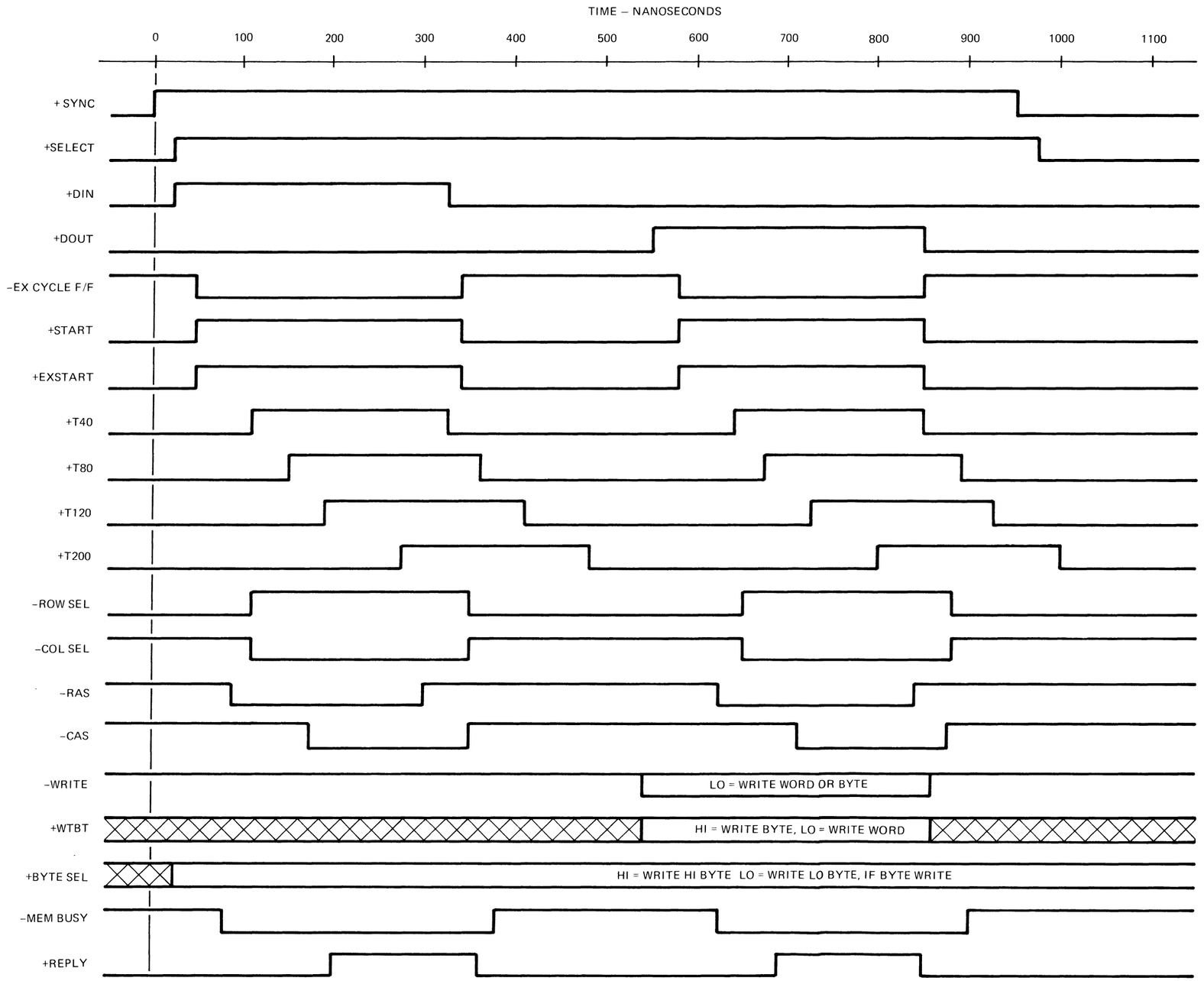
ADDR/DATA RECEIVER-DRIVERS
WRITE PARITY GEN

MATERIAL
FINISH
TOLERANCE ANG 2 PL 3 PL
NEXT ASSY USED ON
T.K. 7/26/78
UNLESS OTHER SPECIFIED

National Semiconductor Corporation
2900 Semiconductor Drive, Santa Clara, Calif. 95051

SCHEMATIC DIAGRAM
NS 23 P

SIZE D | DWG NO 8701103625 | 001
SCALE | SHEET 4 OF 6



NOTE: THE MINIMUM TIMING IS SHOWN

Figure 2-9. Read-Modify-Write Cycle (DATIO-B) - Internal Timing Diagram

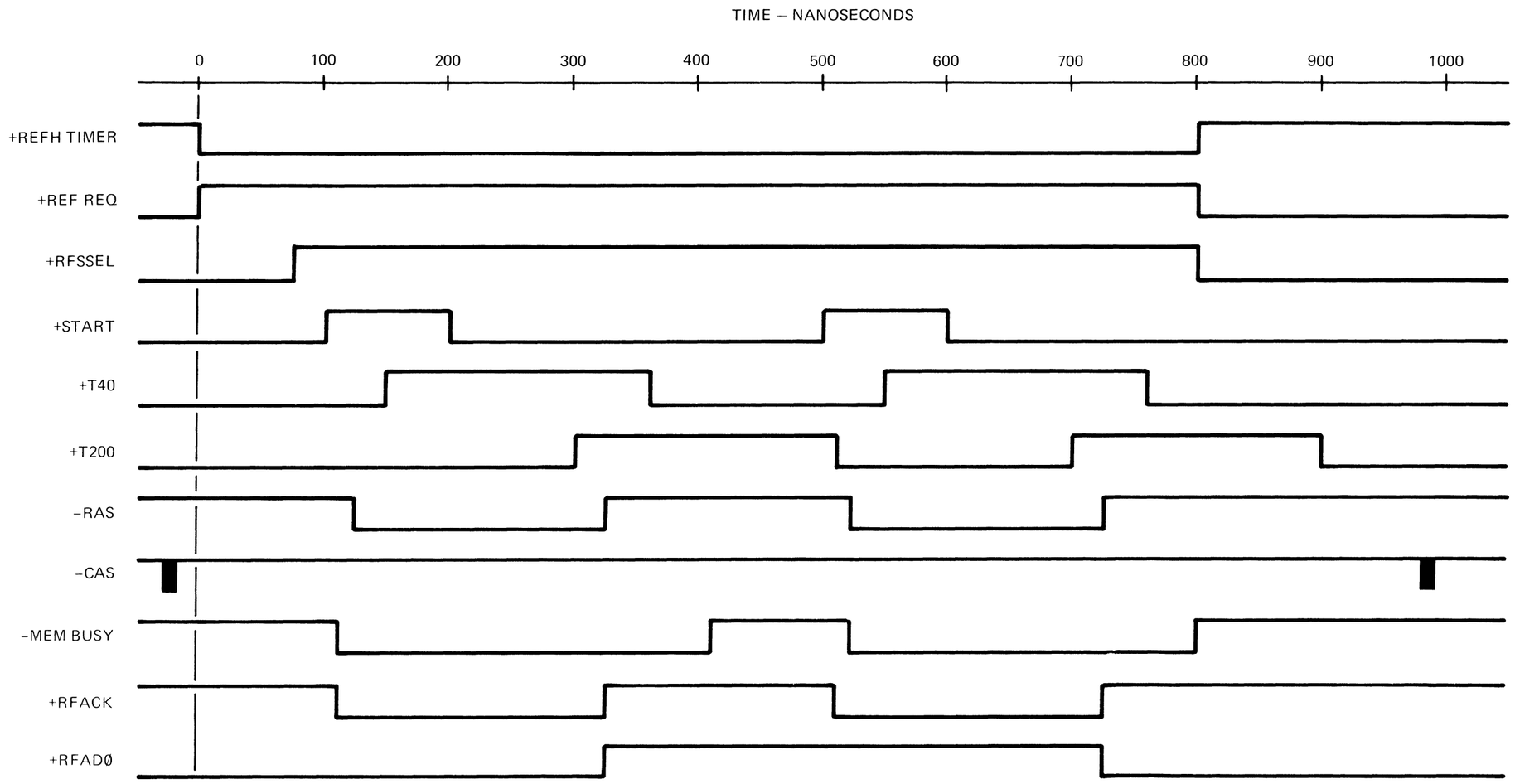
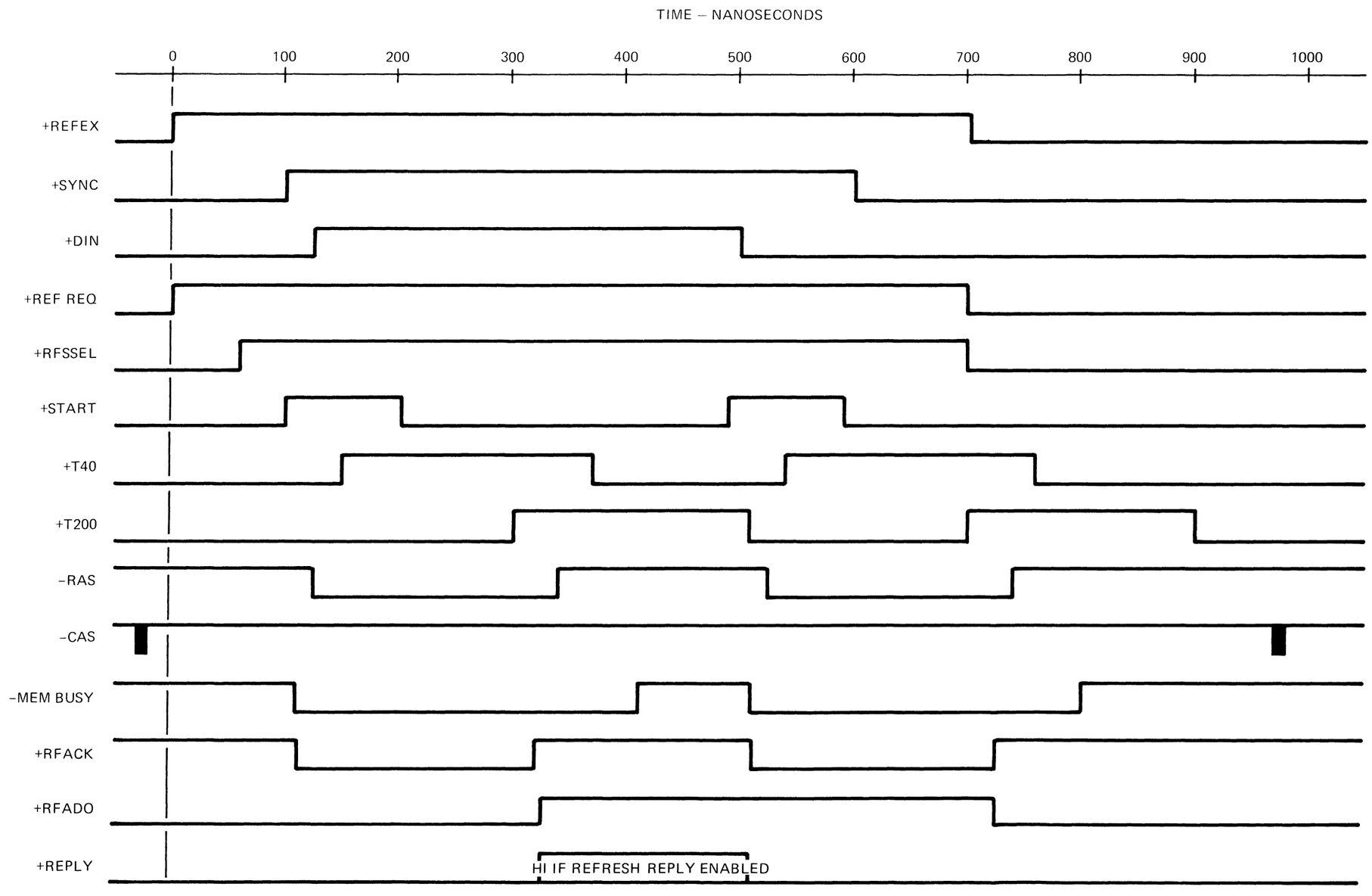


Figure 2-10. Internal Refresh Cycle



NOTE: THE MINIMUM TIMING IS SHOWN

Figure 2-11. External Refresh Cycle

When E9 pin 3 goes low, H10 pin 3 goes high, beginning the timing chain by setting the output of E10 pin 5 high to start the first refresh cycle. The TRAS flip-flop E10 output pin 5 going low, cleared by the timing terms input to E11 pins 4 and 5 and output E11 pin 6 going low, sending E10 pin 1 low, forms the refresh address clock at E9 pin 8. This rising edge changes the least significant refresh address, address 0, to memory. When -MEMBUSY becomes unbusy at H8 pin 2 going high, this again begins the second refresh timing edge, proceeding through gate H10 pin 11, E9 pin 11, H10 pin 8, E9 pin 3, then finally through H10 pin 3, and back to the RAS flip-flop E10 pin 3.

When the second refresh cycle has been completed, the 74S74 flip-flop J6 (Figure A-1, sheet 3, zone B8) output pin 6 goes high, that triggers the one-shot timer J7 pin 4, which forms a slight delay. Its output at pin 7 then triggers the one-shot time J7 at pin 12, and its output deselects the refresh request. When 15 microseconds elapse, the time constant for the IC J7, the dual refresh cycle begins again.

If jumper W4 (Figure A-1, sheet 3, zone A3) is closed for external refresh, the external request begins with the refresh request signal (+REFEX) input to gate H6 pin 1, which gets inverted to a low at gate H6 pin 3 then becomes +REFRQ at gate J8 pin 13, just as with the internal request.

2.6.2 RESERVED I/O

Under the standard card configuration, signal BS7 to the memory looks at the upper 4k, as I/O reserve; however, the user may gain more active read-write memory by switch-selecting only the upper 2k, 1k, or 512-words as peripheral or I/O reserve.

The reserved I/O switches are shown as S12-S14 at location F3, Figure A-1, sheet 3, zone B3. Closing the switches limits the I/O reserve by routing address terms AD011, ADD10, or ADD9 through the switches to gate F7 output pin 6 to form an additio-

nal arm of the module select term. The address terms ADD11, 10, and 9, as well as BS7 must be in their active state.

2.7 MEMORY ADDRESSING

Low order addressing is done by the three 74S373 IC's E1, E2, and F1 (Figure A-1, sheet 3, zone 6). Inputs to these IC's form the row and column addresses. External addresses are derived from the DAL01-14 lines; internally input signals to E1 ADD0-5 and AP12 become the row address, and input signals to E2 ADD 6-11 and AP13 become the column address. Refresh addressing is performed by IC F1, as a driver, in conjunction with H7, the address counter, and is done entirely internally.

IC's E1, E2, and F1 have their outputs paralleled to function as a tri-state driver, and are time-multiplexed to switch in and out as needed. When an external cycle is performed, the row select term that is input active low to E1 pin 1, causes the outputs of E1 to be enabled; the outputs of E2 and F1 are disabled and the row address is driven to memory. When the column address is issued active low to E2 pin 1, the inputs to E1 and F1 remain high, and the column address is sent to the memory array. Similarly, at refresh time, -RFSSEL sends pin 1 of F1 low, and E1 and E2 turn off. The outputs A0-A6 are run through 33 ohm series resistors to damp out any oscillation that might occur in signal transitions to the array.

IC's E1 and E2, in addition to being multiplexed drivers, are also the row-column latch for external address. The latch term is the G input at E1 pin 11, and is derived from the bus sync signal (BSYNC). The output of the refresh driver F1 is not latched; it is enabled only at pin 1 by the output of the refresh select flip-flop J6 pin 8.

Refresh address counter H7 provides five of the six address terms driven to memory. The sixth term, refresh address (RFAD0), the least significant address, comes from D-type

flip-flop J6 pin 6. J6 pin 6 toggles from its high state to its low state, addressing once when RFAD0 is low and once when RFAD0 is high, thus providing the dual refresh (whether refresh is internal or external). The clock input to J6 pin 3 is the control signal +RFACK generated in the timing control system. J6 is enabled at pin 1 by +RFSSEL, which is active high when refresh is enabled. When the memory is not performing a refresh, +RFSSEL goes low and clears J6, placing the output at pin 5 low. Refresh counter H7 is also clocked at pin 1 by J6 output pin 5.

The higher order address terms are sent to IC's H3, H4, H5 pin 10, and H5 pin 5. H3, a 74LS283 4-bit full adder, in conjunction with H5, a 74S08 with input pins 4, 5, and output pin 6, and H6, a 74S86, pins 4, 5, and output pin 6, form a 5-bit binary adder and produce the start address control term of the output of H3 pin 9 (upper right hand quadrant of Figure A-1, sheet 3). This term, run through switch S11 to IC F7 pin 10, selects and determines whether the address term presented to it on the bus is above or equal to the selected address toggled into switches S1-S5 at E3.

IC H4, in conjunction with H5 pin 9, 10, and 8, forms a 5-bit adder that performs the stop address function by comparing the external address with the address set in E3 switches S6-S10. The output of H4 pin 9 is the carry term which, when active high, sends H6 pin 8 and F7 pin 12, active low, and determines that the external address is outside the selected range. Similarly, the output of H3 pin 9, when switch S11 is activated, sets F7 pin 10 high and determines that the external address is within the selected range.

If the external address is within the selected range, if refresh is not being initiated, if the dc power is on, and if the bank select has not been asserted, then F7 output pin 8 goes low and J8 output pin 4 sends a high signal to input pin 14 of F4, the select latch, which sends its output pin 15 high forming the

signal +SELECT and allowing the memory to perform an external cycle.

SECTION 3

INSTALLATION

This section contains the basic information for installing the NS23P memory card.

3.1 TOOLS REQUIRED

A ball-point pen or small stylus may be needed to set the switches mounted on the memory card. Otherwise, no special tools are required for installation.

3.2 UNPACKING AND INSPECTION

The memory card should be unpacked with care and examined for physical shipping damage (i.e., broken, bent or dented parts).

NOTE

If physical damage is apparent, do not attempt to install or operate the memory card.

3.3 CONFIGURATION

The NS23P card has a switch selectable option for the address range to which the memory responds and a switch selectable option for the I/O reserve address range to which the memory does not respond.

3.3.1 ADDRESS RANGE SELECTION (EXAMPLE)

Set switches S1-S5 and S11 for the desired start address; set switches S6-S10 for the desired stop address. The location of the switches is illustrated in Figure 3-1; settings are listed in Table 3-1.

For example, to install the NS23P 16k memory card within the address range of 4k to 20k. The start address is 4k $(20,000)_8$ and the stop address is 20k $(117,776)_8$. Set switches as follows:

Start-4k		Stop=20k	
S1	OFF	S6	OFF
S2	OFF	S7	OFF
S3	OFF	S8	ON
S4	OFF	S9	OFF
S11	ON	S10	OFF

3.3.2 RESERVING I/O SPACE

The upper portion of system address is reserved for peripheral devices, normally for the uppermost 4k bank. The NS23P has the capacity to reduce this space to 2k, 1k or 512 words according to switches S12, S13, and S14. The switches should be set as follows:

S12	S13	S14	Reserved I/O Space (Words)
OFF	OFF	OFF	4k
ON	OFF	OFF	2k
ON	ON	OFF	1k
ON	ON	ON	512

The locations of the switches are shown in Figure 3-1.

3.3.3 ADDITIONAL CONFIGURATION JUMPERS

The NS23P also has factory settable jumpers for the following options: 16k/8k RAMs, internal/external refresh, external refresh RPLY active/inactive, and battery back-up active/inactive. Locations of these jumpers are shown in Figure 3-1. Definitions of jumper installation/removal are shown in Table 3-2.

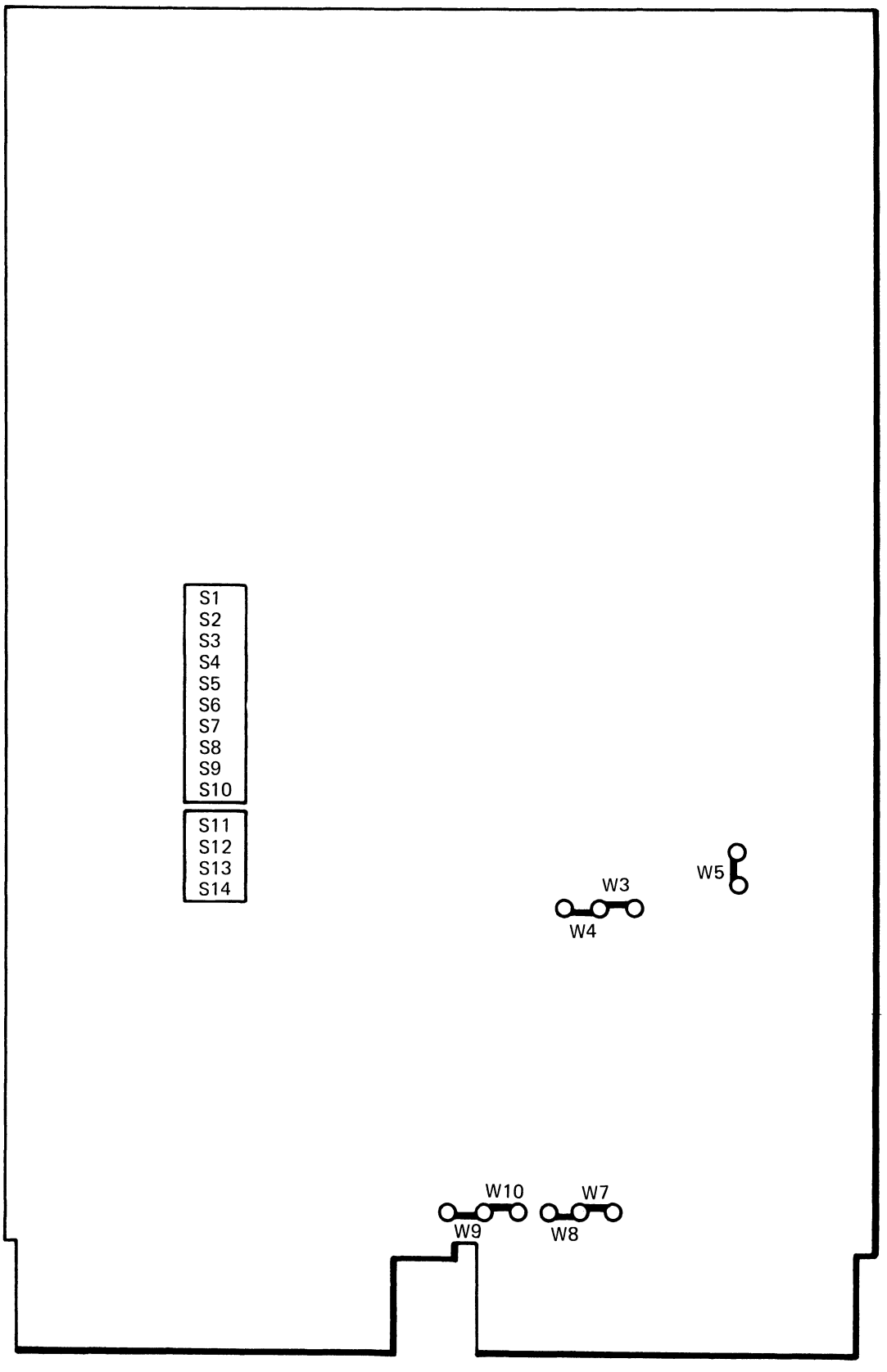


Figure 3-1. Switch and Jumper Locations

Table 3-1. Address Range Switch Programming

ABSOLUTE ADDRESS	S5 S10	S4 S9	S3 S8	S2 S7	S1 S6	S11 -	START STOP
0k	1	1	1	1	1	0	
4k	0	0	0	0	0	1	
8k	1	0	0	0	0	1	
12k	0	1	0	0	0	1	
16k	1	1	0	0	0	1	
20k	0	0	1	0	0	1	
24k	1	0	1	0	0	1	
28k	0	1	1	0	0	1	
32k	1	1	1	0	0	1	
36k	0	0	0	1	0	1	
40k	1	0	0	1	0	1	
44k	0	1	0	1	0	1	
48k	1	1	0	1	0	1	
52k	0	0	1	1	1	1	
56k	1	0	1	1	0	1	
60k	0	1	1	1	0	1	
64k	1	1	1	1	0	1	
68k	0	0	0	0	1	1	
72k	1	0	0	0	1	1	
76k	0	1	0	0	1	1	
80k	1	1	0	0	1	1	
84k	0	0	1	0	1	1	
88k	1	0	1	0	1	1	
92k	0	1	1	0	1	1	
96k	1	1	1	0	1	1	
100k	0	0	0	1	1	1	
104k	1	0	0	1	1	1	
108k	0	1	0	1	1	1	
112k	1	1	0	1	1	1	
116k	0	0	1	1	1	1	
120k	1	0	1	1	1	1	
124k	0	1	1	1	1	1	
128k	1	1	1	1	1	1	

1 = Switch CLOSED
0 = Switch OPEN

3.4 INSTALLATION

The memory card is placed into the backplane's connector slots A and B, or into connector slots C and D; in both cases, as close to the CPU as possible. The memory card's components should face row 1. Positions of components and connector slots are shown in Figure 3-2.

The following precautions should be observed during installation:

- Turn off memory power before installing or removing the memory card to avoid damage.
- Do not attempt to insert the memory card into slot one on the backplanes. Slot one is reserved for the LSI-11 processor on both backplanes.
- If the DDV11-B expanded backplane is being used, insert the memory card into the AB connectors of the backplane.
- The REV11 DMA refresh must be the highest priority DMA device on the bus when this option is being used. If not, refresh may not operate properly and loss of memory data may occur.
- When systems with expansion boxes are being used in addition to the REV11 DMA refresh board, install a REV11-C board (no termination resistors) into row 2A & B (the highest priority row), then install a TEV11 termination board in the last row of the bus.

3.5 VERIFICATION

After the NS23P memory card has been installed, apply memory power and verify operation by running system diagnostics to test the memory.

Table 3-2. Option Jumpers

Jumper	Status	Function
W3 W4	I R	Internally controlled on-board Refresh
W3 W4	R I	Externally controlled Refresh
W5 W6	I R	Refresh reply disabled for Externally controlled Refresh.
W5 W6	R I	Refresh reply enabled for Externally controlled Refresh.
W7 W8	I R	Configuration for +5V power For non-battery Back-up System.
W7 W8	R I	Configuration for +5V power For battery back-up systems.
W9 W10	I R	Configuration for +12V power For non-battery back-up systems.
W9 W10	R I	Configuration for +12V power For battery back-up systems.

Note: See assembly drawings sheet 2, and Table 3-2A below, for jumper locations and information.

I = Install

R = Remove

Table 3-2A. Option Jumpers

W3	=	J to K
W4	=	H to J
W5	=	M to N
W7	=	E to F
W8	=	D to E
W9	=	A to B
W10	=	B to C

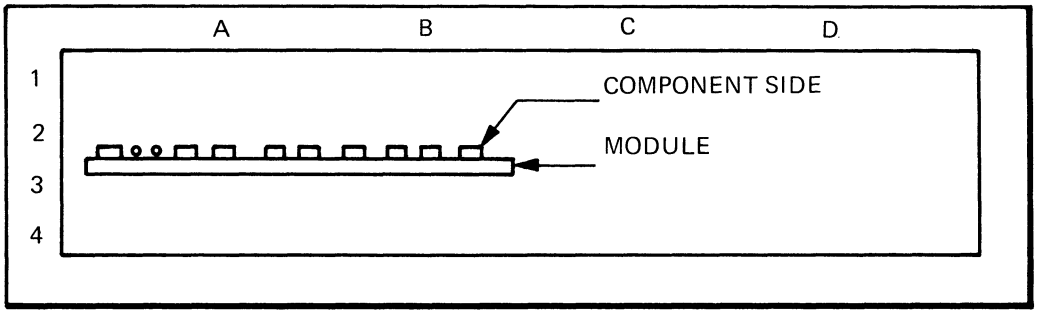


Figure 3-2. Module Installation

- (TBD)
- MOS/CORE memory exercizer for 0 to 124k with or without parity bits.

SECTION 4

MAINTENANCE AND TROUBLESHOOTING

4.1 MAINTENANCE

The NS23P memory card does not require routinely scheduled maintenance checks. However, systems diagnostics for both the NS23P memory card and the LSI-11 Microcomputer System should be performed occasionally to verify correct operation.

4.2 TROUBLESHOOTING

If problems occur, check the following:

- Are the address range switches and the I/O reserve switches set properly?
- Are the option jumpers installed/removed for the appropriate features?
- Are all power supplies turned on? Make sure that +5V and +12V power is applied to the backplane.
- Has the DMA priority daisy chain been maintained? Verify that there are no empty slots between the first and last board.
- Are the system cables installed correctly? Check that the cables are connected at both ends.

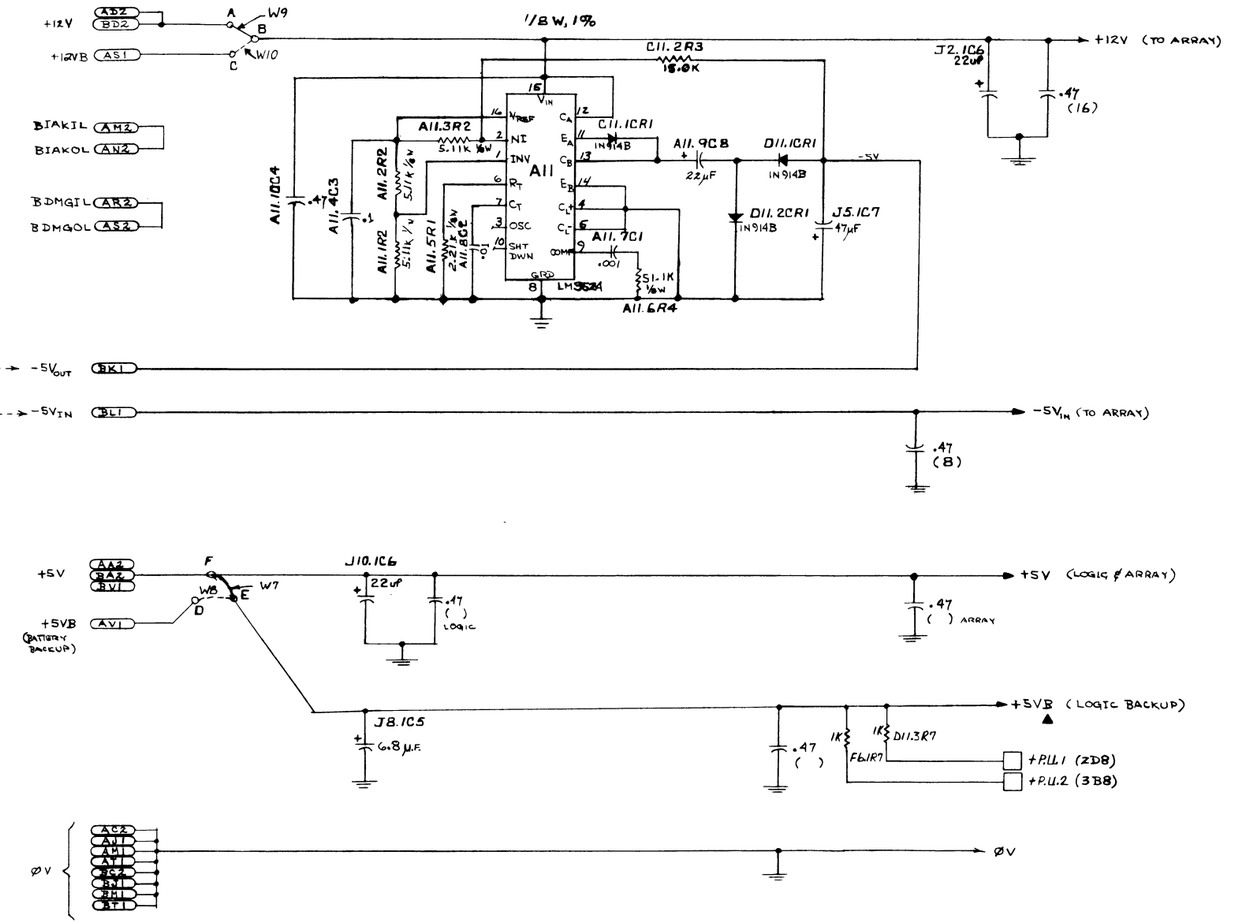
Appendix A

Reference Drawings

This appendix contains the required reference schematic and assembly drawings for the NS23P memory.

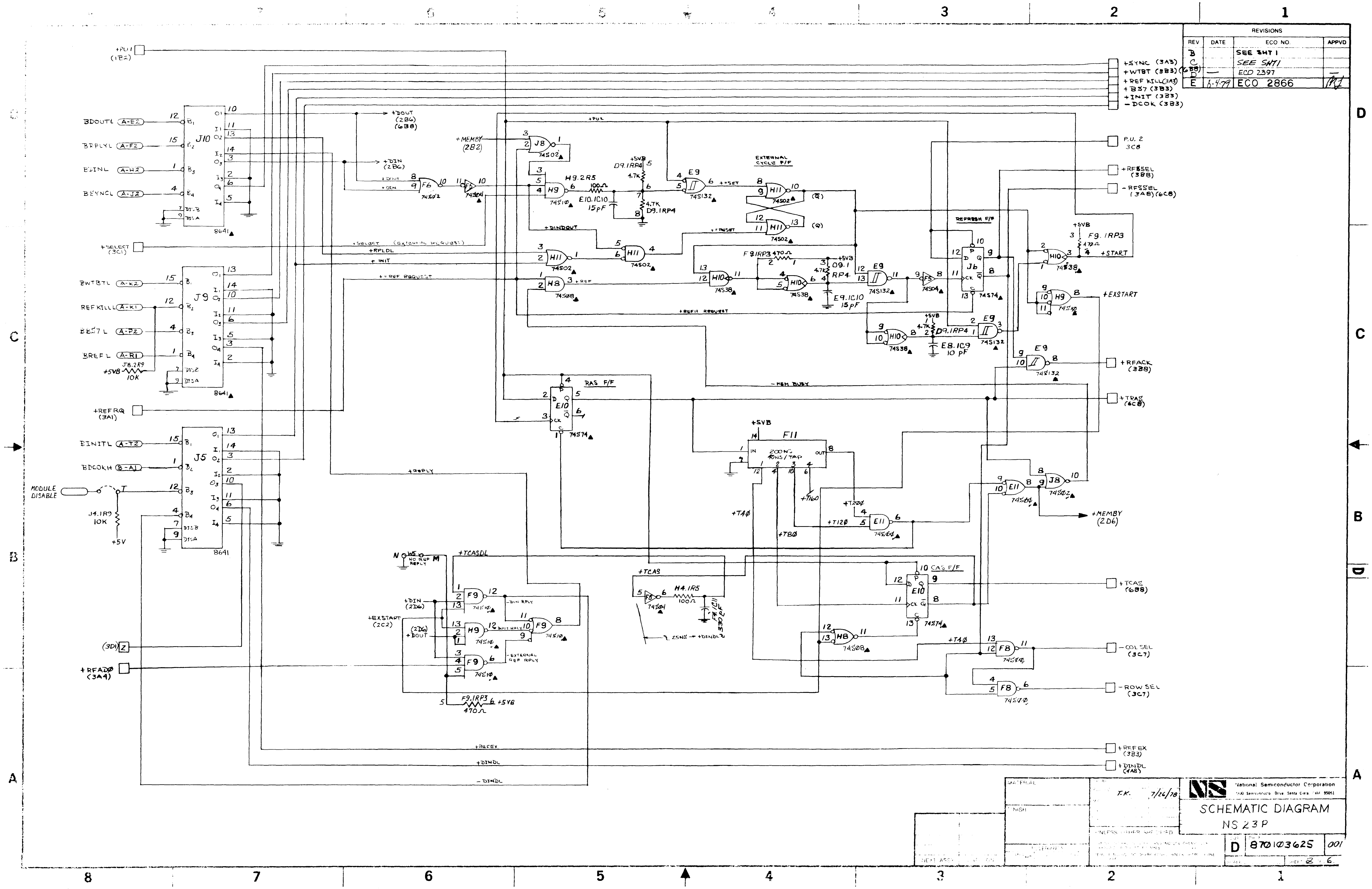
Figure A-1	870103625-001	Schematic
Figure A-2	980103625-000	Assembly

REVISIONS			
REV	DATE	ECO NO.	APPVD
A	9-15-8	PDD 2654	
B	11-10-8	PDD 3054 RA	
C	3-2-79	PDD 3386 [illegible]	
D	3-19-79	ECD 2397, ECO REL.	
E	6-4-79	ECO 2866	



NOTES: 1. ▲ DENOTES POWER DERIVED FROM +5VB.
2. ALL DESCRETE RESISTORS ARE 1/8W.
(UNLESS OTHERWISE SPECIFIED)

MATERIAL		DR BY SGO 6-13-78	National Semiconductor Corporation, 2900 Semiconductor Drive, Santa Clara, Calif. 95051
FINISH		CHK BY T.K. 7-26-78	SCHEMATIC DIAGRAM NS 23 P
TOLERANCE: ANG ± 2 PL ± 3 PL		APP'D 11-10-8	UNLESS OTHER SPECIFIED: DIMENSIONS ARE IN INCHES AND SECTION DIMENSIONS ARE TO BE COMPLETED AFTER PLATING. REMOVE BURRS AND SHARP EDGES. BREAK CORNERS .015 MAX.
NEXT ASSY	USED ON		SIZE D; DR NO 8701Ø3625 001; SCALE; SHEET 2 OF 6


REVISIONS
REV | DATE | ECO NO. | APPVD
B | | SEE SHT 1 |
C | | SEE SHT1 |
D | — | ECO 2397 |
E | 6-4-79 | ECO 2866 |
+SYNC (3A3)
+WTBT (3B3)
+REF KILL (3A3)
+BS7 (3B3)
+INIT (3B3)
-DCOK (3B3)
+PU1 (1B2)
BDOUTL (A-E2)
BRPLYL (A-F2)
BDINL (A-H2)
BSYNCL (A-J2)
J10
8641
+DOUT (2B6) (6B8)
+DIN (2B6)
+MEMBY (2B2)
J8 74S02
H9 74S10
H9.2R5 100Ω
E10.1C10 15pF
D9.1RP4 4.7K
E9 74S132
+SET
EXTERNAL CYCLE F/F
H11 74S02
+RESET
+SELECT (3C1)
BWTBTL (A-K2)
REF KILLL (A-K1)
BBS7L (A-P2)
BREFL (A-R1)
+5VB J8.2R9 10K
J9
8641
+REFRQ (3A1)
BINITL (A-T2)
BDCOKH (B-A1)
MODULE DISABLE
J4.1R9 10K
+5V
J5
8641
RAS F/F
E10 74S74
+DIN DOUT
+RPLDL
+INIT
+REF REQUEST
H8 74S08
+REFR REQUEST
F9.1RP3 470Ω
D9.1RP4
E9.1C10 15pF
H10 74S38
F5 74S04
REFRESH F/F
J6 74S74
F9.1RP3 470Ω
+START
+EXSTART
E8.1C9 10 pF
+MEM BUSY
P.U. 2 3C8
+RFSSEL (3B8)
-RFSSEL (3A8)(6C8)
+RFACK (3B8)
+TRAS (6C8)
F11
200NS 40NS/TAP
+T40
+T80
+T120
+T160
+T200
E11 74S00
+MEMBY (2D6)
+TCASDL
NO REF REPLY
+DIN (2D6)
+EXSTART (2C2)
+DOUT (2D6)
F9 74S10
-DIN RPLY
DOUT RPLY
-EXTERNAL REF RPLY
(3D1)
+RFADØ (3A4)
F9.1RP3 470Ω +5VB
+TCAS
H4.1R5 100Ω
F8/C11 330pF
+DINDL
CAS F/F
E10 74S74
+TCAS (6B8)
-COL SEL (3C7)
-ROW SEL (3C7)
F8 74S00
+REFEX
+REFEX (3B3)
+DINDL (4A8)
-DINDL
National Semiconductor Corporation
T.K. 7/26/78
SCHEMATIC DIAGRAM
NS23P
D 870103625 001

REVISIONS			
REV	DATE	ECO NO	APPVD
B		SEE SHT 1	
C		SEE SHT 1	
D	—	ECO 2397	—
E	6-77	ECO 2866	

T.K.	7/26/78

SCHEMATIC DIAGRAM
NS 23P

87010625 001

3 6

NOTES: 1. S1-S5 = START ADDR.
2. S6-S12 = STOP ADDR.
3. S11-S13 = I/O SPACE RESERVE.
4. S14 = INTERNAL/EXTERNAL REFR. SELECT.

REVISIONS			
REV	DATE	ECO NO.	APPVD
B		SEE SHT 1	
C		SEE SHT 1	
D	—	ECO 2397	—
E	6-4-79	ECO 2866	

8641, J4
BDAL0 (A-U1) 15 B1
BDAL1 (A-V2) 12 B2
BDAL2 (B-E2) 1 B3
BDAL3 (B-F2) 4 B4
7 DISB
DISA 9
O1 13, I1 14, O2 10, I2 11, O3 3, I3 2, O4 6, I4 5

8641, J3
BDAL4 (B-N2) 12 B2
BDAL5 (B-J2) 15 B1
BDAL6 (B-K2) 1 B3
BDAL7 (B-L2) 4 B4
7 DISB
DISA 9
O2 10, I2 11, O1 13, I1 14, O3 3, I3 2, O4 6, I4 5

8641, J2
BDAL8 (B-N2) 12 B2
BDAL9 (B-N2) 15 B1
BDAL10 (B-P2) 1 B3
BDAL11 (B-R2) 4 B4
7 DISB
DISA 9
O2 10, I2 11, O1 13, I1 14, O3 3, I3 2, O4 6, I4 5

8641, J1
BDAL12 (B-S2) 12 B2
BDAL13 (B-T2) 15 B1
BDAL14 (B-U2) 1 B3
BDAL15 (B-V2) 4 B4
7 DISB
DISA 9
O2 10, I2 11, O1 13, I1 14, O3 3, I3 2, O4 6, I4 5

+SELECT (3C1) 9
+DINDL (2A2) 10
F8 74S20, 8

8641, J11
BDAL16 (A-C1) 15 B1
BDALIY (A-D1) 1 B5
B2, B4, 7 DISB, DISA 9
O1 13, I1 14, O3 3, I3 2, C2, I2, C4, I4

BYTE ADD (3D3)

ADDRESS SHT3 (3C7):
+ADD0 (3D7)
+ADD1 (3C7)
+ADD2 (3C7)
+ADD3 (3C7)
+ADD4 (3C7)
+ADD5 (3C7)
+ADD6 (3C7)

DATA TO SHT 6:
DTBIT0
DTBIT1
DTBIT2
DTBIT3
DTBIT4
DTBIT5
DTBIT6
DTBIT7

74S280, E5
4, 2, 1, 10, 11, 12, 13, 9, 8
Σ EV 5
Σ OD 6
DTPA0 SHT 6

DOBIT0
DOBIT1
DOBIT2
3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13
DOBIT 14
DOBIT 15
DATA OUT SHTS

ADDRESS SHT3 (3C7):
+ADD7 (3C7)
+ADD8 (3C7)
+ADD9 (3D3) (3C7)
+ADD10 (3D3) (3C7)
+ADD11 (3D3) (3C7)
+ADD12 (3C3)
+ADD13 (3C3)
+ADD14 (3D3)
+ADD15 (3D3)
+ADD16 (3D3)

DATA TO SHT 6:
DTBIT8
DTBIT9
DTBIT10
DTBIT11
DTBIT12
DTBIT13
DTBIT14
DTBIT15

+WWP (+= WRITE WRONG PARITY)

74S280, E6
1, 2, 4, 10, 11, 12, 13, 9, 8
Σ EV 5
Σ OD 6
DTPA1 SHT 6

+PARER (5C4)

ADDR/DATA RECEIVER-DRIVERS
WRITE PARITY GEN

MATERIAL		T.K. 7/26/78	National Semiconductor Corporation, 2900 Semiconductor Drive, Santa Clara, Calif. 95051
FINISH			SCHEMATIC DIAGRAM NS 23 P
TOLERANCE		UNLESS OTHER SPECIFIED	SIZE D, DR NO. 8701103625 001
NEXT ASSY	USED ON		SCALE —, SHEET 4 OF 6

REVISIONS			
REV	DATE	ECO NO.	APPVD
B		SEE SHT 1	
C	——	SEE SHT 1	
D	——	ECO 2397	
E	6-4-79	ECO 2866	

DATA FROM SHT 6

DOBIT 0
1
2
3
4
5
6
DOBIT 7
DOPA 0
DOBIT 8
9
10
11
12
13
14
DOBIT 15
DOPA 1

74S280
E8
Σ_{EV} 5
Σ_{OD} 6
A 4
B 2
C 1
D 9
E 10
F 11
G 12
H 13
I 8

74S280
E7
Σ_{EV} 5
Σ_{OD} 6
A 4
B 12
C 1
D 2
E 9
F 10
G 11
H 13
I 8

−PER
−PER
F8
74S00
3 = ERROR
+PARER (4AS)

DOBIT 0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
DOBIT 15

DATA OUT SHT 4

READ DATA REGISTER
READ PARITY CHECK

MATERIAL		DR BY	
FINISH		CHK BY T.K. 7/26/78	National Semiconductor Corporation, 2900 Semiconductor Drive, Santa Clara, Calif. 95051
TOLERANCE ANG ± 2 PL ± 3 PL		UNLESS OTHER SPECIFIED DIMENSIONS ARE IN INCHES AND TO BE CHEMICALLY BLACKENED TIN PLATED FINISHES REMOVE BURRS AND SHARP EDGES BREAK SHARP CORNERS .001 MAX	SCHEMATIC DIAGRAM NS 23 P
NEXT ASSY	USED ON		SIZE D DR NO 87010362S 001
			SCALE SHEET 5 OF 6

REVISIONS			
REV	DATE	ECO NO	
B		SEE SHT 1	
C		SEE SHT 1	
D		ECO 2397	
E	6-4-79	ECO 2866	MR

TYP MEM CHIP
48210259B

-5V, +12V, +5V, ØV

DO BIT 0 … DO BIT 7, DO PA 0, DO BIT 8 … DO BIT 15, DO PA 1 — DATA FROM SHT 5

A Ø, A 1, A 2, A 3, A 4, A 5, A 6 — ROW-COL ADDRESS SHT 3

1ST K/8K

2N016/8K

(NOTE: MEM ARRAY CHIP ADDR A5 IS EXTERNAL ADDR A6 AND CHIP ADDR A6 IS EXTERNAL ADDR A5).

DTPA 1, DTBIT/5 … DTBIT 8, DTPA 0, DTBIT 7 … DTBIT Ø — DATA TO SHT 4

+TRAS (2B2)
RC SEL (2D4)
-RFS SEL (2D2)
+TCAS (2B2)
+WRT (2D2)
+BYTE SEL (2C1)
+DOUT (2D6)

74S00, 74S37, C9.2RPI 33Ω, C9.1RPI 33Ω

BYTE Ø, BYTE 1

RAS, CAS AND WE DRIVERS
RAM ARRAY

MATERIAL		T.K. 7/26/78	National Semiconductor Corporation, 2900 Semiconductor Drive, Santa Clara, Calif. 95051
FINISH		9-15-8	SCHEMATIC DIAGRAM NS 23P
TOLERANCE UNLESS OTHER SPECIFIED	NEXT ASSY	USED ON	SIZE D, DWG NO 8701Ø3625, 004, SCALE, SHEET 6 OF 6

⑤	TABULATED DATA
VERSION	REMARKS
-001	32K X 18 16K CHIP (PARITY)
-002	32K X 16 16K CHIP (NON-PARITY)
-101	16K X 18 16K CHIP (PARITY)
-102	16K X 16 16K CHIP (NON-PARITY)
-111	16K X 18 8K CHIP PR (PARITY)
-112	16K X 16 8K CHIP PR (NON-PARITY)
-121	16K X 18 8K CHIP PL (PARITY)
-122	16K X 16 8K CHIP PL (NON-PARITY)
-211	8K X 18 8K CHIP PR (PARITY)
-212	8K X 16 8K CHIP PR (NON-PARITY)
-221	8K X 18 8K CHIP PL (PARITY)
-222	8K X 16 8K CHIP PL (NON-PARITY)

⑦ MEMORY ELEMENT PART NO & POPULATION CHART			
VERSION	QTY	MEM. ELEMENT P/N	POPULATED LOCATIONS
-001	36	48210 2598-022	AI-9, BI-9, CI-9, DI-9.
-002	32	2598-022	AI-8, BI-8, CI-8, DI-8.
-101	18	2598-022	AI-9, BI-9.
-102	16	2598-022	AI-8, BI-8.
-111	36	2989-112	AI-9, BI-9, CI-9, DI-9.
-112	32	2989-112	AI-8, BI-8, CI-8, DI-8.
-121	36	3060-112	AI-9, BI-9, CI-9, DI-9.
-122	32	3060-112	AI-8, BI-8, CI-8, DI-8.
-211	18	2989-112	AI-9, BI-9.
-212	16	2989-112	AI-8, BI-8.
-221	18	3060-112	AI-9, BI-9
-222	16	48210 3060-112	AI-8, BI-8

⑧⑫ FACTORY INSTALLED JUMPERS			
VERSION	INSTALLED	REMOVED	REMARKS
-001, 002 -101, 102	W11, 17, 18.	W12, 13, 14. W15, 16, 19.	16K MEM CHIP
-111, -112 -211, -212	W13, 16, 19.	W11, 12, 14. W15, 17, 18.	8K PR CHIP
-121, -122 -221, -222	W12, 16, 19.	W11, 13, 14. W15, 17, 18.	8K PL CHIP

MARKETING CONFIGURATION CODE	⑩⑪⑫ REFERENCE ONLY USER SELECTABLE OPTION JUMPERS		
	INSTALLED	REMOVED	REMARKS
0AA	W3	W4	INTERNAL REFRESH
1AA	W4	W3	EXTERNAL REFRESH
A0A	W5	—	DISABLE REFRESH REPLY
A1A	—	W5	ENABLE REFRESH REPLY
AA0	W7 W9	W8 W10	NO BATTERY BACKUP
AA1	W8 W10	W7 W9	BATTERY BACKUP IMPLEMENTED

EXAMPLE: MCC-001
- BATTERY BACK UP
- DISABLE REFRESH REPLY
- INTERNAL REFRESH

REFERENCE ONLY-SEE MCC TABLE FOR THE JUMPERS TO BE INSTALLED			
⑪⑫ JUMPER LOCATION CHART			
JUMPER DESIG.	FROM	TO	
W3	J	K	⑬
W4	H	J	⑬
W5	M	N	
W7	E	F	
W8	D	E	
W9	A	B	
W10	B	C	

REVISIONS			
REV	DATE	ECO NO.	APPVD
A	11-10-78	PDD 2654	
B	11-10-78	PDD 3054RA ETCH 1 REWORK, CREATE ETCH 2	
C	3-2-79	PDD 3386 REWORK CREATE ETCH 3	
D	3-19-79	ECO 2397 ECO REL.	
E	6-4-79	ECO 2866	

NOTES:
1. ASSEMBLE AND SOLDER PER NSC SPEC. 429101895.
2. MARK ASSY. DASH NO. WITH .12-.18 HIGH CHARACTERS WHERE SHOWN.
3. DELETED.
4. REFERENCE DESIGNATION NOT USED: W1, W2, W6.
5. MARK ASSY WITH REV LEVEL USING .12 — .18 CHARACTERS WHERE SHOWN.
6. MARK S/N WITH .12-.18 HIGH CHARACTERS WHERE SHOWN.
7. INSTALL MEMORY IC'S ACCORDING TO THE MEMORY ELEMENT POPULATION CHART.
8. INSTALL JUMPERS ACCORDING TO THE FACTORY INSTALLED JUMPERS TABLE.
9. VERSION NUMBERS ARE ESTABLISHED TO THE FOLLOWING CODE: -XYZ

X = CAPACITY	Y = MEM CHIP 16K/8K PL/R	Z = PARITY / NON-PARITY
X=0 32K	Y=0 16K	Z=1 PARITY
X=1 16K	Y=1 8K PR	Z=2 NON-PARITY
X=2 8K	Y=2 8K PL	

10. INSTALL/REMOVE WIRE-WRAP JUMPERS AS DEFINED BY THE MARKETING CONFIGURATION CODE. AFTER FINAL TEST.
11. SEE JUMPER LOCATION CHART FOR LOCATION OF SELECTABLE OPTION JUMPERS.
12. JUMPER P/N'S ARE LISTED IN ITEMS 8 & 10 OF B/M SHT 1.
13. THESE JUMPERS MAY HAVE TO BE INSTALLED WITH A HAND WIRE-WRAP TOOL.

NEXT ASSY	USED ON

MATERIAL

FINISH

TOLERANCE: ANG. | 2 PL | 3 PL

DR BY [signature] 11/6/78
CHK'D
M E
E E
P M [signature] 11-10-78

UNLESS OTHER SPECIFIED
DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES.
REMOVE BURRS AND SHARP EDGES. BREAK SHARP CORNERS .015 MAX.

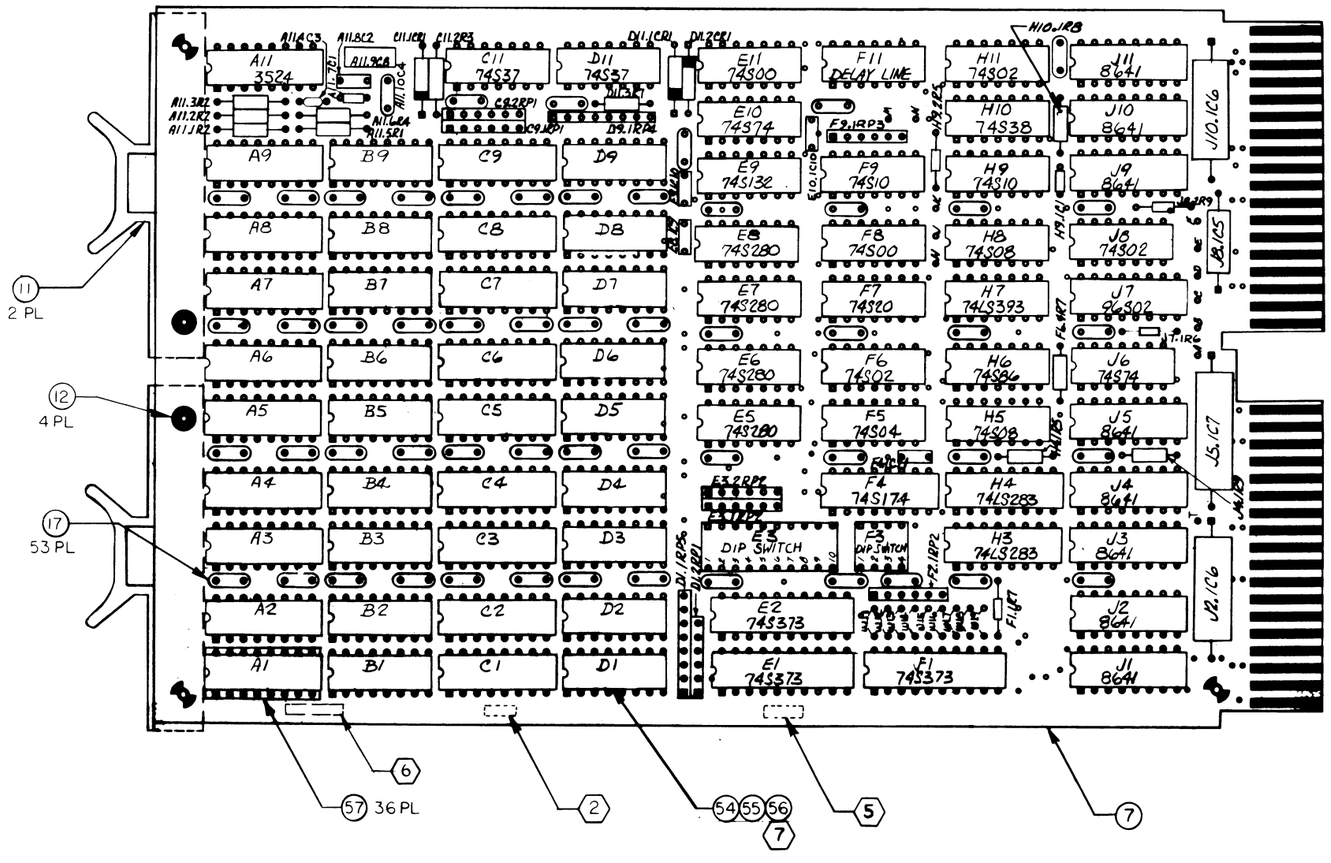
National Semiconductor Corporation
2900 Semiconductor Drive, Santa Clara, Calif. 95051

P.C.B. ASSEMBLY
NS23P 32K X 18

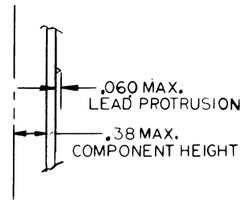
SIZE D | DR NO 980103625 | 000

SCALE 2:1 | SHEET 1 OF 3

REVISIONS			
REV	DATE	ECO NO.	APPVD
B		SEE SHEET ONE	
C		SEE SHEET 1	
D	–	ECO 2397	–
E	6-4-79	ECO 2866	



COMPONENT SIDE



MATERIAL		DR BY	
FINISH		CHKD	
		ME	
		EE	
		PE	
NEXT ASSY	USED ON	UNLESS OTHER SPECIFIED	
		TOLERANCE ANG / 2 PL / 3 PL	

DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES.
REMOVE BURRS AND SHARP EDGES. BREAK SHARP CORNERS .015 MAX

National Semiconductor Corporation
2900 Semiconductor Drive, Santa Clara, Calif. 95051

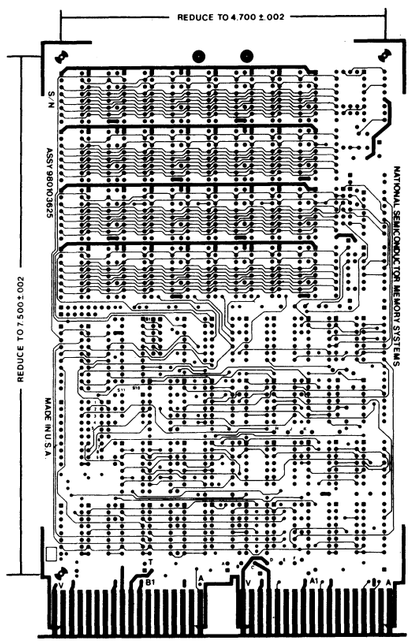
P.C.B. ASSEMBLY
NS 23P 32K X 18

SIZE D | DR NO 980103625 | 000

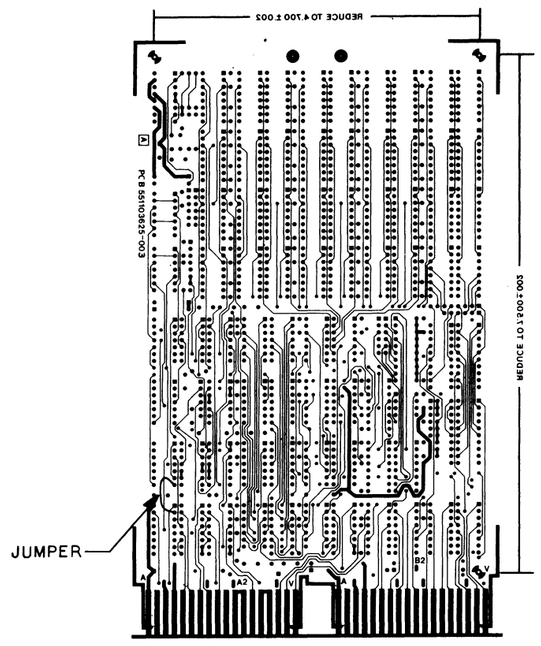
SCALE | SHEET 2 OF 3

REVISIONS			
RE.	DATE	ECO NO	APPVD
A		SEE SHT 1	
B		SEE SHT 1	
C		SEE SHT 1	
D		SEE SHT 1	
E	6-4-79	ECO 2866	

REWORK INSTRUCTIONS



COMPONENT SIDE



CIRCUIT SIDE

ADD JUMPER
FROM J11-2 TO H11-7

J.C. Jacobs 5-30-79

National Semiconductor Corporation
2900 Semiconductor Drive Santa Clara Calif. 95051

P.C.B. ASSEMBLY

NS23P 32K X 18

D	980103625	000
	1:1	3 3

UNIT OF MEAS: 01 • EACH, 02 • INCH, 03 • FEET, 04 • BULK, 05 • AS REQD, 09 • OTHER — KEY (1): A • WITH B/M, D • WITHOUT B/M, R • REFERENCE, S • SPECIFICATION — KEY (2) — RELEASED FOR ASSEMBLY — BILL OF MATERIAL NO. 980103625-000

ITEM/FIND NO	QUANTITY PER ASSEMBLY 000	UNIT OF MEAS	KEY (1)	KEY (2)	PART NUMBER/REFERENCE DOCUMENT	TITLE/DESCRIPTION	REF DESIG.	REMARKS
1								
2								
3	0	04	R		870103625-001	SCHEMATIC		
4								
5	0	04	S		426103625-001	PRODUCT SPEC & INSTAL. PROC.		
6	0	04	S		425103625-001	TEST SPECIFICATION		
7	1	04	D		551103625-003	PC BOARD		
8	0	04	D		600100158-005	WIRE, PVC, #30, SOLID, GRN		W3,4,5, 11-19.
9								
10	0	04	D		600100155-005	WIRE, PVC, #24, SOLID, GRN		W7-W10
11	2	04	D		740101006-001	HANDLE		
12	4	04	D		283101130-003	RIVET, 1/8 X 3/16		
13	11	04	D		283102019-001	WIRE-WRAP POST, .025 SQ	A, B, C,	D, E, F, H, J, K, [illegible]
14	2	04	D		151101308-025	CAP., CER, 1000pf, 100V, ±10%	C1	
15	1	04	D		151101308-037	CAP, CER, .01µF, 50V, +80 -20 %	C2	
16	1	04	D		151000048-001	CAP, CER, .1µF, 50V, +80 -20 %	C3	

NOTES

ASSY USAGE REF

ENG. CHG	REV	B	C	D	E
	CHG NO.	PSD 3054R	PDA 3386	ECO 2397	ECO 2866
	DATE	11-10-8	3-2-79	3-19-79	6-4-79
	APPR	[signature]	[signature]	[signature]	[signature]

WRITTEN BY SGO DATE 9-14-8 — DESIGN DATE — CHECKED BY DATE — APPROVED [signature] DATE 11-10-8

TITLE NS23P 32K X 18

National Semiconductor Corporation
2900 Semiconductor Drive, Santa Clara, Calif. 95051

SIZE — BILL OF MATERIAL NO 980103625-000 — SH 1 OF 5

FORM NO 0011A

BILL OF MATERIAL NO. 980103625-000

ITEM/FIND NO	QUANTITY PER ASSEMBLY 000	UNIT OF MEAS	KEY (1)	KEY (2)	PART NUMBER/REFERENCE DOCUMENT	TITLE/DESCRIPTION	REF DESIG.	REMARKS
17	53	01	D		151000055-001	CAP, CER, .47µF, 50V, +80 -20 %	C4	
18	1	01	D		155100632-039	CAP, CER, 6.8µF, 35V, ±20%	C5	
19	2	01	D		151100631-045	CAP, TANT, 22µF, 35V, ±10%	C6	
20	1	01	D		155100624-049	CAP, TANT, 47µF, 20V, ±20%	C7	
21	1	01	D		155104570-003	CAP, TANT, 22µF, 35V, ±20%	C8	KEMET T330D226M-035AS
22								
23	1	01	D		151101308-001	CAP, CER, 10pF, 100V, ±10%	C9	
24	2	01	D		151101308-003	CAP, CER, 15pF, 100V, ±10%	C10	CK05BX150K
25	1	01	D		151101308-019	CAP, CER, 330pF, 100V, ±10%	C11	CK05BX331K
26								
27	1	01	D		474102565-038	RES, FILM, 2.21K, 1/8W, 1%	R1	MIL-R-10509 RN55D2211F
28	3	01	D		-073	5.11K,	R2	5111F
29	1	01	D		-117	15.0K,	R3	1502F
30	1	01	D		474102565-166	, FILM, 51.1K, , 1%	R4	RN55D5112F
31	2	01	D		470101134-039	, CC, 100Ω, ±5%	R5	A-B BB-101-5
32	1	01	D		470101134-089	RES, CC, 12K, 1/8W, ±5%	R6	A-B BB-123-5

ENG. CHG	REV	B	C	D	E
	CHG NO.	SEE SHT 1	SEE SHT 1	ECO 2397	ECO 2866
	DATE			—	6-4-79
	APPR			—	[signature]

TITLE NS23P 32K X 18

National Semiconductor Corporation
2900 Semiconductor Drive, Santa Clara, Calif. 95051

BILL OF MATERIAL NO 980103625-000 — SH 2 OF 5

FORM NO 0011A

BILL OF MATERIAL NO. 980103625-000

ITEM/FIND NO	QUANTITY PER ASSEMBLY 000	UNIT OF MEAS	KEY (1)	KEY (2)	PART NUMBER/REFERENCE DOCUMENT	TITLE/DESCRIPTION	REF DESIG.	REMARKS
33	3	04	D		470101134-063	RES, CC, 1K, 1/8W, ±5%	R7	A-B BB-102-5
34	1	04	D		470101134-109	RES, CC, 82K, 1/8W, ±5%	R8	A-B BB-823-5
35	2	04	D		470101134-087	RES, CC, 10K, 1/8W, ±5%	R9	A-B BB-103-5
36								
37								
38	3	04	D		474104568-005	RES. MOD, 6 PIN, 3/33Ω	RP1	BOURNS 4306R-102-330
39	3	04	D		474100806-041	RES. MOD, 6 PIN, 5/1K	RP2	
40	1	04	D		474104568-033	RES. MOD, 6 PIN, 3/470Ω	RP3	BOURNS 4306R-102-471
41	1	04	D		474104569-057	RES. MOD, 8 PIN, 4/4.7K	RP4	BOURNS 4308R-102-472
42	1	04	D		474104569-005	RES. MOD, 8 PIN, 4/33Ω	RP5	BOURNS 4308R-102-330
43								
44								
45	1	04	D		513 100 986-010	SWITCH, DIP, 10-POS, ROC		
46	1	04	D		513 100 986-004	SWITCH, DIP, 4-POS, ROC		
47								
48								

ENG. CHG	REV	B	C	D	E
	CHG NO.	SEE SHT 1	SEE SHT 1	ECO 2397	ECO 2866
	DATE			—	6-4-79
	APPR			—	[signature]

TITLE NS 23P 32K X 18

National Semiconductor Corporation
2900 Semiconductor Drive, Santa Clara, Calif. 95051

BILL OF MATERIAL NO 980103625-000 — SH 3 OF 5

FORM NO 0011A

BILL OF MATERIAL NO. 980103625-000

ITEM/FIND NO	QUANTITY PER ASSEMBLY 000	UNIT OF MEAS	KEY (1)	KEY (2)	PART NUMBER/REFERENCE DOCUMENT	TITLE/DESCRIPTION	REF DESIG.	REMARKS
49	3	04	D		481000083-001	DIODE, IN914B	CR1	
50								
51	1	04	D		482104567-002	REG. PULSE WIDTH MODULATOR		NS LM3524J
52								
53	1	04	D		611104536-005	DELAY LINE, ACTIVE, 200NS, 5-TAP		POLANA ENG'G 54-074
54	0	04			482102598-022	I.C. 16K RAM, 200NS		⟨7⟩
55	0	04			482103060-112	I.C. 8K PLH RAM, 200NS		⟨7⟩
56	0	04			482102989-112	I.C. 8K PRH RAM, 200NS		⟨7⟩
57	36	01	D		214102685-003	SOCKET, DIL, 16-PIN		
58								
59	1	01	D		482102062-001	I.C. 96S02		
60	8	01	D		482103697-001	I.C. 8641		
61	2	01	D		482000079-001	I.C. 74S00		
62	3	01	D		482000334-001	I.C. 74S02		
63	1	01	D		482000180-001	I.C. 74S04		
64	2	01	D		482100672-001	I.C. 74S08		

ENG. CHG	REV	B	C	D	E
	CHG NO.	SEE SHT 1	SEE SHT 1	ECO 2397	ECO 2866
	DATE			—	6-4-79
	APPR			—	[signature]

TITLE NS 23P 32K X 18

National Semiconductor Corporation
2900 Semiconductor Drive, Santa Clara, Calif. 95051

BILL OF MATERIAL NO 980103625-000 — SH 4 OF 5

FORM NO 0011A

BILL OF MATERIAL NO. 980103625-000

ITEM/FIND NO	QUANTITY PER ASSEMBLY ALL	UNIT OF MEAS	KEY (1)	KEY (2)	PART NUMBER/REFERENCE DOCUMENT	TITLE/DESCRIPTION	REF DESIG.	REMARKS
65	2	01	D		482001344-001	I.C. 74S10		
66	1	01	D		482001345-001	I.C. 74S20		
67	2	01	D		482100777-001	I.C. 74S37		
68	1	01	D		482100778-001	I.C. 74S38		
69	2	01	D		482000179-001	I.C. 74S74		
70	1	01	D		481100300-001	I.C. 74S86		
71	1	01	D		482100840-001	I.C. 74S132		
72	1	01	D		482000337-001	I.C. 74S174		
73	4	01	D		482000342-001	I.C. 74S280		
74	2	01	D		482103983-001	I.C. 74LS283		
75	3	01	D		482102641-001	I.C. 74S373		
76	1	01	D		482102639-001	I.C. 74LS393		
77								
78								
79								
80								

ENG. CHG	REV	B	C	D	E
	CHG NO.	SEE SHT 1	SEE SHT 1	ECO 2397	ECO 2866
	DATE			—	6-4-79
	APPR			—	[signature]

TITLE NS 23P 32K X 18

National Semiconductor Corporation
2900 Semiconductor Drive, Santa Clara, Calif. 95051

BILL OF MATERIAL NO 980103625-000 — SH 5 OF 5

FORM NO 0011A