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DZS11-EA

OPTION DESCRIPTION

digital

Computer Special Systems

NOTEBOOK SECTION

3.1

OPTION NUMBER

DZS11-EA

DRAWING SET NUMBER

YA-CØ6LB-ØØ

PROGRAM NUMBER

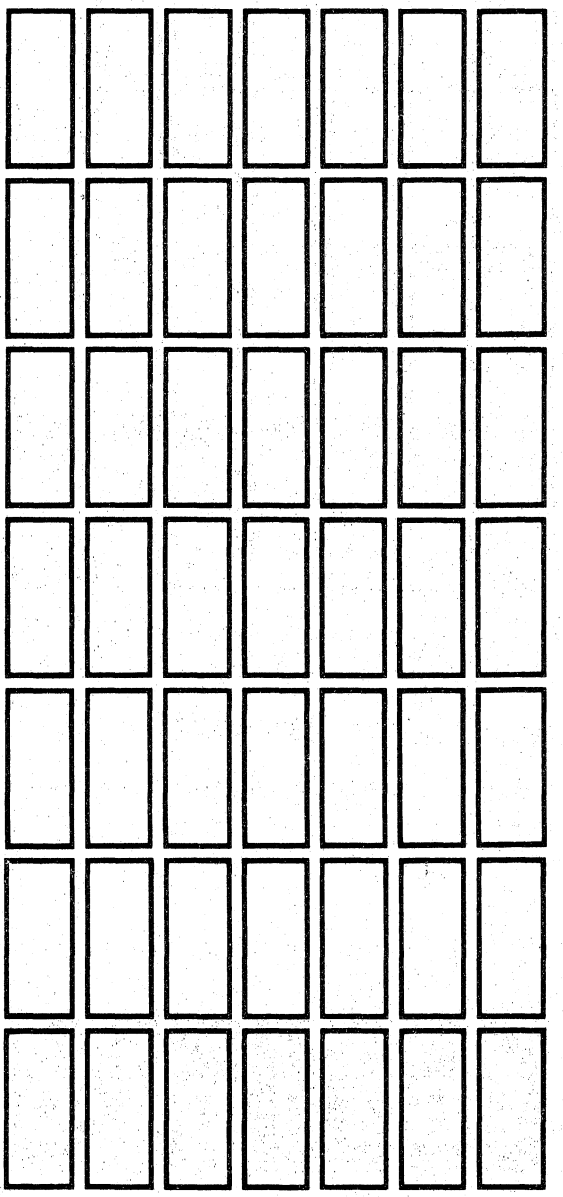
N/A

DOCUMENT NUMBER **REVISION**

YA-CØ6LC-ØØ A (X006)

DATE

AUGUST, 1981



DZS11-EA

OPTION DESCRIPTION

digital

Computer Special Systems

AUSTRALIA

First Edition August, 1981

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PREFACE

This manual describes in detail the installation requirements, programming and operational considerations, and maintenance procedures including diagnostic support, for the DZS11-EA Statistical Multiplexer (M7190). A variety of appendices are provided to supplement the above.

Complete understanding of the documents contents requires that the reader have a general knowledge of statistical multiplexing techniques, digital circuitry and a basic understanding of PDP-11 computers.

Other publications which support this document are:-

- DZS11-EA Print Set
- VT1XX-EA/EB Technical Manual
- PDP-11 Processor Handbook
- PDP-11 Peripherals Handbook
- PDP-11 Paper Tape Software Handbook
- Appropriate System User's Manual

CHAPTER 1

INTRODUCTION

1.1 SCOPE

Sections 1.1 through 1.3 of this chapter contains an introduction to the DZ Statistical Multiplexer network; including DZS11-EA, VT1XX-EA, VT1XX-EB, and VT1XX-EC.
Section 1.4 of this chapter contains DZS11-EA specifications.

1.2 ENGINEERING DRAWINGS

A complete set of engineering drawings and circuit schematics is provided in a companion volume to this manual entitled DZS11-EA Field Maintenance Print Set. The general logic symbols used on these drawings are described in the DIGITAL Logic Handbook. Specific symbols and conventions are also included in certain PDP-11 systems manuals. The following paragraphs describe the signal nomenclature convention used on the drawing set.

Signal names in the DZS11-EA print set are given in the following basic form:

SOURCE SIGNAL NAME POLARITY

SOURCE indicates the drawing number of the print set where the signal originates. The drawing number of a print is located in the lower right corner of the print title block (S1, S2, S3 etc). SIGNAL NAME is the proper name of the signal. The names used in the print set are also used in this manual. POLARITY is either H or L to indicate the voltage level of the signal. H means +3 V; L means ground. As an example, the signal:

(S2) SELECT L

originates on sheet 2 of the M7190 module drawing and is read, when SELECT is true, this signal is at ground.
UNIBUS signal lines do not carry a SOURCE indicator. These signal names represent a bidirectional wire-ORed bus; as a result, multiple sources for a particular bus signal exist. Each UNIBUS signal name is prefixed with the word BUS.

1.3 DZ11 STATISTICAL MULTIPLEXER GENERAL DESCRIPTION

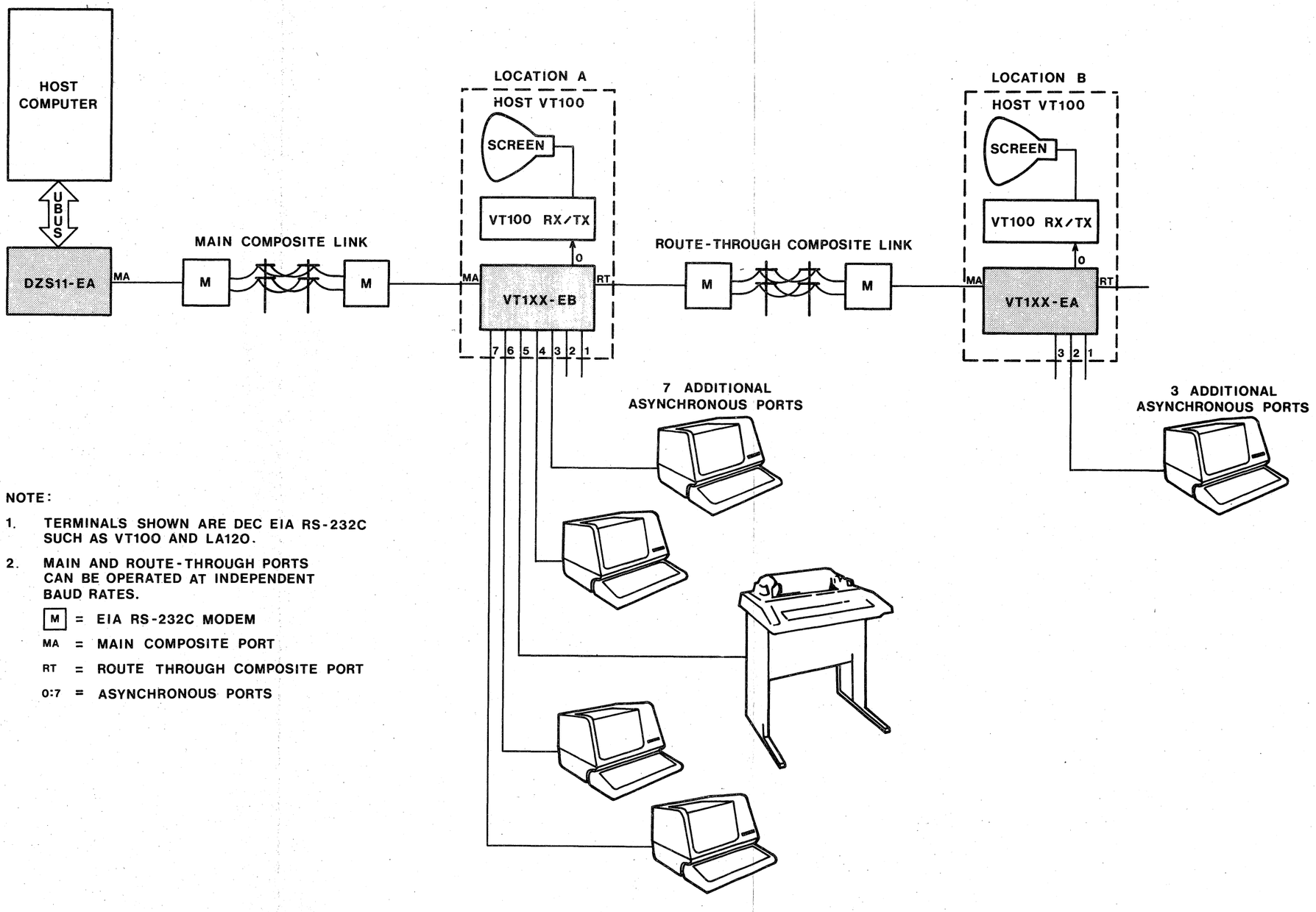
The DZ Statistical Multiplexer (DZ STAT MUX) is a term used to describe a statistical multiplexer network consisting of one DZS11-EA as described by this manual and any combination of one or two VT1XX-EA or VT1XX-EB remote statistical multiplexers enabling a max of 8 remotely located asynchronous terminals to share a common composite communications link.

Figure 1-1 shows a typical DZ STAT MUX network consisting of eight asynchronous terminals connected to a computer system via a serial composite communication link.
The network consists of a DZS11-EA statistical multiplexer mounted in the computer system, a VT1XX-EB eight channel statistical multiplexer at location "A" and a VT1XX-EA four channel statistical multiplexer at location "B".
The DZS11-EA and VT1XX-EB are interconnected by the Main composite link, the VT1XX-EB and VT1XX-EA are interconnected by the Route-Through composite link. Both VT1XX-EA and VT1XX-EB options have route through ports and can therefore be interchanged in Figure 1.1.
Both composite links conform to the X.25 level 2 communication protocol, thereby offering a high degree of data integrity through automatic re-transmission upon detection of transmission errors.
Integral long line drive devices on all components of the network enable direct interconnection of the composite links with cable lengths in excess of one km., where modem connections are not required. This feature uses RS-422 full differential transceivers and is selectable at installation time by means of quick connect straps.

Both VT1XX-EA and VT1XX-EB mount within a standard VT100 enclosure, and so when installed, the first asynchronous terminal and statistical multiplexer become an integral unit. Any combination of the maximum eight asynchronous terminals, can be located across locations "A" and "B", e.g six may be connected at location A and two may be connected at location B. The host VT100 housing the VT1XX-EA/EB option need not be one of these terminals. Asynchronous ports are enabled/disabled at installation.

Features of the DZ11 Statistical Multiplexer include:-

- Integral DZ11-A asynchronous communications multiplexer and statistical multiplexer on one hex module
- DZ11-A, DZ11-C asynchronous multiplexer software compatibility.
- Integral VT100 and VT1XX-EA/EB statistical multiplexer at terminal location
- Connection of up to 8 asynchronous terminals (including host VT100s) located at one or two remote locations via one composite communication link and route through composite link in the case where two VT1XX-EA/EBs are used.
- High communication efficiency of the composite link through dynamic bandwidth allocation.
- Data integrity between asynchronous terminal port and computer, through composite port high level protocol which handles message sequencing and error correction by automatic re-transmissions.
- Comprehensive micro diagnostic tools for network and option diagnosis.
- Echoplex or local echo operation for asynchronous ports.
- Ability to format asynchronous ports through system software SET commands.



NOTE:

1. TERMINALS SHOWN ARE DEC EIA RS-232C SUCH AS VT100 AND LA120.
2. MAIN AND ROUTE-THROUGH PORTS CAN BE OPERATED AT INDEPENDENT BAUD RATES.

[M] = EIA RS-232C MODEM

MA = MAIN COMPOSITE PORT

RT = ROUTE THROUGH COMPOSITE PORT

0:7 = ASYNCHRONOUS PORTS

Figure 1-1 Typical DZ Stat Mux Network

1.3.1 DZS11-EA General Description

The DZS11-EA is a single module containing DZ11-A asynchronous multiplexer emulator and statistical multiplexer. The option is program compatible to the DZ11-A and therefore interfaces to the operating system via standard device drivers. To the operating system, a DZ STAT MUX network consisting of DZS11-EA, and one or two VT1XX-EA/EB stat muxes appears as eight asynchronous terminals connected via a standard DZ11-A multiplexer.

1.3.2 VT1XX-EA General Description

The VT1XX-EA statistical multiplexer is a component of the DZ STAT MUX network. The option is a four channel stat mux enabling four asynchronous terminals to be statistically multiplexed to a DZS11-EA via the composite communication link. The VT1XX-EA has two composite communication ports, the Main and the Route-through.

The Main composite communication port interfaces to a primary device, (a DZS11-EA or another VT1XX-EA/EB when the VT1XX-EA is the second cluster controller) via the Main composite link while the Route-through port interfaces to the secondary device in the case where Route-through is implemented. Both composite ports operate independently at baud rates from 1200 to 19200 bits/second from an internal or external timing source.

Asynchronous port parameters are down line loaded via the DZS11-EA at network initialization time or following operating system SET commands. This feature enables asynchronous ports to be re-formatted at the terminal keyboard by issuing the appropriate operating system SET command.

1.3.3 VT1XX-EB General Description

The VT1XX-EB statistical multiplexer is a component of the DZ STAT MUX network and is shown in Figure 1.1 at location "A". The option is identical in operation to the VT1XX-EA with the exception of an additional four asynchronous ports, thus enabling a maximum of up to eight asynchronous terminals to be statistically multiplexed to a DZS11-EA.

1.3.4 VT1XX-EC General Description

The VT1XX-EC is an option for the VT1XX-EA four channel statistical multiplexer. The option is field installable, and modifies a VT1XX-EA (4 channel stat. mux) to a VT1XX-EB (8 channel stat. mux).

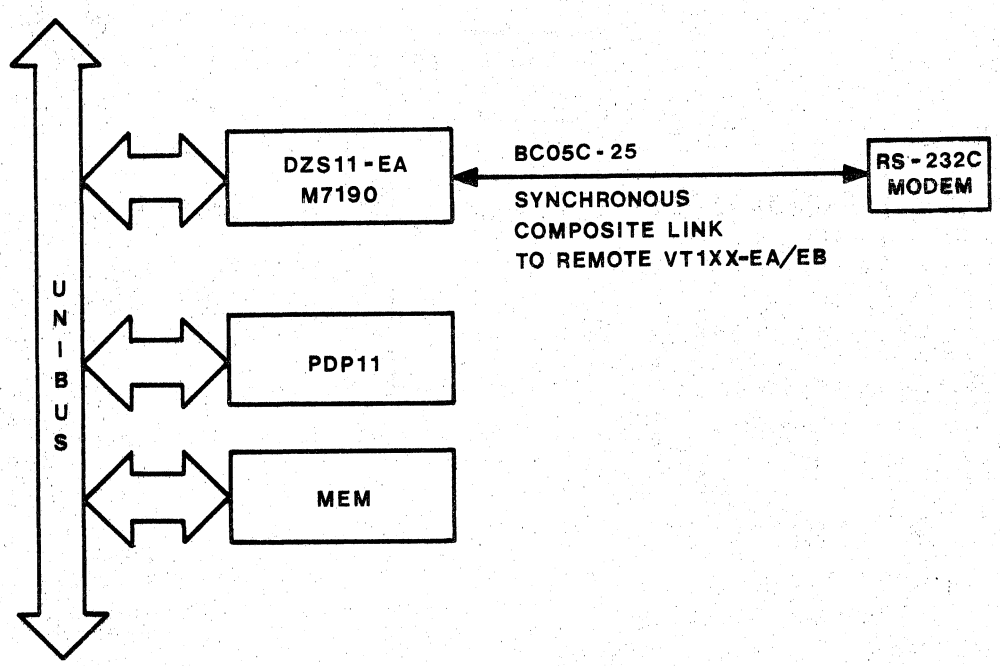


Figure 1-2 Typical PDP11 Application

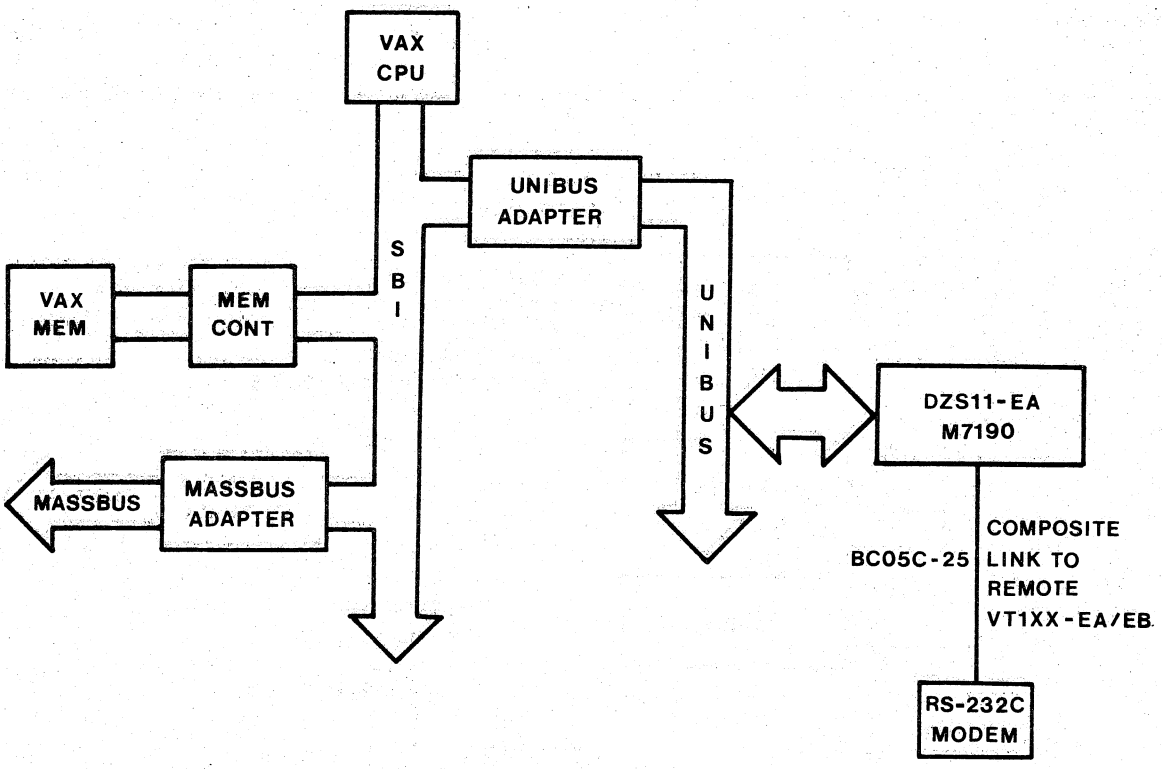


Figure 1-3 Typical VAX-11/780 Application

1.4 PHYSICAL DESCRIPTION

1.4.1 DZS11-EA Physical Description

The DZS11-EA consists of one hex size printed circuit board and composite port interconnect cable as shown in Figure 1-4. The option replaces the functionality of a DZ11-A, distribution panel, eight interconnect cables and the traditional stand alone statistical multiplexer.
The option interfaces to the UNIBUS via a standard small peripheral controller slot (SPC), and to the DZ STAT MUX network via a standard RS-232C interrconnect cable (BCØ5C-25).
An on board 8 bit microcontroller performs the DZ11-A emulation and statistical multiplexing functions. Microdiagnostics can be evoked by maintenance personnel, enabling diagnosis of both the DZS11-EA option and DZ STAT MUX network.

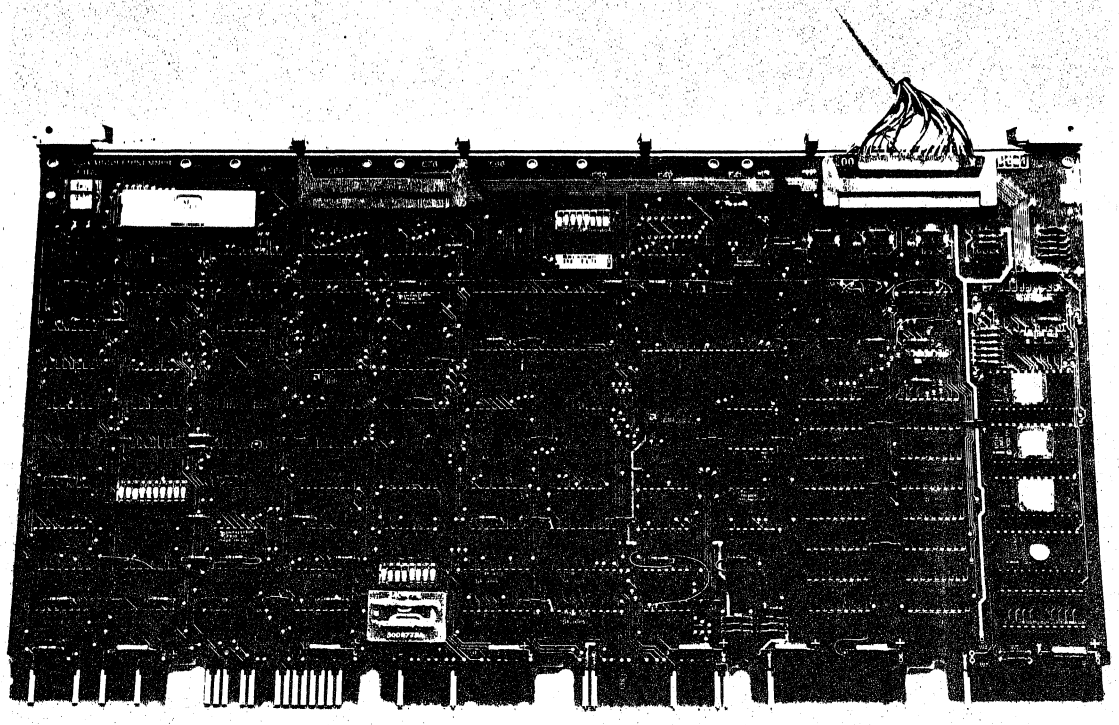


Figure 1-4 DZS11-EA Option (M719Ø)

1.4.2 VT1XX-EA Physical Description

The VT1XX-EA four channel statistical multiplexer is a printed circuit board set, plus mounting hardware, specifically designed to mount into a VT100 mounting enclosure. When installed, the VT1XX-EA and host VT100 become an integral option, with the host VT100's communication port connected to the first asynchronous port (port 0) of the VT1XX-EA.
Figure 1-5 shows the components of the VT1XX-EA.
Figure 1-6 shows a rear view of the host VT100 following installation of the VT1XX-EA. Note, that the VT100's communications port has become the Main composite port for the VT1XX-EA with the Route-Through composite port directly above. Of the seven additional asynchronous ports shown on the distribution panel, only the first 3 (ports 1, 2, and 3) are operational in the case of the VT1XX-EA.

1.4.3 VT1XX-EB Physical Description

The VT1XX-EB eight channel statistical multiplexer consists of one VT1XX-EA plus one VT1XX-EC four channel expansion option. (Refer Section 1.4.4).
Figure 1-7 shows the VT1XX-EB, consisting of VT1XX-EA with VT1XX-EC installed.

1.4.4 VT1XX-EC Physical Description

The VT1XX-EC is an expansion option for the VT1XX-EA statistical multiplexer. The option connects a VT1XX-EA to a VT1XX-EB by the addition of four asynchronous ports. The VT1XX-EC option consists of one printed circuit board and cable as shown in Figure 1-8. The printed circuit board clips to the VT1XX-EA/EB control module. The BC05Z-01 cable connects the four additional UARTS to the distribution board.

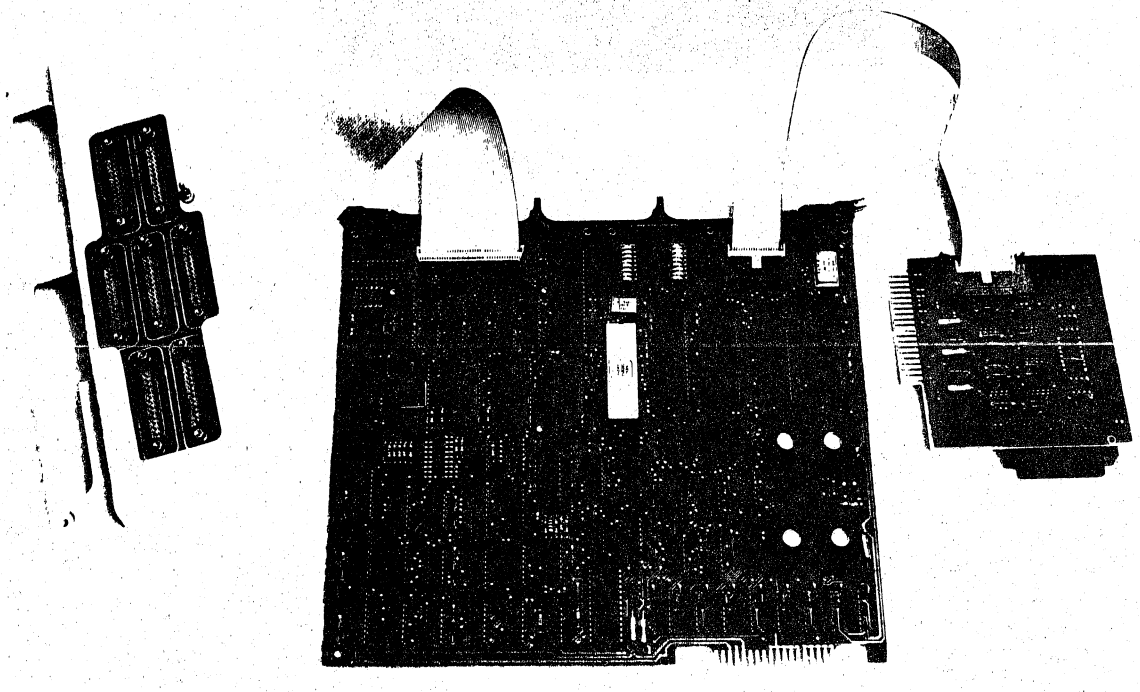


Figure 1-5 VT1XX-EA Module Set

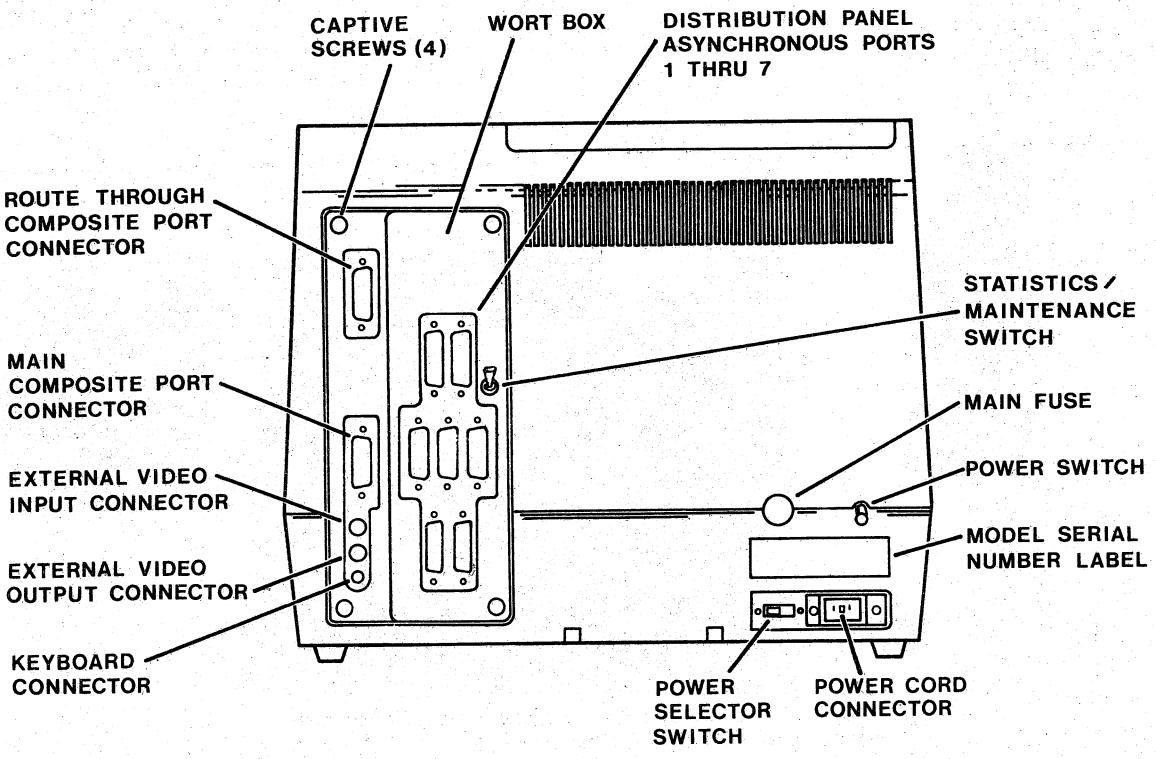


Figure 1-6 VT100 Rear View with VT1XX-EA/EB Installed.

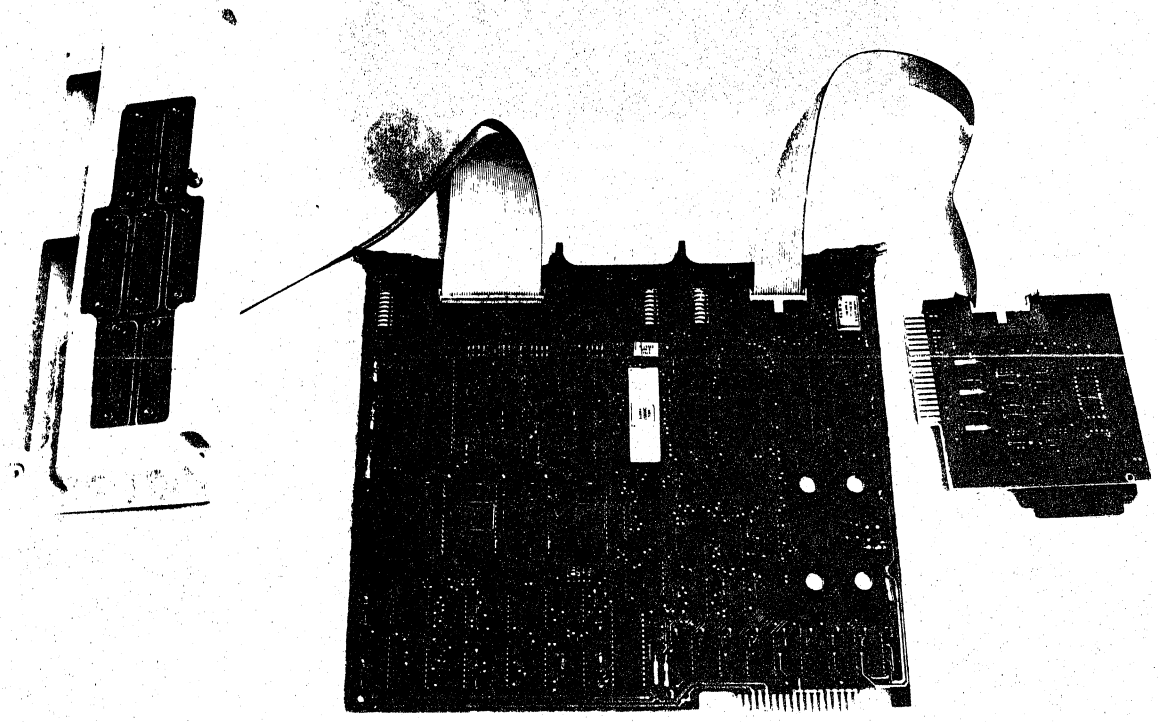


Figure 1-7 VT1XX-EB Module SET

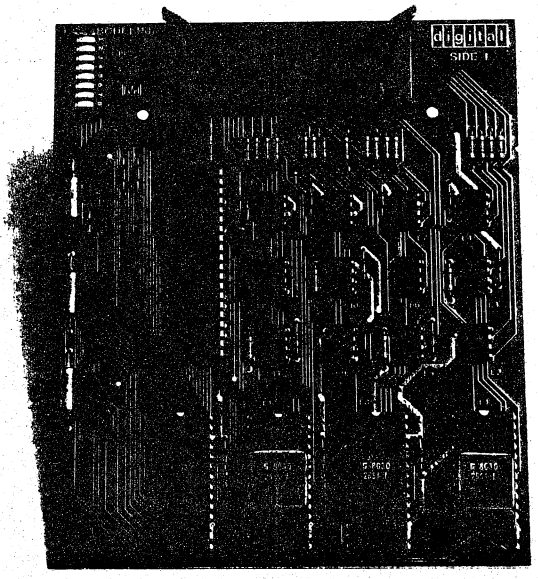


Figure 1-8 VT1XX-EC Option

1.5 SPECIFICATIONS

The following paragraph contains electrical, environmental and performance specifications for the DZS11-EA. Performance specifications are listed in two separate categories, composite and asynchronous ports. Table 1-2 lists the composite port parameters, Table 1-3 lists the VT1XX-EA/EB asynchronous port parameter supported by the DZS11-EA.

1.5.1 Electrical

M7190 Module Power Requirements

+5V ± 5%	3.35 ampers typical	(3.5 ampers max)
+15V ± 3%	Ø.Ø13 ampers typical	(Ø.Ø69 ampers max)
-15V ± 3%	Ø.Ø2Ø ampers typical	(Ø.Ø8Ø ampers max)

UNIBUS loading

ac loading = 1 unit load
dc loading = 1 unit load

1.5.2 Environmental

Operating: 5°C to 5Ø°C (4Ø°F to 122°F) with a relative humidity of 5% to 95% (noncondensing), with adequate airflow across the module. When operating at the maximum temperature (5Ø°C or 122°F), air flow must maintain the inlet to outlet air temperature rise across the module at no more than 5°C (9°F).

Storage: -4Ø°C to 8Ø°C (-4Ø°F to 176°F) with a relative humidity of 5% to 95% noncondensing.

NOTE

Before operating a module that has been stored in an environment outside the specified operating environment, the module must be allowed to stabilize at the operating environment for at least 5 minutes minimum.

1.5.3 Physical

Height	40	cm (15.7	in) typical
Width	1.27	cm (0.5	in) typical
Length	22.8	cm (8.9	in) typical

1.5.4 Operational

Operational specification for the DZS11-EA statistical multiplexer are listed below in tables 1-1, 1-2, and 1-3.

Table 1-1 lists DZS11-EA UNIBUS operational specification
Table 1-2 lists DZ STAT. MUX, multiplexing specifications
Table 1-3 lists VT1XX-EA/EB asynchronous port specifications.

Table 1-1 DZS11-EA UNIBUS Operational Specifications

PARAMETER	DESCRIPTION
Registers	Control and Status Register (CSR) Receive Buffer Register (RBUF) Line Parameter Register (LPR) Transmit Control Register (TCR) Modem Status Register (MSR) Transmit Data Register (TDR)
Register Addresses	CSR 760010 Read/Write RBUF 760012 Read Only LPR 760012 Write Only TCR 760014 Read/Write MSR 760016 Read Only TDR 760016 Write Only **NOTE:** Address specified is first address of the floating address space. Refer to Appendix B Floating Device Addresses and Vectors.
Interrupt Vector Addresses	300 Receiver Interrupt 304 Transmitter interrupt. See floating Vectors Appendix B.
Priority Level	Normally, a level 5 priority plug is supplied. The interface level can be modified to level 4, 6, or 7 by using the proper priority plug.
Interrupt Types	**RDONE** Occurs each time a character appears at the silo output. **SA** Silo Alarm. Occurs after 16 characters enter the silo. Rearmed by reading the silo. This interrupt disables the RDONE interrupt. **TRDY** Occurs when the scanner finds a line ready to transmit on. **NOTE** There are no modem interrupts.

Table 1-2 DZ STAT MUX Multiplexing Specification

PARAMETER	DESCRIPTION
Apparent Efficiency	Up to 400% depending on application. Defined as aggregate asynchronous terminal port Bandwidth divided by Composite port Bandwidth.
Real Efficiency	% Baud Rate xx 1200 xx 2400 xx 4800 xx 9600 xx 19200 **Note:** Real efficiency is a measure of the net composite port bandwidth available for information transfer. The percentage quoted does not include character compression from asynchronous to synchronous, e.g. removal of start, parity and stop bits. In a typical system where 8 data bits, 1 start and 1 stop bit are compressed into 8 data bits, the net bandwidths listed above are increased by a factor of 120%.
Transit Delay	Min Max Baud Rate xxxms xxxms 1200 b/s xxxms xxxms 2400 b/s xxxms xxxms 4800 b/s xxxms xxxms 9600 b/s xxxms xxxms 19200 b/s **NOTE:** Transit delays specified above are approx. and are defined as the echoplex time, i.e. the time taken for a full round trip journey from asynchronous port through network not including operating system and back to asynchronous port.
Character Compression	Up to 16 space characters (40_8) are transmitted as one 8 bit character.
Buffer Space	DZS11-EA 3K characters VT1XX-EA/EB 12K characters

Table 1-3 Asynchronous Port Specifications

PARAMETER	DESCRIPTION
Operating Mode	Full Duplex
Data Format	Asynchronous, serial by bit, 1 start and 1, 1-1/2 (5-level codes only) or 2 stop bits supplied by the hardware under program control.
Character Size	5,6,7 or 8 bits; program-selectable. (Does not include parity bit).
Parity	Parity is program-selectable. There may be none, or it may be odd or even.
Order of Bit	Transmission/reception low-order bit first.
Baud Rates	50, 75, 110, 135.5, 150, 300, 600, 1200, 1800, 2000, 2400, 3600, 4800, 7200 and 9600.
Breaks	Can be generated and detected on each line.
Throughput	Up to 115% (Real Efficiency) of DZS11-EA composite baud rate
Asynchronous	Pin 1 Protective Ground Pin 7 Signal Ground Pin 2 Transmitted Data Pin 3 Received Data Pin 20 Data Terminal Ready Pin 22 Ring Indicator Pin 8 Carrier
Distortion	The maximum "space to mark" and "mark to space" distortion allowed in a received character is 40 percent. The maximum speed distortion allowed in a received character for 2000 baud is 3.8 percent. All other baud rates allow 4 percent. The maximum speed distortion from the transmitter for 2000 baud is 2.2 percent. All other baud rates have less than 2 percent.

Table 1-3 Asynchronous Port Specifications cont.

PARAMETER	DESCRIPTION
Asyn. Port Enable/Mapping	Individual ports can be enabled or disabled at VT1XX-EA/EB installation by appropriate setting of dual in line (DIL) switches. This feature enables the maximum configuration of 16 physical ports to be logically connected to the 8 DZS11-EA ports. At network initialisation, enabled ports are logically mapped to the eight DZS11-EA ports, e.g. in a network consisting of two VT1XX-EB's with six enabled ports at the primary VT1XX-EB and two enabled ports at the secondary VT1XX-EB, the six enabled ports at the VT1XX-EB will be mapped to DZS11-EA ports 0 thru 5 inclusive, while the remaining 2 enabled port at the secondary VT1XX-EB will be mapped to ports 6 and 7. Only the first 8 of the enabled ports in the network are mapped.
Port Flow Synchronisation	Data synchronisation is necessary on each asynchronous port to control the flow of data. Two methods are available to the user, they are:- o Software XON/XOFF control characters o Hardware DTR/DSR signals The user has the choice of one of the above procedures on a per line basis. This is enabled at installation time by setting DIL switches.
Local Echo/ Echoplex	Asynchronous ports can be operated in either echoplex mode or local echo mode. The modes can be operator configured by modifying SET UP B field 5 of the host VT100. Field 5 contains four bits, each bit controls two ports.

1.5.5 Composite Port

This section contains an introduction to and specification of the DZ STAT MUX network composite links. The term "Main composite link" as used throughout this manual, denotes the logical data link between DZS11-EA and primary VT1XX-EA/EB. The term "Route-through composite link" as used through-out this manual denotes the logical data link between primary VT1XX-EA/B and secondary VT1XX-EA/EB. Both Main and Route-through composite links are shown in Figure 1-1.

The composite links are used for link control between the DZ STAT MUX components, and for the transfer of data between DZS11-EA UNIBUS interface and the VT1XX-EA/EB asynchronous ports.
Link control tasks include; Network initialisation, following system initialisation and or power up. Down line loading of asynchronous port parameters e.g baud rate, and character format from DZS11-EA to VT1XX-EA/EB, and control of data flow, in the form of frame sequencing and re-transmission control.

1.5.5.1 Composite Port Interface

The DZS11-EA composite port conforms to EIA RS-232C and EIA RS-423 interface standards simultaneously. Interconnection to the Main composite link is via a BC05C-25 cable, (Figure 1-9). Table 1-4 lists the correlation between connector pins and signal functions for this cable. Although the DZS11-EA is shipped with the composite port conforming to EIA RS-232C for modem connection, the port can be re-configured for long line driver capability at installation time utilising RS-422 full differential transceivers. The modification requires component changes on the DZS11-EA module plus the addition of an option cable to replace the standard BC05C-25. The exact cable type is dependent upon the network configuration, however, cable type BC05Z-25 is such a cable and is therefore included in Table 1-4 as an example. Figure 1-10 shows the BC05Z-25.

Table 1-4 DZS11-EA Composite Port Connector Pinning

PIN	SIGNAL/FUNCTION	DB25P PIN	BCO5Z-25
A	PROTECTIVE GROUND	7	-
B	SIGNAL GROUND	1	-
C	DATA SPEED SELECT	23	-
D:E	NO CONNECTION	-	-
F	EIA XMIT DATA	2	-
H	H833 TEST CON. FLAG	-	-
J	EIA SERIAL DATA IN	3	-
K	RX DATA DIFF +	-	R
L	EIA CLOCK EXT	24	-
M	NO CONNECTION	-	-
N	EIA XMIT CLOCK	15	-
P	NO CONNECTION	-	-
R	EIA REC CLOCK	17	-
S	RX DATA DIFF -	-	T
T	CLEAR TO SEND	5	D
U	NO CONNECTION	-	-
V	REQUEST TO SEND	4	C
W:Y	NO CONNECTION	-	-
Z	DATA SET READY	6	E
AA	TX DATA DIFF +	-	P
BB	CARRIER DETECT	8	F
CC	TX CLOCK DIFF +	-	Y
DD	DATA TERMINAL READY	2Ø	H
EE	CLOCK EXIT DIFF -	-	W
FF	NO CONNECTION	-	-
HH	RX CLOCK DIFF +	-	V
JJ	NO CONNECTION	-	-
KK	TX DATA DIFF -	-	S
LL:NN	NO CONNECTION	-	-
PP	CLOCK EXIT DIFF +	-	U
RR	NO CONNECTION	-	-
SS	RX CLOCK DIFF -	-	X
TT	TX CLOCK DIFF -	-	a
UU	SIGNAL GROUND	7	-
VV	PROTECTIVE GROUND	1	-

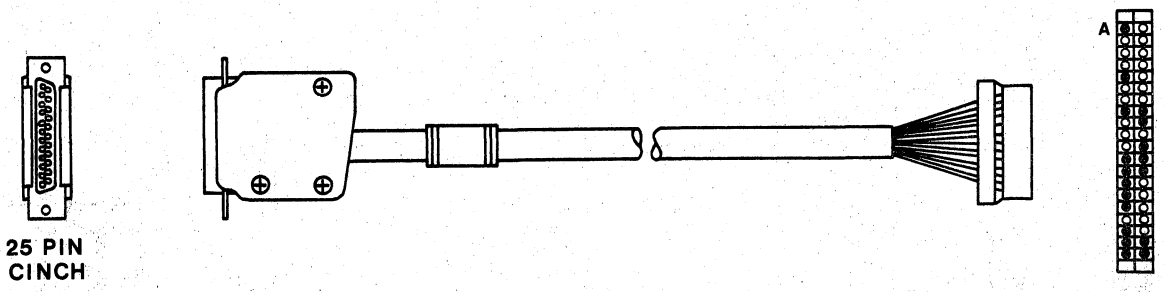


Figure 1-9 BCØ5C-25 RS-232C Cable

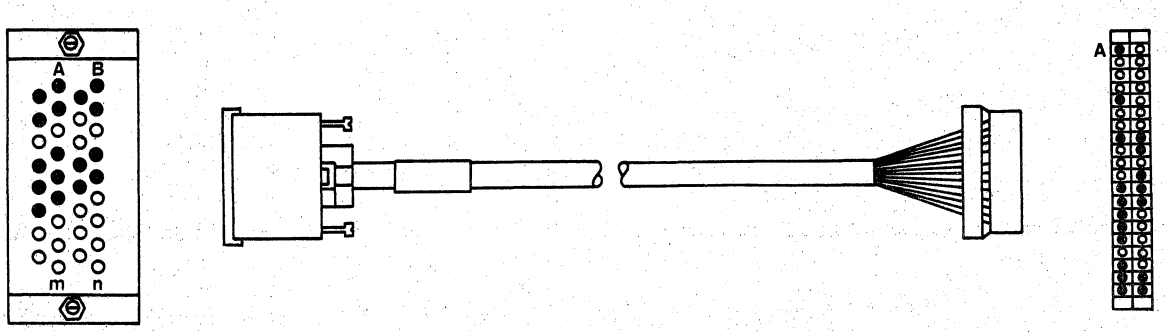


Figure 1-1Ø BCØ5Z-25 Long Line Driver Cable

1.5.5.2 Composite Port Interface Signals

A description of each composite port signal is provided below.

Protective Ground - pin 1
This conductor is electrically bonded to the computer chassis which is connected to the ground lead of the AC power cord. The use of this conductor for reference potential purposes is not allowed.

Transmit Data - pin 2
The DZS11-EA transmits serially encoded data on this conductor. A constant transmission of flag characters are maintained on this conductor at all times when data is not being transmitted.

Receive Data - pin 3
The DZS11-EA receives serially encoded data on this conductor.

Request to Send - pin 4
Not Used.

Clear to Send - pin 5
This conductor is ignored at all times.

Data Set Ready - pin 6
Not Used.

Signal Ground - pin 7
This conductor establishes the common ground reference potential for all voltages on the respective interface.

Carrier Detect - pin 8
This signal is ignored at all times.

Transmission Clock - pin 15
When the DZS11-EA is selected for external timing, the option receives a timing signal on this conductor which is in turn used by the DZS11-EA to clock the serially encoded data being transmitted on pin 2. When operated in the internal timing mode, this conductor is ignored.

Receive Clock - pin 17
When the DZS11-EA is operated in the external timing mode, a timing signal is received on this conductor which is used to time reception of serial data on pin 3. When operated in the internal timing mode the DZS11-EA ignores this conductor.

Data Terminal Ready - pin 20
Not Used.

Clock External - pin 24
The DZS11-EA uses this conductor to provide an external baud rate timing signal. A timing signal is present on this conductor irrespective of whether the DZS11-EA is in internal or external timing mode. The signal frequency is equal to the operational baud rate and is defined by an on board switch register.

1.6 DZ STAT MUX OPTIONS

Table 1-5 lists all DZ STAT MUX network options.

Table 1-5 DZ STAT MUX Network Options

PART NUMBER	DESCRIPTION
DZS11-EA	Eight channel statistical multiplexer for UNIBUS machine (local mux).
VT1XX-EA	Four channel statistical multiplexer for mounting in VT100 enclosure (remote mux).
VT1XX-EB	Eight channel statistical multiplexer for mounting in VT100 enclosure (remote mux).
VT1XX-EC	Four channel expansion option for VT1XX-EA. The VT1XX-EC converts the VT1XX-EA to an VT1XX-EB.
VT100-YE	VT100-AA with VT1XX-EA installed (110V).
VT100-YF	VT100-AB with VT1XX-EA installed (240V).
VT100-YH	VT100-AA with VT1XX-EB installed (110V).
VT100-YJ	VT100-AB with VT1XX-EB installed (240V).

1.7 DZ STAT MUX CABLES

1.7.1 DZS11-EA Cables

The standard DZS11-EA is shipped conforming to EIA RS-232C standards. The option as shipped, includes a 25 foot RS-232C cable (BCØ5C-25) for direct connection to a modem.
In cases where other standards are required, e.g. EIA RS-423 and long line driver facility, optional cables will be necessary.
Details of these cables is given in Section 2 (Installation) of this manual.
It should be noted that if interface standards other than EIA RS-232C are required for this option, then optional cables will be required.

1.7.2 VT1XX-EA/EB Composite Port Cables

VT1XX-EA and VT1XX-EB composite port interfaces are as shown in Figure 1-6. Note, modem interface cables are not shipped with these options.

Where EIA RS-232C interface connections are required, one BCØ5D-25 cable should be ordered for each composite port being implemented. E.G. for a network consisting of one only VT1XX-EA/EB, one only BCØ5D-25 is required. In a network consisting of two VT1XX-EA/EB's, three BCØ5D-25 cables will be required.

1.7.3 VT1XX-EA/EB Asynchronous Port Cables

The VT1XX-EA/EB asynchronous ports may work in conjunction with several peripheral device cables and options, thus providing great flexibility when configuring systems. Figure 1-12 shows the possible cables and options used with the VT1XX-EA/EB asynchronous ports as well as the primary application of each.

NOTE

The VT1XX-EA and VT1XX-EB are not supplied with cables. All cables shown in Figure 1-12 are options.

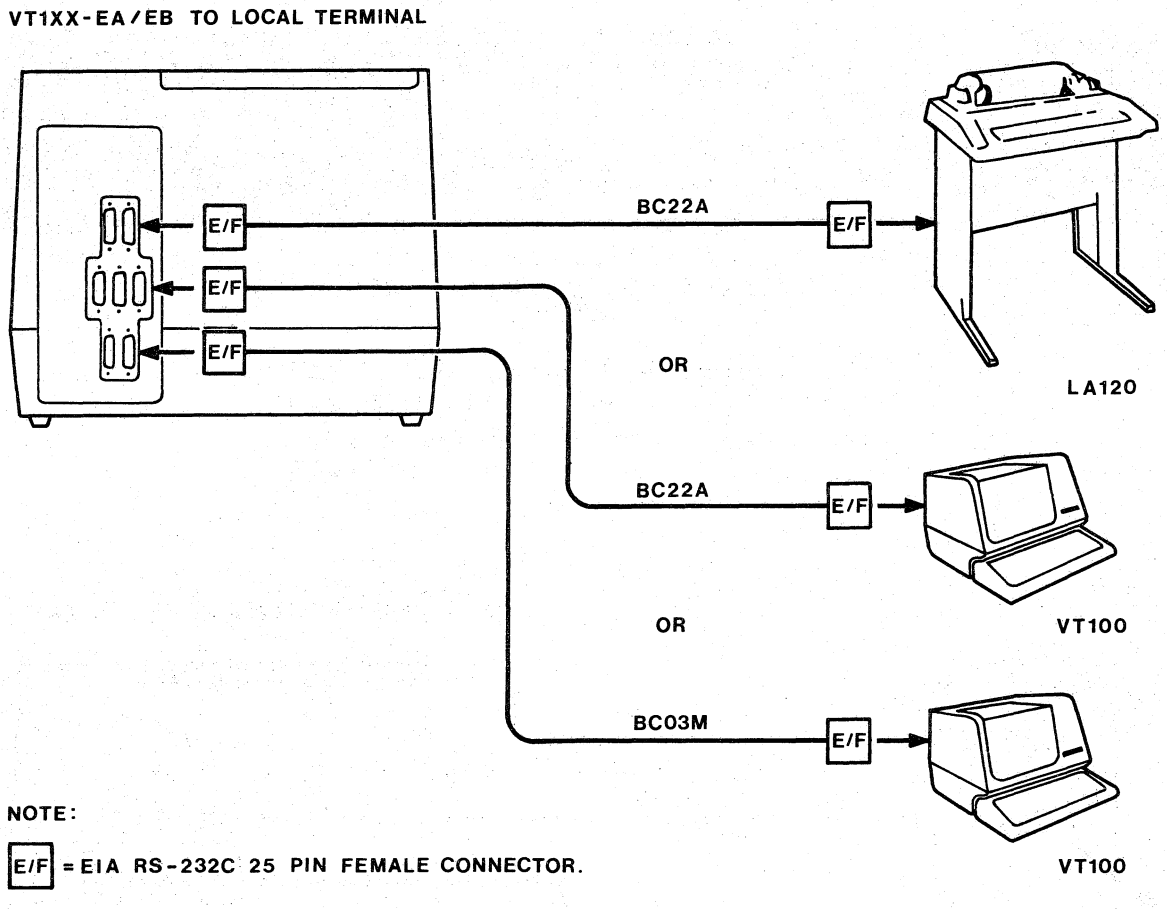
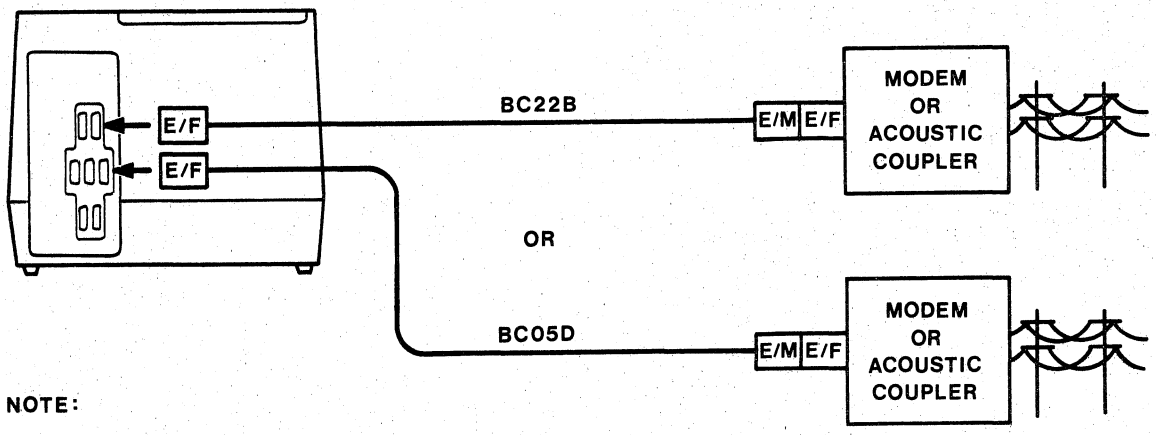


Figure 1-12 VT1XX-EA/EB Asynchronous Port Cables
(Sheet 1 of 2)

VT1XX-EA/EB TO MODEM OR ACOUSTIC COUPLER



NOTE:

E/F = EIA RS-232C 25 PIN FEMALE CONNECTOR.
E/M = EIA RS 232C 25 PIN MALE CONNECTOR.

Figure 1-12 VT1XX-EA/EB Asynchronous Port Cables
(Sheet 2 of 2)

CHAPTER 2

INSTALLATION

2.1 SCOPE

This chapter provides the necessary information for configuring, installing, testing and acceptance of the DZS11-EA Statistical Multiplexer.

2.2 UNPACKING AND INSPECTION

The DZS11-EA is packaged according to commercial packing practices. When unpacking, remove all packing material and check the equipment against the shipping list (Appendix A). Inspect all parts and carefully inspect the module for cracks, loose components and separation in the etched paths. Report damages or shortages to the shipper and notify the DEC representative.

2.3 INSTALLATION CONSIDERATIONS

Installation of the DZS11-EA statistical multiplexer should be done in four phases:

- Phase 1 - Pre-installation Considerations.
  Verify system requirements, system placement, and network requirements.

- Phase 2 - DZS11-EA Module Installation.
  Configure, install module, cable, and verify via appropriate diagnostic.

- Phase 3 - VT1XX-EA/VT1XX-EB Installation.
  Install in accordance with Chapter 2 of VT1XX-EA/EB option description, and verify via appropriate microdiagnostics.

- Phase 4 - DZ11 Stat Mux Network Testing.
  Verify the DZ11 Stat mux network (including DZS11-EA and VT1XX-EA and/or VT1XX-EB) operation with the functional diagnostics and network exercise programs.

2.4 PRE-INSTALLATION CONSIDERATIONS

The following should be considered prior to ordering a DZS11-EA Statistical Multiplexer to ensure that the system can accept the device and that it can be installed correctly. The steps should also be verified at installation time.

2.4.1 Device Placement

The DZS11-EA requires one hex-height, small peripheral controller (SPC) backplane slot. Any SPC backplane (DD11-B (REVE) or later) can accept the DZS11-EA. The DZS11-EA is a bus request (BR) device and should therefore be placed on the UNIBUS following NPR devices.

2.4.2 System Requirements

2.4.2.1 UNIBUS Loading

1 UNIBUS dc load
1 UNIBUS ac load

2.4.2.2 Power Requirements

Check the power supply loading before and after installation to ensure against overloading. The DZS11-EA total current requirement for the +5V supply is approximately 3.5 ampers. Additionally the unit requires ± 15 volts for the silos, and communication port, level conversion logic.
Power requirements for the DZS11-EA, are listed in Table 2-1.

Table 2-1 DZS11-EA Voltage Chart

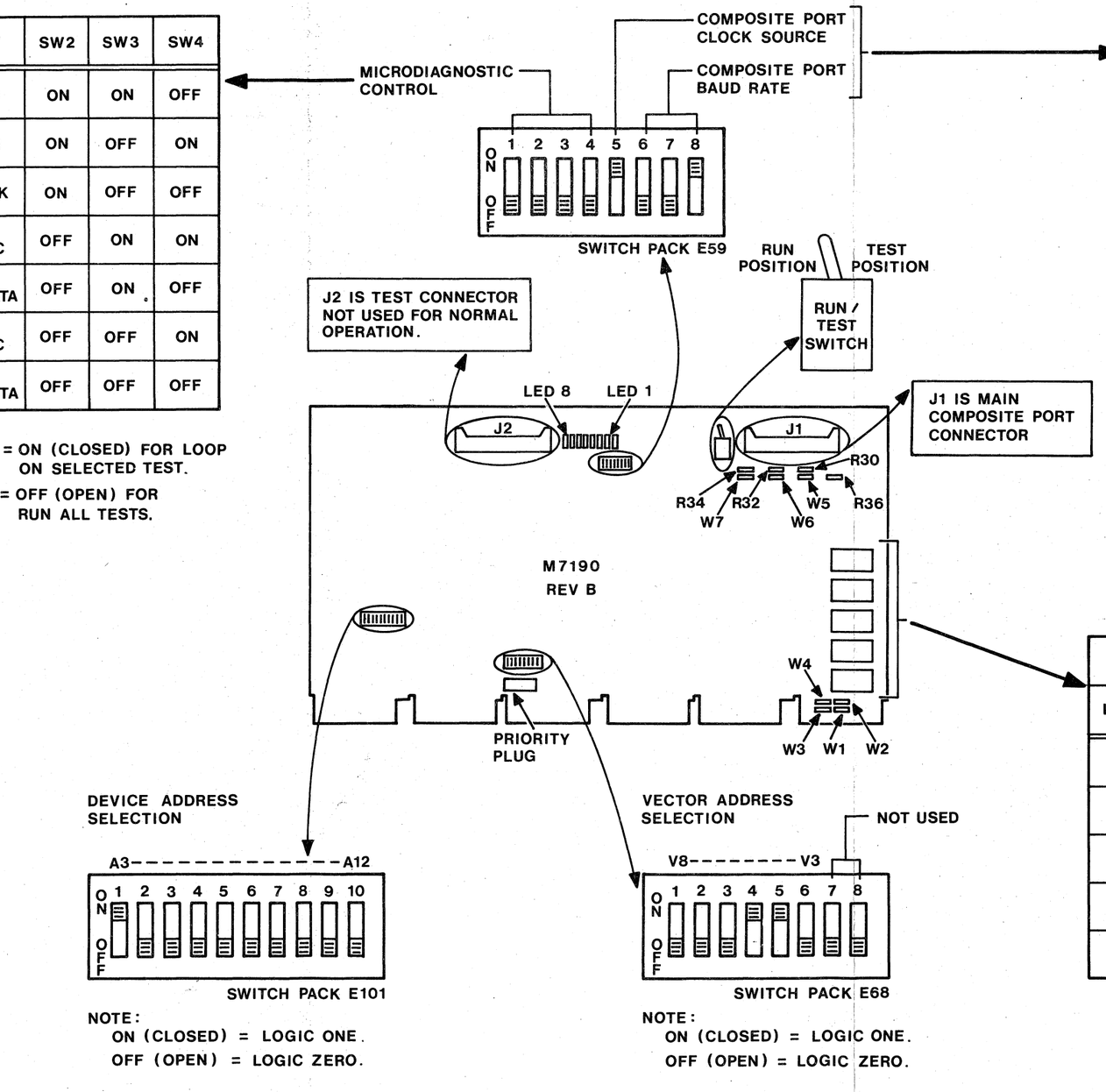
Voltage Rating	Maximum Voltage	Minimum Voltage	Back Plain Pin
+5 Volts @ 3.5A	5.25	+5.Ø	C1A2
+15 Volts @ Ø.Ø7A	+15.75	+14.25	C1U1
-15 Volts @ Ø.Ø8A	-15.75	-14.25	C1B2

2.4.2.3 Interrupt Priority

The interrupt priority is selected by priority plug E67 on the M719Ø Module. This plug is preset to select priority five (BR5). Refer to Figure 2-1 for the priority plug location.

TEST	SW2	SW3	SW4
ROM	ON	ON	OFF
RAM	ON	OFF	ON
CLOCK	ON	OFF	OFF
X.25 LOGIC	OFF	ON	ON
X.25 INT. DATA	OFF	ON	OFF
DMA LOGIC	OFF	OFF	ON
X.25 EXT. DATA	OFF	OFF	OFF

NOTE:
SW 1 = ON (CLOSED) FOR LOOP ON SELECTED TEST.
SW1 = OFF (OPEN) FOR RUN ALL TESTS.



BAUD RATE	SW 6	SW 7	SW 8
1200	ON	ON	ON
1800	ON	ON	OFF
2400	ON	OFF	ON
3600	ON	OFF	OFF
4800	OFF	ON	ON
7200	OFF	ON	OFF
9600	OFF	OFF	ON
19200	OFF	OFF	OFF

NOTE:
SW5 = ON (CLOSED) SELECTS EXTERNAL CLOCK.
SW5 = OFF (OPEN) SELECTS INTERNAL CLOCK.

EPROM LOCATION	
LOCATION	PART NUMBER
E5	23 - 289E2 - 04
E4	23 - 290E2 - 04
E3	23 - 291E2 - 04
E2	23 - 292E2 - 04
E1	NOT USED

NOTE:
ON (CLOSED) = LOGIC ONE.
OFF (OPEN) = LOGIC ZERO.

NOTE:
ON (CLOSED) = LOGIC ONE.
OFF (OPEN) = LOGIC ZERO.

Figure 2-1 DZS11-EA Component and Jumper Configuration Summary

2.4.2.4 Device Address Assignment

The DZS11-EA resides in the floating address space of the input/output (I/O) page of memory. The ranking assignment of the DZS11-EA is equal to the DZ11-A, ranking number 8.

The selection of the device address is accomplished by Switch Pack E1Ø1 on the M719Ø module. Refer to Figure 2-1 for the switch pack placement.
Refer to Appendix B for further information on the floating address allocation.

2.4.2.5 Device Vector Address Assignment

The DZS11-EA resides in the floating vector space of the reserved vector area of memory. The ranking assignment of the DZS11-EA is equal to the DZ11-A ranking number 28. The selection of the device vector address is accomplished by Switch Pack E68 on the M719Ø module. Refer to Figure 2-1 for the location of the switch pack. Appendix B contains more information on floating vector allocation.

2.4.3 Composite Port Requirements

2.4.3.1 Composite Port Cable Requirements

The DZS11-EA composite port (M719Ø J1) can be configured for signal line compatibility with EIA RS-232C, RS-423, or RS-422 type long line driver. The port meets both EIA RS-232C and RS-423 requirements simultaneously, however component changes are necessary to implement the RS-422 type long line driver.

When interconnecting equipment that meets compatible, but different EIA standards, the performance of the channel is limited by the least efficient EIA specification. Specifically EIA RS-232C/RS-423 mixed connections are limited to EIA RS-232C performance capabilities and EIA RS-423/RS-422 mixed connections are limited to EIA RS-423 performance capabilities. This consideration is critical when choosing baud rates and cable lengths for the DZS11-EA composite port. Figure 2-2 gives the relationship between baud rate and cable length for both EIA RS-423 and RS-422 specifications. Remember, when connecting equipment that adheres to EIA RS-232C specifications, the baud rate is limited to 19.2K bits per second with a maximum cable length of 5Ø feet.

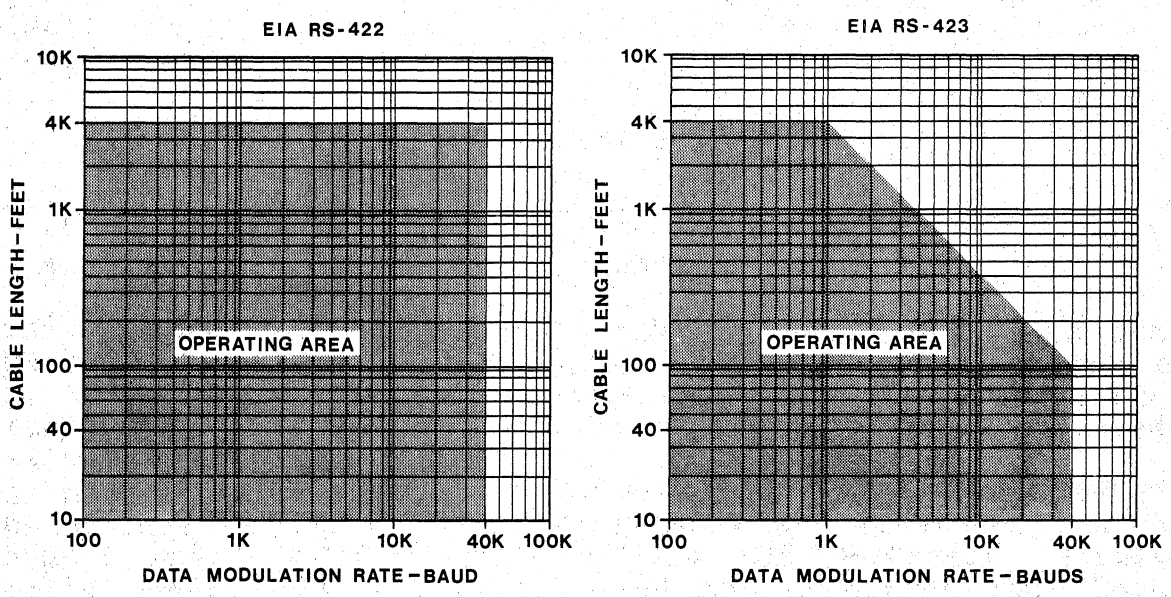


Figure 2-2 Baud Rate vs Cable Length

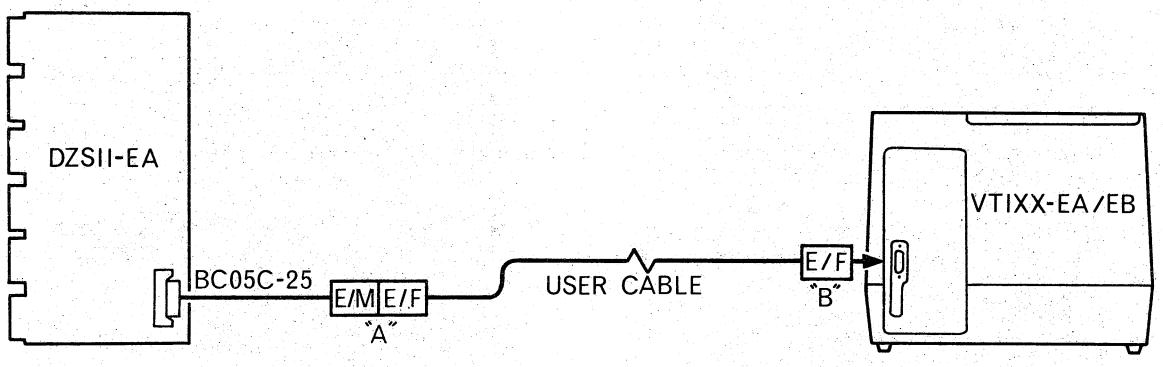
2.4.3.2 EIA RS-232C AND EIA RS-423

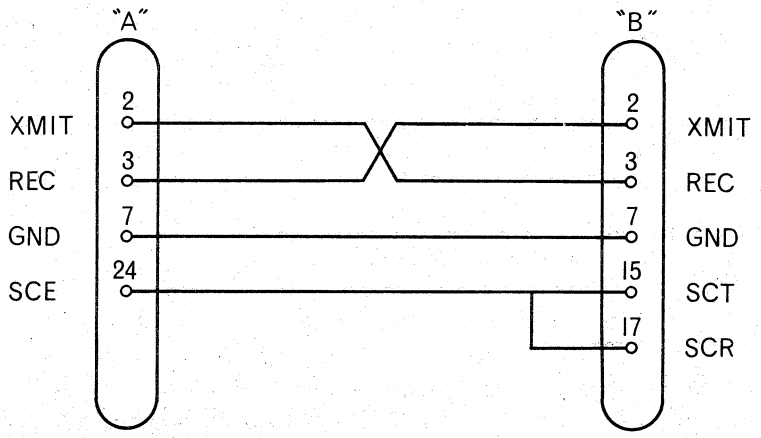
The DZS11-EA is shipped conforming to both EIA RS-423 and RS-232C standards simultaneously. If the composite port is to be connected to a EIA RS-232C compatible modem using the supplied BCØ5C-25 cable then cable length should be limited to the 25 foot supplied.

In network configurations where the cabling distance between components of the DZ STAT MUX network are relatively short and/or where modem connections are not necessary, direct cable connections are possible on the condition that both cable length and operating baud rate conform to the chart shown in Figure 2-2 for EIA RS-423 interconnections.

This type of interconnection will require the fabrication of a special interconnect cable, however component changes on the the DZS11-EA module will not be necessary.

Figure 2-3 shows the necessary interconnections for both the Main and Route-through composite links for direct cable connections. Figure 2-4 shows the cable requirements for a modem connection.



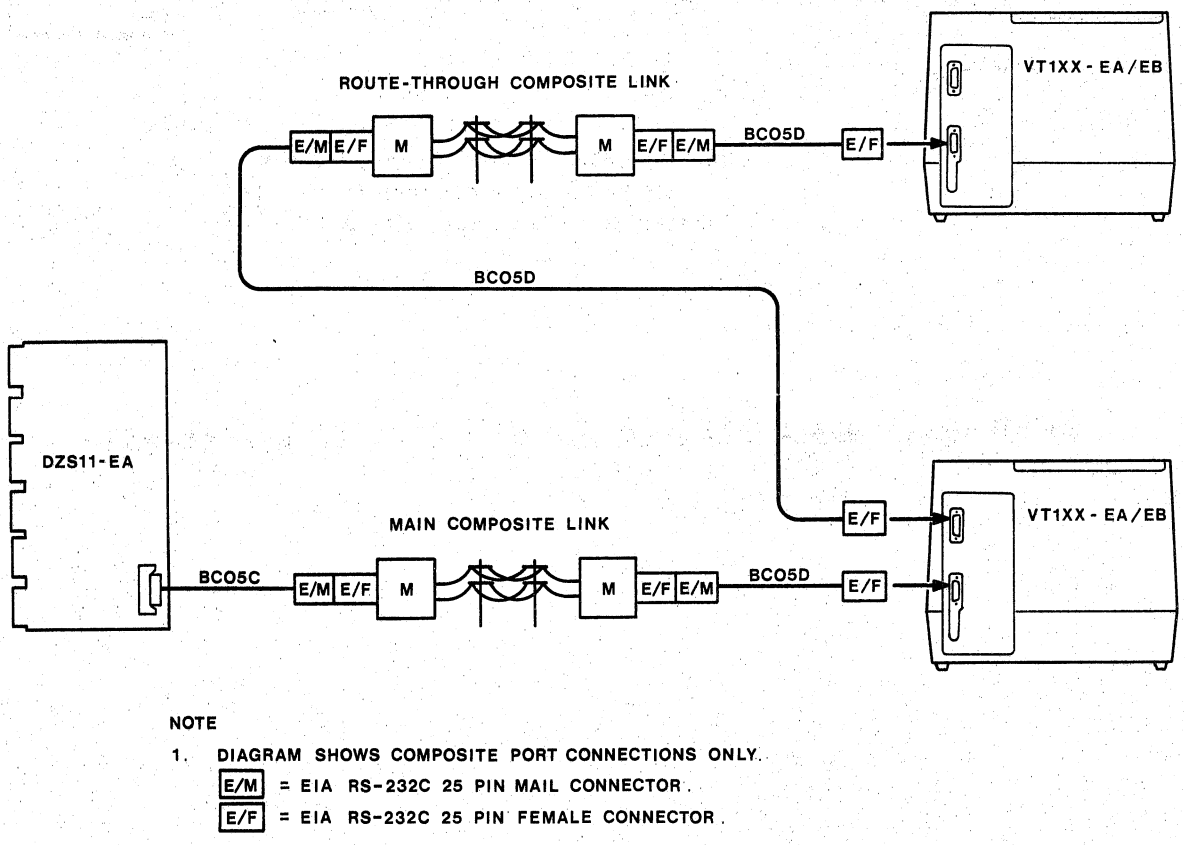


MAIN LINK RS 423 CABLE INTERCONNECTIONS

NOTE

E/M = EIA RS-232C 25 PIN MALE CONNECTOR
E/F = EIA RS-232C 25 PIN FEMALE CONNECTOR

Figure 2-3 DZ STAT MUX EIA RS-423 Direct Cable Connection



NOTE

1. DIAGRAM SHOWS COMPOSITE PORT CONNECTIONS ONLY.
   E/M = EIA RS-232C 25 PIN MAIL CONNECTOR.
   E/F = EIA RS-232C 25 PIN FEMALE CONNECTOR.

Figure 2-4 DZ STAT MUX EIA RS-232C Modem Connection

2.4.3.3 EIA RS-423, RS-232C Slew Rates

The signal rise and fall time may be controlled on the composite port when configured for EIA RS-423 or RS-232C standards. Configuration is by installing (soldering) an appropriate value of non-wirewound, 1/4W resistor into the wave-shaping resistor pads provided (R36). An appropriate resistor value can be selected by referring to Table 2-2. The DZS11-EA is shipped with a 22K ohm resistor installed enabling the composite port to operate at any of the specified baud rates over a cable distance of 100 feet.

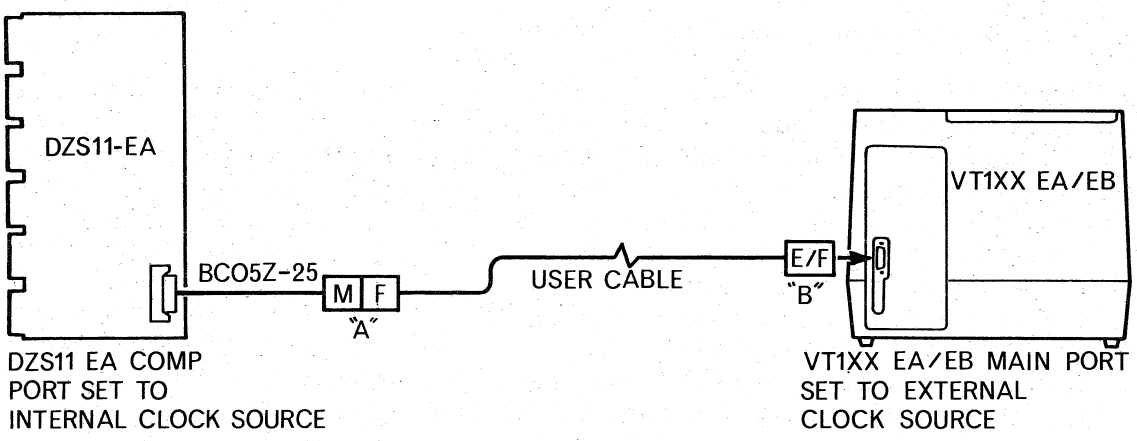
Table 2-2 EIA RS-423 and RS-232C
Wave Shaping Resistor Values

BAUD RATE	RESISTOR VALUE
19.2K	51 000 ohms
9.6K	120 000 ohms
4.8K	200 000 ohms
2.4K	430 000 ohms
1.2K	820 000 ohms

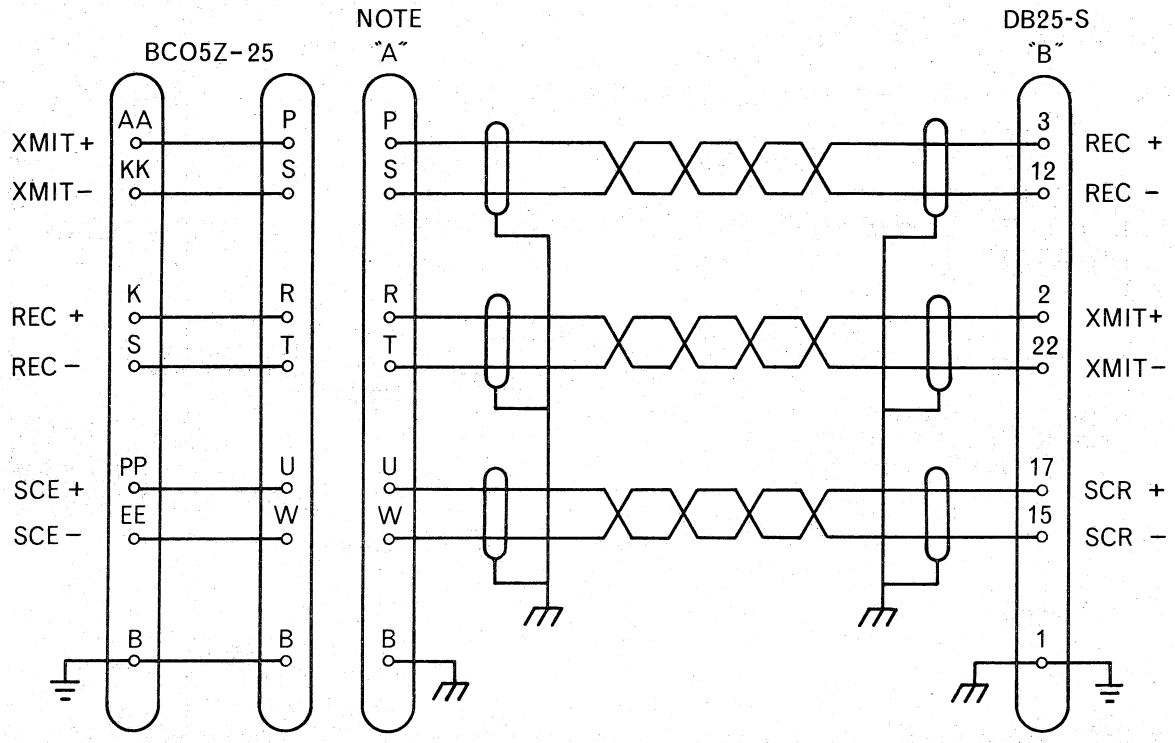
2.4.3.4 EIA RS-422 Long Line Driver

In network configurations where direct connections are required, however baud rate and/or cable length is beyond that specified for EIA RS-423 operation shown in Figure 2-2, then the integral long line driver may be configured. The long line driver utilises RS-422 full differential transceivers and conforms to the baud rate and cable distance specification shown in Figure 2-2.
The modification requires component changes on the DZS11-EA module plus the supply of a special user interconnect cable. The interconnection should be made as shown in Figure 2-5 using cable conforming to the following specifications:-

- 3 twisted pairs, individually shielded 22 to 24 gauge wire.
- Mutual capacitance < 20 pf/foot.
- Stray capacitance < 40 pf/foot.
- Resistance < 30 ohms/1000 feet.



MAIN COMPOSITE LINK CONNECTION

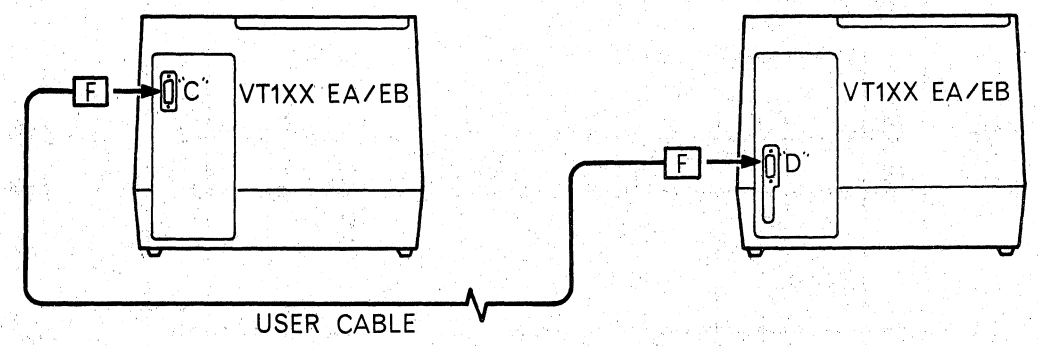


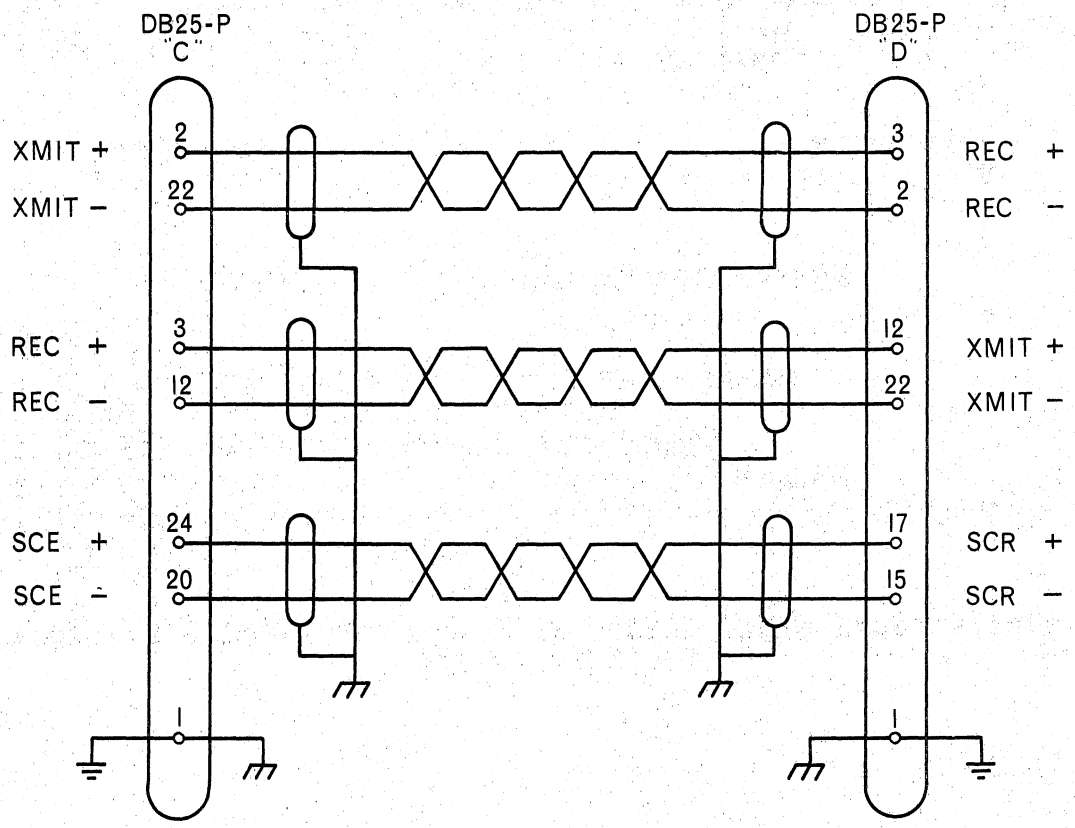
MAIN LINK RS422 CABLE INTERCONNECTIONS

NOTE

CONNECTOR (A) DEC PART NUMBERS ARE AS FOLLOWS
12-13033-00 CONNECTOR BODY.
12-10290-01 SOCKET CONTACT.
12-13032-0 HOOD.

Figure 2-5 DZS11-EA Long Line Driver Cable Requirements (Sheet 1 of 2)





ROUTE-THROUGH RS422 CABLE INTERCONNECTIONS

NOTE:

1. IT IS MANDATORY THAT CABLE SHIELD BE ELECTRICALLY CONNECTED TO THE CHASSIS AT THE ENTRY POINT.
2. SET DZS11-EA PORT TO INTERNAL CLOCK SOURCE.
3. SET VT1XX-EA/EB MAIN PORT TO EXTERNAL CLOCK SOURCE.
4. SET VT1XX-EA/EB ROUTE-THROUGH PORT TO INTERNAL CLOCK SOURCE.

F = DB25-P FEMALE CONNECTOR.

Figure 2-5 DZS11-EA Long Line Driver Cable Requirements (Sheet 2 of 2)

2.4.4 Composite Port Clock Source

The DZS11-EA composite port contains three interface clock signals. Two of these signals are received by the DZS11-EA and supply the Receive and Transmit timing for the port. The DZS11-EA monitors these two signals only when external timing is selected. Refer to Figure 2-1 for DZS11-EA composite port clock source DIL switch location and setting.
The third signal is a clock out signal. The DZS11-EA transmits a square wave signal on this conductor equal in frequency to the composite port baud rate set on the baud rate switch pack 5-9 shown in Figure 2-1.

The DZS11-EA composite port is normally set to external timing when connection is made via modems and set to internal, when connection is by direct cable connection.

2.4.5 Composite Port Baud Rate

When the DZS11-EA composite port is set for external timing source, the operational baud rate is determined by the external timing source.
When the DZS11-EA composite port is set for internal timing source the operational baud rate is determined by an on board baud rate generator. The frequency of this baud rate generator is set by the baud rate DIL switch E59, refer Figure 2-1.

NOTE
The composite port baud rate DIL switch E59 must always be set to equal the composite port operational baud rate, independently of the clock source switch settings. The baud rate value is required by the DZS11-EA microcode to dynamically modify the component port algorithm.

2.4.6 Microdiagnostic Controls

The on board microdiagnostics are controlled by two switches and are shown in Figure 2-1. They are the RUN/TEST Switch and microdiagnostics control DIL switch E59.
The RUN/TEST switch select either DZ STAT MUX operational code or the on board diagnostics. Normal operation, DZ STAT MUX code, is with this switch in the RUN position. The microdiagnostic DIL switch enables the microdiagnostic to run through all microdiagnostic sub-tests or the continuous operation of a selected test. Normal operation is with E59 SW1 in the OFF (OPEN) position.

2.5 M7190 CONFIGURATION

Perform the following checks on the DZS11-EA M7190 module.

2.5.1 Check Factory Configured Components

Verify that jumpers W1, W2, W3, W4 and W8 are installed correctly (Refer to component and configuration Summary Table 2-3 and Figure 2-1).

2.5.2 Check Socketed Devices

Verify that all socketed devices are properly seated in their respective sockets. (Refer to Figure 2-1).

2.5.3 Set Device UNIBUS Address

Configure Switch Pack E101 to implement the correct device address for the DZS11-EA as determined from the floating address allocation. Refer to Table 2-4 for the correlation between switch number and address bit. A switch ON (closed) responds to a logic one on the UNIBUS. Refer to Appendix B for additional information on floating address allocation.

2.5.4 Set Device Vector Address

Configure switch pack E68 to implement the correct vector address for the DZS11-EA as determined from the floating vector allocation. Refer to Table 2-5 for the correlation between switch numbers and vector bit. A switch ON (closed) responds to a logical one on the UNIBUS. Refer to Appendix B for additional information on floating vector allocation.

2.5.5 Check Priority Plug

Verify that the priority plug is a BR5 and is installed correctly in location E67.

2.5.6 Check Composite Port Signal Conditioning Components

Verify that the composite port signal conditioning components, W5, W6, W7, R30, R32, R34 and R36 are selected and installed in accordance with Table 2-2 and Section 2.4.3.

2.5.7 Set Composite Port Baud Rate

Configure switch pack E59 to implement composite port timing source and operational baud rate.

NOTE

DZS11-EA composite port baud rate must be set on switch pack E59. The value set in this switch is used by the microcode to control the composite port algorithm.

2.5.8 Set RUN/TEST Switch

Verify that the M7190 maintenance switch is set to the (RUN) position, enabling normal operation.

Table 2-3 Component Configuration Summary

Component	Normal Configuration	Function
W1	IN	Rom sockets E5 and E4 (Roms Ø and 1) configured for 2K X 8 bit devices.
W2	IN	Rom sockets E3 and E2 (Roms 2 and 3) configured for 2K X 8 bit devices.
W3	OUT	Rom sockets E5 and E4 (Rom Ø and 1) configured for 4K X 8 bit devices.
W4	OUT	Rom sockets E3 and E2 (Roms 2 and 3) configured for 4K X 8 bit devices.
W5 W6 W7	IN IN IN	Enables serial port receivers to operate in RS-423 or RS-232C mode when installed. When removed enables receiver to operate in RS-422 mode. See also R3Ø, R32, R34 and R36.
W8	IN	Oscillator Enable - To be removed only for factory automatic testing. Jumper should always be installed in field.
R3Ø R32 R34	OUT OUT OUT	RS-422 Termination Resistors. They are 1ØØ ohm 1/4 W, non wire wound fusible resistors and are installed only when RS-422 operation is required. Normal operation (RS-423; RS-232C) requires that these devices not be installed.

Table 2-3 Component Configuration Summary cont:

Component	Normal Configuration	Function
R36	IN (22 Kohms)	Wave shaping resistor. (Slew rate). Required for RS-423 and RS-232C operation only. This resistor determines the serial port transmitter slew rate. Refer Section 2.4.3.2.
NOTE W1 and W3 are mutually exclusive. Only one or the other can be installed, not both. Similarly W2 and W4 are mutually exclusive.		

Table 2-4 UNIBUS Address Selection (E1Ø1)

Switches	FUNCTION
1-1Ø	UNIBUS device address selection:

NOTE

Switch On equals a logic one (1) on the UNIBUS

MSB LSB

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	SWITCH PACK E101										0	0	0

SWITCH NUMBER	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1	DEVICE ADDRESS
										ON	760010
									ON		760020
									ON	ON	760030
								ON			760040
								ON		ON	760050
								ON	ON		760060
								ON	ON	ON	760070
							ON				760100
											- - -
						ON					760200
											- - -
						ON	ON				760300
											- - -
					ON						760400
											- - -
					ON		ON				760500
											- - -
					ON	ON					760600
											- - -
					ON	ON	ON				760700
											- - -
				ON							761000
											- - -
			ON								762000
											- - -
			ON	ON							763000
											- - -
		ON									764000

NOTE: SWITCH ON RESPONDS TO LOGICAL ONE ON THE UNIBUS

SWITCH PACK E101
DEVICE ADDRESS
SELECTION

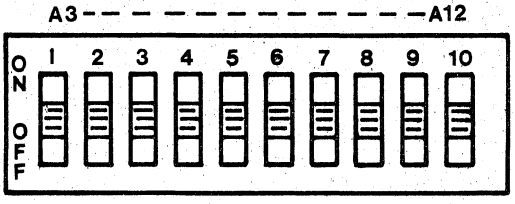


Table 2-5 UNIBUS Vector Selection (E68)

Switches	FUNCTION
1-8	Vector Address Selection

NOTE

SWITCH ON equals a logic one (1) on the UNIBUS

MSB LSB

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	SWITCH PACK E68						1/0	0	0

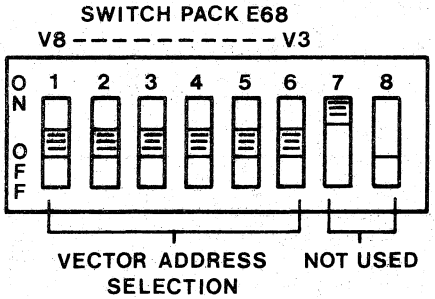
SWITCH NUMBER	S1	S2	S3	S4	S5	S6	VECTOR ADDRESS
		ON	ON				300
		ON	ON			ON	310
		ON	ON		ON		320
		ON	ON		ON	ON	330
		ON	ON	ON			340
		ON	ON	ON		ON	350
		ON	ON	ON	ON		360
		ON	ON	ON	ON	ON	370
	ON						400

	ON		ON				500

	ON	ON					600

	ON	ON	ON				700

NOTE: SWITCH ON PRODUCES LOGICAL ONE ON THE UNIBUS.



2.6 DZS11-EA MODULE INSTALLATION

2.6.1 Backplane considerations.

Perform the following checks on the SPC slot that will contain the DZS11-EA, M7190 module.

- Verify that the backplane voltages are within the specified tolerances listed in Table 2-1.

2.6.2 M7190 Insertion

Carefully insert the M7190 statistical multiplexer into the selected SPC slot and perform the following tasks:-

1. Perform resistance checks on the backplane voltage sources to ground to ensure that no short circuit conditions exist on the module. Refer to Table 2-1 for backplane pin assignments.

2. Insert the module test connector (H883) into J1 of the M7190. Refer to Figure 2-1 for J1 location. Be sure to insert with "Side-1" (etched on the test connector) visible from the component side of the M7190.

   Schematics and outline drawings of DZS11-EA test connectors are provided in Figure 2-6.

3. Turn system power ON and verify that backplane voltages are within the specified tolerance listed in Table 2-1.

2.7 DZS11-EA M7190 TEST

2.7.1. Initialise DZS11-EA

Initialise the DZS11-EA (M7190). This is achieved either by system initialisation in the form of BUS INIT; or device initialisation. Refer Table 3-3 for device initialisation.

2.7.2 Run the On Board Microdiagnostic

Set the M7190 maintenance switch to the TEST position. Refer to Figure 2-1 for maintenance switch location.
The M7190 microcontroller will commence execution of the on board microdiagnostic. LED 7 will be ON and LED 6 will be OFF. Leds 5, 4, and 3 will indicate the sub test being executed and LED 2, 1, and 0 will indicate microdiagnostic errors if detected. Allow the microdiagnostic to complete at least two error free end passes. Microdiagnostic passes are indicated by LEDs 5, 4, and 3 incrementing from sub test 7 to sub test 1. Refer to APPENDIX C for microdiagnostic description.

2.7.3. Load and Run the UNIBUS Diagnostic

Set the M7190 maintenance switch to the RUN position and leave the H883 test connector in J1 (composite port socket) of the M7190. At completion of the current microdiagnostic pass, the microcontroller will switch from OFF LINE microdiagnostic to UNIBUS microdiagnostic. (LED 7 ON, LED 6 ON). Load and execute the appropriate UNIBUS diagnostic as detailed in Section 5 of this document.
Upon obtaining a minimum of five error free END passes of the UNIBUS diagnostics proceed with step 4.

NOTE

THE H883 test connector must be installed in J1 to enable the UNIBUS microdiagnostic code.

2.7.4. Test the BC05C-25 Cable

At this point the M7190 module has been tested as far as the serial I/O connector. The next step is to install and test the I/O cable.

Remove the (H883) test connector from J1.

Install the I/O cable (DC05C-25) with the 40 pin berg connector mating with J1 of the M7190 module. Be sure to install with the "THIS SIDE UP" sticker visible from the component side of the M7190.

Install the H325 test connector into the DB25P end of the BC05C-25 cable.

Restart the M7190 on board microdiagnostics by moving the maintenance switch S1 (Refer Figure 2-1) into the test position. The microdiagnostic will now exercise the I/O cable.

Upon obtaining a minimum of five error free passes of the microdiagnostic, move the RUN/TEST switch into the RUN position, remove the H325 test connector and connect the DB25-P connector end of the BC05C-25 cable to the modem. Finally, re-initialise the DZS11-EA as in Section 2.7.1 and proceed with next section.

Table 2-6 Microdiagnostic Switch Pack (E59)

<table>
<tr><th>Switches</th><th>FUNCTION</th></tr>
<tr><td>1</td><td>NOTE
Switch OFF (open) equals a logic one (1).
When OFF (open), will select on board microdiagnostic sub test for continuous operation. The test number is determined by switches 2, 3 and 4 as specified below.
This switch is enabled by the RUN/TEST switch, see Figure 2-1.
When RUN/TEST switch is in the RUN position this switch is disabled. When RUN/TEST switch is in the TEST position this switch is enabled.</td></tr>
<tr><td>2:4</td><td>Microdiagnostic test number, selects one of 7 microdiagnostics for continuous operation. Enabled by switch 1 of E59.

<table>
<tr><th>TEST DESCRIPTION</th><th>SW2</th><th>SW3</th><th>SW4</th></tr>
<tr><td>ROM TEST</td><td>ON</td><td>ON</td><td>OFF</td></tr>
<tr><td>RAM TEST</td><td>ON</td><td>OFF</td><td>ON</td></tr>
<tr><td>CLOCK TEST</td><td>ON</td><td>OFF</td><td>OFF</td></tr>
<tr><td>X.25 LOGIC TEST</td><td>OFF</td><td>ON</td><td>ON</td></tr>
<tr><td>X.25 INT. DATA</td><td>OFF</td><td>ON</td><td>OFF</td></tr>
<tr><td>DMA LOGIC TEST</td><td>OFF</td><td>OFF</td><td>ON</td></tr>
<tr><td>X25 EXT. DATA</td><td>OFF</td><td>OFF</td><td>OFF</td></tr>
</table></td></tr>
</table>

Table 2-7 Composite Port Parameter Switch Pack (E59)

<table>
<tr><th>Switches</th><th>FUNCTION</th></tr>
<tr><td>5</td><td>Serial port clock source. When OFF (open) enables the serial communication port to be timed from the internal clock source.
When ON (closed) enables serial communication port timing to be derived from an external source (normally modem) via the serial I/O connector J1.</td></tr>
<tr><td>6:8</td><td>Baud Rate Selection. Used to select one of 8 baud rates for the composite communication port.

NOTE

These switches must be set to the operational baud rate even if external timing is selected (E59-5 OFF).

<table>
<tr><th>Baud Rate</th><th>SW6</th><th>SW7</th><th>SW8</th></tr>
<tr><td>1200</td><td>ON</td><td>ON</td><td>ON</td></tr>
<tr><td>1800</td><td>ON</td><td>ON</td><td>OFF</td></tr>
<tr><td>2400</td><td>ON</td><td>OFF</td><td>ON</td></tr>
<tr><td>3600</td><td>ON</td><td>OFF</td><td>OFF</td></tr>
<tr><td>4800</td><td>OFF</td><td>ON</td><td>ON</td></tr>
<tr><td>7200</td><td>OFF</td><td>ON</td><td>OFF</td></tr>
<tr><td>9600</td><td>OFF</td><td>OFF</td><td>ON</td></tr>
<tr><td>19200</td><td>OFF</td><td>OFF</td><td>OFF</td></tr>
</table>
</td></tr>
</table>

2.8 VT1XX-EA/VT1XX-EB INSTALLATION

The next step in the installation and test procedures of the DZ Stat mux network is to install and test the remote VT1XX-EA and or VT1XX-EB multiplexers.

Detailed steps of this procedure are given in the VT1XX-EA/EB Option Description.

2.9 DZ STAT MUX NETWORK TESTING

At this point all network components, including DZS11-EA, VT1XX-EA, and/or VT1XX-EB, have been installed and tested as far as their composite communication port connectors.
Perform the following steps to complete the network installation and test.

2.9.1. Set DZS11-EA into RUN Mode

Set the M7190 maintenance switch into the RUN position.
The microcontroller will now execute the main DZS11-EA microcode. LED 7 and LED 6 will start a rotating bit pattern.

2.9.2 Connect DZS11-EA to DZ STAT MUX Network

Remove the H325 test connector from the BC05C-25 cable. Connect the DB25-P end of the BC05C-25 cable to the network communication medium. In most instances this will be a modem, in short hall applications this will be a direct interconnecting cable to the VT1XX-EA/EB. Refer Section 2.4.3.

2.9.3. Test DZ STAT MUX Composite Link

The next step is to test continuity and integrity of the communication link.
This is done by running the OFF LINE microdiagnostic, this time through the network.
Test 7 of the microdiagnostic is a X.25 external communication test.
The microdiagnostic transmits specially sequenced and formatted X25 frames, expecting to receive them within a time out period for information verification. Normally the test frame is looped back to the DZS11-EA by a test connector in the form of H883 or H325. Similarly test frames can be looped back by a modem in test or by an operational VT1XX-EA/EB at the remote site. This feature enables the DZS11-EA network to be tested either completely (from DZS11-EA to VT1XX-EA/EB and return to DZS11-EA) or in incremental steps using loop back connectors.
In a similar manner, the DZS11-EA will loop back a test frame received from the remote VT1XX-EA/EB. This feature enables testing of the network without having to visit both locations.

1. Set the M7190 maintenance switch to the TEST position and allow the OFF LINE microdiagnostic to run for at least five end passes. If errors are detected by sub test 7 it will be necessary to eliminate the faulty section or sections of the communication network. To do this the network should be tested at incremental stages through the communications network by using appropriate loop back connectors. On completion of five end passes proceed.

2. Set the M7190 maintenance switch to the RUN position.
   At completion of the current microdiagnostic pass, the microcontroller will switch to the main operational code. LEDs 7 and 6 will now commence a rotating bit pattern.

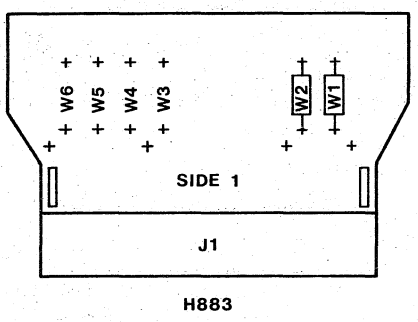
2.1Ø CUSTOMER ACCEPTANCE

In most communication networks, transmission errors are experienced, thus the reason for high level data link protocols employing redundancy checks with re-transmission on error detection. The exact quantity of transmission errors depends on the transmission medium quality. A good transmission medium would have errors less than one per hour, a bad network could experience several over the same period. Customer acceptance cannot therefore be based on successful transmission over a network outside of the direct control of Digital Equipment Corporation.

Customer acceptance constitutes the successfull completion of sections 2.7, 2.8, and 2.9 of this document. However in situations where transmission error rates in section 2.9.3 are untenable then customer acceptance will consist of one of the following:-

a) Successful completion of sections 2.7, 2.8, and 2.9 with faulty transmission medium removed, i.e. DZS11-EA and VT1XX-EA/EB back to back using a modem eliminator.

b) Successful completion of sections 2.7, 2.8, and 2.9.1 and 2.9.2 with the faulty transmission medium connected.



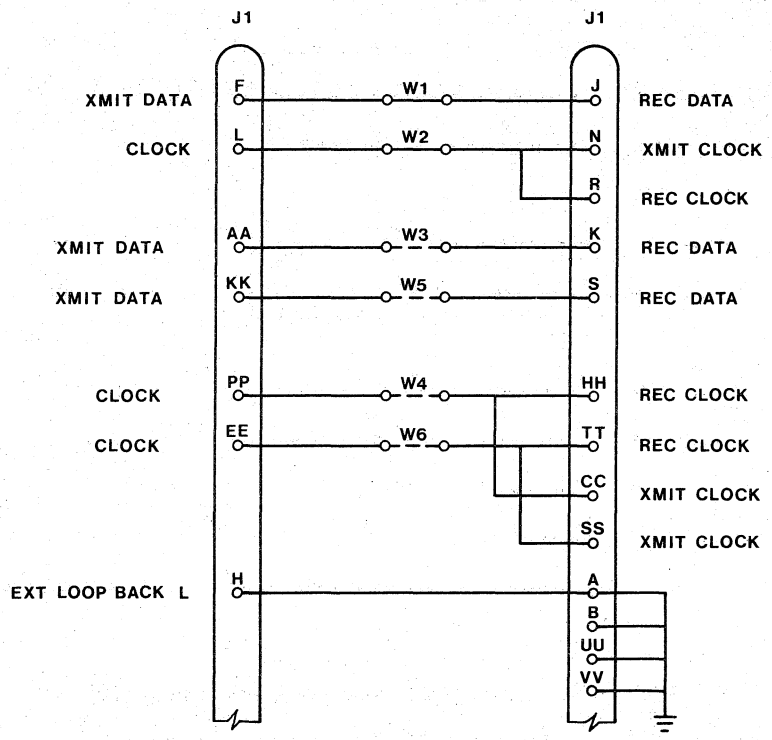


Figure 2-6 DZS11-EA Turnaround Test Connectors
(Sheet 1 of 3)

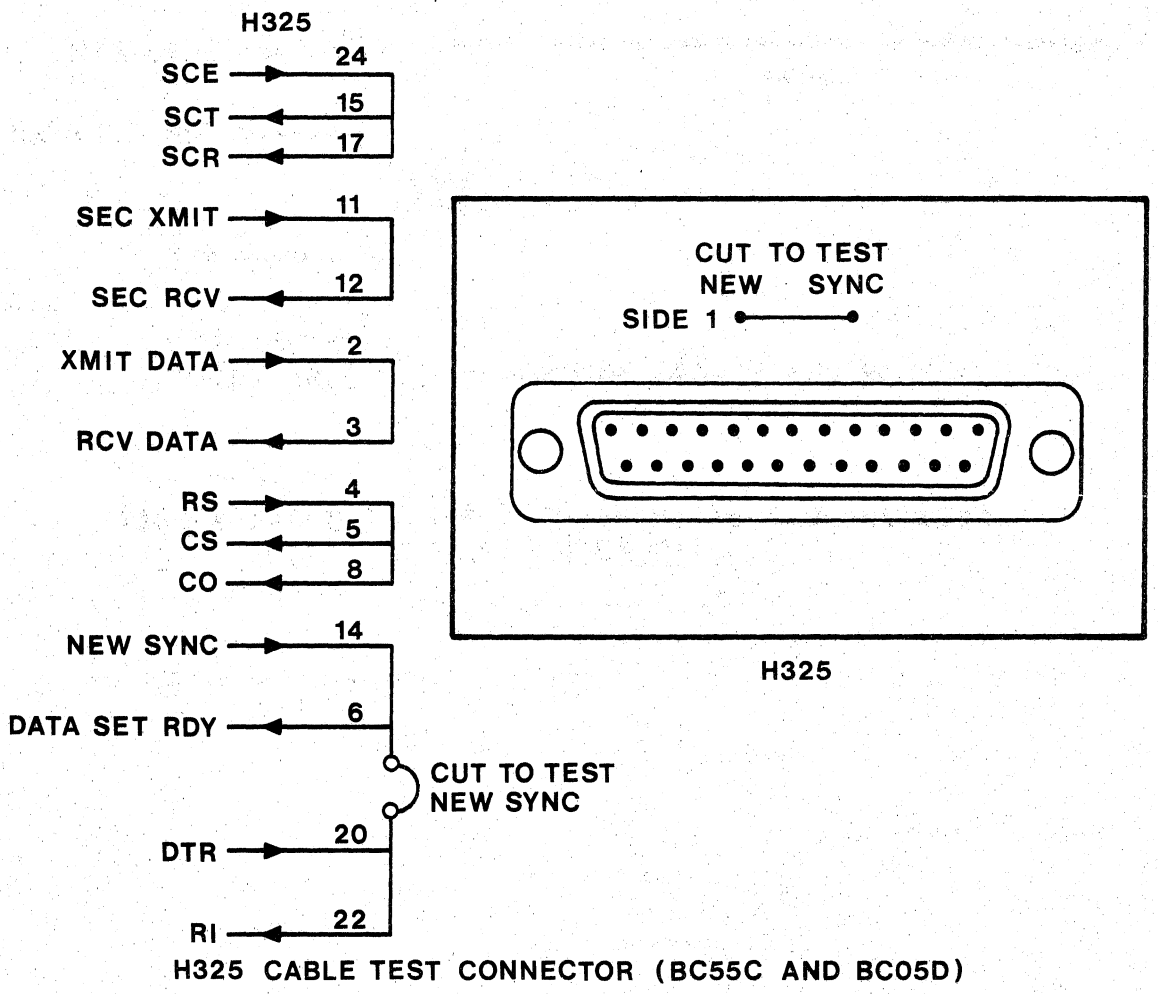


Figure 2-6 DZS11-EA Turnaround Test Connectors
(Sheet 2 of 3)

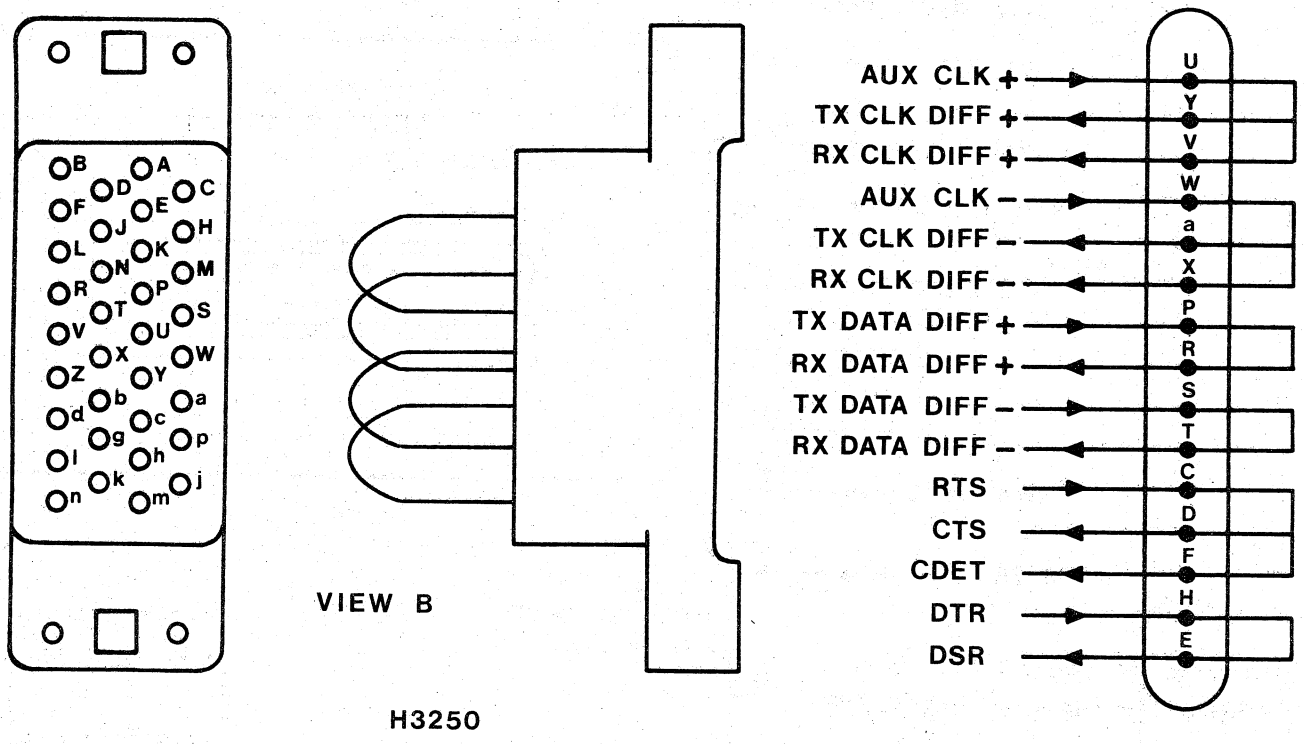


Figure 2-6 DZS11-EA Turnaround Test Connectors
(Sheet 3 of 3)

CHAPTER 3

PROGRAMMING and OPERATION

3.1 INTRODUCTION

This chapter provides the necessary information to program and operate the DZS11-EA component of the DZ STAT MUX network.

Section 3.2 provides information on DZS11-EA on board controls and indicators.

Sections 3.3 to 3.5 provide a detailed description of the DZS11-EA operation at register level, and are thus of interest to the reader who needs to program the DZS11-EA directly at the machine language level.

However, since the DZS11-EA is almost identical to a standard DZ11-A when viewed from the UNIBUS, it works transparently with the standard DZ11-A drivers contained in such operating systems as RSTS/E, RSX11-M, and VMS. Thus the DZS11-EA user would normally have no need to write a driver for the DZS11-EA but would be more interested in high level information on the operation and behaviour of the total DZS11-EA/VT1XX-EA/EB network. This is discussed in sections 3.6 to 3.11.

3.2 DZS11-EA CONTROLS AND INDICATORS

3.2.1 DZS11-EA Manual Controls

A number of on board switches are provided to enable configuration and fault diagnosis of the DZS11-EA. All but one of these switches have been mounted so that normal access is restricted while the option is installed in the system backplane. Detailed information is given on these switches in Section 2 of this document.

3.2.1.1 RUN/TEST Switch

The RUN/TEST switch is located at the top edge of the DZS11-EA (M7190) module to enable operator access when the module is inserted in the system backplane. Refer to Figure 2-1 for switch location.
The RUN/TEST switch, switches the on board microcontroller between normal operation mode and diagnostic mode.
Normal operation is with this switch set to the RUN position.
Diagnostic mode is with this switch set to the TEST position.

3.2.2 DZS11-EA LED Indicators

A group of eight light emitting diodes (LED) are located along the top edge of the module so that the status can be checked without having to remove the module from the system backplane. This group of LEDs indicates both operational and diagnostic status information. When RUN/TEST switch is in the RUN position they indicate DZ STAT MUX operational mode status.
With the RUN/TEST switch in the TEST position they indicate M7190 microdiagnostic status.

3.2.2.1 RUN Mode LED Status

Figure 3-1 shows the location of the LEDs, Table 3-1 lists each group with meanings.

Table 3-1 LED Display Status (Run Mode)

LED No.	RUN MEANING
8:7	Heart beat and run mode indicator. A rotating bit pattern indicates that the DZS11-EA microcontroller is in the RUN mode. The rate at which they rotate indicates the microcontroller heart beat.
6:4	DZS11-EA Composite port transmit error count. The binary value of LEDs 6, 5 and 4 indicate the number of transmit errors detected on the composite port. The maximum error count is 7, after which the counter resets to zero. LED 4 is the least significant bit.
3:1	DZS11-EA Composit Port receive error count. The binary value of LEDs 3, 2 and 1, indicate the number of receive errors detected on the composite port. The maximum error count is 7, after which the counter resets to zero. LED 1 is the least significant bit.

3.2.2.2 Test Mode LED Status

Figure 3-2 shows the location of the LEDs, Table 3-2 lists each LED with meaning.

Table 3-2 LED Display Status (Test Mode)

<table>
<tr><th>LED No.</th><th>TEST MEANING</th></tr>
<tr><td>8:7</td><td>Microdiagnostic type indicator.
A steady state pattern indicates that the DZS11-EA microcontroller is in the test mode. The following sub-table lists the three legal states of LEDs 8 and 7 when in the TEST mode.

<table>
<tr><th>8</th><th>7</th><th>TEST TYPE</th></tr>
<tr><td>OFF</td><td>ON</td><td>GO/NO GO test running</td></tr>
<tr><td>ON</td><td>OFF</td><td>OFF line test running</td></tr>
<tr><td>ON</td><td>ON</td><td>UNIBUS test running</td></tr>
</table></td></tr>
<tr><td>6:4</td><td>Test number indicator. Only valid for OFF LINE microdiagnostic.
The following sub-table lists the valid test numbers for the OFF LINE microdiagnostic.

<table>
<tr><th>6</th><th>5</th><th>4</th><th>TEST</th></tr>
<tr><td>OFF</td><td>OFF</td><td>ON</td><td>ROM test</td></tr>
<tr><td>OFF</td><td>ON</td><td>OFF</td><td>RAM test</td></tr>
<tr><td>OFF</td><td>ON</td><td>ON</td><td>CLOCK test</td></tr>
<tr><td>ON</td><td>OFF</td><td>OFF</td><td>X.25 logic test</td></tr>
<tr><td>ON</td><td>OFF</td><td>ON</td><td>X.25 int. data test</td></tr>
<tr><td>ON</td><td>ON</td><td>OFF</td><td>DMA locic test</td></tr>
<tr><td>ON</td><td>ON</td><td>ON</td><td>X.25 ext. data test</td></tr>
</table></td></tr>
<tr><td>3:1</td><td>Error Indicator.
This field indicates error states for GO/NO GO test and OFF LINE test. Refer to Section C-5 for error numbers and meaning.</td></tr>
</table>

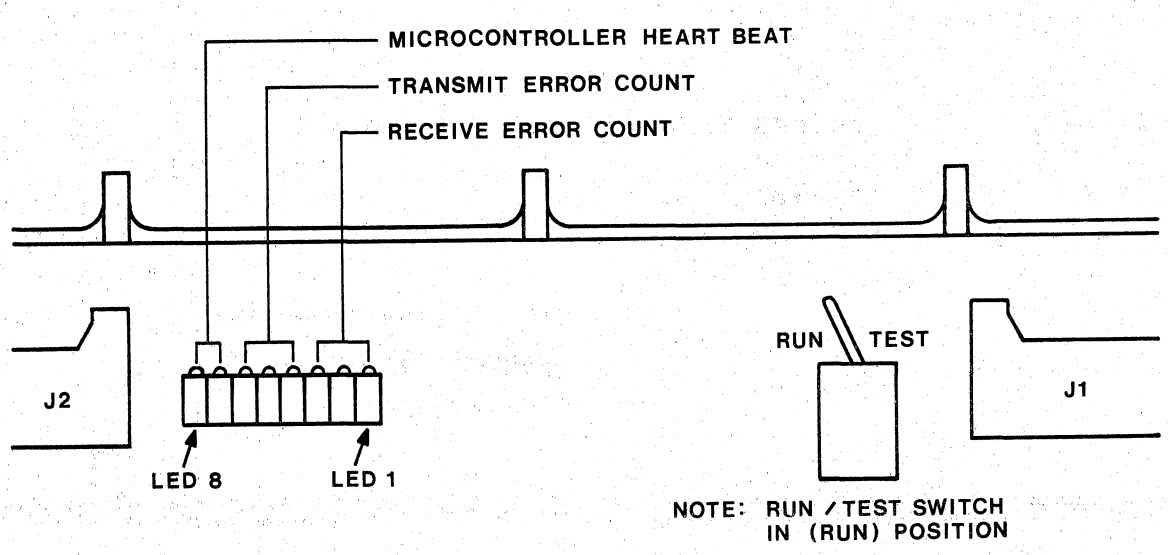


Figure 3-1 Run Mode LED Status

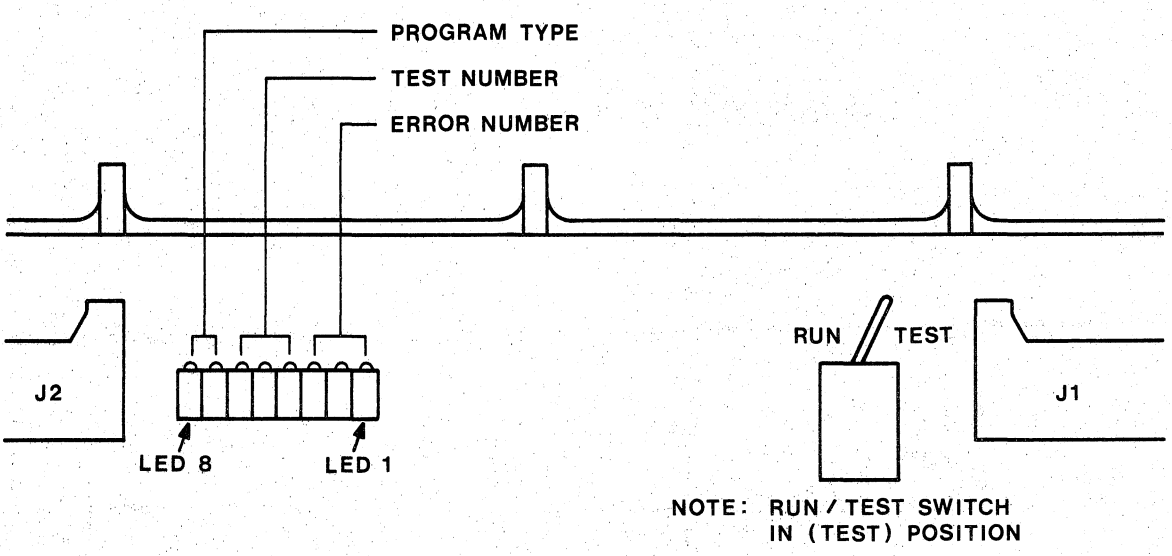


Figure 3-2 Test Mode LED Status

3.2.3 DZS11-EA Initialisation (DEVICE RESET)

There are three ways to perform an option reset on the DZS11-EA.

- System reset, in the form of BUS INIT.
- Device reset, in the form of BIS, operation of bit 4 of the device CSR register.
- Soft reset, by setting the RUN/TEST switch to the TEST position and then back to the RUN position.

The third option reset method can only be achieved on the condition that the DZS11-EA microcontroller is functional.

3.3 REGISTER BIT ASSIGNMENTS

This section provides basic information for programming the DZS11-EA. A description of each DZS11-EA register, its format, programming constraints, and bit functions are presented to aid programming and maintenance efforts.
A comprehensive pictorial of all register bit assignments is shown in Figure 3-3. The four device registers (DRØ, DR2, DR4, and DR6) are subdivided to form six unique registers. This subdivision is accomplished in DR2 and DR6 by assigning read-only (RO) or write-only (WO) status to each register. Since the reading and writing of DR2 and DR6 accesses two registers, PDP-11 processor instructions that perform a read-modify-write (DATIP) bus cycle cannot be used with DR2 or DR6. Also, DR2 permits only word instructions, but either byte or word instructions may be used with DR6. DRØ and DR4 have no programming constraints. In all register operations, the following applies: read-only bits are not affected by an attempt to write, and write-only and "not-used" bits appear as a binary Ø if a read operation is performed. Specific programming constraints for each register are discussed in the following paragraphs. A description of each bit function is presented in Tables 3-3 through 3-5.

3.3.1 Control and Status Register (CSR)

The control and status register (CSR) contains the status of flags and enable bits for scanning, processor interrupts, clearing, and maintenance. The 16-bit CSR has no programming constraints. The format is depicted in Figure 3-3, and bit functions are described in Table 3-3. Write-only and "not-used" bits are read as zeros by the UNIBUS, and read-only bits are not affected by write attempts.

		BYTES HIGH								LOW							
		MSB 15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	LSB 00
R/W 0	CONTROL & STATUS (CSR)	RO / TRDY	RW / TIE	RO / SA	RW / SA	NOT USED	RO / TLINE C	RO / TLINE B	RO / TLINE A	RO / RDONE	RW / RIE	RW / MSE	RW / CLR	RW / MAINT	NOT USED	NOT USED	NOT USED
2	RECEIVER BUFFER (RBUF)	RO / DATA VALID	RO / OVRN	RO / FRAM ERR	RO / PAR ERR	NOT USED	RO / RX LINE C	RO / RX LINE B	RO / RX LINE A	RO / RBUF D7	RO / RBUF D6	RO / RBUF D5	RO / RBUF D4	RO / RBUF D3	RO / RBUF D2	RO / RBUF D1	RO / RBUF D0
Same Add. R 2	LINE PARAMETER (LPR)	NOT USED	NOT USED	NOT USED	WO / RX ON	WO / FREQ D	WO / FREQ C	WO / FREQ B	WO / FREQ A	WO / ODD PAR	WO / PAR ENAB	WO / STOP CODE	WO / CHAR LGTH B	WO / CHAR LGTH A	WO / LINE C	WO / LINE B	WO / LINE A
4	TRANSMIT CONTROL (TCR)	RW / DTR 7	RW / DTR 6	RW / DTR 5	RW / DTR 4	RW / DTR 3	RW / DTR 2	RW / DTR 1	RW / DTR 0	RW / LINE ENAB 7	RW / LINE ENAB 6	RW / LINE ENAB 5	RW / LINE ENAB 4	RW / LINE ENAB 3	RW / LINE ENAB 2	RW / LINE ENAB 1	RW / LINE ENAB 0
ONLY 4																	
6 R	MODEM STATUS (MSR)	RO / CO 7	RO / CO 6	RO / CO 5	RO / CO 4	RO / CO 3	RO / CO 2	RO / CO 1	RO / CO 0	RO / R17	RO / R16	RO / R15	RO / R14	RO / R13	RO / R12	RO / R11	RO / R10
Same Add. 6 W	TRANSMIT DATA (TDR)	WO / BRK 7	WO / BRK 6	WO / BRK 5	WO / BRK 4	WO / BRK 3	WO / BRK 2	WO / BRK 1	WO / BRK 0	WO / TBUF 7	WO / TBUF 6	WO / TBUF 5	WO / TBUF 4	WO / TBUF 3	WO / TBUF 2	WO / TBUF 1	WO / TBUF 0

MASTER SCAN ENABLE

Figure 3-3 DZS11-EA Register Bit Assignments

Table 3-3 CSR Bit Functions

Bit	Title	Function
ØØ-Ø2	Not used	
Ø3	Maintenance (MAINT)	A read/write bit that, when set, causes a corresponding flag to set in the micro-controller. Cleared by BUS INIT and CLR.
Ø4	Clear(CLR)	A read/write bit that fires a one-shot to generate a 15 millisecond reset which clears the receiver microcontroller and the CSR. After a CLR is issued, the CSR and line parameters must be set again. CLR in progress is indicated by CLR = 1. Modem control registers are not affected, nor are bits ØØ through 14 of RBUF.
Ø5	Master Scan Enable	A read/write bit that enables the transmit control logic and receiver silo. Cleared by CLR and BUS INIT.
Ø6	Receiver Interrupt Enable	A read/write bit that enables the receiver interrupt. Cleared by CLR and BUS INIT.
Ø7	Receiver Done (RDONE)	A read-only bit (hardware set) that generates RCV INT if bit Ø6 = 1 and bit 12 = Ø. The bit clears when the RBUF is read and resets when another word reaches the output of the silo (RBUF). If bit Ø6 = Ø, RDONE can be used as a flag to indicate that the silo contains a character. If bit 12 = 1, RDONE does not cause interrupts but otherwise acts the same.

Table 3-3 CSR Bit Functions (cont).

Bit	Title	Function
08-10	Transmit Line A-C (TLINE)	When bit 15 = 1, these three read only bits indicate the line that is ready to transmit a character. Bit 15 cleares when the character is loaded into the transmit buffer, but sets again if another line is ready. A new line number could appear within a minimum of 1.9 microseconds. Bits 08-10 return to line 0 after a CLR or BUS INIT. These bits are meaningful only when bit 15 (TRDY) is true.
11	Not used	
12	Silo Alarm Enable (SAE)	A read/write bit that enables the silo alarm and prevents RDONE from causing interrupts. If bit 06 = 1, the SAE allows the SA (bit 13) to cause an interrupt after 16 entries in the silo. If bit 06 = 0, the SA can be used as a flag. The bit is cleared by CLR and BUS INIT.
13	Silo Alarm (SA)	A read-only bit is set by the hardware after 16 characters enter the silo. It causes an interrupt if bit 06 = 1 and is cleared by CLR, BUS INIT, and reading the RBUF. When the silo flag occurs (SA = 1), the silo must be emptied because the flag will not be set again until 16 additional characters enter the silo.
14	Transmitter Interrupt Enable (TIE)	A read/write bit that allows an interrupt if bit 15 (TRDY) = 1.
15	Transmitter Ready (TRDY)	A read-only bit that is set by hardware when a line number is found that has its transmit buffer empty and its LINE ENAB bit set. It is cleared by CLR, BUS INIT, and by loading the TBUF register.

3.3.2 Receiver Buffer (RBUF)

The receiver buffer (RBUF) register contains the received character bits, with line identification, error status, and data validity flag. As one of two registers in DR2 (RBUF and LPR), RBUF is accessed when a read operation is performed (write operation accesses the LPR). The programming constraints for the RBUF register are as follows:-

- Byte instructions cannot be used
- It is a read-only register
- TST or BIT instructions cannot be used because they cause the loss of a character
- The register requires master scan enable (CSR, bit Ø5) to be set in order to be functional. When this bit is off, bits ØØ to 14 of the RBUF become invalid regardless of the state of bit 15 (data valid) and the silo is held empty. The register format of RBUF is depicted in Figure 3-3 and bit functions are described in Table 3-4. Each reading of the RBUF register advances the silo and presents the next character to the program. Bits ØØ through 14 do not go to zero after a CLR or BUS INIT; however, they become invalid and the silo is emptied. Bit 15 (data valid) does clear to zero. (See Table 3-4).

Table 3-4 RBUF Bit Functions

Bit	Title	Function
ØØ:Ø7	Received Character	These bits contain the received character. If the the selected code level is less than eight bits wide, the high-order bits are forced to zero.
Ø8:1Ø	Line Number	These bits present the line number on which the character was received.
11:14	Not used.	
12	Parity Error	This bit always read as zero.
13	Framing Error	This bit always read as zero.
14	Overrun	This bit always read as zero.
15	Data Valid	This bit indicates that the character read from the silo (RBUF) is valid. The RBUF is read until the data valid bit = Ø, indicating an invalid character and empty silo. Cleared by CLR and BUS INIT.

3.3.3 Line Parameter Register (LPR)

The line parameter register is a 16 bit register that sets asynchronous line parameters at the remote VT1XX-EA and/or VT1XX-EB. The parameters controlled by this register are, stop code lengths, parity, speed, receiver enable and character length. Writing to this register causes a transfer to the DZS11-EA microcontroller. On detection of change in line parameter information, the DZS11-EA transmits the changed line parameter information to the appropriate VT1XX-EA/EB. Line parameters for each line must be reloaded after a CLR (bit Ø4 of CSR) or BUS INIT operation on the DZS11-EA. The programming constraints for the LPR are as follows:-

- It is a write-only register
- BIS or BIC instructions are not allowed
- Byte operations cannot be used.

Table 3-5 LPR Bit Functions

Bit	Title	Function
ØØ:Ø2	Line Number	These bits select the line for parameter loading.
Ø3:Ø4	Character Length	These bits set the character length for the selected line. The parity bit is not part of the character length. Ø4 Ø3 Ø Ø 5 bits Ø 1 6 bits 1 Ø 7 bits 1 1 8 bits
Ø5	Stop Code	This bit sets the stop code length (Ø = 1-unit stop, 1 = 2-unit stop or 1.5-unit stop is a 5-level code is employed).
Ø6	Parity	This bit selects the parity option (Ø = no parity check, 1 = parity enabled on TRAN and RCV).
Ø7	Odd Parity	This bit selects the kind of parity (Ø = even parity select, 1 = odd parity select). Bit Ø6 must be set for this bit to have effect.
Ø8:11	Speed Select	These bits select the TRAN and RCV speed for the line selected by bits ØØ-Ø2. Refer to Table 3-4 for a list of available baud rates.
12	Receiver On	This bit must be set when loading parameters to activate the receiver. A CLR or BUS INIT turns the receiver off.

3.3.4 Transmit Control Register (TCR)

The DZS11-EA Transmit Control Register contains two 8 bit bytes. The high byte contains 8 DTR bits and the low byte contains 8 transmit enable bits.

The high byte contains a read/write DTR bit for each line. This register is included for DZ11-A compatibility only and is only used for maintenance purposes. Change of state within this register does not reflect a change of state on the DTR line of VT1XX-EB asynchronous ports.
This byte is changed by BUS INIT only, not by CLR.
The low byte of TCR contains a read/write line enable bit for each line. A set bit allows transmission on the corresponding line.
Paragraph 3.4.7 explains how to properly use this bit. This byte is cleared by CLR and BUS INIT.

3.3.5 Modem Status Register (MSR)

The MSR is a 16 bit read only register, and has been included for DZ11-A compatibility only.

The MSR consists of two bytes: the low byte (bits ØØ:Ø7) and the high byte (15:Ø8). The low byte is the RING register, the high byte is the CARRIER register. These registers remain reset at all times and thus read as all zero.
In maintenance mode the DTR register is copied into both the high and low byte of this register.

3.3.6 Transmit Data Register (TDR)

The TDR consists of two 8 bit bytes. The low byte is the transmit buffer (TBUF) and is used to transfer the transmit character to the DZS11-EA microcontroller. The microcontroller packages the character into an X25 frame and transmits it to the appropriate remote VT1XX-EA/EB mux.
The high byte is the break register with each line controlled by an individual bit. When a break bit is set the VT1XX-EA/EB asynchronous line associated with that bit starts sending zeros, following a delay of between 50 msec to 400 msec (depending on the speed of the composite communication line and the prevailing network loading). The TDR is the write-only portion of DR6 and has the following programming characteristics:-

- It is a write-only register.
- BIS or BIC instructions cannot be used.
- For character lengths less than 8 bits, the character loaded into the TBUF must be right justified because the hardware forces the most significant bits to zero.
- The break register has no effect when running in the maintenance mode (i.e. CSR bit 03 = 1).
- It is cleared by CLR and BUS INIT.
- Bit format is shown in Figure 3-1.

3.4 PROGRAMMING FEATURES

The DZS11-EA has several programming features that allow control of VT1XX-EA baud rate, character length, stop bits, parity and DZS11-EA interrupts. This section discusses the application of these controls to achieve the desired operating parameters.

3.4.1 Baud Rate

The selection of the desired VT1XX-EA asynchronous port transmission and reception speed is controlled by the conditions of bits Ø8 through 11 of the DZS11-EA LPR. Table 3-5 depicts the required bit configuration for each operating speed. The baud rate for each line is the same for both the transmitter and receiver. The receiver clock is turned on and off by setting and clearing bit 12 in the LPR for the selected line.

Table 3-6 Baud Rate Selection Chart

Bits				Baud Rate
11	10	09	08	
0	0	0	0	50
0	0	0	1	75
0	0	1	0	110
0	0	1	1	134.5
0	1	0	0	150
0	1	0	1	300
0	1	1	0	600
0	1	1	1	1200
1	0	0	0	1800
1	0	0	1	2000
1	0	1	0	2400
1	0	1	1	3600
1	1	0	0	4800
1	1	0	1	7200
1	1	1	0	9600
1	1	1	1	Not used.

3.4.2 Character Length

The selection of one of the four available character lengths for the VT1XX-EA/EB asynchronous ports, is controlled by bits 03 and 04 of the DZS11-EA LPR. The bit conditions for bits 04 and 03, respectively, are as follows: 00 (5-level), 01 (6-level), 10 (7-level) and 11 (8-level). For character lengths of 5, 6 and 7, the high-order bits are forced to zero.

3.4.3 Stop Bits

The length of the stop bits in a serial character string is determined by bit 05 of the LPR. If bit 05 is zero, the stop length is one unit; bit 05 set to a one selects a 2-unit stop unless the 5-level character length (bits 03 and 04 at zero) is selected, in which case the stop bit length is 1.5 units.

3.4.4 Parity

The VT1XX-EA asynchronous port parity option is selected by bit Ø6 of the DZS11-EA LPR. Parity is enabled on transmission and reception setting bit Ø6 to a one. Bit Ø7 of the LPR allows selection of even or odd parity, and bit Ø6 must be set for bit Ø7 to be significant. The parity bit is generated and checked by hardware, and does not appear in the RBUF or TBUF.

3.4.5 Interrupts

The receiver interrupt enable (RIE) and silo alarm enable (SAE) bits in the CSR control the circumstances upon which the DZS11-EA receiver interrupts the PDP-11 processor.

If RIE and SAE are both clear, the DZS11-EA will not interrupt the PDP-11 processor. In this case, program must periodically check for the availability of data in the silo and empty the silo when data is present. If the program operates off a clock, it should check for characters in the silo at least as often as the time it takes for the silo to fill, allowing a safety factor to cover processor response delays and time to empty the silo. The RDONE bit in the CSR will set when a character is available in the silo. The program can periodically check this bit with a TSTB or BIT instruction. When RDONE is set, program should empty the silo.

If RIE is set and SAE is clear, the DZS11-EA will interrupt the PDP-11 processor to the DZS11-EA receiver vector address when RDONE is set, indicating the presence of a character at the bottom of the silo. The interrupt service routine can obtain the character by performing a MOV instruction from the RBUF. If the program then dismisses the interrupt, the DZS11-EA will interrupt when another character is available (which may be immediately if additional characters were placed in the silo while the interrupt was being serviced). Alternatively, the interrupt service routine may respond to the interrupt by emptying the silo before dismissing the interrupt.

If RIE and SAE are both set, the DZS11-EA will interrupt the PDP-11 processor to the DZS11-EA receiver vector when the silo alarm (SA) bit in the CSR is set. Th SA bit will be set when 16 characters have been placed in the silo since the last time the program has accessed the RBUF. Accessing the RBUF will clear the SA bit and the associated counter. The program should follow the procedure described in Paragraph 3.4.6 to empty the silo completely in response to a silo alarm interrupt. This will ensure that any characters placed in the silo while it is being emptied are processed by the program.

NOTE

If the program processes only 16 entries in response to each silo alarm interrupt,characters coming in while interrupts are being processed will build up without being counted by the silo alarm circuit and the silo may eventually overflow without the alarm being issued.

If the silo alarm interrupt is used, the program will not be interrupted if fewer than 16 characters are received. In order to respond to short messages during periods of moderate activity, the PDP-11 program should periodically empty the silo. The scanning period will depend on the required responsiveness to received characters. While the program is emptying the silo, it should ensure that DZS11-EA receiver interrupts are inhibited. This should be done by raising the PDP-11 processor priority. The silo alarm interrupt feature can significantly reduce the PDP-11 processor overhead required by the DZS11-EA receiver by eliminating the need to enter and exit an interrupt service routine each time a character is received.

The transmitter interrupt enable bit (TIE) controls transmitter interrupts to the PDP-11 processor. If enabled, the DZS11-EA will interrupt the PDP-11 processor to the DZS11-EA transmitter interrupt vector when the transmitter ready (TRDY) bit in the CSR is set, indicating that the DZS11-EA is ready to accept a character to be transmitted.

3.4.6 Emptying the Silo

The program can empty the silo by repeatedly performing MOV instructions from the RBUF to temporary storage. Each MOV instruction will copy the bottom character in the silo so it will not be lost and will clear out the bottom of the silo, allowing the next character to move down for access by a subsequent MOV instruction. The program can determine when it has emptied the silo by testing the data valid bit in each word moved out of the RBUF. A zero value indicates that the silo has been emptied. The test can be performed conveniently by branching on the condition code following each MOV instruction. A TST or BIT instruction must not access the RBUF because these instructions will cause the next entry in the silo to move down without saving the current bottom character. Furthermore, following a MOV from the RBUF, the next character in the silo will not be available for at least 1 micro second. Therefore, on fast CPUs, the program must use sufficient instructions or NOPs to ensure that successive MOVs from the RBUF are separated by a minimum of 1 micro second. This will prevent a false indication of an empty silo.

3.4.7 Transmitting a Character

The program controls the DZS11-EA transmitter through five registers on the UNIBUS: the control and status register (CSR), the line parameter register (LPR), the line enable register, the transmitter buffer (TBUF), and the break register (BRK).

Following DZS11-EA initialisation, the program must use the LPR to specify the speed and character format for each line to be used and must set the master scan enable (MSE) bit in the CSR. The program should set the transmitter interrupt enable (TIE) bit in the CSR if it wants the DZS11-EA transmitter to operate on the program interrupt basis.

The line enable register is used to enable and disable transmission on each line. One bit in this 8-bit register is associated with each line. The program can set and clear bits by using MOV, MOVB, BIS, BISB, BIC and BICB instructions. (If word instructions are used, the line enable register and the DTR registers on M7819 modules are simultaneously accessed).

The DZS11-EA transmitter is controlled by a scanner which is constantly looking for an enabled line (line enable bit set). When the scanner finds such a line, it loads the number of the line into the 3-bit transmit line number (TLINE) field of the CSR and sets the TRDY bit, interrupting the PDP-11 processor if the TIE bit is set. The program can clear the TRDY bit by moving a character for the indicated line into the TBUF or by clearing the line enable bit. Clearing the TRDY bit frees the scanner to resume its search for lines needing service.

To initiate transmission on an idle line, the program should set the TCR bit for that line and wait for the scanner to request service on the line, as indicated by the scanner loading the number of the line into TLINE and setting TRDY. The program should then load the character to be transmitted into the TBUF by using a MOVB instruction. If interrupts are to be used, a convenient way of starting up a line is to set the TCR bit in the main program and let the normal transmitter interrupt routine load the character into the TBUF.

NOTE

The scanner may find a different line needing service before it finds the line being started up. This will occur if other lines request service before the scanner can find the line being started. The program must always check the TLINE field of the CSR when responding to TRDY to ensure it loads characters for the correct line. Assuming the program services lines as requested by the scanner, the scanner will eventually find the line being started. If several lines require service, the scanner will request service in priority order as determined by line number. Line 7 has the highest priority and line Ø the lowest.

To continue transmission on a line, the program should load the next character to be transmitted into the TBUF each time the scanner requests service for the line as indicated by TLINE and TRDY.

To determine transmission on a line, the program loads the last character normally and waits for the scanner to request an additional character for the line. The program clears the line enable bit at this time instead of loading the TBUF.

The normal rest condition of the transmitted data lead for any line is the 1 state. The break register (BRK) is used to apply a continuous zero signal to the line. One bit in this 8-bit register is associated with each line. The line will remain in this condition as long as the bit remains set. The program should use a MOVB instruction to access the BRK register. If the program continues to load characters for a line after setting the break bit, transmitter operation will appear normal to the program despite the fact that no characters can be transmitted while the line is in the continuous zero sending state.

It should be remembered that for each line in the DZS11-EA, significant amounts of data characters are buffered. The program must not set the BRK bit too soon or the data characters preceding the break may not be transmitted. The program must also ensure that the line returns to the 1 state at the end of the zero sending period before transmitting any additional data characters. The following procedure will accomplish this. When the scanner requests service the first time after the program has loaded the last data character, the program should load an all-zero character. The program should then wait for at least one second before setting the BRK bit for the line. At the end of the zero sending period, the program should first clear the BRK bit, then wait at least 1 second before sending the next data character to be transmitted on that line.

3.5 PROGRAMMING EXAMPLES

The following six examples are sample programs for the DZS11-EA option. These examples are presented only to indicate how the DZS11-EA can be used.

Example 1 - Initialising the DZS11-EA

The DZS11-EA in initialised by a power-up sequence, a reset instruction, or a device clear instruction.

Device Clearing the DZS11-EA

```
001000  012737  START:  MOV #20,DZCSR   ;Set bit 4 in the
001002  000020                         ;DZS11-EA control and
001004  160100                         ;status register
001006  032737  1$:     BIT #20,DZCSR   ;Test bit 4.
001010  000020
001012  160100
001014  001374          BNE 1$          ;If bit 4 is still
                                        ;set, the branch
                                        ;condition is true
                                        ;and the device clear
                                        ;function is still in
                                        ;progress
001016  000000          HALT            ;The device clear
                                        ;function is complete
                                        ;and the DZS11-EA has been
                                        ;cleared.
```

DZCSR = Control and Status Register Address = 160100.

Example 2 - Transmit Binary Count Pattern on One Line

```
001000  012737  START:  MOV #20,DZCSR   ;Set bit 4 in the DZS11-EA
001002  000020                         ;control and status
                                        ;register.
001004  160100
001006  032737  1$:     BIT #20,DZCSR   ;Test bit 4.
001010  000020
001012  160100
001014  001374          BNE 1$          ;If bit 4 is still set,
                                        ;the branch condition
                                        ;is true and the device
                                        ;clear function is still
                                        ;in progress.
001016  012737          MOV #N,DZLPR    ;Load the parameters
001020  001070                         ;for line 0:8-bit
                                        ;character; 2 stop bits;
                                        ;110 baud
001024  012737          MOV #1,DZTCR    ;Enable line 0
                                        ;transmitter.
```

```
001026  000001
001030  160104
001032  012737          MOV #m,DZCSR    ;Set scanner enable bit
001034  000040                          ;5 in the control and
001036  160100                          ;status register.
001040  005000          CLR RO          ;Set binary count
                                        ;pattern to zero.
001042  005737  2$:     TST DZCSR       ;Test the transmitter
001044  160100                          ;ready flag (bit 15).
001046  100375          BPL 2$          ;If branch condition
                                        ;is false, continue;
                                        ;otherwise test again.
001050  110037          MOVB R0,DZTDR   ;Load character to be
001052  160106                          ;transmitted.
001054  105200          INCB R0         ;Increment binary count.
001056  100371          BPL 2$          ;If branch condition is
                                        ;false, the binary count
                                        ;pattern is complete.
001060  000000          HALT
```

R0 = Register 0 = Binary Count Pattern
DZCSR = DZS11-EA Control and Status Register Address = 160100
DZLPR = DZS11-EA Line Parameter Register Address = 160102
DZTCR = DZS11-EA Transmit Control Register Address = 160104

Example 3 - Transmit a Binary Count in Maintenance Loopback Mode, with the receiver "On" in the Interrupt Mode

Output Received Data to Console

```
001200  005000          CLR R0          ;Set binary count
                                        ;to zero.
001202  012701          MOV 1400,R1     ;Set R1 to first
001204  001400                          ;address of data
                                        ;buffer.
001206  012706          MOV #SP,R6      ;Initialise stack
001210  001100                          ;pointer.
001212  012737          MOV #INT,RVEC   ;Set DZS11-EA vector
001214  001304                          ;address to start of
001216  000300                          ;receiver interrupt
                                        ;routine.
001220  005037          CLR (RVEC+2)    ;Set up processor
001222  000302                          ;status word for DZS11-EA
                                        ;receiver interrupt.
001224  012737          MOV #20,DZCSR   ;Set bit 4 in the
001226  000020                          ;DZS11-EA control and
                                        ;status register.
```

```
001230  160100
001232  032737  1$      BIT #20 DZCSR   ;Test bit 4.
001234  000020
001236  160100
001240  001374          BNE 1$          ;If bit 4 is still
                                        ;set, the branch
                                        ;condition is true
                                        ;and the device clear
                                        ;function is still in
                                        ;progress.
001242  012737          MOV #PAR,DZLPR  ;Load the parameters
001244  011070                          ;for line 0: 8-bit
001246  160102                        ;character; 2 stop bits;
                                        ;110 baud; no
                                        ;parity; receiver on.
001250  012737          MOV #1, DZTCR   ;Enable line 0
                                        ;transmitter.
001252  000001
001254  160104
001256  012737          MOV #150,DZCSR  ;Turn scanner on,
001260  000150                          ;enable receiver
001262  160100                        ;interrupts, and loop
                                        ;lines back on themselves.
001264  005737  2$      TST DZCSR       ;Test the transmitter
001266  160100                        ;ready flag.
001270  100375          BPL 2$          ;If branch condition is
                                        ;false, continue;
                                        ;otherwise test again.
001272  110037          MOVB R0,DZTBUF  ;Load character to be
001274  160106                        ;transmitted.
001276  105200          INCB R0         ;Increment binary count.
001300  001371          BNE 2$          ;If branch condition is
                                        ;false, the binary count
                                        ;pattern is complete.
001302  000777          BR.             ;Wait for last character
                                        ;transmitted to be
                                        ;received.
```

Receiver Interrupt Service Routine

```
001304  013711          MOV DZRBUF,(R1) ;Store received
001306  160102                          ;character in memory
                                        ;table.
001310  022721          CMP #100377,    ;Check for last
001312  100377          (R1)+           ;character
001314  001401          BEQ.+2          ;Branch condition is
                                        ;true when last
                                        ;transmitted character
                                        ;is received.
001316  000002          RTI             ;Exit routine.
001320  012701          MOV #1400,R1    ;Initialise pointer
001322  001400                          ;to start of received
                                        ;data buffer in memory.
001324  105737  3$      TSTB TPS        ;Test to see if console
001326  177564                        ;is ready.
001330  100375          BPL 3$          ;Wait, and test again.
                                        ;If condition is met,
001332  111137          MOVB (R1),TPB   ;transfer character
001334  177566                        ;to console.
001336  022721          CMP #100377,    ;Check for last
001340  100377          (R1)+           ;character.
001342  001370          BNE 3$          ;Not finished if
                                        ;condition is true.
001344  000000          HALT            ;finished.
```

```
RVEC    = DZS11-EA Receiver Interrupt Vector Address
DZCSR   = DZS11-EA Control and Status Word Address
DZLPR   = DZS11-EA Line Parameter Register (Write-Only) Address
DZTCR   = DZS11-EA Transmit Control Register Address
DZTBUF  = DZS11-EA Transmit Buffer Address
DZRBUF  = DZS11-EA Receiver Buffer Address (Read-Only Register)
TPS     = Teletype* Punch Status Register Address
TPB     = Teletype Punch Data Register Address
```

*Teletype is a registered trademark of Teletype Corporation

Example 4 - Transmit and Receive in Maintenance Mode on a Single Line

The switch register bits (SWR00-SWR07) hold the desired data pattern (character).

```
001000  012737  START:  MOV #LINE,DZTCR ;Select the line for
001002  000002                         ;transmitting on.
                                       ;Choose one of eight.
001004  160104                         ;Line #1 selected.
001006  012737          MOV #PAR,DZLPR ;Select desired line
001010  017471                         ;parameters for
                                       ;transmitting line
001012  160102                         ;and turn on receiver
                                       ;for that line.
                                       ;8-level code, 2 stop
                                       ;bits, and no parity
                                       ;selected.
                                       ;19.2K baud selected
                                       ;Note: 19.2K baud is
                                       ;not used by the
                                       ;customer but can be
                                       ;used for diagnostic
                                       ;purposes to speed up
                                       ;the transmit-receive
                                       ;loop to make it easier
                                       ;to scope.
001014  012737          MOV #N,DZCSR   ;Start scanner and set
001016  000050                         ;maintenance bit 3.
001020  160100
001022  005737  Test 1: TST DZCSR       ;Test for bit 15
001024  160100                         ;(transmitter ready).
001026  100375          BPL Test 2     ;If the branch condition
                                       ;is false, the transmitter
                                       ;is ready, if true, go
                                       ;back and test again.
001030  113737          MOVB SWR,      ;Load the transmit
001032  177570          DZTBUFF        ;character from the
001034  160106                         ;switch register.
001036  000240          NOP            ;No operation. This
                                       ;location can be changed
                                       ;to a branch instruction
                                       ;if only test 1 is
                                       ;desired (replace 000240
                                       ;with 000771).
```

```
001040  012701          MOV #DEL,R1     ;Delays equals a
        177670                          ;constant that will
                                        ;allow enough time for
                                        ;the receiver done
                                        ;flag to set before
                                        ;recycling the test.
                                        ;The value will change
                                        ;with baud rate and
                                        ;processor. The
                                        ;constant given is
                                        ;good for 19.2K baud
                                        ;on a PDP-11/05.

001042  105737  Test 2: TSTB DZCSR       ;Test bit 2 (receiver
001044  160100                          ;done flag).
001046  100402          BMI 1$          ;When the branch
                                        ;condition is true,
                                        ;the receiver done
                                        ;flag is set.
001050  005201          INC R1          ;Increment delay.
001052  001373          BNE TEST 2      ;If the branch
                                        ;condition is true, the
                                        ;delay is not finished.
001054  013700  1$      MOV DZRBUF,R0   ;Read the DZS11-EA
001056  160102                          ;receiver buffer to
                                        ;register 0.
001060  000760          BR TEST 1       ;Loop back and
                                        ;test again.
```

Example 5 - Transmit and Receive on a Single Line Using Silo Alarm in Maintenance Mode

```
001200  012706          MOV #1100,R6    ;Initialise stack
001202  001100                          ;pointer.
001204  012737          MOV #3$,TVEC    ;Initialise transmitter
001206  001274                          ;vector address.
001210  000304
001212  005037          CLR TVEC+2      ;Initialise transmitter
001214  000306                          ;vector processor status
                                        ;word.
001216  012700          MOV #DBUF,R0    ;Set first address of
001220  001304                          ;input data table
                                        ;into R0.
001222  012737          MOV #1,DZTCR    ;Enable line 0
                                        ;transmitter.
```

```
001224  000001
001226  160104
001230  012737          MOV #17470,     ;Set up line parameters
001232  017470          DZLPR           ;and turn on the receiver
001234  160102                          ;clock for line 0.
001236  012737          MOV #50050,     ;Enable transmitter
001240  050050          DZCSR           ;interrupt and silo
001242  160100                          ;alarm. Turn on
                                        ;scanner and maintenance
                                        ;mode.
001244  032737  1$      BIT #20000,     ;Test for silo alarm
001246  020000          DZCSR
001250  160100
001252  001774          BEQ 1$          ;Loop until silo alarm
                                        ;flag sets.
001254  013720  2$      MOV DZRBUF,     ;Read DZS11-EA silo
001256  160102          (R0)+           ;receiver buffer output.
001260  000240          NOP             ;Delay to allow next
001262  000240          NOP             ;word in silo to filter
                                        ;down to the silo
                                        ;output.

001264  100773          BMI 2$          ;Data valid set says
                                        ;that word is good,
                                        ;go back for more.
001266  012700          MOV #DBUF,R0    ;Silo has been emptied.
001270  001303                          ;Reinitialise data
                                        ;table address pointer.
001272  000764          BR 1$           ;Do it again.
```

Transmitter Interrupt Service Routine

```
001274  112737  3$      MOVB DAT,DZTBUF ;Transmit
001276  000252                          ;character 252
001300  160106
001302  000002          RTI
```

Data Table

```
1304    100252   ;Word 1
1306    100252

  .       .          .

          .          .

  .       .          .

  .       .          .

  .       .          .

  .       .          .

1304    100252   ;Word 16
1342    000252   ;Data valid
                 ;not set
                 ;character is
                 ;invalid
```

NOTE

It is possible to get more than 16 words because they are being put into the silo simultaneously with the reading of the silo.

Example 6 - Echo Test on a Single Line (Transmit Received Data)

```
001000  012737  START   MOV #PAR,DZLPR  ;Load line parameters
                                        ;for line being used.
001002  011073                          ;Line 3, 8-bit
001004  160102                          ;character, 2 stop
                                        ;bits, no parity,
                                        ;110 baud, and receiver
                                        ;clock on.
001006  012737          MOV #LINE,DZTCR ;Turn line 3
001010  000010                          ;transmitter on.
001012  160104
001014  012737          MOV #n,DZCSR    ;Turn scanner on
001016  000040                          ;(set CSR-5)
001020  160100
001022  105737  1$      TSTB DZCSR      ;Test (bit 7) for
001024  160100                          ;RDONE
001026  100375          BPL 1$          ;If bit 7 is not set,
                                        ;go back and test again.
001030  005737  2$      TST DZCSR       ;Test (bit 15) for
001032  160100                          ;TRDY
001034  100375          BPL 2$          ;If bit 15 is not set
                                        ;go back and test again.
001036  013700          MOV RBUF,R0     ;Read received data
001040  160102                          ;word into R0
001042  110037          MOVB R0, DZTDR  ;Load character
001044  160106                          ;into DZS11-EA TBUF
                                        ;register for
                                        ;transmitting.
001046  000765          BR 1$           ;Repeat.
```

3.6 NETWORK DESCRIPTION

As shown in Figure 1-1, a DZS11-EA terminal multiplexer network is composed of the DZS11-EA connected to a remote VT1XX-EA/EB, and perhaps with a further route-through connection to a second remote VT1XX-EA/EB.

The following sections will discuss the operational characteristics of such a network.

3.7 NETWORK INITIALISATION

3.7.1 DZS11-EA Role in Network Initialisation

On power up, after a successful run of a GO/NO GO self test diagnostic, the DZS11-EA begins operation and tries to establish communication by sending a special 'RESET' message out to the remote VT1XX-EA/EB, while constantly waiting to receive a 'RIM' (Request Initialisation Mode) from it.

The 'RESET' frame is re-transmitted every 10 seconds, until a 'RIM' is received from the VT1XX-EA/EB.

3.7.2 'RESET' Message

When a VT1XX-EA/EB receives a 'RESET' message coming into its main composite port, it will restart operation by emulating a power up sequence.
The 'RESET' message allows network operation to be re-established in the case of as a temporary loss of power supply at the DZS11 local mux: on regaining power, the DZS11 sends a 'RESET' to the VT1XX, which re-initialises itself and responds with a 'RIM' message thus starting the network initialisation sequence.

3.7.3 The 'RIM' Message

On power up, the VT1XX-EA/EB first carries out a self-test diagnostic (cf. VT1XX-EA/EB Option Description). It then transmits a 'RIM' message, out of its main composite port every two seconds, requesting the local mux DZS11 to supply it with initialisation parameters for its active ports. (A 'RIM' from a secondary (route-through) VT1XX-EA/EB will be relayed by the primary (nearer) VT1XX-EA/EB to the DZS11-EA, with the Address Field set to 1).

The 'RIM' message has one byte of information reflecting the 'Active Ports' switch on the VT1XX, with one bit for each of the 8 terminal ports driven by the VT1XX-EA/EB: a bit is set to denote that the corresponding port is to be active.

Based on information contained in the 'RIM' messages it receives, the DZS11-EA will determine the network mapping between the ports on the remote VT1XXs and the eight DZ lines it controls.

For example, consider the case where the Primary Remote Mux says that it has five active ports, namely Port Ø, Port 3, Port 4, Port 5 and Port 6. Also the Secondary Remote Mux says that it has five active ports, Port Ø, Port 2, Port 3, Port 4, and Port 5.

The information bytes in the RIM messages from each remote mux are as shown below.

RIM MESSAGE	PORT NUMBER							
	Ø	1	2	3	4	5	6	7
PRIMARY REMOTE MUX	1	Ø	Ø	1	1	1	1	Ø
SECONDARY REMOTE MUX	1	Ø	1	1	1	1	Ø	Ø

NOTE that in this example the total number of active remote ports is greater than 8.

The DZS11-EA will always give precedence to the Primary Remote Mux RIM, in the case of such conflict over the total number of active ports.

In this example, the DZS11-EA will allocate five DZ lines, from DZØ through DZ4 to the Primary Remote Mux, and the 3 remaining lines (DZ5 thru DZ7) to the Secondary Remote Mux according to the following mapping:

DZ LINE	REMOTE MUX	PORT NUMBER
DZ Ø	Primary	Port Ø
DZ 1	Primary	Port 3
DZ 2	Primary	Port 4
DZ 3	Primary	Port 5
DZ 4	Primary	Port 6
DZ 5	Secondary	Port Ø
DZ 6	Secondary	Port 2
DZ 7	Secondary	Port 3

The Local Mux, after having worked out this mapping table will then build up appropriate SIM messages and send them to both remote muxes, to give them the DZ line parameters corresponding to each allocated active port on the two remote muxes.

3.7.4 The 'SIM' Message

On receipt of a 'RIM' request from a remote VT1XX-EA/EB, the DZS11-EA will respond with a 'SIM' (Set Initialisation Mode) message.

The information field of a SIM frame consists of 16-bit subfields, each subfield giving all the operating parameters for an active port on the remote VT1XX-EA/EB, including line speed, character format and DZ line number mapped to this port. This is used by the VT1XX-EA/EB to initialise its active ports for operation.

3.8 SYNCHRONISATION

3.8.1 General

This section discusses the synchronisation method regulating data flow between the host computer and the terminals connected to it through a STAT MUX network, to prevent data overflow.

3.8.2 Data Flow from Host Computer to Terminals

A terminal connected to a VT1XX-EA/EB asynchronous port may not be able to keep up with incoming data sent from the host computer. The terminal may signal this condition to the VT1XX-EA/EB in one of two ways.

- Transmit Ø23 octal (XOFF or DC3)
- Lower DTR (data terminal ready) signal line.

3.8.2.1 Synchronisation Using DTR Signal From Terminals

At installation time, the VT1XX-EA/EB can be configured to use either XON/XOFF or EIA control signals to synchronise data flow to the terminals, on a per line basis. For terminal ports configured to use EIA control, the VT1XX-EA/EB always checks that the DTR signal from a terminal is asserted before transmitting a character to that terminal. If a terminal lowers its DTR line, the VT1XX-EA/EB will suspend transmission to that terminal, and starts to buffer up characters for that terminal in its internal buffer space. When the terminal is ready to accept more characters, it asserts its DTR signal, whereupon the VT1XX-EA/EB resumes its transmission to the terminal.

3.8.2.2 Synchronisation Using XON/XOFF

At installation time, the VT1XX-EA/EB can be configured to process XON/XOFF synchronisation on a per line basis. The VT1XX-EA/EB will immediately suspend its transmission to any port which has been set up to use XOFF/XON, on receiving an XOFF character (Ø23 octal) from that port. The VT1XX-EA/EB will resume its transmission only when an XON (Ø21 octal) is later received from that port. The received XOFF and XON characters are not passed onto the host computer.

3.8.2.3 Control Mechanism To Prevent VT1XX-EA/EB Buffer Overflow

The host computer will not be aware that the remote VT1XX-EA/EB has suspended transmission to a terminal on detection of a lowered DTR signal, or on receiving an XOFF from that terminal. Thus the host computer may continue sending more characters for that terminal.

In that case, the VT1XX-EA/EB will store incoming characters from the host computer in its internal buffer. Depending on how long transmission to the terminal is suspended, some or all of the following events may occur.

- When the total number of characters buffered for any terminal port has reached 1,ØØØ characters, the VT1XX-EA/EB sends a special control frame to the DZS11-EA, requesting the DZS11-EA to stop sending characters for that particular terminal. The DZS11-EA will then start to store characters coming from the host computer for the terminal involved into its internal buffers (while continuing to send characters for other terminals to the VT1XX-EA/EB).

- When the number of characters stored for that terminal inside DZS11-EA buffers has reached a high mark the DZS11-EA then pushes an XOFF character (Ø23 octal) with the appropriate line number into the host computer DZ11-EA receive silo (RBUF). Also from then on, the DZS11-EA will request from the host CPU, a character to transmit to that line only once in every Ø.3 second, i.e. the DZS11-EA will set that line number into bits 8-1Ø (TX-line) of its CSR, together with setting bit 15 (TRDY) of its CSR, only once in every Ø.3 second.

NOTE: The DZS11-EA stores transmit characters for each line in a separate circular buffer 256 characters long. If the host computer software does not support XOFF synchronisation, it will in the above circumstances give the DZS11-EA up to three characters every second for that terminal. Therefore, it is possible (during extended link downline) that a circular buffer wraps around resulting in lost characters.

- When the terminal is again ready to accept more characters it indicates this to the VT1XX-EA/EB either by raising its DTR signal line, or by transmitting an XON (Ø21 octal) character. VT1XX-EA will resume transmitting to the terminal the characters stored inside its buffers.

- When the number of characters buffered inside the VT1XX-EA/EB buffers for this terminal drops below 25Ø characters, the VT1XX-EA/EB sends a special control frame to the DZS11-EA notifying it that it can again send characters for that line to the VT1XX-EA/EB.

- As the DZS11-EA resume sending characters buffered up inside its own buffers for that line, the number of characters buffered will eventually drop below a low mark, when the DZS11-EA gives an XOFF character with the appropriate line number to the host CPU, and resumes requesting characters to transmit to that line.

3.8.3 Data Flow From Terminals to Host Computer

3.8.3.1 XON/XOFF From Host Computer

XON (Ø21 octal) and XOFF (Ø23 octal) characters transmitted from the host CPU are not processed in any way by either the DZS11-EA or the VT1XX-EA/EB. These characters are simply passed onto the destination terminal as standard data characters, and it is left to the terminal to recognise and process these as appropriate.

3.8.3.2 XON/XOFF From VT1XX-EA/EB

Characters coming from terminals to the VT1XX-EA/EB are stored in individual circular buffers (64 characters long) to be later grouped into composite frames and transmitted to DZS11-EA. During normal operation, characters are packaged up and transmitted very soon after they are put into the circular buffer, the number of characters in each buffer is rarely greater than three.

If due to the same abnormal conditions (eg. communication line break down) the number of characters stored in a buffer reach 48, then the VT1XX-EA/EB will send an XOFF (Ø23 octal) to the corresponding terminal to request it to stop transmission. When the number of characters drop below 16, the VT1XX-EA/EB will send an XON (Ø21 octal) to the terminal to signal that it may resume transmission. If the terminal does not recognise the receipt of XOFF and XON, it is possible that characters will be lost through circular buffer overwrapping.

3.9 NETWORK RECONFIGURATION FOR OPTIMUM RESPONSE AND THROUGHPUT

A significant feature of the DZ Statistical Multiplexer is the ease with which the terminal configuration can be adapted to changes in network load conditions, to achieve optimum response and throughput.

Consider the case where a line-printer and seven VDU's are multiplexed to a host computer through a single 4800 baud communication line.

During peak periods when the line-printer is printing at full speed and all seven VDU's are being used, the VDU's would probably work most smoothly at 1200 baud.

During low activity periods, when no printing is being done, and only a few VDU's are being used, the VDU users may want to operate their terminals at 4800 baud to make full use of the communication line capacity, and be able to scan through text files more quickly on their screens.

Since the DZS11-EA is fully compatible to the Standard DZ11-A, changing terminal ports baud rate can be achieved very simply by the same procedure as applicable to a local terminal connected directly to a standard DZ11-A port:

1. Log into the host operating system.

2. Type in the appropriate command to request the operating system to change the terminal baud rate.

   (e.g. For RSTS/E : SET SPEED nnnn
   For RSX11/M : SET /SPEED = TI: nnnn:nnnn
   For VMS : SET TERMINAL/SPEED = nnnn)

   (On receipt of this command, the operating system will give the new terminal baud rate to the DZS11-EA, which will use a special control message to relay this new speed to the remote VT1XX-EA/EB Multiplexer. The VT1XX-EA/EB will then reset its relevant port to operate at this new baud rate).

3. Change the set up of the terminal itself to the new baud rate (eg. via the Set Up Mode for a VT100 or LA120, or via baud rate switches for VT52's...). The terminal is now communicating to the host at the new baud rate.

3.10 NETWORK ERROR DETECTION AND RECOVERY

The DZS11-EA Multiplexer uses the X.25 level 2 protocol to ensure data integrity. Each data frame sent on the communication line is protected by a frame sequence number and a 16-bit CRC check sequence. When an error is detected, the protocol automatically causes the frame in error to be retransmitted until error free reception is confirmed. During communication line failures, data is buffered inside the DZS11-EA and VT1XX-EA/EB buffer memory and normal operation is automatically resumed without any loss of data when the communication line recovers.

Statistics on communication errors are included on the network status display which can be obtained at any time as discussed in the next section.

3.11 NETWORK STATUS AND STATISTICS DISPLAY

3.11.1 DZS11-EA Status Display

The DZS11 operating status is displayed through a set of eight LED's (Light Emitting Diodes), that we will number from right to left as LED 1 to LED 8.

LEDs 7 and 8 indicate the operating mode of the DZS11-EA as follows:

LED 8	LED 7	DZS11 Operating Mode
OFF	ON	Running the off-line microdiagnostic.
ON	OFF	Running the DZ11 Unibus Diagnostic.
(FLASHING ALTERNATELY ON AND OFF)		Normal network operation.

The meaning for LEDs 1 to 6 during the running of diagnostics is discussed in Section 3.2.

During normal network operation, LEDs (1 to 3), and (4 to 6), form two 3-bit counters which are used to display the current count (modulo 8) of receive errors and transmit errors on the communication line.

3.11.2 VT1XX-EA/EB Status Display

Any time during normal network operation, the small STATUS switch on the VT1XX-EA/EB back distribution panel can be switched ON then OFF, to obtain on the host VT1ØØ screen the network status display shown in Figure 3-4.

The first two lines of the display show the following network statistics for the main link (to host computer), and the route-through link (to the second route-through VT1XX-EA/EB):

- Total numbers of frames received including both control frames and information frames.
- The number of information frames (i.e. actually carrying data characters) among the above number of received frames.
- Total number of receive errors encountered on the line.
- Number of errors (among the above) which are CRC check sequence errors.
- Total number of frames transmitted.
- Number of information frames among the above transmitted frames.
- Total number of transmit errors encountered on the line.
- Number of time-outs, without receiving an ACK after transmitting an information frame(s).

All the above counters are 16-bit counters, i.e. they wrap around to zero on reaching 65535.

The next section of the display shows for each of the four (or eight) ports of the VT1XX-EA/EB the following information:

- To which DZ line (from Ø to 7) is this port mapped to. The mapping is determined according to the VT1XX-EA/EB's (and the route-through VT1XX-EA/EB's) terminal port mapping switch setting, configured at installation time.
- The operational baud rate, and character format (number of bits and stop bits, odd/even or no parity) as set by the host computer for the corresponding DZ line, and thus applicable to this terminal port.

VT1XX-EB STATISTICS

LINK	TOTAL FRAMES RECD	DATA FRAMES RECD	TOTAL RECD ERRORS	CRC RECD ERRORS	TOTAL FRAMES XMIT	DATA FRAMES XMIT	TOTAL XMIT ERRORS	XMIT TIME-OUTS
MAIN	486	473	5	0	196	122	0	0
R-THRU	0	0	0	0	33	0	0	0

PORT NO	0	1	2	3	4	5	6	7
MAPPED	DZ0	DZ1	DZ2	DZ3	DZ4	DZ5	DZ6	DZ7
SPEED	2400	4800	4800	4800	9600	9600	1200	4800
CHAR LEN	8	8	8	8	8	8	8	8
STOP BTS	1	1	1	1	1	1	1	1
PARITY	N	N	N	N	N	N	N	N

Figure 3-4 VT1XX-EA/EB Network Statistics Display

3.12 ASYNCHRONOUS DATA LOCAL ECHO

In terminal multiplexer networks where the baud rate of the composite communication line is low (1200 baud to 2400 baud), echo delays could become long during busy periods of peak throughput, when all terminals and printers are simultaneously active.

Local echo operation is sometimes used to avoid the echo delay: in local echo mode, a character input from a terminal connected to the remote multiplexer is echoed back immediately by the remote multiplexer itself, while normally the echo has to come back from the host computer.

The VT1XX-EA/EB can be setup to support local echo: all characters received from a terminal port set to local echo will be re-transmitted back to the terminal by the VT1XX-EA/EB. The next sections describe how to setup the VT1XX-EA/EB for local echo operation, and discusses the implication of using local echo in conjunction with the RSTS/E, RSX-11/M and VMS operating systems.

3.12.1 Setting the VT1XX-EA/EB for Local Echo Operation

The user can select local echo operation on the selected VT1XX-EA/EB ports by setting the appropriate bit in the switch group 5 on the host VT100 SET-UP B display.

On power up the VT1XX-EA/EB sends a "Request Terminal Parameters" escape sequence to the host VT100. The VT100's reply includes the value of switch group 5, which is then used by the VT1XX-EA/EB to determine which of its terminal ports should provide local echo.

Setting the VT1XX-EA/EB for local echo operation is performed by the following steps:

1. Make sure that users of all terminals connected to this VT1XX-EA/EB have finished their terminal sessions and logged off the host computer systems.

2. Enter SET-UP mode on the host VT100 (containing the VT1XX-EA/EB) by pressing the host VT100's SETUP key.

3. Select SET-UP B mode (by pressing the 5 key). The last line on the SET-UP B display is shown in Figure 3-5.

4. Use the <- and -> keys to position the cursor above the group 5 bits, and change these bits to the appropriate values by pressing Key 6.

5. Press SHIFT/S to save the new SET-UP values. Wait until the display returns to SET-UP A mode.

6. Press the Ø key to reset both the VT1ØØ and the VT1XX-EA/EB. The VT1XX-EA/EB on going through its power up sequence, will get the new values for the group 5 bits, and will now provide local echo to the selected ports.

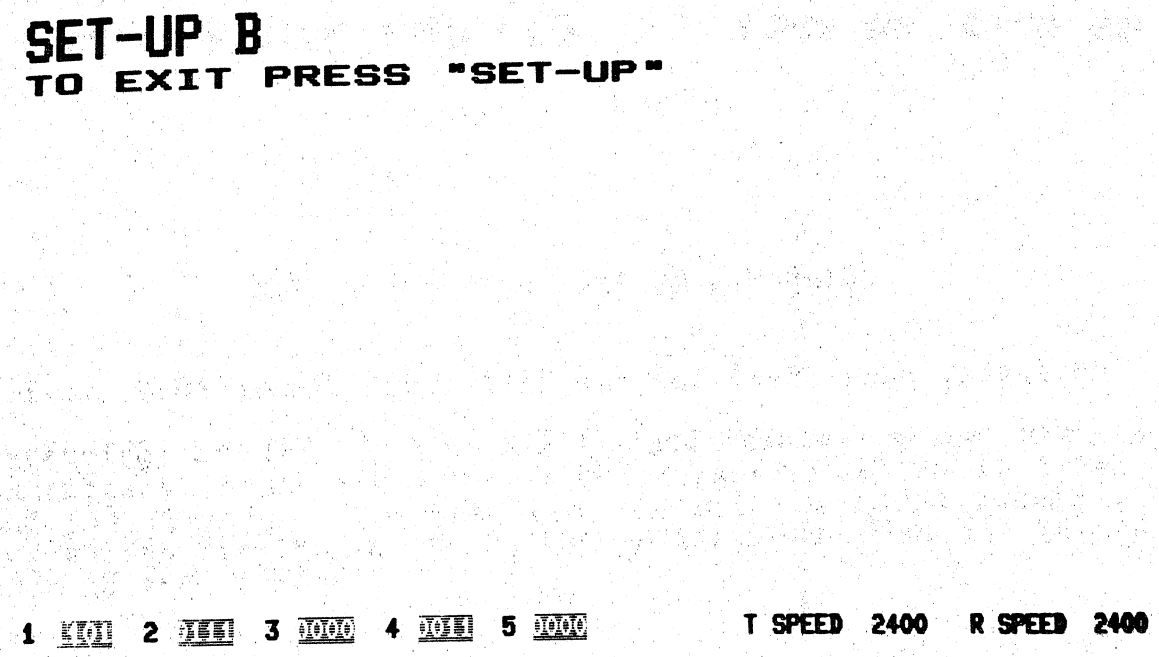


Figure 3-5 VT1ØØ SET UP B Display

3.12.2 Programming Considerations for Local Echo Operation

Referring to the 7 bit ASCII code table, there are 33 characters classified as control characters (Ø to 37 octal, and 177 octal). Of these only six will normally result in any screen display (or printing) action, when they are echoed back to the terminal:

Octal Code	Character
Ø1Ø	BS Backspace
Ø11	HT Horizontal Tab
Ø12	LF Line Feed
Ø13	VT Vertical Tab
Ø14	FF Form Feed
Ø15	CR Carriage Return

In general, all other control characters when echoed back to the terminal will be discarded by the terminal as non-displayable or non-printable characters.

For a VT1XX-EA/EB terminal port in local echo mode, if the host computer software also echoes each received character, then each input character will be echoed twice, once by the VT1XX-EA/EB and again by the host computer. Therefore, for correct operation, the host computer software should not echo characters received from the local echo mode terminal ports. The host computer software which processes (and possibly echoes) input characters can either be:

- a user-written application program which intercepts each character as it comes in: in this case, the application programmer controls the appropriate echoing.

- the host operating system's terminal driver, which stores (and normally echoes) input characters until a line terminator character is received, when the whole line is given to the user program. In this case, the operating system needs to be told which terminal lines are operating in local echo, so that echoing is appropriately suppressed for the relevant terminal lines. This will be discussed further in a later section for the RSTS/E, RSX11/M and VMS operating systems.

All characters received from a local echo port including control characters are re-transmitted back unchanged by the VT1XX-EA/EB. The only two exceptions are the XON and XOFF characters (21 and 23 octal) which are not echoed.

A possible problem in local echo operation is the echo of the CARRIAGE RETURN KEY. When echo is done by the host computer software, a single received 'RETURN' character (Ø15 octal) will result in two characters being transmitted back as echoes: a Line Feed character (Ø12 octal) plus a CR (Carriage Return) character (Ø15 octal), thus positioning the terminal cursor at the start of a new line.

In local echo however, a received CR character is echoed just as a single CR character, and this could result in overwriting the next line on top of the previous line. This problem can be overcome if the terminal itself can be set into a New Line mode. (i.e. SET-UP B Group B, switch 3 equals 1 for VTlØØ, or SET-UP W equals 3 for LA12Ø): then a single CR character is interpreted by the terminal as equivalent to both carriage return and line feed.

3.12.3 Local Echo in RSTS/E

Local echo mode is particularly suited to terminals connected to a RSTS/E operating system.

When the command:

SET LOCAL ECHO

has been entered at the RSTS/E terminal, the RSTS/E terminal driver will then not echo back any printable characters (4Ø octal to 176 octal). However, the operating system will still send out the appropriate expected echo sequences on receiving control characters with special RSTS/E meanings such as CTRL/R, CTRL/U, CTRL/Z, CTRL/C, CTRL/O, thus in RSTS/E echoing to a local echo terminal occurs correctly for the whole ASCII character set.

3.12.4 Local Echo in RSX11/M and VMS

Echo from the operating system VMS or RSX11/M terminals can be disabled by the following respective commands:

SET TERMINAL/NOECHO (for VMS)

or: SET /NOECHO = TT: (for RSX11/M)

However, in this mode, regardless of the received input character, no echo character will ever be sent out from the host operating system: thus the normal expected echo sequence in reply to special echo characters (CTRL/R, CTRL/U, DELETE...) will not occur. Local echo in RSX11/M and VMS is thus more suitable to special applications in which the terminal input stream is assigned to a user written program which intercepts each character as it comes in, and provides appropriate special echo sequences required for any special control characters.

CHAPTER 4

DETAILED DESCRIPTION

4.1 SCOPE

This chapter contains detailed descriptions of the DZS11-EA hardware operation, signal flow and firmware operation. The device is first divided into functional blocks to describe in general each sections function. Once an overall description has been presented each sub section is described in detail.

4.2 ENGINEERING DRAWINGS

A complete set of engineering and circuit schematics is provided in a companion volume to this manual entitled DZS11-EA Field Maintenance Print Set. The general logic symbols used on these drawings are described in the DIGITAL Logic Handbook. Specific symbols and conventions are also included in certain PDP-11 system manuals. The following paragraphs describe the signal nomenclature convention used on the drawing set.

Signal names in the DZS11-EA print set are given in the following basic form:

SOURCE SIGNAL NAME POLARITY

SOURCE indicates the drawing number of the print set where the signal originates. The drawing number of a print is located in the lower right corner of the print title block (S1, S2, S3 etc). SIGNAL NAME is the proper name of the signal. The names used in the print set are also used in this manual. POLARITY is either H or L to indicate the voltage level of the signal. H means +3 V; L means ground. As an example, the signal:

(S2) SELECT H

originates on sheet 2 of the M7190 module drawing and is read, when SELECT is true, this signal is at +3V.
UNIBUS signal lines do not carry a SOURCE indicator. These signal names represent a bidirectional wire-ORed bus; as a result, multiple sources for a particular bus signal exist. Each UNIBUS signal name is prefixed with the word BUS.

4.3 GENERAL DESCRIPTION

4.4 FUNCTIONAL BLOCK DESCRIPTION

4.4.1 UNIBUS Interface

The DZS11-EA UNIBUS interface provides access for the DZS11-EA system to the PDP-11 UNIBUS. All signals that pass between the UNIBUS and the DZS11-EA are routed through the interface. This logic can be divided into three major areas: Address Selection, Data Transceivers and Interrupt Control. These are shown in Figure 4-1.
The interface logic performs the following functions:-

1. Selection and recognition of the DZS11-EA addresses and device registers.

2. Determination of the DZS11-EA mode of operation with the PDP-11 processor (DATI or DATO Word or Byte).

3. Handling of data to and from the microcontroller interface.

4. Controlling interrupts between the DZS11-EA and PDP-11 processor.

4.4.1.1 Address Selection

The address selection logic determines the DZS11-EA device address and recognises that address when it appears on the UNIBUS. A recognised address indicates that the DZS11-EA has been selected by the processor or another bus "master". The desired address is selected by switches that correspond to UNIBUS address bits Ø3 through 12. Bits 13 through 17 are always decoded as binary 1s. Bits ØØ through Ø2 determine which device register is to be selected. This bit scheme allows device addresses from 16ØØØX8 to 17777X8. However, the DZS11-EA uses only the floating address space from 16ØØ1Ø8 to 1637ØØ8. A detailed description of the DZS11-EA address assignments is presented in Appendix B.

4.4.1.2 Interrupt Control

The interrupt control logic handles the processor to UNIBUS to DZS11-EA dialogue to permit processor interrupts. The logic generates the vector address and receives interrupt commands from the CSR. The DZS11-EA operates at priority levels 5A (receiver) and 5B (transmitter). When two DZS11-EA modules are used, the first module (slot 1) has priority over the second (slot 2). The priority insert establishes the DZS11-EA priority level by directing the UNIBUS request and grant signals from the appropriate UNIBUS lines to the DZS11-EA. A series of switches permit alteration of the vector address to suit programming requirements. Refer Appendix B of this manual for vector selection and assignment.

4.4.1.3 Data Transceivers

The data transceivers control the flow of data between UNIBUS and microcontroller interface. Transfer of data and control information between UNIBUS and microcontroller is via a tristate bidirectional bus generated by the data transceivers. The vector bits, determined by the interrupt control logic are transferred to the UNIBUS by the data transceivers.

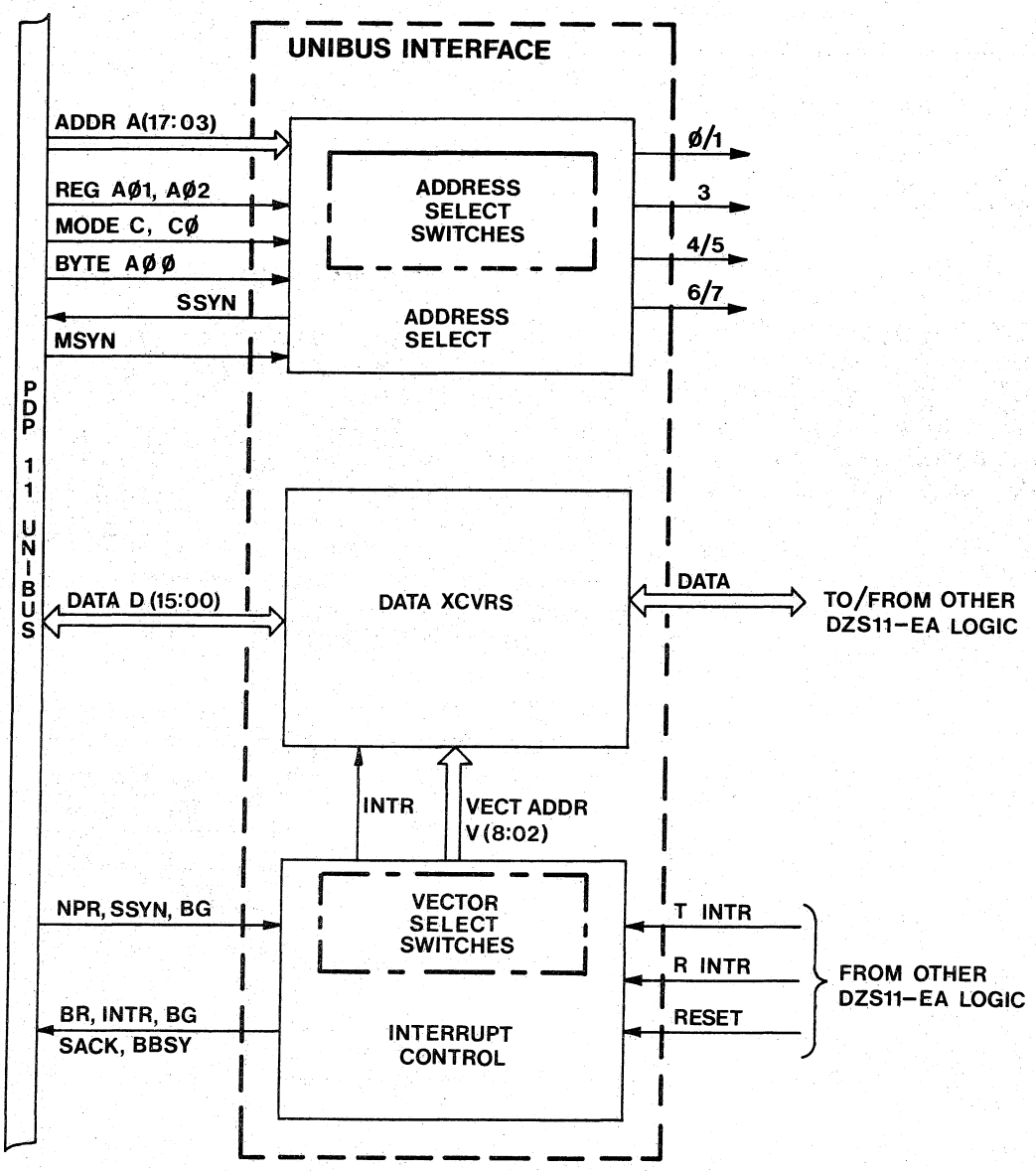


Figure 4-1 UNIBUS Interface Block Diagram

4.4.2 UNIBUS - Microcontroller Interface

The microcontroller interface controls the flow of data and control information between UNIBUS and the microcontroller. This logic can be divided into four major sections: received data silo, transmit control, line control and status silo and UNIBUS registers. These are shown in Figure 4-2. The interface logic performs the following functions:-

- Transfers received data with appended line numbers and status information to the UNIBUS.
- Requests transmit characters from the UNIBUS and passes same through to the microprocessor for transmission via the composite data port and remote VT1XX-EA/EB to the respective asynchronous ports (terminal).
- Transfers line control and parameter information for the remote asynchronous ports, from UNIBUS to microcontroller.
- Transfers DZS11-EA control and status information between UNIBUS and microcontroller.

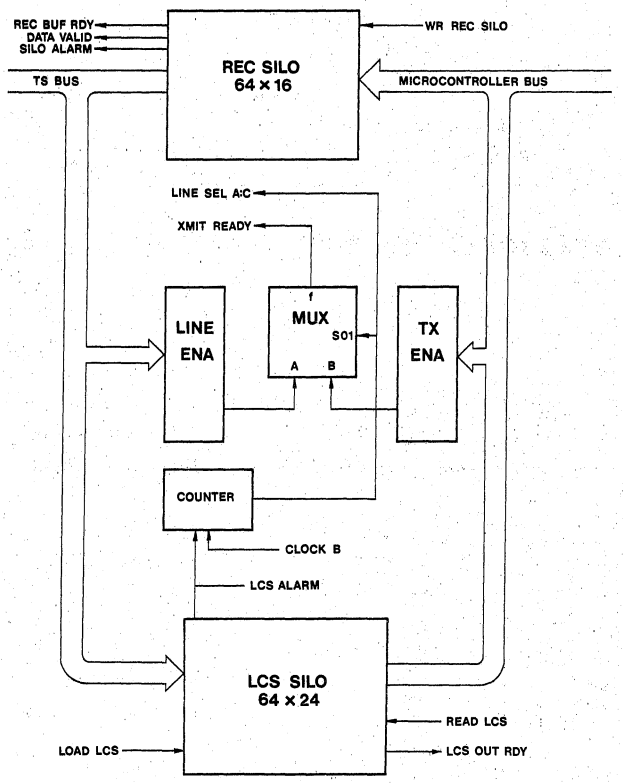


Figure 4-2 UNIBUS - Microcontroller Interface Block Diagram

4.4.2.1 Received Data Silo

The received data silo is an asynchronous first in first out (FIFO) memory. The device is 16 bits wide and 64 locations deep. The received data silo is loaded by the microcontroller and unloaded by the UNIBUS through the RBUF register.

The operation is as follows.

At the remote VT1XX-EA, a character is received from one of 8 asynchronous ports. This character is appended to the next X.25 frame to be transmitted from VT1XX-EA to DZS11-EA via the composite port. The character is appended to the composite X.25 frame along with characters from other asynchronous ports, such that on reception of the X.25 frame, the DZS11-EA is able to unpack the character, encode a 3 bit line number and append to the character.
The character; with 3 bit line number and status bits (ERROR, FRAMING, OVERRUN, PARITY) are then loaded into the receive silo by the microcontroller. The character then ripples to the bottom of the SILO (OUTPUT) where it can be accessed by the UNIBUS via the RBUF register. The receive silo is 16 bits wide enabling each character (5, 6, 7 or 8 bit) to carry with it a 3 bit line number (Ø:78) plus 4 status bits with one space remaining.

4.4.2.2 Transmit Control Logic

The transmit control logic interfaces to both UNIBUS and microcontroller. It's function is to request transmit characters from the UNIBUS via the TBUF register and pass these characters, with a 3 bit line number through to the microcontroller which then in turn includes this character in the next X.25 information (I) frame to be transmitted to the remote VT1XX-EA via the composite link.
The transmit control logic is controlled by two enable registers, one from the UNIBUS and one from the microcontroller. The UNIBUS control register is the Transmit Enable Register (TER) and is used to enable and terminate transmission at the remote VT1XX-EA/EB asynchronous ports. The microcontroller transmit enable register is used to clutch transmit characters, that is when the microcontroller decides that it has sufficient transmit data from the UNIBUS for transfer to the remote VT1XX-EA it uses this register to temporarily suspend UNIBUS requests for transmit characters.

4.4.2.3 Line Control and Status Silo

The line control and status (LCS) silo is an asynchronous first in first out (FIFO) memory. The fifo is 64 words deep by 24 bits wide.

The LCS silo forms the main interface between UNIBUS and microcontroller. All information being written to the DZS11-EA, with the exception of the CSR is written to this FIFO for transfer to the microcontroller. The information passing through this fifo includes:-

- Asynchronous line parameter information (LPR word only)
- Data terminal ready (DTR) bits (TCR high byte only)
- Transmit character and Break register. (TDR word or byte)

The LCS FIFO is similar in operation to the receive data FIFO, with the exception that it's flow is in the reverse direction (UNIBUS to microcontroller) is 24 rather than 16 bits wide, and is sourced from multiple pseudo register on the UNIBUS.

4.4.2.4 UNIBUS Registers

The fourth section of the UNIBUS - Microprocessor interface, known as UNIBUS register is a group of registers that do not directly affect the microcontroller.

These registers include:-

- Control and Status Register (CSR)
- Data Terminal Ready Register
- Ring Register (MSR)
- Carrier Register (MSR)

4.4.3 Microcontroller

The DZS11-EA is a microprocessor-controlled system that utilises the interaction of firmware programs with hardware circuits to enable emulation of the DZ11-A and perform statistical multiplexing functions.
As shown in Figure 4-3, the microcontroller section of the DZS11-EA consists of microprocessor, memory and peripheral devices all communicating via a common data bus. Peripheral devices within the microcontroller section of the DZS11-EA include the following major functional devices:-

- UNIBUS interface
- Programmable clock and baud rate generator
- X.25 Controller

Figure 4-3 Microcontroller Block Diagram

4.4.3.1 Microprocessor

The DZS11-EA firmware is executed by a 8Ø85A eight bit microprocessor running from a 3.Ø72 MHZ clock. Although the microprocessor has a 16 bit memory address space, only part of the address is decoded by the on board memory and I/O devices.

4.4.3.2 Program PROM

The DZS11-EA program PROM is an 1ØK X 8 bit memory (expandable to 16K X 8 bit) containing instructions and data tables for the microprocessor. The memory is implemented in five 2K packages using UV Erasable PROMs type 2716. The DZS11-EA has been designed to optionally accept 4K X 8 bit 2732 devices thus increasing the PROM space to 16K X 8 in 4 packages.
Checksum data stored in each PROM allows the DZS11-EA microcontroller to confirm the condition of its program code at self test.

4.4.3.3 Scratch RAM

The scratch RAM is an 8K X 8 bit memory containing the microprocessor stack, various flag bytes, control tables and communication buffers.

4.4.3.4 Programmable Clock

The microcontroller has three internal timing devices. All are sourced from the one programmable clock, the 8253-5.

Clock "A" is the internal baud rate (bits/second) timing signal for the X.25 communication port. This signal connects directly to the communication connector (J1) and supplies the clock out signal in applications where external modem baud rate timing is not implemented. The same signal can be used in Maintenance applications, i.e. a test connector can be used to connect the clock out timing signal back to the Receive and Transmit timing signals. In addition clock "A" connects to the X.25 controller chip via a 2 to 1 multiplexer. The second port of the multiplexer is the external (modem) timing signal. This enables programmable selection of internal or external baud rate timing.

Clock "B: is an internal timing signal used by the transmit control section of the UNIBUS Microcontroller interface. Clock "B" is programmed by the microprocessor at power up as a square wave signal and runs at variable frequency which is dependent upon the composite port baud rate. This clock sets the rate at which transmit characters are requested from the UNIBUS. The signal clocks a 4 bit counter within the transmit control logic which in turn samples the 8 transmit enable signals from both UNIBUS and microcontroller.

Clock "C" is the microprocessors real time clock. The signal connects to Restart (RST) 7.5 interrupt pin of the 8Ø85 chip. This generates timed interrupts to the micro-program enabling the measurement of time.
The frequency of this interrupt is set to 4.ØØ milli seconds.

4.4.3.5 UNIBUS Interface

The UNIBUS interface consists of ten 8-bit registers. These registers are used for the control and passage of data between UNIBUS and microcontroller. The ten registers fall into five categories:-

- UNIBUS Input (UNIBUS -> MICRO)
- VT1XX-EA/EB received data (Micro -> UNIBUS)
- Transmit Control
- Modem Status (Micro -> UNIBUS)
- Maintenance

The UNIBUS input group consists of four 8-bit registers, all are read only by the microcontroller. They are, the UNIBUS Status register USR, Line Control and Status register 1, 2 and 3.
The USR is a status register only, it contains control flags for the UNIBUS input and receive data, group of registers.
LCS registers 1,2 and 3 are the bottom of a 64 x 24 bit silo used to pass control and transmit data from UNIBUS to the Microcontroller.

The Received Data registers are two 8-bit registers and are the inputs to a 64 x 16 bit silo used for passage of VT1XX-EA/EB received characters from microcontroller to UNIBUS.
The output of the silo is the RBUF register as seen by the UNIBUS.

The Transmit Control Register is a single 8-bit register used by the microcontroller to enable or disable requests made by the transmit control logic for transmit characters from the UNIBUS. This register is used by the microcontroller to suppress the flow of outward data (TX) to the remote terminals via the composite link, i.e. XON XOFF.

The Modem Status group consists of two 8-bit write only registers. These connect directly to the UNIBUS (Carrier Ring) register. These registers exist only for DZ11-A compatibility. At microcontroller initialisation they are cleared to zero and thus read as zero by the UNIBUS.
During UNIBUS maintenance mode, any write to the DTR register will be copied to both the ring and carrier registers.

The fifth group is the maintenance group and consists of two 8-bit registers.
The first is a read only 8-bit switch register. This register is used to set the composite port timing requirement (4 bits) i.e. internal/external time and baud rate.
The second function of the MSR is that of microdiagnostic control. (4 bits) This function enables the continuous operation of selected tests during microdiagnostic mode.
The second maintenance register is an 8-bit write only LED status display. During operation the LEDs are used to indicate microcontroller heart beat and composite port status.

4.4.3.6 Composite Port Controller

The composite port controller consists of two devices, a programmable DMA controller (8237-2) and a HDLC communication protocol controller (8273). These devices connect to the microprocessor control bus and enable the reception and transmission of composite data under direct memory access (DMA) control.
The DMA controller enables the transfer of data between scratch RAM and HDLC controller on demand from the HDLC controller. The HDLC controller maintains the composite data link, by supporting much of the X.25 level 2 protocol requirement such as flag detection, CRC generation and checking, and frame address recognition.

4.5 UNIBUS INTERFACE DETAILED DESCRIPTION

4.5.1 Address Selection Logic

The switches and resistor network (shown at the left of sheet 2) provide a reference voltage to be used by the voltage comparators. These voltages are compared with UNIBUS address bits AØ3 through A12. When a switch is open, a high-level voltage is compared to the incoming address bit; when a switch is closed, a low-level voltage is compared. The output of the voltage comparators are wire-ANDed to provide a signal output that is at a high level when the device is selected. This only happens when the voltages on all three voltage comparators match; otherwise, the output remains low and the device will not respond. For example, if BUS AØ3 through BUS A1Ø are at a high level and BUS A11 and BUS A12 are at a low level, a match only occurs if switches 1 through 8 are closed and switches 9 and 1Ø are open. From the voltage comparator circuitry, the output is inverted and used by the device response logic and the register select and control logic.

The device response logic provides a delay to slave sync to allow for decoding and strobing data.
All DZS11-EA UNIBUS load signals are decoded by the ROM decoder E78.
All UNIBUS register enable signals (UNIBUS Read) are decoded by the 2 to 4 decode E85.

4.5.2 Receiver Interrupt Control

The receiver interrupt signals the processor when the DZS11-EA receives a character from the terminal and stores the character in the RBUF (silo buffer). After processing by the microcontroller, the character is loaded into the silo, and CSR bit Ø7 (RDONE) is set; RDONE causes generation of the RINT signal. RINT is fed to the receiver interrupt logic and the BR signal is transmitted to the processor via the UNIBUS at priority level 5. When the processor status goes below level 5, a BG5 signal is routed through the priority insert (on the DZS11-EA module) to the BG IN input of the receiver interrupt chip, causing generation of MASTER, BUS SACK, and BUS BBSY. The MASTER signal is inverted and gated to create BUS INTR for transmission to the UNIBUS. The receiver interrupt is also caused by silo alarm. INTR is created to strobe the vector address to the UNIBUS from the output data transceivers.

4.5.3 Transmitter Interrupt Control

The transmitter interrupt occurs when the DZS11-EA is engaged in character transmission and the processor must be interrupted to request additional data for transmission. The interrupt sequence begins with assertion of TRDY with TIE set, which generates the TINT pulse. TRDY is the result of the line being enabled and the microcontroller being able to accept a character for that line. The TINT signal begins the processor interrupt dialogue via the UNIBUS. The transmitter interrupt priority is less than that of the receiver; therefore, bus grants are received only when a receiver interrupt is not in process. The transmitter interrupt logic causes generation of the same signals as the receiver logic, including strobing the vector address; however, the transmitter vector is located two words after the receiver vector. For example, a receiver vector of 300 automatically places the transmitter vector at 304.

4.5.4 Data Transceivers

The data transceivers allow data to flow directly to and from the UNIBUS. Line BUS D (15:00) converts information and control data on the UNIBUS to correct levels used by the DZS11-EA and are sent to the device registers by way of the bidirectional line TS BUS (15:00).

4.5.5 Receiver Control Logic

The receiver control logic consists of a 64 x 16 bit silo and alarm counter.
Loading of the silo is controlled by the microcontroller while unloading is controlled by the UNIBUS via the RBUF register. The loading and unloading of the silo is asynchronous.
The receive silo alarm consists of a 4 bit counter, that sets an alarm flag at the count of 16 entries into the silo. The counter is incremented each time the microcontroller writes an entry to the silo and is cleared to zero each time the UNIBUS reads RBUF.
Refer to Section 3 for UNIBUS programming requirement and Section 4.4.8 for the microcontroller programming requirements.

4.5.6 Transmit Control Logic

The transmit control logic is located on sheet 7 of the DZS11-EA print set.

The 4 bit counter E9Ø is clocked by CLOCK B H which is sourced from the microcontroller programmable clock. The three least significant outputs of the 4 bit counter form the transmit request line number XMIT LINE SELA:C and can be read by the UNIBUS as bits 8:1Ø respectively via the DZS11-EAs CSR. In addition to connecting to the CSR, the three bits connect to the select inputs of two 8 to 1 multiplexers E75 and E89.
The inputs to multiplexer E75 are the microcontroller transmit enable bits, one for each of the 8 lines, and are sourced from the microcontroller TER register on sheet 9. The inputs to multiplexer E89 are the UNIBUS transmit enable bits, one for each of the 8 lines, and are sourced from UNIBUS transmit enable register, sheet 4.

The 4 bit counter, E9Ø continuously scans each of the 8 lines at the clock B rate, testing for a condition where both UNIBUS and microcontroller have enabled transmission on a line. If a match is found, the XMIT Ready flag (E115-5) is set, and the enable flag (E115-9) is reset. At this point the 4 bit counter E9Ø is disabled, scanning halts, and the UNIBUS transmit ready flag is set (bit 15 CSR).

The transmit control logic remains in the request state until one of 4 events occurs, they are:-

- A Transmit character is loaded by the UNIBUS into the DZS11-EA
- The UNIBUS lowers (Resets) it's transmit enable bit for the line with the active transmit request.
- The Master scan enable bit is reset.
- The DZS11-EA is reset.

Loading of a transmit character into the TBUF by the UNIBUS, asserts the signal LD XMIT BUF L, clears the XMIT READY flag, sets the enable flag and re-enables the 4 bit scanner.
The transmit character loaded by the UNIBUS is written to the LCS silo for transfer to the microcontroller.

The UNIBUS may terminate a transmit request without transmitting a character. This is accomplished by resetting the UNIBUS transmit enable bit for the respective line. This will cause a High to Low transition on the input of the NAND gate E112-2, will generate a pulse at E112-6 and reset the XMIT ready flag, set the enable flag and restart the scanner.

The remaining two transmit request termination events are device reset and/or resetting master scan enable. Either or both events will cause the transmit request flag to reset, however, the enable flag will remain reset and so no further transmit requests will be detected.

The one remaining controlling event or rather suppression event is the assertion of LCS ALARM (Ø)H.
The signal asserts when an alarm condition of 16 entries has been reached in the line control and status silo (LCS).
The event suppresses all requests for transmit characters until the alarm is reset thus avoiding an overflow of transmit characters in the LCS silo.

4.5.7 UNIBUS Registers

The DZS11-EA uses four device registers in a manner that yields six uniquely accessible registers, each having a 16-bit word capacity. The six discrete registers temporarily store input/output data, establish DZS11-EA operating status, and monitor control signal conditioning. Depending on the function of the register, some are accessible in bytes or words; others are restricted to word-only operations. Since registers can be read or written into, the selection of either a read or write operation allows two of the device registers to function as four independent registers.

The subsequent paragraphs describe the operation of each DZS11-EA UNIBUS register. Refer to Chapter 3 of this manual for additional information regarding register bit assignments, bit functions, and programming techniques.

4.5.7.1 UNIBUS Control and Status Register

The control and status register (CSR) comprises two 74LS175 chips. Additional gates are used to control the register and generate signals that are CSR bits but are not stored in the 74LS175 chips. The UNIBUS lines, after routing through the bus transceivers, direct the operation of the DZS11-EA in accordance with the PDP-11 system requirements. Bits (Ø3:Ø6), 12 and 14 are stored in the CSR chips since they are read or write bits. The CSR is controlled by LD HCSR, LD LCSR signals from the address selection logic. These signals are gated within the address decoder to yield selection of the upper (HCSR) or lower (LCSR) portions of the register. The RINT and TINT signals are produced by the outputs of the CSR and other logic that receive signals required to generate receiver and transmitter interrupt commands. The CSR is reset by a RESET L pulse to the CLR input of the chips. Several bits (ØØ, Ø1, Ø2, and 11) are not used and have no effect on DZS11-EA operation.

4.5.7.2 UNIBUS Receiver Buffer

The receiver buffer (RBUF) is a read-only register that contains the received character (lower byte), the receiver line number (bits Ø8-1Ø), and four character-condition signals relating to errors in reception (bits 12-15). Bit 11 is not used in the RBUF. The RBUF read command is generated in the address select logic. The RD RBUF signal is inverted and fed to the receiver control logic to cause the first-in character of the silo to be read from the "bottom" (RBUF) of the silo. The trailing edge of the RD RBUF command causes a SHO H signal to be sent to the silo to shift the next character down through the 16-character positions.

4.5.7.3 UNIBUS Line Parameter Register

The line parameter register (LPR) is a write-only segment of device register 2. The LPR is a pseudo register, that is, it does not physically exist within the DZS11-EA hardware. All write operations to the LPR register address are written to the LCS silo for transfer to the microcontroller. The microcontroller maintains an LPR register for each of the 8 communication channels. On detection of change of LPR or following initialisation, the LPR data is transmitted via the composite communication link to the remote VT1XX-EA, enabling re-initialisation of UART parameters.
The LPR contains various line parameters such as line number, character length, stop code, parity, DZS11-EA asynchronous port baud rate, and a receive enable bit.

4.5.7.4 UNIBUS Transmit Control Register

The transmit control register (TCR) is a read/write register that comprises two 8542 read write 4-bit registers and one 8 bit 74LS299 read write register.
The two 8542 registers are used for the low byte and contain the line transmission enable bits.
The 8 bit 74LS299 is written from the high byte and is the data terminal ready bits DTR. Writing to the DTR register will cause a parallel entry of identical data to the LCS silo. The microcontroller transmits this information to the remote VT1XX-EA on change. The 74LS299 8 bit register is included in hardware too because it is a Read/Write register and thus enabling DZ11-A compatibility.

4.5.7.5 UNIBUS Modem Status Register

The modem status register (MSR) is a read only segment of device register 6. The MSR is updated by the microcontroller and reflects the status of the carrier and ring signals of the remote asynchronous port.
The register is dynamic in that it represents the current state of the carrier and ring lines. These lines must be continuously monitored, as transitions on them do not cause interrupts.

4.5.7.6 UNIBUS Transmit Data Register

The transmit data register (TDR) is a write-only segment of device register 6. The TDR register is a pseudo register, that is, it does not physically exist within the DZS11-EA hardware. All write operations to the TDR are written directly to the LCS silo for transfer to the microcontroller. The data is then transmitted to the remote VT1XX-EA via the composite data link.

The low byte of this register contains the transmit character, the high byte contains the break registers. Setting of a break bit will cause the respective asynchronous port at the VT1XX-EA to be placed into a break condition (space condition).

4.6 MICROCONTROLLER DETAILED DESCRIPTION

The DZS11-EA has an 8085 microprocessor at the heart of its intelligence. The 8085 performs all the usual functions of a stored program computer, fetching instructions and data from ROM and RAM and responding to service requests from various devices in the system.

4.6.1 8085 Microprocessor

The 8085 (Figure 4-4) contains a set of general and special purpose registers (the register array), timing and control logic which responds to machine code instructions, and an accumulator and arithmetic logic unit which performs the computations associated with the microprocessor operation.

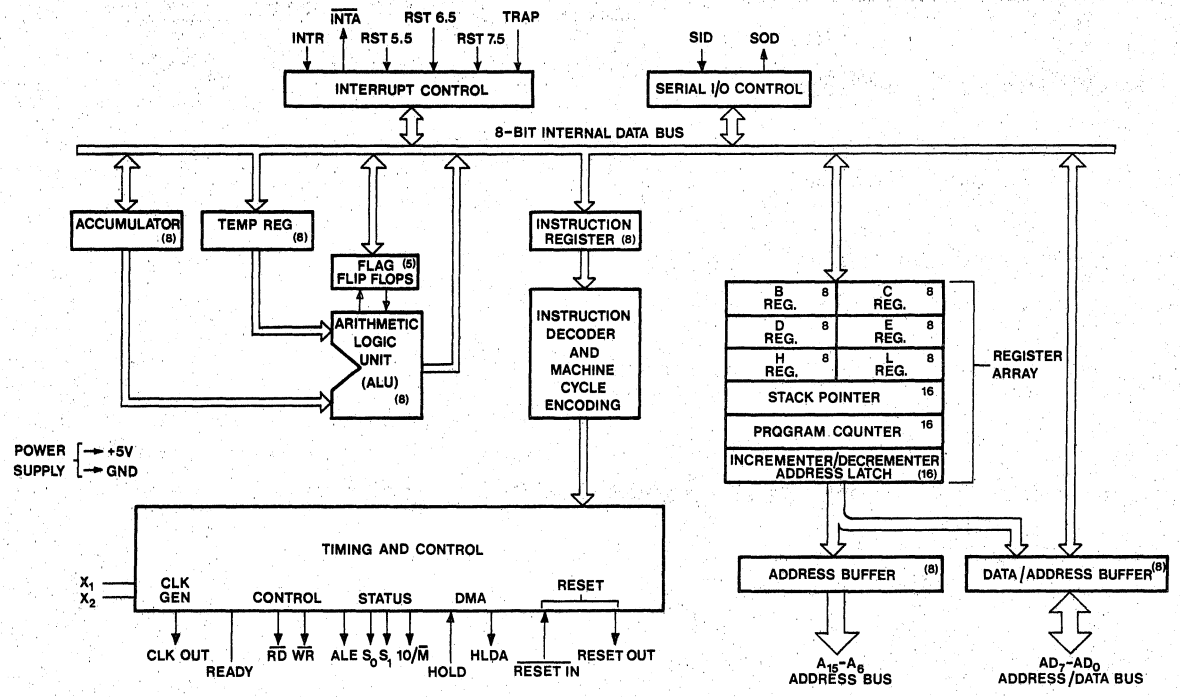


Figure 4-4 8085 Block Diagram

Most of the pins on the 8085 are tristate data and address lines. The following is a list of 8085 pins with descriptions.

Table 4-1 8085 Pin Descriptions

Pin	Symbol	Function
21:21	A8-A15	Address Bus: The most significant 8 bits of the memory address or the 8 bits of the I/O address, 3-stated during Hold and Halt modes and during RESET.
12:19	AD0:7	Multiplexed Address/Data Bus: Lower 8 bits of the memory address (or I/O address) appear on the bus during the first clock cycle (T state) of a machine cycle. It then becomes the data bus during the second and third clock cycles.
30	ALE	Address Latch Enable: It occurs during the first clock state of a machine cycle and latches the low order address bits into the 74LS373 address latch. The falling edge of ALE is set to guarantee setup and hold times for the address information. ALE is never 3-stated.
29 33 34	S0 S1 IO/M	Machine cycle status: See Section 4.6.2
32	RD	READ control: A low level on RD indicates the selected memory or I/O device is to be read and that the Data Bus is available for the data transfer, 3-stated during Hold and Halt modes and during RESET.

Table 4-1 8085 Pin descriptions cont:

Pin	Symbol	Function
31	WR	WRITE control: A low level on WR indicates the data on the Data Bus is to be written into the selected memory or I/O location. Data is set up at the trailing edge of WR. 3-stated during Hold and Halt modes and during RESET.
35	READY	If READY is high during a read or write cycle, it indicates that the memory or peripheral is ready to send or receive data. If READY is low, the CPU will wait an integral number of clock cycles for READY to go high before completing the read or write cycle. Ready is permanently set high.
39	HOLD	HOLD indicates that the DMA controller is requesting the use of the address and data buses. The CPU, upon receiving the hold request, will relinquish the use of the bus at the completion of the current bus transfer. Internal processing can continue. The processor can regain the bus only after the HOLD is removed. When the HOLD is acknowledged, the Address, Data, RD, WR, and IO/M lines are 3-stated.
38	HLDA	HOLD ACKNOWLEDGE: Indicates that the CPU has received the HOLD request and that it will relinquish the bus in the next clock cycle. HLDA goes low after the Hold request is removed. The CPU takes the bus one half clock cycle after HLDA goes low.

Table 4-1 8Ø85 Pin Descriptions cont:

Pin	Symbol	Function
1Ø	INTR	INTERRUPT REQUEST: is used as a general purpose interrupt. It is sampled only during the next to the last clock cycle of an instruction and during Hold and Halt states. If it is active, the Program Counter (PC) will be inhibited from incrementing and an INTA will be issued. During this cycle a RESTART instruction is inserted to jump to the interrupt service routine. The INTR is enabled and disabled by software. It is disabled by Reset and immediately after an interrupt is accepted.
11	INTA	INTERRUPT ACKNOWLEDGE: Is used instead of (and has the same timing as) RD during the instruction cycle after an INTR is accepted. It can be used to activate the 81LS97.
9 8 7	RST 5.5 RST 6.5 RST 7.5	RESTART INTERRUPTS: These three inputs have the same timing as INTR except they cause an internal RESTART to be automatically inserted. The priority of these interrupts is ordered as shown in Table 4-4. These interrupts have a higher priority than INTR. In addition, they may be individually masked out using the SIM instruction.
6	TRAP	Trap interrupt is a nonmaskable RESTART interrupt. It is recognised at the same time as INTR or RST 5.5-7.5. It is un-affected by any mask or interrupt Enable. It has the highest priority of any interrupt.

Table 4-1 8085 Pin Descriptions cont:

Pin	Symbol	Function
36	RESET IN	Sets the Program Counter to zero and resets the Interrupt Enable and HLDA flip-flops. The data and address buses and the control lines are 3-stated during RESET and because of the asynchronous nature of RESET, the processor's internal registers and flags may be altered by RESET with unpredictable results. RESET IN is a Schmitt-triggered input, allowing connection to an R-C network for power-on RESET delay. The CPU is held in the reset condition as long as RESET IN is applied.
3	RESET OUT	Indicates CPU is being reset. Is used as a system reset. The signal is synchronised to the processor clock and lasts an integral number of clock periods.
1 2	X1, X2,	X1 and X2 are connected to a 6.144 MHZ crystal, to drive the internal clock generator. The input frequency is divided by 2 to give the processor's internal operating frequency of 3.072 MHZ.
37	CLK	Clock Output for use as a system clock. The period of the clock is 325 nano seconds.
5	SID	Serial input data line. The data on this line is loaded into accumulator bit 7 whenever a RIM instruction is executed. This bit is not used.
4	SOD	Serial output data line. The output SID is set or reset as specified by the SIM instruction. This bit is not used.
40	Vcc	+5 volt supply.
20	GND	Ground Reference.

4.6.2 Bus Timing

The 8Ø85A has a Multiplexed Data Bus. ALE is used as a strobe to sample the lower 8-bits of address on the Data Bus. Figure 4-5 shows an instruction fetch, memory read and I/O write cycle (as would occur during processing of the OUT instruction). Note that during the I/O write and read cycle that the I/O port address is copied on both the upper and lower half of the address.

There are seven possible types of machine cycles. Which of these seven takes place is defined by the status of the three status lines (IO/M, S1, SØ) and the three control signals (RD, WR, and INTA). (See Table 4-2).

A machine cycle normally consists of three T states, with the exception of OPCODE FETCH, which normally has either four or six T states (unless WAIT or HOLD states are forced by the receipt of READY or HOLD inputs). Any T state must be one of ten possible states.

Table 4-2 8Ø85A Machine Cycle Chart

MACHINE CYCLE	STATUS			CONTROL		
	IO/M	S1	SØ	RD	WR	INTA
OPCODE FETCH (OF)	Ø	1	1	Ø	1	1
MEMORY READ (MR)	Ø	1	Ø	Ø	1	1
MEMORY WRITE (MW)	Ø	Ø	1	1	Ø	1
I/O READ (IOR)	1	1	Ø	Ø	1	1
I/O WRITE (IOW)	1	Ø	1	1	Ø	1
ACK. INTR (INA)	1	1	1	1	1	Ø
BUS IDLE (Bl):	Ø	1	Ø	1	1	1
RST TRAP	1	1	1	1	1	1
HALT	TS	Ø	Ø	TS	TS	1

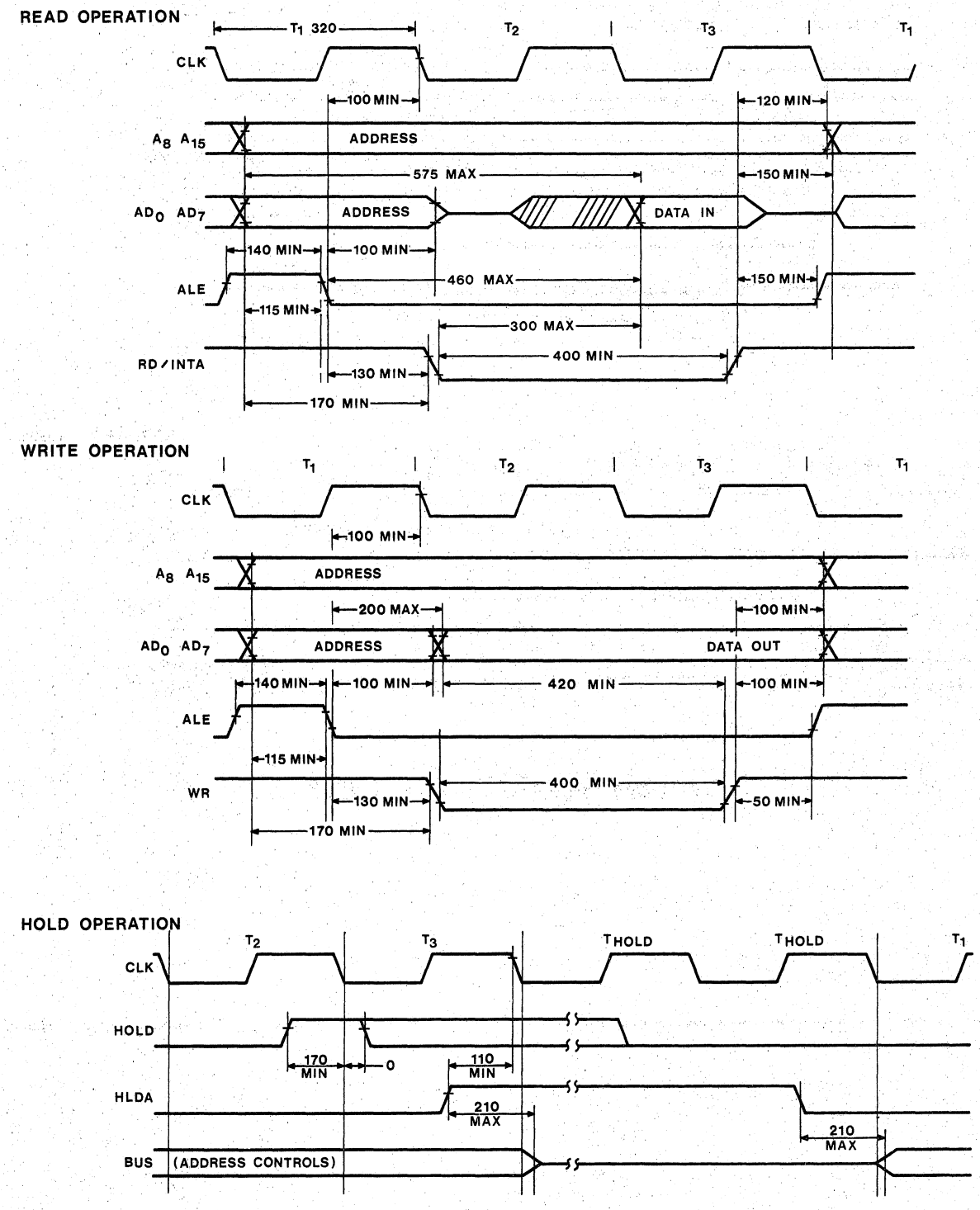


Figure 4-5 8085 Bus Timing

4.6.3 Microprocessor Memory

The basic DZS11-EA contains 10K bytes of program PROM and 8K bytes of static RAM. (One byte = 8 bits).
The 10K bytes of PROM are configurable with 5 sockets enabling the insertion of 2716 devices. The first four sockets (E2 to E5) can be modified by changing wire link W1:W4 (see section 2.5.1) to accept 2732 (4K X 8) devices thus enabling a maximum of 16K bytes of PROM space.
The RAM is sixteen 1K X 4 ICs arranged in pairs. The microprocessor can address up to 64K memory locations.

4.6.3.1 Memory Decoding

PROM addressing space is from 0 to 16K. When IOMH is asserted and MEM REQ H is asserted the memory decoder is enabled. The AND condition of IOMH, not EXT MEM H and MEM REQ H assert E35-6 and enable the ROM decoder E6.
E6 pin 7 enables the 74LS138 RAM decoder which in turn decodes the RAM page from 16K to 24K in 1K increments.
The signal EXT MEM L connects to the option port J2 and is used by option to overlay or disable memory locations by the assertion of this signal.

4.6.4 Microprocessor Memory I/O Map

The I/O page is mapped to its own I/O page in addition to being mapped into the top 32K of the memory page. This enables I/O devices to be addressed via the standard I/O page using the IN and OUT instructions or via the memory page using memory reference instructions, example MOV r, M. This mapping procedure enables the following I/O manipulations.

Via I/O page

```
        IN              ;read I/O register
        OUT             ;load I/O register
```

Via memory page

```
        Move r, M       ;move memory to register
        Move M, r       ;move register to memory
        MVI M           ;move immediate memory
        LHLD            ;load H and L direct
        SHLD            ;store H and L direct
        ADD M           ;add memory to A
        ANA M           ;and memory with A
        LDA             ;load A direct
        STA             ;store A direct
```

Table 4-3 lists the I/O address assignments for both the memory and I/O page.
Table 4-3 lists the I/O interrupt vectors.

Table 4-3 Microcontroller Address Assignments

Device	Type	I/O Page	Memory Page
DMA (8237-5)	RD/WR	8Ø HEX	8ØØØ HEX
COMM (8273)	RD/WR	AØ HEX	AØØØ HEX
CLK (8253-5)	RD/WR	CO HEX	CØØØ HEX
PIE Ø (8255-5)			
- LCS 1	RD	C4 HEX	CØØ4 HEX
- LCS 2	RD	C5 HEX	CØØ5 HEX
- LCS 3	RD	C6 HEX	CØØ6 HEX
- PIE Ø CONTROL	RD/WR	C7 HEX	CØØ7 HEX
PIE 1 (8255-5)			
- MSR	RD	C8 HEX	CØØ8 HEX
- TER	WR	C9 HEX	CØØ9 HEX
- USR	RD	CA HEX	CØØA HEX
- PIE 1 CONTROL	RD/WR	CB HEX	CØØB HEX
RING	WR	CC HEX	CØØC HEX
CARRIER	WR	CD HEX	COOD HEX
STATUS	WR	CE HEX	COOE HEX
RECEIVE SILO Ø	WR	C4 HEX	CØ1Ø HEX
RECEIVE SILO 1	WR	C5 HEX	CØ11 HEX

Table 4-4 Microcontroller Vector Addresses

INTR	PRIORITY	VECTOR	DEVICE
TRAP	1	24H	NOT USED
RST 7.5	2	3CH	REAL TIME CLOCK
RST 6.5	3	34H	X.25 RECEIVE
RST 5.5	4	2CH	X.25 TRANSMIT
RST 7:1	5		NOT USED
RST Ø	5	ØØH	RESET

4.6.5 I/O Decoding

As mentioned in Section 4.6.4, I/O devices can be addressed via the I/O page using the In and OUT instruction or via the memory page using memory reference instruction. The latter enables double byte operations e.g. LDLD and SHLD.
The I/O decoder consists of a ROM decoder E76 and the 74LS139 decoder E85 (sheet 11). The 74LS139 decoder E85 is enabled by the negation of address bit 15 (32K to 64K) and selects the DMA controller, communication controller, and the ROM decoder E76 which decodes the UNIBUS I/O select line.

4.6.6 Interrupt Vectors

The 8Ø85A has 5 interrupt inputs: INTR, RST 5.5, RST 6.5, RST 7.5, and TRAP. Each of the three RESTART inputs, 5.5, 6.5, and 7.5, has a programmable mask. INTR and TRAP are not used. Restart 7.5 is connected to CLOCK CH and is the microcontrollers real time clock. RESTART 6.5 is composite port receiver interrupt and RESTART 5.5 is the composite port transmit interrupt.

The three maskable interrupts cause the internal execution of RESTART (saving the program counter in the stack and branching to the RESTART address) if the interrupts are enabled and if the interrupt mask is not set.

There are two different types of inputs in the restart interrupts. RST 5.5 and RST 6.5 are high level-sensitive like INTR and are recognized with the same timing as INTR. RST 7.5 is rising edge-sensitive.

For RST 7.5, only a pulse is required to set an internal flip-flop which generates the internal interrupt request. The RST 7.5 request flip-flop remains set until the request is serviced. Then it is reset automatically. This flip-flop may also be reset by using the SIM instruction or by issuing a RESET IN to the 8085A. The RST 7.5 internal flip-flop will be set by a pulse on the RST 7.5 pin even when the RST 7.5 interrupt is masked out.

The status of the three RST interrupt masks can only be affected by the SIM instruction and RESET IN.

The interrupts are arranged in a fixed priority that determines which interrupt is to be recognized if more than one is pending as follows: TRAP - highest priority, RST 7.5, RST 6.5, RST 5.5, INTR - lowest priority. This priority scheme does not take into account the priority of a routine that was started by a higher priority interrupt. RST 5.5 can interrupt a RST 7.5 routine if the interrupts are re-enabled before the end of the RST 7.5 routine.

4.6.7 Microcontroller Clock

An 8253-5 programmable internal timer is used by the microcontroller to provide a real time clock in addition to two other timing functions. The 8253-5 has an assigned microcontroller bus address as specified by Table 4-3. Clock A is used by the composite port controller for baud rate timing, clock B is used for the UNIBUS transmit control logic timing and clock C is used as the microcontroller real time clock.

At power up the microprocessor initialises the 8253-5 for the desired mode of operation which includes, output type, and signal frequency.
Both A and B clock are initialised into mode 3, (square wave output). The frequency of clock A is set to the composite port baud rate which is defined by the mode switch register. Clock B drives the transmit control scanner (S7) and thus controls the rate at which transmit characters are requested from the UNIBUS. Transmit characters are only requested as fast as they can be transferred via the composite port, and so clock B frequency is set relative to CLOCK A the composite port baud rate.
Table 4-4 lists frequency of clocks A and B against composite port baud rate.

Following system initialisation, clock C is initialised into mode 2, (Rate generator). In this mode, clock C provides a low going edge on the RST 7.5 input of the 8085 at 4.00 milli second intervals. The microcode uses this signal as a means of measuring the passage of time.

Table 4-5 Clock A and B Frequency Settings

CLOCK A		CLOCK B		COMPOSITE PORT
FREQ HZ	PERIOD MICRO S	FREQ HZ	PERIOD MICRO S	BAUD RATE
1200	833.3	2400	416.6	1200 BAUD
2400	416.6	4800	208.3	2400 BAUD
4800	208.3	9600	104.2	4800 BAUD
9600	104.2	19200	52.1	9600 BAUD
19200	52.1	38400	26.0	19200 BAUD

4.6.7.1 Clock Operational Description

The complete functional definition of the 8253-5 is programmed by the microprocessor. A set of control words must be sent out by the CPU to initialise each counter of the 8253 with the desired MODE and quantity information. These control words program the MODE.

All counter modes are programmed by the microprocessor using I/O operations on the Control Word Register (address C3 HEX). Table 4-5 details the control word format.

Table 4-6 8253 Control Word Format

<table>
<tr><th>Bit</th><th>Name</th><th>Meaning</th></tr>
<tr><td>7:6</td><td>SC1:SCØ</td><td>Used to select counter.
<table><tr><th>SC1</th><th>SCØ</th><th>Meaning</th></tr><tr><td>Ø</td><td>Ø</td><td>Counter Ø</td></tr><tr><td>Ø</td><td>1</td><td>Counter 1</td></tr><tr><td>1</td><td>Ø</td><td>Counter 2</td></tr><tr><td>1</td><td>1</td><td>Illegal</td></tr></table></td></tr>
<tr><td>5:4</td><td>RL1:RLØ</td><td>Read/load select bits
<table><tr><th>RL1</th><th>RLØ</th><th>Meaning</th></tr><tr><td>Ø</td><td>Ø</td><td>Counter Latch</td></tr><tr><td>Ø</td><td>1</td><td>Read/load MS Byte</td></tr><tr><td>1</td><td>Ø</td><td>Read/load LS Byte</td></tr><tr><td>1</td><td>1</td><td>Read/load LSB/MSB</td></tr></table></td></tr>
<tr><td>3:2:1</td><td>M2:M1:MØ</td><td>Select Count Mode
<table><tr><th>M2</th><th>M1</th><th>MØ</th><th>Meaning</th></tr><tr><td>Ø</td><td>Ø</td><td>Ø</td><td>Mode Ø (Not used)</td></tr><tr><td>Ø</td><td>Ø</td><td>1</td><td>Mode 1 (Not used)</td></tr><tr><td>Ø</td><td>1</td><td>Ø</td><td>Rate generator.</td></tr><tr><td>Ø</td><td>1</td><td>1</td><td>Square wave gen.</td></tr><tr><td>Ø</td><td>Ø</td><td>Ø</td><td>Mode 4 (Not used)</td></tr><tr><td>1</td><td>Ø</td><td>1</td><td>Mode 5 (Not used)</td></tr></table></td></tr>
<tr><td>Ø</td><td>BCD</td><td>Used to select mode of counting
Ø = Binary counter
1 = B.C.D. counter. (4 DECADES)</td></tr>
</table>

The count register is not loaded until the count value is written (one or two bytes, depending on the mode selected by the RL bits), followed by a rising edge and a falling edge of the clock. Any read of the counter prior to that falling clock edge may yield invalid data.

MODE 2: Rate Generator. Divide by N counter. The output will be low for one period of the input clock. The period from one output pulse to the next equals the number of input counts in the count register. If the count register is reloaded between output pulses the present period will not be affected, but the subsequent period will reflect the new value.

MODE 3: Square Wave Rate Generator. Similar to MODE 2 except that the output will remain high until one half of the count has been completed (for even numbers) and go low for the other half of the count. This is accomplished by decrementing the counter by two on the falling edge of each clock pulse. When the counter reaches terminal count, the state of the output is changed and the counter is reloaded with the full count and the whole process is repeated.

If the count is odd and the output is high, the first clock pulse (after the count is loaded) decrements the count by 1. Subsequent clock pulses decrement the clock by 2. After timeout, the output goes low and the full count is reloaded. The first clock pulse (following the reload) decrements the counter by 3. Subsequent clock pulses decrement the count by 2 until timeout. Then the whole process is repeated. In this way, if the count is odd, the output will be high for (N+1)/2 counts and low for (N-1)/2 counts.

4.7 COMPOSITE PORT COMMUNICATION CONTROLLER

The composite port communication controller is a DMA X.25 communication controller consisting of a 8237-5 DMA controller and an 8237 HDLC controller. Microcontroller bus address for the devices are listed in section 4.6.4., Table 4-3.

4.7.1 DMA Controller

The 8237 contains 344 bits of internal memory in the form of registers. Table 4-6 lists the register names and shows the size of each. A detailed description of the registers and their functions can be found under Register Description.

Table 4-7 8237 Internal Registers

Name	Size	Number
Base Address Registers	16 bits	4
Base Word Count Registers	16 bits	4
Current Address Registers	16 bits	4
Current Word Count Registers	16 bits	4
Temporary Address Register	16 bits	1
Temporary Word Count Register	16 bits	1
Status Register	8 bits	1
Command Register	8 bits	1
Temporary Register	8 bits	1
Mode Registers	6 bits	4
Mask Register	4 bits	1
Request Register	4 bits	1

The following is a list of 8237-2 pins and definitions.

CLK (Clock,Input)
This input controls the internal operations of the 8237 and its rate of data transfers. This pin is driven at 3.Ø72 MHZ.

CS (Chip Select,Input)
Chip Select is an active low input used to select the 8237 as an I/O device during the Idle cycle. This allows CPU communication on the data bus.

RESET (Reset,Input)
Reset is an asynchronous active high input which clears the Command, Status, Request and Temporary registers. It also clears the first/last flip/flop and sets the Mask register. Following a Reset the device is in the Idle cycle.

READY (Ready,Input)
Ready is an input normally used to extend the memory read and write pulses from the 8237 to accommodate slow memories or I/O peripheral devices.

HLDA (Hold Acknowledge,Input)
The active high Hold Acknowledge from the CPU indicates that control of the system bus has been relinquished.

DREQØ-DREQ3 (DMA Request,Input)
The DMA Request lines are individual asynchronous channel request inputs used by peripheral circuits to obtain DMA service. In Fixed Priority, DREQØ has the highest priority and DREQ3 has the lowest priority. A request is generated by activating the DREQ line of a channel. DACK will acknowledge the recognition of DREQ signal. Polarity of DREQ is programmable. Reset initialises these lines to active high. DREQ must be maintained until the corresponding DACK goes active.

DBØ-DB7 (Data Bus,Input/Output)
The Data Bus lines are bidirectional three-state signals connected to the system data bus. The outputs are enabled in the condition during the I/O Read to output the contents of an Address register, a Status register, the Temporary register or a Word Count register to the CPU. The outputs are disabled and the inputs are read during an I/O Write cycle when the CPU is programming the 8237 control registers. During DMA cycles the most significant 8 bits of the address are output onto the data bus to be strobed into an external latch by ABSTB. In memory-to-memory operations, data from the memory comes into the 8237 on the data bus during the read-from-memory transfer. In the write-to-memory transfer, the data bus outputs place the data into the new memory location.

IOR (I/O Read,Input/Output)
I/O Read is a bidirectional active low three-state line. In the Idle cycle, it is an input control signal used by the CPU to read the control registers. In the Active cycle, it is an output control signal used by the 8237 to access data from a peripheral during a DMA Write transfer.

IOW (I/O Write,Input/Output)
I/O Write is a bidirectional active low three-state line. In the idle cycle, it is an input control signal used by the CPU to load information into the 8237. In the Active cycle, it is an output control signal used by the 8237 to load data to the peripheral during a DMA Read transfer.

EOP (End of Process,Input/Output)
EOP is an active low bidirectional signal. Information concerning the completion of DMA services is available at the bidirectional EOP pin. The 8237 allows an external signal to terminate an active DMA service. This is accomplished by pulling the EOP input low with an external EOP signal. The 8237 also generates a pulse when the terminal count (TC) for any channel is reached. This generates an EOP signal which is output through the EOP Line. The reception of EOP, either internal or external, will cause the 8237 to terminate the service, reset the request, and, if Autoinitialise is enabled, to write the base registers to the current registers of that channel. The mask bit and TC bit in the status word will be set for the currently active channel by EOP unless the channel is programmed for Autoinitialise. In that case, the mask bit remains clear. During memory-to-memory transfers, EOP will be output when the TC for channel 1 occurs. EOP chould be tied high with a pull-up resistor if it is not used to prevent erroneous end of process inputs.

A0-A3 (Address,Input/Output)
The four least significant address lines are bidirectional three-state signals. In the Idle cycle they are inputs and are used by the 8237 to address the control register to be loaded or read. In the Active cycle they are outputs and provide the lower 4 bits of the output address.

A4-A7 (Address,Output)
The four most significant address lines are three-state outputs and provide 4 bits of address. These lines are enabled only during the DMA service.

HRQ (Hold Request,Output)
This is the Hold Request to the CPU and is used to request control of the system bus. If the corresponding mask bit is clear, the presence of any valid DREQ causes the 8237 to issue the HRQ. After HRQ goes active at least one clock cycle (TCY) must occur before HLDA goes active.

DACKØ-DACK3 (DMA Acknowledge,Output)
DMA Acknowledge is used to notify the individual peripherals when one has been granted a DMA cycle. The sense of these lines is programmable. Reset initialises them to active low. This output enables the 8-bit latch containing the upper 8 address bits onto the system address bus. AEN can also be used to disable other system bus drivers during DMA transfers. AEN is active HIGH.

ADSTB (Address Strobe,Output)
The active high Address Strobe is used to strobe the upper address byte into an external latch.

MEMR (Memory Read,Output)
The Memory Read signal is an active low three-state output used to access data from the selected memory location during DMA Read or a memory-to-memory transfer.

MEMW (Memory Write,Output)
The Memory Write signal is an active low three-state output used to write data to the selected memory location during a DMA Write or a memory-to-memory transfer.

4.7.1.1 DMA Operation

The 8237 is designed to operate in two major cycles. These are called Idle and Active cycles. Each device cycle is made up of a number of states. The 8237 can assume seven separate states, each composed of one full clock period. State I (SI) is the inactive state. It is entered when the 8237 has no valid DMA requests pending. While in SI, the DMA controller is inactive but may be in the Program Condition, being programmed by the processor. State 0 (SO) is the first state of a DMA service. The 8237 has requested a hold but the processor has not yet returned an acknowledge. An acknowledge from the CPU will signal that transfer may begin. S1, S2, S3 and S4 are the working states of the DMA service.

4.7.1.2 Idle Cycle

When no channel is requesting service, the 8237 will enter the Idle cycle and perform "SI" states. In this cycle the 8237 will sample the DREQ lines every clock cycle to determine if any channel is requesting a DMA service. The device will also sample CS, looking for an attempt by the microprocessor to write or read the internal registers of the 8237. When CS is low and HRQ is low, the 8237 enters the Program Condition. The CPU can now establish, change or inspect the internal definition of the device by reading from or writing to the internal registers. Address lines AØ-A3 are inputs to the device and select which registers will be read or written. The IOR and IOW lines are used to select and time reads or writes. Due to the number and size of the internal registers, an internal flip-flop is used to generate an additional bit of address. This bit is used to determine the upper or lower byte of the 16-bit Address and Word Count registers. The flip-flop is reset by Master Clear or Reset. A separate software command can also reset this flip-flop.

Special software commands can be executed by the 8237 in the Program Condition. The commands are decoded as sets of addresses with the CS and IOW. The commands do not make use of the data bus. Instructions include Clear First/Last Flip-flop and Master Clear.

4.7.1.3 Active Cycle

When the 8237 is in the Idle cycle and a channel requests a DMA service, the device will output an HRQ to the microprocessor and enter the Active cycle. It is in this cycle that the DMA service will take place in the following mode.

The 8237 uses a Rotating Priority. The last channel to get service becomes the lowest priority channel with the others rotating accordingly.

With Rotating Priority in a single chip DMA system, any device requesting service is guaranteed to be recognized after no more than three higher priority services have occurred. This prevents any one channel from monopolising the system.

4.7.1.4 Address Generation

In order to reduce pin count, the 8237 multiplexes the eight higher order address bits on the data lines. State S1 is used to output the higher order address bits to the external latch (74LS37) from which they are placed on the address bus. The falling edge of Address Strobe (ADSTB) is used to load these bits from the data lines to the latch. Address Enable (AEN) is used to enable the bits onto the address bus through a three-state enable. The lower order address bits are output by the 8237 directly.

During Block and Demand Transfer mode services, which include multiple transfers, the addresses generated will be sequential. For many transfers the data held in the external address latch will remain the same. This data need only change when a carry or borrow from A7 to A8 takes place in the normal sequence of addresses. To save time and speed transfers, the 8237 executes S1 states only when updating of A8-A15 in the latch is necessary. This means for long services, S1 states may occur only once every 256 transfers.

4.7.1.5 Current Address Register

Each channel has a 16-bit Current Address register. This register holds the value of the address used during DMA transfers. The address is automatically incremented or decremented after each transfer and the intermediate values of the address are stored in the Current Address register during the transfer. This register is written or read by the microprocessor in successive 8-bit bytes.

4.7.1.6 Current Word Register

Each channel has a 16-bit Current Word Count register. This register holds the number of transfers to be performed. The word count is decremented after each transfer. The intermediate value of the word count is stored in the register during the transfer. When the value in the register goes to zero, a TC will be generated. This register is loaded or read in successive 8-bit bytes by the microprocessor in the Program Condition.

4.7.1.7 Base Address and Base Word Count Registers

Each channel has a pair of Base Address and Base Word Count registers. These 16-bit registers store the original value of their associated current registers. During Autoinitialise these values are used to restore the current registers to their original values. The base registers are written simultaneously with their corresponding current register in 8-bit bytes in the Program Condition by the microprocessor. These registers cannot be read by the microprocessor.

4.7.1.8 Command Register

This 8-bit register controls the operation of the 8237. It is programmed by the microprocessor in the Program Condition and is cleared by Reset.

4.7.1.9 Mode Register

Each channel has a 6-bit Mode register associated with it. When the register is being written to by the microprocessor in the Program Condition, bits Ø and 1 determine which channel Mode register is to be written.

4.7.1.1Ø Request Register

The 8237 can respond to requests for DMA service which are initiated by software as well as by a DREQ. Each channel has a request bit associated with it in the 4-bit Request register. These are non-maskable and subject to prioritisation by the Priority Encoder network. Each register bit is set or reset separately under software control or is cleared upon generation of a TC or external EOP. The entire register is cleared by a Reset. To set or reset a bit, the software loads the proper form of the data word.

4.7.1.11 Mask Register

Each channel has associated with it a mask bit which can be set to disable the incoming DREQ. Each mask bit is set when its associated channel produces an EOP if the channel is not programmed for Autoinitialise. Each bit of the 4-bit Mask register may also be set or cleared separately under software control. The entire register is also set by a Reset. This disables all DMA requests until a clear Mask register instruction allows them to occur. The instruction to separately set or clear the mask bits is similar in form to that used with the Request register.

4.7.1.12 Status Register

The Status register is available to be read out of the 8237 by the microprocessor. It contains information about the status of the devices at this point. This information includes which channels have reached a terminal count and which channels have pending DMA requests. Bits Ø-3 are set every time TC is reached by that channel or an external EOP is applied. These bits are cleared upon Reset and on each Status Read. Bits 4-7 are set whenever their corresponding channel is requesting service.

4.7.1.13 Temporary Register

The Temporary register is used to hold data during memory-to-memory transfers. Following the completion of the transfers, the last word moved can be read by the microprocessor in the Program Condition. The Temporary register always contains the last byte transferred in the previous memory-to-memory operation, unless cleared by a Reset.

Table 4-8 8237 Command Register Bit Definitions

Bit	Meaning
Ø	Memory to memory enable/disable. When set enables memory to memory transfers. When reset disables memory to memory transfers.
1	When set channel Ø current address will be held. When reset channel Ø current address will not be held. This bit is disabled when bit Ø is reset.
2	When set enables controller. When reset disables controller.
3	When set compresses the DMA bus timing. When reset enables normal DMA bus timing. This bit is disabled if memory to memory transfer (bit Ø) is enabled.
4	When set enables rotating DMA priority. When reset enables fixed DMA priority.
5	When set enables extended write pulse selection. When reset enables late write selection.
6	When set, makes DREQ pin active low. When reset, makes DREQ pin active high.
7	When set, makes DACK pin active high. When reset, makes DACK pin active low.

Table 4-9 8237 Mode Register Bit Definitions

Bit	Meaning
Ø:1	Channel Select Bit. ØØ select Ø Ø1 select 1 1Ø select 2 11 select 3
2:3	Transfer Type ØØ Verify transfer Ø1 Write transfer 1Ø Read transfer 11 Illegal Note, disabled if cascade mode selected.
4	When set enables autoinitialisation. When reset disables autoinitialisation.
5	When set, current address register decrements. When reset, current address register increments.
6:7	Mode Select Bits. ØØ Demand mode Ø1 Single mode 1Ø Block mode 11 Cascade mode.

Table 4-1Ø 8237 Request Register Bit Definitions

Bit	Meaning
Ø:1	Channel Select ØØ Channel Ø Ø1 Channel 1 1Ø Channel 2 11 Channel 3
2	When set, will set request bit. When reset, will reset request bit.
3:7	Not used.

Table 4-11 8237 Mask Register Bit Definitions

Bit	Meaning
Ø	When set will set channel Ø mask. When reset will clear channel Ø mask.
1	When set will set channel 1 mask. When reset will clear channel 1 mask.
2	When set will set channel 2 mask. When reset will clear channel 2 mask.
3	When set will set channel 3 mask. When reset will clear channel 3 mask.
4:7	Not used.

Table 4-12 8237 Status Register

Bit	Meaning
Ø:3	Terminal Count (TC) Indicator. Ø - channel Ø 1 - channel 1 2 - channel 2 3 - channel 3
4:7	Channel Request Indicator Ø - channel Ø request 1 - channel 1 request 2 - channel 2 request 3 - channel 3 request

4.7.1.14 Software Commands

These are additional special software commands which can be executed in the Program Condition. They do not depend on any specific bit pattern on the data bus. The two software commands are:

Clear First/Last Flip-Flop: This command is executed prior to writing or reading new address or word count information to the 8237. This initialises the flip-flop to a known state so that subsequent accesses to register contents by the microprocessor will address upper and lower bytes in the corrrect sequence.

Master Clear: This software instruction has the same effect as the hardware Reset. The Command, Status, Request, Temporary, and Internal First/Last Flip-Flop registers are cleared and the Mask register is set. The 8237 will enter the Idle cycle.

Table 4-13 8237 Software Commands

Signals						Operation
A3	A2	A1	AØ	IOR	IOW	
1	Ø	Ø	Ø	Ø	1	Read Status Register
1	Ø	Ø	Ø	1	Ø	Write Command Register
1	Ø	Ø	1	Ø	1	Illegal
1	Ø	Ø	1	1	Ø	Write Request Register
1	Ø	1	Ø	Ø	1	Illegal
1	Ø	1	Ø	1	Ø	Write Single Mask Register Bit
1	Ø	1	1	Ø	1	Illegal
1	Ø	1	1	1	Ø	Write Mode Register
1	Ø	Ø	Ø	Ø	1	Illegal
1	1	Ø	Ø	1	Ø	Clear Byte Pointer Flip/Flop
1	1	Ø	1	Ø	1	Read Temporary Register
1	1	Ø	1	1	Ø	Master Clear
1	1	1	Ø	Ø	1	Illegal
1	1	1	Ø	1	Ø	Illegal
1	1	1	1	Ø	1	Illegal
1	1	1	1	1	Ø	Write All Mask Register Bits

4.7.2 HDLC Controller

The 8273 HDLC controller is a microcomputer peripheral device which supports the International Standards Organization (ISO) High Level Data Link Control (HDLC). This controller minimises CPU software by supporting a comprehensive frame-level instruction set and by hardware implementation of the low level tasks associated with frame assembly/disassembly and data integrity. The data transparency is achieved by using a zero-bit insertion/deletion technique. The frames are automatically checked for errors during reception by verifying the Frame Check Sequence (FCS); the FCS is automatically generated and appended before the final flag in transmit. The 8273 recognizes and can generate flags (Ø1111110), Abort Idle and GA (EOP) characters).

The following is a functional description of each 8273 pin.

Vcc (4Ø)
+5V Supply

GND (2Ø)
Ground

RESET (4)
A high signal on this pin will force the 8273 to an idle state. The 8273 will remain idle until a command is issued by the CPU. The modem interface output signals are forced high. Reset must be true for a minimum of 1Ø TCY.

CS (24)
The RD and WR inputs are enabled by the chip select input.

DB_7-$DB_Ø$ (19-12)
The Data Bus lines are bidirectional three-state lines which interface with the system Data Bus.

WR (1Ø)
The Write signal is used to control the transfer of either a command or data from CPU to the 8273.

RD (9)
The Read signal is used to control the transfer of either a data byte or a status word from the 8273 to the CPU.

TxINT (2)
The Transmitter interrupt signal indicates that the transmitter logic requires service.

RxINT (11)
The Receiver Interrupt signal indicates that the Receiver logic requires service.

TxDRQ (6)
Requests a transfer of data between memory and the 8273 for a transmit operation.

RxRDQ (8)
Requests a transfer of data between the 8273 and memory for a receive operation.

TxDACK (5)
The Transmitter DMA acknowledge signal notifies the 8273 that the TxDMA cycle has been granted.

RxDACK (7)
The Receiver DMA acknowledge signal notifies the 8273 that the RxDMA cycle has been granted.

A_1-A_0 (22-21)
These two lines are CPU Interface Register Select lines.

TxD (29)
This line transmits the serial data to the communication channel.

TxC (28)
The transmitter clock is used to synchronise the transmit data.

RxD (26)
This line receives serial data from the communication channel.

RxC (27)
The Receiver Clock is used to synchronise the receive data.

32X CLK (25)
The 32X clock is used to provide clock recovery when an asynchronous modem is used. In loop configuration the loop station can run without an accurate 1X clock by using hte 32X CLK in conjunction with the DPLL output. (This pin must be grounded when not used).

DPLL (23)
Digital Phase Locked Loop output can be tied to RxC and/or TxC when 1X clock is not available. DPLL is used with 32X CLK.

FLAG DET (1)
Flag Detect signals that a flag (01111110) has been received by an active receiver.

RTS (35)
Request to Send signals that the 8273 is ready to transmit data.

CTS (3Ø)
Clear to Send signals that the modem is ready to accept data from the 8273.

CD (31)
Carrier Detect signals that the line transmission has started and the 8273 may begin to sample data on RxD line.

PA_{2-4} (32-34)
General purpose input ports. The logic levels on these lines can be Read by the CPU through the Data Bus Buffer.

PB_{1-4} (36-39)
General purpose output ports. The CPU can write these output lines through Data Bus Buffer.

CLK (3)
A square wave TTL clock.

4.7.2.1 CPU Interface

The CPU utilises the CPU interface to specify commands and to transfer data. It consists of seven registers addressed via CS, A1, AØ, RD and WR signals and two independent data registers for receive data and transmit data. A1, AØ are generally derived from two low order bits of the address bus.

4.7.2.2 Register Description

Command
Operations are initiated by writing an appropriate command in the Command Register.

Parameter
Parameters of commands that require additional information are written to this register.

Result
Contains an immediate result describing an outcome of an executed command.

Transmit Interrupt Result
Contains the outcome of 8273 transmit operation (good/bad completion).

Receive Interrupt Result
Contains the outcome of 8273 receive operation (good/bad completion), followed by additional results which detail the reason for interrupt.

Status
The status register reflects the state of the 8273 CPU interface.

4.7.2.3 DMA Transfers

The 8273 CPU interface supports two independent data interfaces; receive data and transmit data. At high data transmission speeds the data transfer rate of the 8273 is great enough to justify the use of direct memory access (DMA) for the data transfers. When the 8273 is configured in DMA mode, the elements of the DMA interfaces are:

TxDRQ: Transmit DMA Request
Requests a transfer of data between memory and the 8273 for a transmit operation.

TxDACK: Transmit DMA Acknowledge
The TxDACK signal notifies the 8273 that a transmit DMA cycle has been granted. It is also used with WR to transfer data to the 8273 in non-DMA mode.

RxDRQ: Receive DMA Request
Requests a transfer of data between the 8273 and memory for a receive operation.

RxDACK: Receive DMA Acknowledge
The RxDACK signal notifies the 8273 that a receive DMA cycle has been granted. It is also used with RD to read data from the 8273 in non-DMA mode.

RD, WR: Read, Write
The RD and WR signals are used to specify the direction of the data transfer.

DMA transfers require the use of DMA controller such as the Intel 8237. The function of the DMA controller is to provide a sequential address and timing for the transfer, at a starting address determined by the CPU. Counting of data block lengths is performed by the 8273.

To request a DMA transfer the 8273 raises the appropriate DMA REQUEST. DMA ACKNOWLEDGE and READ enables DMA data onto the bus (independently of CHIP SELECT). DMA ACKNOWLEDGE and WRITE transfers DMA data to the 8273 (independent of CHIP SELECT).

It is also possible to configure the 8273 in the non-DMA data transfer mode. In this mode the CPU module must pass data to the 8273 in response to non-DMA data requests indicated by the status word.

4.7.2.4 Serial Data Logic

The serial data is synchronised by the user transmit (TxC) and receive (RxC) clocks. The leading edge of TxC generates new transmit data and the trailing edge of RxC is used to capture receive data.

The diagnostic features included in the Serial Data logic are programmable loop back of data and selectable clock for the receiver. In the loop-back mode, the data presented to the TxD pin is internally routed to the receive data input circuitry in place of the RxD pin, thus allowing a CPU to send a message to itself to verify operation of the 8273.

4.7.2.5 Principles of Operation

The 8273 is an intelligent peripheral controller which relieves the CPU of many of the rote tasks associated with constructing and receiving frames. As a peripheral device, it accepts commands from a CPU, executes these commands and provides an interrupt and result back to the CPU at the end of the execution. The communication with the CPU is done by activation of CS, RD, Wr pins, while the A1, AØ select the appropriate registers on the chip as described in the Hardware Description Section.

The 8273 operation is composed of the following sequence of events:

COMMAND PHASE CPU writes command and parameters into the 8273 command and parameter registers.

EXECUTION PHASE The 8273 is on its own to carry out the command.

RESULT PHASE The 8273 signals the CPU that the execution has finished. The CPU must perform a read operation of one or more of the registers.

The Command Phase

During the command phase, the software writes a command to the command register. The command bytes provide a general description of the type of operation requested. Many commands require more detailed information about the command. In such a case up to four parameters are written into the parameter register. The flowchart of the command phase indicates that a command may not be issued if the Status Register Indicates that the device is busy. Similarly if a parameter is issued when the Parameter Buffer shows full, incorrect operation will occur.

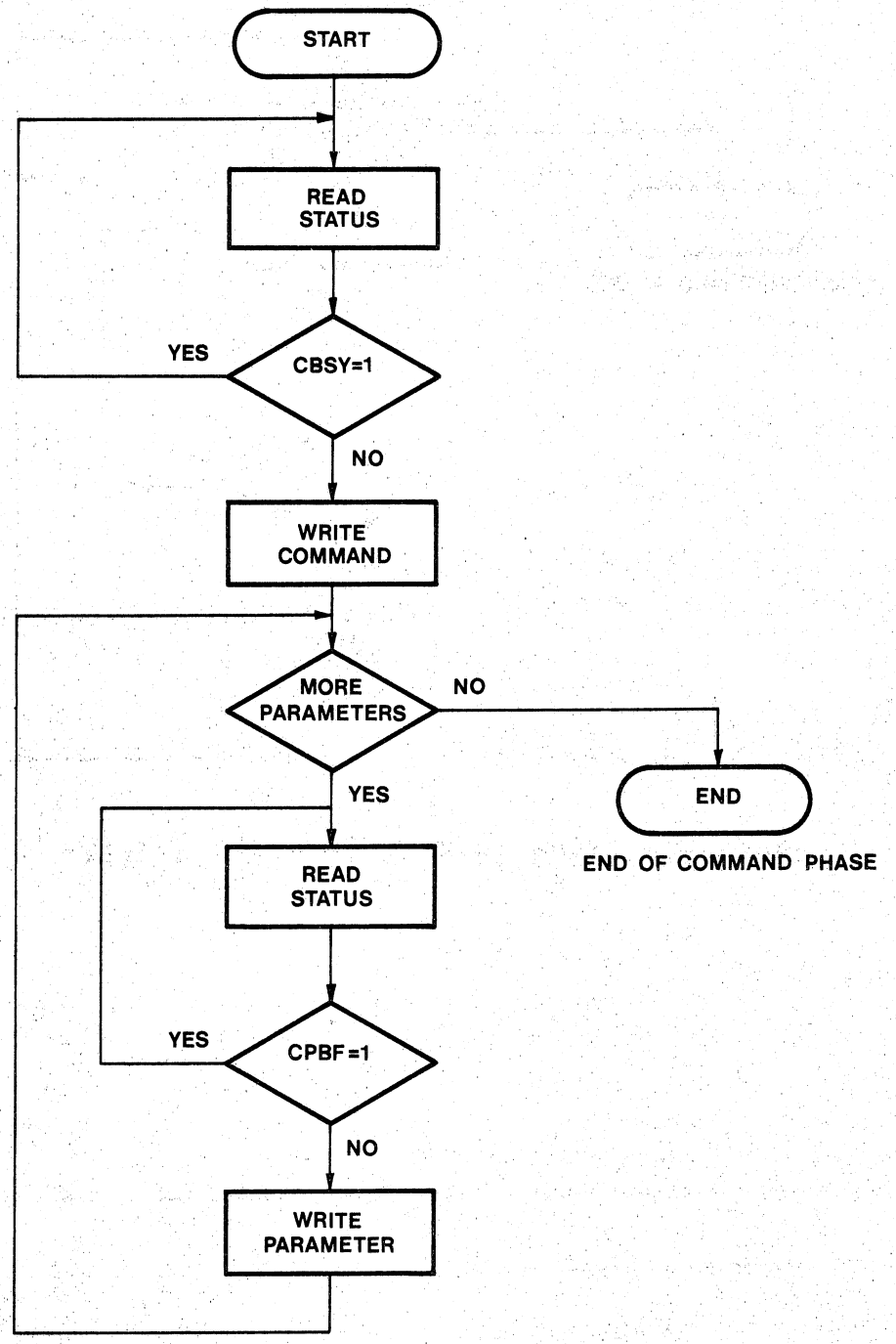


Figure 4-6 8273 Command Phase Flowchart

Status Register

The status register contains the status of the 8273 activity.

Bit 7 CBSY (Command Busy)
Indicates in-progress command, set for CPU poll when Command Register is full, reset upon command phase completion. It is improper to write a command when CBSY is set; it results in incorrect operation.

Bit 6 CBF (Command Buffer Full)
Indicates that the command register is full, it is reset when the 8273 accepts the command byte but does not imply that execution has begun.

Bit 5 CPBF (Command Parameter Buffer Full)
CPBF is set when the parameter buffer is full, and is reset by the 8273 when it accepts the parameter. The CPU may poll CPBF to determine when additional parameters may be written.

Bit 4 CRBF (Command Result Buffer Full)
Indicates that an executed command immediate result is present in the Result Register. It is set by 8273 and reset when CPU reads the result.

Bit 3 RxINT (Receiver Interrupt)
RxINT indicates that the receiver requires CPU attention. It is identical to RxINT (pin 11) and is set by the 8273 either upon good/bad completion of a specified command or by Non-DMA data transfer. It is reset only after the CPU has read the result byte or has received a data byte from the 8273 in a Non-DMA data transfer.

Bit 2 TxINT (Transmitter Interrupt)
The TxINT indicates that the transmitter requires CPU attention. It is identical to TxINT (pin 2). It is set by 8373 either upon good/bad completion of a specified command or by Non-DMA data transfer. It is reset only after the CPU has read the result byte or has transferred transmit data byte to the 8273 in a Non-DMA transfer.

Bit 1 RxIRA (Receiver Interrupt Result Available)
The RxIRA is set by the 8273 when an interrupt result byte is placed in the RxINT register. It is reset after the CPU has read the RxINT register.

Bit Ø TxIRA (Transmitter Interrupt Result Available)
The TxIRA is set by the 8273 when an interrupt result byte is placed in the TxINT register. It is reset when the CPU has read the TxINT register.

The Execution Phase

Upon accepting the last parameter, the 8273 enters into the Execution Phase. The execution phase may consist of a DMA or other activity, and may or may not require CPU intervention. The CPU intervention is eliminated in this phase if the system utilises DMA for the data transfers, otherwise, for non-DMA data transfers, the CPU is interrupted by the 8273 via TxINT and RxINT pins, for each data byte request.

The Result Phase

During the result phase, the 8273 notifies the CPU of the execution outcome of a command. This phase is initiated by:

1. The successful completion of an operation
2. An error detected during an operation.

To facilitate quick network software decisions, two types of execution results are provided:

1. An Immediate Result
2. A Non-Immediate Result

Table 4-14 Rx Interrupt Result Byte Format

D4	D3	D2	D1	DØ	Receiver INTR Result Code	Rx STAT AFTER INTR
Ø	Ø	Ø	Ø	Ø	A1 match or REC	Active
Ø	Ø	Ø	Ø	1	A2 match	Active
Ø	Ø	Ø	1	1	CRC error	Active
Ø	Ø	1	Ø	Ø	Abort detected	Active
Ø	Ø	1	Ø	1	Idle detect	Disabled
Ø	Ø	1	1	Ø	EOP detected	Disabled
Ø	Ø	1	1	1	Frame less than 32 bits	Active
Ø	1	Ø	Ø	Ø	DMA overrun detected	Disabled
Ø	1	Ø	Ø	1	Memory buffer overflow	Disabled
Ø	1	Ø	1	Ø	Carrier detect failure	Disabled
Ø	1	Ø	1	1	Receive INTR overrun	Disabled

Table 4-15 Tx Interrupt Result Byte Format

D4	D3	D2	D1	DØ	Meaning
Ø	1	1	Ø	Ø	Early transmit interrupt
Ø	1	1	Ø	1	Frame transmit complete
Ø	1	1	1	Ø	DMA underrun
Ø	1	1	1	1	Clear to send (CTS) error
1	Ø	Ø	Ø	Ø	Abort complete

Immediate result is provided by the 8273 for commands such as Read Port A and Read Port B which have information (CTS, CD, RTS, etc.) that the network software needs to make quick operational decisions.

A command which cannot provide an immediate result will generate an interrupt to signal the beginning of the Result phase. The immediate results are provided in the Result Register; all non-immediate results are available upon device interrupt, through Tx Interrupt Result Register TxI/R or Rx Interrupt Result Register RxI/R. The result may consist of a one-byte interrupt code indicating the condition for the interrupt and, if required, one or more bytes which detail the condition.

Tx and Rx Interrupt Result Registers

The Result Registers have a result code, the three high order bits D7-D5 of which are set to zero for all but the receive command. This command result contains a count that indicates the number of bits received in the last byte. If a partial byte is received, the high order bits of the last data byte are indeterminate.

All results indicated in the command summary must be read during the result phase.

4.8 UNIBUS MICROCONTROLLER INTERFACE

The UNIBUS microcontroller interface is a register array consisting of eleven 8-bit registers. Each register has an assigned microprocessor address and can be read and or loaded by the microprocessor.
Six of the eleven registers are configured with 8255-5 programmable interface elements (PIE). Each PIE has a control register, used by the microprocessor for device initialisation. Both control registers have assigned microprocessor bus addresses and thus the real UNIBUS-Microprocessor register array count is thirteen.

4.8.1 Line Control and Status Register (LCS)

The line control and status register array consists of three 8-bit read only registers; LCS1, LCS2 and LCS3. The LCS array forms the main UNIBUS microcontroller interface for the transfer of information from UNIBUS to microcontroller. The LCS interface consists of a 24 bit by 16 character SILO (S8) and a 8255-5 PIEØ (S9). The three LCS registers are the output of the 24 x 16 bit character silo and are read by the microprocessor via the three ports of the 8255-5 PIEØ.
Loading of the LCS SILO is by any UNIBUS write (word or byte) to any of the following UNIBUS registers:-

- Line Parameter Register LPR (WORD only)
- Transmit Control Register TCR (WORD or BYTE)
- Transmit Data Register TDR (WORD or BYTE)

A write to any of the above registers by the UNIBUS will result in the signal " LD LCS L" being asserted by the ROM decoder E78 (S2) and will cause a parallel load direct from the UNIBUS to the LCS silo. The UNIBUS low data byte is loaded into LCS1, UNIBUS high data byte into LCS2, and the UNIBUS A02:00 and C0 bits are loaded into LCS3. The address and C0 bits are used by the microprocessor to compute the content of LCS1 and 2.

A02 and A01 encode the UNIBUS register, A00 C0 flag word, or high/low byte transfer, that is, both LCS1 and LCS2 valid or only one, if so which one, high or low byte? LCS1 and LCS2 have the same bit definition as the corresponding UNIBUS register and are detailed in Figure 3-1.

The LCS SILO alarm (S8) monitors the LCS level. The alarm counts to 16 and sets the LCS ALARM flip flop E103 on the sixteenth count. The LCS alarm counter E104 is clocked by UNIBUS writes to the LCS silo and is cleared by microprocessor reads from the silo. LCS alarm sets a flag in the microcontrollers UNIBUS status register and disables the transmit request scanner (S7), i.e. transmit characters are not requested from the UNIBUS if the LCS alarm is set.

Table 4-15 defines LCS3 bits.

Table 4-16 LCS3 Bit Definition

7	6	5	4	3	2	1	Ø	LCS3 BIT
A02	A01	A00	C0	N/U	TLINE C	TLINE B	TLINE A	NAME
Ø	1	Ø	Ø	X	X	X	X	LPR (WORD)
1	Ø	Ø	Ø	X	X	X	X	TCR (WORD)
1	Ø	Ø	1	X	X	X	X	TCR (LOW BYTE)
1	Ø	1	1	X	X	X	X	TCR (HIGH BYTE)
1	1	Ø	Ø	X	(- SEE NOTE -)			TDR (WORD)
1	1	Ø	1	X	(- SEE NOTE -)			TDR (LOW BYTE)
1	1	1	1	X	X	X	X	TDR (HIGH BYTE)

NOTE: The TLINE bits A, B and C contain the transmit line number and are valid only when LCS1 contains a transmit character, i.e. TDR WORD or TDR LOW BYTE transfer.
These bits will be random during all other operations.
X = NOT VALID.

4.8.2 Transmit Enable Register

The transmit enable register has an assigned microcontroller bus address of C8 HEX, is write only and is implemented via port A of PIE1, (S9). This register is used by the microcontroller to control the transmit control logic, (S7). The register contains 8 bits, one for each transmit line. Setting a bit to logic one enables the transmit scanner to request characters for the respective line, clearing a bit disables transmit request for the line. Bit Ø of this register controls line Ø and bit 7 controls line 7. This register can not be used by the microcontroller to dismiss transmit request similar to the UNIBUS TCR register, it is used to suppress transmit characters in the form of XON/XOFF.

4.8.3 Receiver Buffer

The microcontroller receiver buffer register array consists of two 8-bit registers. The registers correspond to the UNIBUS RBUF register in bit definition. The receiver buffer registers are the input to the UNIBUS received data silo and are used by the microcontroller to transfer received data with line number and status through to the UNIBUS.
The receiver buffer registers have assigned microcontroller bus addresses of C4 HEX, C5 HEX and are write only registers. RBUF1 (C4 HEX) is the received data register, RBUF2 (C5 HEX) is the received data status register. Refer to Figure 3-3 for bit definitions.

4.8.4 UNIBUS Status Register (USR)

The UNIBUS status register (USR) ia an 8-bit read only register with an assigned microcontroller bus address of CA HEX. This register interfaces via port C of PIE1 (sheet 9). This register contains a number of misc. flags, their definitions are given below in Table 4-16.

Table 4-17 USR Bit Definitions

BIT	NAME	MEANING
7	LCS RDY	When set, (1) indicates that the LCS silo contains one or more UNIBUS entries and is ready to be read. When reset, (Ø) indicates that the LCS silo is empty.
6:5	NOT USED.	
4	MICRO MAINT	Microcontroller maintenance flag. When set indicates that S1 is in the TEST position. When pre-set indicates that S1 is in the RUN position.
3	MAINT 2	Maintenance Flag 2. This bit is connected to option port J2 of the M7190 module, and is reserved. This bit is always read as a one bit.
2	MAINT 1	This bit is connected to bit Ø3 of the UNIBUS CSR. When reset (Ø) indicates that bit Ø3 of the UNIBUS CSR is set. When set (1) indicates that bit Ø3 of the UNIBUS CSR is reset. This bit reads as a one bit (1) following RESET.
1	LCS ALARM	When set indicates that 16 or more entries have been moved into the LCS SILO by the UNIBUS. Once set the micro-controller must perform sucessive reads until the silo becomes empty. (LCS RDY = Ø). This bit is read as Ø following a RESET.
Ø	RBUF READY	Receiver Buffer Ready. When set indicates that the receiver silo can accept another receiver character for transfer to the UNIBUS. When RESET indicates that the receiver silo is not ready. Cleared by RESET.

4.8.5 Switch Register

The microcontroller switch register reads the state of eight switches located in a DIL switch pack, location E59 (sheet 9). The switch register has an assigned microcontroller bus address of C9 HEX and is read only. The register interfaces to the bus via Port B of the 8255A-5 E57.
A switch ON (closed) corresponds to a logic zero (read as Ø) and a switch OFF (open) corresponds to a logic ONE (read as 1). Table 4-17 below defines each switch.

Table 4-18 Switch Register Definition

BIT	NAME	MEANING
7	ENA LOOP TEST	When open (logic ONE) enables selected OFF line microdiagnostic sub test to loop continuously. When closed (logic zero) enables OFF line microdiagnostic to run through all sub test, normal operation. The OFF line microdiagnostic sub test is selected by bits 6:4 of this switch register.
6:4	Test No.	Used to select OFF line microdiagnostic sub test number. Following is a list of valid switch settings with corresponding sub test number. S6 S5 S4 TEST NO. Ø Ø 1 ROM test Ø 1 Ø RAM test Ø 1 1 Clock Test 1 Ø Ø X.25 logic 1 Ø 1 X.25 data 1 1 Ø DMA LOGIC 1 1 1 X.25 ext. data 1 = Switch OFF (OPEN) Ø = Switch ON (CLOSED)
3	Clock Source	Selects source of baud rate timing for composite port communication controller. When closed (ON) selects external clock. When open (OFF) selects internal clock.
2:Ø	Baud Rate	Selects composite port baud rate. S2 S1 SØ Baud Rate Ø Ø Ø 1200 Ø Ø 1 1800 Ø 1 Ø 2400 Ø 1 1 3600 1 Ø Ø 4800 1 Ø 1 7200 1 1 Ø 9600 1 1 1 19200

4.8.6 LED Display Register

The microcontroller LED display register is a write only register and has a microcontroller bus address of CE HEX. This register is used by the microcontroller to display DZS11-EA operational and maintenance status.

Table 4-19 LED Display Format

<table>
<tr><th>MODE</th><th>LED No.</th><th>M7190 Meaning</th></tr>
<tr><td>RUN</td><td>8:7</td><td>Run Mode Indicator.
A rotating bit pattern indicates that the DZS11-EA microcontroller is in the run mode. (Normal Operation).</td></tr>
<tr><td>RUN</td><td>6:4</td><td>DZS11-EA. Transmit Error Count.
The binary value of LEDs 6, 5 and 4 indicate the number of transmit errors detected since initialisation. The maximum error count is 7, after which the counter resets to zero. LED 4 is the least significant digit.</td></tr>
<tr><td>RUN</td><td>3:1</td><td>DZS11-EA Receive Errors Count.
The binary value of LEDs, 3, 2 and 1 indicate the number of receive errors detected since initialisation. The maximun error count is 7, after which the counter resets to zero. LED 1 is the least significant digit.</td></tr>
<tr><td>TEST</td><td>8:7</td><td>Microdiagnostic Type Indicator.
A steady state pattern indicates that the DZS11-EA microcontroller is in the TEST mode. The following table lists the three legal states of LEDs 8 and 7 when in the TEST mode.
<table>
<tr><th>LED 8</th><th>LED 7</th><th>TEST Type</th></tr>
<tr><td>OFF</td><td>ON</td><td>GO/NO GO Test Running</td></tr>
<tr><td>ON</td><td>OFF</td><td>OFF Line Test Running</td></tr>
<tr><td>ON</td><td>ON</td><td>UNIBUS Test Running</td></tr>
</table>
</td></tr>
</table>

Table 4-19 LED Display Format cont:

<table>
<tr><th>MODE</th><th>LED No.</th><th>M7190 Meaning</th></tr>
<tr><td>TEST</td><td>6:4</td><td>Test Number Indicator
This field is used by the OFF LINE microdiagnostic to indicate the subtest being executed.
The following table lists the valid subtest numbers for the OFF LINE Microdiagnostic.

<table>
<tr><th>LED 6</th><th>LED 5</th><th>LED 4</th><th>TEST</th></tr>
<tr><td>OFF</td><td>OFF</td><td>ON</td><td>PROM test</td></tr>
<tr><td>OFF</td><td>ON</td><td>OFF</td><td>RAM test</td></tr>
<tr><td>OFF</td><td>ON</td><td>ON</td><td>CLOCK test</td></tr>
<tr><td>ON</td><td>OFF</td><td>OFF</td><td>X.25 logic</td></tr>
<tr><td>ON</td><td>OFF</td><td>ON</td><td>X.25 Int. DATA</td></tr>
<tr><td>ON</td><td>ON</td><td>OFF</td><td>DMA LOGIC</td></tr>
<tr><td>ON</td><td>ON</td><td>ON</td><td>X.25 Ext. DATA</td></tr>
</table>
</td></tr>
<tr><td>TEST</td><td>3:1</td><td>Error Number.
This field indicates error status. This field is used by both the GO/NO GO and OFF LINE microdiagnotsics.
Refer to Section C-5 for Error types and meaning.</td></tr>
</table>

4.8.7 Modem Status Register (MSR)

The modem status register array consists of two 8-bit 74LS374 latches (sheet 9). They are write only and have assigned microcontroller bus address of CC HEX and CD HEX. The ring register is CC HEX and the carrier register is CD HEX.
They do not have a direct hardware reset, and so are cleared by the microprocessor at device initialisation time. The carrier and ring registers have the same bit definition as the UNIBUS MSR registers.

CHAPTER 5

MAINTENANCE

5.1 SCOPE

This chapter provides information for servicing the DZS11-EA. It includes the maintenance philosophy, maintenance functions, preventive maintenance, and corrective maintenance. The section on corrective maintenance contains brief descriptions of the diagnostics associated with the DZS11-EA.

5.2 MAINTENANCE PHILOSOPHY

The field replaceable unit (FRU) for the DZS11-EA is either a faulty module or cable. Training of field service personnel is directed to functional and application trouble shooting, using diagnostics, for fault isolation to the (FRU). Spare parts for module repairs are not stocked in the field. Typical applications of the DZS11-EA do not permit lengthy troubleshooting sessions and component troubleshooting/repair requires, at least, a 16-channel logic analyser.

CAUTION

When inserting or removing the M7190 DZS11-EA module, be sure not to dislodge the priority plug or other socketed devices.

Ensure that all socketed devices are seated firmly and in the correct sockets; otherwise erratic operation of the DZS11-EA may result.

5.3 PREVENTIVE MAINTENANCE

There is no specific DZS11-EA preventive maintenance (PM) schedule. A general check of voltages and connections should be done when system PM is performed. After handling the DZS11-EA module or cable, a complete checkout of the device, by running all diagnostics is necessary. Special care must be exercised for the following reason:-

- o EPROM chips installed in sockets are easily dislodged during removal and replacement of the DZS11-EA module or adjacent modules. The EPROM chips may accidently come in contact with the etch side of the adjacent module.

5.4 TEST EQUIPMENT REQUIRED

Maintenance procedures for the DZS11-EA requires the test equipment and diagnostic programs listed in Table 5-1, in addition to standard hand tools, cleaners, test cables and probes.

Table 5-1 Test Equipment Required

EQUIPMENT	MANUFACTURER	DESIGNATION
Multimeter	Triplett or Simpson	Model 630-NA0260
Oscilloscope	Tektronix	Type 454 or equivalent
Module Extender	DIGITAL	W904 Hex
Test Connectors	DIGITAL	H325 and Hxxx
Diagnostic	DIGITAL	MAINDEC-11-DZDZA

5.5 ON BOARD MAINTENANCE FEATURES

On board maintenance features in the form of resident microdiagnostics are available to the user. This microdiagnostic is invoked by means of a maintenance switch. Diagnostic status and error codes are displayed by means of eight LED devices mounted at the top edge of the module. Refer to Appendix C for description and operating procedures of microdiagnostic.

5.6 CORRECTIVE MAINTENANCE ON A PDP-11 PROCESSOR

Since the FRU is either a module or cable, all corrective diagnosis should be directed towards isolating the failing FRU. Two levels of diagnostic are designed to aid in the isolation process.
The on board microdiagnostic is intended to diagnose the on board microprocessor and the composite link.
The UNIBUS diagnostic is intended to diagnose the DZS11-EA UNIBUS-Microcontroller interface.

When isolating the fault, the on board microdiagnostic should be run first followed by the UNIBUS diagnostic DZDZA. Further information including operating procedures for the microdiagnostic can be found in Appendix C of this document.

5.6.1 Loading PDP11 Diagnostic DZDZA

Follow the standard loading procedures as detailed in the MAINDEC-11-DZDZA-E-D diagnostic description.

5.6.2 Starting PDP11 Diagnostic DZDZA

The diagnostic should be started at address 200 with switch bits SW4 and SW0 set. On the first start of the diagnostic the following questions are asked and must be answered.

"1ST CSR ADDRESS (160000:163700):"
You must type in the first DZS11-EA CSR in the system you wish testing to begin at.

"1ST VECTOR ADDRESS (300:770):"
You must type in the vector of the first DZS11-EA in the system under test. Range 300:370.

"BR LEVEL (4:6)"
Type in the priority level of the DZS11-EA that the above information has been given about. Range 4 or 5 or 6.

"TYPE "A" FOR EIA MODULE OR "B" FOR 20 MA (A:B):"
You must type "A" for the DZS11-EA.

"MAINTENANCE MODE
[EXTERNAL <H325> - EIA ONLY (E)]
[INTERNAL <DZCSR03=1> (I)]
[STAGGERED <H3271> - EIA ONLY (5)]
[STAGGERED <H3190> - 20MA ONLY (5)]:"

You must type "I" for the DZS11-EA.

"# OF DZ11'S <IN OCTAL> (1:20):"
Type total number of DZS11-EA to be tested in the system. Range is 1 thru 20 in octal. The diagnostic will then print a MAP of DZS11-EA Status followed by the prompt.

ENTER DELAY PARAMETER:

You must now type in a delay parameter of at least 500. This delay parameter should be increased when testing on fast CPUs.

The diagnostic will then print the message

"RUNNING"

When the diagnostic has completed a pass the following is an example of the print out to be expected.

"END PASS DZDZA-E CSR:160010 VEC:300 PASSES 000001 ERRORS: 000000"

This message is printed at the completion of each pass.

Refer to DZDZA-E description for error messages.

5.7 CORRECTIVE MAINTENANCE ON A VAX PROCESSOR

To be supplied.

APPENDIX A

DZS11-EA SHIPPING LIST

A.1 GENERAL

The following is a list of equipment and documentation furnished with each DZS11-EA.

Table A-1 DZS11-EA Shipping List

ITEM	PART NO:	DESCRIPTION
1	M7190	8 channel statistical mux control board
2	BC05C-25	Cable, modem
3	H325	Test connector, (cable)
4	H883	Test connector, (M7190)
5	YA-C06LB-00	DZS11-EA PRINT SET
6	YA-C065C-00	DZS11-EA USERS MANUAL

APPENDIX B

FLOATING DEVICE ADDRESSES AND VECTORS

B.1 FLOATING DEVICE ADDRESSES

UNIBUS addresses starting at 760010 and continuing through 763776 are designated as floating device addresses (see Figure B-1). These are used as register addresses for communications (and other) devices interfacing with the PDP-11 and VAX-11/780.

NOTE
Some devices are not supported by VAX-11/780,however, the same scheme applies; that is, gaps are provided as appropriate. The convention for assigning these addresses is as follows:

Floating CSR Address Devices

Rank	Option	Decimal Size	Octal Modulus
1	DJ11	4	10
2	DH11	8	20
3	DQ11	4	10
4	DU11	4	10
5	DUP11	4	10
6	LK11A	4	10
7	DMC11/DMR11	4	10
8	DZ11*and DZS11-EA	4	10
9	KMC11	4	10
10	LPP11	4	10
11	VMV21	4	10
12	VMV31	8	20
13	DWR70	4	10
14	RL11 and RLV11	4	10 (extra only)

A gap of 10_8 must be left between the last address of one device type and the first address of the next device type. The first address of the next device type must start on a modules 10_8 boundary. The gap of 10_8 must also be left for devices that are not installed but are skipped over in the priority ranking list. Multiple devices of the same type must be assigned contiguous addresses. Reassignment of device types already in the system may be required to make room for additional ones.

*DZ11E and DZ11F are dual DZ11s and are treated by the algorithm as two DZ11s.

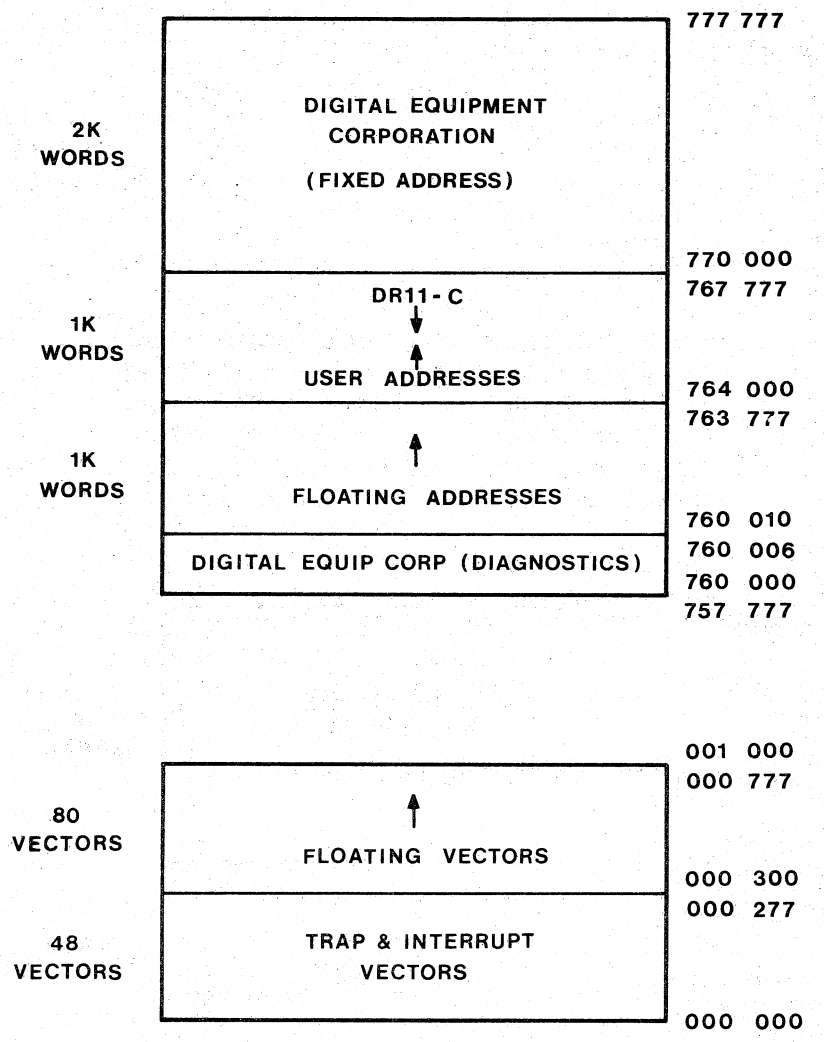


Figure B-1 UNIBUS Address Map

B.2 FLOATING VECTOR ADDRESSES

Vector addresses, starting at 300 and proceeding upward to 777, are designated as floating vectors. These are used for communications (and other) devices that interface with the PDP-11 and VAX 11/780.

NOTE

Some devices are not supported by VAX-11/780, however, the same scheme applies. Vector size is determined by the device type.

There are no gaps in floating vectors unless required by physical hardware restrictions (in data communications devices, the receive vector must be on a zero boundary and the transmit vector must be on a 4_8 boundary).

Multiple devices of the same type would be assigned vectors sequentially. The following chart shows the assignment sequence.

Floating Interrupt Vector Devices

Rank	Option	Decimal Size	Octal Modulus
1	DC11	4	10
2	KL11 (extra)	4	10*
2	DL11-A (extra)	4	10*
2	DL11-B (extra)	4	10
3	DP11	4	10
4	DM11-A	4	10
5	DN11	2	4
6	DM11-BB	2	4
6	DH11 modem control	2	4
7	DR11-A	4	10*
8	DR11-C	4	10*
9	PA611 (reader)	2	10*
10	PA611 (punch)	2	10*
11	LPD11	4	10
12	DT11	4	10*
13	DX11	4	10*
14	DL11-C	4	10*
14	DL11-D	4	10*
14	DL11-E	4	10*
15	DJ11	4	10*
16	DH11	4	10**
17	GT40	8	10
18	LPS11	12	30*
19	DQ11	4	10**
20	KW11-W	4	10
21	DU11	4	10*
22	DUP11	4	10*
23	DV11	4	10*
24	DV modem control	2	4
25	LK11-A	4	10
26	DWUN	4	10
27	DMC11/DMR11	4	10*
28	DZ11/DZS11-EA	4	10*
29	KMC11	4	10
30	LPP11	4	10
31	VMV21	4	10
32	VMV31	4	10
33	VTV01	***	***
34	DWR70	4	10*
35	RL11/RLV11	2	4
36	RX02	2	4
37	TS11	2	4(after the first)
38	LPA11-K	4	10
39	IP11/IP300	2	4

* The vector for the device of this type must always be on a 10_8 boundary.

** These devices can have either a M7820 or M7821 interrupt control module. However, it should always be on a 10_8 boundary.

*** To be determined.

B.3 EXAMPLES OF DEVICE AND VECTOR ADDRESS ASSIGNMENT

Example 1

The first device requiring address assignment in this example is a DH11 (Number two in the device address assignment sequence; Number 16 in the vector address assignment sequence).

The only devices used are:

2 DH11s
2 DQ11s
1 DUP11
1 DZS11-EA

Device (Option)	Device Address	Vector Address	Comment
	760010		Gap left for DJ11 (one on device address assignment sequence) which is not used
DH11	760020	300	First DH11
DH11	760040	310	Second DH11
	760060		Gap between the last DH11 used and the next device
DQ11	760070	320	First DQ11
DQ11	760100	330	Second DQ11
	760110		Gap between the last DQ11 used and the next device
	760120		Gap left for DU11s not used
DUP11	760130	340	Only one DUP11
	760140		Gap left between DUP11 and next device
	760150		Gap left for LK11-As not used
DZS11-EA	760160	350	Only one DZS11-EA
	760170		Gap left after the last device (in this case, the DZS11-EA) to indicate that none follow.

Example 2

The only devices used in this example are:

1 DJ11
1 DH11
2 DQ11s
2 DUP11s
2 DZS11-EAs

Device (Option)	Device Address	Vector Address	Comment
DJ11	760010	300	Only one DJ11
	760020		Gap left between DJ11 anf the next device
	760030		Gap - The next device, DH11, must start on an addresss boundary that is a multiple of 20
DH11	760040	310	Only one DH11
	760060		Gap left between DH11 and next device
DQ11	760070	320	First DQ11
DQ11	760100	330	Second DQ11
	760110		Gap left between DQ11 and next device
	760120		Gap left for DU11s not used
DUP11	760130	340	First DUP11
DUP11	760140	350	Second DUP11
	760150		Gap left between the last DUP11 and next device
	760160		Gap left for LK11-As not used
DZS11-EA	760170	360	First DZS11-EA
DZS11-EA	760200	370	Second DZS11-EA
	760210		Gap left after the last device (in this case the DZS11-EA) to indicate that none follow.

Example 3

Only one of each of the following devices are used in this example:

DC11	DQ11
DJ11	DUP11
DH11	DZS11-EA
GT40	DZS11-EA

Device (Option)	Device Address	Vector Address	Comment
DC11		300	DC11 has a fixed device address
DJ11	760010	310	Only one DJ11
	760020		Gap left between DJ11 and the next device
	760030		Gap- The next device, DH11, must start on an address boundary that is a multiple of 20
DH11	760040	320	Only one DH11
	760060		Gap left between DH11 and next device
GT40		330	GT40 has a fixed device address
DQ11	760070	340	Only one DQ11
	760100		Gap left between DQ11 and the next device
	760110		Gap left for DU11s not used
DUP11	760120	350	Only one DUP11
	760130		Gap left between DUP11 and the next device
	760140		Gap left for LK11-As not used
DZS11-EA	760150	360	Only one DZS11-EA
DZS11-EA	760160		Gap left after the last device (DZS11-EA) to indicate that none follow.

APPENDIX C

DZS11-EA MICRODIAGNOSTIC

C.1 INTRODUCTION

This section describes the on board microdiagnostic features of the DZS11-EA. There are three microdiagnostics; GO/NO GO test, OFF LINE test, and UNIBUS test, all can be used as preventive and corrective maintenance tools.

C.1.1 GO/NO GO Test

This test is initiated following device initialisation. Its function is to perform a confidence test on the microcontroller hardware prior to execution of control code. If errors are detected by this test, the following occurs:-

- Error type is displayed by maintenance LEDs.
- Microcontroller, transmit control logic is disabled
- Test halts at common halt location.

C.1.2 Off Line Microdiagnostic

The Off Line microdiagnostic is a preventive and corrective maintenance tool for the DZS11-EA microcontroller hardware. The microdiagnostic is resident within the microcontroller PROMS and is initiated by a maintenance switch mounted at the top edge of the M7190 module. Normal operation of the OFF LINE microdiagnostic can be enabled without having to remove the M7190 module from its slot, however if sub tests are to be run in continuous mode, then the module must be removed to enable access to the maintenance control switch (E59). Ref. C.3.4.
One of the OFF LINE microdiagnostic sub tests is an external X.25 communication test. This test can be used to test the composite port, in incremental steps or in whole from the M7190 module to the remote VT1XX-EA/EB. This is achieved by using a pre set X.25 maintenance format for the test data. This enables an operational VT1XX-EA or VT1XX-EB, at the remote end of the composite port to receive and loop back without manual intervention. The composite port can therefore be tested in whole from DZS11-EA to VT1XX-EA/EB; or in incremental steps by looping the TX back on the RX at modem or cable test points.
The OFF LINE microdiagnostic and the main control code are mutually exclusive, that is, only one can operate at any one time. If the OFF LINE microdiagnostic is enabled, the DZS11-EA stat mux network will stop.

C.1.3 UNIBUS Microdiagnostic

The DZS11-EA uses a PDP resident diagnostic for preventive and corrective maintenance of the DZS11-EA UNIBUS interface. The UNIBUS microdiagnostic as described in this section is not the PDP resident diagnostic referred to above, it is a microprogram specifically called by the microcontroller for the control of the microcontroller's UNIBUS interface during execution of the PDP resident UNIBUS diagnostic.
The UNIBUS microdiagnostic is initiated by insertion of a test connector (H883) into J1 of the M7190 module, the RUN/TEST switch must be in the RUN position.

C.2 REQUIREMENTS

C.2.1 Equipment

Two test connects are required to run the DZS11-EA OFF LINE microdiagnostic (H325 and H883). The H883 test connector loops TX data to RX data at J1 OF THE M7190. The H325 test connector tests the BC05C-25 cable in a similar manner. The H883 test connector is also required to run to UNIBUS microdiagnostic.

C.2.2 Storage

All microdiagnostics are resident within the M7190 microcontroller PROM space.

C.2.3 Microdiagnostic Status Display

Eight light emitting diodes (LEDs) are used to display DZS11-EA status. The eight LEDs are mounted along the top edge of the M7190 module as shown in Figure 2.1.

There are two types of status information displayed, RUN and TEST.

In the RUN mode the LEDs, display status relating to the DZS11-EA stat mux network in the form of composite port Receive and Transmit Errors.

In the TEST mode the LEDs, display microdiagnostic status e.g. Test number, sub test number and error type if any. Table C.1 (LED Display Format) defines the various LED patterns for both the RUN and TEST modes.

Table C-1 LED Display Format

<table>
<tr><th>MODE</th><th>LED No.</th><th>M7190 Meaning</th></tr>
<tr><td>RUN</td><td>8:7</td><td>Run Mode Indicator.
A rotating bit pattern indicates that the DZS11-EA microcontroller is in the run mode. (Normal Operation).</td></tr>
<tr><td>RUN</td><td>6:4</td><td>DZS11-EA. Transmit Error Count.
The binary value of LEDs 6, 5 and 4 indicate the number of transmit errors detected since initialisation. The maximum error count is 7, after which the counter resets to zero. LED 4 is the least significant digit.</td></tr>
<tr><td>RUN</td><td>3:1</td><td>DZS11-EA Receive Errors Count.
The binary value of LEDs, 3, 2 and 1 indicate the number of receive errors detected since initialisation. The maximum error count is 7, after which the counter resets to zero. LED 1 is the least significant digit.</td></tr>
<tr><td>TEST</td><td>8:7</td><td>Microdiagnostic Type Indicator.
A steady state pattern indicates that the DZS11-EA microcontroller is in the TEST mode. The following table lists the three legal states of LEDs 8 and 7 when in the TEST mode.
<table>
<tr><th>LED 8</th><th>LED 7</th><th>TEST Type</th></tr>
<tr><td>OFF</td><td>ON</td><td>GO/NO GO Test Running</td></tr>
<tr><td>ON</td><td>OFF</td><td>OFF Line Test Running</td></tr>
<tr><td>ON</td><td>ON</td><td>UNIBUS Test Running</td></tr>
</table>
</td></tr>
</table>

Table C-1 LED Display Format cont:

<table>
<tr><th>MODE</th><th>LED No.</th><th>M7190 Meaning</th></tr>
<tr><td>TEST</td><td>6:4</td><td>Test Number Indicator
This field is used by the OFF LINE microdiagnostic to indicate the subtest being executed.
The following table lists the valid subtest numbers for the OFF LINE Microdiagnostic.

<table>
<tr><th>LED 6</th><th>LED 5</th><th>LED 4</th><th>TEST</th></tr>
<tr><td>OFF</td><td>OFF</td><td>ON</td><td>PROM test</td></tr>
<tr><td>OFF</td><td>ON</td><td>OFF</td><td>RAM test</td></tr>
<tr><td>OFF</td><td>ON</td><td>ON</td><td>CLOCK test</td></tr>
<tr><td>ON</td><td>OFF</td><td>OFF</td><td>X.25 logic</td></tr>
<tr><td>ON</td><td>OFF</td><td>ON</td><td>X.25 Int. data</td></tr>
<tr><td>ON</td><td>ON</td><td>OFF</td><td>DMA logic</td></tr>
<tr><td>ON</td><td>ON</td><td>ON</td><td>X.25 Ext. DATA</td></tr>
</table>
</td></tr>
<tr><td>TEST</td><td>3:1</td><td>Error Number.
This field indicates error status. This field is used by both the GO/NO GO and OFF LINE microdiagnotsics.
Refer to Section C-5 for Error types and meaning.</td></tr>
</table>

C.3 STARTING PROCEDURE

C.3.1 Starting GO/NO GO Test

The GO/NO GO test is initiated each time the DZS11-EA microcontroller is initialised, (BUS initialisation or device initialisation).
Note, if the UNIBUS microdiagnostic is selected, the GO/NO GO test is not run. In this case, control is passed to the UNIBUS microdiagnostic following device INITIALISATION.

C.3.2 Starting OFF LINE Microdiagnostic

The OFF LINE microdiagnostic is initiated by the RUN/TEST switch (S1) (see Figure 2-1) being set to the TEST position. Should the DZS11-EA microcontroller already be in the UNIBUS microdiagnostic mode, the RUN/TEST switch overrides and forces the microcontroller into OFF LINE test. The OFF LINE microdiagnostic requires a turn around plug installed or a working VT1XX-EA/EB connected to the remote end of the communication network, for sub test 7 to pass.

C.3.3 Starting UNIBUS Microdiagnostic

Insert the H883 test connector into the J1 of the M7190 insuring that SIDE 1 of the test connector is visible from the component side of the DZS11-EA (M7190) control module.
Set the RUN/TEST switch into the RUN position and initialise the DZS11-EA either by BUS initialisation or device clear, (bit 04 of CSR).

C.3.4 DZS11-EA Control Switch Settings

Eight control switches are located in a DIL switch pack located at position E59 (refer Figure 2-1). They enable both composite communication port parameters and maintenance control features to be set.
The maintenance control switches are E59-1 through E59-4. Table C-2 lists the control function of these switches.

Table C-2 Maintenance Switch Settings (E59)

SW1	SW2	SW3	SW4	Meaning
OFF	X	X	X	Disable test select switches 2:4
ON	X	X	X	Enable test select switches 2:4. When set will force the OFF line microdiagnostic to continuously execute the test selected by switches 2:4. (See LED display Table C-1 for test number).

C.4 OPERATING PROCEDURES

C.4.1 GO/NO GO Test

The GO/NO GO test starts automatically following initialisation. Assuming an error free pass, control is transferred to the DZS11-EA control code on completion.
If errors are detected by the GO/NO GO microdiagnostic the microcontroller halts with error displayed. See Section C.5.1 for errors.

C.4.2. OFF LINE Diagnostic

The OFF LINE microdiagnostic is initiated by setting the RUN/TEST switch (Figure 2-1) into the TEST position.
Test 7 of the OFF LINE microdiagnostic requires an external loop back connector. Two test connectors are supplied with the DZS11-EA option, H883 and H325.
The H883 loops transmit to receive at J1 of the M719Ø module enabling the DZS11-EA to be tested without external cable.
The H325 connects transmit to receive at the DB25-P end of the BCØ5C-25 cable, enabling the module and cable to be tested.
If the OFF LINE microdiagnostic detects an error it sets the appropriate LED error indicator and loops on the failing test. The one exception is test 7, the external X25 communication test. In this instance the microdiagnostic sets the LEDs to indicate the test number (Test 7) and error type and continues to test until 1Ø successful frames have been transmitted and received.

C.4.3 UNIBUS Microdiagnostic

To run the UNIBUS PDP or VAX resident diagnostic the UNIBUS microdiagnostic must first be invoked.

Set the RUN/TEST switch into the RUN position.
Insert the H883 test connector into J1 of the M719Ø module.
Load and run the PDP resident diagnostic. (Refer Section 5.6 and 5.7).

C.5 MICRODIAGNOSTIC ERRORS

C.5.1 GO/NO GO Errors

On detection of errors while running the GO/NO GO test, the microcontroller displays the error number in LED Ø:4, disables the transmit control logic by writing zero to the transmit enable register and jumps to a common halt location. Table C-3 lists all possible error types.

Table C-3 GO/NO GO Error Types

8	7	6	5	4	3	2	1	Error Type
Ø	1	Ø	Ø	Ø	Ø	Ø	1	ROM 1 faulty
Ø	1	Ø	Ø	Ø	Ø	1	Ø	ROM 2 faulty
Ø	1	Ø	Ø	Ø	Ø	1	1	ROM 3 faulty
Ø	1	Ø	Ø	Ø	1	Ø	Ø	ROM 4 faulty
Ø	1	Ø	Ø	Ø	1	Ø	1	ROM 5 faulty
Ø	1	Ø	Ø	Ø	1	1	Ø	RAM ØK-1K faulty
Ø	1	Ø	Ø	Ø	1	1	1	RAM 1K-2K faulty
Ø	1	Ø	Ø	1	Ø	Ø	Ø	RAM 2K-3K faulty
Ø	1	Ø	Ø	1	Ø	Ø	1	RAM 3K-4K faulty
Ø	1	Ø	Ø	1	Ø	1	Ø	RAM 4K-5K faulty
Ø	1	Ø	Ø	1	Ø	1	1	RAM 5K-6K faulty
Ø	1	Ø	Ø	1	1	Ø	Ø	RAM 6K-7K faulty
Ø	1	Ø	Ø	1	1	Ø	1	RAM 7K-8K faulty

Note.
1 = LED ON
Ø = LED OFF

C.5.2 OFF LINE Microdiagnostic Errors

Table C-4 lists the possible error types detected by the OFF LINE microdiagnostic.

Table C-4 OFF LINE Error Types

8	7	6	5	4	3	2	1	Error Type
1	Ø	Ø	Ø	1	Ø	Ø	Ø	ROM test running
1	Ø	Ø	Ø	1	Ø	Ø	1	ROM 1 faulty
1	Ø	Ø	Ø	1	Ø	1	Ø	ROM 2 faulty
1	Ø	Ø	Ø	1	Ø	1	1	ROM 3 faulty
1	Ø	Ø	Ø	1	1	Ø	Ø	ROM 4 faulty
1	Ø	Ø	1	Ø	Ø	Ø	Ø	RAM test running
1	Ø	Ø	1	Ø	Ø	Ø	1	High RAM faulty (5ØØØH to 5FFFH)
1	Ø	Ø	1	Ø	Ø	1	Ø	Low RAM faulty (4ØØØH to 4FFFH)
1	Ø	Ø	1	1	Ø	Ø	Ø	Clock test running
1	Ø	Ø	1	1	Ø	Ø	1	Clock slow
1	Ø	Ø	1	1	Ø	1	Ø	Clock fast
1	Ø	1	Ø	Ø	Ø	Ø	Ø	X.25 logic test running
1	Ø	1	Ø	Ø	Ø	Ø	1	8237 error
1	Ø	1	Ø	Ø	Ø	1	Ø	8273 error
1	Ø	1	Ø	1	Ø	Ø	Ø	X.25 int. data test running
1	Ø	1	Ø	1	Ø	Ø	1	RX error
1	Ø	1	Ø	1	Ø	1	Ø	TX error
1	Ø	1	Ø	1	Ø	1	1	Recd.data not matching transmitted data.
1	Ø	1	Ø	1	1	Ø	1	TX time-out
1	Ø	1	Ø	1	1	1	Ø	RX time-out
1	Ø	1	1	Ø	Ø	Ø	Ø	DMA logic test running
1	Ø	1	1	Ø	Ø	Ø	1	DMA error
1	Ø	1	1	Ø	Ø	1	Ø	Data error high memory
1	Ø	1	1	Ø	Ø	1	1	Data error low memory
1	Ø	1	1	1	Ø	Ø	Ø	X.25 ext. data test running
1	Ø	1	1	1	Ø	Ø	1	RX error
1	Ø	1	1	1	Ø	1	Ø	TX error
1	Ø	1	1	1	Ø	1	1	Recd.date not matching transmitted data.
1	Ø	1	Ø	1	1	Ø	1	TX time-out
1	Ø	1	Ø	1	1	1	Ø	RX time-out

C.6 MISCELLANEOUS

C.6.1 Execution Times

The following is a list of error free execution times for the microdiagnostic.

Test	Time
GO/NO GO	Ø.ØØ sec.
OFF LINE TEST 12ØØ baud	X.XX sec.
OFF LINE TEST 24ØØ baud	X.XX sec.
OFF LINE TEST 48ØØ baud	X.XX sec.
OFF LINE TEST 96ØØ baud	X.XX sec.
OFF LINE TEST 192ØØ baud	X.XX sec.

C.7 TEST DESCRIPTION

C.7.1 General

Two hardware flags are used by the microcode following device initialisation to control the desired start-up sequence. Standard sequence is to run the GO/NO GO test prior to operational code. The two hardware flags used are; the RUN/TEST maintenance switch and the H883 flag. The RUN/TEST switch is self explanatory, it selects either operational code or the OFF line microdiagnostic. The H883 flag is asserted when the H883 test connector is installed in J1 of the M7190 module. This flag is used to select the UNIBUS microdiagnostic. The RUN/TEST flag overrides the H883 flag, i.e. if the UNIBUS microdiagnostic is selected and the RUN/TEST switch is moved to the TEST position, then the OFF LINE microdiagnostic will be selected. This feature enables the H883 test connector to be used with off line microdiagnostics as a data loop back connector.
Figure C-1 is a flow diagram showing the diagnostic flag check sequence.

Figure C-1 Microdiagnostic Flag Check Sequence
(Sheet 1 of 2)

Figure C-1 Microdiagnostic Flag Check Sequence
(Sheet 2 of 2)

C.7.2 GO/NO GO Test

This test is made up of a RAM test and a ROM test.

RAM Test: This writes and reads RAM, verifying the values. Errors are shown in the LED's and a halt is executed.

1. Set LED's
2. Write location
3. Read location, HALT on error
4. If not end at 1K block GOTO 2
5 If not end at RAM GOTO 1
6 END

ROM Test: This recalculates the checksum for all ROM's. Any errors are shown in the LED's.

1. Set LED's
2. Read location
3. Add to checksum
4. If not end at 2K block GOTO 2
5. If checksum error HALT
6. If not end of ROM GOTO 1
7. EXIT

C.7.3 OFF LINE Diagnostic

C.7.3.1 Test 1

ROM Test: This test recalculates the checksum for each 2K of ROM. The 2K block number is displayed prior to the block being tested. On checksum error, the test halts with the block number displayed on the LEDs.

1. Set LED's (1ØØØ1ØØ)
2. Recalculate checksum
3. If error in checksum set LED's and HALT
4. If last block RETURN
5. Increment block number
6. GOTO 1

C.7.3.2 Test 2

RAM Test: This test verifies that the RAM is able to be read and written.

1. Display test number (1001000)
2. Write 1K RAM
3. READ and compare 1K RAM, on error GOTO 20
4. If all RAM written GOTO 6
5. GOTO 2
6. READ and compare all RAM, on error GOTO 20
7. Repeat (2) to (6) using complement of data
8. RETURN

20. Error, set LED's
21. Continue writing and reading error location

C.7.3.3 Test 3

Clock Test: This test verifies the clock interrupts at the correct frequency.

1. Display test number
2. Initialise clock
3. Wait
4. If the number of interrupts are within $\pm$ 2 counts GOTO 6
5. Set LED's to error
6. If no errors RETURN
7. GOTO 2

C.7.3.4 Test 4

X.25 Initialisation Test: This test initialises the X.25 controller and verifies the status is correct.

1. Set LED display (1010000)
2. INIT 8273
3. Read status and compare
4. If error set LED's (10100010)
5. INIT 8237
6. Read status and compare
7. If error set LED's (10100001)
8. Repeat 2-7 10 times
9. If any errors repeat 2-7 continuously
10. EXIT

C.7.3.5 Test 5

X.25 Internal Logic Test: This test checks the on board logic of the X.25 link. All testing is done with internal loopback set on the device. The test uses all speeds and large messages.

1. Set LED's (1Ø1Ø1ØØ)
2. INIT X25 port to 19.2Kb internal clock, internal loopback
3. Set up RX
4. TX message
5. Wait for completion reporting TX timeouts and RX timeouts
6. Decrease speed
7. Repeat 2-6 until all speeds tested
8. GOTO 2

C.7.3.6 Test 6

X.25 DMA Addressing Test: Using the X.25 control logic set to internal loop back this test verifies data can be transferred into all memory. The test runs for 1 minute.

1. Set LED's (1Ø11ØØØ)
2. INIT for 19.2Kb internal loop back
3. Set high memory to AAH
4. TX high memory to low memory
5. Check data
6. Set high memory to 55H
7. TX low memory to high memory
8. Check data
9. Set low memory to 55H
10. TX low memory to high memory
11. Check data
12. Set low memory to AAH
13. TX high memory to low memory
14. Check data
15. Repeat 1Ø times

C.7.3.7 Test 7

X.25 External Test: This test allows the operator to check both the DZS11-EA option and all comms cables using X.25 messages. The test requires turn around plug to be connected or a running VT1XX-EA to be connected. The line speed set in the switch is used.

1. Set LED's (1Ø111ØØ)
2. INIT X25 port to switch
3. Set up Read
4. TX message
5. Wait for TX complete, report timeouts and TX errors
6. Wait for RX complete, report timeouts and RX errors
7. Check data
8. EXIT

C.7.4 DZS11-EA UNIBUS Diagnostic

This microcode emulates a DZ11-A in MAINTENANCE MODE. The microcode loops character as needed and creates the necessary intercharacter timeouts for TX characters.
Figure C-2 is a flow chart for a single line under test.

Figure C-2 UNIBUS Microdiagnostic State Diagram

APPENDIX D

DZ STAT MUX PROTOCOL

D.1 GENERAL.

D.1.1 Functions of the Protocol.

The functions to be supported by the protocol are:

- link set up and initialisation
- information transfer
- supervisory and error control functions
- transfer of DZ11-specific information

D.1.2 Terminology.

D.1.2.1 Use of X.25 Terminology

Terminology from the CCITT X.25 specifications will be used to discuss the information transfer, and supervisory functions.

D.1.2.2 Route-through Terminology

Referring to route through-configurations, "Primary Remote Mux" designates the first level remote mux, nearest to the local mux.

"Secondary Remote Mux" designates a second level remote mux, further away from the Local Mux.

D.2 MAIN CHARACTERISTICS OF THE PROTOCOL

D.2.1 Multiplexed Link Protocol

Information transfer, supervisory and error control functions on the multiplexed link, are based on a simplified interpretation of the CCITT-X25 Level 2 specifications, with the following deviations:-

- the use of the address field for route-through addressing (1.3.3)
- the Poll/Final bit is used only the RR/RNR frames, to enquire status, it is set to zero in all other frames (Table 1)
- the use of the HDLC RSET frame to implement power fail network restart
- the use of the special LPBK (loopback) frame for diagnostic purposes

D.2.2 Communication Mode

The communication mode will be based on the Asynchronous Balanced Mode (LAPB), where both ends of the link (the Local Mux and the Remote Mux) have balanced link control capability.

D.2.3 Route-through Addressing Algorithm.

The provision of route-through will be implemented by using the Address field in the HDLC frame.

An Address field value of Ø denotes a frame coming from or destined to the Primary Remote Mux.

The Address field value of a route through frame coming from or destined to a Secondary Remote Mux is equal to 1 for the first Secondary Remote Mux, 2 for the next level Secondary Remote Mux, etc.

When any Remote Mux (whether primary or secondary), builds a frame using characters received from its terminal ports, to be transmitted out of its communication port, it always sets the Address field to Ø. When a Remote Mux received a frame coming from a secondary Remote Mux into its Auxiliary port, it increments the frame's Address field by 1, before queuing the frame for re-transmission out of its communication port.

Thus, by the time a frame reaches the Local Mux, its address field always reflects the correct address of the Remote Mux from which it originates.

When a Remote Mux receives an I frame coming to its communication port, it accepts and processes the frame if the Address Field is zero; else it decrements the Address Field by 1, before retransmitting the frame out of its Auxiliary Port.

Since the Local Mux always puts the correct Address number into the Address Field, the Address Field of a frame originating from the Local Mux gets decremented to zero, when the frame reaches its destination Remote Mux.

This arrangement allows the Primary and Secondary Remote Mux to have identical control programs and avoid the need for setting switches to configure a remote mux into primary or secondary versions.

Table D-1 Commands and Responses

FORMAT	COMMANDS	RESPONSES	CONTROL FIELD STRUCTURE								
			LSB 1	2	3	4	5	6	7	MSB 8
INFORMATION	I (INFORMATION)	I (INFORMATION)	0	N(S)			0	N(R)		
SUPERVISORY	RR (RECEIVE READY)	RR (RECEIVE READY)	1	0	0	0	P/F	N(R)		
	RNR (RECEIVE NOT READY)	RNR (RECEIVE NOT READY)	1	0	1	0	P/F	N(R)		
		REJ (REJECT)	1	0	0	1	0	N(R)		
UNNUMBERED	RIM (REQUEST INITIALIZATION MODE)	SIM (SET INITIALIZATION MODE)	1	1	1	0	0	0	0	0
	SABM (SET ASYNC BALANCED MODE)		1	1	1	1	0	1	0	0
		UA (UNNUMBERED) ACKNOWLEDGMENT)	1	1	0	0	0	1	1	0
	RSET (RESET)		1	1	1	1	0	0	0	1
	LPBK (LOOPBACK)	LPBK (LOOPBACK)	1	1	0	1	0	1	1	1

N(S) = SEND SEQUENCE NUMBER (BIT 2 IS LSB)
N(R) = RECEIVE SEQUENCE NUMBER (BIT 6 IS LSB)
P = POLL BIT
F = FLAG BIT

D.3 ELEMENTS OF THE PROTOCOL

Table D-1 lists the types of frames which constitute the protocol elements.

These elements will be discussed further in subsequent sections.

In a nutshell:

RIM, SIM and RSET are used for link set up and initialisation.

I, RR, RNR, SABM and UA are used for information transfer, supervisory and error control functions, according to the CCITT X-25 protocol level 2..

LPBK is a special unnumbered frame used for diagnostic purpose.

D.4 LINK SET UP AND INITIALISATION

D.4.1 RIM (REQUEST INITIALISATION MODE) FRAME

Sent from	:	Remote Mux
To	:	Local Mux
When	:	at power up, repetitively at 5 seconds interval, until a SIM response from the local Mux is received in reply.
Purpose	:	notify local mux which ports on remote mux are active.
Expected Response	:	SIM RESPONSE FROM local mux, giving DZ parameters.

D.4.1.1 RIM Information Field Format.

Eight bits, one for each port.

Bit set (=1) means port active
Bit Reset (=Ø) means port not active

D.4.1.2 Expected Response from Local Mux.

The local mux has control over eight DZ lines, which we will name as DZØ to DZ7.

At power up, the Primary Remote Mux and the Secondary Remote Mux will each send a separate RIM frame to the Local Mux.

For example, take the case where the Primary Remote Mux says that it has five active ports, namely Port Ø, Port 3, Port 4, Port 5 and Port 6. Also the Secondary Remote Mux says that it has four active ports, Port 2, Port 3, Port 4 and Port 5.

The RIM messages from each remote Mux are as shown below.

NOTE that in this example the total number of active remote ports is greater than 8.

PORT NUMBER	Ø	1	2	3	4	5	6	7
PRIMARY RIM	1	Ø	Ø	1	1	1	1	Ø
SECONDARY RIM	Ø	Ø	1	1	1	1	Ø	Ø

Figure D-1 RIM Message Format

The Local Mux will always give precedence to the Primary Remote Mux RIM, in the case of such conflict over the total number of active ports.

In this example, the Local Mux will allocate five DZ lines, from DZØ to DZ4 to the Primary Remote Mux, and the 3 remaining lines (DZ5 to DZ7) to the Secondary Remote Mux according to the following mapping:

DZ LINE	REMOTE MUX	PORT NUMBER
DZ Ø	Primary	Port Ø
DZ 1	Primary	Port 3
DZ 2	Primary	Port 4
DZ 3	Primary	Port 5
DZ 4	Primary	Port 6
DZ 5	Secondary	Port 2
DZ 6	Secondary	Port 3
DZ7	Secondary	Port 4

The Local Mux, after having worked out this mapping table will then build up appropriate SIM messages and send them to both remote muxes, to give them the DZ line parameters corresponding to each allocated active port on the two remote muxes.

D.4.2 SIM (SET INITIALISATION MODE) FRAME.

Sent from : Local Mux

To : Remote Mux

When : after receipt of RIM message from Remote Mux.

Purpose : to give line parameters corresponding to each allocated active ports on the Remote Mux.

Expected Response : None. The Remote Mux will use information in Sim frame to initialise its terminal ports (to the right baud rate etc...)

D.4.2.1 SIM Information Field Format.

The information field of a SIM frame is composed of 16-bit subfields, each 16-bit subfield carrying the parameters for one terminal port at the remote mux.

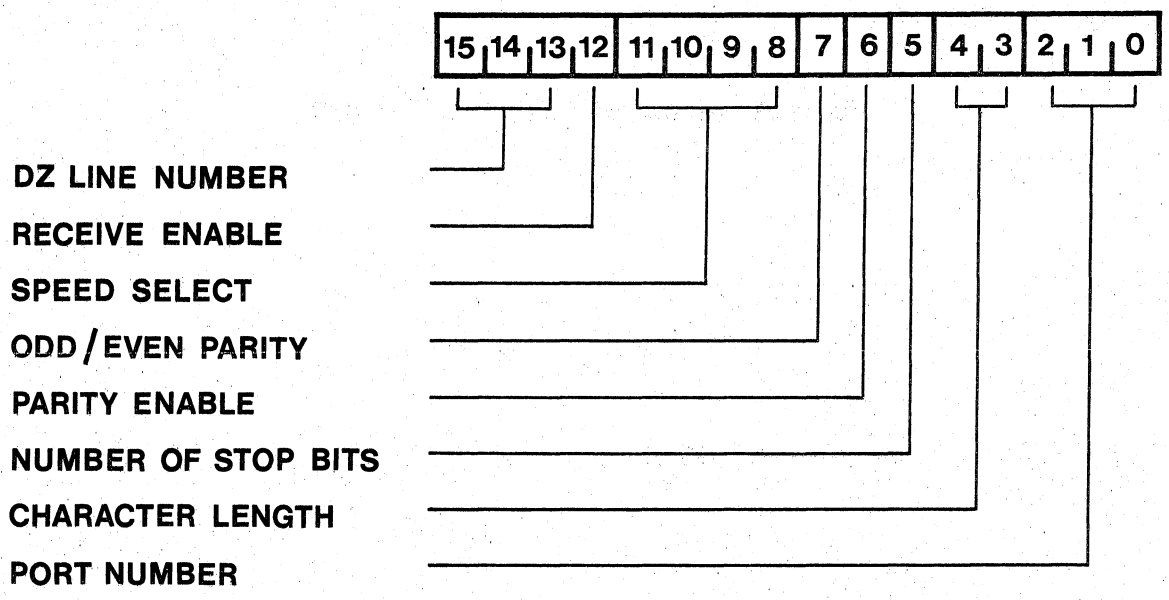


Figure D-2 SIM Message Format

Table D-2 SIM Frame Bit Definitions

Bit	Description
ØØ-Ø2	Port number : terminal port number on remote mux, to which these parameters apply.
Ø3-Ø4	Character Length : Bit 4 Bit 3 Ø Ø 5 bit characters Ø 1 6 bit characters 1 Ø 7 bit characters 1 1 8 bit characters
Ø5	Number of stop bits : Ø 1 stop bit 1 2 stop bits
Ø6	Parity Enable : Ø no parity bit 1 parity enable
Ø7	Odd/Even Parity : Ø even parity 1 odd parity
Ø8-11	Speed Select: Bit 11 Bit 1Ø Bit 9 Bit 8 Baud Rate Ø Ø Ø Ø 5Ø Ø Ø Ø 1 75 Ø Ø 1 Ø 11Ø Ø Ø 1 1 134.5 Ø 1 Ø Ø 15Ø Ø 1 Ø 1 3ØØ Ø 1 1 Ø 6ØØ Ø 1 1 1 12ØØ 1 Ø Ø Ø 18ØØ 1 Ø Ø 1 2ØØØ 1 Ø 1 Ø 24ØØ 1 Ø 1 1 36ØØ 1 1 Ø Ø 48ØØ 1 1 Ø 1 72ØØ 1 1 1 Ø 96ØØ 1 1 1 1 Reserved
12	Receive Enable : Ø disabled. 1 enabled.
13-15	DZ line number mapped to port.

D.4.3 RSET (RESET) Frame

Sent from : Local Mux, or Remote Mux, out of its Auxiliary Port.

To : Remote Mux

When : At power up

Purpose : Request Remote Mux to go through reset (power-up) sequence.

When a remote Mux received a RSET frame coming into its main communication ports, it resets itself and emulates a power up initialisation sequence.

For example, after a temporary power loss at the local mux or the Primary Remote Mux, a reset frame will be sent to the Remote Mux (or to the Secondary Remote Mux), causing the latter to reset itself for resuming operation.

D.4.4 LPBK (LOOPBACK) Frame

Sent from : any Mux (Local, Primary or Secondary Remote)

To : any other Mux

Purpose : request the receiving Mux to send back the same frame for diagnostic purpose.

D.5 INFORMATION TRANSFER, LINK SUPERVISORY & ERROR CONTROL FUNCTIONS.

These functions are implemented through the use of the I, RR, RNR, FRMR, REJ, SABM, UA frames, conforming to the CCITT X.25 level 2 protocol.

Only the I frame will be discussed here, all the other frames being identical in format and usage to the X.25 protocol elements.

D.5.1 I Frame Information Field: Terminal Port Encoding Scheme

The frame format of I frames are as defined in the CCITT X.25 Level 2 specifications.

The information field within an I frame however will be structured according to the terminal port encoding scheme shown in Figure D-3.

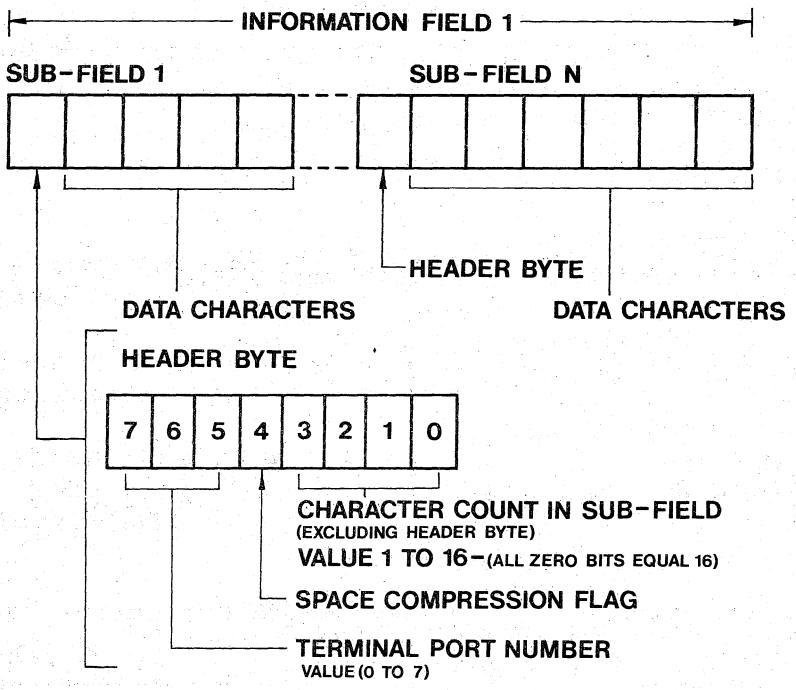


Figure D-3 Terminal Port Encoding Format

The information field is composed of a number of sub-fields. Each sub-field has an integral number of 8-bit characters, the first character in a sub-field being the sub-field's Header Byte. This Header Byte encodes the number of characters in the sub-field, and the terminal port number (on the remote mux) to which all the data characters in the sub-field belong.

The space compression flag, when set to 1, denotes that this is a special sub-field composed of only the header byte, equivalent to a number of space characters equal to the sub-field character count (1 to 16).

D.6 TRANSFER OF DZ-SPECIFIC INFORMATION

This is achieved through the special Information Frames denoted by bit 7 of the Address field being set to 1.

The information field of such an I frame consists of 16-bits. The most significant bits (bits 13-15) denote the type of the message:

Transfer Direction: From Local Mux to Remote Mux

Bit 15	Bit 14	Bit 13	UI Message Type:
Ø	1	Ø	Line Parameters
1	Ø	1	DTR
1	1	Ø	Break Command

Transfer Direction: From Remote Mux to Local Mux

Bit 15	Bit 14	Bit 13	UI Message Type:
Ø	Ø	1	Carrier Detect (CAR)
Ø	1	Ø	Transmit Enable
Ø	1	1	Transmit Disable
1	Ø	1	Route-through Disable
1	1	Ø	Route-through Enable
1	1	1	Ring

(NOTE that DTR, CAR, RING, will not be implemented in the first version of the DZ STAT MUX).

D.6.1 Line Parameters

This message is sent from the local mux to notify the remote mux of new line paramaters for a terminal port on the remote mux.

Bits ØØ to 12 of the information field have identical format and meaning as Bits ØØ to 12 of the SIM information field (see section 2.2.1).

D.6.2 Break

This message is sent from the local mux to the remote mux, to ask the remote mux to set selected terminal ports into a continuous space condition. Bits Ø to 7 corresponds to ports Ø to 7: a bit if set to 1, indicates the corresponding port is to be set into a break condition; a bit if set to zero, indicates that the corresponding port should not be in a break condition.

Bits 8-12 are unused.

D.6.3 Transmit Disable

This message is sent from the remote mux to the local mux, to inform the local mux that some terminal ports are not ready to accept more transmit characters. (This is to cater for slow terminal ports, or terminals who have sent on XOFF to the remote mux).

Bits Ø-2 of the I field give the terminal port number of the remote mux which is not ready to receive more characters.

Bits 3 to 12 are unused.

D.6.4 Transmit Enable

This message is sent from the remote mux to tell the local mux to re-enable a particular remote mux terminal port for transmission. The encoding is identical to the Transmit Disable sub-field in D.6.3.

D.6.5 Route-through Disable

This message is sent from a remote mux to tell the local mux not to send any more I frames destined to the route-through remote mux (further away from the host computer than the remote mux originating the UI message).

This is needed in such cases as a temporary breakdown of the communication line linking the two remote muxes and the primary remote mux has accumulated within its own buffer space more than 1Ø consecutive I frames destined for the secondary route-through remote mux.

D.6.6 Route-through Enable

This message tells the local mux to resume transmission to the route-through remote mux.

D.6.7 DTR, CAR, RING

These will not be implemented in Version 1 of the DZ STAT MUX. DTR is sent from the local mux, while CAR and RING go in the reverse direction, and implement the corresponding function of the DZ11.

In all these messages, bits Ø to 7 correspond to ports Ø to 7, while bits 8 to 12 are unused.

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