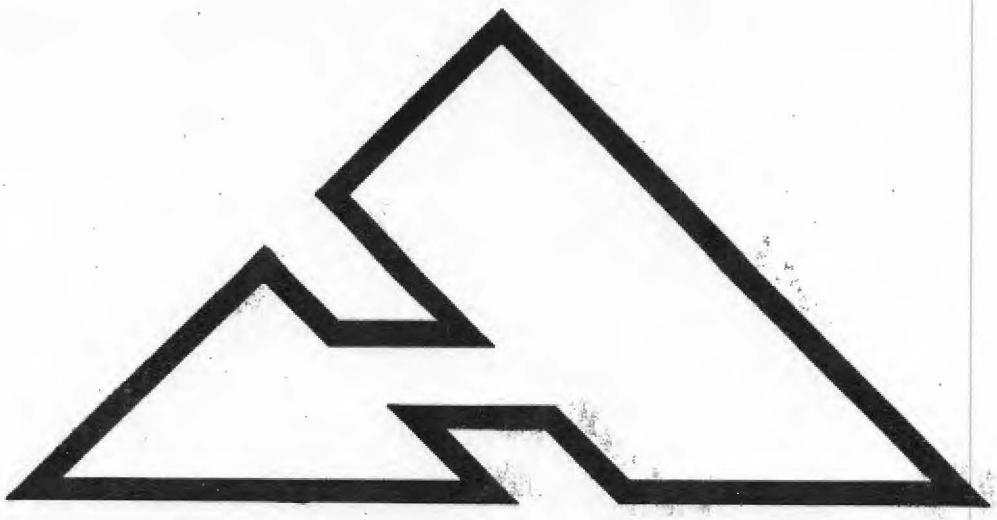

FLEX - 02

USERS GUIDE

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ADVANCED ELECTRONICS DESIGN, INC.
HEADQUARTERS: 440 Potrero Avenue • Sunnyvale, California 94086
CABLE: Disksystem • TELEX: 357498 • TELEPHONE: (408) 733-3555

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ADVANCED ELECTRONIC DESIGN, INC

FLEX02 USERS GUIDE

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DOUBLE SIDE SOFTWARE PATCHES

FOR DEC(*) RT11 V04

1.0 THE FOLLOWING PATCHES ARE REQUIRED TO OPERATE THE DEC(*) RT11 V04 DY: DRIVER WITH DOUBLE SIDED DISCS. THESE PATCHES CORRECT 3 ERRORS IN THE DY: DOUBLE SIDE CODE. TWO UNDEFINED SYMBOLS ARE DEFINED, THE LOGICAL SECTOR NUMBER (LSN) IS LOADED INTO A REGISTER BEFORE USE, AND THE DOUBLE SIDE CONTROL IS ADDED TO THE BOOTSTRAP ROUTINE (ALLOWING FILES DY.SYS, RT11FB, AND SWAP.SYS TO BE LOCATED ANYWHERE ON THE DISC).

NOTE: 'DEC' AND 'RT11' ARE REGISTERED TRADEMARKS OF DIGITAL CORP, AND ARE USED HERE WITH THAT UNDERSTANDING.

2.0 THESE PATCHES ARE MADE TO FILE 'DY.MAC' BEFORE ASSEMBLY.

```
.TECO DY.MAC                                                    <CR>
*NELDY<ESC>V<ESC><ESC>
ELDY == 2
*N177170<ESC>V<ESC><ESC>
        .DRDEF   DY,6,FILST$!SPFUN$,494.,177170,264
*1L<ESC><ESC>
*I.IIF NDF DY$DS, DY$DS = 1     ;IF UNDEFINE, MAKE 2S   <CR>
DBSID2 = 2                      ;DEFINE                  <CR>
MAXLSN = 1734*2                 ;HIGHEST SIDE 1 LSN      <CR>
<ESC><ESC>
*N<CR>
DOXFER<ESC>1LV<ESC><ESC>
.IF NE  DY$DS
*1L<ESC><ESC>
*I      MOV    DYLSN,R3      ;R3= LSN                    <CR>
<ESC><ESC>
*SDYLSN<ESC>V<ESC><ESC>
        MOV  DYLSN,R3
*0L<ESC><ESC>
*I.IF EQ DY$DS           ;R3 = LSN (FROM ABOVE FOR 2S)  <CR>
<ESC><ESC>
*1L<ESC><ESC>
*I.ENDC                                                  <CR>
<ESC><ESC>
*NBOOT1<ESC>V<ESC><ESC>
        .DRBOT   DY,BOOT1,READ1
*N<CR>
2$:<ESC>V<ESC><ESC>
2$:     MOV     #DY$CSR,R5
*I<CR>
;TEST FOR SIDE 2                                          <CR>
        CMP    R0,#MAXLSN      ;LSN ON SIDE 0?            <CR>
        BLT    22$             ;YES                       <CR>
        BIS    #CSHEAD,REDCMD  ;NO:SET SIDE 1             <CR>
        SUB    #MAXLSN,R0      ;TWEEK WORKING LSN         <CR>
22$:                                                      <CR>
<ESC><ESC>
*EX<ESC><ESC>
.
```

ADVANCED ELECTRONIC DESIGN REV 07/27/81

DOUBLE SIDED SOFTWARE PATCHES

FOR DEC (*) RSX11M V3.2 SHT 1 OF 2

NOTE: 'DEC' AND 'RSX11M' ARE REGISTERED TRADEMARKS OF DIGITAL CORP., AND ARE USED HERE WITH THAT UNDERSTANDING.

1.0 THE DEC (*) RSX11M DY: DRIVER DOES NOT CORRECTLY CONVERT THE LSN TO SIDE, TRACK, SECTOR FOR LSN'S ABOVE SIDE 2, TRACK 53. THE PATCH TO FIX THIS BUG CLEARS THE UPPER BYTE OF R0 AFTER THE BYTE SIGN BIT WAS PROPAGATED THRU THE UPPER BYTE.

2.0 SEVERAL PROBLEMS ARE ENCOUNTERED WHEN OPERATING UNDER FLX FOR FILE INTERCHANGES, BECAUSE FLX DOES NOT PERFORM SENCE MEDIA OPERATIONS.

2.1 IF THE PREVIOUS DISC WAS DOUBLE DENSITY AD THE CURRENT DISC IS SINGLE DENSITY, A 'FLX' ACCESS WILL REPORT A HARD ERROR ON THE FIRST ACCESS, THEN OPERATE OK ON SUBSIQUENT ACCESSES. A PATCH TO THE DRIVER ERROR HANDLING LOGIC IS PROVIDED TO CORRECT THIS PROBLEM.

2.2 IF THE PREVIOUS DISC WAS SINGLE SIDED AND THE CURRENT DISC IS DOUBLE SIDED, 'FLX' WILL REPORT A DRIVER ERROR (-20, LBN TOO LARGE). THE DRIVER'S INTERNAL MEDIA CHARACTERISTIC'S TABLE IS NOT UPDATED BEFORE THE DRIVER REJECTS THE OPERATION. SINCE A PATCH TO CORRECT THIS BUG WOULD CHANGE THE BASIC DRIVER LOGIC, NO PATCH IS IMPLIMENTED.

2.3 IF A MOUNT OPERATION IS ATTEMPTED BEFORE A 'FLX' OPERATION (EVEN THOUGH THE MOUNT WILL FAIL), THEN 'FLX' OPERATIONS WILL OPERATE SUCESSFULLY, BECAUSE THE MOUNT OPERATION WILL PERFORM A SENCE MEDIA FUNCTION BEFORE FAILURE, WHICH WILL CORRECT THE DRIVER CONFIGURATION TABLES.

THE FOLLOWING SLP CORRECTION FILE TO THE RX02 DEVICE DRIVER (DYDRV) WILL CORRECT THE DOUBLE SIDED BUG, PLUS THE SINGLE DENSITY FAULT.

```
DYDRV.MAC;2/AU:72./-BF=DYDRV.MAC;1
\
-2,2
     .IDENT  /01C/
-11,11
; VERSION 01C
-1,4
; MODIFIED BY:
;
;            RP025 -- CORRECT BUFFER OVERFLOW DETECTION
;
;            PJC001 -- CORRECT INVALID DEVICE NOT READY ERROR
;
;            AED000 -- CORRECT BLOCK CONVERSION, DUAL SIDE
;                      CORRECT SINGLE DENSITY RETRY
;
%
-525,525,/; PJC001/
     BEQ     400$                ; IF EQ NO
395$:        JMP     190$                ; GO DECLARE IE.VER ERROR
-527,52/,/; PJC001/
     BEQ     395$                ; IF EQ NO, ERROR
-541,,/; AED000/
     BIC     #SDEN,U.BUF(R5) ; SET SINGLE DENSITY COMMAND
-597,,/; AED000/
     BIC     #177400,R0          ; MASK TRACK NUMBER
-660,664,/; RP025/
     BIT     #DEN,U.CW2(R5)   ; SINGLE DENSITY?
     BEQ     5$                  ; IF EQ YES
     ADD     #256.,U.BUF+2(R5)  ; UPDATE BUFFER ADDRESS FOR DOUBLE DENSITY
     BR      10$                 ; AND CONTINUE
5$:  ADD     #128.,U.BUF+2(R5)  ; UPDATE BUFFER ADDRESS FOR SINGLE DENSITY
10$:         BCC     15$                 ; IF CC, NO OVERFLOW
/
```

FOLLOW THE RELEASE NOTES PROCEDURE FOR UPDATING AN EXISTING MODULE OR DEVICE DRIVER.

1.0 INTRODUCTION

THIS DOCUMENT PRESENTS A GENERAL DESCRIPTION AND A DETAILED INSTALLATION GUIDE FOR THE AED FLEX02 FLOPPY DISC CONTROLLER.

THE FLEX02 CONTROLLER IS AN EXACT EMULLATOR OF THE DEC (*) RX02 DISC CONTROLLER, AND IS COMMAND SET AND MEDIA COMPATABLE WITH IT. IT WILL RUN UNDER THE RT11 AS WELL AS OTHER DEC (*) OPERATING SYSTEMS, AND IS COMPATABLE WITH THE DEC (*) RX02 DIAGNOSTIC PROGRAMS.

THE FLEX02 ALSO PROVIDES 2 HEADED DRIVE OPERATION UNDER THE RT11 OPERATING SYSTEM.

THE FLEX02 CONTROLLER IS PACKAGED ON A DUAL WIDE LSI11 PCB, AND IS CABLED TO A 5 1/4 INCH HIGH DRIVE CABINET.

* NOTE: 'DEC' AND 'RT11' ARE REGISTERED TRADE MARKS OF DIGITAL EQUIPMENT CORP. AND ARE USED IN THIS DOCUMENT WITH THAT UNDERSTANDING.

2.0 RELEVANT DOCUMENTS

SHUGART	SA800	O.E.M. MANUAL
QUME	DT/8	O.E.M. MANUAL
DEC	RX02	SYSTEMS USERS GUIDE

3.0 GENERAL DESCRIPTION

THE FLEX02 IS 100% COMPATABLE WITH THE DEC RX02. THERE ARE NO ENHANCEMENTS AFFECTING THE COMMAND INTERFACE OR MEDIA COMPATABILITY. COMMAND INTERFACE COMPATIBILITY MEANS THE FLEX02 WILL OPERATE UNDER RT11, AND ALL RX02 DIAGNOSTIC PROGRAMS PROVIDED BY DEC. MEDIA COMPATABILITY MEANS THERE IS COMPLETE INTERCHANGIBILITY BETWEEN DEC RX02 GENERATED DISCS AND FLEX02 GENERATED DISCS.

3.1 MEDIA ARCHITECTURE

THE FLEX02 WILL HANDLE EITHER SINGLE DENSITY (DEC RX01, IBM 3740), OR DOUBLE DENSITY (DEC RX02) FORMATS. IT WILL ALSO HANDLE DOUBLE SIDED DOUBLE DENSITY FORMAT. A USER MAY USE EITHER A PRE-FORMATTED SINGLE DENSITY DISC (AND BY USING A STAND ALONE PROGRAM, AVAILABLE FROM DEC, # ZRXEA0.BIC, CAN BE CONVERTED INTO A DOUBLE DENSITY DISC), OR THE USER MAY USE BLANK DISCS WHICH THE FLEX02 WILL FORMAT IN SINGLE, DOUBLE, OR DOUBLE SIDED DOUBLE DENSITIES.

THE FLEX02 CONTROLLER PROVIDES DISC FORMAT STATUS TO THE OPERATING PROGRAM, WHICH ALLOWS THE PROGRAM TO PROVIDE DENSITY CONTROL AUTOMATICALLY. FOR EXAMPLE, THE DEC RT11 OPERATING SYSTEM DOES THIS, ALLOWING THE THE USER TO BE UNCONCERNED WITH THE FORMAT OF A PARTICULAR DISC. ONCE INSERTED INTO THE DRIVE, THE OPERATING SYSTEM READS THE ACTUAL FORMAT AND PERFORMS ALL DATA TRANSFERS AND SECTOR MAPPING FOR THE ACTUAL FORMAT. IN ADDITION THE OPERATING SYSTEM TESTS THE FORMAT WHEN INITIALIZING THE DISC'S DIRECTORY TO SET UP THE CORRECT SIZE.

THE FORMAT OF THE DISC IS 77 TRACKS PER SIDE, NUMBERED 00-76, WITH 26 SECTORS PER TRACK, NUMBERED 01-26. EACH SECTOR INCLUDES A HEADER FIELD CONTAINING THE HEAD, TRACK, AND SECTOR NUMBER (RECORDED IN SINGLE DENSITY), AND A DATA FIELD OF 128 OR 256 BYTES (RECORDED IN EITHER SINGLE OR DOUBLE DENSITY). THE DATA FIELD IS PRECEDED BY A DATA MARK WHICH IDENTIFIES THE DENSITY OF THE DATA FIELD (HOWEVER, ALL SECTORS ON A DISC MUST BE THE SAME DENSITY). WHEN USING A DOUBLE SIDED DISC, UNDER RT11, THE DATA IS RECORDED UP THE FIRST SIDE, THEN UP THE SECOND SIDE. EXCEPT FOR THE FORMAT OPERATION PROVIDED BY THE FLEX02 DURING THE BOOTSTRAP CONSOLE SESSION, THE CONTROLLER NEVER ALTERS THE HEADER FIELD ON A DISC.

MEDIA CAPACITY WITH THE FLEX02 IS:

SINGLE DENSITY	256,256 BYTES
DOUBLE DENSITY	512,512 BYTES
DOUBLE DENSITY, DOUBLE SIDE	1,025,024 BYTES

3.2 CONTROLLER ARCHITECTURE

THE FLEX02 CONTROLLER INTERFACES A DEC LSI11 COMPUTER DIRECTLY TO TWO FLOPPY DISC DRIVES WHICH HAVE A SHUGART 800 COMPATIBLE INTERFACE. IT RESIDES WITHIN THE COMPUTER CARD CAGE. THE CONTROLLER IS MICROPROCESSOR BASED, MOST INTERNAL OPERATIONS ARE PERFORMED IN MICROCODE.

THESE OPERATIONS INCLUDE:

- COMPUTER COMMAND DECODING AND EXECUTION
- DMA DATA TRANSFER CONTROL AND ADDRESSING
- STATUS WORD ASSEMBLY AND UPDATING
- DRIVE CONTROL LOGIC (STEP, SELECT, READY, ETC.)
- DRIVE R/W MODE SETUP
- WRITE/ERASE GATE TIMING
- ADDRESS HEADER COMPARISON
- DISC FORMAT ANALYSIS
- DISC FORMATTING FUNCTIONS
- DISC DRIVE TYPE DETECTION
- END OF TRANSFER INTERRUPT GENERATION
- DIAGNOSTIC ROUTINES

IN CONJUNCTION WITH THIS MICROPROGRAM, AN ADDITIONAL MICROPROGRAMMED SEQUENCER IS USED FOR SERIAL DISC DATA TRANSFERS WITH THE FOLLOWING FUNCTIONS:

- SERIALIZE/DESERIALIZE DATA
- WRITE PRECOMPENSATION
- PHASE LOCK OSCILLATOR CONTROL
- CLOCK ENCODING/DECODING
- RECORD MARK GENERATION/DETECTION
- CRC ACCUMULATION

A THIRD LOGICAL AREA IS THE CIRCUITS FOR BUS INTERFACING TO SYCHRONIZE THE HOST BUS CYCLES WITH THE INTERNAL MICROPROCESSOR.

TWO DATA FLOW PATHS EXIST WITHIN THE FLEX02. DATA TRANSFER BETWEEN THE DISC AND THE CONTROLLER'S INTERNAL SECTOR BUFFER IS ONE OPERATION, TRANSFERS BETWEEN THE INTERNAL BUFFER AND HOST MEMORY ES A SEPARATE OPERATION. THUS, THERE IS NO DANGER OF DATA OVERRUNS DUE TO DMA CONTENTION FROM OTHER DEVICES IN THE HOST'S COMPUTER SYSTEM.

4.0 FLEX02 PROGRAM IO INSTRUCTION SET

4.1.0 PIO ADDRESSING (STANDARD ASSIGNMENT)

```
177170....CSR-----COMMAND-STATUS REGISTER
177172....ESR-----EXTENDED STATUS REGISTER
177172....DBR-----DATA BUFFER REGISTER

   264....INTERRUPT VECTOR
```

4.1.1 CSR BIT DEFINITION

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
ERR	INT	MAD	MAD	1	0	SID	DEN	TR	INE	RDY	UN	FUN	FUN	FUN	GO
R	W	W	W	R		R/W	R/W	R	R/W	R	R/W	W	W	W	W

ERR: ANY CONTROLLER ERROR
INT: CONTROLLER RESET
MAD: EXTENDED BUS ADDRESS BITS 17,16
SID: SIDE SELECT
DEN: DENSITY SELECT (0 = SINGLE, 1 = DOUBLE)
TR: DBR TRANSFER REQUEST
INE: INTERRUPT ENABLE
RDY: CONTROLLER READY
UN: UNIT SELECT
FUN: CONTROLLER FUNCTION SELECT

CODE	FUNCTION
000	FILL BUFFER
001	EMPTY BUFFER
010	WRITE SECTOR
011	READ SECTOR
100	SET DENSITY (FORMAT)
101	READ DRIVE STATUS
110	WRITE SECTOR (DELETED DATA MARK)
111	READ FULL ERROR STATUS

GO: COMMAND INITIATE FLAG

4.1.2 DBR DEFINITION

THE DBR IS DEFINED IN THE VARIOUS COMMAD SEQUENCES.

WARNING: NEVER READ OR WRITE TO THE DBR EXCEPT IN THE CORRECT SEQUENCE, OR A UNDEFINED FAILURE MAY OCCUR FOR THE FUNCTION IN PROGRESS.

IN GENERAL, THE USER MUST NEVER WRITE INTO THE DBR, EXCEPT WHEN THE TR BIT IS SET IN THE CSR DURING A COMMAND SEQUENCE. THE USER MUS NEVER READ FROM THE DBR EXCEPT WHEN THE CONTROLLER IS READY (RDY BIT IS SET IN THE CSR).

4.1.3 ESR BIT DEFINITIONS

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	NXM	OVF	SID	UN	DRY	DEL	DEN	DNE	ALO	INT	SRY	CRC

NXM: NON-EXISTANT MEMORY
OVF: WORD COUNT OVERFLOW
SID: SIDE SELECTED (ACTUAL)
UN: UNIT SELECTED (ACTUAL)
DRY: DRIVE READY (SELECTED DRIVE)
DEL: DELETED DATA SECTOR READ
DEN: DENSITY (ACTUAL) (0 = SINGLE, 1 = DOUBLE)
DNE: DENSITY ERROR
ALO: DRIVE CABINET AC LOW
INT: CONTROLLER RESET DONE
SRY: SIDE 2 READY
CRC: CRC ERROR

THE ESR CAN BE READ FROM THE DBR AT THE COMPLETION OF ANY COMMAND, OR CAN BE AQUIRED IN THE DBR BY EXECUTING A READ DRIVE STATUS COMMAND.

4.2.0 COMMAND SEQUENCES

THE FOLLOWING COMMAND SEQUENCES ARE DESCRIBED FOR OPERATION UNDER PROGRAM CONTROL.

WHEN MANUALLY EXECUTING COMMANDS USING THE CONSOLE ODT, THE FIRST DBR WORD MUST BE PRE-WRITTEN BEFORE WRITING THE CSR COMMAND, BECAUSE WHEN ODT OPENS THE DBR LOCATION, IT FIRST READS IT, WHICH WILL CAUSE THE FLEX02 TO RESET THE TR FLAG BIT, READ THE DBR DATA, AND SET THE TR BIT FOR THE SECOND DATA WORD.

4.2.1 FILL/EMPTY BUFFER FUNCTIONS

```
WRITE: MAD:DEN:FUN:GO=1---INTO CSR (TYP:401/403; 001/003 OCTAL)
@TR=1:
WRITE: WORD COUNT---------INTO DBR (0-200/0-100 OCTAL)
@TR=1:
WRITE: BUS ADDRESS--------INTO DBR
```

THE CONTROLLER FILLS/EMPTIES ITS INTERNAL BUFFER FROM/INTO THE CPU'S MEMORY.

A FILL OPERATION WILL POST FILL ITS BUFFER WITH ZEROES IF THE WORD COUNT IS LESS THAN THE MAX WORD COUNT

4.2.2 READ/WRITE/WRITE(DELETED DATA) FUNCTIONS

```
WRITE: SID:DEN:UN:FUN:GO=1--INTO CSR (TYP: 407/405; 007/005 OCTAL)
@TR=1:
WRITE: SECTOR #-------------INTO DBR (1-32 OCTAL)
@TR=1:
WRITE: TRACK #--------------INTO DBR  (0-114 OCTAL)
```

THE SELECTED READ/WRITE OPERATION FROM/TO THE DISC DRIVE IS PERFORMED INTO/FROM THE CONTROLLER'S INTERNAL BUFFER.

4.2.3 READ DRIVE STATUS

```
WRITE: SID:UN:FUN:GO=1--INTO CSR (TYP: 013 OCTAL)
```

DRIVE READY (DISC INSERTED), DISC DENSITY, AND NUMBER OF HEADS ARE TESTED FOR THE SELECTED UNIT. STATUS IS RETURNED IN THE ESR.

WARNING: REQUIRES 250 MS FOR COMMAND COMPLETION.

4.2.4 SET MEDIA DENSITY (FORMAT DISKETTE)

```
WRITE: DEN:UN:FUN:GO=1--INTO CSR (TYP: 411/011 OCTAL)
@TR=1:
WRITE: KEYWORD----------INTO DBR (TYP: 0111 OCTAL ('I' ASCII))
```

THIS COMMAND WRITES ALL SECTORS OF ALL TRACKS OF ALL HEADS IN THE SELECTED DENSITY. THE DATA WRITTEN ARE ALL ZEROES. THE COMMAND DOES NOT REWRITE THE HEADER INFORMATION.

WARNING: REQUIRES 15 SEC FOR COMMAND COMPLETION.

WARNING: IF COMMAND IS ABORTED BEFORE COMPLETION,
A FALLICIOUS DISC WILL BE REMAIN.

4.2.5 READ FULL ERROR STATUS

WRITE: FUN:GO=1--------INTO CSR (TYP: 017 OCTAL)
@TR=1:
WRITE: BUS ADDRESS----INTO DBR

THE CONTROLLER EMPTIES ITS INTERNAL STATUS REGISTERS
INTO THE CPU'S MEMORY

THE CPU MEMORY FORMAT IS:

BA+0:<15:8> WORD COUNT.....<7:0> ERROR CODE
BA+2:<15:8> CURRENT TRACK, UN1...<7:0> CURRENT TRACK, UN0
BA+4:<15:8> TARGET SECTOR.....<7:0> TARGET TRACK, LAST ACCESS
BA+6:<15:8> TRACK (ERR CODE 150).<7:0> MISC STATUS BITS

MISC STATUS BITS:
- BIT 7: UNIT SELECTED
- BIT 6: DRIVE DENSITY: UN1
- BIT 5: HEAD LOAD FLAG
- BIT 4: DRIVE DENSITY: UN0
- BIT 3: 0
- BIT 2: 0
- BIT 1: 0
- BIT 0: DENSITY (READ ERROR REG COMMAND)

THE ERROR CODES ARE:

000	-----	--
010	SEEK	HOME NOT FOUND (UN 0)
020	SEEK	HOME NOT FOUND (UN 1)
030	-----	--
040	SYST	ACCESS ATTEMPT TO TRACK .GT. 76
050	SEEK	HOME FOUND BEFORE TARGET TRACK FOUND
060	-----	--
070	R/W	TARGET SECTOR NOT FOUND BEFORE 52 SECTORS PAST
100	SYST	WRITE ATTEMPT ON A WRITE PROTECTED DISC
110	R/W	NO DISC TRANSITION FOUND IN 40 US
120	R/W	NO PREAMBLE FOUND
130	R/W	PREAMBLE FOUND BUT NO ID MARK FOUND
140	R/W	CRC ERROR ON WHAT APPEARS TO BE THE HEADER
150	SEEK	TRACK ADDRESS NOT EQUAL TO TARGET TRACK
160	R/W	TOO MANY TRIES FOR AN IDAM
170	R/W	DATA MARK NOT FOUND FOR TARGET SECTOR
200	CRCE	CRC DATA ERROR FOUND
210	-----	--
220	DIAG	R/W ELECTRONICS FAILURE
230	SYST	WORD COUNT OVERFLOW
240	DENS	DENSITY ERROR
250	SYST	WRONG KEYWORD FOR SET DENSITY COMMAND
260*	R/W	SIDE DOES NOT EQUAL TARGET SIDE
270*	SYST	ATTEMPT TO ACCESS SIDE 2 OF 1 SIDED DISC

ERROR CLASSES:
- SYST--PROGRAMMING ERROR
- DIAG--CONTROLLER SELF DIAGNOSTIC ERROR
- SEEK--DRIVE SEEKING ERROR
- R/W---DRIVE READ/WRITE ERROR
- DENS--DISC DENSITY DISCREPANCY

4.2.6 CONTROLLER RESET

EITHER: WRITE: INT=1------INTO CSR (AT ANY TIME)

OR: EXECUTE THE CPU RESET INSTRUCTION

OR: PERFORM AN EXTERNAL SYSTEM RESET
(LIKE THE POWER UP RESET)

OR: TURN THE FLEX02 DRIVE CABINET AC POWER ON
(AFTER CPU POWER ON)

THE CONTROLLER WILL DO THE FOLLOWING UPON RECEIPT OF
AND OF THESE RESET FUNCTIONS:

A. HARD RESET THE CONTROLLER (EXCEPT FOR DRIVE CABINET POWER ON). ALL ERROR BITS ARE CLEARED, READY IS RESET, INTERRUPT ENABLE IS RESET.
B. EXECUTE A SELF DIAGNOSTIC PROGRAM (RETURNING STATUS IN THE CSR, ESR, AND VIA THE READ FULL ERROR STATUS COMMAND, WHEREVER POSSIBLE, OR NECESSARY).
C. RETURN BOTH DRIVES TO THE HOME POSITION.
D. READ UNIT 0, TRACK 0, HEAD 0, SECTOR 0 INTO THE CONTROLLERS INTERNAL BUFFER.
E. TERMINATE THE FUNCTION BY ASSERTING READY IN THE CSR, AND INITIALIZE DONE IN THE ESR.

4.2.7 DRIVE AC POWER OFF

WHENEVER THE DRIVE AC POWER IS OFF, THE CONTROLLER WILL ASSERT THE AC LOW FLAG IN THE ESR IN RESPONCE TO ANY COMMAND, AND ASSERT A CONTROLLER ERROR STARUS BIT IN THE CSR IN RESPONCE TO ANY DRIVE ORIENTED COMMAND. SEE PARAGRAPH 4.2.6 FOR OPERATION WITH A NEW POWER ON CONDITION.

4.3.0 • BOOTSTRAP FUNCTIONS

THE FLEX CONTROLLER PROVIDES BOOTSTRAP CAPABILITY FOR ALL STANDARD CPU DISC DEVICES, AS WELL AS BOOTSTRAPPING FROM ITSELF. IT ALSO PROVIDES THE CAPABILITY FOR FORMATTING BLANK DISCS ON THE FLEX02 SYSTEM.

THE FLEX02 BOOTSTRAP IS A HOST PROGRAM, RESIDING AT A STARTING ADDRESS OF 173000 (OCTAL) TO ALLOW USE OF THE STANDARD CPU POWER UP JUMP FUNCTION. THE BOOTSTRAP PROGRAM USES THE CPU CONSOLE DEVICE FOR CONTROL, WHICH MUST BE AT ADDRESS 177560.

4.3.1 BOOTSTRAP COMMANDS

THE BOOTSTRAP FUNCTIONS LOAD HEAD 0, TRACK 0, SECTOR 1 OF THE SELECTED UNIT (UNIT 0 IF NO UNIT SPECIFIED) OF THE SELECTED DEVICE INTO CPU MEMORY STARTING AT MEMORY LOCATION 0, LOADS THE UNIT NUMBER INTO THE CPU'S REGISTER 0, AND TRANSFERS CONTROL TO THE CPU AT LOCATION 0.

THE FLEX02 BOOTSTRAP PROGRAM WILL AUTOMATICALLY BOOTSTRAP LOAD FROM THE FLEX02, UNIT 0 IF THE OPERATOR DOESN'T TYPE ANOTHER FUNCTION WITHIN 1.5 MINUTES AFTER THE BOOTSTRAP PROGRAM BEGINS EXECUTION, TO PROVIDE AUTOMATIC RELOADING AT UNATTENDED SITES AFTER POWER FAILURES.

DY<CR>: DY0<CR>, DY1<CR>: BOOT FROM FLEX02, UNIT 0,1

DL<CR>, DL0<CR>, DL1<CR>: BOOT FROM RL01/RL02, UNIT 0,1

DK<CR>, DK0<CR>--DK7<CR>: BOOT FROM RK05, UNIT 0--7

FD<CR>, FD0<CR>--FD3<CR>: BOOT FROM AED31/6200, UNIT 0--3

4.3.2 SYSTEM COMMANDS

OD<CR>: TRANSFER CONTROL TO THE CPU'S ODT MONITOR (IE: HALT)

4.3.3 FLEX02 DISC FORMATTING COMMANDS

THE USER IS PROVIDED WITH THE FACILITY TO FORMAT DISC HEADER INFORMATION ONTO BLANK DISCS. THE CONTROLLER GENERATES A STANDARD IBM TRACK PATTERN, BEGINNING EACH TRACK AT THE INDEX MARK, AND NUMBERING THE SECTORS IN ACCENDING ORDER. IF A TWO SIDED DISC IS INSERTED, BOTH SIDES ARE FORMATTED.

THE FOLLOWING 2 COMMANDS MUST BE ISSUED TO FORMAT A DISC. NONE MAY BE LEFT OUT. THE FORMAT FUNCTION REQUIRES ABOUT 15 SECONDS TO COMPLETE.

XD1<CR>, XD2<CR>: SELECT SINGLE OR DOUBLE DENSITY

XU<CR>, XU0<CR>, XU1<CR>: SELECT UNIT 0,1 AND GO DO IT

5.0 INSTALATION GUIDE

5.1 PRESETTUP REQUIREMENTS

THE FLEX02 DRIVE CABINET IS DESIGNED TO MOUNT IN A STANDARD 19 INCH RACK. THE PACKAGE FITS INTO A 5 1/4 INCH VERTICAL SPACE, AND IS 21 INCHES DEEP.

THE DRIVE CABINET REQUIRES THE FOLLOWING AC VOLTAGES:

115 VAC, 10% TOL, 60 HZ, 0.5 HZ TOL
100 VAC, 10% TOL, 50 HZ, 0.5 HZ TOL
100 VAC, 10% TOL, 60 HZ, 0.5 HZ TOL
1.7 AMP MAX OPERATING
2.9 AMP MAX STARTUP

230 VAC, 10% TOL, 50 HZ, 0.5 HZ TOL
200 VAC, 10% TOL, 50 HZ, 0.5 HZ TOL
1.3 AMP MAX OPERATING
2.1 AMP MAX STARTUP

POWER DISSIPATION IS 200 WATTS.

THE CONTROLLER MOUNTS INSIDE THE CPU CABINET. IT WILL REQUIRE:

+5 VDC, 5% TOL, 1.9 AMP TYPICAL, 3.5 AMP MAX
+12 VDC, 10% TOL, 0.1 AMP MAX

5.2 MOUNTING PROCEDURE

THE DRIVE CABINET IS COMPOSED OF TWO PIECES, A TOP/SIDES ASSEMBLY, AND A BASE/BACK ASSEMBLY. THE TOP/SIDES ASSEMBLY IS PERMINENTLY MOUNTED INTO THE RACK, WHILE THE BASE/BACK ASSEMBLY (WHICH INCLUDES THE DRIVES, POWER SUPPLY, AND AC WIRING) SLIDES IN OR OUT OF THE TOP/SIDES ASSEMBLY FOR SERVICING.

THE TWO ASSEMBLIES ARE SHIPPED BOLTED TOGETHER. TO MOUNT IN A RACK:

A. REMOVE 4 SCREWS FROM BACK, AND 4 SCREWS FROM THE BASE. SLIDE THE BASE/BACK ASSEMBLY OUT OF THE TOP/SIDES ASSEMBLY, FROM THE FRONT.
B. INSTALL THE TOP/SIDES ASSEMBLY INTO THE RACK WITH 4 SCREWS FOR THE FRONT MOUNTING, AND 4 SCREWS FOR THE REAR MOUNTING. FOR THE REAR MOUNTING, TWO MOUNTING BRACKETS MUST BE ATTACHED TO THE TOP/SIDES ASSEMBLY SPACED ACCORDING TO THE RACK DEPTH.
C. SLIDE THE BASE/BACK ASSEMBLY INTO THE TOP/SIDES ASSEMBLY, MAKING SURE THE FLAT CABLE IS ROUTED OVER THE TOP OF THE BACK IN THE GROOVE PROVIDED. INSTALL THE 4 SCREWS INTO THE BACK TO RETAIN THE BASE/BACK ASSEMBLY IN PLACE.
D. SNAP ON THE FRONT BEZEL.
E. INSTALL THE FLEX02 CONTROLLER IN THE LSI11 CARD CAGE, ROUTE AND CONNECT THE FLAT SIGNAL CABLE BETWEEN THE DRIVE CABINET AND FLEX02 PCB.

5.3 HOST CONFIGURATION REQUIREMENTS

THE HOST CPU (DEC LSI11/02,03,23) CONFIGURATIONS WHICH INVOLVE THE FLEX02 ARE THE POWER UP JUMP OPTION ON THE CPU BOARD. TO ENABLE THE FLEX02 BOOTSTRAP FEATURES, THE CPU SHOULD BE JUMPERED TO JUMP TO ADDRESS 173000 (OCTAL) AT POWER UP. TO USE THE FLEX02 BOOTSTRAP, NO OTHER BOOTSTRAP DEVICES SHOULD COEXIST WITH THE FLEX02.

FOR TEST PURPOSES, IF ANOTHER BOOTSTRAP DEVICE EXISTS IN THE SYSTEM, THE FLEX02 BOOTSTRAP CAN BE ENTERED AT ADDRESS 173400, IF THE OTHER DEVICE DOES NOT USE ADDRESSES ABOVE 173376 (FOR EXAMPLE, THE AED 6200/3100 DISCS USE THE ADDRESS RANGE 173000-173010).

5.4 FLEX CONFIGURATION JUMPERING

FOR ILLUSTRATION OF CONFIGURATION JUMPERING, SEE LOGIC DIAGRAM #120014-01, SHEET 11.

THE I/O ADDRESS OF THE FLEX CAN BE FREELY JUMPERED WITHIN THE RANGE 160000-177776.

THE INTERRUPT VECTOR OF THE FLEX CAN BE SELECTED FROM A SET OF FOUR:

264: STANDARD VECTOR, FIRST CONTROLLER
270: STANDARD VECTOR, SECOND CONTROLLER
160: ALTERNATIVE VECTOR
170: ALTERNATIVE VECTOR

OTHER VECTORS MUST BE SPECIAL ORDERDED FROM AED.

THE BOOTSTRAP STARTING ADDRESS IS 173000. TO DISABLE THE BOOTSTRAP FUNCTION OR TO SELECT AN ALTERNATE ADDRESS, IT MUST BE SPECIAL ORDERED FROM AED. THE BOOTSTRAP PROGRAM OCCUPIES 512 BYTES IN THE ADDRESS RANGE 173000-173776.

THE FLEX02 IS COMPATIBLE WITH THE LSI11/23 4 LEVEL PRIORITY INTERRUPT FEATURE. IT MUST BE CONNECTED IN THE POSITION DEPENDENT CONFIGURATION AND CAN ONLY BE OPERATED ON PRIORITY LEVEL 4, AS DESCRIBED IN THE LSI11 MICROPROCESSOR HANDBOOK.

5.5 TO BE ADDED

5.6 POWER ON OPERATION

APPLY POWER. SYSTEM SHOULD LOAD HEADS ON BOTH FLEX02 DRIVES AND SEEK TRACK 0 ON EACH (THE FLEX02 WILL DO THIS ANY TIME A BUS INIT IS DONE BY THE CPU). THE SYSTEM SHOULD THEN PRINT OUT A DOLLAR SIGN ON THE CONSOLE DEVICE. INSERT A BOOTSTRAPPABLE DISC AND TYPE IN:

$DY<CR> (OR DY1<CR>, OR OTHER COMMAND TO A BOOTSTRAPPABLE DISC UNIT)

THE OPERATING CODE SHOULD LOAD INTO THE CPU AND BEGIN EXECUTING.

5.7 NOTES ON THE DEC(*) DIAGNOSTIC PROGRAM

THE DEC DIAGNOSTIC PROGRAM (VENDOR # ZRXDA0.BIC) WILL RUN WITH OUT MODIFICATION ON THE FLEX02 CONTROLLER. REFER TO THE USERS GUIDE FOR THIS PROGRAM FOR OPERATING INSTRUCTIONS.

ONE NOTE OF ADDITIONAL INFORMATION IS REQUIRED FOR TESTING 2 HEADED SYSTEMS. IN THIS DIAGNOSTIC, THE SECOND HEAD IS TESTED AS A SEPARATE UNIT FROM THE FIRST HEAD. TESTING 2 HEADED SYSTEMS IS NOT SPELLED OUT IN THE USERS GUIDE. A SAMPLE DIALOG FOR THIS DIAGNOSTIC FOR TESTING TWO 2 HEADED DRIVES FOLLOWS:

TYPEOUT	TYPEIN	COMMENTS
DS-B>	START	START TEST
UNITS?	4	2 HEADS OF 2 DRIVES
UN1 ADRS	<CR>	USE DEFAULT ADDRESS
VECT	<CR>	USE DEFAULT VECTOR
DRIVE	0<CR>	DRIVE 0
EXPANSION	0<CR>	HEAD 0
UN2 ADRS	<CR>	
VECT	<CR>	
DRIVE	0<CR>	DRIVE 0
EXPANSION	1<CR>	HEAD 1
UN3 ADRS	<CR>	
VECT	<CR>	
DRIVE	1<CR>	DRIVE 1
EXPANSION	0<CR>	HEAD 0
UN4 ADRS	<CR>	
VECT	<CR>	
DRIVE	1<CR>	DRIVE 1
EXPANSION	1<CR>	HEAD 1
CHANGE SWITCH?	Y<CR>	YES
HELP?	Y<CR>	IF DESIRED
EXERCISE	3<CR>	OR OTHER; 3=WRITE/READ/COMPARE
DATA PATTERN?	0<CR>	OR OTHER; 0=RANDOM DATA
TRACK SEQUENCE?	1<CR>	OR OTHER; 1=ASSENDING ORDER
DOUBLE DENSITY?	Y<CR>	DOUBLE DENSITY
DELETED DATA?	<CR>	DEFAULT
FLAGS?	<CR>	
TRACK LIMITS	<CR>	TRACK 00-76
SECTOR LIMITS	Y<CR>	SPECIFY LIMITS
MIN	1<CR>	SECTORS 1-26; ENTER SECTOR
MAX	26<CR>	MIN=1, MAX=1 TO SPEED UP TEST
FUTURE EXPANSION?	Y<CR>	MUST BE ANSWERED 'Y' IF ANY UNIT SELECT EXPANSION QUESTIONS WERE ANSWERED '1'

(THE DIAGNOSTIC NOW BEGINS RUNNING)

6.0 FLEX DRIVE JUMPER REQUIREMENTS (GENERAL)

THE FLEX IS CONSTRUCTED TO INTERFACE TO A 50 PIN FLAT CABLE WITH PINOUTS OF THE SHUGART 800 STRUCTURE. ANY DRIVE WITH SIMILAR STRUCTURE MAY BE INTERFACED.

6.1 THE FOLLOWING DRIVE JUMPER OPTIONS MUST BE USED TO INTERFACE CORRECTLY. THE NOMENCLATURE USED HERE IS THE STANDARD SHUGART NOMENCLATURE, THE SAME NOMENCLATURE IS USED BY MOST ALTERNATIVE VENDORS. REFER TO VENDOR DOCUMENTS FOR PHYSICAL JUMPER LOCATIONS WITHIN THE DRIVES.

A...INSTALLED	CONTROLS DSEL, HL FUNCTIONS
B...DELETED	CONTROLS DSEL, HL FUNCTIONS
X...INSTALLED	CONTROLS DSEL, HL FUNCTIONS
R...INSTALLED	ENABLES DRIVE READY STATUS
I...INSTALLED	ENABLES DRIVE INDEX STATUS
Z...DELETED	ALT INPUT PIN ENABLES HL FUNCTION
HL..INSTALLED	HL FUNCTION ENABLES STEPPER POWER
Y...INSTALLED	HL FUNCTION LOCKS DOOR, LITES LED
DL..DELETED	IN USE LOCKS DOOR
DS..DELETED	DSEL DOES NOT ENABLE STEPPER POWER
2S..INSTALLED	ENABLES 2 SIDE STATUS (FOR 2 SIDE DRIVES ONLY)
DC..INSTALLED	ENABLES DISC CHANGE STATUS
D...DELETED	DISABLE IN USE SIGNAL

6.2 THE FOLLOWING JUMPER OPTIONS ALLOW USAGE WITH STANDARD PERFORMANCE DRIVES (FOR 1 HEAD DRIVES, A STEPPING RATE OF 8.0 MS, FOR 2 HEAD DRIVES, A STEPPING RATE OF 3.0 MS). THEY CONTROL WHICH UNIT IS ACCESSED BY THE CONTROLLER.

6.2.1 UNIT #0 (PHYSICALLY THE LEFT HAND DRIVE)

DS1.INSTALLED	DRIVE SELECT 1
C...INSTALLED	ALT INPUT: HEAD LOAD 1

TERMINATOR IS INSTALLED (2 R-PACKS)

6.2.2 UNIT #1 (PHYSICALLY THE RIGHT HAND UNIT)

DS2.INSTALLED	DRIVE SELECT 2
(IO PIN 16 CONNECTED TO C)	ALT INPUT: HEAD LOAD 2

TERMINATOR IS REMOVED (2 R-PACKS)

6.3 THE FOLLOWING JUMPER OPTIONS ALLOW USAGE WITH DRIVES WITH A STEP RATE OF 11.0 MS (LIKE PERTEC 514)

6.3.1 UNIT #0 (PHYSICALLY THE LEFT HAND DRIVE)

DS3.INSTALLED — DRIVE SELECT 3
C...INSTALLED — ALT INPUT: HEAD LOAD 1
TERMINATOR IS INSTALLED (2 R-PACKS)

6.3.2 UNIT #1 (PHYSICALLY THE RIGHT HAND DRIVE)

DS4.INSTALLED — DRIVE SELECT 4
(IO PIN 16 CONNECTED TO C) — ALT INPUT: HEAD LOAD 2
TERMINATOR IS REMOVED (2 R-PACKS)

6.4 THE FOLLOWING IS A SUMMARY OF THE DRIVE PARAMETERS ASSUMED BY THE FLEX CONTROLLER.

STANDARD (1 HEAD)	STANDARD (2 HEAD)	SPECIAL (1 HEAD)	
8.0 MS	3.0 MS	11.0 MS	.....STEPPING RATE
8.0 MS	15.0 MS	20.0 MS	.....STEP SETTLING TIME
35.0 MS	35.0 MS	40.0 MS	.....HEAD LOAD TIME
....	....	50.0 MS	.....LAST STEP TO TRACK 0 STATUS

6.4.1 THE FOLLOWING ARE OTHER PARAMETERS PROVIDED BY THE FLEX CONTROLLER.

10.0 US.....STEP PULSE WIDTH
590.0 US.....WG END TO NEXT STEP PULSE
(TUNNEL ERASE DELAY)
590.0 US.....WG END TO READ DATA VALID
2.0 SEC.....POWER ON TO VALID DRIVE OPERATIONS DELAY
0.0 MS.....DRIVE SELECT TO READ DATA VALID
(ASSUMES THAT HEAD LOAD CONTROLS STEPPER POWER, NOT DRIVE SELECT)

6.5 DRIVE DAISY CHAIN

CABLE DRIVES IN THE FOLLOWING ORDER: FLEX CONTROLLER, DRIVE 1 (RIGHT HAND DRIVE), DRIVE 0 (LEFT HAND DRIVE). MAXIMUM CABLE LENGTH IS 15.0 FT (TOTAL CABLE LENGTH).

6.6 +24 VOLT POWER CHARACTERISTICS

WITH BOTH HEADS UNLOADED, THE SYSTEM DRAWS MINIMUM (IDLE) CURRENT. WITH BOTH HEADS LOADED (NOT STEPPING, OR ONE STEPPING) THE SYSTEM DRAWS MAXIMUM POWER.

6.7 SYSTEM GROUNDING

THE DRIVE CABINET DC GROUND AND AC/NEMA GROUND SHOULD NOT BE CONNECTED. DC GROUND POTENTIAL IS ESTABLISHED THRU THE SIGNAL CABLE TO THE CPU SYSTEM GROUND POINT.

TABLE XX: 1 SIDE/ 2 SIDE DISC IDENTIFICATION

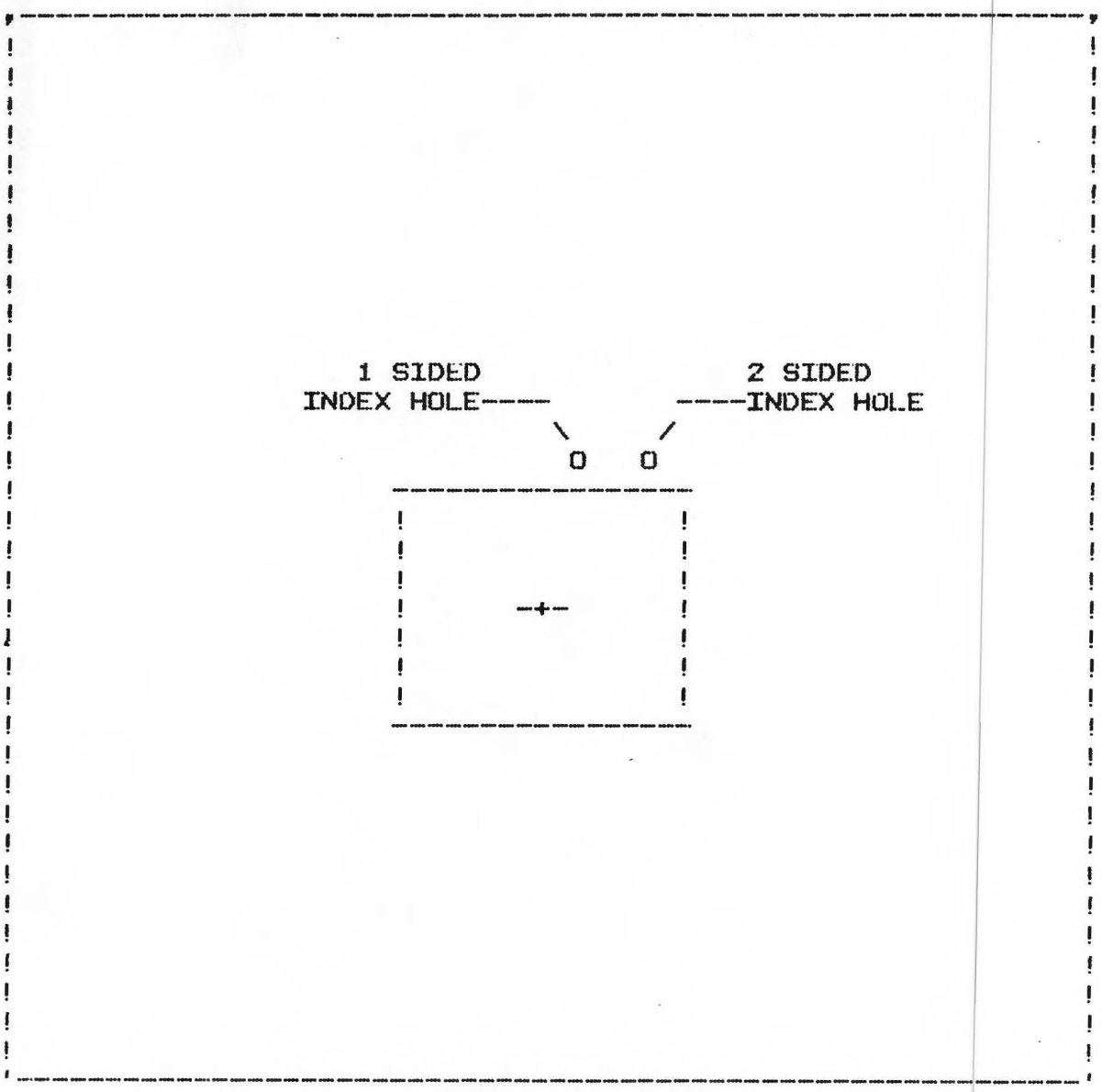

TABLE YY: DRIVE CABLE PINOUTS

PIN#	MNEUM	I/O	DESCRIPTION
2	LOWC	O	LOW WRITE CURRENT
4	XXXX	X	UNUSED
6	XXXX	X	UNUSED
8	XXXX	X	UNUSED
10	2SIDE	I	TWO SIDE STATUS
12	DCNG	I	DISC CHANGE STATUS
14	SIDE	X	SIDE SELECT
16	HL2	O	HEAD LOAD 2 (UNIT 1)
18	HL1	O	HEAD LOAD 1 (UNIT 0)
20	INDEX	I	INDEX STATUS
22	READY	I	READY STATUS
24	XXXX	X	UNUSED
26	SEL1	O	DRIVE SELECT 1 (UNIT0)
28	SEL2	O	DRIVE SELECT 2 (UNIT1)
30	SEL3	O	DRIVE SELECT 3 (UNIT0-SPECIAL)
32	SEL4	O	DRIVE SELECT 4 (UNIT1-SPECIAL)
34	DIR	O	STEP DIRECTION
36	STEP	O	STEP PULSE
38	WDAT	O	WRITE DATA
40	WG	O	WRITE DATA GATE
42	TR00	I	TRACK 00 STATUS
44	WPROT	I	WRITE PROTECT STATUS
46	RDAT	I	READ DATA
48	XXXX	X	UNUSED

ALL ODD PINS GROUNDED

ADVANCED ELECTRONIC DESIGN

FLEX02 OPERATING SYSTEM NOTES

1.0 INTRODUCTION

THIS DOCUMENT DESCRIBES OPERATION OF THE AED FLEX02 CONTROLLER UNDER THE DEC RT-11 OPERATING SYSTEM.

* NOTE: 'DEC' AND 'RT-11' ARE REGISTEED TRADE MARKS OF DIGITAL EQUIPMENT CORP. AND ARE USED IN THIS DOCUMENT WITH THAT UNDERSTANDING.

2.0 RELEVANT DOCUMENTS

DEC RX02 SYSTEMS USERS GUIDE
DEC RT11 SYSTEMS MANUALS

3.0 STANDARD RT11 RX02 OPTIONS

3.1 DOUBLE DENSITY ONLY SUPPORT: INHIBITS USE OF THE AUTOMATIC SINGLE/DOUBLE DENSITY IDENTIFICATION OF THE CURRENTLY INSTALLED DISC, IF THE OPTION IS SELECTED.

3.2 SECOND RX02 CONTROLLER SUPPORT: ALLOWS USE OF A SECOND AED FLEX02 CONTROLLER IDENTIFIED AS 'DY2:' AND 'DY3:' FOR ITS DRIVE 0 AND 1 UNITS.

3.3 CSR AND VECTOR ADDRESSES: STANDARD ADDRESSES ARE: FIRST FLEX02: CSR= 177170
VECTOR= 264
SECOND FLEX02: CSR= 177150
VECTOR= 270

4.0 EXTENDED RT11 SUPPORT: DOUBLE SIDED OPERATION

THE RT11 DY: DRIVER SOURCE CODE WILL SUPPORT DOUBLE SIDED FLEX02 OPERATION, BUT IS NOT ENABLED BY THE NORMAL SYSGEN QUESTION AND ANSWER SESSION. IN ADDITION, THE DY DRIVER AND DY BOOTSTRAP ROUTINES HAVE ERRORS IN THE SOURCE CODE SUPPORTING TWO SIDED OPERATION.

TO CORRECT THE TYPO IN RT11 V3B DY DRIVER:

```
.EDIT DY.MAC<CR>
*FDY$DS<ESC>0A<ESC><ESC>
*I.IIF NDF DY$PAT, DY$PAT=0<CR>
<ESC><ESC>
*FDBSID1<ESC>0A<ESC><ESC>
*I.IF NE DY$PAT<CR>
      DBSID2= 02    ;SIDE 2 READY<CR>
.ENDC<CR>
<ESC><ESC>
*F<CR>
30$:<ESC>V<ESC><ESC>
30$:  MOV R1,@R4
*I<CR>
.IF NE DY$PAT                                    <CR>
        MOV RXLSN,R3   ;SET R3= LSN              <CR>
        TST R1         ;SPEC FUNCT?              <CR>
        BMI 301$       ;YES                      <CR>
        CMP R3,#MAXLSN ;LSN ON SIDE 0?           <CR>
        BLT 301$       ;YES                      <CR>
        BIS #CSHEAD,R1 ;SET HEAD BEFORE OUTPUT   <CR>
301$:                                            <CR>
.ENDC                                            <CR>
<ESC><ESC>
*EX<ESC><ESC>
.
```

(NOTE: THIS CODE PATCH (A) DEFINES TERM 'DBSID2' TO BE 'HEAD READY BIT', AND (B) INSERTS CODE TO TEST AND SET/RESET THE HEAD BIT BEFORE OUTPUTTING THE HEAD BIT INTO THE CONTROLLER CSR)

TO ADD 2 SIDED OPERATION IN RT11 V3B DY BSTRAP:

```
.EDIT BSTRAP.MAC <CR>
*F.IIF NDF $DYSYS<ESC>1A<ESC><ESC>
*I.IIF NDF DY$PAT, DY$PAT=0 <CR>
.IIF NDF DY$DS, DY$DS=0      <CR>
<ESC><ESC>
*FCSDN<ESC>0A<ESC><ESC>
*I.IF NE DY$DS                                          <CR>
.IF NE DY$PAT                                           <CR>
CSHEAD  =       1000                                    <CR>
MAXLSN  =       1734*2                                  <CR>
.ENDC                                                   <CR>
.ENDC                                                   <CR>
<ESC><ESC>
*FNXT..=.<ESC>-1A<ESC><ESC>
*I.IF NE DY$DS                                          <CR>
.IF NE DY$PAT                                           <CR>
        ASL     R0      ;R0=LSN                         <CR>
1$:                                                     <CR>
        CMP     R0,#MAXLSN ;LSN ON SIDE 0? <CR>
        BLT     LSN     ;YES                            <CR>
        BIS     #CSHEAD,REDCMD ;NO,SET SIDE 1   <CR>
        SUB     #MAXLSN,R0   ;TWEEK LSN  <CR>
.ENDC                                                   <CR>
.ENDC                                                   <CR>
<ESC><ESC>
*FLSN:<ESC><ESC>
*I<CR>
.IF EQ DY$DS                                            <CR>
.IF EQ DY$PAT                                           <CR>
<ESC><ESC>
*F1$:<ESC><ESC>
*I<CR>
.ENDC                                                   <CR>
.ENDC                                                   <CR>
<ESC><ESC>
EX<ESC><ESC>
.
```

(NOTE: THIS CODE PATCH (A) DEFINES TERMS 'CSHEAD' AND 'MAXLSN', THE CSR HEAD BIT AND THE MAX LSN ON SIDE 0. IT (B) INSERTS CODE TO TEST FOR SIDE 1 ACCESSES AND SET THE HEAD BIT AND SUBTRACT SIDE 0 SECTORS FROM THE WORKING LSN).

TO ENABLE DOUBLE SIDED EXPANSION:

AFTER RUNNING SYSGEN, AND
BEFORE RUNNING @SYSBLD,

```
.EDIT SYCND.MAC<CR>
*R/A<ESC><ESC>
*I     DY$DS = 1   ;DOUBLE SIDED<CR>
       DY$PAT = 1   ;ENABLE DOUBLE SIDE PATCHES<CR>
<ESC><ESC>
*EX<ESC><ESC>
.
```

THEN RUN @SYSBLD.

NO OTHER CHANGES ARE REQUIRED TO RT11.