GP-6 ANALOG COMPUTER

OPERATOR'S MANUAL

COMDYNA, Inc.

COMPUTERS FOR DYNAMIC ANALYSIS

305 Devonshire Road, Barrington, IL 60010, tel & fax 847/381-7560

GP-6 ANALOG COMPUTER
Operators & Maintenance Manual

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GP-6 OPERATING PROCEDURES

1.0 CONNECTION OF EXTERNAL READOUT INSTRUMENTS

The GP-6 offers a choice of slow and fast time scales. Slow time outputs are normally recorded with an XY plotter or strip chart recorder; fast time outputs are normally displayed by an oscilloscope.

A time base is provided and should be used wherever possible as the X input to an XY plotter or XY oscilloscope. Use of the interal time base offers two advantages. 1. The time base is calibrated to match the integrator time scales. 2. It sweeps across a fixed range of co-ordinates regardless of the time period being plotter or displayed.
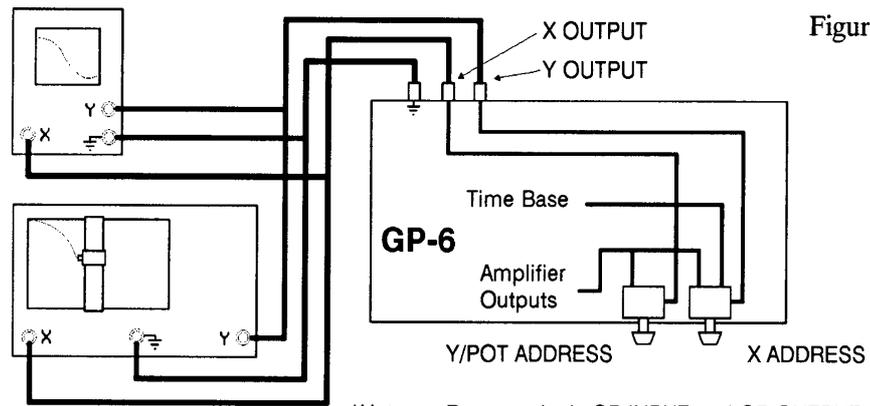
Figure 1-1

*Note: Rear terminals OP INPUT and OP OUTPUT must be connected for normal operation. (See para 1.6)

Rear binding post terminals offer convenient connections to the X and Y inputs of the plotter and/or oscilloscope. The three connections are shown in Figure 1-1 and listed below.

1. **GND**...signal ground.

2. **Y OUTPUT**...selection of the Y ADDRESS switch, to be connected as the plotter and/or oscilloscope vertical input.

3. **X OUTPUT**...selection of the X ADDRESS switch, to be connected as the horizontal input.

    Note: If the oscilloscope's internal time base and external trigger is to be used for display of high speed repetitive outputs, it will be convenient to connect its external trigger input to the OP OUTPUT rear terminal.

1.1 CALIBRATION OF READOUT INSTRUMENTS

The range and zero position of a plotter or oscilloscope should be selected and positiooned so that their full scale horizontal and vertical axes span the GP-6 minus and plus ten volts reference. (Fig. 1-2.)
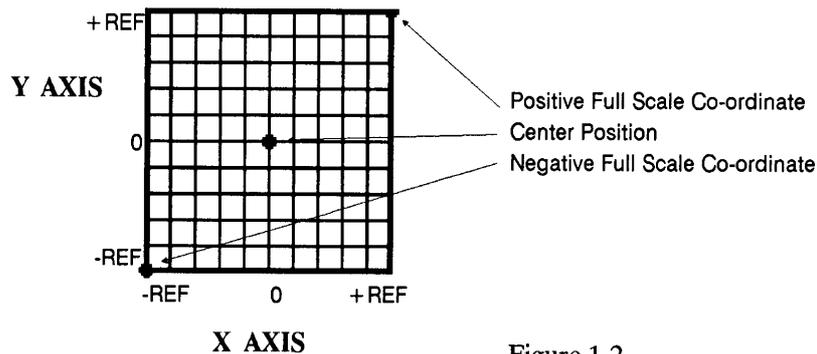
Figure 1-2

The following are procedures for input scaling adjustments:

1. Position the MODE SELECTOR switch to OPR.

2. Depress the IC mode control push button.

3. Position both the Y/POT ADDRESS and X ADDRESS switches to GND. 4. Adjust the plotter or oscilloscope X and Y zero controls until plotter's pen or oscilloscope's dot is the the graph or display center.

5. Position the Y/POT ADDRESS and X ADDRESS switches to -REF.

6. Adjust the plotter or oscilloscope X and Y gain controls until the pen or dot is the pen or dot negative full scale deflection.

7. Position the Y/POT ADDRESS and X ADDRESS switches to +REF.

8. Check the pen or dot. It should be the positive full scale deflection.

9. Repeat the procedures if necessary.

The readout instruments will either plot or display an amplifier output as a function of time or of another amplifier output, as selected by Y and X ADDRESS switch positions (para 1.5.) Regarding time functions, zero time begins at the negative full scale deflection and sweeps to positive full scale, where the positive full scale deflection equals the compute time period (para. 1.3.)

> *If the oscilloscope internal time base is used for the repetitive operation display, the fast time scale ratio of 400:1 must be considered: one computer time second equals 2.5 milliseconds real time.*

1.2 SETTING COEFFICIENT POTENTIOMETERS

Coefficients are set in a potentiometer setting mode where a setting is displayed by the digital voltmeter and a selected potentiometer is adjusted until the desired setting is observed. Setting procedures are:

1. Complete all patching so that settings are made under their operating loads. (If pots 7 and 8 are to be used as normal attenuators, check to assure that their bottom ends are patched to ground.)

2. Position the MODE SELECTOR switch to POT SET.

3. Position the Y/POT ADDRESS switch to the number of the pot to be set.

4. Adjust the pot knob until the desired setting is displayed.

1.2.1 Effects of Amplifier Overrange

An amplifier overrange will alter the setting of any pot patched to the overranged amplifier input. If the overload alarm appears when the POT SET mode is selected, remove the overrange condition by patching overranged amplifier outputs directly to their summing junctions. Be sure to remove these patch cords prior to running the program.

1.3 SETTING THE COMPUTE TIME PERIOD

The Compute Time Period is the time taken by the internal time base to sweep from minus to plus reference. It is the full scale X axis co- ordinate of plotted or displayed time response curves. It is adjustable from 10 to approximately 100 computer time seconds by the COMPUTE TIME control. Setting procedures are:

1. Position the MODE SELECTOR switch to POT SET.

2. Position the Y/POT ADDRESS switch to GND/X.

3. Position the X ADDRESS switch to CTP.

4. Adjust the COMPUTE TIME control until the desired compute time period divided by 100 is displayed. (The display for a compute time period of 20 computer time seconds will show .200)

1.4 DIGITAL VOLTMETER MEASUREMENTS OF ANALOG VARIABLES

Static conditions of analog variables may be measured as follows:

1.4.1 Measurement of Amplifier Outputs in the POT SET Mode.

1. **Position the MODE SELECTOR to the POT SET position.**
2. Position the Y/POT ADDRESS switch to GND/X.
3. Position the X ADDRESS switch to the number of the amplifier output to be measured.
4. Read the display.

1.4.2 Measurement of Amplfier Outputs in the OPR Modes.

1. Patch the Y OUTPUT rear terminal to METER INPUT.
2. Position the MODE SELECTOR to the OPR position.
3. Position the Y/POT ADDRESS switch to the number of the amplifier output to be measured.
4. Read the display.

1.4.3 Measurement of the Sum of Integrator Inputs.

1. Patch the Y OUTPUT rear terminal to METER INPUT.
2. Position the MODE SELECTOR to the OPR position.
3. Depress the IC mode control push button.
4. Patch the SJ jack of the integrator input to be measured to the SJ jack of an unused amplifier; the unused amplifier to have a 1 resistor feedback (except should an overrange result and then the feedback would be changed to .1.)
5. Follow normal procedures 1.4.2 to measure the amplifier output which is the inverted sum of the integrator inputs.

1.4.4 Measurement of External Inputs

1. Position the MODE SELECTOR to the OPR position.
2. Connect the external input to be measured to METER INPUT rear terminal.
3. Read the display.

1.5 PROBLEM SOLUTION

The typical analysis of an analog computer simulation is to evaluate the response curves of dependent variables (ampliier outputs) as functions of the independent variable (time.)

To produce time response curves:

1. Position the Y/POT ADDRESS switch to the amplifier output that is to be the curve's ordinate.
2. Position the X/ADDRESS switch to TIME, the curve's abscissa.

Oscilloscope Display:

3. Depress the RO mode control push button. (The entire response curve is displayed.)

XY Recorders:

3. Depress the IC mode control push button. (All integrators are simultaneously placed into an initial condition mode.)
4. Depress the OP push button. (All integrators are placed into an operate or run state and a plot of the response curve is drawn.)

Evaluation of Time Response Curves Based on Physical Units

Y Axis...Where zero is the center co-ordinate, the full scale co-ordinates are equated to physical units by setting them equal to the amplifier output's amplitude scale factor: the maximum estimated amplitude assigned to derive a program's scaled equations so that an output in physical units equals the voltage output times the scale factor.

X Axis...The full scale X axis co-ordinate is the compute time period in computer time units divided by the program's time scale factor.

Changing the Compute Time Period

If it is determined that the compute time period is either too long or short for convenient display or recording, the COMPUTE TIME control may be adjusted and a new compute time period established. A new compute time period does not affect the response, only the time period of the response. If a convenient readout is not obtainable with the range of compute time period selections, a new program time scale factor must be selected.

To produce dependent variables vs. dependent variable curves:

Producing curves where an amplifier output replaces time as the abcissa requires only that the X ADDRESS switch be positioned to the desired amplifier number. In such cases, zero shall be the center co-ordinate; the oscilloscope or plotter plus and minus full scale co-ordinates, like the Y axis scaling, shall be set equal to the amplifier output's amplitude scale factor.

1.6 SLAVING TWO OR UNITS TOGETHER

When problem requirements exceed the capacity of one GP-6, two or more units may be slaved into a single operating system.

1. Designate a unit to be the master; others shall then be slaves to the master.
2. Connect a common ground between units: rear terminals GND suggested.
3. On all slave units remove the shorting wire between rear terminals OP OUTPUT and OP INPUT.
4. Connect the rear terminal OP OUTPUT of the master to the OP INPUT terminals of all slave units.
5. Patch each unit and the interconnections between units.
6. Run the program from the master.

   Note: After the slaved operation has been completed, in con-sideration of the next user, replace the OP OUTPUT to OP INPUT shorting wire.

1.7 OVERRANGE

When any of the eight operational amplifiers exceed either plus or minus reference, the OVLD light will turn on. (The actual overrange threshold is normally set to about 1.05. See the 970 Overload Indiator circuit description for adjustment procedures.)

1.8 POWER

The AC power switch is a part of the COMPUTE TIME control. To turn power on, rotate the COMPUTE TIME control clockwise from the OFF position. The above located pilot light indicates a power on condition.

GP-6 OPERATOR FUNCTIONS

Figure 2-1
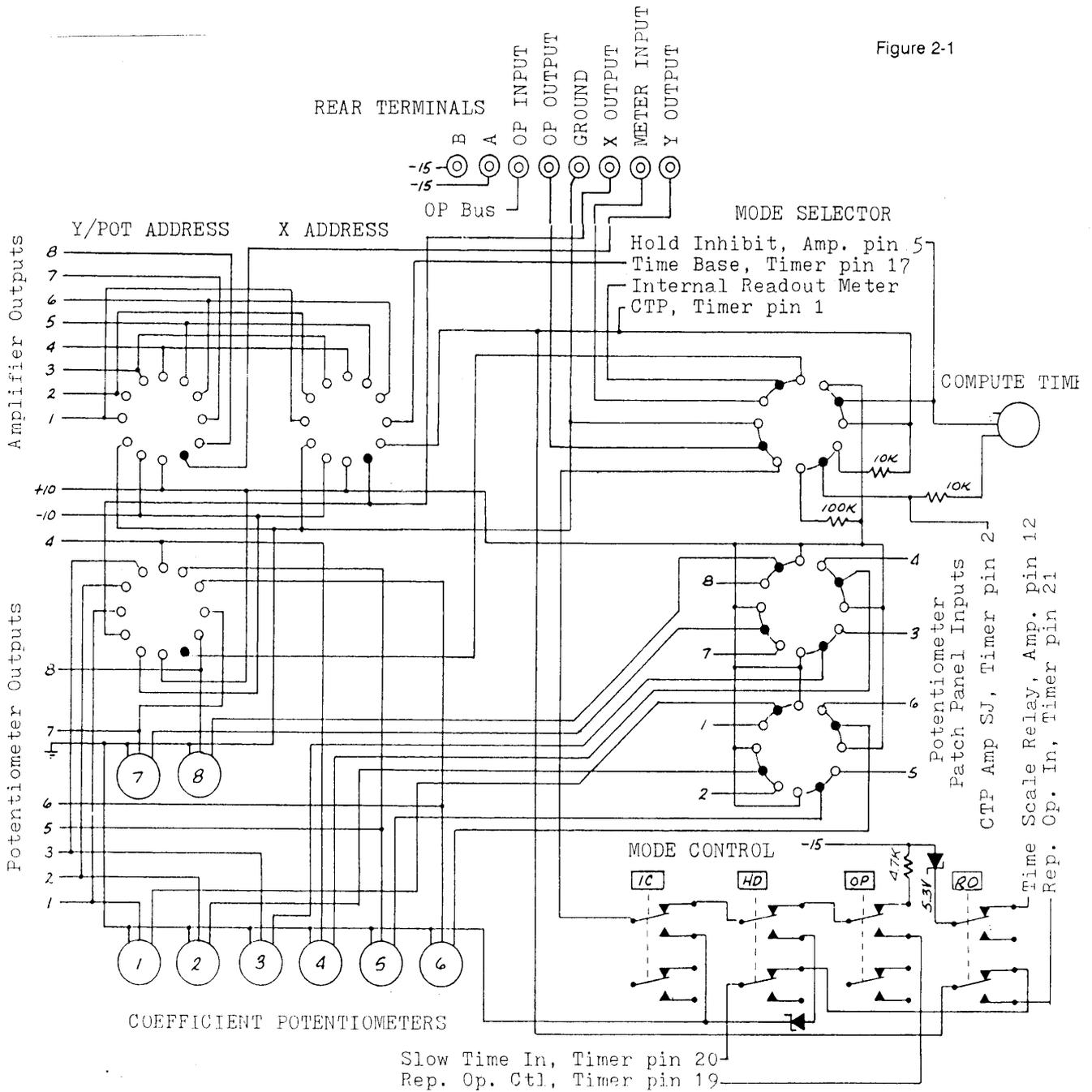
Figure 2-1 is a schematic of operator functions. Descriptions of the individual operations are described in the following:

2.1 Y/POT ADDRESS

The Y/POT ADDRESS switch is an 11 position, 2 pole rotary switch. One section selects amplifier outputs for external readout; the other section selects coefficient potentiometer outputs for setting attenuator constants. The amplifier selector wiper is connected to the rear terminal Y OUTPUT; the pot selector wiper is brought to a MODE SELECTOR switch contact to be the input to the internal digital voltmeter (DVM) when the switch is in the POT SET position. (It is noted that the GND/X position of the pot selector section is con-nected to the X ADDRESS switch wiper so that the DVM may be used to measure X ADDRESS selections while in the pot set mode.)

2.2 X ADDRESS

The X ADDRESS switch is an 11 position, 1 pole rotary switch. It selects amplifier outputs, the internal time base (TIME) and the compute time output (CTP.) Its wiper is connected to the rear terminal X OUTPUT and the GND/X position of the Y/POT ADDRESS switch, pot selector section.

2.3 MODE CONTROL

The following system integrator modes are controlled with the four mode control push buttons.

2.3.1 Initial Condition

Depression of the IC push button pulls the OP bus to ground for reset of system integrators.

2.3.2 Hold

Depression of the HD push buttons pulls the OP bus to a hold mode control voltage level (approximately -2 volts) for placement of system integrators into a hold mode condition.

2.3.3 Operate

Depression of the OP push button releases the OP bus to an operate mode control level (-5 to -15 volts) for placement of system integrators into a slow time, operate condition.

2.3.4 Repetitive Operation

Depression of the RO push button de-energizes the integrator time scale relays and connects the OP bus to the repetitive operation timing unit mode control. Integrator time constants are reduced by a factor of 400 and mode control is repetitively switched from initial condition to operate.

2.4 MODE SELECTOR

The MODE SELECTOR switch is a 2 position, 12 pole rotary switch. It selects the following functions to distinguish between the computer's POT SET and OPR modes.

2.4.1 Setting of Coefficient Potentiometers

The top end input to each coefficient potentiometer is connected to one of eight poles. In the OPR position, the poles are switched to the patch panel input; in POT SET, the poles are switch to +10 volts. Thus in the pot set mode the inputs to all potentiometers are replaced by computer reference and the potentiometer output values are measurements of the settings.

2.4.2 Internal Digital Voltmeter

One pole is connected to the DVM input. In POT SET, the pole is switched to the Y/POT ADDRESS switch wiper, pot selector section; in OPR the pole is switched to the rear terminal METER INPUT.

2.4.3 Integrator Mode Control

One pole is connected to the rear terminal OP OUTPUT. In POT SET, the pole is switched to ground; in OPR the pole is switched to the push button mode control switch selection. Thus in the pot set mode, all integrators are placed into an initial condition state; in the operate mode, all integrators are controlled by the push button selections.

2.4.4 Compute Time Period Amplifier

Two poles are used to program the CTP amplifier, shown in Figures 2-1 and 2-2. The CTP amplfier is a part of the Timer PC board assembly.
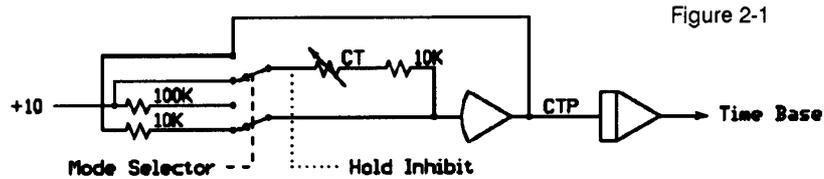
Figure 2-1

In OPR, + 10 volts is applied through the COMPUTE TIME control (100K ohms) and a series 10K ohm resistor to the CTP amplifier summing junction. A 10K ohm resistor is the feedback. Therefore:

$$CTP = -10/(CT + 10) \times 10 \text{ volts.}$$

In POT SET, + 10 volts is applied through a 100K ohm resistor to the CTP summing junction. The COMPUTE TIME control and 10K ohm resistor are the feedback. Therefore:

$$CTP = -(CT + 10)/100 \times 10 \text{ volts.}$$

The CTP amplifier output in POT SET is one tenth the reciprocal of its value in OPR. As the CTP output is the input to the time base integrator, its reciprocal is an indicator of the compute time period.

2.4.5 Hold Inhibit

One pole is connected to the integrator hold inhibit control. In the normal integrator initial condition mode, the hold switch is shut off, thereby isolating the input resistor network. As poten-itometers must be set with their resistor loads, it is necessary to disable the hold switches during the pot set mode. In POT SET, the pole is switched to a positive voltage and all integrator hold switches are held in an "on" condition; in OPR the pole is switched negative and all integrator all allowed to function under normal hold mode control.

2.5 COMPUTE TIME

The COMPUTE TIME control is a combination 100K ohm variable resistor and off-on switch. While in the operate mode the variable resistor is the CTP amplifier input. The CTP amplifier is scaled so that the COMPUTE TIME control adjusts its output within a range of -10 volts to -1 volt. The time base integrator is scaled so that a -10 volt input produces a compute time period of 10 computer seconds; a -1 volt input produces 100 seconds.

The off-on switch is the primary AC power switch.

2.6 COEFFICIENT POTENTIOMETERS

The coefficient potentiometers are ten turn, 5K ohm variable resistors. Pots 1 - 6 are arranged as attenuators with their bottom ends grounded; pots 7 & 8 have their bottom ends terminated at the patch panel.

2.7 OVERLOAD INDICATORS

The OVLD lamp is a light alarm that indicates when one or more of the eight patch panel amplifier outputs exceed either a positive or negative 10 volts reference.

2.8 DIGITAL VOLTMETER

The DVM includes the features of 3 1/2 digits display, 10 volts full scale and autopolarity. Its decimal is positioned so that 10 volts appears as unity (1.000: a conformance to normallized or dimensionaless amplitude scaling.

2.9 REAR TERMINALS

The following is a wiring list for the rear binding post terminals

Terminal	Color	Description
0	Red	-15 volts.
1	Green	+15 volts.
OP OUTPUT	Red	Integrator mode control output.
OP INPUT	Green	Integrator mode control input, connected to the patch panel OP jacks and the time base integrator control. For normal operation a jumper wire connects OP OUTPUT to OP INPUT.
X OUTPUT	Red	Output of the X ADDRESS switch.
GND	Black	Signal Ground.
Y OUTPUT	Red	Output of the Y/POT ADDRESS switch amplifier selector section.
METER INPUT	Green	Input to the DVM when the the MODE SELECTOR switch is in the OPR position.

2.10 INTERFACE CONNECTOR

The interface connector is located below the rear terminals. From looking inside the chassis, the pin terminations are as follows:

1. -15V
2. +15V
3. +10V
4. -10V
5. Analog Ground
6. nc.
7. OP Bus Output
8. OP Bus Input
9. Time Scale Relay Bus
10. nc.
11. nc.
12. Digital Ground
13. Vcc (+5V)
14. nc
15. nc
16. nc.
17. nc
18. Amplifier #1.
19. Amplifier #2.
20. Amplfier #3.
21. Amplifier #4.
22. Amplifier #5.
23. Amplifier #6.
24. Amplifier #7.
25. Amplifier #8

3. GP-6 PATCH PANEL

REFERENCE

COEFFICIENT POTENTIOMETERS
1 2 3 4 5 6

7 8

SW OP SW OP X Y MULTIPLIERS X Y SW OP SW OP

Patch panel graphics use standard analog computer programming symbols. Amplifiers 1 thru 4 are single ended, high gain amplifiers with electronic mode switches and summing resistor/integrating capacitor networks that may be programmed as summer/inverters, integrators, track/store and single pole, double throw electronic switch amplifiers. Amplifiers 4 and 5 are summer/inverters. Amplifiers 7 and 8 are inverters only. Potentiometers 1 thru 6 are grounded attenuators. Potentiometers 7 and 8 have their bottom ends open and may be used as either voltage dividers or attenuators. Multiplier networks produce current outputs for direct connection to amplifier summing junctions, and thus may be patched as multipliers, dividers, squarers and square root extractors.

The following is an explanation of patch panel symbols:

SYMBOL	COLOR CODE	DESCRIPTION
+	Red	Positive reference, considered unity (1.000) for normalized programming. (Actual amplitude is 10 volts.)
—	Yellow	Negative reference.
(5)		High gain operational amplifier.
(3)		High gain operational amplifier with electronic switch.
(7)		Inverter.
⊢	Red	Amplifier output.
SJ	Gray	The summing junctions for amplifiers 1 - 6. (Active for amplifiers 1 - 4 when a logic "1" is patched to the SW switch control jack or when there is no switch control patching.)

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| SYMBOL	COLOR CODE	DESCRIPTION
SJ′	Gray	Alternate summing junction for amplifiers 1 - 4. (Conducting when a logic "0" is patched to the SW switch control jack.)
1 —W—	Green	Standard input summing resistor, normalized as a unity value to simplify programming. (Actual resistance is 50K ohms.)
.1 —W—	Green	Summing resistor input one tenth the standard value. (Actual resistance is 5K ohms.)
⊣⊢ B	Green	One end of standard integrating capacitor, normalized so that the "1" resistor and B capacitor combine to produce a one second time constant, as referred to programming time scales. (Actual capacitance is 20 ufd for the slow and .05 ufd for the fast time scales.
⊣⊢.1B	Green	Integrating capacitor that has a value one tenth the standard B capacitor. (Actual capacitance is 2 ufd for the slow and .005 ufd for the fast time scales.)
SJ′ —W— IC	Green	Resistor network for the SJ′ summing junction. Amplifier becomes an inverter when SJ′ is conducting. Normally used for integrator initial conditions. May also be used as the feedback and input with the SJ summing netwokr. (See Summer patching.)
	Yellow	Attenuator: bottom end grounded; top end input and wiper output brought out to the panel -- wiper indicated by the arrow.
	Yellow	Voltage divider: top and bottom end inputs and wiper brought out to the panel -- wiper indicated by the arrow.
	Black	System ground.
		Multiplier network symbol.
X	Brown	One of two multiplier inputs.
Y	Brown	One of two multiplier inputs.
Y	Gray	Multiplier output, a current proportional to the product of "X" and "Y;" normalized so that when connected to the summing junction of an operational amplifier with a "1" resistor feedback, and with reference patched as both inputs, the amplifier output equals reference.
SW	White	Electronic switch control. Logic 0 (ground or positive voltage,) SJ′ conducts, SJ shuts off. Logic 1 (-5V or less,) SJ conducts and SJ′ shuts off. Hold logic (-2V thru -3V) SJ′ shuts off and the summer resistor network is disconnected electronically from the amplifier/capacitor feedback.
OP	White	Computer's operate bus, integrator mode logic from the central operpush button control, patched to "SW' for normal integrator operation.

PATCH PANEL OPERATIONS

FUNCTION	OPERATION	PATCHING
SUMMER (amplifiers 1 - 4)	**Fundamental Summer Operation** $E_O = -R_f(E_1/R_1 + E_2/R_2 \ldots + E_n/R_n)$ $E_O = -(A + B + 10C + 10D)$ NO PATCHING TO SWITCH CONTROL "SW"	
SUMMER (amplifiers 1-4 using IC networks)	$E_O = -(A + B + C)$ NO PATCHING TO SWITCH CONTROL "SW"	
SUMMER (amplifiers 5 & 6)	$E_O = -(.1A + .1B + .1C)$	
INVERTER (amplifiers 7 & 8)	$E_O = -A$	

FUNCTION	OPERATION	PATCHING
INTEGRATOR (amplifiers 1 - 4)	**Fundamental Integrator Operation** $E_O = -R_f \int (E_1/R_1 + E_2/R_2 \ldots + E_n/R_n) dt - Eic$ $E_O = -\int (A + C + D + 10E + 10F) dt - A$	
ATTENUATOR (pots 1-6)	 $E_O = K(A)$	
ATTENUATOR (pots 7 & 8)	 $E_O = K(A)$	
VOLTAGE DIVIDER (pots 7 & 8)	 $E_O = K(A - B) + B$	
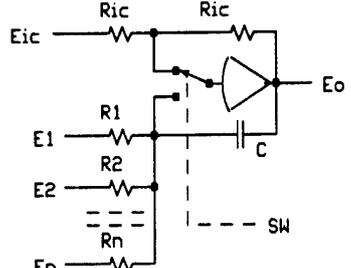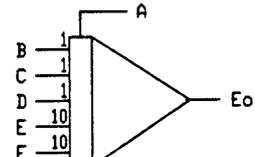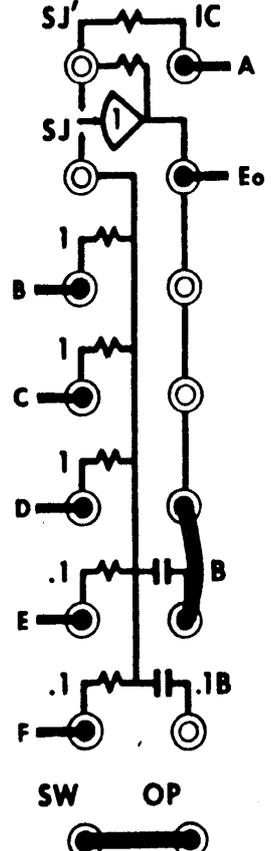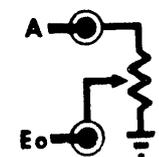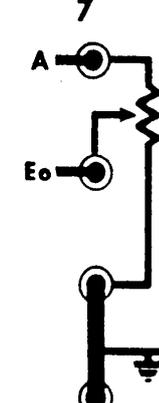
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FUNCTION	OPERATION	PATCHING
MULTIPLIER	**Fundamental Multiplier Operation** $E_O = -(EX * EY)$ $E_O = -(A * B)$	
DIVIDER	 $E_O = -(A/B) \quad B > 0$	
SQUARER	 $E_O = -A^2$	
SQUARE ROOT	 $E_O = -A^{1/2} \quad A < 0$	

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FUNCTION	OPERATION	PATCHING
DIFFERENTIATOR (amplifiers 1 - 4)	**Fundamental Differentiator Operation** $E_O = - d\text{Ein}/dt$ $E_O = - dA/dt$ NO SWITCH CONTROL PATCHING	
TRACK/STORE (amplifiers 1 - 4)	$Eo' = - A$ when Q is a logic 0. $Eo' = - A$ when Q is a logic 1. A' is the stored value of A when Q switches from 0 to 1. $Eo = A'(n-1)$ when Q is a logic 0. $Eo = A'(n)$ when Q is a logic 1 and next logic 0.	
DPDT **Electronic Switch** (amplifiers 1 - 4)	$Eo = - E1$ when Q is a logic 0. $Eo = - (Rf/Rin)E2$ when Q is a logic 1.	
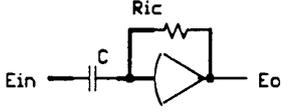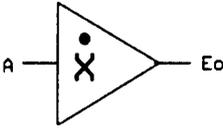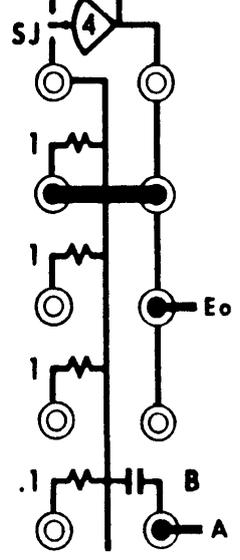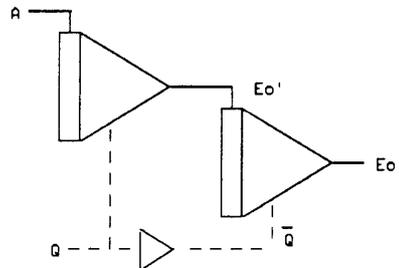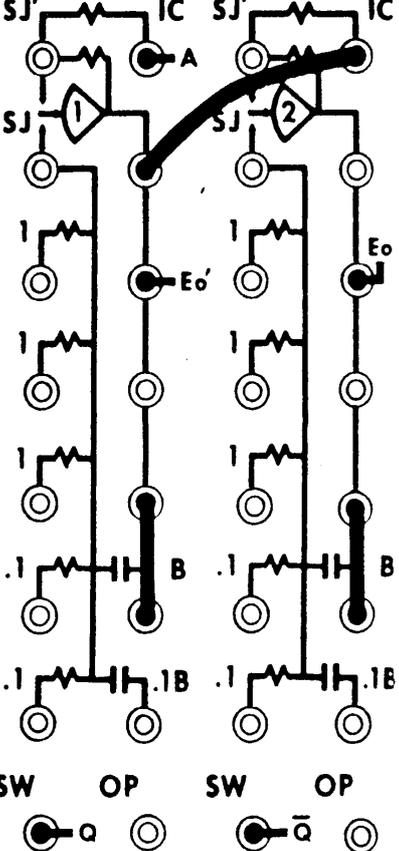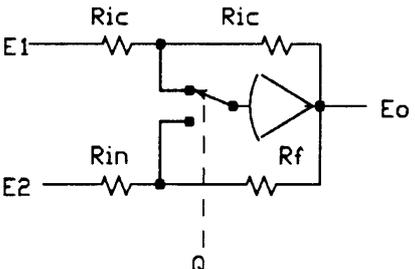
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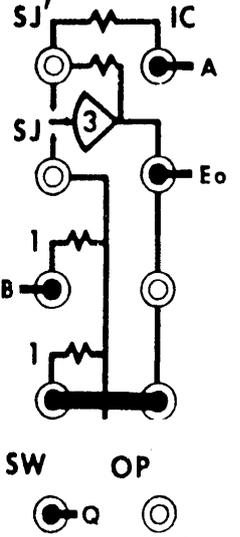
CIRCUIT DIAGRAMS

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GP-6 SYSTEM LAYOUT

Below is a layout of GP-6 assembliles. Please refer to Section 2 for a wiring schemataic and description of system operating functions. Refer to individual drawings for information covering assemblies.
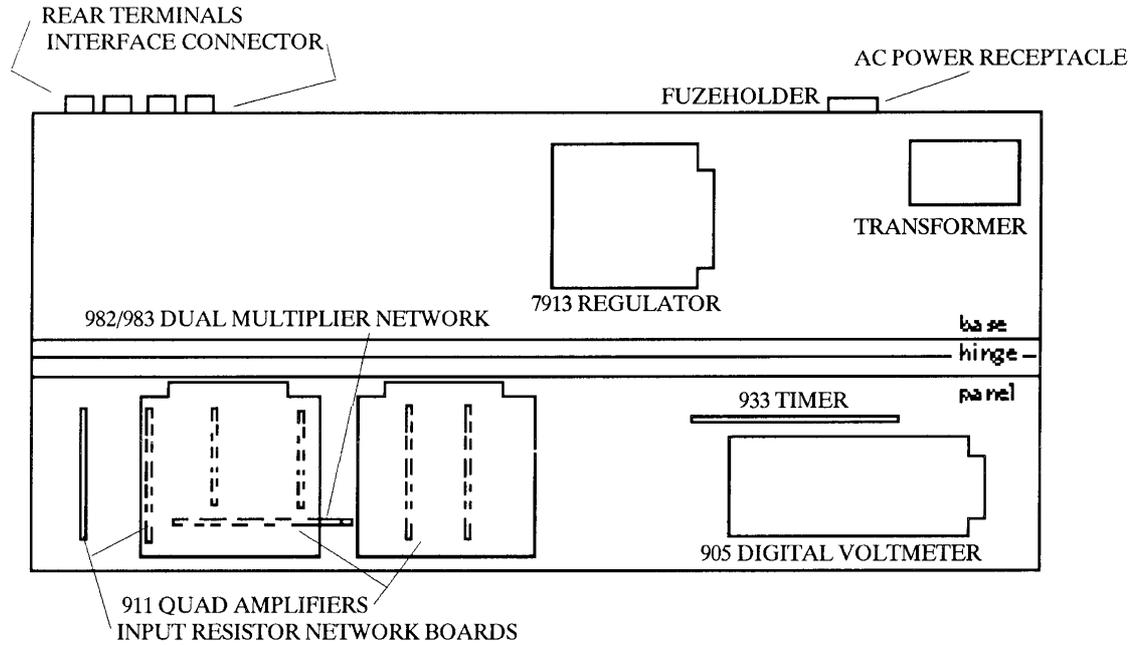
Input summing resistors for integrator and summer amplifiers are located on the **Input Resistor Network Boards**. Resistors are 5.00Kand 50.0K, metal film, 0.1%.

Color coding of power wiring is: **+15V** *Red*; **-15V** *White;* **-10V** *Yellow;* **+10V** *Orange;* **Ground** *Black*.

The following is a parts list for the GP-6 system. Component parts lists are found within individual assembly drawings.

| DESCRIPTION	MANUFACTURE	PART NUMBER
Patch panel jacks	E.F. Johnson	108-09xx-001
Rear terminals	E.F. Johnson	111-01xx-001
Y/Pot Address Switch	Centralab	PA-1005
X Address Switch	Centralab	PA-1001
Mode Control Switch	Centralab	PA-1029
Mode Control Switch	Switchcraft	65041K-206
Pilot Light	Leecraft	36EN2111
Overload Indicator	Leecraft	45-RNG 3-2111
Coefficient Pot entiometer	C.T.S.	VA 45D
Compute Time/Power Switch	C.T.S	GC-45-8D
AC Power Receptacle	Belden	17253
Fuzeholder	Littlefuze	372001
Fuze, AC power	Littlefuze	8 AG 1 amp
Amplifier Connectors	Amphenol	143-022-01
Regulator Connector	Amphenol	143-018-01
DVM and Mult Connectors	Amphenol	143-010-01
Transformer	Proprietary	

7913.1 REGULATOR

The 7913 assembly rectifies/filters from the 28 VCT secondary to produce an unregulated +UN and -UN outputs, which are also regulated as plus/minus 15 volts, precision plus/minus 10 volts reference and Vcc (plus 5 volts.)

Positive refernce is produced by ua723 regulator I4. Negative reference is inverted positive reference. Lamp L1 offers negative reference output protection.

Reference Adjustments

1. Adjust potentiometer P1 until the positive reference equals +10.000 volts.

2. Adjust potentiometer P2 until negative reference equals the inverted positive refernce.

Schematic
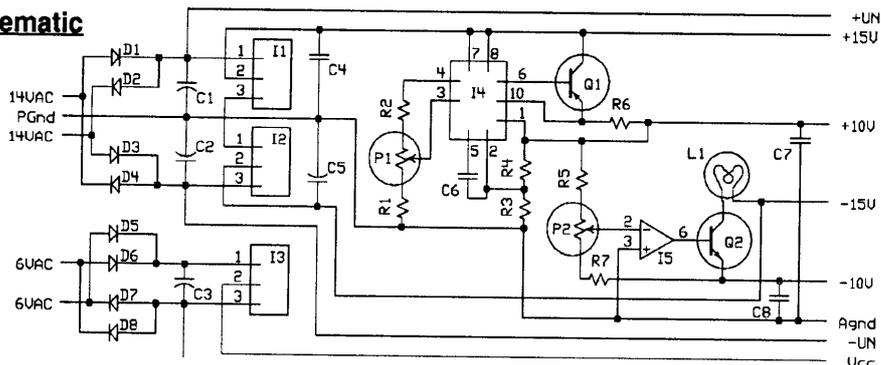
Assembly Drawing

Parts List

R6	10	ohm	
R2	2.32	K#*	
R3	2.43	K#	
R5,R7	4.99	K#	
R1	6.04	K#	
R4	9.76	K#	
L1	12V .04A	INC	
P1,P2	50	ohm	
C1,C2,C3	2200	ufd	elec
C4	.1	ufd	cer
C5	1	ufd	tant
C6	100	pfd	cer
C8	.01	ufd	cer
D1 - D8	1N4001		
Q1	2N4124		
Q2	2N4403		
I1	ua7815		
I2	ua7915		
I3	ua7805		
I4	ua723		
I5	Mc1741CG		
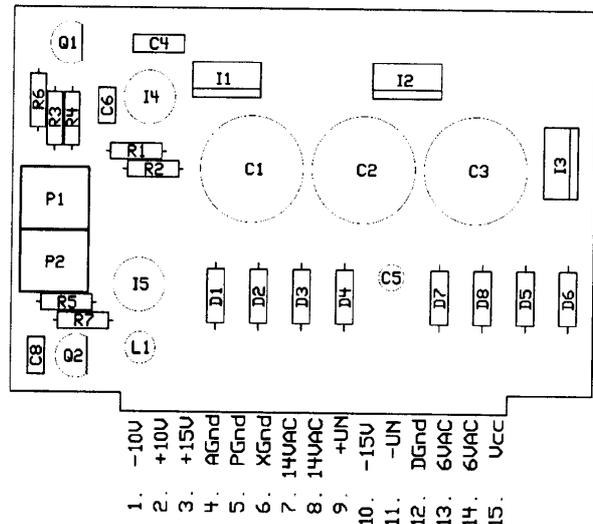
NOTES: #metal film resistor

*value may be altered

Rectifier diodes D1 - D4 may be 2N5401 for high current applications.

911-4 QUAD AMPLIFIER ASSEMBLY

The 911 board provides two single input, high gain operational amplifiers and two high gain operational amplifiers with electronic switch/integrator networks.

Amplifiers A and D are the single input amplifiers. Their patch panel summing junctions are connected directly to the interting bases. Back-to-back diodes D2 and D3 offer protection by limiting summing junction potential. Capacitor C1 reduces peaking.

Amplifiers B and C are single input amplifiers with electronic switch/integrator networks. The electronic switches create two summing junctions, SJ and SJ'. When the switch control input (OP) is a logic 0 (ground or positive) summing junction SJ' conducts; when a logic 1 (more negative than -5 volts) summing junction SJ conducts.

The integrating capacitors are connected to the SJ summing junction so that an integrator is programmed by patching an amplifier output to a capacitor input. Two capacitor inputs (B and .1B) offer 10:1 time scale selection. The Time Scale Relay switches the time scale change (400:1) that is required for high speed repetitive operation. Where the repetitive operation feature is provided, the repetitive operation capacitors are connected directly to SJ. When the relay is energized, slow time capacitors are switched parallel the repetitive operation capacitors. (The relay is energized when an approximate negative 10 volts, not negative reference, is applied to the relay control input.)

Signal switching is performed by N-channel FET transistors Q6 thru Q8. Bipolar transistors Q1 thru Q5 are the FET switch drivers. Q6 is the Hold FET (its an on resistance is less than 30 ohms to minimize summing errors.) Voltage divider resistors R8 and R12 are selected so that when OP is between -1 to -3 volts, Q6 shuts off; when OP is more negative Q6 turns on. Q7 is the shunt switch, Q8 is the SJ series switch and Q9 is the SJ' series switch. Table 5-1 shows the switch states for the OP logic control voltage levels. N-channel FETs conduct with a zero gate voltage and shut off with approximately -7 volts. Back-to-back diodes D4 and D5 limit the SJ' potential when Q9 is off. Diodes D2 and D3 provide summing junction protection. D1 allows the Hold Inhibit control to override Q1 and turn Q6 on. (Hold Inhibit logic is applied in the Pot Set Mode to ground SJ summing junctions that would otherwise be floating.)

Capacitors C7 and resistors R13 provide amplifier compensation. Capacitorss C1 reduces peaking when SJ has a resistor feedback. A similar capacitor is provided the SJ' summing jucntion.

BALANCING

To balance amplifiers A and D, patch resistor feedbacks and adjust potentiometers PA and PD until each amplifier output is a zero potential.

Amplifiers B and C should be balanced when programmed as integrators. Adjust PB and BC until each integrator produces a minimum integrator drift.

Assembly Drawing
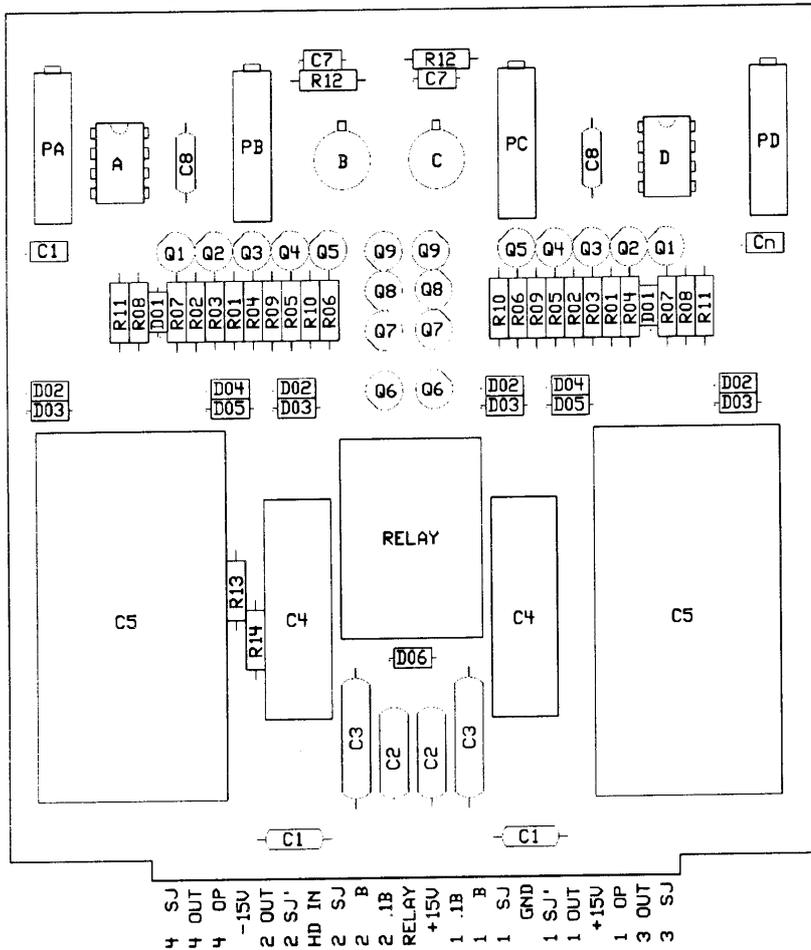
Parts List

R12	. . . . .	1	K
R14	. . . . .	2.2	K
R2 - R7	. . . .	15	K
R1,R14	. . . .	27	K
R8 - R10	. . .	47	K
R11	. . . . .	330	K
PA - PD	. . . .	10	K
C1	. . . . . .	15	pf
C2	. . . . . .	.005	uf
C3	. . . . . .	.05	uf
C4	. . . . . .	2	uf
C5	. . . . . .	20	uf
C6	. . . . . .	0.1	uf
C7	. . . . . .	500	pf
Q1 - Q5	. . . .	2n4403	
Q6	. . . . .	2N4091	
Q7 - Q9	. . . .	2N5485	
Amplifiers A,D		UA741CJG	
Amplifiers B,C		LH0042CH	
Relay	. . . . .	4A, 24V	

Table 5-1

OP LOGIC	Q6	Q7	Q8	Q9
OP > 0	OFF	ON	OFF	ON
-1V > OP > -3V	OFF	ON	OFF	ON
OP < -5V	ON	OFF	ON	OFF

Circuit Diagram

COMDYNA, INC.
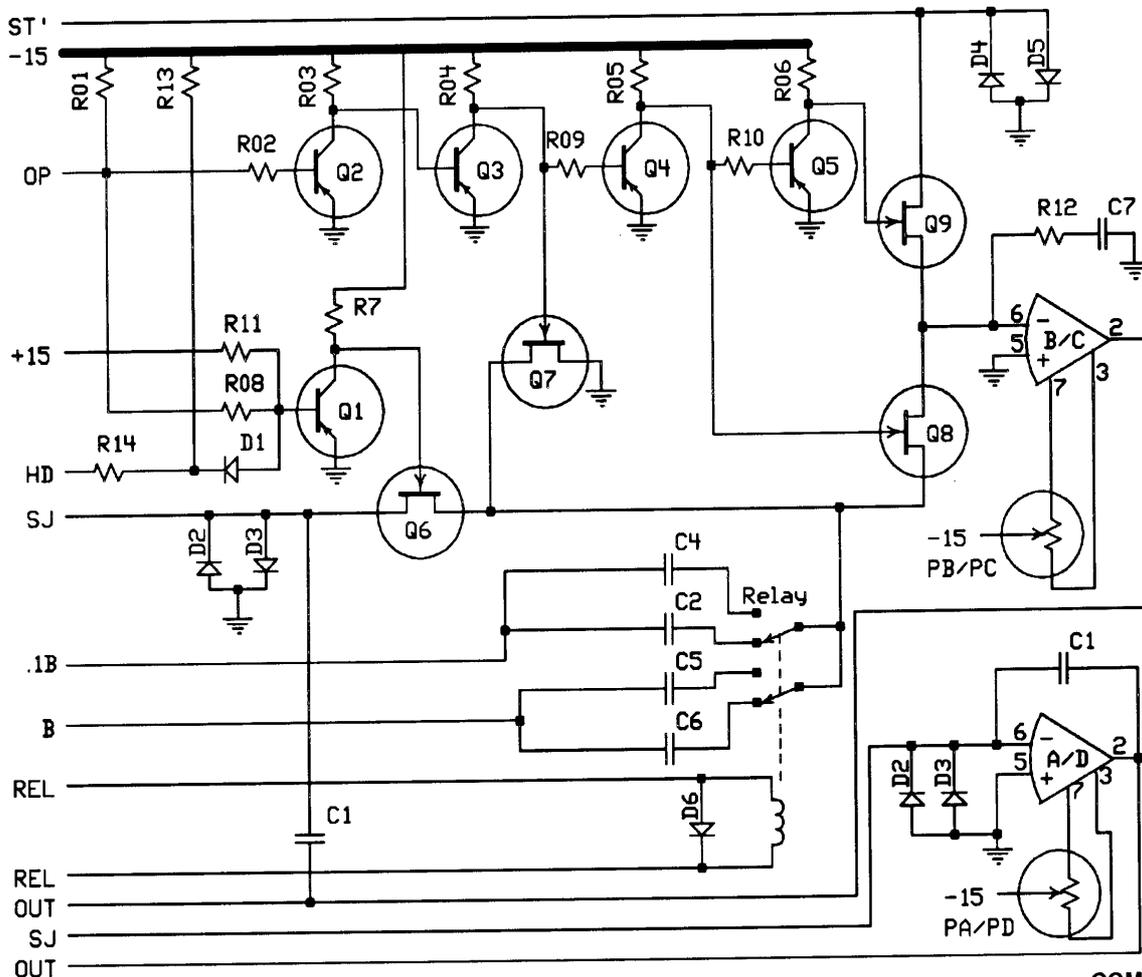
933.4 MODE CONTROL AND TIME BASE ASSEMBLY

Mode control is a push button, four stage, two pole, double throw interlocked switch. Each station places a system into one of four integrator modes:

Initial Condition (IC)

Hold (HD)

Operate (OP)

Repetitive Operation (RO)

To produce the above modes, it is necessary to control the OP Bus voltage (mode logic,) the Time Scale Relay Bus (slow or fast integrator time scales,) and the repetitive operation timing circuit (slow or fast time base ramp.)

Referring to the circuit diagram, the following is a description of the four modes:

Initial Condition... Time Scale Relay Bus energized (see Repetitive Operation.) The OP Bus pulled to ground.

Hold... Time Scale Relay Bus energized. The OP Bus pulled to the hold voltage state (approximately -1.7v.) Input to the time base integrator disconnected (see Time Base Circuits.)

Operate... Time Scale Relay Bus energized. The OP Bus released to the operate voltage state (less than -5v.)

Repetitive Operation... Time Scale Relay Bus de-energized. The OP Bus switched from the slow time modes (IC, HD, OP) to the repetitive operation logic.

Time Base Circuits... The time base integrator (amplifier B) provides both the slow and high speed repetitive operation time bases, both linear sweeps from negative to positive 10v reference. The input originates from amplifier A which is externally programmed to provide an adjustable voltage in the range of -1v to -10v. (A 1 volt input produces a compute time period of 100 sec; a -10v input produces 10 sec. The time base integrator circuit is the same as that of the 911 general purpose integrator. Please see the 911 data sheet for the circuit descriptionc.) When OP is depressed, the output of A is directed through the HD switch to R22 to produce an integration rate of 2 volts/sec; when RO is depressed the input is R23 and the rate is 800 volts/sec. Also, when RO is depressed the monostable circuit of amplifiers C and D becomes the OP Bus and thus the repetitive operation mode control, (the time constant of C4-R18 producing an initial condition state of approximately 2 milliseconds.)

Capacitors C1 and C2 with resistors R1 and R2 decouple amplifiers C and D to eliminate power supply disturbance.

For the amplifier A Compute Time Period programming, please refer to section 2.0 of the GP-6 operator's manual.

Adjustments

Slow time and repetitive operation time base rates are adjusted with potentiometers P1 and P2. Both are adjusted to match patch panel integrator time constants.

Program a patch panel amplifier as an integrator. Apply positive reference as an initial condition. Patch negative reference to a coefficient potentiometer and patch the wiper to a gain 1 input. Set the potentiometer to .200. The integrator will then sweep from negative to positive reference in a 10 unit (second) period.

Slow Time Adjustment... Observe (with an XY recorder or oscilloscope) the slow time output of the patch panel integrator as a function of the time base. Adjusts potentiometer P1 until the function passes through the positive reference-positive reference coordinate (+ 10, + 10.)

Repetitive Operation Adjustment... Repeat the above procedure observing the entire integrator output on the X-Y oscilloscope. Adjust potentiometer P2 until the oscilloscope trace passes through the + 10, + 10 coordinate.

Assembly Drawing

OP out
A SJ
A out
RAMP
+15U
−15U
OP in
+10U
GND
Relay

R01
R02
C1
C2
A/B
C3
R11
R15
Q5
R07
R09
R06
R08
R05
R21
R04
R03
C/D
Q6
D01
D02
Q7
R23
R22
R10
Q4
Q3
Q2
Q1
R19
R20
R18
C4
C5
R17
P2
P1
ZH
R01
ZR

IC   HD   OP   RO

Parts List

R1,2	100	ohm	
R17	1	K	
R20,24	4.7	K	
R15,16	10.0	K*	
R4-7	15	K	
R21	27	K	
R3,8,9,19	47	K	
R10	100	K	
R18	330	K	
R22	1.0	K*	
P2	5	K	
P1	50	K	
C1,2	33	ufd	electrolytic
C3	1	ufd	polycarbonate
C4	.022	ufd	mylar
C5	3500	pf	mylar
D1,2	1N4148		
ZH	1N4370		
ZR	1N5231		
Q1-4	2N4403		
Q5-7	2N5485		
A/D	TL082CP		
C/D	Mc1458		

Schematic

IC   HD   OP   RO

OP Out

RELAY

Zh   R24

Zr

−15U

R21   R04   R05   R06   R07

R03   Q1   R08   Q2   Q3   R09   Q4

OP IN

A Out
A SJ
A

P1   R23

R10   R22

Q6   Q7   R15   +10U

P2   Q5   C3   D1   D2

B   R16   R19   R20   R18   C   R17   D   C4

+15U   R01   +15U'   −15U   R02   −15U'

C1   C2

RAMP
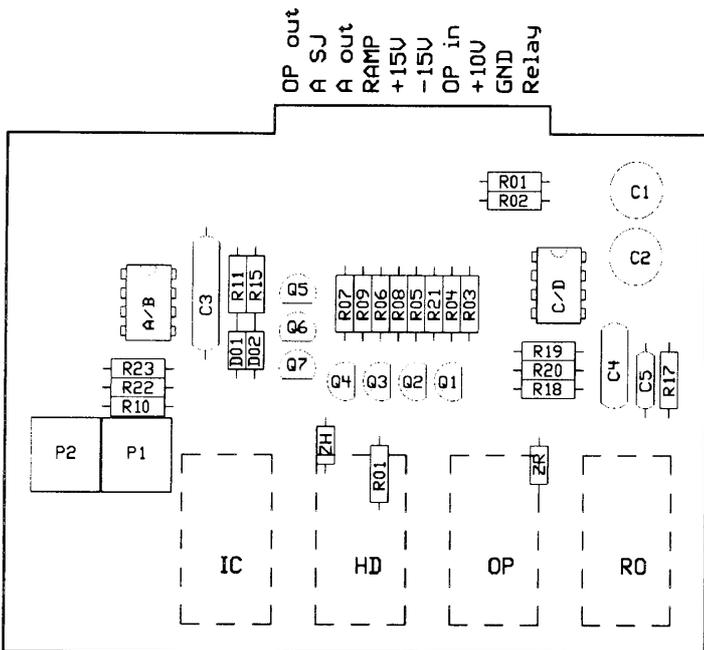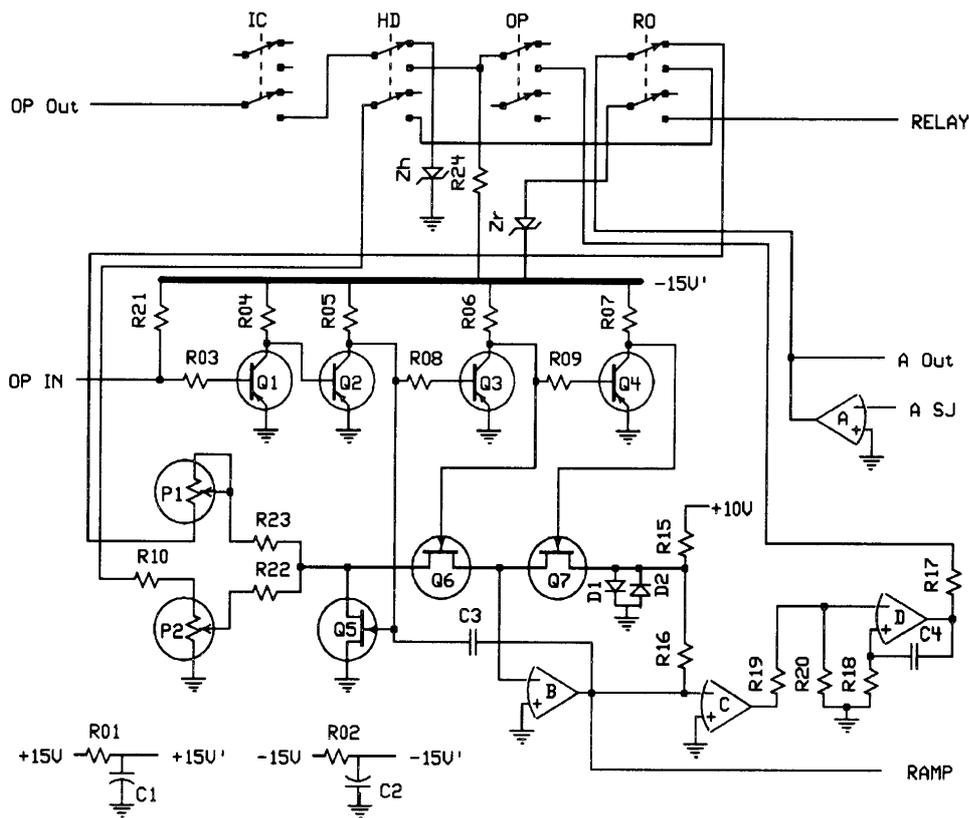
970-1 OVERLOAD INDICATOR

A lamp driver conducts when any of eight amplifier output exceeds a preset positive or negative voltage.

With negative overrange, Q1 shuts off and Q2 conducts. With positive overrange, Q3 conducts, pulling Q2 on. The lamp is pulled to ground or on when Q6 conducts. Resistor R5, capacitor C1 and transistor Q4 provide a temporary latch so that momentary overrange may be overserved with the lamp alarm.

Adjustments

Adjustments are to turn the lamp alarm on at an approximate 10.5 volts, 0.5 volts overrange. Patch to be +10.5 volts. Adjust potentiometer P2 until the lamp indicator is on. Invert the output to -10.5 volts. Adjust P1 until the lamp tunrs on.

Schematic
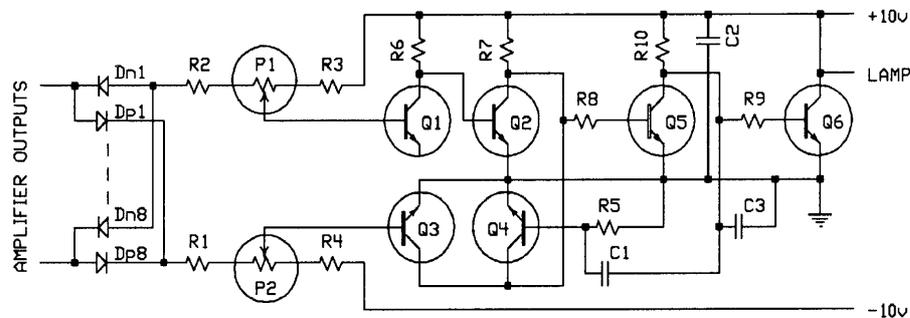
Assembly Drawing
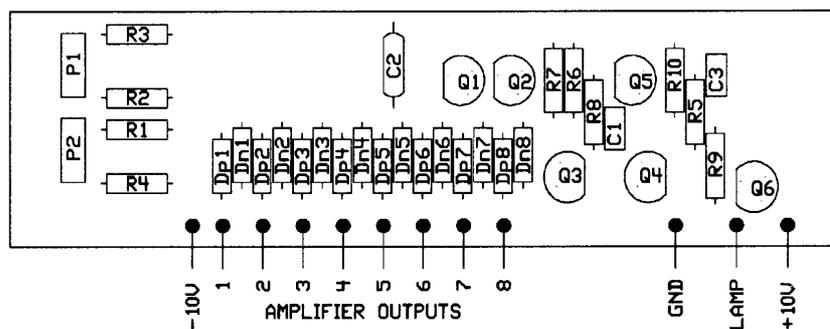
Parts List

R8, R9	4.7	K
R1 - R4, R6, R7, R10	15	K
R5	27	K
P1, P2	5	K
C1	6.8	ufd
C2	0.1	ufd
C3	0.01	ufd
Q1 - Q5	.2N4124	
Q6	.MPSA13	
Diodes	.1N4148	

982/983 DUAL MULTIPLIER NETWORKS

The 982.2/983 board assemblies provide two independent multiplier networks, configured so that each, when used with an external operational amplifier may be programmed as a multiplier, divider, squarer or square root extractor.

Two inputs (Xin and Yin) are multiplied by integrated circuit M to produce a voltage proportional to the product X*Y. The voltage is converted to a current by resistor R5, scaled so that when connected to the summing junction of a patch panel amplifier, and where the feedback is a standard *gain 1* 50K ohm resistor, the amplifier will produce a full scale 10 volts output with 10 volts as the X and Y inputs.

Adjustments

Each network is orginally adjusted at the factory. The networks should, however, be checked and readjusted, if necessary, during the initial checkout. Thereafter, the networks should be periodically checked to assure their most accurate operation. About 10 to 20 minutes should be allowed for warm-up before adjusting.

Adjustment consists of zero offset balancing (model 783 only) and a trim for gain and linearity. The suggested procedures are as follows:

1. Program the network as a multiplier.
2. With inputs X and Y patched to ground, adjust potentiometer Pz for a zero output. *Disregard for the 982.2 network.*
3. Program an integrator as a ramp function to sweep from minus to plus 10 volts reference. (For convenience make all adjustments in the repetitive operation mode.) Display the multiplier output vs. the ramp input. Patch the ramp to the Y input; the X input should remain patched to ground. Adjust potentiometer Px until a best zero curve is obtained.
4. Reverse the X and Y inputs. Adjust potentiometer Py until a best zero error is obtained.
5. Readjust Pz if necessary.
6. Patch Reference (+ or -) to the X input and the ramp to the Y input. Sum the product with the correct polarity of the ramp to display an error curve. Adjust potentiometer Pg until a best error curve is obtained. Reverse the X and Y inputs, recheck and readjust if necessary. Check the error curve with the opposite polarity Reference input and reverse inputs as done with the original polarity. Trim potentiometer Pg until a best compromise of error curves is obtained for all four input combinations.

982.2 DUAL MULTIPLIER NETWORK

Assembly Drawing
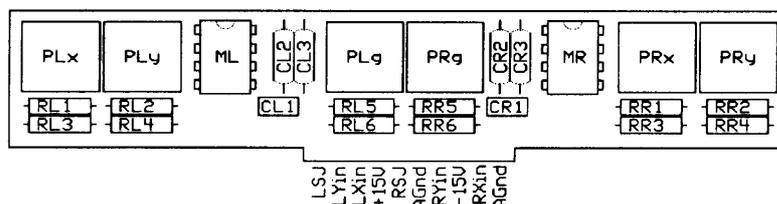
Schematic
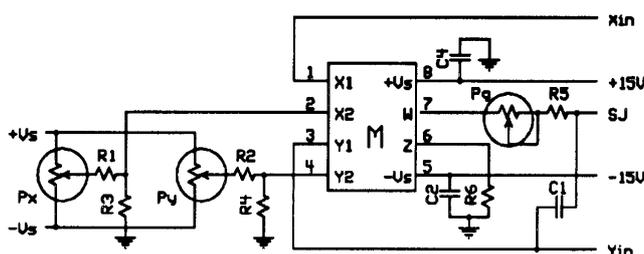
Parts List

|		
R6	100	
R3, R4	1	K
R5	49.9	K
R1, R3	330	K
Px, Py	50	K
Pg	500	
C1	33	pf
C2, C3	.1	uf
M	AD633JN	

905.4 DIGITAL VOLTMETER

The 905 assembly is a digital voltmeter that functions as a rationeter of input voltage signals to an input voltage reference. For analog computer applicaitons, the scale 1.000 reading is a unity ratio of a 10 volts input:10 volts reference.

All active circuitry is contained within the intersil 7107 component. For a description of the circuit, please refer to Intersil data sheet 11-77-00B.

Adjustment

The single adjustment should be made so that the display shows +1.000 when the input is +10 volts reference.

Assembly Drawing

| 1. | Gnd |
2.	-15V
3.	nc
4.	HGnd
5.	IN
6.	nc
7.	nc
8.	+10V
9.	Vcc
10.	nc

Schematic

Digital Segments
N   - units
N' - tens
N" - 100's
N"' - 1000's
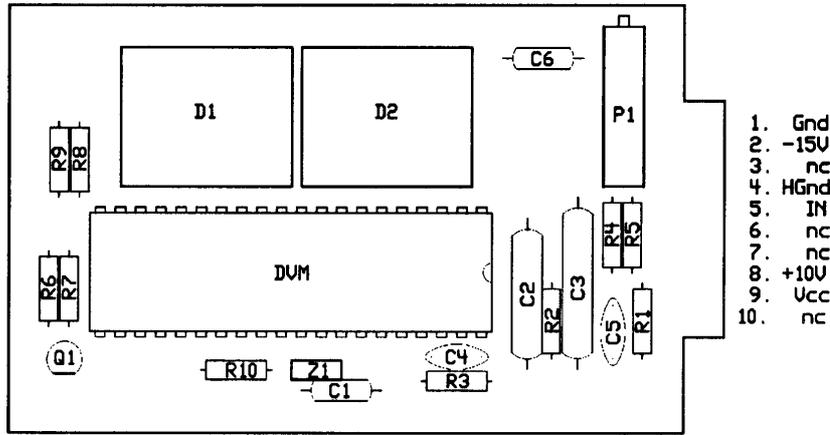
Parts List

R7-9	180	
R10	4.7	K
R6	47	K
R2	47	K
R1	49.9	K*
R3	100	K
R4	100	K*
R5	1	M*
P1	10	K
C4	100	pfd
C5	.01	ufd
C1,C6	.1	ufd
C3	.22	ufd
C2	.47	ufd
Z1	1N5231	
Q1	2N4124	
DVM	ICL7107CPL	
D1	MAN6730	
D2	MAN6710	

*1% metal film resistor

SCALING REVIEW

The following is offered as a review of analog computer programming magnitude and time scaling.

EXAMPLE DIFFERENTIAL EQUATION

$$A\,d^2X/dt^2 + B\,dX/dt + C\,X = f(t)$$
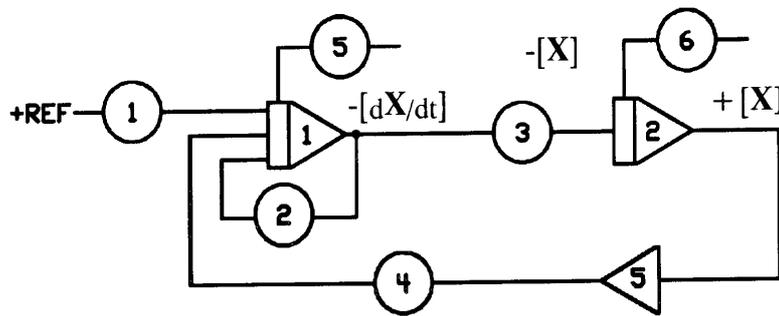
program schematic

Given:

A = .0005

B = (arbitrary)

C = 800

f(t) = .5

Estimated maximum values:

$X_{max.}$	=	.01	X_{scaled}	= [X/.01]
$dX/dt\ max.$	=	4	$dX/dt\ scaled$	= [dX/dt/4]

Rewritten and scaled:

$$[d^2X/dt^2/4] = -\frac{B}{A\beta}[dX/dt/4] - \frac{C}{A\beta} \times \frac{.01}{4}[X/.01] + \frac{1}{A\beta}[f(t)/4]$$

β = time scale factor

Potentiometer Settings

No.	Parameter	magnitude scale factor	w/o time scale	w/time scale, $\beta = 500$
1.	f(t)/A	1/4	$.25 \times 10^4/\beta$	.500
2.	**B/A**	1	$2B \times 10^4/\beta$	**40B**
3.	dX_{sf}/X_{sf}	4/.01	$.4 \times 10^4/\beta$	.800
4.	C/A	.01/4	$.16 \times 10^4/\beta$	.320
5.	dX_o/dt	1/4	$dX_o/dt/4$	$dX_o/dt/4$
6.	X_o	1/.01	$X_o/.01$	$X_o/.01$