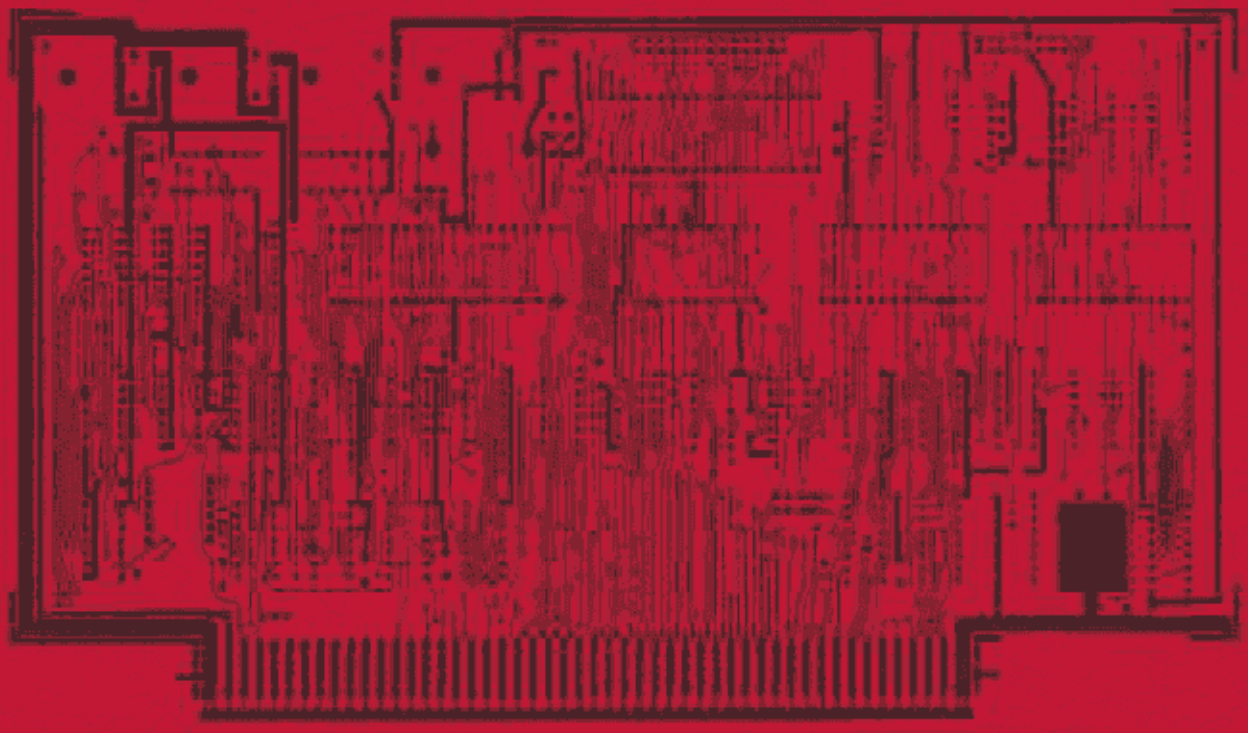
XOR-CPU
OPERATION MANUAL



- 2 – 4 MHz JUMPER SELECT
- POWER ON JUMP TO EPROM
- 2 SERIAL, 3 PARALLEL PORTS
- MEMORY MANAGEMENT ON A16 & A17
- M1 WAIT STATE OPTION
- INDEPENDENT BAUD RATES 50 to 19,200

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GENERAL DESCRIPTION

The XOR CPU was developed in 1977 and since then has undergone numerous design changes to take advantage of advancements in technology, and to conform to the IEEE 696 S-100 standards.

A typical personal or business computer can be configured with only three boards and a mainframe power supply.

1. XOR CPU
   - Z80A 4 Mhz processor
   - 2 Serial RS-232 I/O ports 8251
   - 3 8 Bit parallel I/O ports 8255
   - On board 2716 monitor prom
   - M1 wait state generation
   - Memory management on A16-A17
   - The 8251's have been upgraded to 2716/2732
   - Z80 DART/SIO
   - Board can now be used as a network slave or master.
   - Pull up resistors are now installed on DTR, CTS lines on the A and B RS232 adapter cards.

2. XOR DSK
   - WD 1795 Controller chip set
   - Single Density IBM 3740
   - XOR Double Density 8 in
   - Concurrent 8 in and 5 in operation

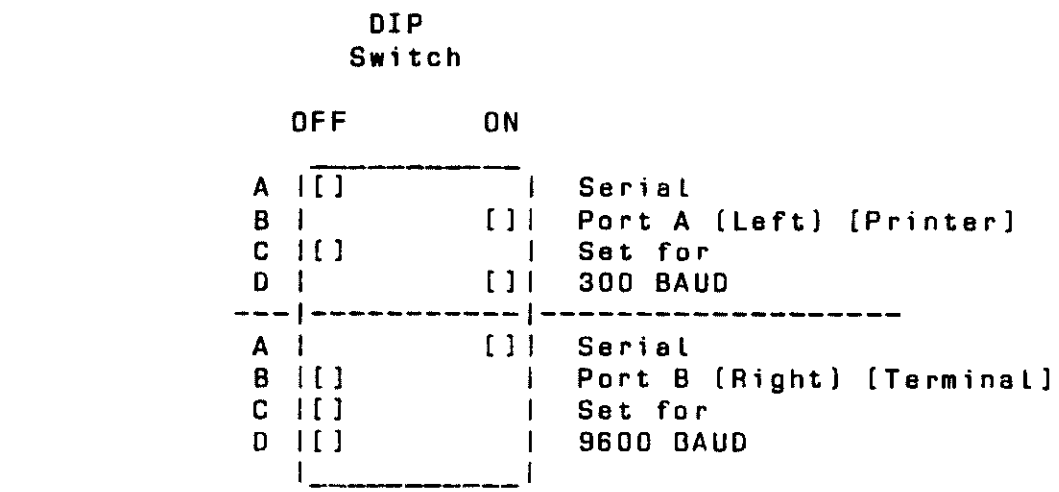
3. XOR 64K Dynamic Ram
   - Featuring 4116 250ns

SERIAL I/O BAUD RATE SELECT

CPU DIP SWITCH

The 8 position DIP switch at the lower right hand corner of the board is broken into two 4 bit sections. The upper 4 bits select the IO baud for the left 8251 and the lower 4 bits select the baud for the right. We connect the left 8251 to the "A" paddle card and the right one to the "B" paddle card. The paddle cards are mounted to the rear panel and make strapping adjustments easier. The "A" port is committed in the CP/M bios software to the printer, and the "B" port to the CRT Terminal.

The switches are used in a binary pattern to set the rates as follows:



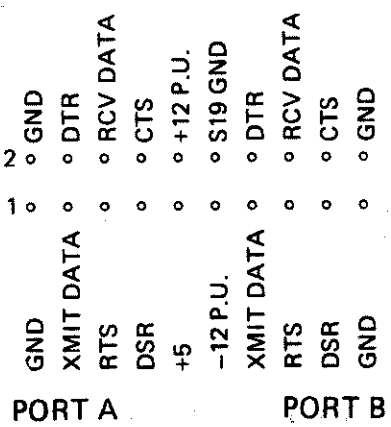
X = O F F O = O N

Baud	D	C	B	A		Baud	D	C	B	A	
50	O	O	O	O	(00H)	1200	O	X	X	X	(07H)
75	O	O	O	X	(01H)	1800	X	O	O	O	(08H)
110	O	O	X	O	(02H)	2000	X	O	O	X	(09H)
134.5	O	O	X	X	(03H)	2400	X	O	X	O	(0AH)
150	O	X	O	O	(04H)	3600	X	O	X	X	(0BH)
300	O	X	O	X	(05H)	4800	X	X	O	O	(0CH)
600	O	X	X	O	(06H)	7200	X	X	O	X	(0DH)
						9600	X	X	X	O	(0EH)
						19200	X	X	X	X	(0FH)

N O T E :
Make sure when using the above chart that the positions we show correspond to the type of switch you have on the board. Different manufacturers have the "ON" position on differents sides of the switch.

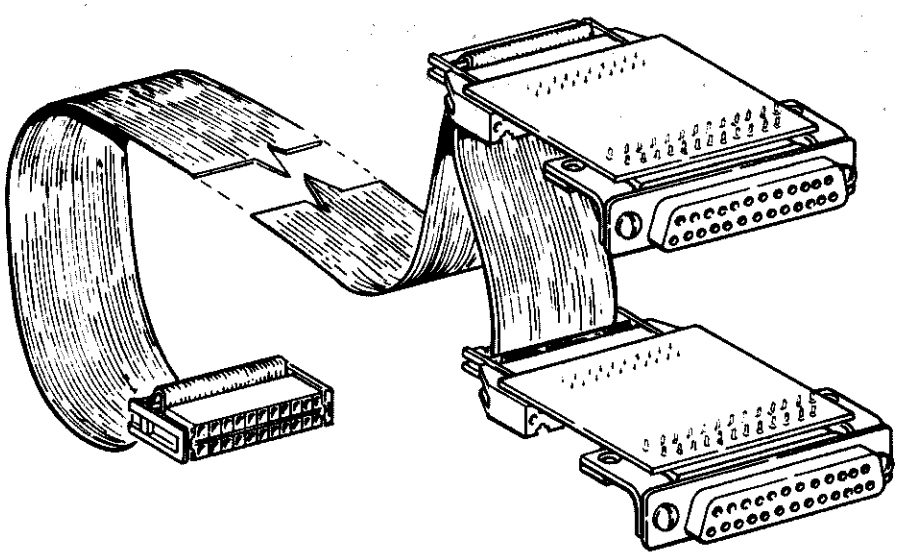
PIN OUT OF SERIAL CONNECTOR

The pin out of the RS-232 connector is as follows:



As an option we can supply a 26 pin ribbon connector with two connectors on one end and one on the other. When mated with a pair of our A and B paddle cards a neat interface to a standard RS-232 connector (chassis mount) may be realized. The cable assembly looks like this.

This cable is is available from your nearest U.S. MICRO SALES office, under stock # C-6000-16.



PARALLEL INTERFACE AND PIN OUT

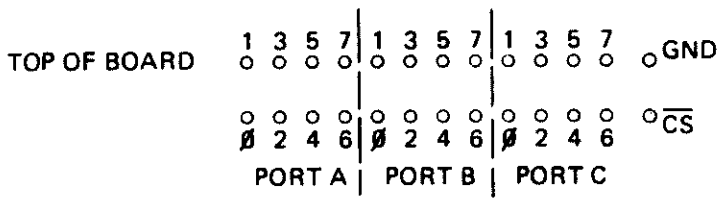
PORT ADDRESSES

The port addresses for the parallel port are as follows:

Port A=04H
Port B=05H
Port C=06H
CMD =07H

PARALLEL 8255 PIN OUT

The Parallel 8255 pin out is as follows:



8255 CHIP

The 8255 chip tech sheet can be found in the appendix.

The chip is programmable in so many configurations that it is not possible to offer an adequate operational guide. Basically the device has three 8 bit ports, A, B,and C. A can be simultaneously input and output. B can be commanded to be an input or an output. C can be part in and part out, or linked with A & B (4 bits each) for handshaking. We have included in the pinout the CS (chip select) line to the 8255. It may have some use in certain applications where buffers are remotely attached to the fairly weak output of the device.

PARALLEL PRINTER DRIVERS

Three methods may be used to "turn on" this driver. As shipped the bios drives the serial port "A" on the CPU with all CP/M list outputs. To switch all output to the parallel port on a temporary basis you can set a byte in memory at EE33H to a 05H. This can be done with DDT or BASIC with "POKE" instruction. This memory can be calculated for different system sizes by picking up the the bios jump table and can be calculated for different system sizes by picking up the warm boot entry address at memory location 1 and 2, and adding 30H to that address. (30H = 48 decimal)

A second method, which is permanent for the disk that the change was made on and all copies of that disk is to use the system utility DDUMP.COM to modify the byte on the system tracks of the floppy. You will find the bios jump table on track 1 sector 20.

```
DDUMP <CR>              (OPERATOR INPUT)
*                       (PROGRAM RESPONSE)
T 1 S 20 EDIT <CR>      (OPERATOR INPUT)
- EDIT                  (PROGRAM RESPONSE)
33 <CR>                 (OPERATOR INPUT)
0033 00                 (PROGRAM RESPONSE)
05 <CR>                 (OPERATOR INPUT)
. <CR>                  (OPERATOR INPUT) TERMINATES EDIT
WRITE <CR>              (OPERATOR INPUT) WRITES YOUR EDIT TO DISK
^C                      (OPERATOR INPUT) RETURNS TO CP/M
```

A third method is to use a text editor to modify the bios source code module IO.ASM which contains the bios jump table. You will need the Digital Research MAC assembler to do this. It may be purchased from your closest U S MICRO SALES OFFICE.

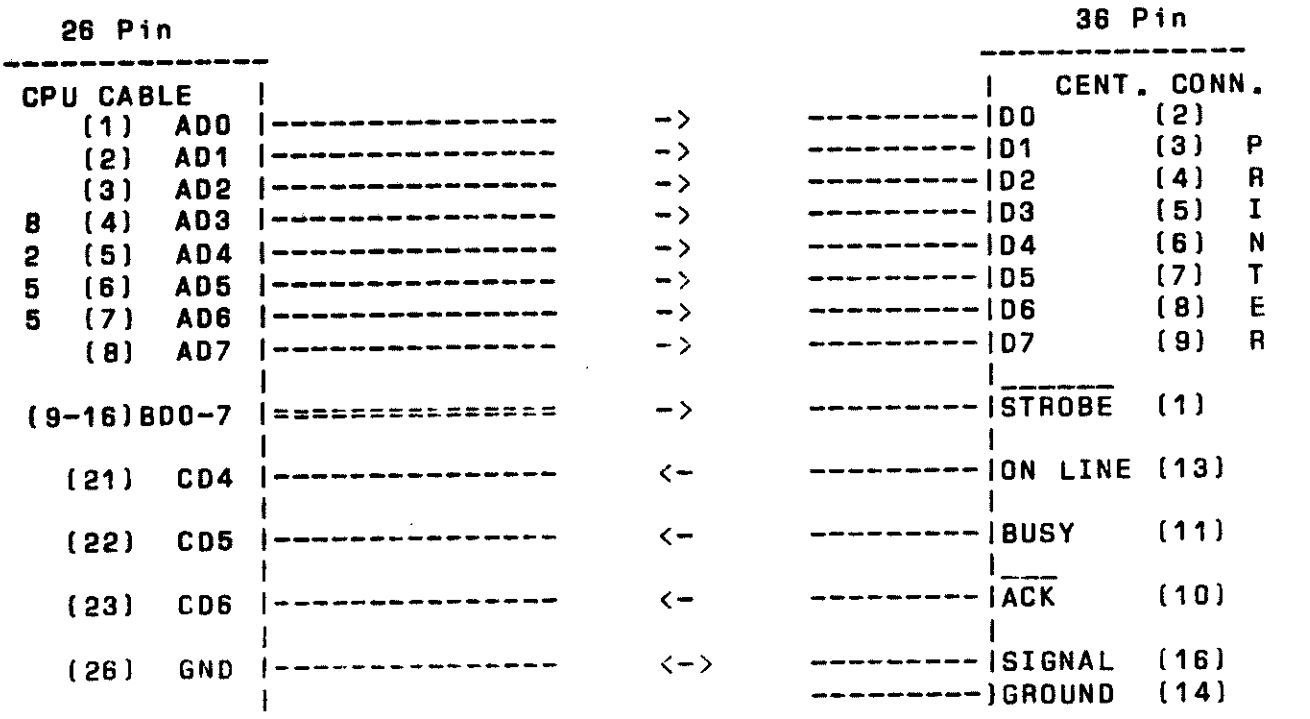
Obviously if you should want to switch back to serial output, the same byte should be set to a "0".

Note that a complex printer driver option has been supplied in the form of CXLST.ASM and its associated PRINTER.COM. CXLST may require modification to get your printer to work properly. In the command submit file BLKSYS61.SUB, several modules are concat-enated by PIP.COM to assemble the system bios. If you plan on changing anything, just tackle the module you need and generate a whole new bios by doing another submit. Up to six printer drivers can be resident in the bios at one time using CXLST.

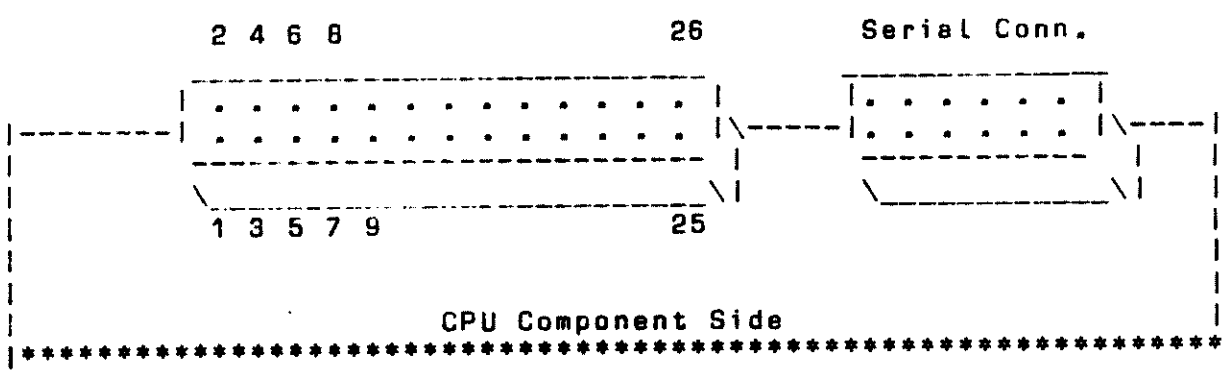
PARALLEL CABLE WIRING

This cable is used for Centronics interface printers. It uses a 8255, PA0-7 are used for data transfer, PB0-7 are tied together for data strobe PC6 for ACK from printer.

NOTE: This cable is available from your U S MICRO SALES SALES OFFICE.



CPU 8255 connector pinout looking from front with edge connector at bottom.



JUMPER OPTIONS

Part location diagrams showing locations of jumpers and a more complete definition of options follows this section.

J1 WAIT/NO WAIT

The wait/no wait jumper j1 is located above the Z80 CPU and is to the left.

J2 2 OR 4 MHZ SELECT

The XOR CPU can run at either 2 or 4 Mhz. The speed is selected by jumper j2. The jumper is located between the two I/O port connectors and is the jumper to the left.

Note: The clock signal that appears on the bus is always 2 Mhz regardless of the speed at which the CPU is operating.

J4-5 EPROM SELECT

To select an Eprom move both jumpers J4 and J5 to the upper position for a 2716 and to the lower position for a 2708. These jumpers are located near the top of the board to the left of the 8255 (REV B CPU). With the REV C CPU the upper jumper is the 2716 and the lower position is the 2732.

J6 E PROM DISABLE

Jumper J6 when placed in the left position will permanently disable the E prom. When enabled the Prom may be used exactly as it has been in the past. It is located above the Z80 CPU and is the jumper to the right. (CPU B only)

J7 I/O PORT ADDRESSES

The I/O ports will be addressed at ports 0-F when jumper J7 is in the right hand position, and 10H to 1FH when the jumper is in the left hand position. It is located between the two I/O port connectors at the top of the board and is the jumper to the left.

J8 MEMORY WRITE

Jumper J8 is memory write and is normally jumpered. To operate with an IMSAI type front panel it must be removed. It is located between two ic's near the bottom of the board.

J9 POWER ON JUMPER DISABLE

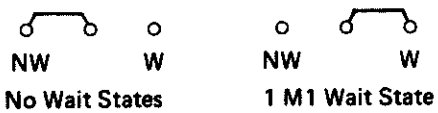
Jumper J9 when placed in the up position will cause the Z-80 to jump to system RAM after a reset. It is located close to the bottom of the board next to the two resistors.

VECTOR INTERRUPT RESPONSE and CTC CHIP

A header at the top of the board connects the various interrupt and timing capabilities of the Zilog CTC Timer chip to their chosen destinations.(The CTC Chip is an option available from your nearest U.S. Micro Sales, sales office.)

WAIT STATE ON M1 CIRCUIT

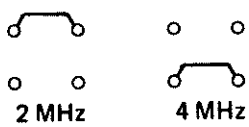
Jumper J1 allows the user to insert 0 or 1 wait state to each instruction fetch (M1) cycle. J1 is located above the Z80 CPU and is to the left.



To get the best system performance at a low cost, it is highly advisable to run the CPU at 4 Mhz with no wait state.

2 OR 4 MHZ SELECT

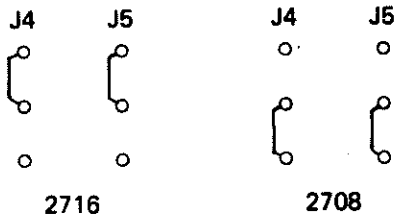
The XOR CPU can run at either 2 or 4 Mhz. The speed is selected by jumper j2. The jumper is located between the two I/O port connectors and is the jumper to the right.



Note: The clock signal that appears on the bus is always 2 Mhz regardless of the speed at which the CPU is operating.

2716 TO 2708 EPROM SELECT (REV B)
2716 TO 2732 EPROM SELECT (REV C)

The XOR CPU B is designed for use with either a 2708 or a 5V only type 2716 (Intel/Mostek), selected by J4, J5.



The Eprom always occupies F800 to FFFF, when enabled whether a 2708 or a 2716 is used.

If it is desired the XOR CPU can be modified for use with the TI 2716 (+5, -5, +12V). The 2708/2716 jumpers should be in the 2708 position. Pins 18 and 20 are affected. Pin 18 is PD/PGM on the 5 V part and CS on the TI part. Pin 20 is CS on the 5 V part and A10 on the TI 2716. Therefore the following changes must be made on IC 8B. (CPU B only)

The XOR CPU C is designed for use with either 2716 or 2732, selected by J4-J5. (See Jumper Options) 2732 starts at F000.

From Pin	To Pin	
IC 8B 18	GND	Cut these traces at IC 8B
IC 8B 20	CS	
IC 8B 18	IC 9C p6	Install these jumpers on the back of the board
IC 8B 20	IC 5B p40	

VECTORED INTERRUPT RESPONSE

The Z-80 has three methods of responding to an interrupt. The XOR CPU supports all three modes. They are : Mode 0, an instruction can be placed on the bus; Mode 1, restart to 0038H; Mode 2, upon initialization an upper page vector is loaded into the Z-80 I register. At interrupt response time, Z-80 will respond with an M1 +IOREQ (an impossible normal combination). At this time the lower page address (which will be added to the upper page previously stored in I register) should appear on the data bus. The Z-80 will use these two bytes to point to a software address where the address of the interrupt routine is to be found.

POWER ON JUMP CIRCUIT

THE XOR CPU has an unusual and totally effective method of starting a computer after a reset. Conceptually the 2708 or 2716 EPROM appears at 0000H for the purpose of initializing the CPU. The EPROM may then be 'moved' to the last 2K of RAM and jumped to. What happens is the CPU executes a few instructions at 0000H, and jumps to itself at 62K. It then does a 'read' of an I/O port which changes the on-board addressing structure. After inputing port 0A the EPROM may only be read at F800, not every 2k boundary as was the case before.

The EPROM may be left in the computer memory space at 62K at all times or removed by writing a 01H into I/O port 9. Writing a 00 into I/O Port 9 will bring it back. RAM and EPROM may exist simultaneously at either the initial 0000 reset location or at the subsequentli directed F800 location. Memory writes or I/O functions are not disturbed by the co-existence of the EPROM only memory reads. By writing the correct code into Port 9, the EPROM may be toggled in and out disabling the ability to read from adjacent RAM.

To disable the Power on Jump to EPROM:

Cut the trace from IC 13C pin 13 to IC 10C pin 11, and install a jumper from pin 13 IC 13 to ground. With this modification, the EPROM can still be accessed normally from F800 to FFFF Hex, and it can also be enabled through I/O port 0A hex. The above applies only to CPU B.

MEMORY MANAGEMENT CIRCUIT

Memory Management Lines A16 and A17.

The IEEE S-100 standard has assigned bus lines 16 and 17 to be extended address bits A16 and A17 respectively. The XOR CPU has on board I/O latches decoded to enable setting these lines to activate parallel banks of memory.

The XOR 64K Dynamic memory board will respond to this type of memory management scheme to allow up to 256K of memory to exist on any given S-100 bus with no conflict.

To set or reset the address lines A16 and A17 simply output the desired bit pattern on I/O port 08H. Bit 0 controls A16 and bit 1 controls A17 and bits 2 through 7 are ignored.

Example: To select the lowest 64K block of memory,

```
MVI A,00H
OUT 08H      A16=0, A17=0
```

to select the highest 64K block of memory,

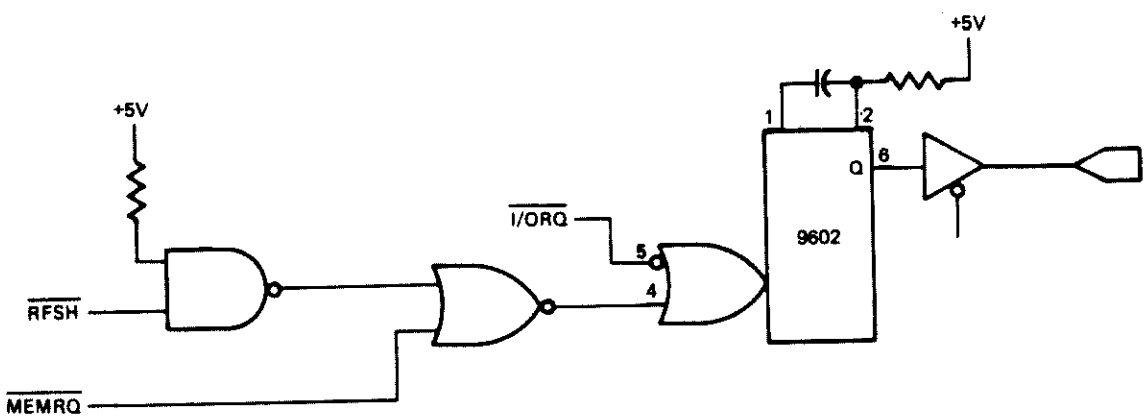
```
MVI A,03H
OUT 08H      A16=1, A17=1
```

Note: A16 & A17 must be initialized in software to the desired levels after each system reset.

P-SYNC GENERATOR

P-Sync is a signal output by an 8080 to indicate that CPU status can be latched off the data bus.

This signal is not produced on the Z80, and therefore must be simulated in order to make a CPU S-100 compatible. This is done as accurately as possible by generating a P-Sync on every MREQ that is not a RFSH and on every I/O operation. This circuitry is provided on the XOR CPU.



PROGRAMMABLE BAUD RATE

The 8116 can be written into under software control of the Z80 at port 0BH to set the baud rate without removing the board from the computer. The lower 4 bits program the CPU serial channel A, and the upper 4 bits program channel B. The baud rate switch may be read through port 0BH. The XOR 1.85 PROM reads this 8 bit switch and loads the 8116 accordingly. Your boot or system initialization software may choose to use these 8 bits (or some part of them) to signal other things to the system.

PORT ASSIGNMENTS

```
00   Channel "A" data
01   Channel "A" status (See status flag below)
02   Channel "B" data
03   Channel "B" status (See status flag below)
04   Parallel "A" data
05   Parallel "B" data
06   Parallel "C" data
07   Parallel command port
08   Memory management
09   Prom Toggle, 00 = on    01 = off
0A   Boot prom disable
0B   Read/ Baud rate switch   Write/ Baud rate generator
0C   CTC chan 1
0D   CTC chan 2          if you have a hard disk system using
0E   CTC chan 3          the WD controller, these ports not
0F   CTC CMD             available for CTC use.
```

SERIAL PORT INITIALIZATION (8251 and SIO)

The following code is an example used to initialize the 8251 on the Rev B CPU or the SIO on the Rev C CPU.

```
; INITLIZE PERIPHERALS
;
        LXI     H,INZLST                ; POINT AT INITLIZE LIST
INZLOOP:                                ;
        MOV     B,M                     ; GET # OF PARAMETERS
        INX     H                       ;
        MOV     C,M                     ; GET PORT
        INX     H                       ;
        DCR     B                       ; TEST FOR 0 PARAMETERS
        INR     B                       ;
        JZ      PERIZFIN                ; IF 0 THEN FINISHED
        OUTIR                           ; BLOCK OUTPUT
        JMP     INZLOOP                 ;
;
; base io address for the sio on the rev c cpu
;
INZLST:                                 ;
                                        ;
        IF      SIO                     ;
;                                       ;
```

```
; SIO1 LIST                                ;
        DB      10                       ; 10 PARAMETERS TO SEND
        DB      LSTSTAT                  ; PORT TO SEND THEM
        DB      18H                      ;
        DB      1                        ;
        DB      00H                      ;
        DB      4                        ;
        DB      4CH                      ;
        DB      5                        ;
        DB      068H                     ;
        DB      3                        ;
        DB      41H                      ;
        DB      00                       ;
                                         ;
        DB      10                       ; 10 PARAMETERS TO SEND
        DB      CONPORT                  ; PORT TO SEND THEM
        DB      18H                      ;
        DB      1                        ;
        DB      00H                      ;
        DB      4                        ;
        DB      4CH                      ;
        DB      05                       ;
        DB      068H                     ;
        DB      3                        ;
        DB      41H                      ;
        DB      00                       ;
        ENDIF                            ;
                                         ;
        IF      I8251                    ;
        DB      4                        ; 4 PARAMETERS TO SEND
        DB      LSTSTAT                  ; PORT TO SEND THEM
        DB      0AAH                     ; SET MODE
        DB      040H                     ; RESET
        DB      0100$1110B               ; 1 STOP BIT, NO PARITY, 8 BITS, 16X
        DB      0011$0111B               ; RTS = 1, ERROR RESET, Rx ENABLED
                                         ; DTR = 1, Tx ENABLED
                                         ;
        DB      4                        ; 4 PARAMETERS TO SEND
        DB      CONPORT                  ; PORT TO SEND THEM
        DB      0AAH                     ; SET MODE
        DB      040H                     ; RESET
        DB      0100$1110B               ; 1 STOP BIT, NO PARITY, 8 BITS, 16X
        DB      0011$0111B               ; RTS = 1, ERROR RESET, Rx ENABLED
                                         ; DTR = 1, Tx ENABLED
                                         ;
        ENDIF                            ;
        DB      0                        ; END OF TABLE MARKER
```

This initialization will set up 8 data bits, one stop bit and no parity. Your printers and terminals have to be set up to receive the same pattern.

STATUS FLAGS FOR REV B CPU WITH 8251

Status Flags (when you input status port, this is what byte will mean):

```
Bit:  07   06   05   04   03   02   01   00
      ---------------------------------
      DSR  SY   FE   OE   PE   TXE RXR TXR <-Output bit (RDY when Hi)
                                  A
                                  |--------Input bit (RDY when Hi)
```

Ports for the 8251 and the Serial IO are:

A Status = 1 A Data = 0 (on left)
B Status = 3 B Data = 2 (on right)

STATUS FLAGS FOR REV C CPU WITH SIO

```
Bit:  07   06   05   04   03   02   01   00
      ---------------------------------
      BRK  TxU  CTS  SYN  DTR  TxR  INT  RxR <-Output bit (RDY when Hi)
                                  A
                                  |--------Input bit (RDY when Hi)
```

PORT ASSIGNMENTS ON OPTIONAL 4 PORT SERIAL BOARD

LOW SERIAL PORTS

20	CHANNEL	A	DATA
21	"	A	STATUS
22	"	B	DATA
23	"	B	STATUS
24	"	C	DATA
25	"	C	STATUS
26	"	D	DATA
27	"	D	STATUS
3A	BAUD RATE SELECT		

HIGH SERIAL PORTS

A0	"	A	DATA
A1	"	A	STATUS
A2	"	B	DATA
A3	"	B	STATUS
A4	"	C	DATA
A5	"	C	STATUS
A6	"	D	DATA
A7	"	D	STATUS
AA	BAUD RATE SELECT		

PMMI MODEM BASE ADDRESS = C0

D [DUMP]

D [DUMP] -The dump command will accept 4 hex bytes, jump to the next field, accept 4 more hex bytes and then display all of the memory locations between those two addresses. If you should wish to enter the numbers without leading zeros, you may do so by hitting a carriage return. For example, you could dump location 2 to location 8 in the computer by typing D2 <cr> followed by 8 <cr>.

L [LOAD]

L [LOAD] - The load command will accept one 4 byte address and then display the contents of that memory location on the screen. The prompt character will allow you to replace what is in that location of memory with the data that you type onto the screen. If you merely want to look at system memory, you can enter a carriage return or a series of carriage returns. The memory locations will not be modified, but will only be displayed on the screen in sequential manner.

F [FILL]

F [FILL] - The "FILL" command accepts a 4 byte [starting] address, moves to the next field, accepts a second 4 byte [ending] address, moves to the next field and accepts a 2 byte set of data. At this point, the "FILL" command will automatically be executed, filling all system memory between the starting address and the ending address with the data character set.

M [MOVE]

M [MOVE] - The "MOVE" command operates in the same manner as the "FILL" command with the exception that the 4 byte addresses are, respectively, the address of the source data and the address of the memory location to which the source data is to be moved. The 2 bytes which are entered next indicate the size [number of bytes in hex] of the block of memory to be moved.

V [VIEW]

V [VIEW] - The "VIEW" command upon receiving a 4 byte starting memory location will display sixteen lines of ASCII data [640 bytes] on the CRT screen. Typing carriage returns following the initial display causes the next sequential 640 byte blocks to appear.

G [GO]

G [GO] Enter destination address.

H [HEX]

H [HEX] Hex String Locate, enter starting address, ending address string to locate.

X [EXAMINE]

X [EXAMINE BANK] For selecting a certain bank to write to in multi user systems.

SERVICE POLICY

We would hope that your XOR would never require service, however, we feel that with a thorough reading of the manual most problems will be resolved. Should you feel the need to consult with our Customer Service personnel, they will be happy to answer your questions. Please call the number (714-898-5525) during normal business hours.

If you should require service on your XOR it will be performed at the plant facilities in Huntington Beach, or at an authorized XOR Service Center.

Equipment will be accepted for service only after you have been assigned a "Return Material Authorization Number". RMA. This number may be obtained by calling the Customer Service Hot Line 714-898-5525. The following information will be required:

The purchase date
The serial number
The problem

All shipments received without an RMA will be returned to the sender.

Warranty (6 months parts/labor, from the date of purchase) repairs will be made at no charge for parts and/or labor for XOR hardware only. Merchandise such as drives, terminals, and printers sold by US MICRO SALES as part of their systems will be sent back to the manufacturer for repair. Repair and freight charges for non-XOR merchandise will be billed to you by US MICRO SALES. All warranties are void if any portion of your computer system is altered by anyone other than factory authorized personnel.

Incoming freight MUST BE PREPAID. US MICRO SALES will not accept incoming freight which is marked COLLECT or COD. Shipping charges for the return of repaired equipment to you that is under warranti will be prepaid by US MICRO SALES except in cases where you specify method of shipment other than the one chosen by US MICRO SALES. All return shipping charges for equipment that is no longer under warranty are the responsibility of the party who sent the equipment for repairs.

SUGGESTIONS

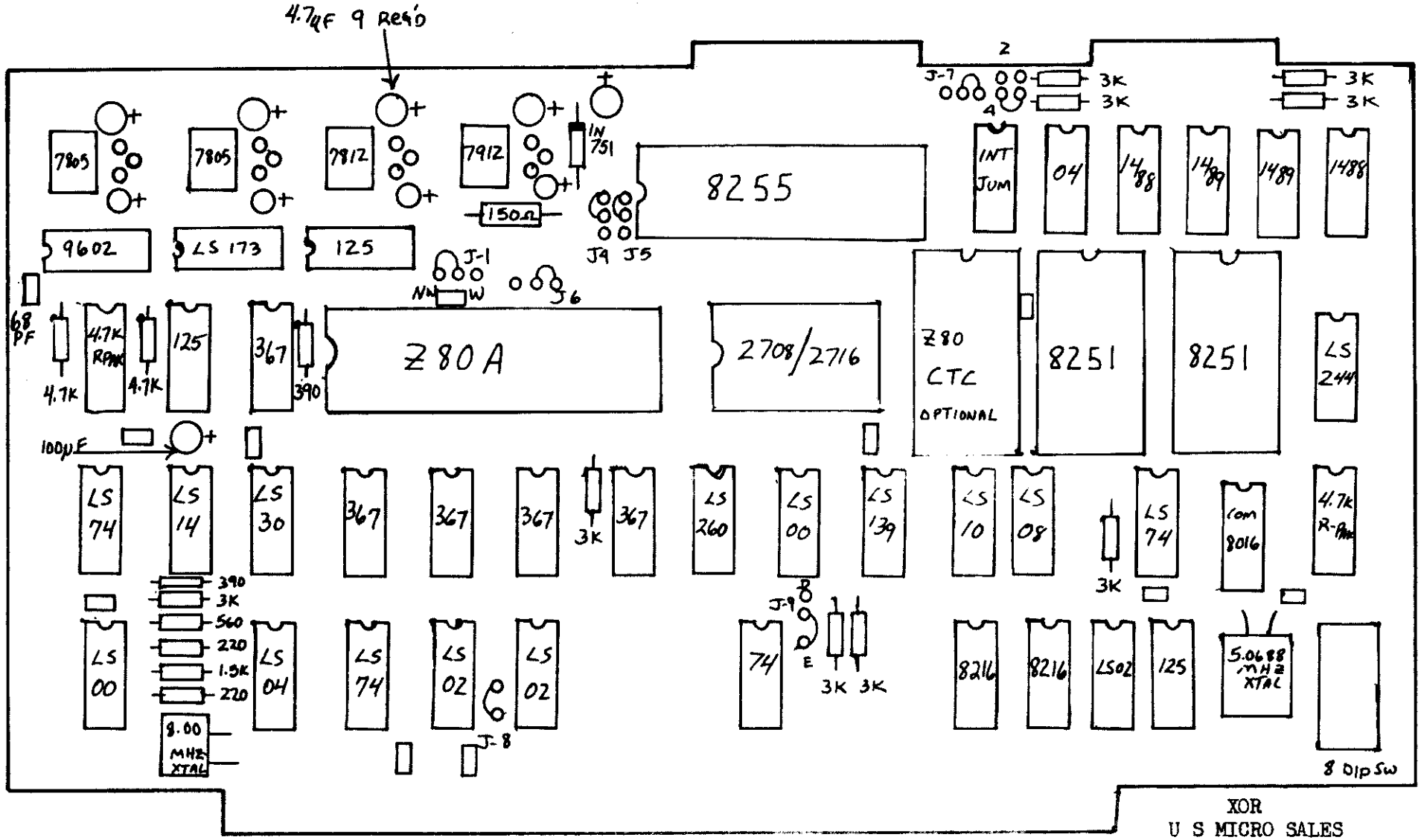
If you should have any suggestions regarding the use of this manual, or have any corrections or additions, we would be happy to hear from you. Please address your correspondence to:

U S MICRO SALES
Tech/Man Dept
15392 Assembly lane
Huntington Beach, CA 92649

rev 050383

1 2 3 4 5 6 7 8 9 10 12 13 14 15

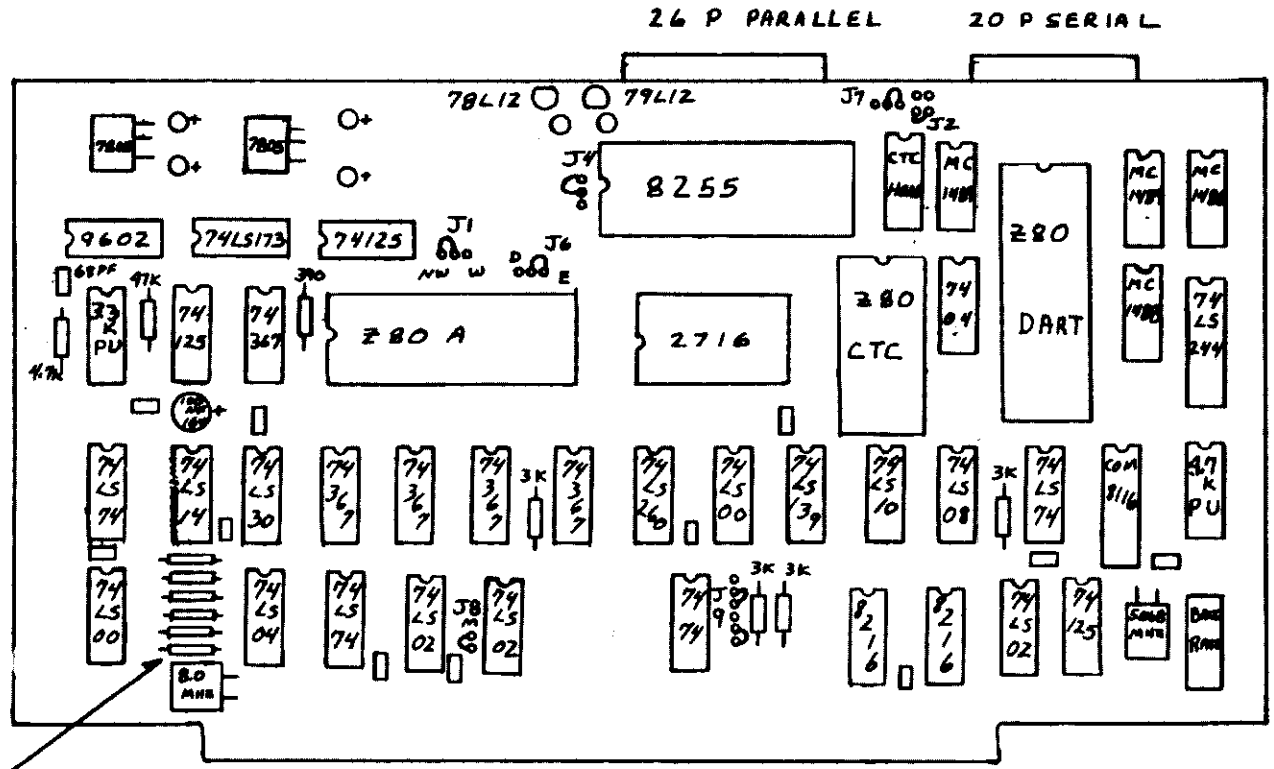
A B C D



XOR
U S MICRO SALES

PARTS LOCATION
XOR CPUB
7-6 12

ALL .1 bycap



390	
3K	
560	
220	
1.5K	
220	

NOTES

1. ALL .1 BY PASS 11 REQ'D
2. ○ ALL 4.7μF TANTALUM 6 REQD
3. BAUD RATE SHOWN BOTH PORTS 9600

SCALE: 1:1	APPROVED BY:	DRAWN BY PWS
DATE: 2-27-85		REVISED

CPU C REV C3A

US MICRO SALES

DRAWING NUMBER

PARTS LIST

CPU REV B

P/N	DESCRIPTION	QTY.	P/N	DESCRIPTION	QTY.
I-0000-06	HTSNK-B	4	I-3000-55	CK68PF	1
I-0000-13	NUT 4-40	4	I-3000-83	150 RES 2W	1
I-0000-24	SCRW4-40-A	4	I-3001-14	1.5 KRES	1
I-1000-06	S1 CPU BD-B	1	I-3001-15	3 KRES	5
I-2000-05	14 PSOC	25	I-3001-17	4.7MF25VR	2
I-2000-06	16 P SOC	10	I-3001-28	390 RES	2
I-2000-07	18 P SOC	2	I-3001-46	100 MF 16 VRB	1
I-2000-08	20 P SOC	1	I-7000-02	REG+5	2
I-2000-09	24 P SOC	1	I-7000-03	REG +12	1
I-2000-10	28 P SOC	3	I-7000-05	REG -12	1
I-2000-11	40 P SOC	2	I-7000-24	ZEN+5.6	1
I-2000-45	20 P CONN M	1	I-7000-33	5.06 MXZXTL	1
I-2000-50	26 P CONN M	1	I-7000-35	8 MHZXTAL	1
I-2000-64	3 SNGLAP	5	I-7000-41	SHINT-BRG	8
I-2000-84	5 DUALAP	1	I-7400-08	Z80 A DART	1
I-3000-01	4.7 KRES	1	I-7400-09	Z80ACPU	1
I-3000-32	14R302RPK	1	I-7400-10	1488	2
I-3000-33	14R472RPK	1	I-7400-11	1489	2
I-3000-39	.1 MF 50VR	13	I-7400-19	7404	1
I-3000-41	22 O RES	2	I-7400-29	7474	1
I-3000-47	4.7 MF 16 VR	6	I-7400-32	8116	1
I-3000-50	47 KRES	1	I-7400-35	8216	2
I-3000-53	560 RES	1	I-7400-36	8251	2
I-3000-54	8DIPSW	1	I-7400-37	8255	1

PARTS LIST CPU REV B (CON'T)

P/N	DESCRIPTION	QTY.	P/N	DESCRIPTION	QTY.
I-7400-45	9602	1	I-7400-78	74LS10	1
I-7400-53	74125	3	I-7400-81	74LS14	1
I-7400-63	74367	5	I-7401-22	74LS30	1
I-7400-71	74LS00	2	I-7401-09	74LS244	1
I-7400-72	74LS02	3	I-7401-12	74LS260	1
I-7400-74	74LS04	1	I-7401-23	74LS173	1
I-7400-76	74LS08	1	I-7401-34	74LS139	1

PARTS LIST

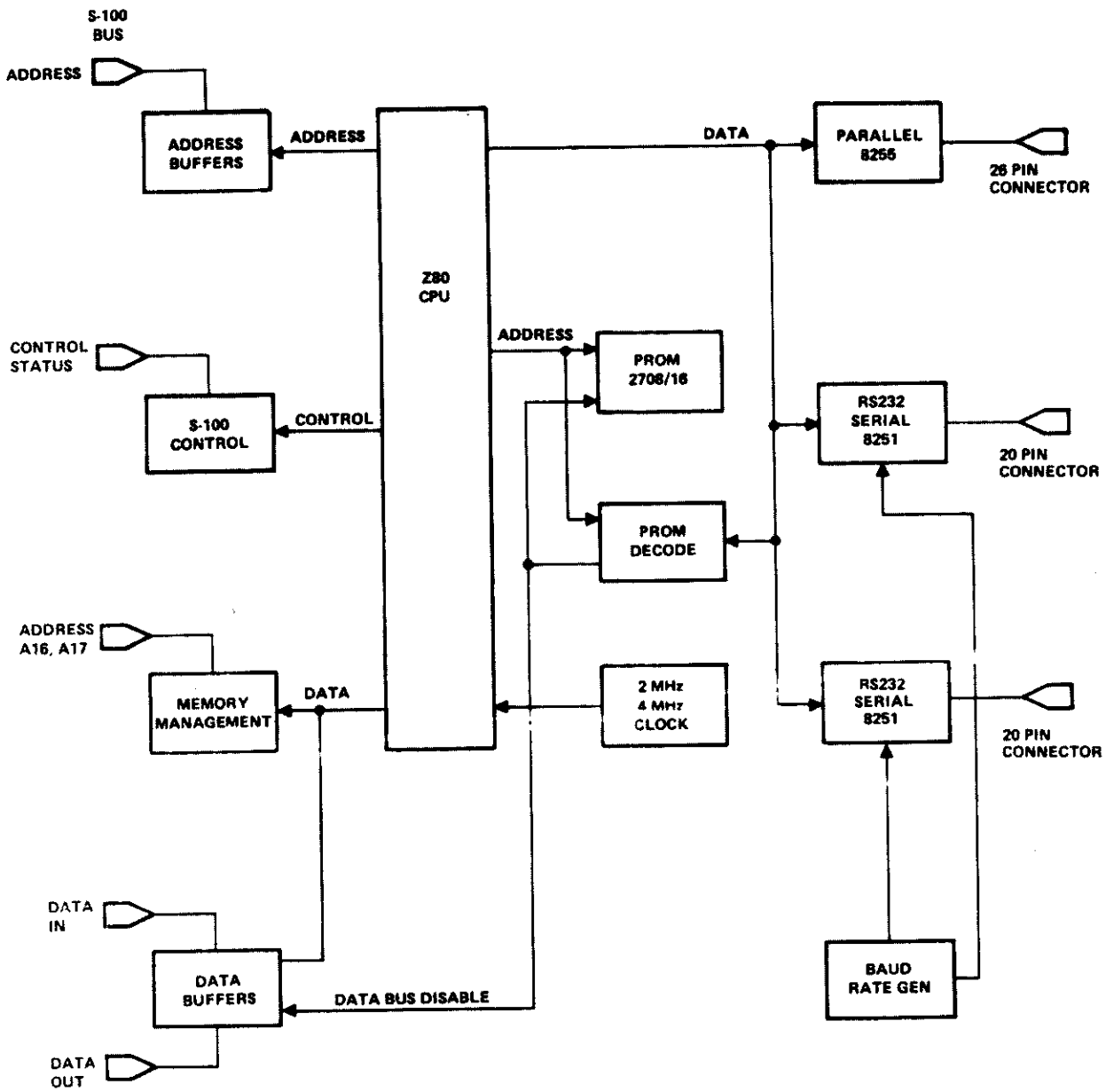
CPU REV C

P/N	DESCRIPTION	QTY.	P/N	DESCRIPTION	QTY.
I-0000-06	HTSNK-B	4	I-3001-15	3 KRES	5
I-0000-13	NUT 4-40	4	I-3001-17	4.7 MF 25VR	2
I-0000-24	SCRW 4-40	4	I-3001-28	390 RES	2
I-1000-37	S1 CPU BD-C	1	I-3001-46	100 MF 16VR B	1
I-2000-05	14 P SOC	25	I-7000-02	REG +5	2
I-2000-06	16 P SOC	10	I-7000-13	78L12	1
I-2000-07	18 P SOC	2	I-7000-14	79L12	1
I-2000-08	20 P SOC	1	I-7000-33	5.06 MHZXTAL	1
I-2000-09	24 P SOC	1	I-7000-35	8 MF ZXTAL	1
I-2000-10	28 P SOC	1	I-7000-41	SHUNT BRG	8
I-2000-11	40 P SOC	3	I-7400-08	Z80 A DART	1
I-2000-45	20 P CONN M	1	I-7400-09	Z80 A CPU	1
I-2000-50	26 CONN M	1	I-7400-10	1488	2
I-2000-64	3 SNGLAP	6	I-7400-11	1489	2
I-2000-65	4 DUALAP	1	I-7400-19	7404	1
I-3000-01	4.7 KRES	1	I-7400-29	7474	1
I-3000-32	14 R302 RPK	1	I-7400-32	8116	1
I-3000-33	14 R472 RPK	1	I-7400-35	8216	1
I-3000-41	220 RES	2	I-7400-37	8255	1
I-3000-47	4.7 MF 16VR	4	I-7400-45	9602	1
I-3000-50	47 KRES	1	I-7400-53	74125	3
I-3000-53	560 RES	1	I-7400-63	74367	5
I-3000-54	8 DIP SW	1	I-7400-71	74LS00	2
I-3000-55	CK68PF	1	I-7400-72	74LS02	3
I-3000-58	.1 MF 50VR	13	I-7400-74	74LS04	1
I-3001-14	1.5 KRES	1	I-7400-76	74LS08	1

PARTS LIST CPU REV C (CON'T)

PARTS LIST CPU REV C (CON'T)

P/N	DESCRIPTION	QTY.	
I-7400-81	74LS14	1	
I-7400-87	74LS74	1	
I-7401-09	74LS244	1	
I-7401-12	74LS260	1	
I-7401-22	74LS30	1	
I-7401-23	74LS173	1	
I-7401-34	74LS139	1	



BLOCK DIAGRAM

X D S PROM NUMBERING CONVENTIONS

PROM 5:
S44 SYSGEM WITH VDC VIDEO BOARD & GEORGE RISK KEYBOARDS

PROM 6:
USED WITH MEMORY TEST STATION, FOR 32K STATIC RAM BOARDS
USED WITH ITHACA AUDIO CPU AND VB1 VIDEO BOARD.

PROM 7:
MODIFIED PROM 5. CONSOLE I/O USE NEW DELTA S44 SERIAL BOARDS.

PROM 9: MODIFIED PROM 7. CAPABLE OF RUNNING IN S100 CPU'S
REV "A" CPU

PROM 1.82
REV "A" CPU. HAS NO PROGRAMMABLE BAUD RATE. (OBSOLETE VERSION)

PROM 1.83
REV "B" & "A" CPU. HAS PROGRAMMABLE BAUD RATE IN REV "B" CPU.

12/20/82

PROM 1.85
REV "B" CPU VERSION. PROGRAM MODIFICATIONS:

1. Prom "version" number returned in HL register pair on call to constat.
2. "X" command added to assist in de-bugging bank switched memory systems.
3. 24 lines are displayed on screen instead of original 15.
4. "VIEW or 'V' command also fills screen.
5. Floppy boot routine upon failure to boot seeks head out five tracks and homes drive. Also reports errors in English instead of hex.

PROM 1.95
REV "C" CPU VERSION OF THAT ABOVE.

PROM 2.80
SHUGART HARD DISK AS1400. REV "B" CPU (OBSOLETE VERSION)
USED WITH CP/M 2.21S DATED BEFORE 5/22/81

PROM 2.81
MODIFIED VERSION OF PROM 2.80. TO BE USED WITH CP/M 2.21S DATED BEFORE 5/22/81 AND AFTER.

PROM 2.82
MODIFIED VERSION OF PROM 2.81. TO BE USED WITH REV "C" SIO CPU.

12/20/82

PROM 2.85
MODIFED VERSION OF PROM 2.81. TO BE USED WITH CP/M 2.2 AND MP/M 2.0.

PROM 2.95
SAME AS 2.85 BUT FOR "C" CPU.

PROM 3.80
NEW PRIAM VERSION. USED WITH REV "B" CPU AND PRIAM CP/M AND MP/M DATED 5/22/81 AND LATER.

PROM 3.81
NEW PRIAM VERSION. USED WITH REV "C" CPU AND PRIAM CP/M AND MP/M AND CP/NET DATED 5/22/81 AND LATER.

PROM 3.82
NEW PRIAM VERSION MODIFIED FROM 3.81 FOR ALL REV CPU'S TO BOOT A CTRL A,B,C FOR THE PRIAM AND F FOR THE FLOPPY.

12/20/82

PROM 3.85
NEW PRIAM VERSION MODIFIED FROM 3.81 FOR CP/M 2.2 AND MP/M 2.0.

PROM 3.95
PRIAM VERSION FOR "C" CPU.

PROM 4.00
PARALLEL KEYBOARD INTERFACE CONSOLE I/O. USED IN ADDS 25/120 TERMINALS. REV "B" CPU.

PROM 4.84
PARALLEL KEYBOARD ADDS 25/120 TERMINALS AS OF 12/20/82 REV "B" CPU.

PROM 4.94
PARALLEL KEYBOARD ADDS 25/120 TERMINALS AS OF 12/20/82 REV "C" CPU.

PROM 4.85
MODIFIED FOR SLAVE NET-WORK OPERATION. REV "C" CPU'S.

PROM 5.81
SMS 10 MEG SYSTEMS FOR REV "B" CPU. CP/M 2.2 AND MP/M 2.0

PROM 5.82
SMS 20 MEG SYSTEMS FOR REV "B" CPU. CP/M 2.2 AND MP/M 2.0

PROM 5.84
SMS 40 MEG SYSTEMS FOR REV "B" CPU. CP/M 2.2 AND MP/M 2.0

PROM 5.9X SERIES
SAME AS 5.8X BUT FOR REV "C" CPU.

PROM 6.8
WD DISK CONTROLLER WITH REV "B" CPU.

PROM 6.90
WD DISK CONTROLLER WITH REV "C" CPU.

PROM 7.80
S100-12 SYSTEMS WITH IOMEGA DRIVES AND "B" CPU.

PROM 7.90
S100-12 SYSTEMS WITH IOMEGA DRIVES AND "C" CPU.

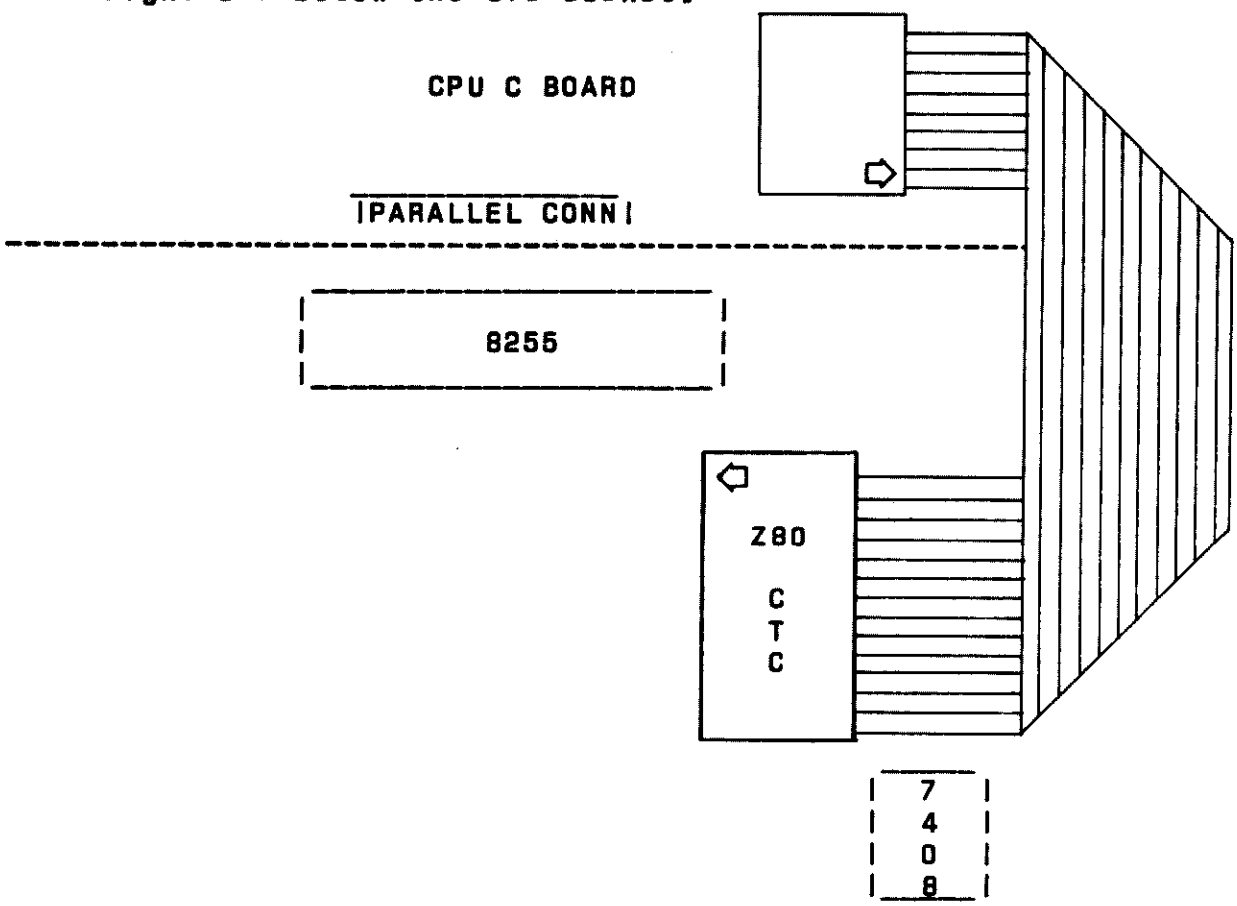
APPENDIX A

CPU C ADDENDUM

NOTES TO MODIFY FOR USE WITH WDC HD ADAPTER.

1. Jumper from 8255 36 to CTC Socket pin 21.

2. Jumper from CTC Socket pin 22 to IC 7408 pin 2 just to the right and below the CTC Socket.



HARD DISK NOTES

U. S. Micro Sales uses various manufacturers for its hard disk systems. Please check reference views in this manual for mechanical details.

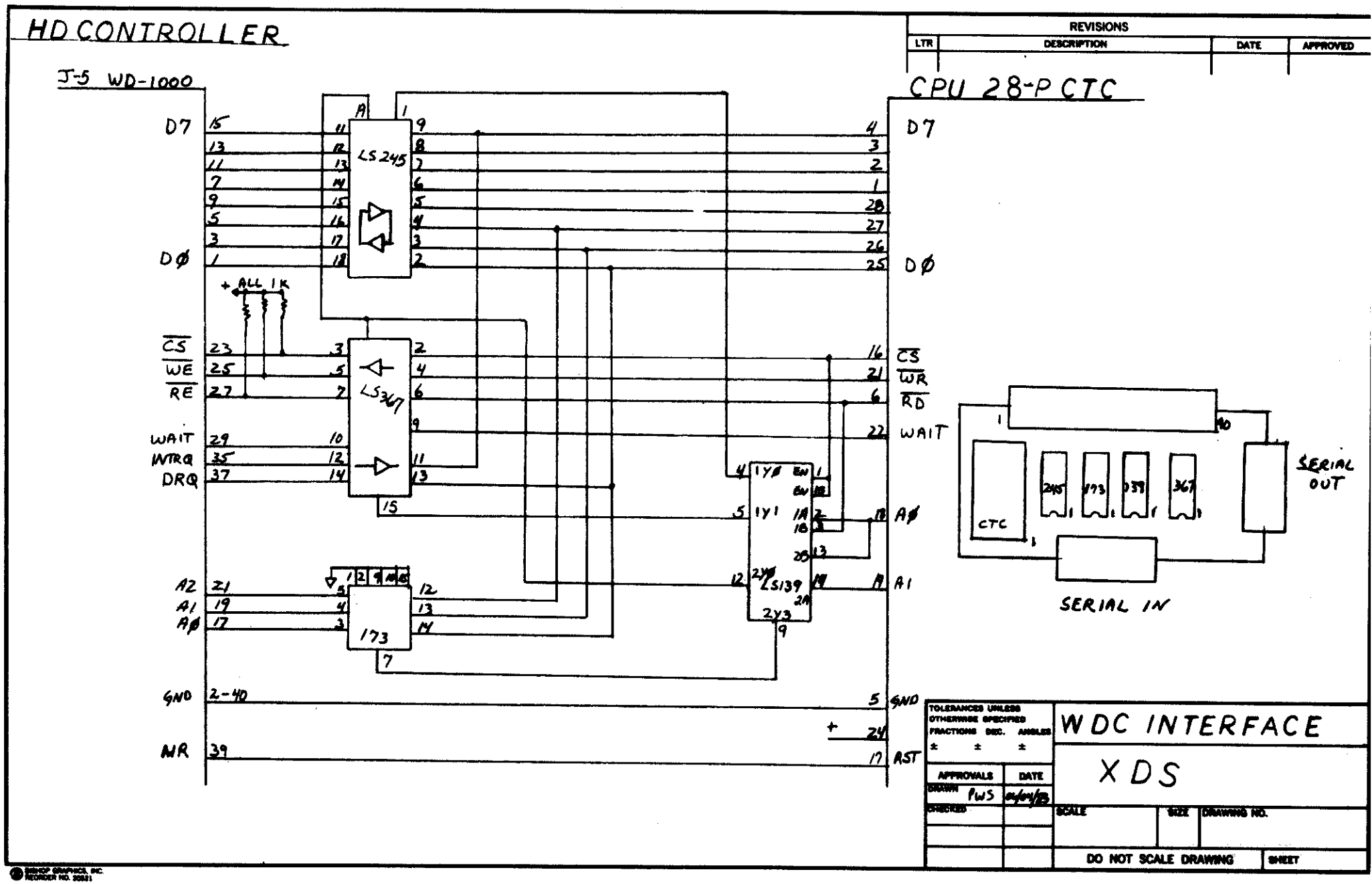
Note the hard disk controller WD 1001-05 is interfaced to the CPU via the CTC socket with a 5 inch 28 pin to 28 pin cable.

The power supply for the drives is set up for +12 volts.

WDC PIGGYBACK REV A

PARTS LIST

PART NUMBER	DESCRIPTION	QTY.
I-1000-43	WDC PCB	1
I-2000-45	20 PIN MALE SOCKET	1
I-2000-43	20 PIN FEMALE SOCKET	1
I-2000-03	40 PIN MALE SOCKET	1
I-2000-10	28 PIN IC SOCKET	1
I-2000-08	20 PIN IC SOCKET	1
I-2000-06	16 PIN IC SOCKET	3
I-3000-59	1K RESISTOR	3
I-3000-47	4.7 OHM 20V CAPACITOR	1
I-3000-58	.1uf OV CAPACITOR	1
I-7401-43	74LS367	1
I-7400-34	74LS139	1
I-7401-23	74LS173	1
I-7401-55	74LS245	1

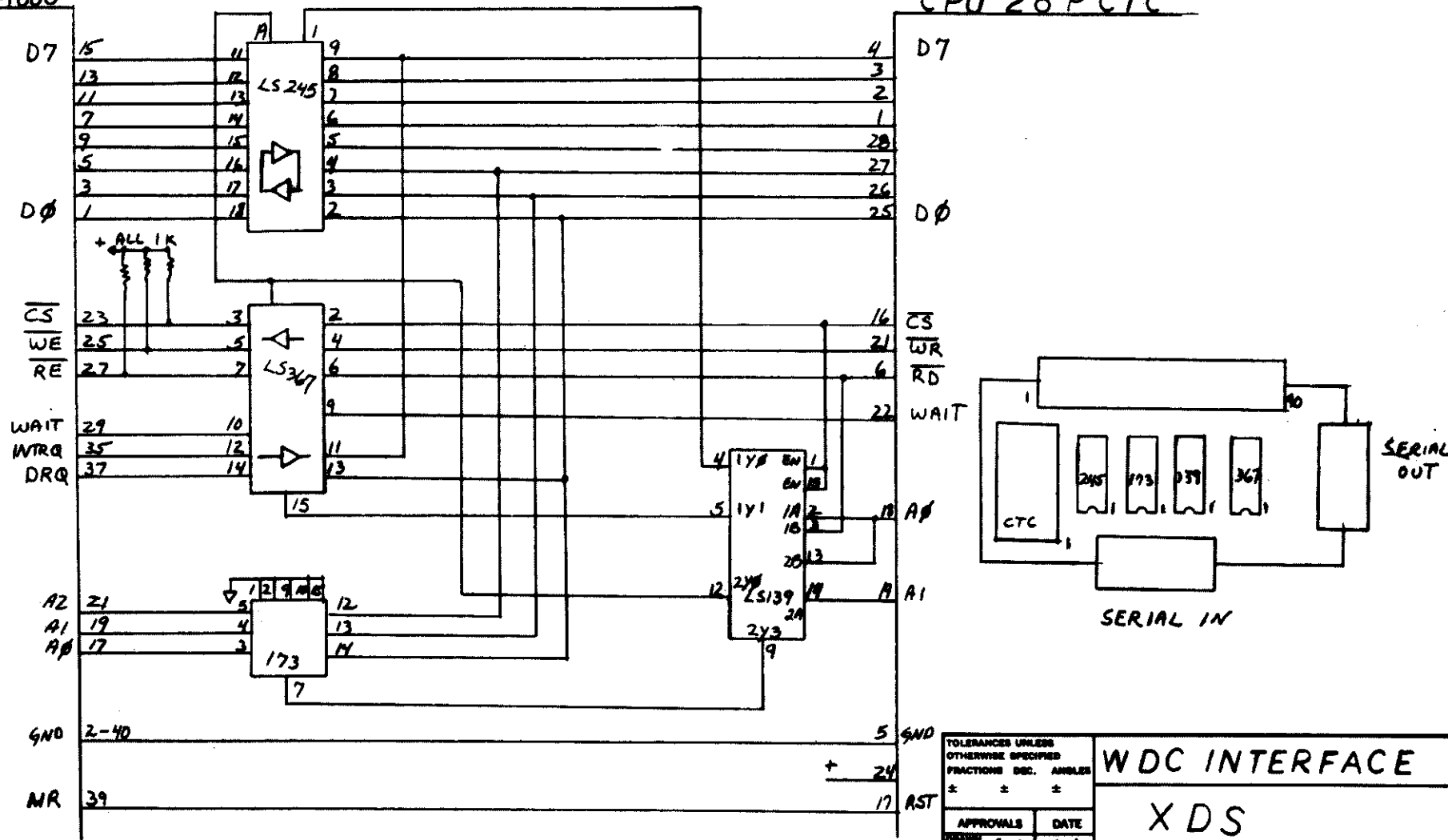

HD CONTROLLER
J-5 WD-1000
REVISIONS
LTR
DESCRIPTION
DATE
APPROVED
CPU 28-P CTC
D7
DØ
CS
WE
RE
WAIT
INTRQ
DRQ
A2
A1
AØ
GND
MR
LS245
LS367
173
LS139
ALL 1K
RST
WR
RD
SERIAL OUT
SERIAL IN
CTC
WDC INTERFACE
XDS
TOLERANCES UNLESS OTHERWISE SPECIFIED
FRACTIONS DEC. ANGLES
APPROVALS
DATE
DRAWN
PWS
SCALE
SIZE
DRAWING NO.
DO NOT SCALE DRAWING
SHEET

HD CONTROLLER

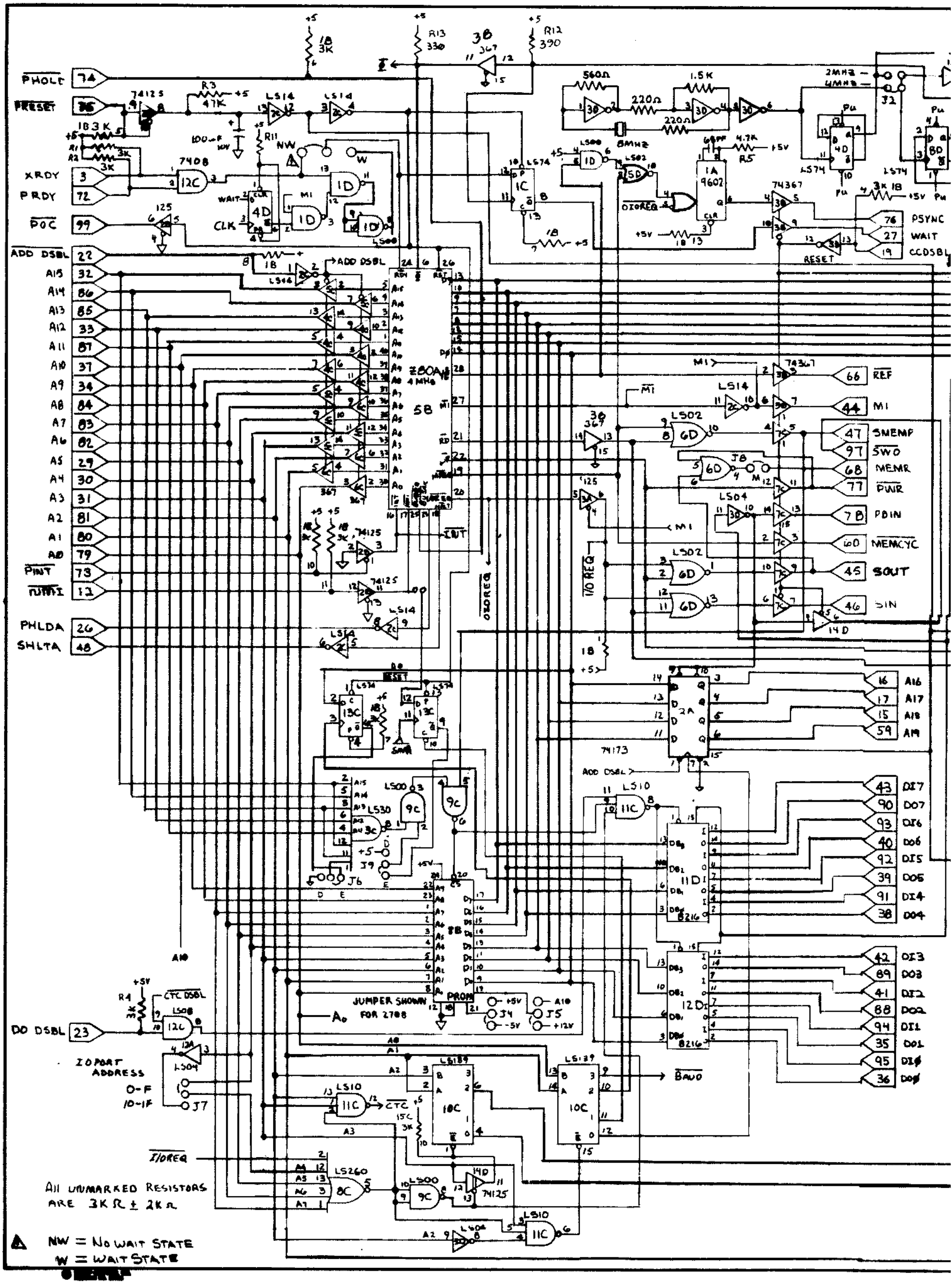
REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

J-5 WD-1000

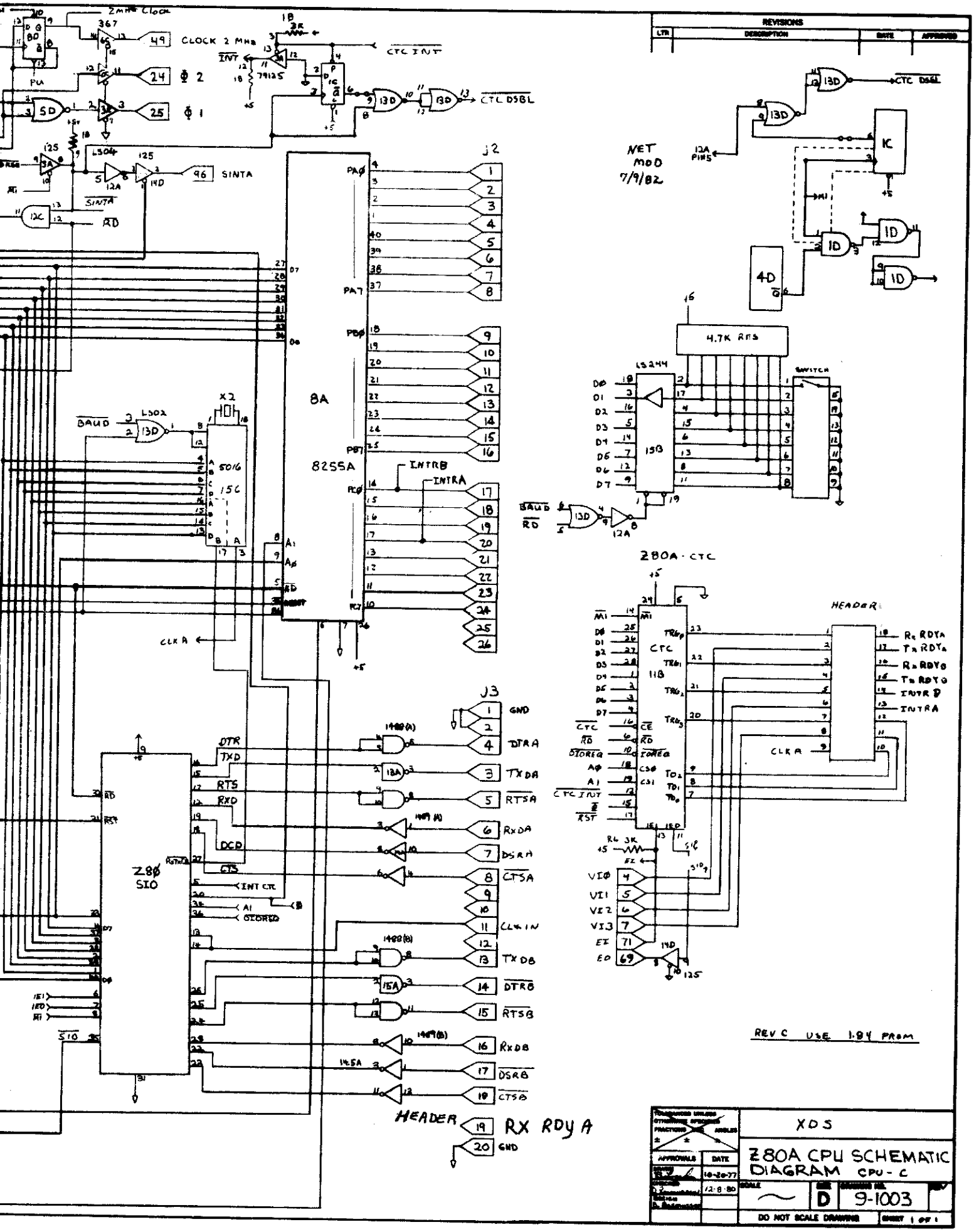
CPU 28-P CTC



TOLERANCES UNLESS OTHERWISE SPECIFIED FRACTIONS DEC. ANGLES ± ± ±		WDC INTERFACE	
APPROVALS	DATE	XDS	
DRAWN PWS	04/04/83	SCALE	SIZE / DRAWING NO.
CHECKED		DO NOT SCALE DRAWING	SHEET



PHOLD 74
PRESET 36
XRDY 3
PRDY 72
POC 99
ADD DSBL 22
A15 32
A14 86
A13 85
A12 33
A11 87
A10 37
A9 34
A8 84
A7 83
A6 82
A5 29
A4 30
A3 31
A2 81
A1 80
A0 79
PINT 73
NMI 12
PHLDA 26
SHLTA 48
DO DSBL 23
Z80A
4 MHz
5B
8MHZ
2MHZ
4MHZ
9602
74367
PSYNC 76
WAIT 27
CCDSBL 19
REF 66
M1 44
SMEMR 47
SWO 97
MEMR 68
PWR 77
PDBIN 78
MEMCYC 60
SOUT 45
SIN 46
A16 16
A17 17
A18 15
A19 59
74173
DI7 43
DO7 90
DI6 93
DO6 40
DI5 92
DO5 39
DI4 91
DO4 38
DI3 42
DO3 89
DI2 41
DO2 88
DI1 94
DO1 35
DI0 95
DO0 36
8216
PROM
JUMPER SHOWN FOR 2708
I/O PORT ADDRESS
0-F
10-1F
BAUD
CTC
I/OREQ
All UNMARKED RESISTORS ARE 3KΩ ± 2KΩ
NW = NO WAIT STATE
W = WAIT STATE


REVISIONS
LTR
DESCRIPTION
DATE
APPROVED
2MHz Clock
CLOCK 2 MHz
CTC INT
CTC DSBL
Φ 2
Φ 1
SINTA
RD
NET MOD 7/9/82
4.7K RES
SWITCH
BAUD
8A
8255A
INTRB
INTRA
X2
5016
J2
J3
GND
DTRA
TXDA
RTSA
RxDA
DSRA
CTSA
CLK IN
TXDB
DTRB
RTSB
RxDB
DSRB
CTSB
Z8Ø SIO
INT CTL
280A - CTC
CTC
HEADER
CLK A
REV C USE 1.8Y PROM
HEADER
19 RX RDY A
20 GND
XDS
Z80A CPU SCHEMATIC DIAGRAM CPU-C
SIZE D
9-1003
DO NOT SCALE DRAWING


XOR