Aug. 13, 84

PX-4

PORTABLE COMPUTER

TECHNICAL MANUAL

訳者注を入れておりますが下記ご訂正願います。

(2) 1. Sub-battery → Auxiliary battery

(2) 2. メモリーカートリッジ、複合形式のデバイスについては、内容が（翻訳の過程で）把握できないため、例えばカートリッジのコマンド、エレメントの定義や用途に誤りがあると思われますので、[illegible]しくご検討、ご訂正下さい。

*. 例えば "Micro cassette drive" 等を原文で名称の統一されていないものについては訳文でも統一がはかられていない場合がありますのでご注意下さい。

** なお、右マージンのドット（...）は、訳者が原文の意味を充分に理解し得ないか、適確な訳表現を思いつかない部分を示します。よろしくご検討下さい。

P/5 1.1 Product Features

..... (1) PX-4 is a battery-drivable notebook size portable computer. This computer is made thinner and weighs less than the existing competing models on a policy of attaching much importance to portability.

Computers are being used in more various locations including places of businesses and sales activities and sites of jobs, etc., expanding from office rooms which have been common places for computers in the past. This trend has presented a strong demand for handy and battery drivable computers. PX-4 is one of the models which most meet this demand.

PX-4 has no selection in locations of use. It can be used anytime and anywhere; in office rooms, in factories, at homes, outdoors, and even in conveyances. (we can work)

(2) Another demand for specialized computers, which can also relieve users from special computer knowledges in contrast to major conventional general purpose computers, is also strong. This demand is (especially) strong for handy portable computers. PX-4, which is itself a general purpose machine using the CP/M operating system, still puts much importance on specialization. The keyboard is modularized and can be easily attached and removed so that the computer can be immediately converted to a specialized machine fit for a specific application by replacing the standard keyboard with an item keyboard and putting specialized sheet on the keytops. The programs for each specialized machine are stored in a ROM capsule which can also

be easily replaced.

Many option features can be attached in addition which help to build a specialized system optimum for each of various applications.

P/6 (3) PX-4 provides the following features which have been selected through studies in pursuit of an easy-to-use computer:

* Manganese battery service - PX-4 can be powered by manganese batteries. It can be used for an unlimited period of time without interruption by replacing the power source batteries.
* Economical uninterrupted service - PX-4 is free from power interruption. A combined use of an AC adaptor and batteries (or a special battery unit) can ensure economical uninterrupted service if the commercial AC source is lost.
* Job protection from unexpected loss of power - If the battery supply is used up or PX-4 is turned off during program run, the program can be resumed by replacing the batteries or turning PX-4 back on.
* Easy program selection by menus - A program can be easily selected via menus on CRT screen.
* Automatic routine program run - A specific routine program can be automatically run only by turning PX-4 on.
* Automatic power off - PX-4 is automatically turned off if inadvertently left on.
* Programmed operation - PX-4 can be automatically turned on at a specified time, a specified program can be automatically run, and PX-4 can be automatically turned off after the program

execution is completed.

In addition, an alarm buzzer can be sounded and a specified message can be displayed at a specified time.

The combination of battery-driven operations and time control capability makes another step forward in widening and diversifying computer usable areas. PX-4 is much expected as a specialized computer in applications such as automatic measurements, automatic control, stock control, schedule control, and education, etc.

P/7 (4) The PX-4 electronics are built using a Z-80 CMOS main CPU and a 7508 4-bit slave CPU in combination as a core.

* The main CPU operates at 3.68 MHz.
* Major control sections are built with custom LSIs for high density circuit integration and reliability.
* As many flat package IC and chip elements as possible are used for high density circuit integration and reliability.

PX-4 can provide an internal memory capacity much larger than existing competing models.

* Up to three 32K byte ROM elements can be incorporated.
* Up to 64K bytes of RAM can be incorporated.

The standard ROM and RAM capacity can be expanded by selecting from the following option memory features:

* ROM cartridge - can contain two 32K byte ROM elements.
* RAM cartridge - can provide a RAM capacity of up to 16K (32K or 64K) bytes.
* Microcassette drive
* External RAM disk - can provide a RAM capacity of up to 64K (128K) bytes.

These memory devices may be replaced with models of higher performance which will be developed in pace with advancement in memory IC technology in future.

A 40 columns wide and 8 lines high LCD (Liquid Crystal Display) panel is used as data display component. This LCD relieves the operator from fatigue of eyes due to variation in contrast, which has been a problem on conventional CRT screens, because of its operating principle of reflecting external light.

For easier view, the LCD panel can be adjusted at various angles to the keyboard face.

Furthermore, the computer body itself can be inclined on the desk top for more ease of operation.

/8 The PX-4 keyboard is modular and can be easily attached and removed. Either the standard keyboard or an item keyboard are available for selection by users.

* The item keyboard is used for a specialized machine.
* The standard keyboard can be converted only by replacing keytops and resetting a DIP switch assembly such that it can be be used in various countries.

A conductive rubber key switch contact used in the keyboards much simplifies key switch structure and ensures higher reliability.

There are the following three categories of option devices which can be attached to PX-4:

* Devices installed directly through the cartridge connector.

* Devices installed directly through the system bus connector.
* Devices externallly attached through an information cable.

PX-4 can use a manganese (or alkali) and Ni-Cd batteries and an AC adaptor as a main power source.

RAM is backed up by a auxiliary (or sub-) Ni-Cd battery while the main manganese (or alkali) battery is replaced.

AC adaptors of barious specifications are prepared for use in all areas of the world.

The batteries have the following minimum lives when PX-4 is used with no option devices attached:

* Ni-Cd battery: 4 hours
* Manganese battery: 5 hours
* Alkali battery: 11 hours

1.2 Maximum Hardware System Configuration

The following figure shows the maximum PX-4 hardare system configuration:

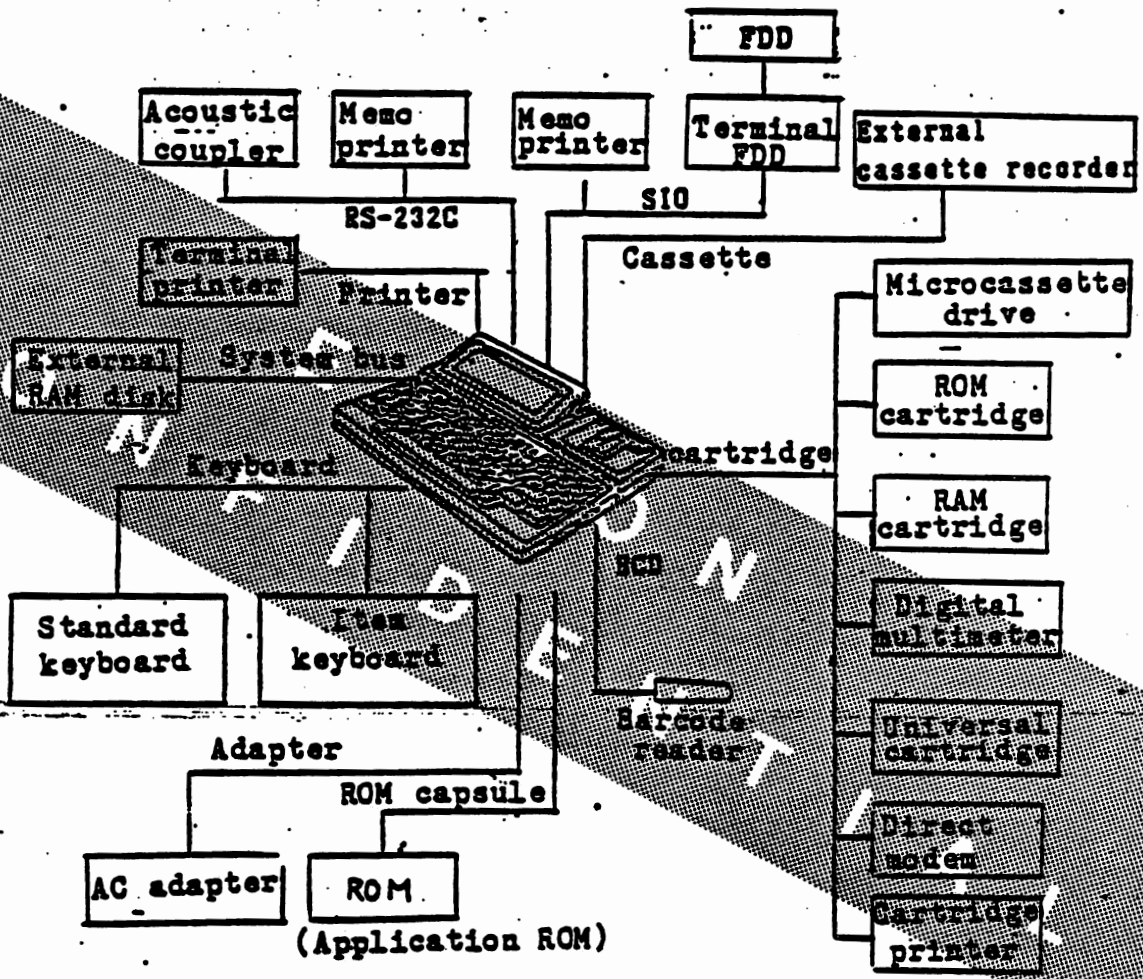


Fig. 1-1: Maximum hardware system configuration

EPSON CORPORATION	TITLE	SHEET REVISION	NO. 6
			NEXT SHEET

The individual option devices which can be attached via the connectors available on the computer frame are described in the following.

1.2.1 Keybarods

(1) Standard keyboard

The standard keyboard, which has 72 key switches and three LEDs, basically uses the ASCII ocde. It can conform to any of various languages only by replacing key tops and selecting the character set with a chardcter set selection DIP switch assembly.

The DIP switch assembly is set as follows:

Table 1-1. Character set selection DIP switch setting

DIPSW 8 7 6 5 4 3 2 1

- 1 — Character set specification switches
- 2 — Listing device specification switches
- 8 — Item keyboard flag switch (need not be set.)

Character set	4	3	2	1
ASCII	ON	ON	ON	ON
French	ON	ON	ON	OFF
German	ON	ON	OFF	ON
English	ON	ON	OFF	OFF
Danish	ON	OFF	ON	ON
Swedish	ON	OFF	ON	OFF
Italian	ON	OFF	ON	OFF
Spanish	ON	OFF	OFF	OFF
Japanese	OFF	ON	ON	ON
Norwegian	OFF	ON	ON	OFF

6	5	Listing device
OFF	OFF	SIO
OFF	ON	Cartridge
ON	OFF	RS-232C
ON	ON	Printer

The ASCII keyboard is used for Spanish and Italian.

The standard keybaord uses a new conductive rubber movable key switch contacts.

(2) Item Keyboard

The item keybaord is required when using PX-4 as a specialized machine.

It has 58 key switches which are classified into item and numeric keys. The 31 item keys can serve for up to 62 functions by using them in combination with the shift key; with two functions assigned to each item key.

The key names can be listed on an attached overlay sheet. They can also be printed on the key tops if desired.

The keyboard also requires a character set selection depending on where it is used.

Item keys are registered using a KEY command in BASIC or a PUT PFK command in BIOS.

The key switches have the same as that of the standard keyboard structure.

1.2.2 Cartridges

(1) Microcassette drive

The microcassette drive is a audio microcassette tape recorder used as a sequential file disk (named drive H).

A microcassette tape has directories at the beginning (up to 12 directories can be contained) in order for quick file search.

The microcassette drive has a CPU built in which operates by control commands from the PX-4. Microcassette operations can also be manually accomplished from the system display.

The microcassette drive panel has two lamps FREE and REC. The microcassette tape may be ejected when the FREE lamp is on.

Data are recorded on tape as two audio frequencies; mark is 1 KHz and space is 2 KHz. Microcassette tape data can be output to a buzzer built in the computer ~~frame~~ or an external speaker.

When connected to the cartridge interface, the microcassette drive operates in ~~the~~ handshake (HS) mode.

(2) ROM cartridge

The ROM cartridge can contain two 32K byte ROM ~~chips~~ IC elements which are used as two read-only disks (respectively assigned drive names J and K).

The ROM cartridge is structured as a ROM capsule and the ROM ~~chips~~ IC elements can be easily replaced by removing the case cover. This ROM capsule can contain N-MOS or C-MOS EPROM ~~chips~~ elements equivalent to 2764, 27128, or 27256, or mask ROM ~~chips~~ elements. Normally, one of the two ~~chips~~ elements is independently ~~designated for read.~~ addressed

However, the two elements can also be continuously read.

When connected to the cartridge interface, the ROM cartridge operates in the data bus (DB) mode.

(3) RAM cartridge

The RAM cartridge can be used in the same way as a floppy disk drive (assigned a drive name I).

This cartridge contains two 64K bit static RAM IC elements and provides a memory capacity of 16K bytes.

Memory data is protected by an incorported lithium battery while PX-4 is turned off. This battery has a capacity of protecting the RAM for three years or longer. When the battery is exhausted, an indicator lamp LOW BATTERY comes on at the time either element is accessed. The battery can be replaced by loosening the case screws.

The present RAM capacity is 16K bytes. 32K or 64K byte cartridges can also be connected.

The RAM cartridge must be formatted via the system display before put in use. The first RAM address is a directory which can contain up to 16 entries.

The cartridge is organized as follows:

Tracks: 0 - 1 (16K bytes)
0 - 3 (32K bytes)
0 - 7 (64K bytes)

Sectors: 0 - 63

When connected to the cartridge, the RAM cartridge operates in the data bus (DB) mode.

(4) Digital multimeter

An automatic measurement system is built by connecting a digital multimeter to PX-4.

A digital meter has an A-D converter IC and a CMOS CPU built-in and measures voltages applied, or resistances connected, across the measurement terminals.

PX-4 sends commands to the digital multimeter to control the power supply and read measured data. This measurement control is accomplished by a BASIC program.

The digital multimeter is connected with the PX-4 and completely electrically isolated from it to ensure teh safety of human body. This means power cannot be supplied from PX-4. Thus, the multimeter operates using two manganese batteries.

Major specifications are listed below.

Measurement ranges: DC voltage 0.1 mV - 500 V (5 ranges)
AC voltage 1.0 mV - 350 V (4 ranges)
Resistance 0.1 - 3M ohms (5 ranges)

Voltage or resistance ranges can be automatically selected.

Input impedance: 10M ohms
Sampling rate: 4 to 5 times/sec.
Power consumption: 9 mW

(5) Universal cartridge

The universal cartridge refers to a universal printed circuit board which has a connector mounted and installed in a cartridge case.

Users can build any circuit on the board to implement a cartridge specific to each user.

The universal cartridge is can be controlled by BASIC programs.

P/14 (6) Direct modem

Direct modems are presently allowed only in the U.S.A.

By using a direct modem, PX-4 can be directly connected to a telephone line for data transmission which ensures communications stabler than through an acoustic coupler. When this direct modem cannot be used, connect a plug wired to a microphone and speaker. It will serve as an acoustic coupler.

When a handset is used, the line can be monitored and PX-4 can be used also as a telephone.

Because of its automatic (pulse and tone) dialing functions, the modem provides the PX-4 with capabilities of automatic call and subsequent data transmission. The modem also has a function of automatic answering through telephone bell detection so that the PX-4 can automatically receive data.

The modem contains a CPU and the cartridge operates in the I/O mode. It is used by BASIC programs.

(7) Cartridge printer

A cartridge printer is an impact-type dot matrix printer which contains a CPU and RAM and provides a print buffer capacity of eight lines of data.

Two models of 40 and 32 digits per line are available which are compared in the table below.

Table 1-2. Cartridge printers

	40 columns/line	32 columns/line
Advantage	Can print in correspondence to the PX-4 display.	Can produce easy to read listing becase of wider charcter spacing.
Disadvantage	Listing is less easy to read because characters are less spaced.	A rightmost portion of screen hardcopy drops.
Print speed	2.5 second/line	2.0 second/line

Either of the two models can be selected depending on the user's preference for conformity to the PX-4 characteristics or ease of use.

Summarized specifications:

* Requires a Ni-Cd battery as main PX-4 power source.
* Uses the PX-4 internal character codes.
* The following functions are program-controlled:
  - International character set selection
  - Enlarded character print
  - Bit image print
  - Print sheet feed
* Print sheet: 57.5 mm wide sheet roll of 22 mm diameter.
* Ribbon: Cassette type.
* Reliability:
  - MCBF: 500,000 lines
  - Ribbon life: 200,000 to 250,000 characters

The cartridge printer is controlled by the system program depending on ~~keyboard~~ DIP switch setting (see table 1-1).

The printer is powered from the main PX-4 battery. It requires a relatively large amount of current and an Ni-Cd battery should be used as main battery. A combined use with the AC adapter is recommended. If a power failure occurs in the PX-4 or power is turned off during a print, the printer operation terminates at that moment and thus the subsequent characters drop.

When connected to the cartridge interface, the printer operates in the Handshake (HS) mode.

P/16 1.2.3 Printer

PX-4 can connect a Centronics-compatible printer. The printer connector installed on the computer frame is internally wired to a special PX-4 interface and a cable assembly #731 is required.

The PX-4 printer interface uses a CMOS line driver IC. If the signal lines require more than 2 mA per line, a printer adapter needs to be inserted between the connector and printer cable. The EPSON DP-100 series printers requires the adapter.

The PX-4 internal character codes are the same as those of HX-20 and PX-8. Thus, a printer conforming to the HX/PX specifications is required when using the graphic codes.

A compact thermal printer P-40P which is battery-drivable is available as a model for sole use by PX-4.

In order to put the computer under the control of the PX-4 system program, the ~~keyboard~~ DIP switch needs to be set according character set sellection

to table 1-1.

If power failes in the PX-4, or power is turned off during a print, the print operation cannot be resumed by a Continue mode and some characters may be lost.

P/17 1.2.4 RS-232C Interface

When using an option device through an internal RS-232C interface, the ~~keyboard~~ DIP switch needs to be set according to table 1-1. The following option devices are available:

* Accoustic coupler: CX-20/21
* Terminal printer: Must conform to the RS-232C specifications.
* Memo printer: C-40, P-40S (for use by PX-8)
* Computer: PX-4/8, QX-10, HX-20

The following communication conditions are selected unless otherwise specified:

Baudrate:	4800 bps
Data format:	8 bits/character
Parity bit:	Not used.
Stop bit:	2 bits
Control line:	Not used.
XON/XOFF:	Not used.
SI/SO:	Not used.

This is a simplified RS-232C interface built with CMOS IC components so that the cable length is restricted. The interfacing conditions are as follow:

Output voltage: ± 5 V

Input voltage:	± 5 V - ± 15 V
Baudrate:	75 - 38.4K bps
Cable length:	1 m (standard)

P/18 1.2.5 Serial I/O (SIO) Interface

When using an option device through an internal serial I/O interface (SIO), the keyboard DIP switch needs to be set according to table 1-1. The following option devices are available:

* Floppy disk drives

  PF-10: 3.5-inch floppy disk drive (battery-driven)

  TF-15: 5.25-inch floppy disk drive

  TF-20: 5.25-inch floppy disk drive (for use by HX-20)

* Memo printers

  C-40: 40-column dot impact printer (battery-driven)

  P-40S: 40-column thermal printer (battery-driven)

... The SIO (interface) is a simplified version of the RS-232C interface. Thus, the memo printers can be connected to either interface.

The following communication specifications are set unless otherwise specified:

Baudrate:	38.4K bps
... Data format:	8 bits/character
Parity bit:	Not used.
Stop bit:	1 bit
Control line:	Not used.
... Protocol:	Provided.

The SIO interface is built with CMOS IC components which provides a higher data transmission speed. Thus; the cable length is restricted. The interface (~~specifications~~ ring conditions) are as follow:

Output voltage:	± 5 V
Input voltage:	± 5 V

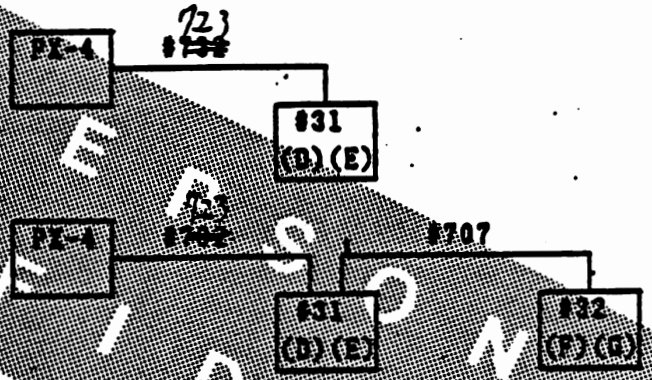
Baudrate: 75 - 38.4K bps

Cable length: 1 m (standard)

Floppy disk drives

PX-4 can connect up to two floppy disk drives of either TF-20 (for use by HX-20) or PF-10. The possible configurations are shown below.

- TF-20 - Set DIP switch to #31 or #31 and #32.



- PF-10 - Set DIP switch to D or D and F

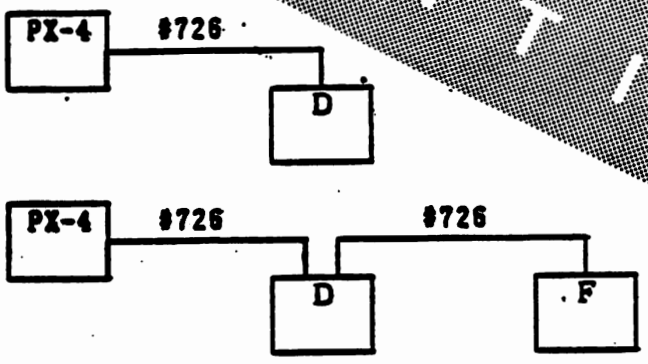


Fig 1-2. Option floppy disk drive configrations

The floppy disk drives are organized as follow:

320K bytes/drive

80 tracks/drive

16 sectors/track

256 bytes/sector

Maximum number of directories: 64

Capacity available for use by user: 278K bytes

1K bytes/access

The drives are assigned drive names D, E, F, and G - see fig. 1-2.

1.2.6 Cassette Recorder

An external cassette recorder can be optionally attached which can be controlled only by BASIC programs.

1.2.7 Barcode Readers (BCD)

PX-4 can connect a bar code reader which requires a special program.

The following models are available:

* HOOBR-JA (Resolution: 0.33 mm)
* HOOBR-HA (Resolution: 0.19 mm)

1.2.8 System Bus

The PX-4 system bus can connect an external RAM disk. It is attached to the computer frame with screws and can be used similarly to a floppy disk.

Two models with capacities of 64K and 128K bytes are available. One more 64K to 1M bit ROM chip can be added to the ROM capsule which can be used for data file.

The RAM disk unit uses the same DRAM components as main memory which are packed up by an incorporated Ni-Cd battery. The PX-4 access the unit through an I/O port.

A Ni-Cd battery is required for main PX-4 power source when the RAM disk unit is used. Unlike the RAM cartridge, this unit is not removable because memory data are lost.

When the unit is attached or removed, the PX-4 system needs to be initialized.

It is assigned a disk drive name A shared with the internal RAM disk which can be used only when no external RAM disk is attached. The RAM disks are organized as follows:

External RAM disk

8 tracks (numbered from 0 to 7)/disk (64K bytes)

16 tracks (numbered from 0 to 15)/disk (128K byte)

Internal RAM disk
5 tracks/disk (numbered 0~4)
64 sectors/track (numbered 0~63)
Max. number of directories: 16

..... 64 sectors (numbered from 0 to 63)/track

Maximum number of directories: 32

The internal RAM disk includes a part of main PX-4 RAM and a maximum capacity of 35K bytes can be specified. The internal RAM disk capacity is specified at system initialization. The standard capacity is 26K butes.

P/21-1 1.2.9 AC Adapter

The PX-4 AC adapter is rated at DC 6 V, 600 mA. It is completely compatible with HX-20 and PX-8.

1.2.10 ROM Capsule

A ROM capsule, which is a removable ROM carrier containing one or two ROM IC elements, can be easily installed in a special socket. The following ROM sockets are structured to

..... accept the ROM capsule:

* Main ROM: Can install 2 CMOS elements.

..... * ROM cartridge: Can install CMOS or NMOS elements.

* External RAM disk: Can install 1 CMOS element.

ROM is used for data files or contains programs. Data file ROM is installed in other than the main ROM socket. Either data file or program ROM can be installed in the main socket. As standard, so called BASIC ROM is installed in the main socket.

P/22 1.3.1 Option I/O Information Cables

The information cables required to all the option I/O devices are listed below.

Table 1-3. Option I/O infomation cables

Option device	Interface	Cable Assy No.	Proper model
Printer	Printer	#731	P-40P(for PX-4 use) - as terminal printer
	SIO	#723 #725	P-40S(for PX-8 use) - as terminal printer
	RS-232C	#723 #725	P-40S(for PX-8 use) - as terminal printer
Floppy disk drive	SIO	#723	TF-20 (TF-20 ⇔ PF-10 TF-15)
		#726	TF-15 PF-10 (PF-10⇔PF-10)
		#707	TF-20⇔TF-20
Acoustic coupler	RS-232C	#724	CX-20 CX-21
External cassette recorder	Cassette	#732	Audio cassette tape recorder
Computer	RS-232C	#726	PX-4 PX-8
		#738	HX-20
		#725	QX-10
RS-232C	RS-232C	#725	Modem

The cable assemblies and their order codes are listed in the following table:

Table 1-4. Cable list

Cable assy	Order code	Length
#707	Y202100300	1.0 m
#723	Y204080000	1.0
#724	Y204080100	1.0
#725	Y204080200	1.0
#726	Y204080300	1.0
#731	Y206040200	1.0
#732	Y206040400	0.75
#738	Y206040600	1.0

1.3.2 AC Adapters

The available AC adapters are listed in the following table together with their applied areas and order codes:

Table 1-5. AC adapters

AC voltage	Model	Applied area	Order code
100 V	H00AAJ	Japan	X510600020
120	H00AAA1	U.S.A. and Canada	X510600010
	H00AAA2	Taiwan and Korea	X510600110
220	H00AAG1	Germany and neighboring areas	X510600060
220	H00AAE1	France and southern Europe	Y201515000
240	H00AAU-A	England	Y201517000
240	H00AAC-B	Oceania	Y203522000
240	H00AA02	Hongkong and Singapore	X510600100

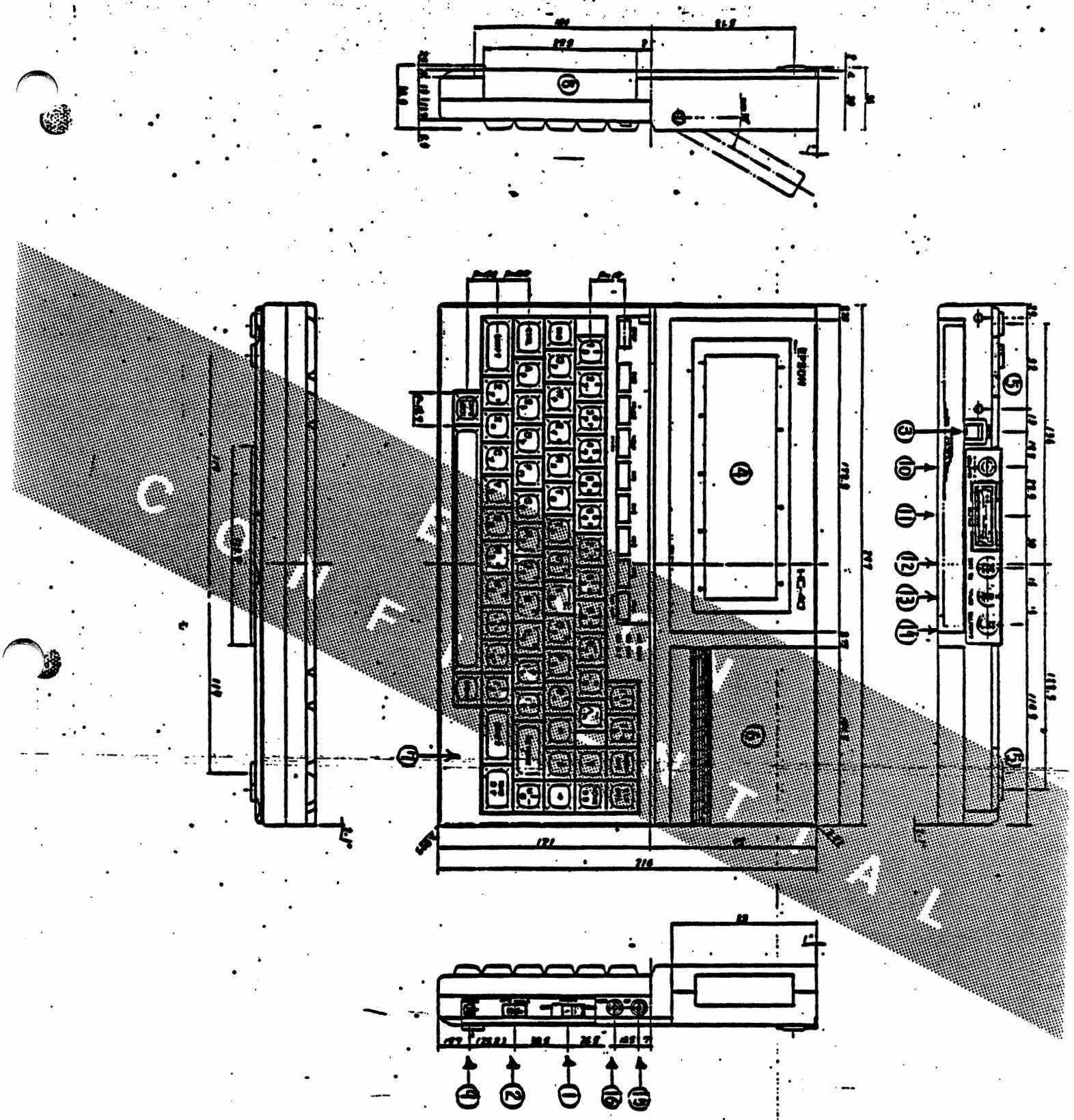


Fig. 1-3. PX-4 dimensions - unit: mm

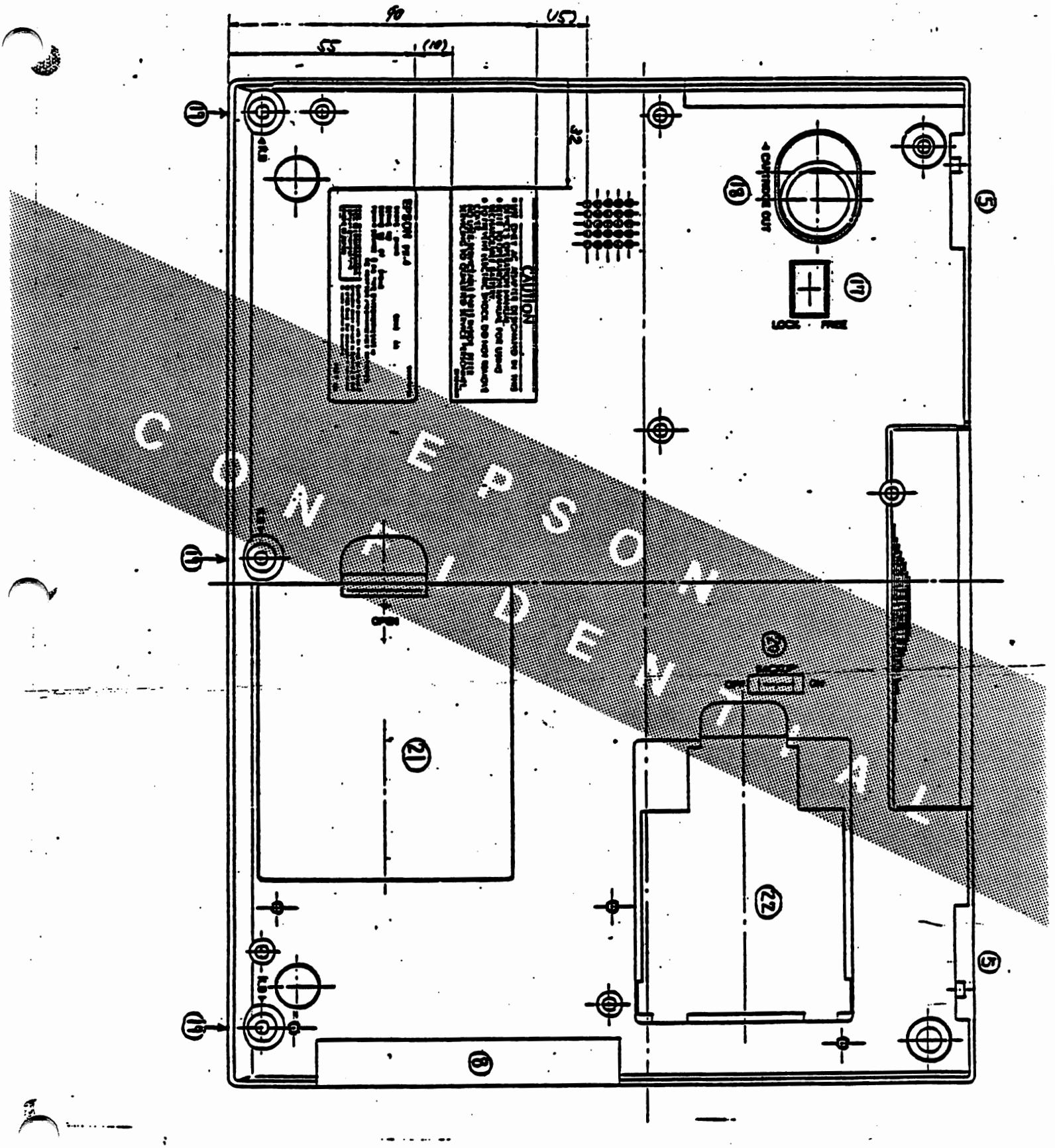


Fig. 1-4. Bottom battery housing

1.4 External ~~Components~~ Mechanical Elements

The ~~external components~~ (mechanical elements) and their purpose and usage are explained here according to the numbers in figs. 1-3 and 1-4.

(1) POWER switch - PX-4 is turned on when this switch is set ON. However, power may be lost even while the switch is ON.

(2) VIEW ANGLE adjustment knob - Allows display contrast adjustment.

(3) PUSH button - Display panel angel can be adjusted by raising the back end of the display unit while pushing this button.

(4) Display unit - Provides the 40 characters by 8 lines LCD panel.

(5) Legs - An angle can be given to the top computer panel by picking these legs down.

(6) Dummy cartridge - Serves as a dummy when the option cartridge is used. It is replaced with the actual cartridge when used.

(7) Keyboard unit (Japanese) - This is the kana character version of the standard keyboard which can be replaced with the item keyboard.

(8) System bus connector cover - Can be removed by pulling it out. A system bus I/O device can be connected to the receptacle behind this cover.

(9) RESET switch - This fool-proof switch can be accessed with a bar such a pencil tip. Pressing this it causes the PX-4 circuit to be reset. This switch is used in cases such as program run away, etc.

(10) ADAPTOR receptackle - The AC adaptor plug is inserted here.

P/27 (11) PRINTER cable connector receptacle - ~~Used to~~ connect a Centronics-compatible printer via a special cable assembly.

(12) RS-232C cable connector receptacle - ~~Used to~~ connect an (interface)

option devices such as acoustic coupler and printer, etc.

(13) SERIAL interface cable connector receptacle - ~~Used to~~ connects option devices such as floppy disk drive and printer, etc.

(14) CASSETTE recorder interface cable connector receptacle - ~~Used to~~ connects an external cassette recorder.

(15) SP (external speaker) output jack - Used for microcassette disk drive azimouth adjustment.

(16) BCR (barcode reader) cable connector receptacle - Connects a barcode reader.

(17) LOCK/FREE knob - Locks/unlocks the cartridge cover to/from the computer body.

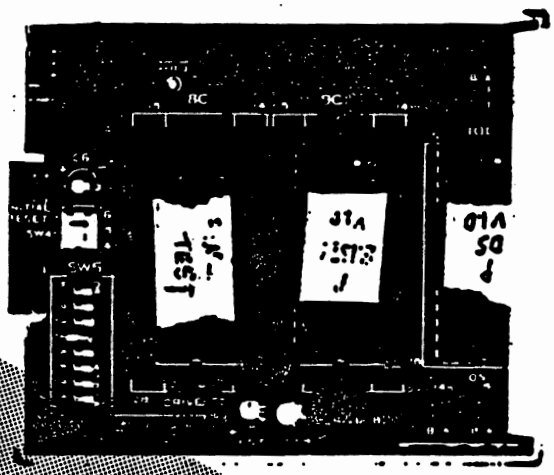
(18) CARTRIDGE OUT lid - Allows the cartridge to be removed from the computer by pulling this lid out.

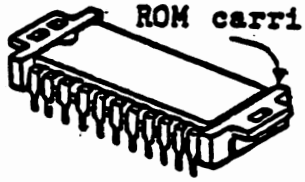
(19) Screws (3) - Clamps the keyboard. The keyboard can be replaced by removing these screws. They can be loosened and tightened with a coin.

(20) BACKUP battery discharge-proof switch - Used to prevent incorporated Ni-Cd battery discharge. This switch should be normally ON (it is set OFF for shipment only).

(21) ROM capsule box cover - Allows access to the ROM components for replacement and the initial reset switch.

The components inside ROM capsule box and ROM component replacement are explained below.





ROM capsule

Fig. 1-5. ROM capsule box

- SW3 DIP switch assembly - The individual switches are assigned as follow :

1	ON	5	OFF	ON	OFF ON
2	ON	6	OFF	OFF	ON ON
3	ON				
4	ON				

ASCII

- Printer
- RS-232C
- Cartridge
- SIO

7 Not used.
8 Not used.

Switches 1 - 4 specify one of various language character sets.

Switches 5 and 6 specify a connector to which the output data are directed.

Whenever either switch group is reset, the reset switch must be pushed.

. SW4 initial reset switch

This switch is pushed when:

A. The program runs away and a recovery trial by the reset switch fails.

B. Power is not removed by resetting the power switch OFF.

C. The battery voltage drops and PX-4 is not powered by connecting the AC adapter.

D. The system fails to normally operate.

When pushed, the Initial Reset switch loses all PX-4 data. This switch should not be used except when recovery fails with the Reset switch.

The system can also be re-initialized by pushing the Reset switch while holding down the two keys GRPH and SHIFT at the right of the keyboard.

. Replacing the ROM component(s)

Before installed, the ROM component is put on a ROM carrier. Then, it is inserted to the socket as mounted on the carrier with power removed. When mounting the ROM on the carrier, take note of the polarity mark for correct polarity.

8K, 16K, and 32K byte mask ROM ~~components~~ elements are available to be used in the ROM capsule. P-ROM ~~components~~ elements 27C64 (8K bytes) and 27C256 (32J bytes) can be used in the capsule. When an 8K byte ROM is used, the jumper plugs J5 and J4 must be reset according to the following:

Table 1-6.Jumper plug setting

DRIVE B	32KB,16KB	Jumper B and open A -standard setting.
J5	8KB	Open B and jumper A.
DRIVE C	32KB,16KB	Jumper B and open A -standard setting.
J4	8KB	Open B and jumper A.

The standard configuration installs the BASIC ROM component in drive B and leaves drive C empty.

BASIC ROM may be installed as either drive B or C. Only the difference is the drive name.

User programs should be written in a CMOS P-ROM which is available as after service parts which also include necessary ~~components~~ elements such as ROM carrier, etc.

P/30 (22) Battery box cover

The battery can be accessed for replacement by removing this cover.

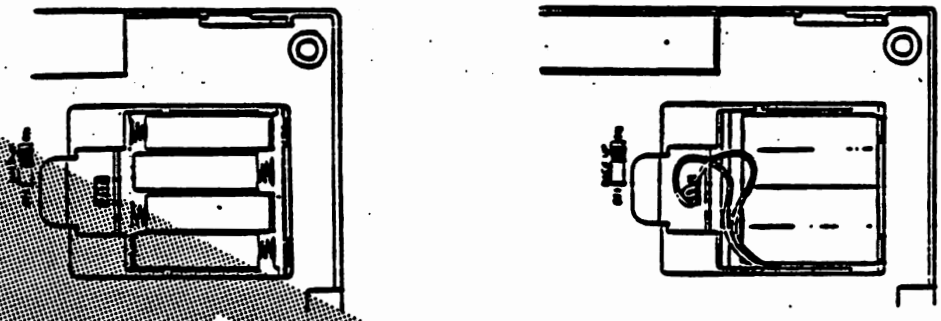
Notes on the batteries and their replacement are summarized in the following:

. Replacing the batteries

Four manganese batteries or a Ni-Cd battery unit is installed in the battery box. Fig. 1-6 illustrates the battery installations.

When a cartrisge printer or microcassette drive is used,

the Ni-Cd battery unit must be installed. Especially for the cartridge printer, the proper performance cannot be ensured without the Ni-Cd battery unit.



Manganese batteries Ni-Cd battery unit

Fig. 1-6. Battery installations in the battery box

Because of considerations for simplest battery replacement, the currently used Ni-Cd battery unit can be replaced, whenever exhausted, with manganese batteries, and the interrupted PX-4 operation can be resumed; RAM is backed up by a sub-battery during main battery replacement.

The standard PX-4 configuration can be used for from four to five hours with the manganese batteries or Ni-Cd battery unit after replaced.

The sub-battery provides a capacity which back up PX-4 RAM for six days (150 hours). RAM is normally powered by both the main and sub-batteries.

The PX-4 batteries continue discharge for backing up RAM even while the POWER switch is OFF. Thus, the batteries need to be replaced or recharged once a month if the PX-4 is not used. If this cannot be ensured, the RAM cartridge should be used.

Power supply combinations

PX-4 can be powered by three supplies which can be combined as follows:

Table 1-7. Possible power supply combination

Combination						Power supply
F	E	D	C	B	A	
	○	○		○		AC adaptor
				○	○	Manganese batteries
		○	○			Ni-Cd battery unit
○	○	○	○	○	○	Auxiliary battery

A. ~~A standard combination~~ This used when no AC-source is available.

B. ~~Another standard combination.~~ However, this combination uses the AC adaptor to minimize battery consumption. No battery discharges while the adaptor is connected to the AC source. The batteries are used only while the AC source is interrupted.

EPSON EPSON CORPORATION	TITLE	SHEET REVISION	NO. 31
			NEXT SHEET

C. A standard condition
This combination is used when the option microcassette drive or cartridge printer is used. Because of its high internal impedance, increase in load current causes a larger voltage drop and shortens battery life.) The Ni-Cd battery can be discharged and recharged 500 times or more. It requires eight recharge hours. (The Ni-Cd battery unit is counted in expendables.)

D. This combination is best suitable when it is desired to continue PX-4 operation if the AC source is interrupted while recharging the Ni-Cd battery. The Ni-Cd battery can be continously charged for one year or more.

E. This combination is used when using PX-4 only with the AC adaptor. The sub-battery can back-up RAM for about six days with the POWER switch OFF. However, the sub-battery must be charged for 30 hours or more before.

F. The back-up battery, which is incorporated in the computer, is devoted for RAM back-up, and cannot support computer operation alone.

1.5 PX-4 Operation Procedures

1.5.1 System Initialization

(First system initialization after unpacking)

(1) Reset the POWER switch OFF.

(2) Set the Back-up switch ON.

(3) Install the main manganese batteries or Ni-Cd battery unit.

(System resetting for recovery from uncontrollable state)

(4) Push the Initial Rest switch.

(5) Set the POWER switch ON.

(6) Adjust the VIEW ANGEL knob.

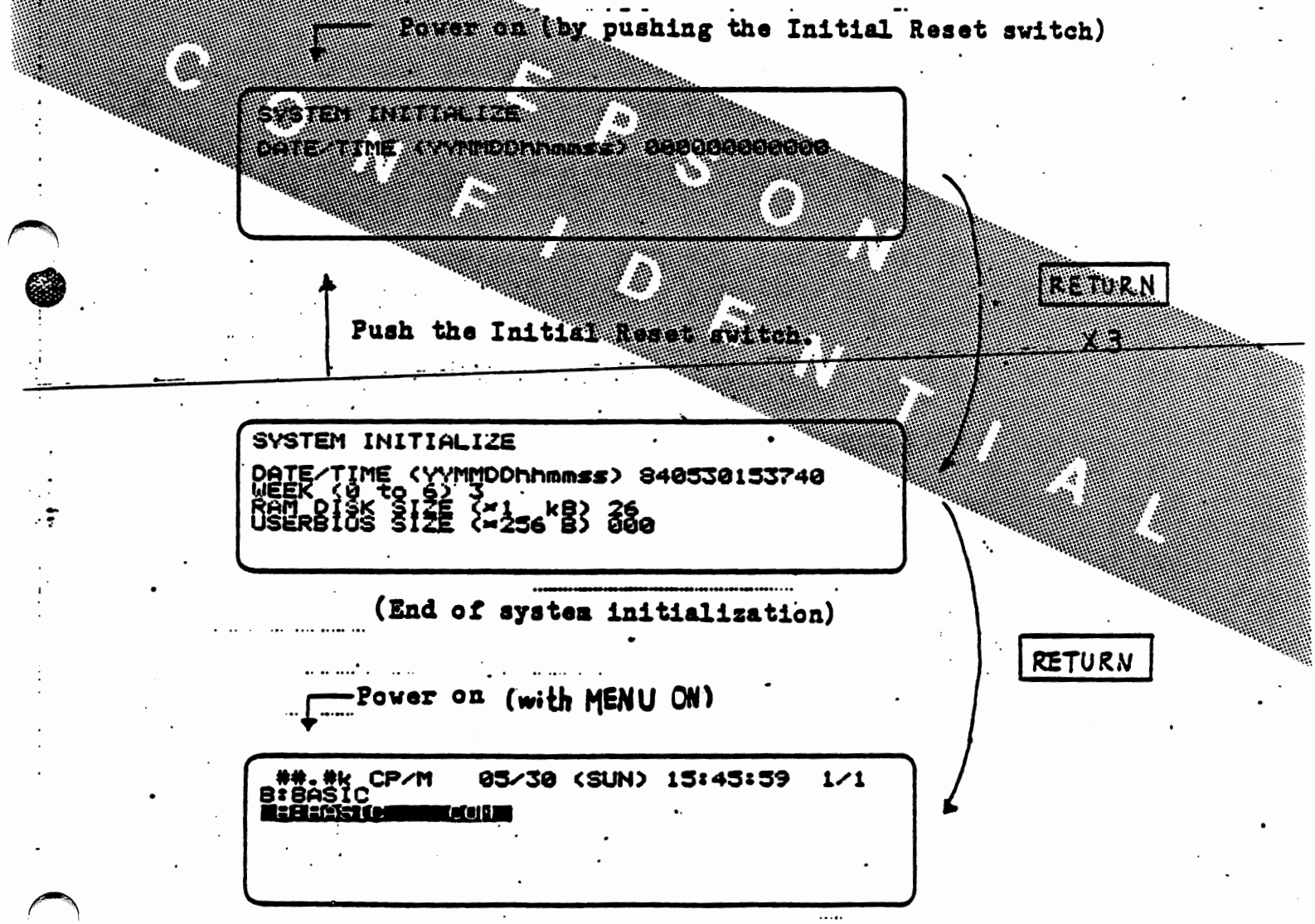


Fig. 1-7. System initialization

1.5.2 Starting the BASIC Processor

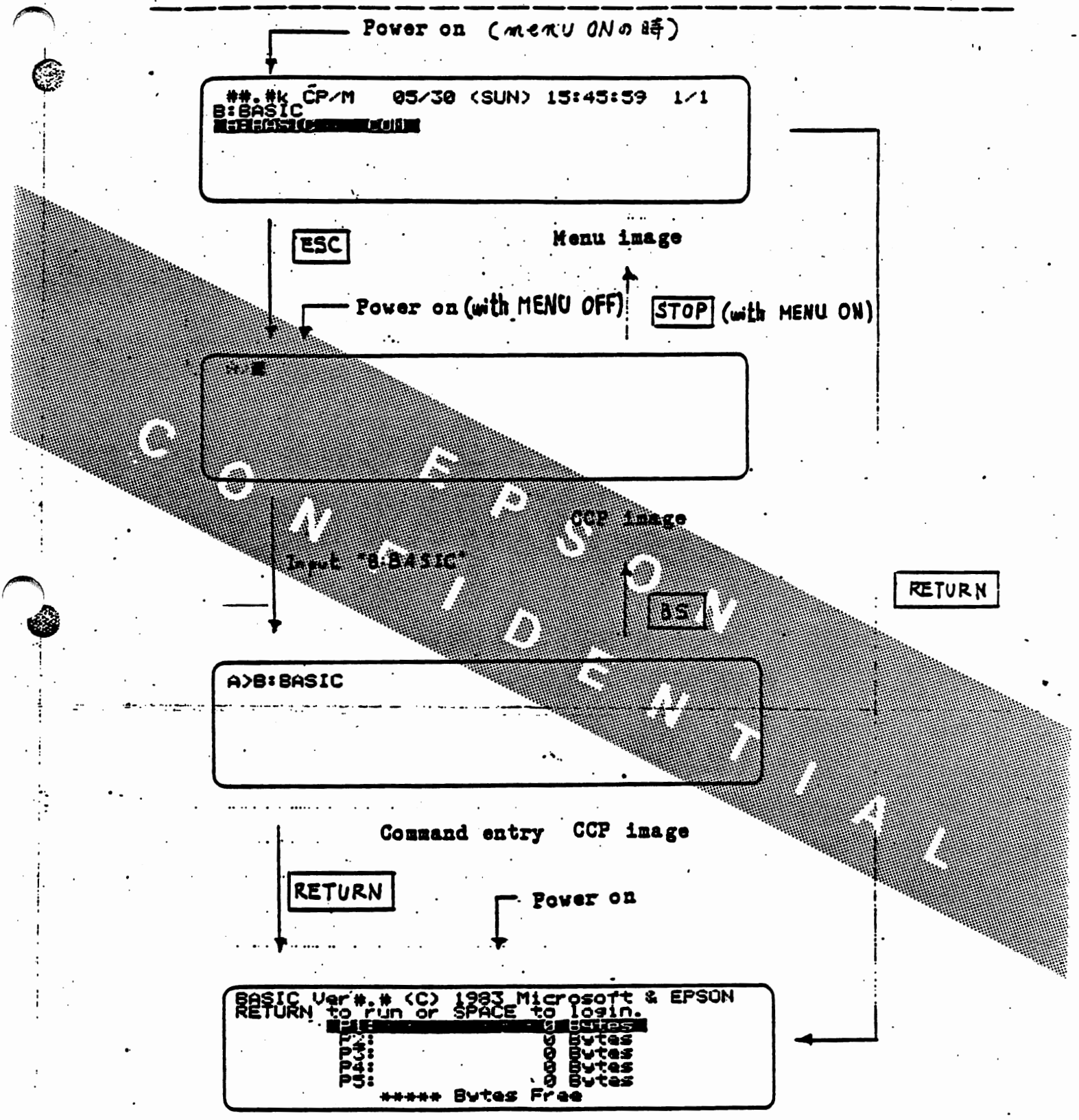
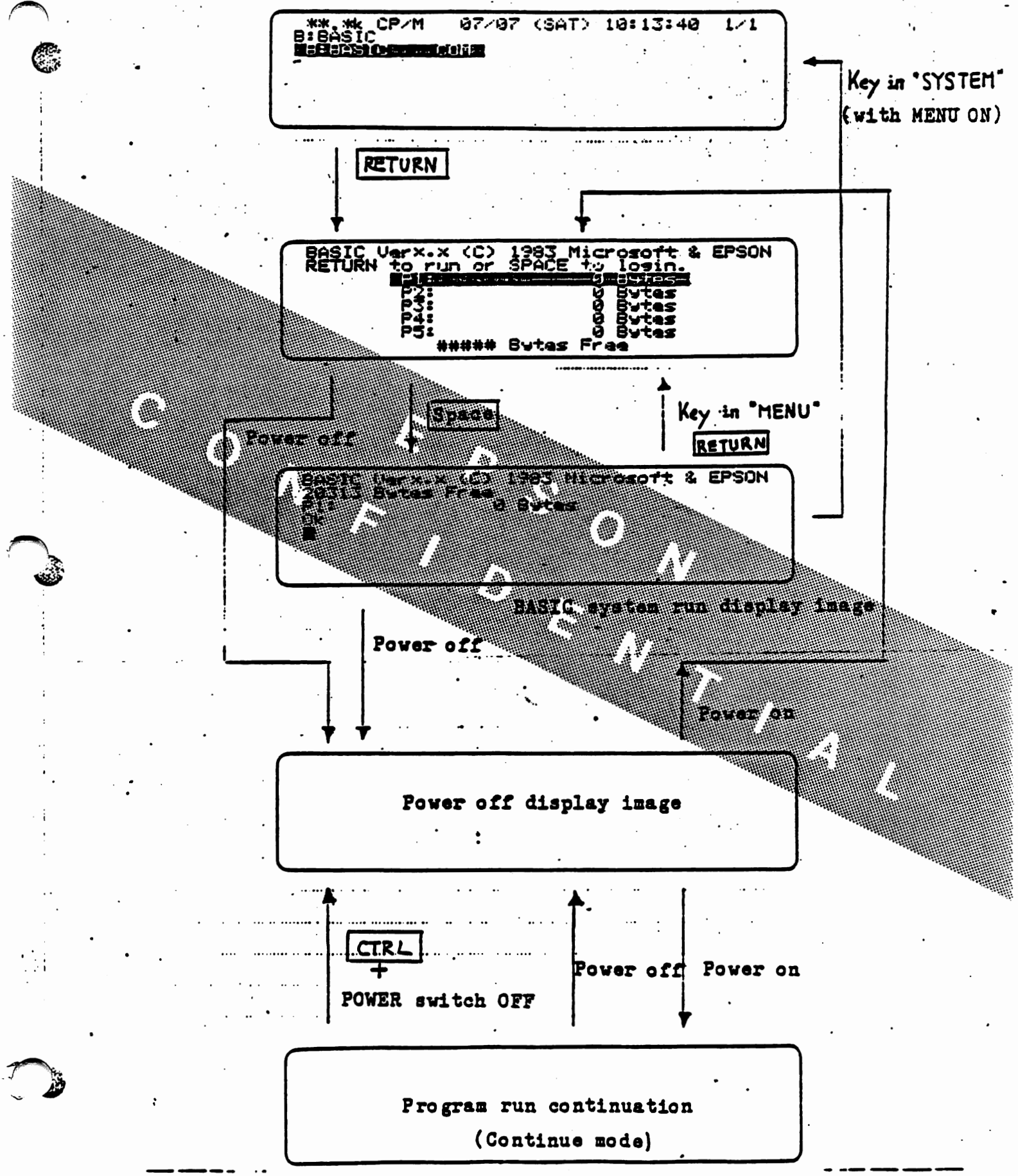


Fig. 1-8. BASIC processor startup

1.5.3 Display Image Selection



1.5.4 Menu Selection (System Display)

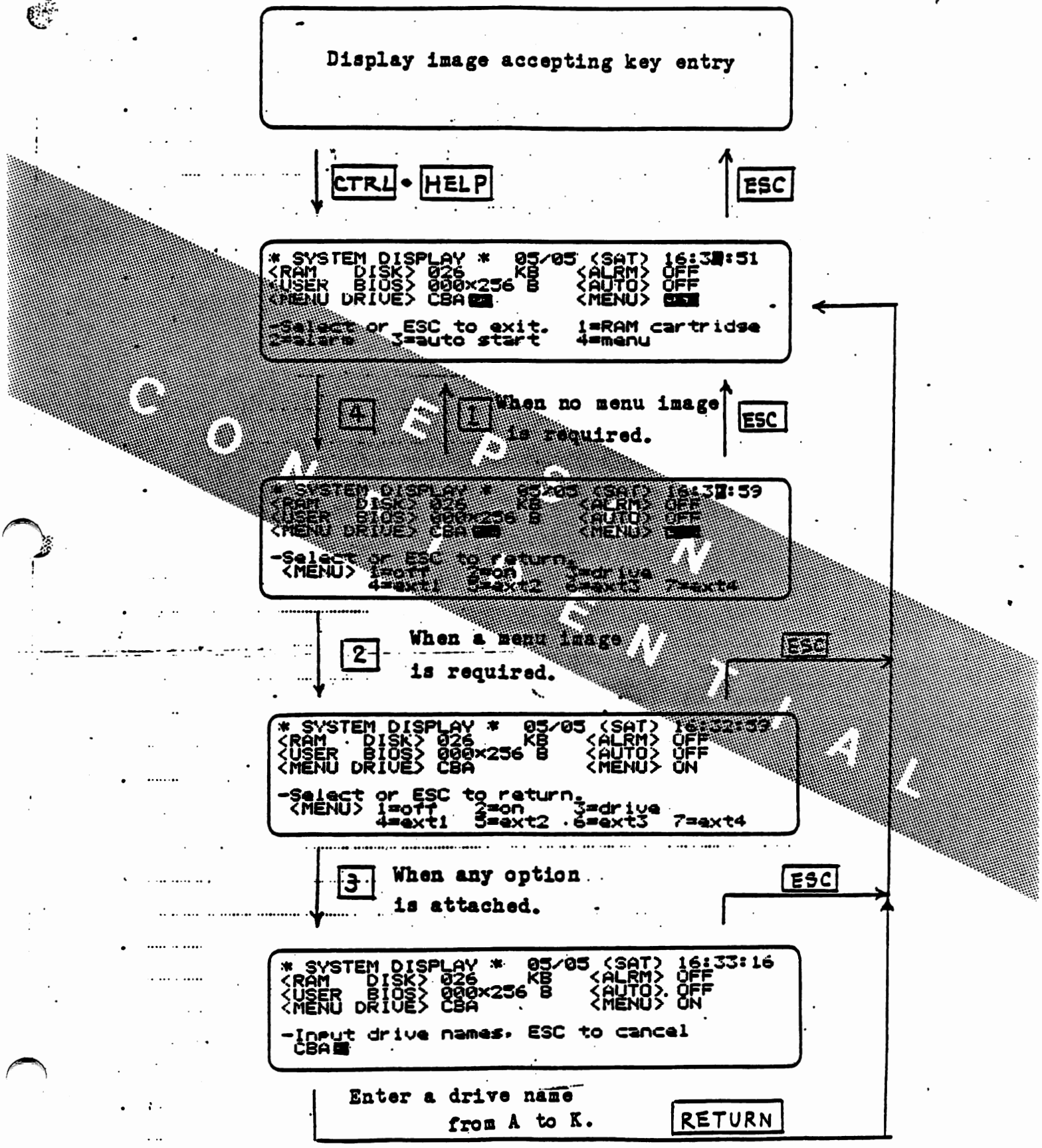
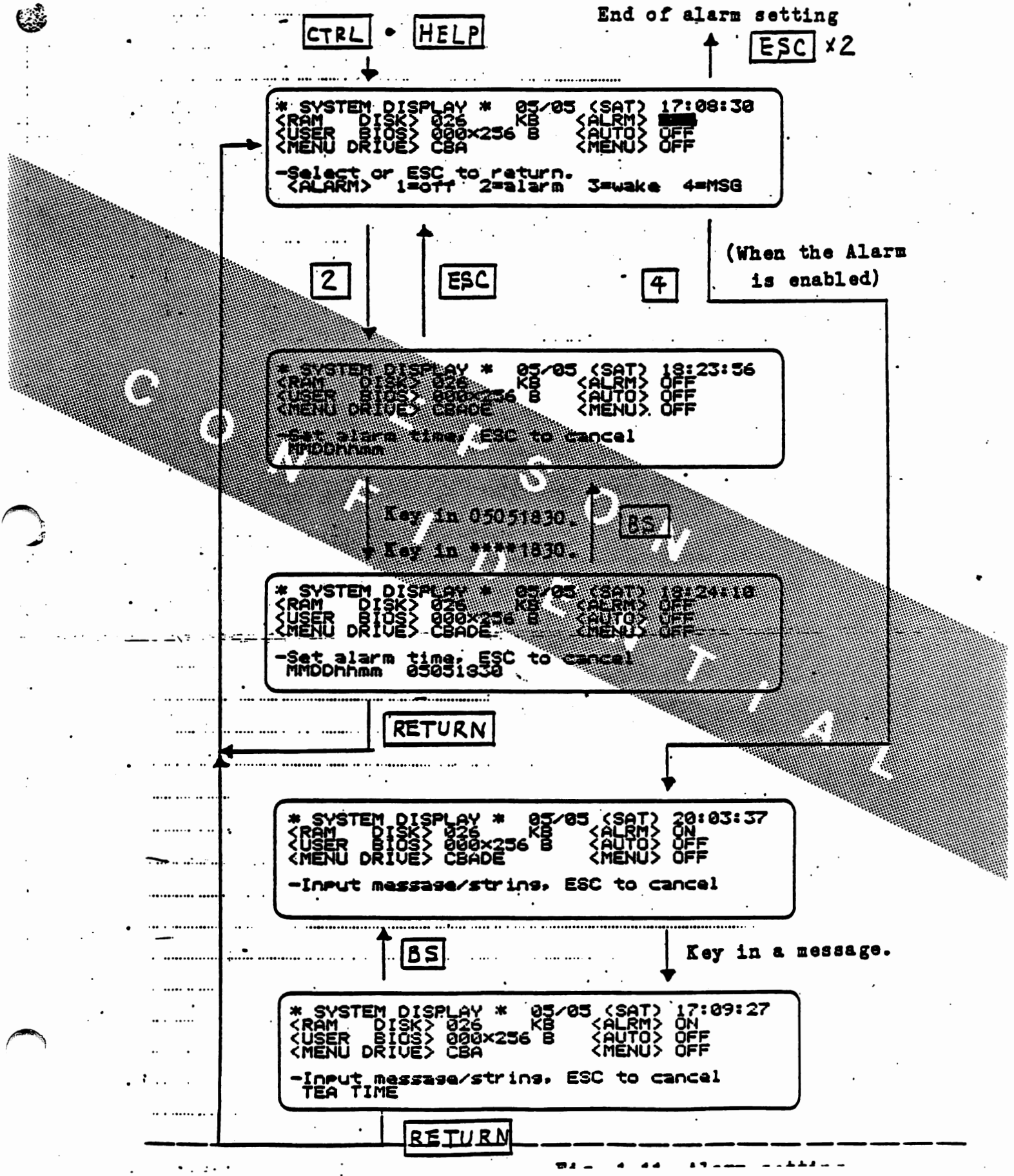


Fig. 1-10. Menu selection

1.5.5 Alarm Setting



1.5.6 Wake Setting

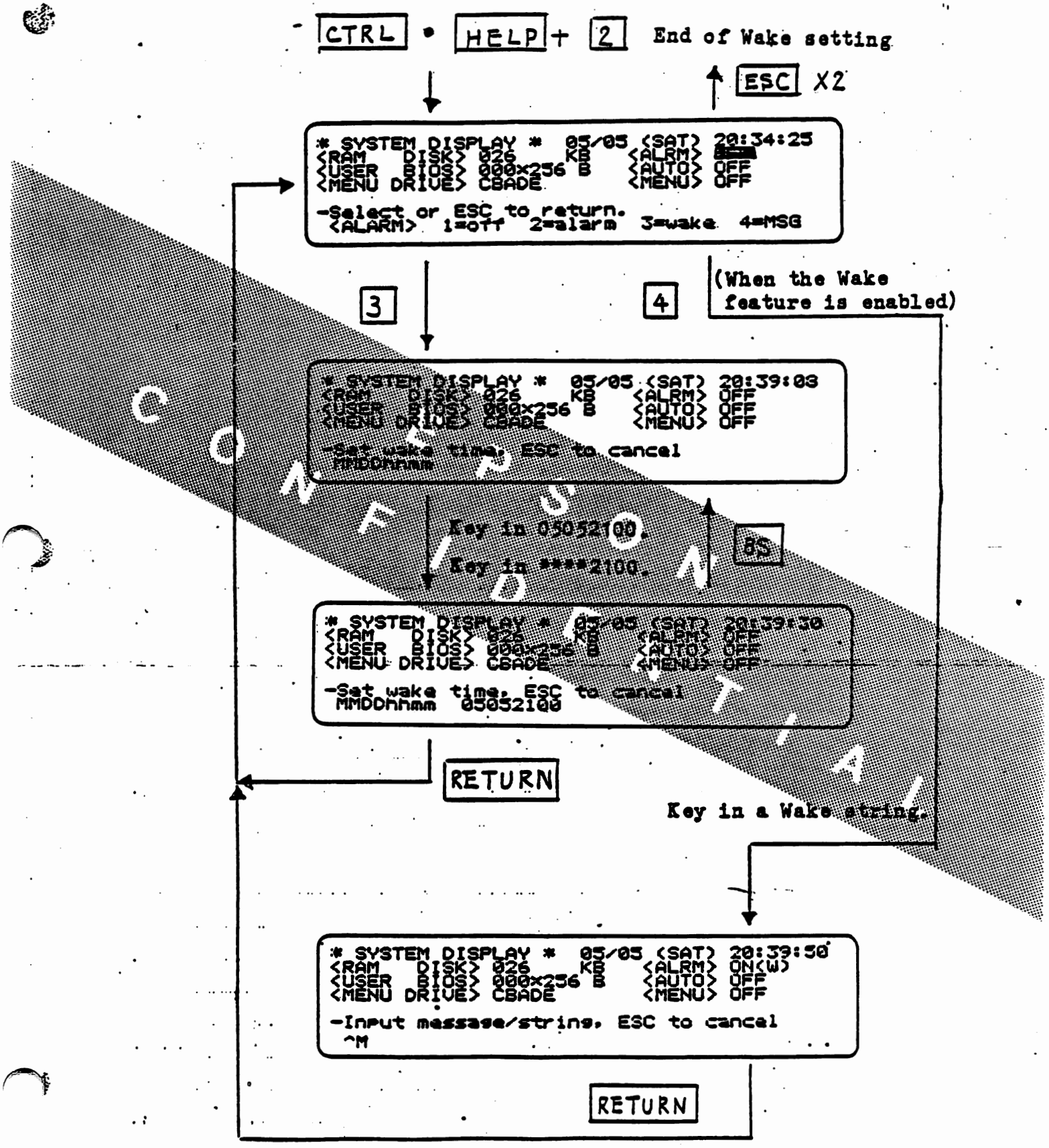


Fig. 1-12. Wake setting

1.5.7 Auto Start Setting

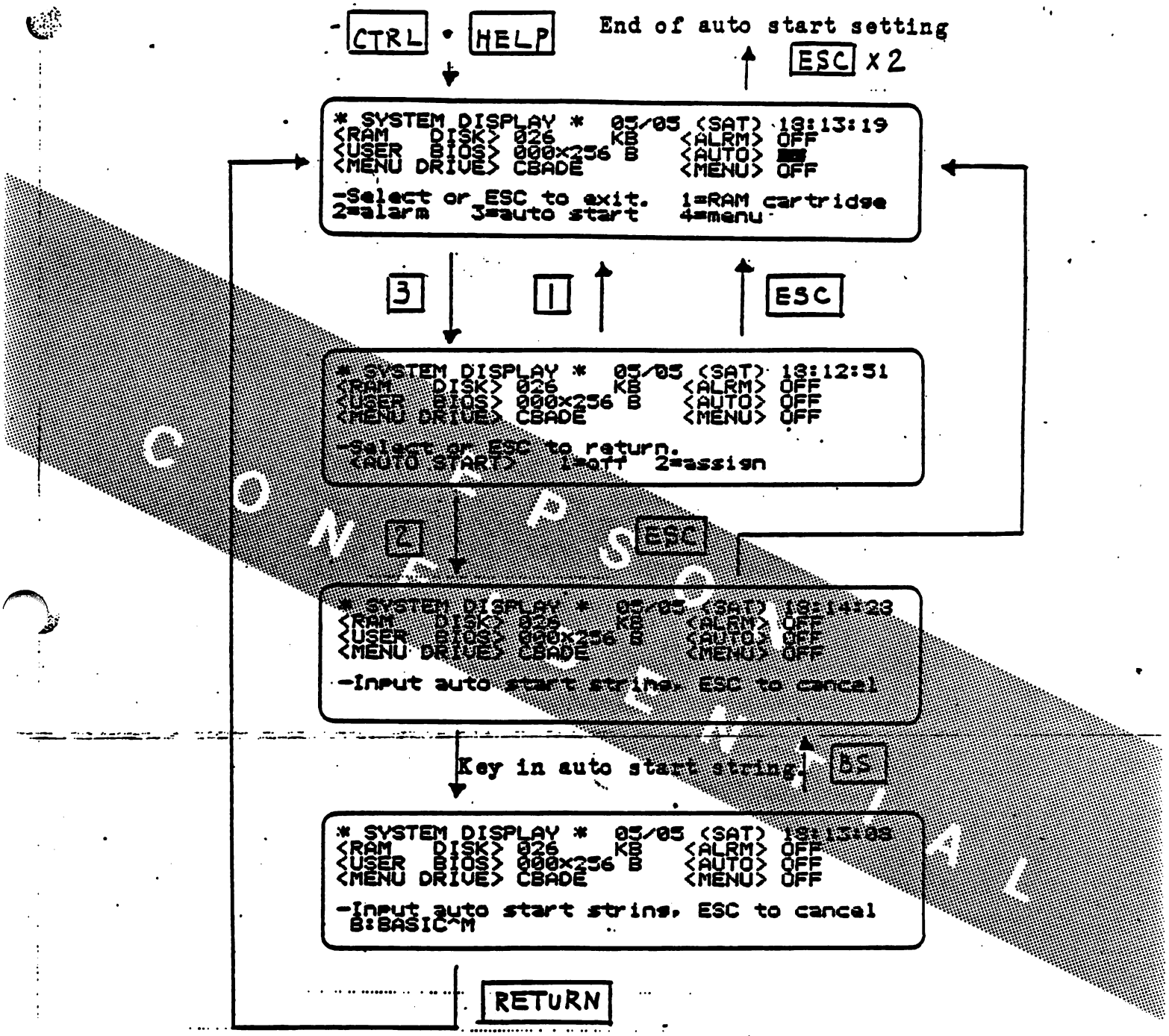


Fig. 1-13. Auto start setting

1.5.8 Auto Start And Wake Strings

An Auto Start string and a Wake string can replace can replace a sequence of key entries required after turning on PX-4. That is, an Auto Start string and Wake string are strings of commands which would otherwise be keyed in to start a particular program after power on; the strings respectively provide automatic system start and system wake ~~capabilities~~ *capabilities*.

The key switches which need to be pressed to start a user program and how to create the corresponding strings are summarized in table 1-8. When the Wake feature is used, PX-4 is not turned off until the POWER switch is reset OFF or Power-Off command is executed within the program.

Table 1-8. Auto Start and Wake string

CP/M ~~name~~

	Key string elements
→	^ + \
↓	^ + [
←	^ +]
↑	^ + ^
RETURN	^ + M
ESC	^ + [

Ascii コードの時のみ. 他の時もある.

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BASIC menu

↓	^ + _
↑	^ + ^
SPACE	SPACE + □
RETURN	^ + M

Note: This table is used for only ascii keyboard when using another keyboard there are some changes in this table.

1.5.9 System Messages

(1) Alarm Time message

When it comes across the specified alarm time with the time-alarm feature enabled, the following message appears on the display panel accompanying an alarm sound.

```
<ALARM TIME>    05/05   13:20
" WE HAVE DINNER "
        Press ESC key
```

(2) Low battery voltage warning message

When the main battery voltage drops below a certain limit, the following message appears. Turn PX-4 off and replace the battery.

```
CHARGE BATTERY
```

(3) RAM disk formatting request message

If the following message appears when the POWER switch set ON or the reset switch is pushed, key in "Y" and reformat the RAM disk.

```
RAM DISK FORMAT (Y/N) ?
```

1.5.10 ROM Cartridge

The ROM IC components on the ROM cartridge are assigned drive names J and K.

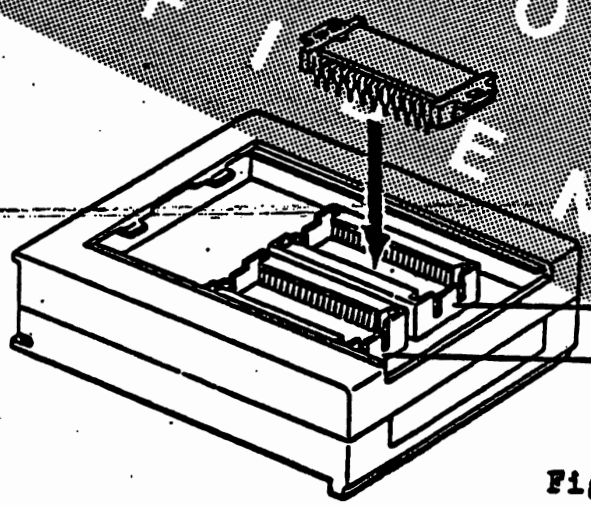

Fig. 1-15. ROM cartridge

Therefore, key the following when reading a program from the cartridge:

A>J: filename, or

A>K: filename

1.5.11 RAM Catridge

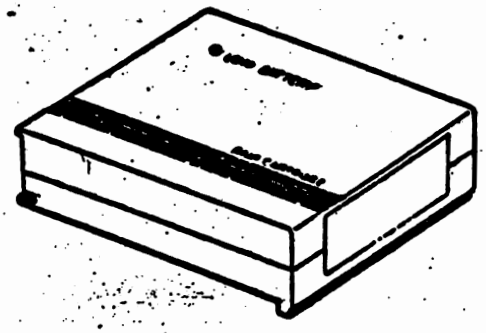

Fig. 1-16. RAM cartridge

The RAM cartridge must be formatted before it can be used. Once formatted, no further formatting is required until stored data are destroyed.

The cartridge is formatted by the following key entry:

CTRL + HELP + 1 or 2

```
* SYSTEM DISPLAY *    03/05 <SAT>  14:41:39
<RAM   DISK> 026    KB    <ALARM> OFF
<USER  BIOS> 000×256 B    <AUTO> OFF
<MENU DRIVE> ABC          <MENU> ON

-Select or ESC to return.
 <RAM FORMAT>   1=no   2=yes
```

Fig. 1-17. RAM formatting procedure

The RAM cartridge is operated as follows:

(1) Under ~~the~~ CP/M system

The cartridge is assigned drive name I. Thus, it is selected by keying in:

A>I:

(2) Under ~~the~~ BASIC system

When saving a program to the cartridge, key in:

SAVE "I:filename"

When loading a program from the cartridge, key in:

LOAD "I:filename"

1.6 Specifications

1. Dimensions: 297 (wide) x 216 (deep) x 34 (high) mm^3
2. Weight: Approx. 1.6 kg
3. Environmental requirements
   * Temperature

Operating:	5°C - 35°C
Charging:	5°C - 35°C
Data storage:	0°C - 40°C
Storage:	-20°C - 60°C
Long term storage:	-20°C - 30°C

   * Humidity (relative)

Operating:	10% - 80% (No condensation allowed)
Storage:	10% - 85% (No condensation allowed)

   * Vibration

Operating:	Must not exceed 0.25 G at 55 Hz
Non-operating:	-

	Non-packing	Packing
Amplitude (mm):	2	2
Frequency (cpm):	1000	1000
Directions:	X, Y, Z	Up down
Duration (min.)	30 in any direction	30

* Shock

Operating: Must not exceed 1 G and 1 G must not last longer than 1 ms.

Non-operating:

Non-packing: Put the computer body on a 3 cm thick flat-surfaced wood plate. Raise the four sides 10 cm above the floor and naturally drop five times each side.

No abnormality should not be observed in external appearance, construction, or general functions.

Packing: Pack the computer at the minimum level. Naturally drop the package on a concrete floor from a height of 50 cm, once with each of the three faces of the left and right sides and the top and bottom faces down.

No abnormality should be observed in external appearance, construction, or general functions.

P/45 4. CPUs and Memory

* Main CPU - Z-80 compatible CMOS CPU

Clock rate: 3.68 MHz

RAM: 64K bytes

ROM: 32K bytes

ROM capsule: Max. 64K bytes

* Slave CPU - 7508 4-bit CMOS CPU

Clock rate: 270 KHz

Internal ROM: 4K bytes

5. Power Supplies

* Main supplies

4 unrechargeable unit-3 dry batteries, or

Ni-Cd battery unit

Capacity: 450 mAH

Nominal output voltage: 4.8 V

Charge current: 70 MA

Charge time: Approx. 8 hours (when turned off), and/or

AC adaptor - DC 6 V, 600 mA

* Sub-battery - Ni-Cd battery

Capacity: 90 mAH

Nominal output voltage: 4.8 V

Charge current: 3 mA

6. Keyboard

* Standard keyboard

Number of keys: 72 typewriter-type keys (including 9 function keys)

Mode indication: Modes are indicated by 3 LEDs.

* Item keyboard

Number of keys: 58

Mode indications: Modes are indicated by 3 LEDs.

7. LCD Unit

Display capacity

Character mode: 40 column by 8 lines

Graphic mode: 240 x 64 dot matrix

Character font: 6 x 8 dot matrix

8. Buzzer

Volume-unadjustable piezoelectric buzzer

9. ROM capsule

Number of slots: 2

Maximum capacity: 32K bytes/slot

ROM components that can be installed (CMOS)

P-ROM: 27C64, 27C256

Mask ROM: 31364, 613128, 613256

10. RS-232C Interface

Signal levels: RS-232C levels (+5 V)

Data transmission rate

Same rate both for transmission and reception:

110, 150, 200, 300, 600, 1200, 2400, 4800, 9600, 19200,

38400 bps

Maximum difference between transmission and reception:

1200/75 or 75/1200 bps

Transmission character format

Start bit: 1 bit

Stop bit: 1 or 2 bits

Data length: 8 bits

Parity bit: Used or not used.

11. Serial Interface

Signal levels: RS-232C levels (± 5 V)

Data transmission rate:

Same rate for both transmission and reception:

110, 150, 200, 300, 600, 1200, 2400, 4800, 9600, 19200, 38400 bps

Maximum difference between transmission and reception:

1200/75, 75/1200 bps

Transmission character fromat

Start bit: 1 bit

Stop bit: 1 or 2 bits

Data length: 8 bits

Parity bit: Used or not used.

12. Printer Interface

Conforms to the Centronics specifications.

13. External Audio Cassette Interface

Data transmission rate: Approx. 1300 bps

Remote-controllable.

14. Barcode Reader Interface

High resolution: 0.19 mm

Low resolution: 0.33 mm

15. Cartridge Interface

A parallel or serial transmission interface for connecting an option cartridge such as the RAM cartridge, ROM cartridge, microcassette disk, or measurement unit.

16. System Bus

Address bus: 16 bit wide

Data bus: 8 bit wide

CHAPTER 2 PRINCIPLES OF OPERATIONS

2.1 Standard PX-4 Hardware Configuration

The standard PX-4 hardware configuration is shown in fig. 2-1 and the standard components are shown in photographs from figs. 2-2 to 2-10.

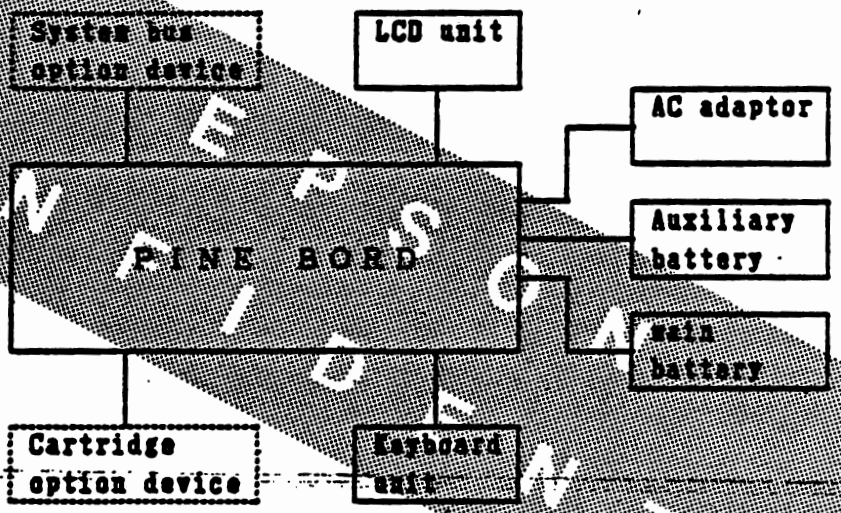

Fig. 2-1. Standard PX-4 configuration

(1) Major circuits are collected on a single board PINE.

(2) The keyboard unit is built with key switches and light emission diodes. There are the two types of keyboard units; standard and item, are available for user's selection. The two units are compatible to each other.

(3) The LCD (Liquid Crystal Display) unit is consists of an LCD panel and an LCD drive circuit.

(4) The PX-4 AC adaptor is completely compatible with those for EPSON HX-20 and PX-8.

(5) The sub-battery is incorporated in the computer. This Ni-Cd battery is solely used by PX-4.

(6) Manganese dry cell batteris or a Ni-Cd battery unit can be used as the main battery. The Ni-Cd battery unit is solely used by PX-4.

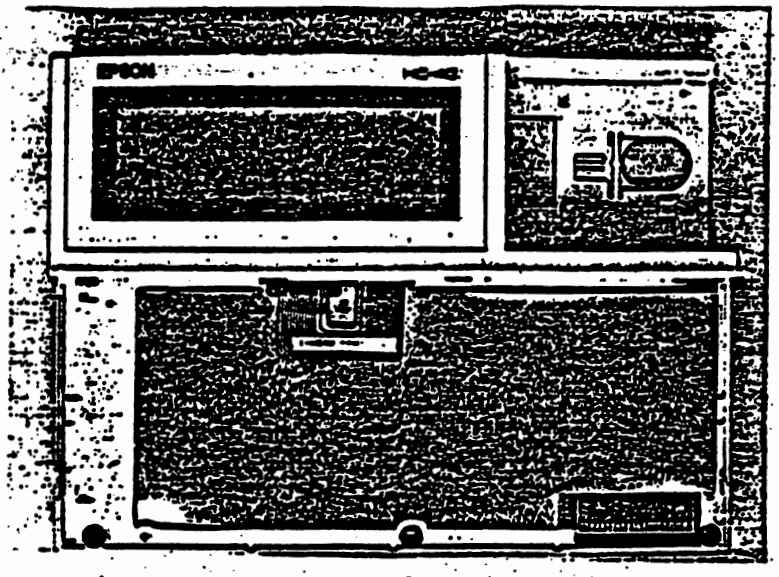

Fig. 2-2. Top computer view as the keyboard unit removed

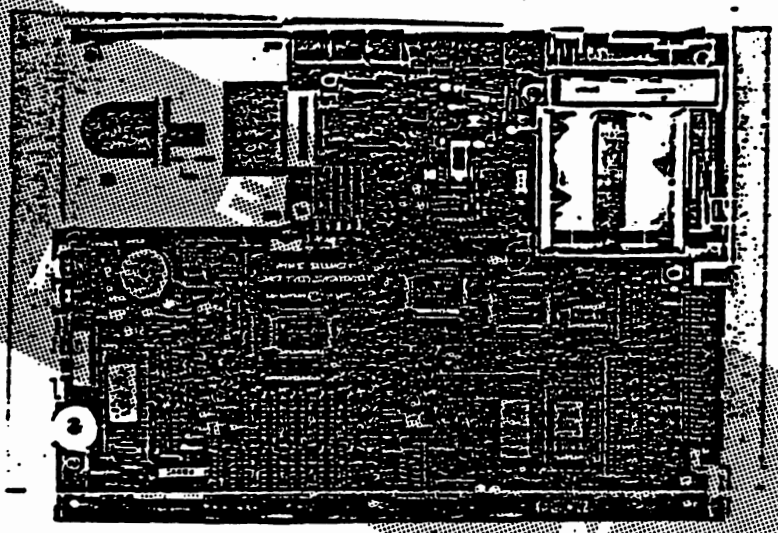

Fig. 2-3. PINE board - element mounting side as the bottom case removed

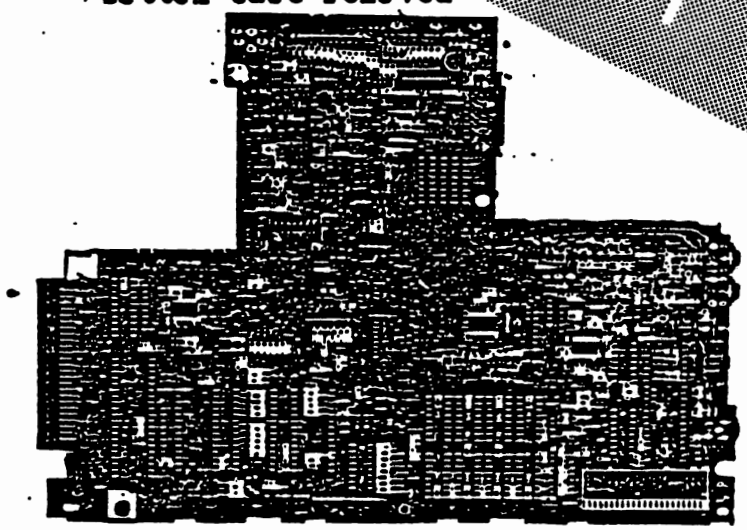

Fig. 2-4. PINE board - wiring side

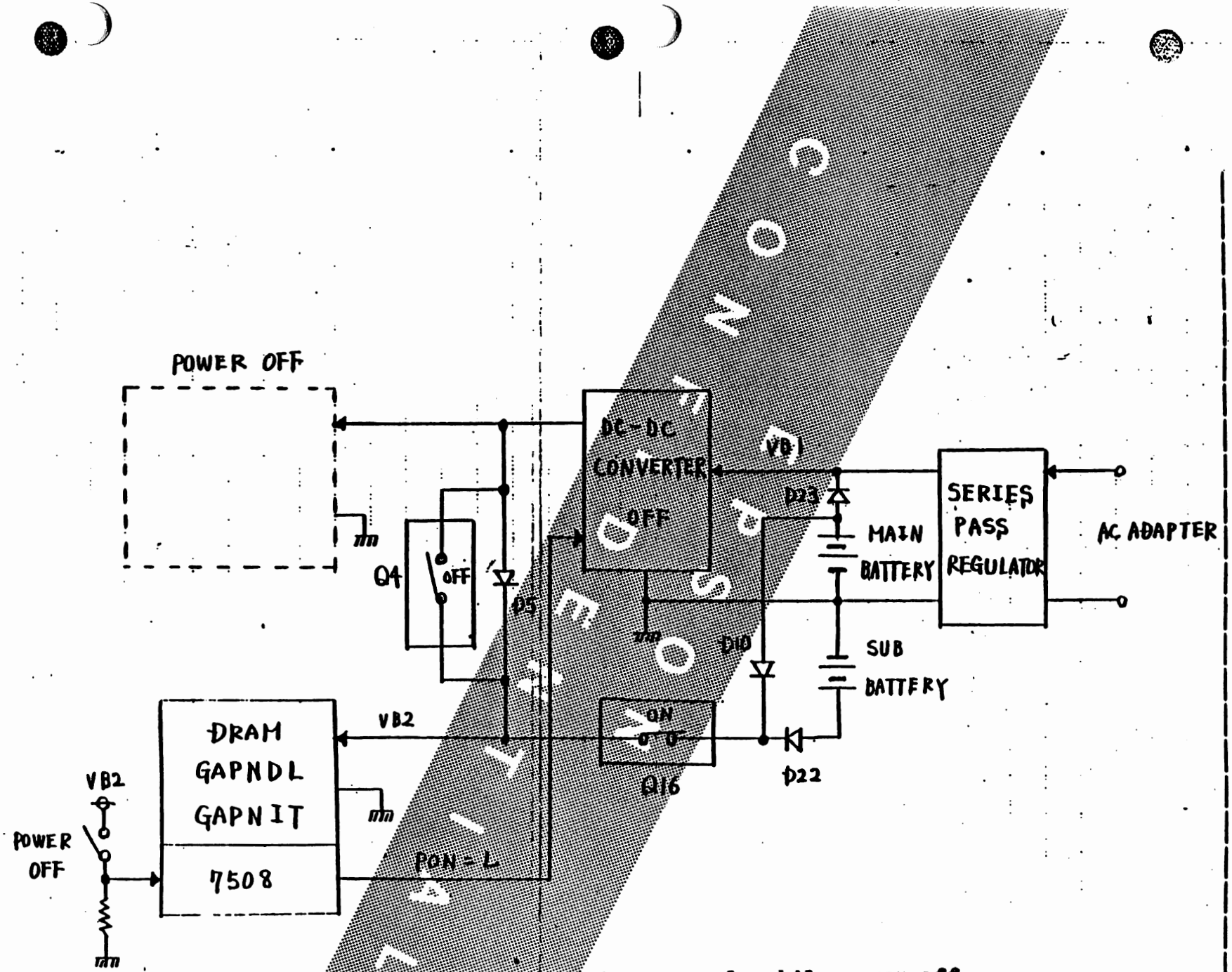

Fig. 2-28. Power supply while power off

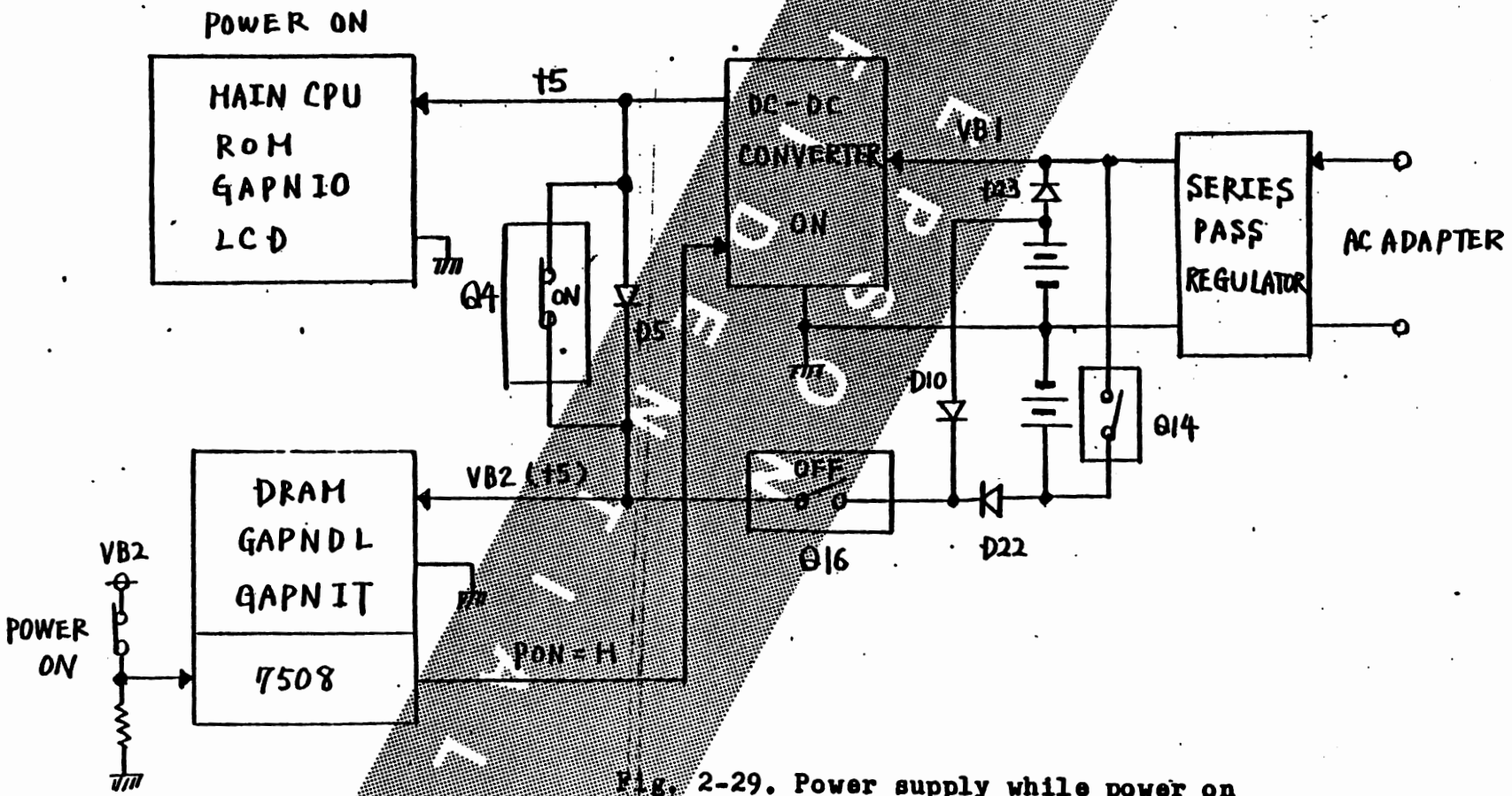

Fig. 2-29. Power supply while power on

2.5.2 Capacities

The DC-DC converter can support a normal system configuration including a usual option device. However, a special measure may be required when:

(1) A circuit of the user's own is connected to the system bus or cartridge interface,

(2) Any option device, which consumes much power, such as direct modem, barcode reader, or microcassette drive is used, or

(3) More than one option device are simultaneously used.

* DC-DC converter specifications

Table 2-1. lists the DC-DC converter output specifications which are guaranteed in an input voltage range from 4 to 7 V and a temperature range from 0 to 40°C.

Table 2-1. DC-DC converter output specifications

Output	Load current	Accuracy
+5	20 ~ 100 mA	± 5 % (+4.75 ~ 5.25 V)
−5	2 ~ 25 mA	+4%, −12% (−4.6 ~ −6.5 V)
+5/−15	0.7 ~ 3 mA	+13%, −11% (17.8 ~ 22.6 V)
CHARGE	3 mA	(11 ~ 13 V)

The output currents need to be in the listed rangea. Thus, the difference between the upper current limit of each output and its current current consumed by the PINE board with no

option device attached is available for option use.

* Power supplies available for options

The following supply currents ara available for options:

Table 2-2. Power supplies available for options

VB1		300 mA	(Average)
VB2	While power on	15 mA	(MAX)
	while power off	0.5 mA	(MAX)
+5		60 mA	(MAX)
-5		20 mA	(MAX)

Fig. 2-30. is a diagram which shows the power distributions to the interfaces; i.e., option devices. As obvious from the diagram, all the voltage sources required by each interface are supplied from PI-4. Thus, the total supply currents must not exceed the values listed in table 2-2. If any is exceeded, the correct voltage cannot be guaranteed. The standing-by and operating currents of an option device are different. Therefore, total interface current requirements must be determined as the maximum values required when operating intended option devices in combination.

The VB1 current value is shown as average in table 2-2 because it is supplied from the main battery. When a load which generates a large surge such as cartridge printer or microcassette drive is used, a Ni-Cd battery unit is required.

If the microcassette drive or ROM cartridge is operated only with the AC adaptor, the VB1 temporarily drops due to surge current. However, the power supply circuit connects the

auxiliary battery to the VB1 line to compensate for the surge, thereby preventing disturbance on the DC-DC converter output

* Combinations of option devices

The +5 V supply can be most critical when using more then one option device in combination. Table lists the operating +5 V supply current requirement of the available option devices.

Table 2-3. +5 V current requirements of option devices

Cartridge	mA
ROM cartridge	2
RAM cartridge	3
Microcassette drive	24
Cartridge printer	2
Direct modem	35
Digital multimeter	5

+

MX-80	
Operating	11
Stand-by	0

+

Barcord reader	
Operating	34
Stand-by	0

Option devices, whose total +5 V current requirement exceeds 60 mA, must not be simultaneously used. If such a combination is required, leave some standing by to reduce the current requirement below the limit.

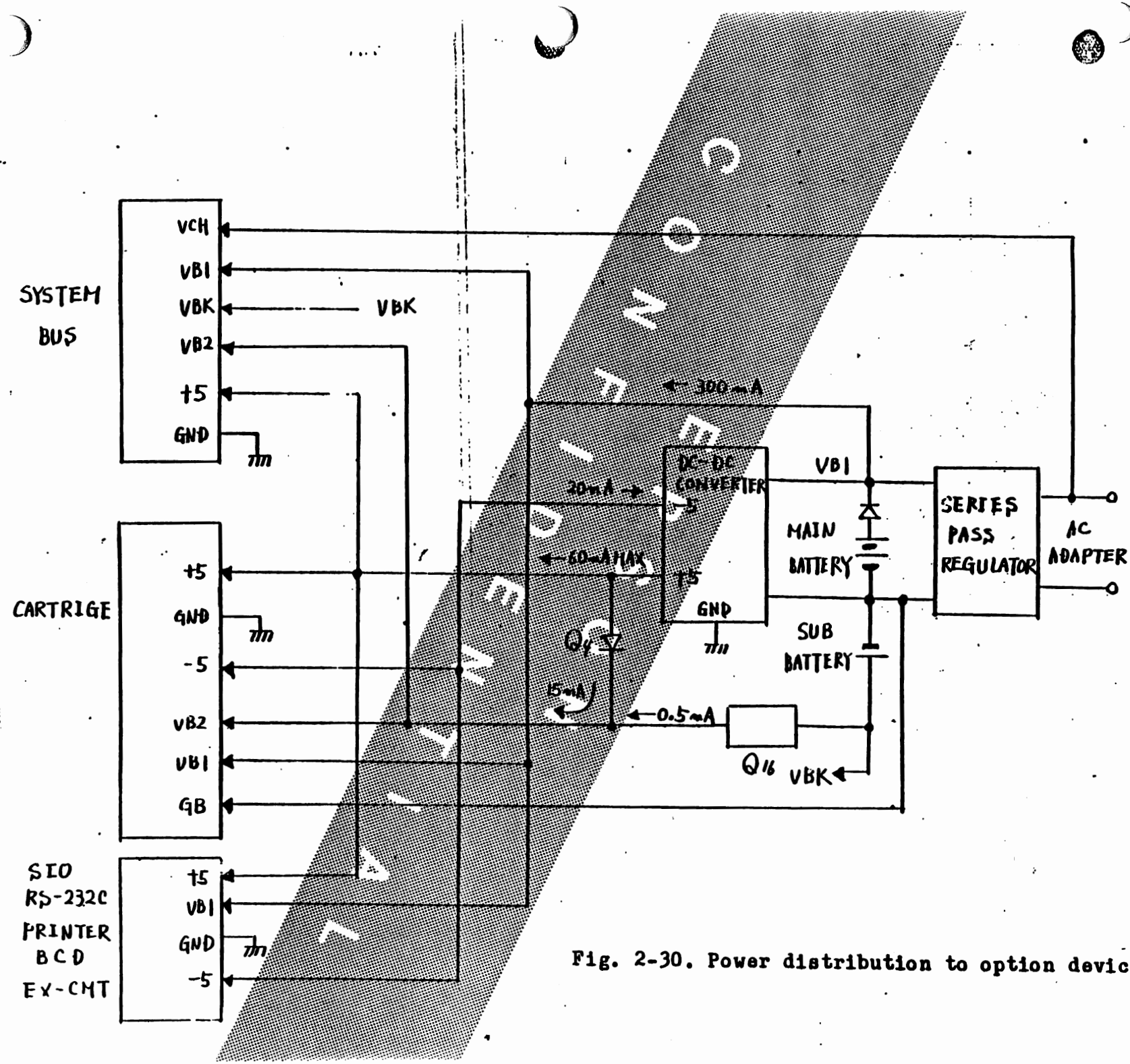

Fig. 2-30. Power distribution to option devices

The following combinations are not simultaneously allowed:

(1) Barcode reader and microcassette drive

(2) Barcode reader and direct modem

* Battery charge cycle

The standard PX-4 configuration (with no option device) can be used without the AC adaptor for the following periods of time without recharging the main battery - battery exhaustion is indicated by a message "CHARGE BATTERY":

Battery	Discharge time (hours)
Ni-Cd	4.25
Manganese	5.5
Alkali	11.5

If the current requirement is known, the discharge time of the Ni-Cd battery whose capacity is 450 mAH can be calculated. If the stand-by current of the attached option device is assumed to be 2 mA for example, the discharge time is 4.28 hours as given by:

Discharge time (H) = 450/105 = 4.28 hours

because the PINE board operating current requirement is 103 mA.

The stand-by current requirement of usual option devices falls within an error range from 2 to 3 mA. However, the following devices a little shortens the main battery discharge time:

Option device	Stand-by current requirement (mA)
Microcassette drive	14.
Direct modem	7
External RAM disk	5.5

* PINE board and option device current requirements

The current requirements of the PINE board and all available option devices are listed below - it is assumed that the VB1 source is supplied from the Ni-Cd battery (VB1 = 5 V).

The total requirements can be obtained by adding the currents consumed in the PINE board and all the attached option devices.

(1) PINE board (when no option device is attached)

+5	Operating:	53 mA (During BASIC run)
	Stand-by:	25 mA (While BASIC waiting for entry)
VB1	Operating:	103 mA
	Stand-by:	65 mA
-5	Always	2.1 mA

(2) ROM cartridge

+5	Always	2 mA	
VB1	Operating:	135 mA	(2 NMOS ROM elements)
		105 mA	(1 NMOS ROM element)
		33 mA	(2 CMOS ROM elements)
	Stand-by:	2 mA	

(3) RAM cartridge

+5	Operating:	3 mA
	Stand-by:	3 uA

(4) Microcassette drive

+5	Operating:	24 mA	
	Stand-by:	11 mA	
VB1	Operating:	130 mA	(During PLAY)
		142 mA	(During WIND)
	Stand-by:	14 mA	

(5) Cartridge printer

+5V	Always	2 mA	
VB1	Operating:	300 mA	(During continuous print)
	Stand-by:	2 mA	

(6) Direct modem

+5	Operating:	35 mA	
	Stand-by:	5 mA	
-5	Operating:	15 mA	
	Stanb-by:	0.2 mA	
VB1	Operating:	13 mA	(While power relay actuated)
	Stand-by:	7 mA	

(7) External RAM disk

VB1	Operating:	26 - 36 mA	
	Stand-by:	5.5 mA	

(8) Digital multimeter

+5	Operating:	5 mA	
	Stand-by:	0	(Power-off mode)

(9) TF-20 (SIO)

VB1	Always	3 mA	
-5	Always	2.5 mA	

(10) MX-80 (Printer)

+5	Operating:	11 mA
	Stand-by:	Nearly 0
VB1	Operating:	16 mA
	Stand-by:	Nearly 0

(11) External cassette recorder

+5	Operating:	Nearly 0
VB1	Operating:	40 mA (While power relay actuated)

(12) Barcode reader

+5	Operating:	35 mA
	Stand-by:	Nearly 0
VB1	Operating:	48 mA
	Stand-by:	Nearly 0

2.5.3 7508 Siganls

7508 is a 4-bit CPU which has internal programs devoted to control PX-4. Its input/output port functions are defined by the programs.

Fig. 2-31 is a block diagram which shows the 7508 signals associated with power-off control.

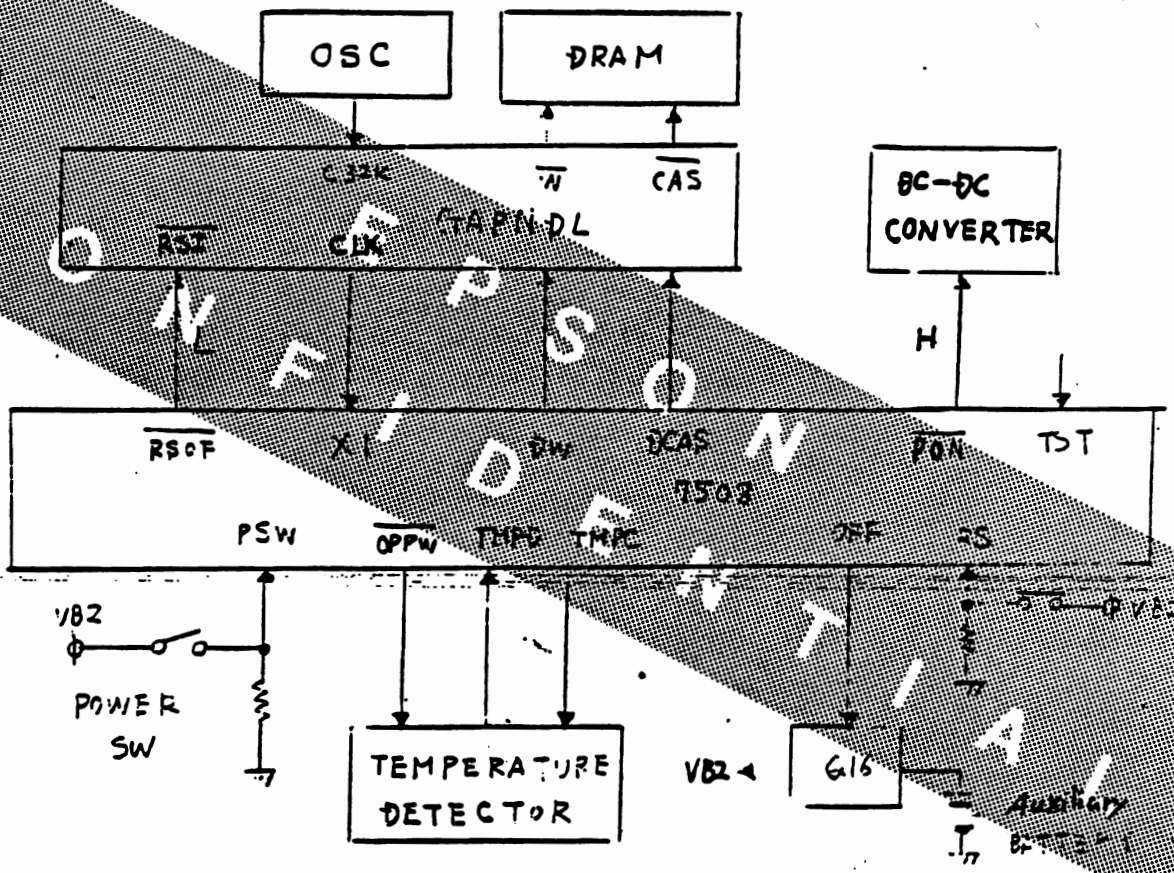

Fig. 2-31 7508 power-off control signals

The individual signals are described below.

PSW: A POWER switch state signal - when low, this signal indicates that the POWER switch is OFF.

$\overline{PON}$: Turns PX-4 on/off - when high, this signal turns PX-4 off.

OFF: A Power Off signal which is activated high when PX-4 is off - this signal connects the sub-battery to the VB2 line.

$\overline{RSOF}$: A Reset signal - low when PX-4 is off.

X1: A Calendar Clock signal.

DW, DCAS: Signals which control DRAM refresh.

$\overline{OPRW}$: A pulse signal of 10-second interval which controls power supply to the temperature sensor circuit.

TMPC: A signal which sets a specific temperature to be detected by the temperature sensor circuit - this signal sets the detected temperature to 47°C when it is low and to 25°C when it is in the high impedance state.

TMPD: The temperature sensor circuit output signal - high when the temperature is higher than the set value.

TST: The 7508 Self-Test signal - serves as an input signal while PX-4 is off and used as an output signal while on. 7508 is self-tested when this signal is high.

RS: The 7508 Reset signal - when high, this signal performs an initial reset on 7508. After the initial reset signal is removed, the internal program initializes necessary I/O ports for output by deactivating their outputs. The I/O port outputs may be initialized not only high or low but also to a high impedance state.

Fig. 2-32 is a block diagem which shows the 7508 signals associated with power-on control.

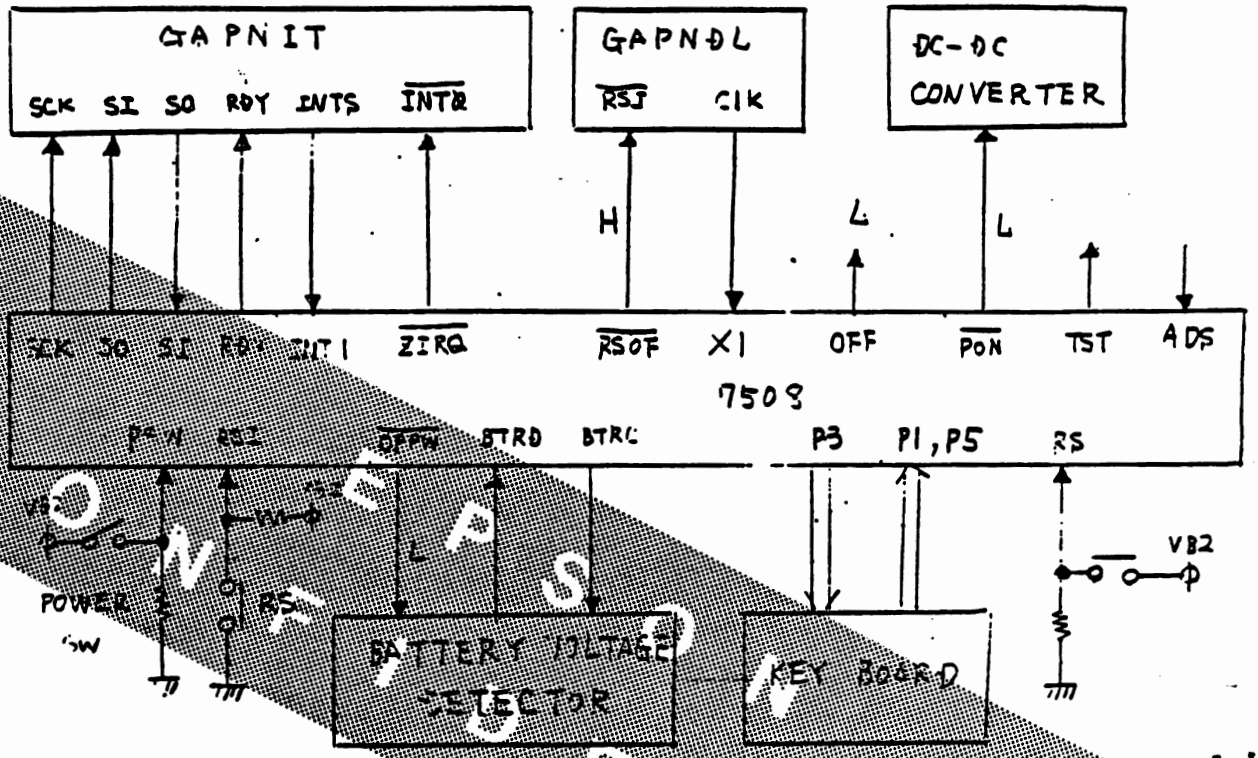

Fig. 2-32. 7508 power-on control signals

The individual signals are described below.

RSI: The Reset Switch State signal - when low, this signal indicates that the Reset switch is activated.

$\overline{\text{OPPW}}$: A signal which supplies power to the battery low voltage detector circuit - when low, this signal supplies power.

BTRC: A signal which sets a voltage limit to be detected as low voltage - this signal sets the limit to 4.99 V when low, and to 4.80 or 4.00 V when in the high impedance.

BTRD: The battery low voltage detector circuit output signal - goes low when power fails.

ADS: A signal which detects whether the AC adaptor is used or not - high when the adaptor is used.

TST: A signal which connects the sub-battery to the VB1 line.

$\overline{\text{ZIRQ}}$: The 7508 interrupt request signal to the main CPU.

SI: Serial data input.

SO: Serial data output.

$\overline{\text{SCK}}$: Shift clock signal.

INTS: Serial data transfer signal.

RDY: 7508 Ready signal.

P3: Key Scan signal.

P1, P5: Key Return signals.

2.5.4 7508 Operations

* While PX-4 is off, 7508 is in a stand-by mode and even the clock signal oscillation is disabled to minimize power consumption.

7508 can be activated from the stand-by mode by an interrupt, which occurs when the POWER switch is set ON, a timer interrupt, which occurs every 10 seconds, or the initial reset.

When started, the clock signal oscillator starts oscillating and the 7508 internal program performs one of the following procedures depending the interrupt:

(1) For the timer interrupt, 7508 supplies power to the temperature monitor and battery low voltage detector operational amplifiers to enable the functions and set a DRAM refresh mode. Then, after checking the time alarm function against

the calendar clock count, it turns the operational amplifiers and returns to the stand-by mode. If the time alarm occurs at this time, 7508 sets the Alarm bit of the status code to 1 and turns power on.

(2) For the POWER switch interrupt, 7508 turns the operational amplifiers to examine the battery voltage. If the voltage is normal, it the Power Switch bit of the status code to 1 and turns power on. If the battery voltage is found too low, 7508 turns the operational amplifiers off and returns to the stand-by mode.

(3) When the Initial Reset switch was reset, 7508 initializes itself and sets the Initial bit of the status code to 1. Then, if the POWER switch is not set ON, it returns to the stand-by mode.

* While PX-4 is on, 7508 scans the keyboard to check if any key is pressed unless it is interrupted by the timer.

When a key is pressed, 7508 detectw the key stroke and interrupts the main CPU which returns a command to 7508 to read the key code.

As long as PX-4 is on, 7508 is interrupted by the timer every one-256th of second and accomplishes the following:

(1) Checks if any command has been received from the main CPU, and processes the command if received.

(2) Checks if the Reset switch ~~has been~~ is pushed ~~and~~ issues the

Reset signal, and sets the status bit to 1, if pushed.

(3) Checks whether the POWER switch is set ON or reset OFF, interrupts the main CPU, and sets the status bit to 1, if ON.

(4) Checks for power failure, interrupts the main CPU, and set the status bit to 1, if any power failure is detected.

(5) Outputs the calendar clock.

(6) Checks for time alarm, interrupts the main CPU, and sets the status bit to 1, if the time alarm occurs.

and??? 7508 returns the status code or data only when requested from the main CPU via a command. 7508 interrupts the main CPU to send data to it.

When interrupted or reset, the main CPU reads and examines the 7508 status code, and takes actions accordingly.

Data or commands are serially transferred between the main CPU and 7508.

* 7508 power failure handling procedures

When a power failure is detected, 7508 performs the following procedure:

(1) Checks if teh AC adaptor is used. If used, 7508 ignores the power failure. This is because PX-4 can recover from power failure and the +5 V supply is not disturbed by power failure when the AC adaptor is used.

If the input to the DC-DC converter drops so much that the +5 V supply cannot be stable, the sub-battery is auto-

matically connected via transistor Q13 to maintain the +5 V supply stable.

(2) Connects the sub-battery to the main battery via transistor Q12.when the main battery is the Ni-Cd battery unit or the AC adaptor is used. Because the Ni-Cd battery voltage drops faster in power failure, the supply line is backed up by the sub-battery until the power failure handling procedure is completed.

(3) Interrupts the main CPU every one second and, if no Power-Off command is returned within 50 seconds, forces the battery supply to be removed.

The following flowchart summarizes the 7508 operations:

* When the main CPU is not operating

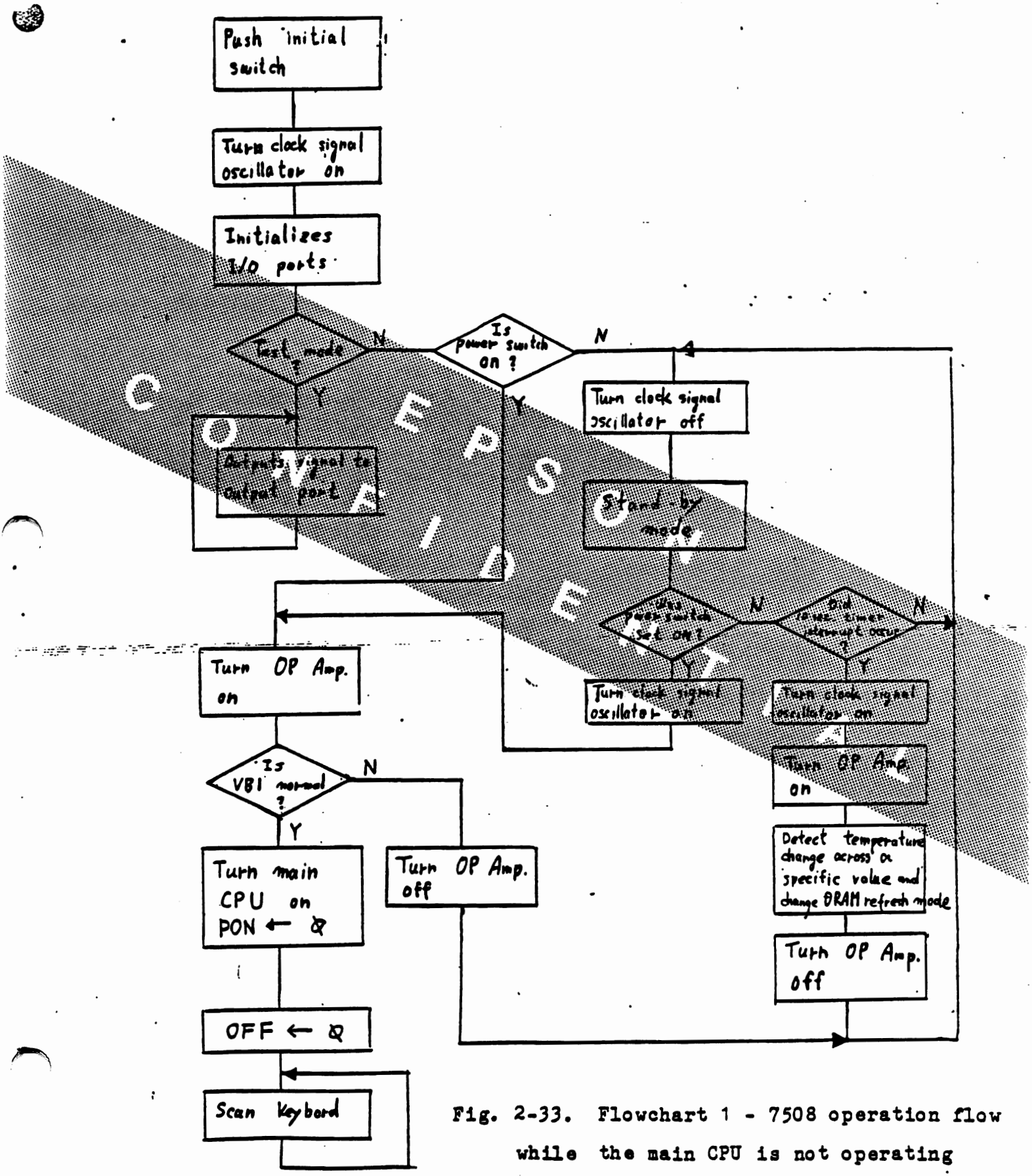

Fig. 2-33. Flowchart 1 - 7508 operation flow while the main CPU is not operating

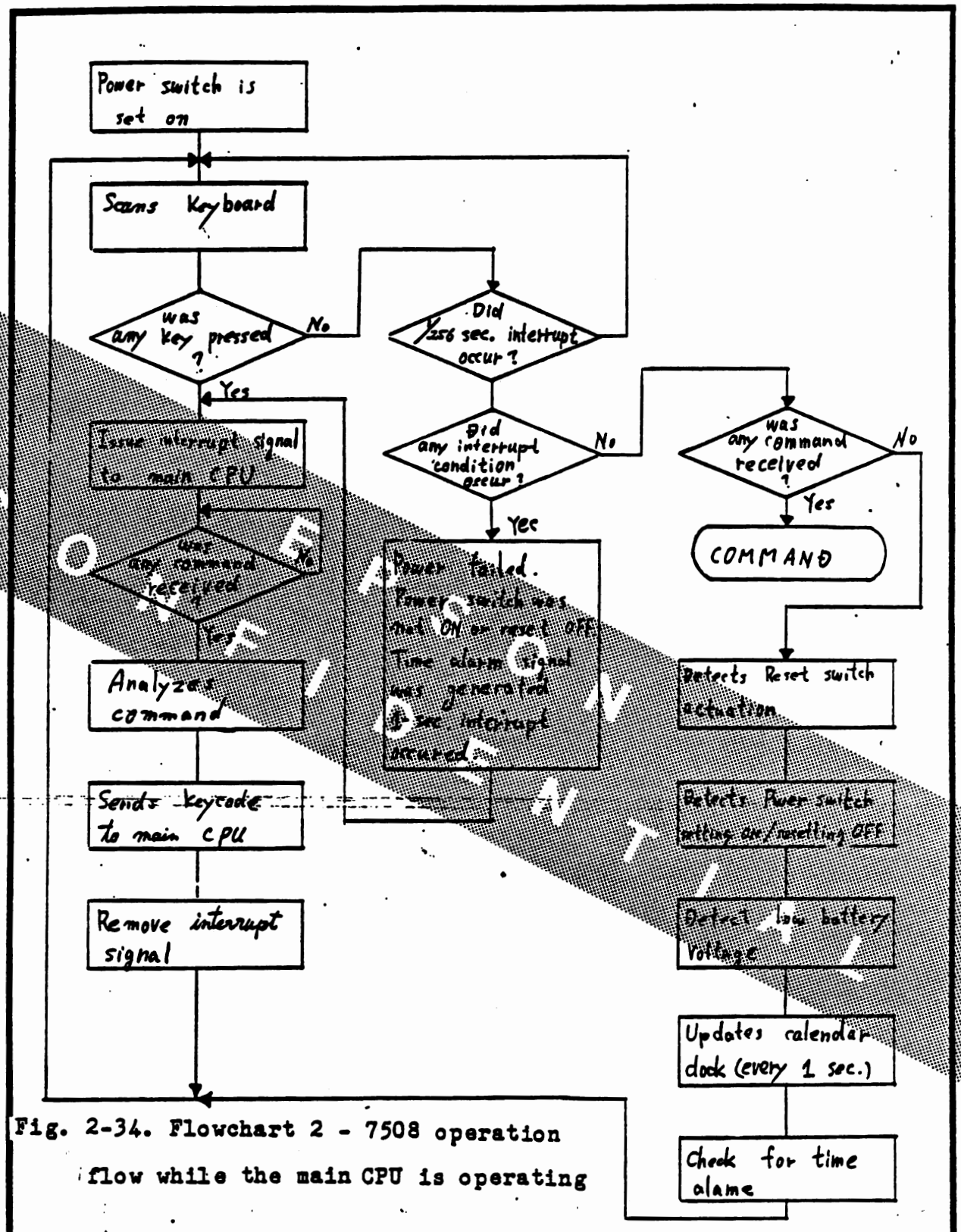

Fig. 2-34. Flowchart 2 - 7508 operation flow while the main CPU is operating

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The following flowchart summarized the 7508 command processing procedure:

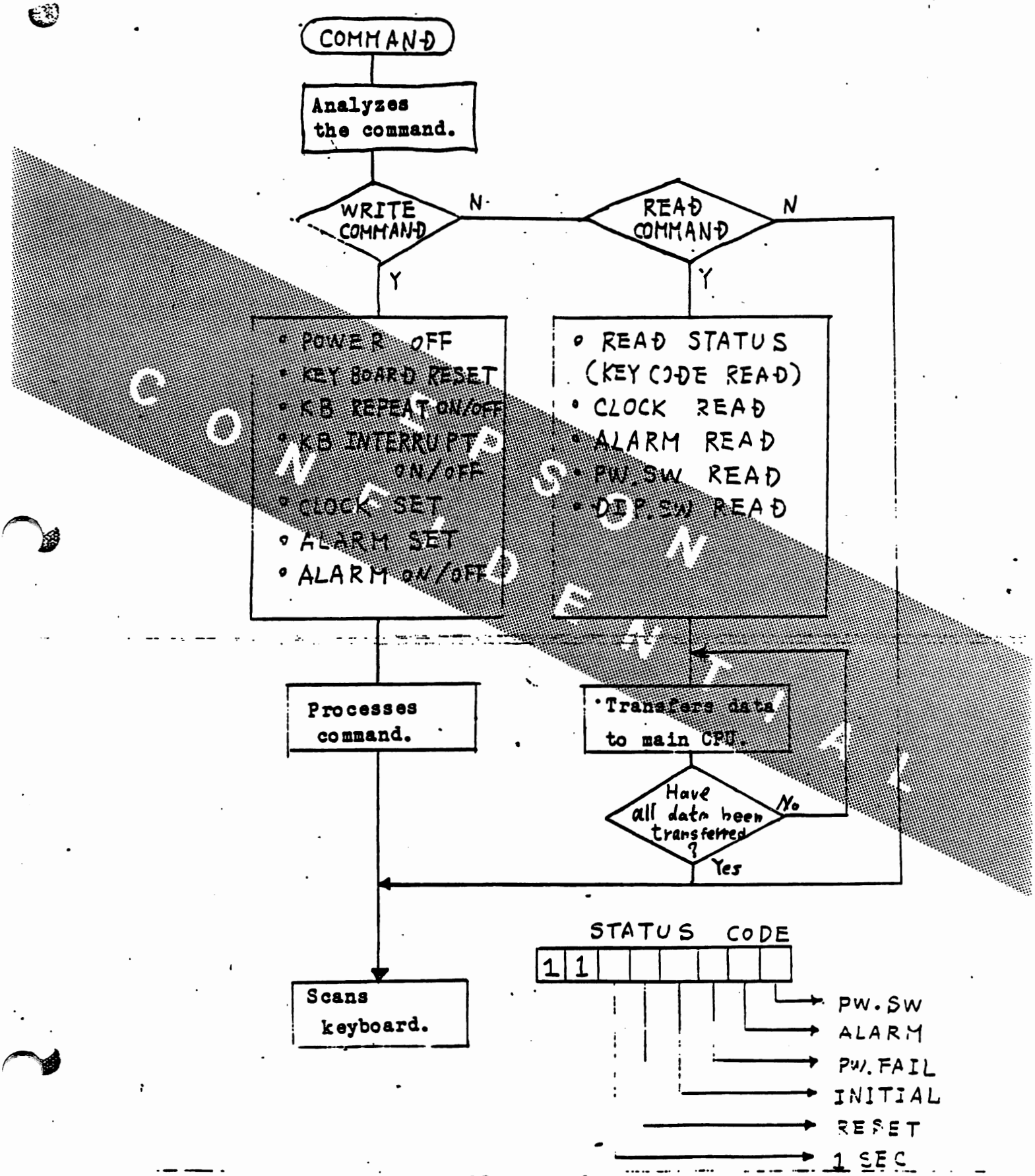
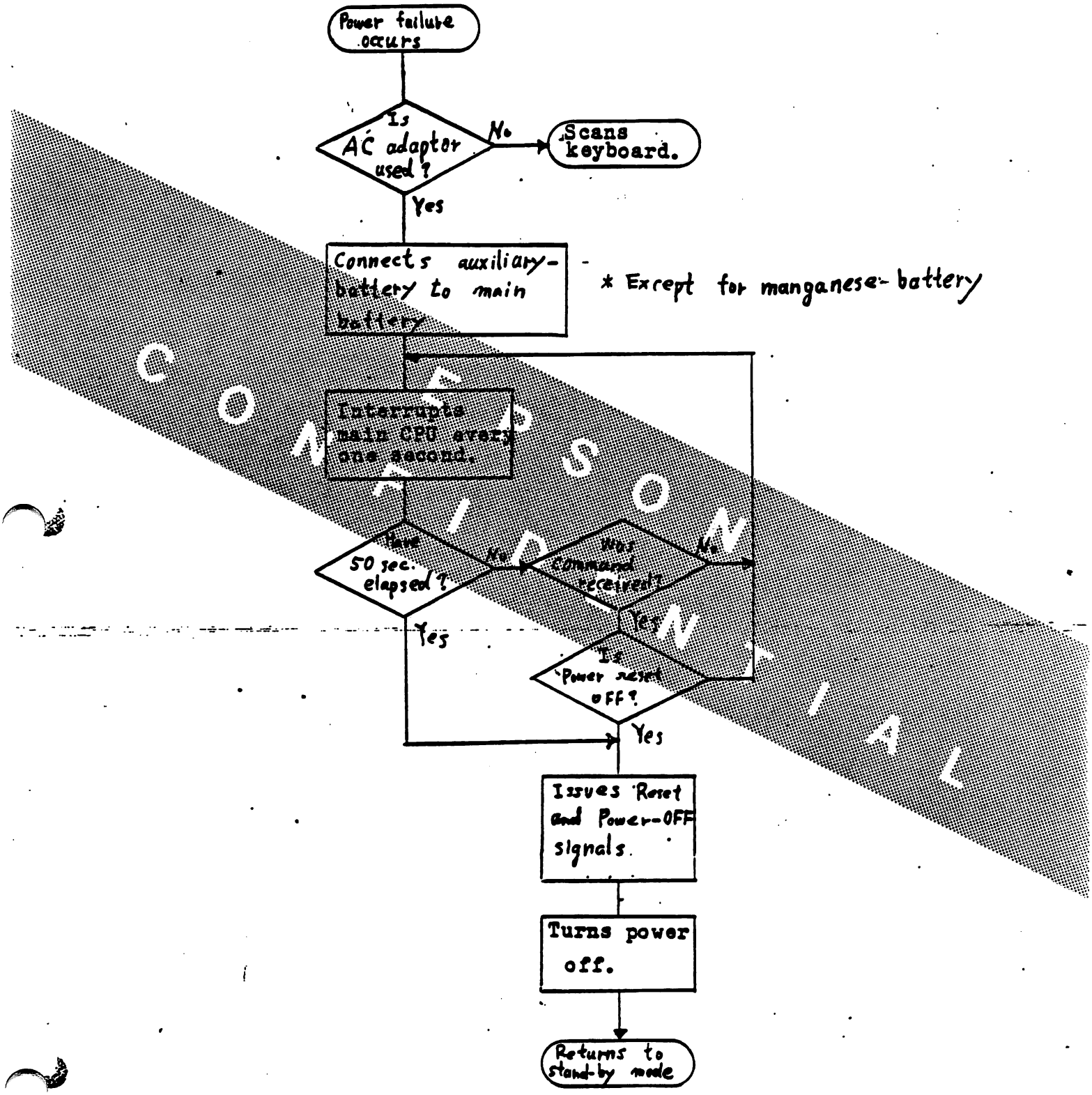


Fig. Flowchart 3 - 7508 command processing

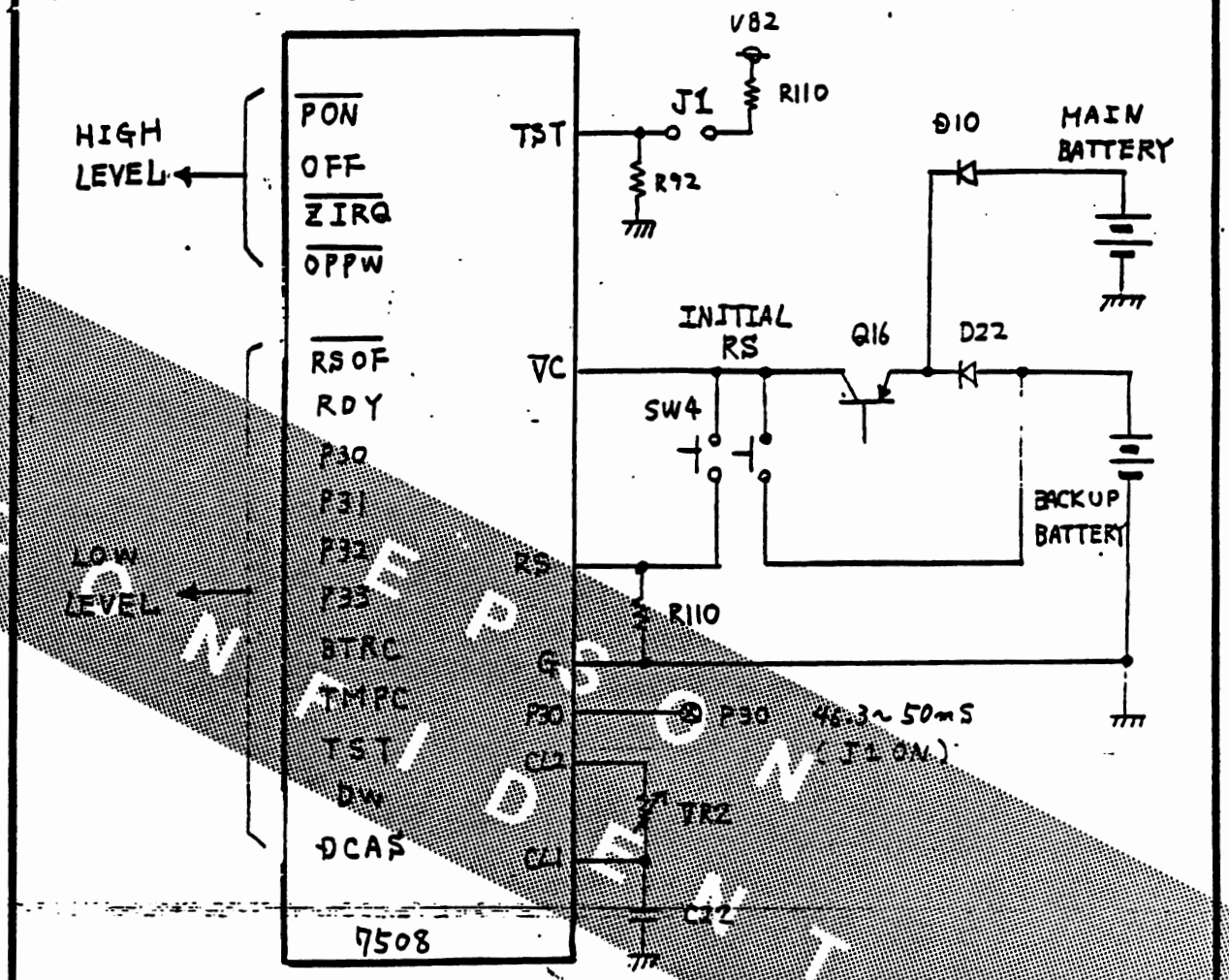
The following flowchart summarizes the 7508 power failure handling procedure:



Power failure handling procedure

Fig. 2-36. Flowchart 4 - power failure handling procedure

2.5.5 Initial reset



1. Fig. 2-37 Initial reset

The initial switch is pressed to start 7508. If SW4 is pressed, the power is applied to 7508 and it is reset initially at the same time. The output port of the 4-bit CPU 7508 is initialized with the beginning of the program contained in itself. The oscillating frequency of the

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clock of 7508 is determined by CR which is connected to CL2 and LC1, and the period at check terminal P30 can be adjusted to 46.3 - 50.0 ms with VR2. When adjusting VR2, short jumper plug J1 with the power switch turned off and press the initial reset switch.

2.5.6 Memory backup

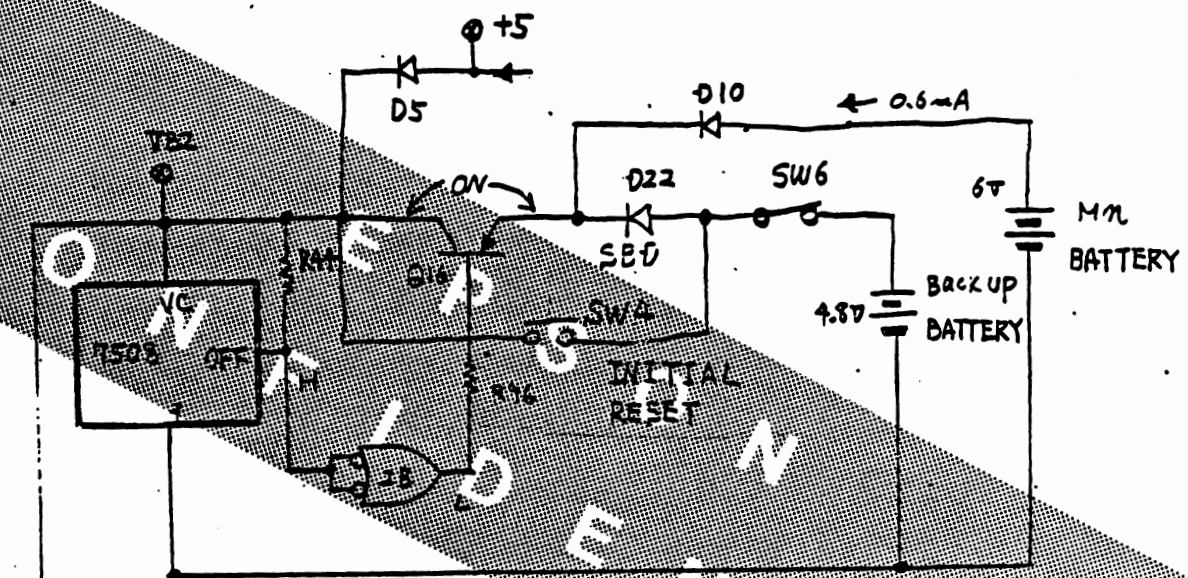

Fig. 2-38 Memory backup

GAPNDL
GAPNIT
DRAM x 8
GATE (2B)
OP. AMP(3B)

If the initial reset switch is pressed, 7508 is started and OFF signal is set to level H. By this, Q16 is turned on, and the backup power is supplied even if SW4 is not pressed. Normally, the backup power is supplied by the Leclanche type dry battery which generates a higher voltage.

D22 is a Schottky barrier diode, the voltage drop of which in the normal direction is little, is used to improve the use efficiency of the battery (VF = 0.31 V). If the power is turned on, the voltage of +5 is applied to VB2, and Q16 is turned off by the OFF signal (level L), then VB2 is disconnected from the sub-battery. When Ni-Cd batteries are used, the voltage drop of D10 (VF = 0.56 V) is larger than that of D22, and therefore the backup power is supplied by the sub-battery.

Table 2-4 Backup current

Auxiliary battery voltage	5.5 V	5.2 V	4.8 V
45 ~ 70°C	1.4 mA	1.2 mA	1.0 mA
25 ~ 45°C	0.7	0.6	0.4
0 ~ 25°C	0.5	0.4	0.3

2.5.7 Setting the output level

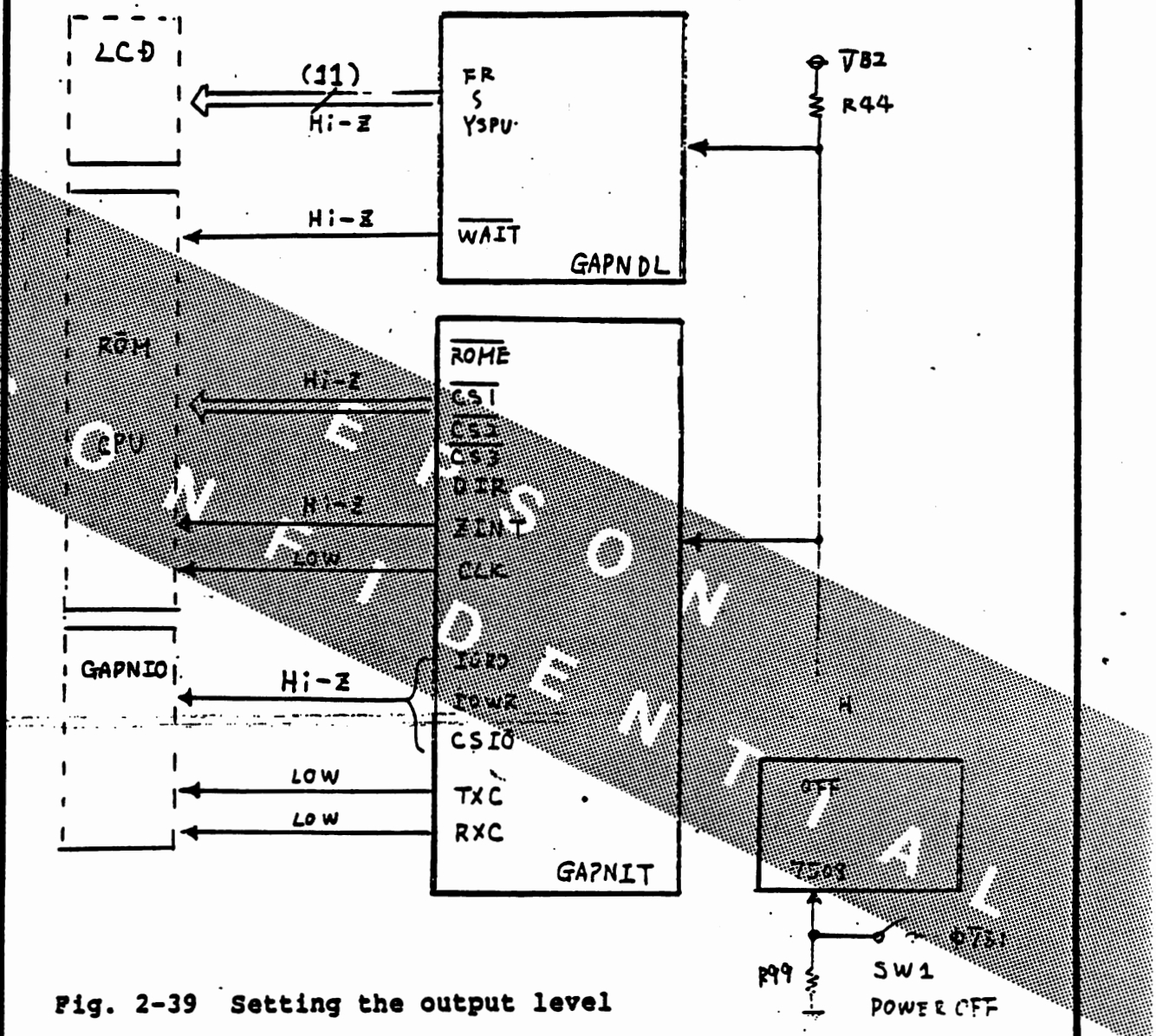

Fig. 2-39 Setting the output level

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If 7508 is started, the OFF signal is set to level H. By this, the output terminals of gate arrays GAPNDL and GAPNIT are set to the high impedance condition or level L. This is performed to prevent an excessive current from flowing out of the IC's which are backed up by the battery, since the power is not supplied to the main CPU and its peripheral circuits and the indicator circuit while the power switch is turned off.

2.5.8 Maintaining the memory

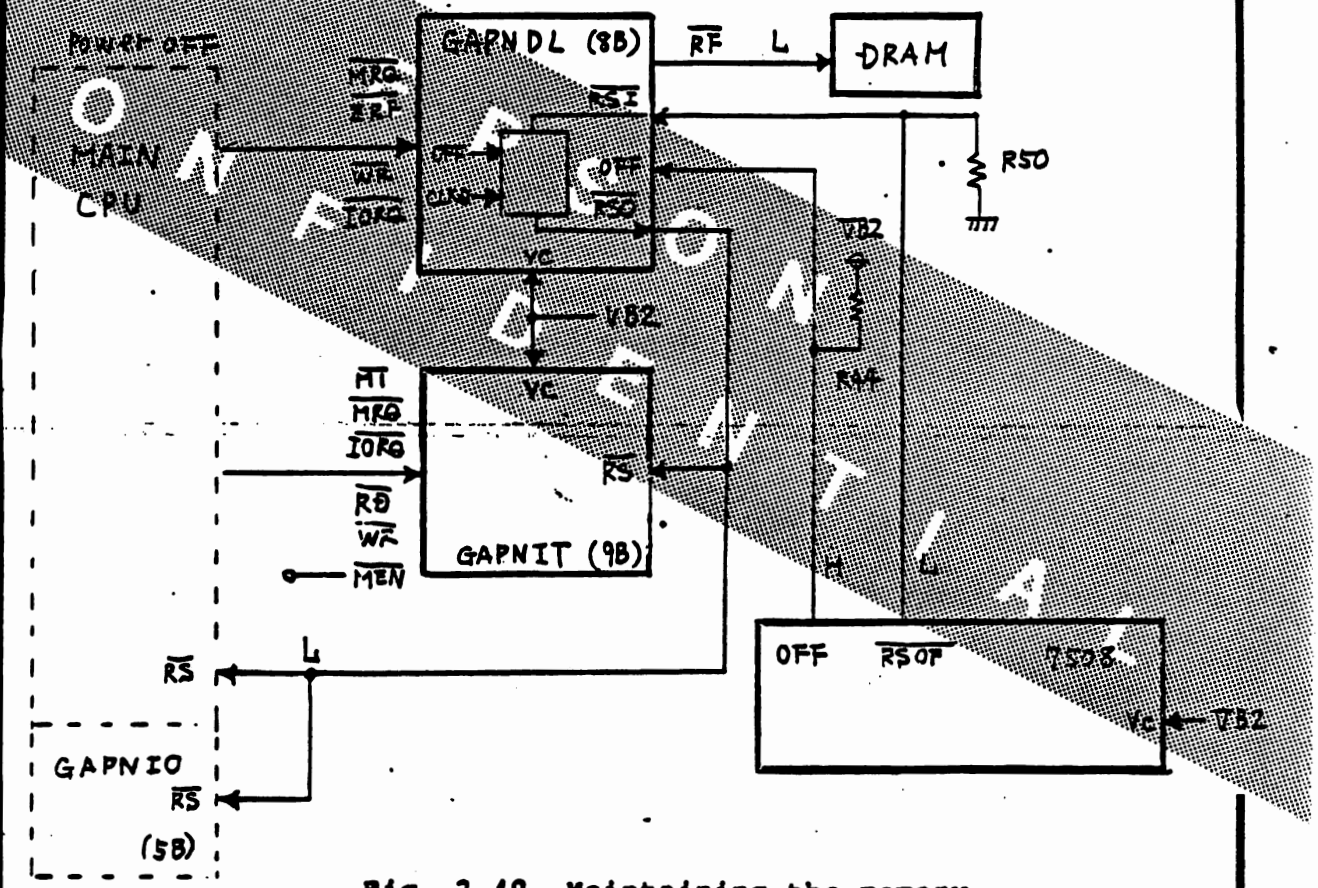

Fig. 2-40 Maintaining the memory

If 7508 is started, OFF signal is set to level H, and RSOF signal is set to level L.

The reset signal RS of the main CPU is output from GAPNDL, but it is set to level L while the power for the main CPU is turned off or it is in the transient state. By this, the input from the main CPU is prohibited by the gate array to maintain the condition of the internal circuit.

The reset signal is outputted to refreshing signal RF, and while it is at level L, the DRAM refreshes itself to maintain the contents of the memory.

2.5.9 Clock for calendar clock

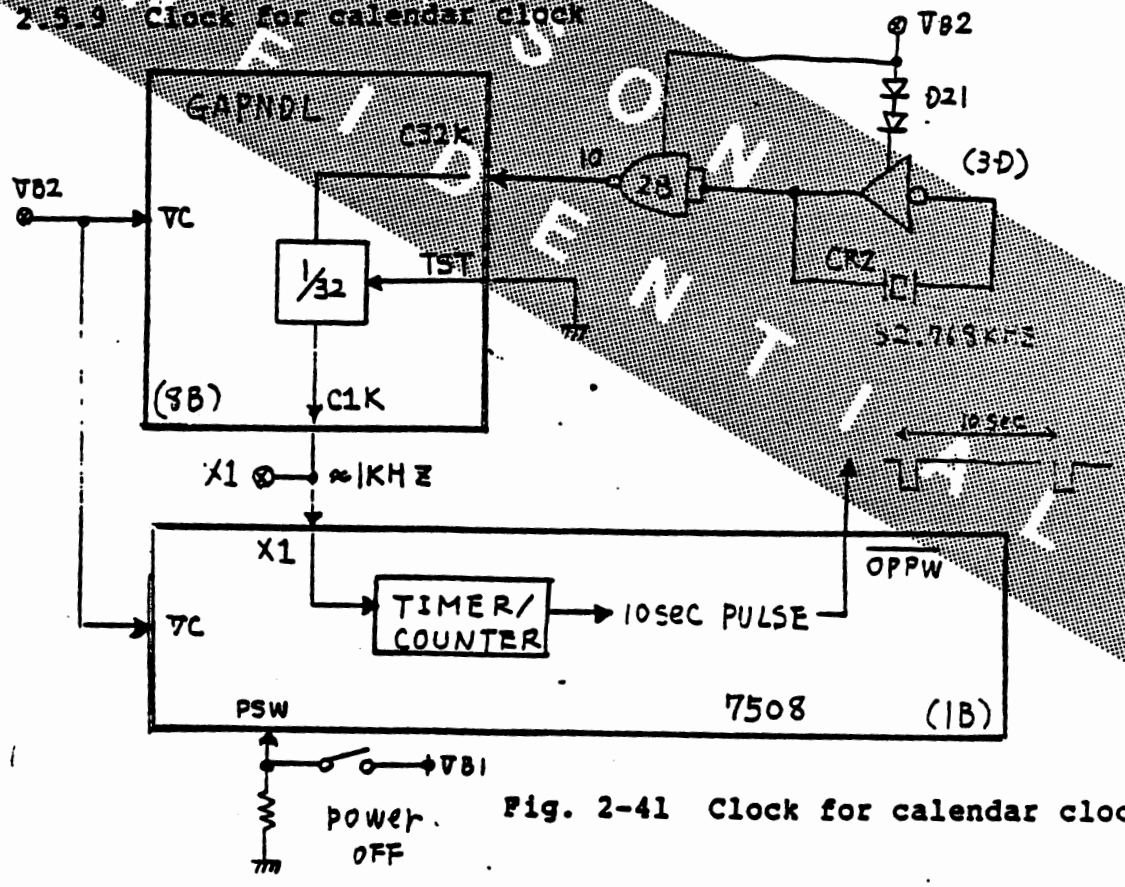

Fig. 2-41 Clock for calendar clock

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Even if the power switch is turned off, the calendar clocke is operated by the battery.

The clock signal is divided into 32 in GAPNDL and inputted to 7508. This signal is further divided in 7508 to obtain the final signal of 10 seconds. By this, 7508 can be started periodically. The functions of calendar clock and alarm are executed by the RAM and programs contained in 7508. The crystal resonator is the same one used for wrist watches, and its accuracy in oscillation is sufficient.

2.5.10 Cotrol of ĐRAM

Table 2-5 Setting the self-refreshing mode

Ambient temperature	Output of 750γ		Input of ĐRAM		Power consumption
	ĐCAS	ĐW	$\overline{CAS}$	$\overline{W}$	
45~75 °c	0	0	H	H	400 μA
25~45°C	0	1	H	L	200 μA
0 ~25°C	1	1	L	Pulse	100 μA

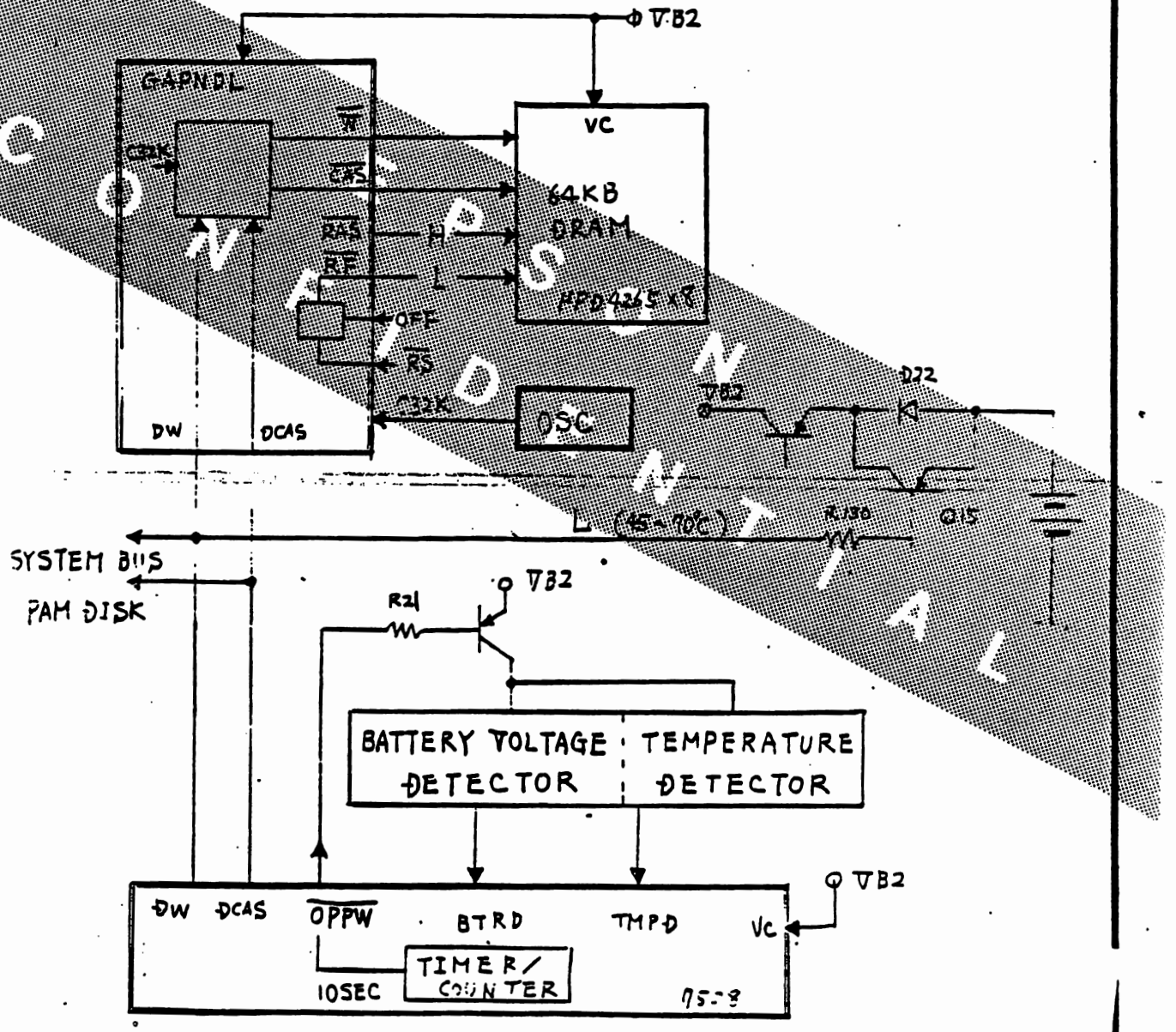

Fig. 2-42 Control of ĐRAM

The memory of the dram used in this device can be refreshed in the IC by setting refreshing signal RF to level L. Therefore, when the power is turned off, the dram refreshes itself. The self-refreshing mode is set 7508 according to the ambient temperature to reduce the power consumption of the dram. The ambient temperature is detected by the temperature sesor circuit through the thermistor and inputted to the drum through GAPNDL. That is, the current determined by input signals W and CAS of the dram as shown in the table flows (into each IC). If the ambient temperature rises above 45°C and the current from the battery increases, Q15 is turned on to reduce the power consumed by D22. 7508 is started every 10 seconds to perform the above process.

2.5.11 Turning on the power

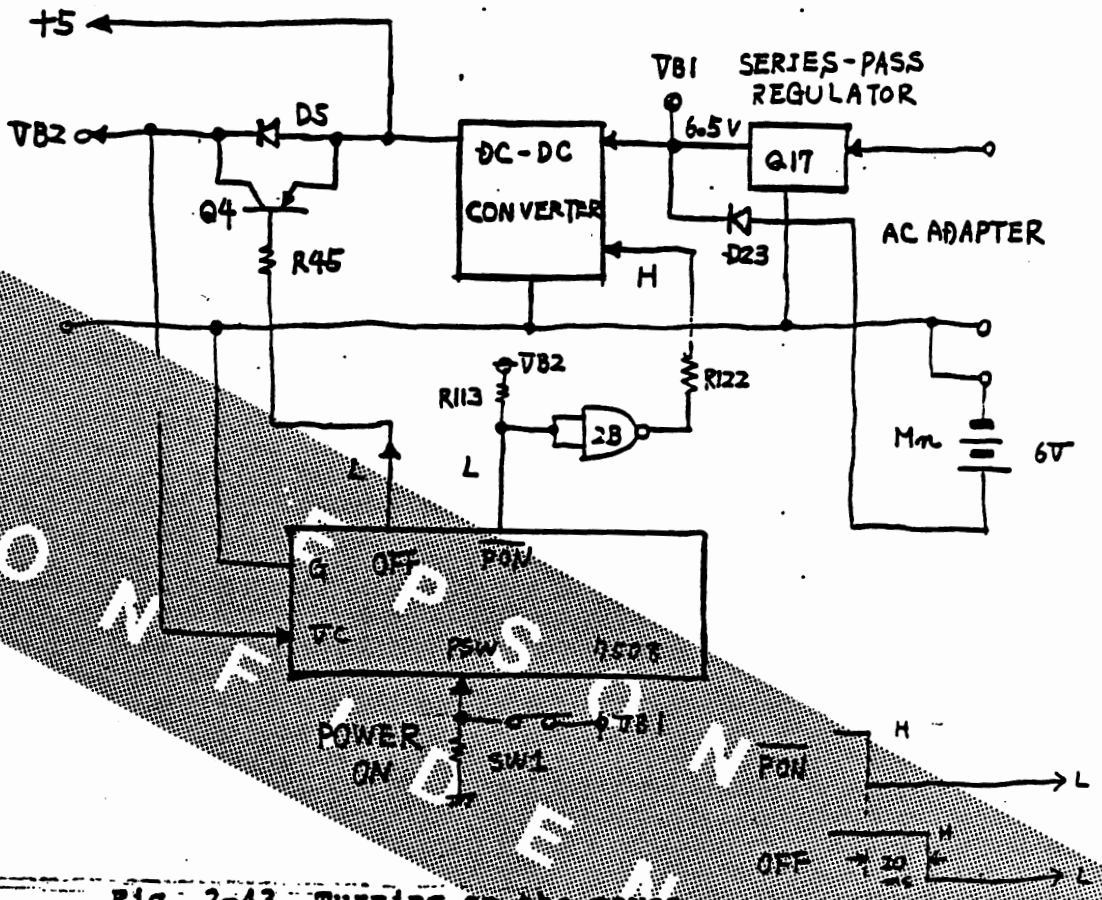

Fig. 2-43 Turning on the power

7508 detects the condition of the power switch. If SW1 is turned on, 7508 set PON to level L at first. By this, level H is inputted to the input of the output control of the DC-DC converter, then the DC-DC converter starts the oscillation.

After +5 V is stabilized, if OFF signal is set to level L, Q4 is turned on and the voltage of VB2 becomes almost +5 V. At this time, the sub-battery which has been

connected to VB2 is disconnected by this signal.

If the AC adapter is connected, the output voltage of the stabilized power supply (Q17) becomes higher than that of the battery, and the current is supplied from the adapter. Therefore, the current from the battery stops. If the current from the AC adapter is cut off, the power is automatically supplied by the battery, that is, the power does not fail. If the voltage of the battery lowers while the power is turned off, the power is not supplied even if the power switch is turned on.

2.5.12 Scanning the keyboard

After setting OFF signal to level L, 7508 starts to scan the keyboard. 7508 is constantly checking for the input of the keyboard. If there is any interruption, 7508 processes it.

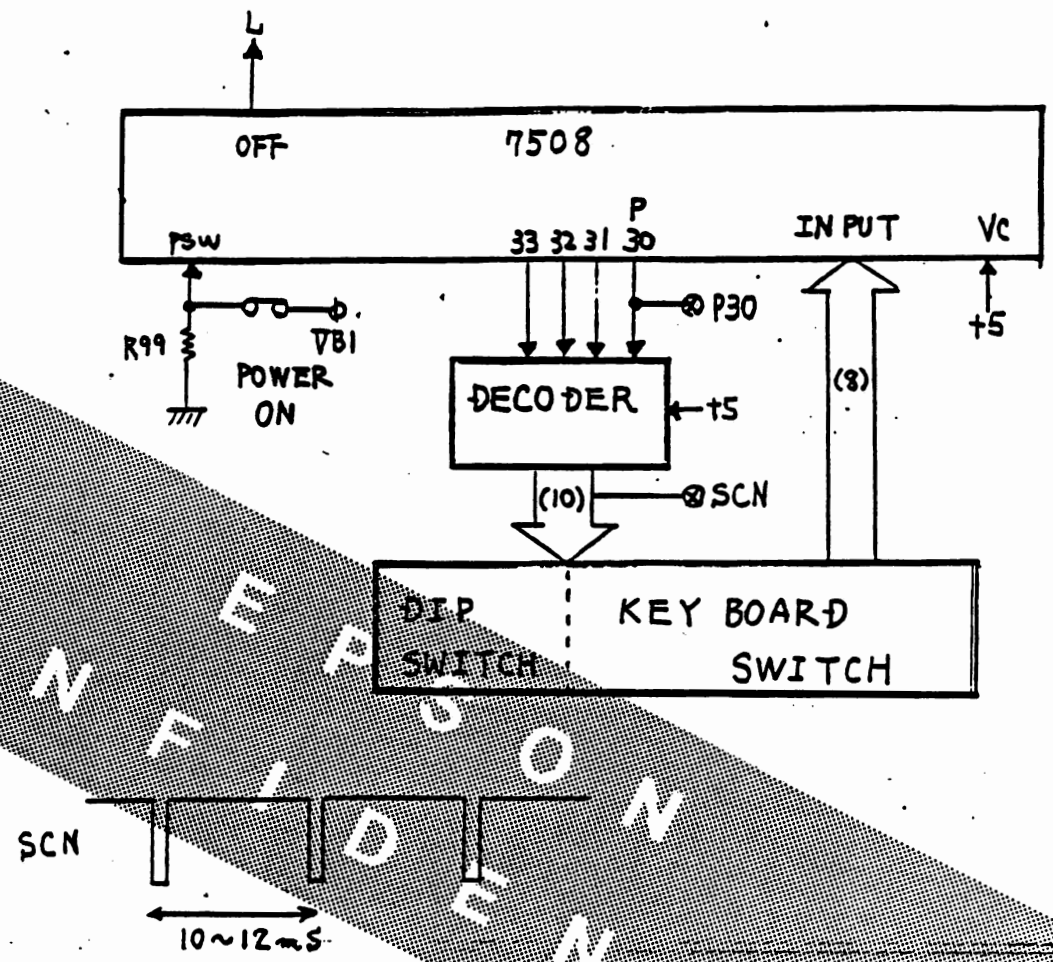

Fig. 2-44 Scanning the keyboard

7508 determines the time of the key scanning signal according to the program, but the period of the key sanning signal is not constant since the interruption by the timer is processed during the key scanning.

2.5.13 Clock signal

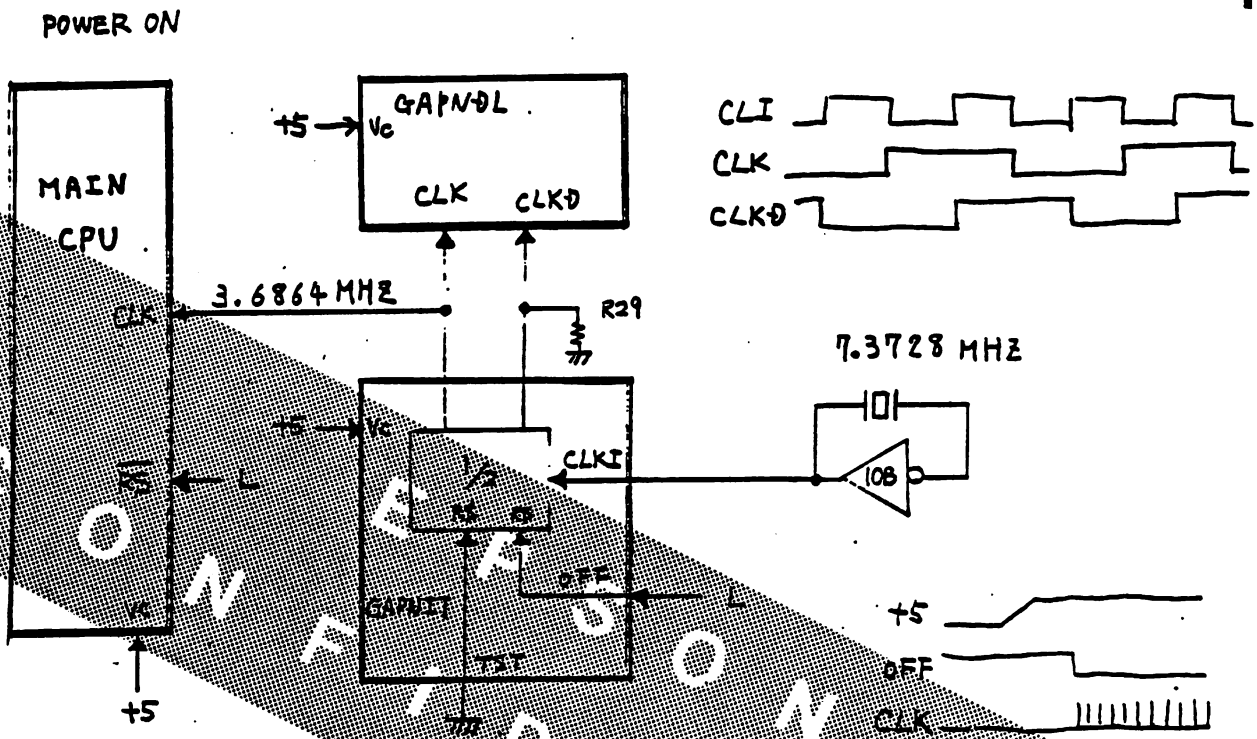

Fig. 2-45 Clock signal

If the DC-DC converter is started, the power (+5) is supplied to the main CPU and the oscillator starts the oscillation.

The clock signal supplied to the main CPU is made by dividing the signal of the oscillator into two within the GAPNIT. Since outputting the clock signal is prohibited by OFF signal, it is outputted when OFF signal is set to level L. Since RS signal is still kept to level L after OFF signal is set to level L, the main CPU is still reset.

2.5.14 Resetting signal

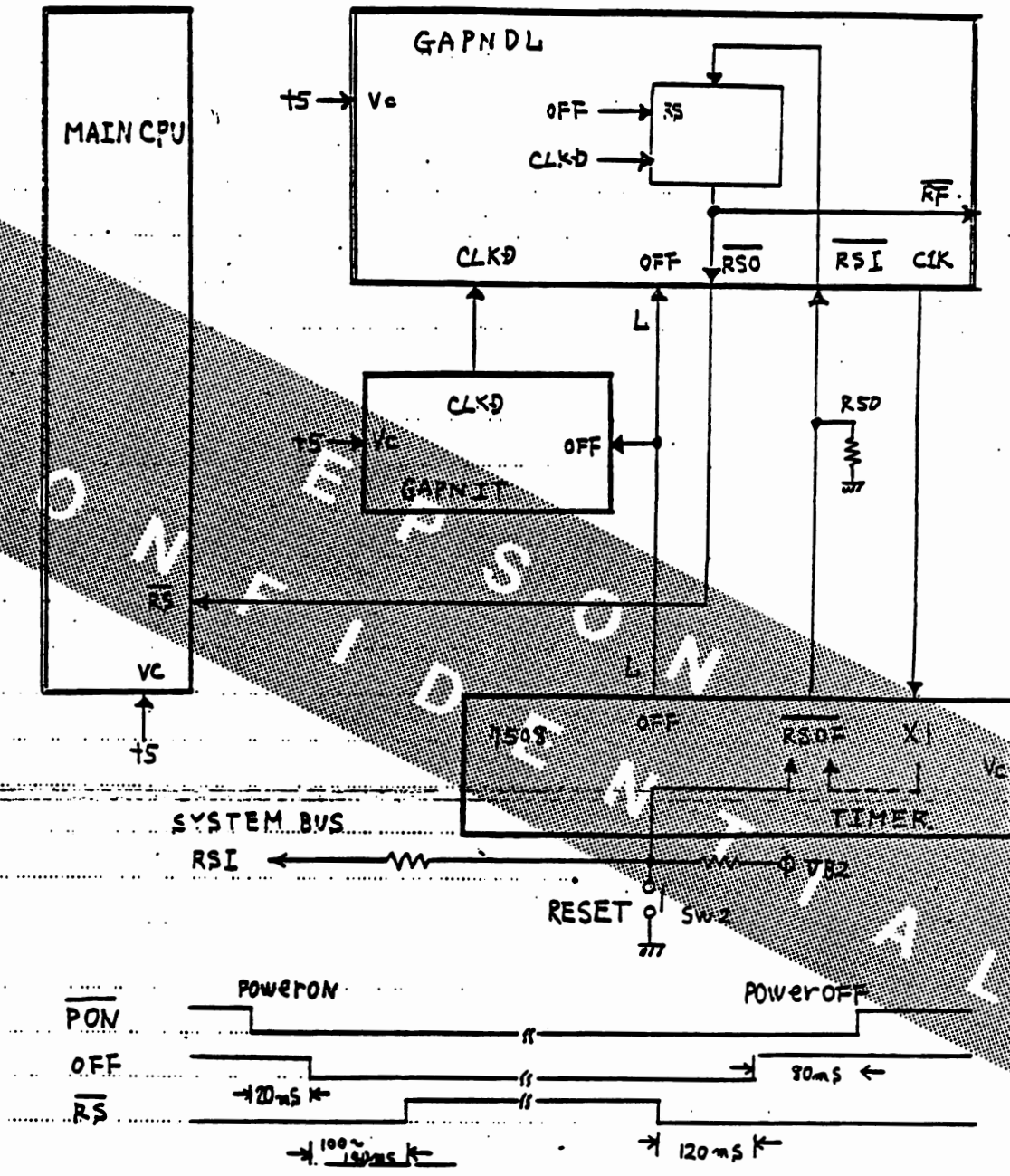

Fig 2-46. Resetting signal

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7508 controls the sequential operation of the power supply and resetting (See the time chart). Sicne RSOF is set to level H in the program of 7508, the interruption by the timer is necessary, and that is possible when X1 is inputtted. RS signal outputs RSOF signal after synchronizing it with the clock signal within GAPNDL. At this time, OFF signal is set to level L. If the reset switch is pressed, 7508 will detect this and resets the main CPU.

2.5.15 Input signal of main CPU

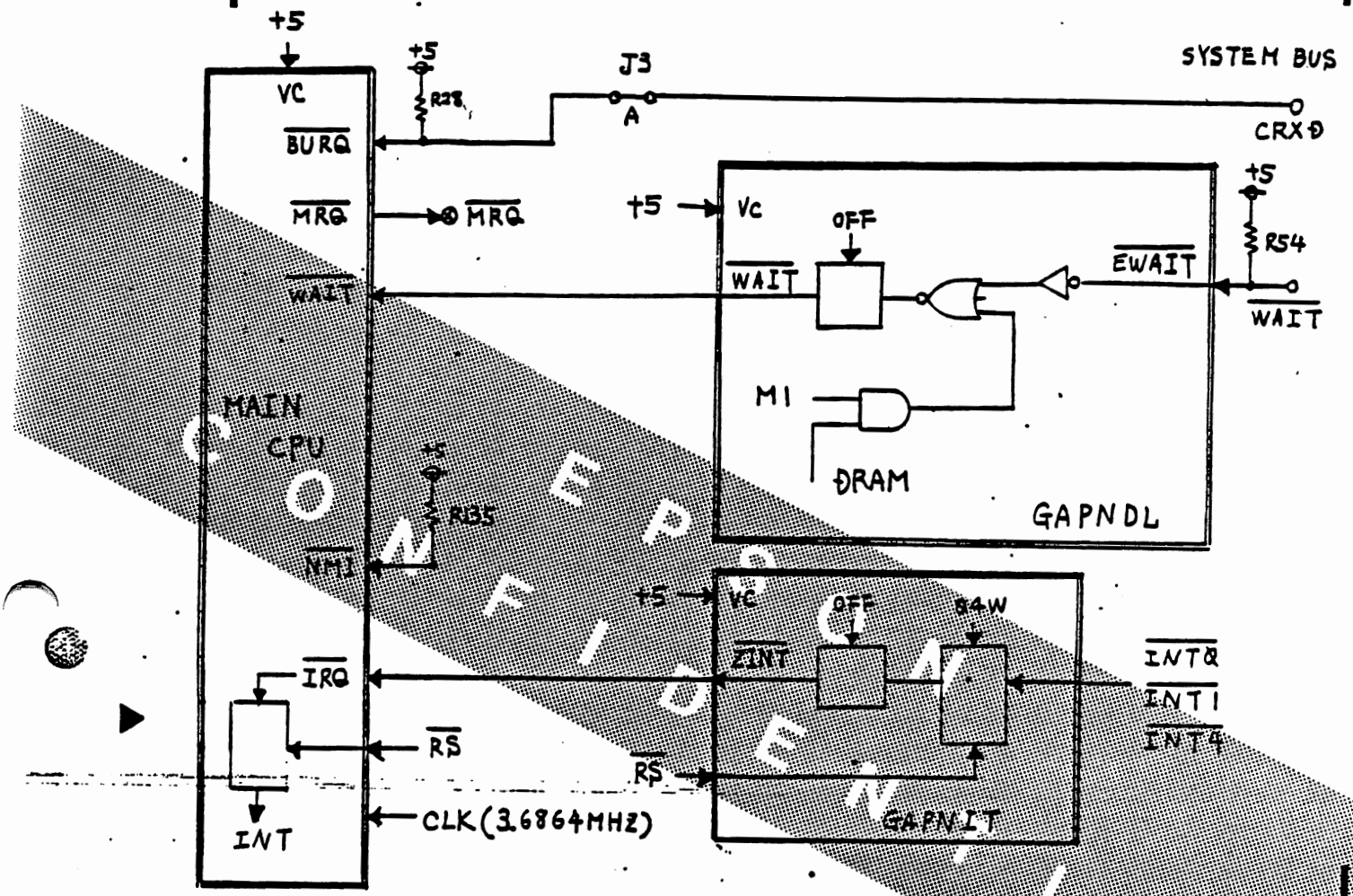

Fig. 2-47 Input signal of main CPU

If the reset signal is set to level H, the main CPU start the operation and outputs the memory request signal MRQ. At this time, if bus rquest signal BURQ or wait signal WAIT signal is set to level L, MRQ is not outputted. BURQ is the signal used to set the address bus and data bus of the main CPU and the system control output

to the high-impedance condition. This signal is kept to level H and used in case of DMA (Direct Memory Access). WAIT is outputted from GAPNDL when the dynamic RAM is accessed at M1 cycle. On receipt of this signal, the main CPU lengthen the access time of the ~~dram~~ DRAM.

The interrupt request (IRQ) is the interrupting signal inputted to the main CPU from outside, and the interruption can be prohibited or permitted by the software. Since inputting IRQ is prohibited by the resetting signal, the CPU is not interrupted until the resetting signal is released by the software.

Similarly, since inputting the interruption is prohibited by the resetting signals of the interruption controller, interruption input INT0 is not outputted to ZINT until the resetting signal is released by I/O command (04W).

The non-maskable interrupt (NMI) is kept to level H and not used.

WAIT signal of the system bus is kept to level H and used when accessing with an external RAM disc installed to the body.

While the power is turned off, outputs WAIT and ZINT of the gate array are set to the high-impedance condition by OFF signal.

2.5.16 Output signal of main CPU

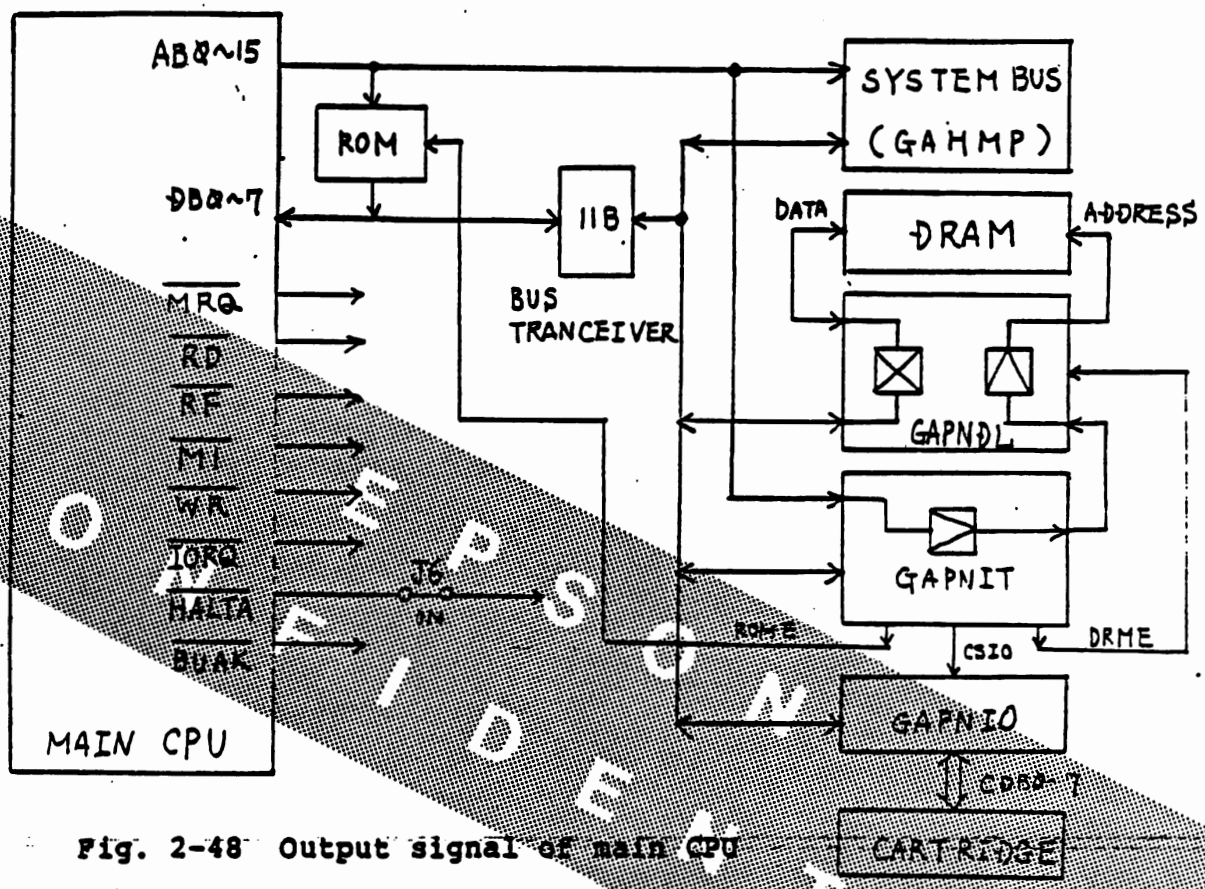

Fig. 2-48 Output signal of main CPU

The main CPU has the stand-by function to reduce the power consumption. If the main CPU is ready to receive an interruption signal from th key board, HLT commande is executed to set the main CPU to the stand-by mode, then the operation for the outside including the memory refreshing is stopped to reduce the power consumed in the circuit. Therefore, the main CPU cannot control the memory refreshing of the dram, but GAPNDL has this

performance instead. The stand-by mode is released when an interrupting signal is inputted, and the main CPU process the date, then set itself to the stand-by mode again.

While the resetting signal is inputted to the main CPU, the address bus and data bus are set to the high-impedance condition and all the control outputs are set to level H. When the main CPU is set to the stand-by mode, the outputs of the address bus and data bus are not stabilized (set to either level H or level L) and HALTA is set to level L and other control outputs are set to level H.

The role of the gate array connected to the main CPU is explained below.

GAPNIT controls all of the memory addresses and I/O addresses of PX-4 and outputs the enable signal to each IC. Therefore, the addresses (AB0 ~ 15) outputted from the main CPU are inputted to GAPNIT and decoded into the enable signals shown below.

(1) When accessing the ROM, the ROM enable signal (ROME) is outputted.

(2) When accessing the DRAM, the DRAM enable signal (DRME) is outputted.

(3) When using GAPNIO, the chip select IO signal (CSIO) is outputted.

(4) The I/O registers in GAPNIT are selected.

CAPNDL controls DRAM (64 kB). The address signals from the main CPU are converted into 16 - 8 signal lines within GAPNIT and inputted to GAPNDL. GAPNDL outputs these signals to DRAM and uses some of them to select the internal I/O registers. The data signals of DRAM is connected from GAPNDL to the main CPU. GAPNIO works as the interface when the main CPU controls the cartridge and I/O devices. GAHMP is connected to the system bus to control the additional memory.

Explanation of each output signal

Address bus AB0 - AB15 (Tri-state output)

The address bus outputs the memory address or I/O address. The memory address can appoint addresses up to 64 kB using AB0 - AB15. The I/O address can appoint up to 256 I/O ports using AB0 - AB15. Although the refreshing address is outputted from the address bus, it is not used.

Data bus DB0 - DB7 (Tri-state output)

The data bus is a two-way bus of 8 bits and used to transfer the data between the memory and CPU and between I/O devices and CPU.

Memory request MRQ (Tri-state output)

This signal is outputted when accessing the memory to indicate an effective address is outputted to the address bus.

Read RD (Tri-state output)

This signal indicates the data bus is in the input state. The memory or an I/O device outputs the data to the data bus synchronizing with this signal.

Refresh RF

This signal is outputted to refresh the dynamic memory. This signal is not used in this device to refresh the memory.

Machine cycle 1 M1

This signal indicates that the machine cycle currently executed is the instruction fetch cycle.

Right WR (Tri-state output)

This signal indicates that the data bus is in the output state. The CPU output the data to be sent to the memory or an I/O device to the data bus synchronizing it with this signal.

I/O request IORQ (Tri-state output)

This signal is outputted when accessing I/O devices and indicates that an effective I/O address is outputted to the address bus. This signal outputted together with MI indicates the acknowledge cycle of interruption, and the I/O device outputs the response vector to the data bus synchronizing with this signal.

Halt HALTA

This signal indicates that the CPU executed the HALT command. The CPU outputs this signal and set itself to the stand-by mode. GAPNDL refreshes the memory synchronizing with the M1 cycle, but if it receives this signal, it starts to refresh the memory according to the clock in the IC.

Be sure to turn on jumper plug J6 when using ?PD70008C as the main CPU.

Bus acknowledge BUAK

This signal indicates the the CPU received signal BURQ and set the tri-state output to the high-impedance condition. This is outputted in case of DMA (Direct Access Memory).

2.5.17

2.5.—

EPSON CORPORATION	TITLE	SHEET REVISION	NO.	
			NEXT	SHEET

P/42 2.5 Detailed Circuit Descriptions

The three gate arrays used in this computer are custom-designed and contains circuits of various functions. They are interrelated with each other in operation and, in addition, circuits of different functions are intermixed in each. Thus, their operations appears complicated to understand.

This section describes individual circuit operations along the flow of signals. Thus, the subsequent descriptions provide trouble shooting procedures including explanations on every check point.

Test point

The descriptions on internal operations of the gate arrays include block diagrams which help readers to understand internal signal flows and input conditions that are required for the circuit operations.

Most (of) trouble shooting in the area including the gate arrays are accomplished by determining whether the failure is in any one of the gate arrays or another element.

If no signal is observed at any output terminal of a gate array, all the associated input signals need to be examined.

P/43 2.5.1 Power Supply

The power supply control is described according to the figs. 2-28 and 2-29.

* Power on

(1) Even while the POWER switch is OFF, power is supplied from the auxiliary battery to circuits which need to operate and memory

for back-up.

(2) When the POWER switch set ON, 7508 detects it and activates the Power On (PON) signal high.

(3) The PON signal starts oscillating the DC-DC converter which supplies power to all circuits.

(4) Transistor Q16 turns off to disconnect the sub-battery from the power supply line. Transistor Q4 turns on at the same time which completes the operation of connecting the +5 V power source to the VB2 line.

* Power off

(1) While the POWER switch is ON, all the computer circuits are powered by the main battery or via the AC adaptor.

(2) When the POWER switch is reset OFF, transistor Q16 turns on to reconnect the sub-battery to the power supply line. At the same time, transistor Q4 turns off.

(3) The PON signal is deactivated low to stop the DC-DC converter. This completes the power off sequence.

(4) Even after ppwer turned off, memory is backed up and some other circuits are maintained active by the auxiliary battery.

* Power failure

When the Ni-Cd battery is exhausted and a power failure condition is detected, transistor Q14 connect the auxiliary battery to the VB1 line to maintain power supply until a power failure handling procedure is completed. When a temporary power failure

is detected due to surge current, no power failure handling procedure takes place because transistor Q14 connects the sub-battery to the VB1 line to maintain the +5 V supply stable.

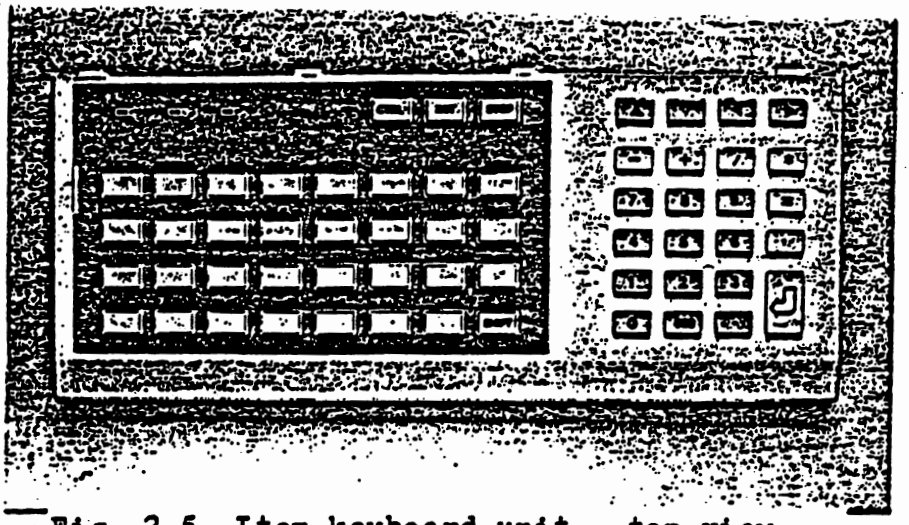

Fig. 2-5. Item keyboard unit - top view

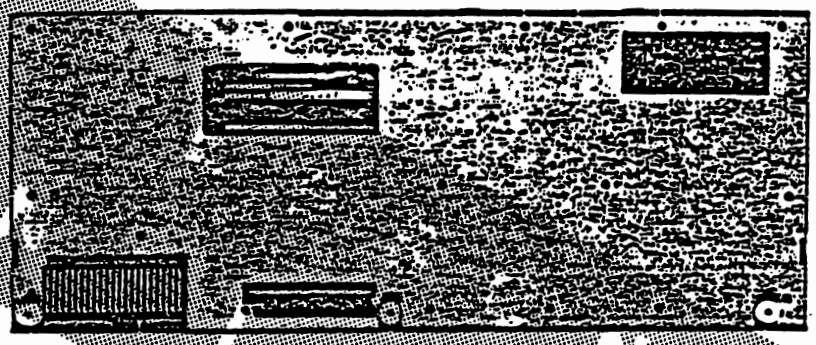

Fig. 2-6. Standard/item keyboard unit - bottom view

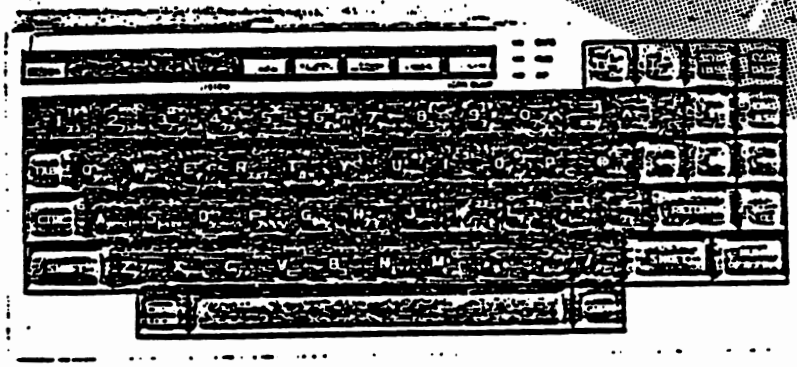

Fig. 2-7. Standard (Japanese) keyboard

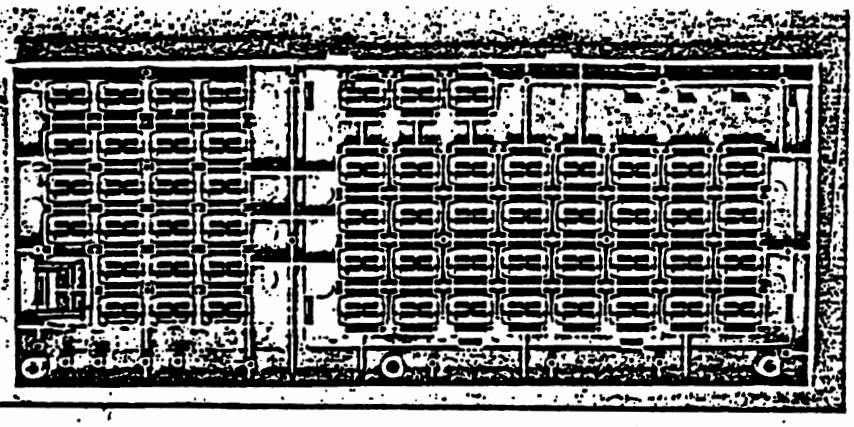

Fig. 2-8. Bottom of the item keyboard keytops

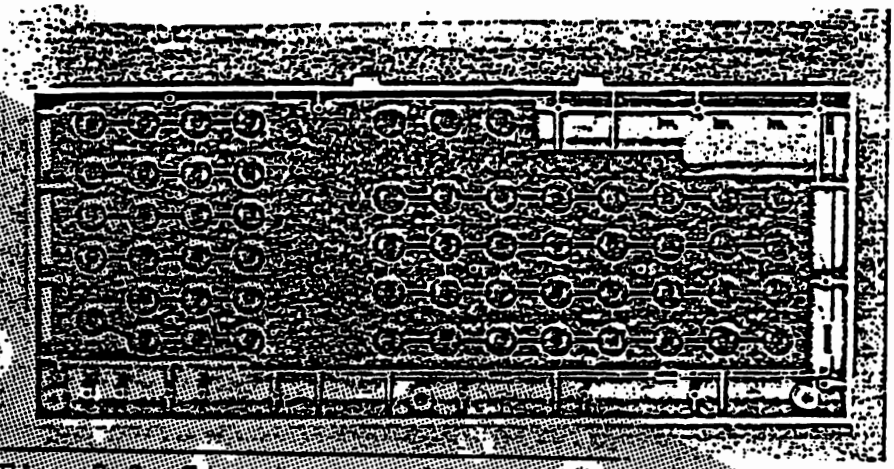

Fig. 2-9. Item key movable contacts (silicon rubber sheet)

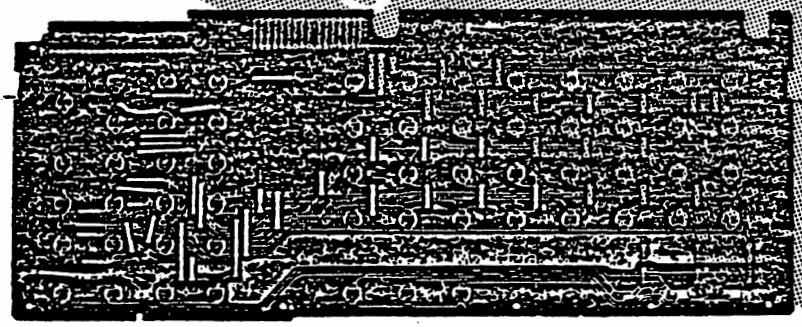

Fig. 2-10. Item key fixed contacts (pc board)

The standard and item keyboards are built in a three-layered structure as illustrated by figs. from 2-8 to 2-10. They can be completed by simply putting the pc board on the silicon rubber sheet and then the key panel on the pc board, and clamp them together with screws.

The movable contacts are conductive rubber chips which are embedded on the silicon rubber sheet. They make use of the elasticity of the silicon to minimize mechanical wear; thus ensureing longest life

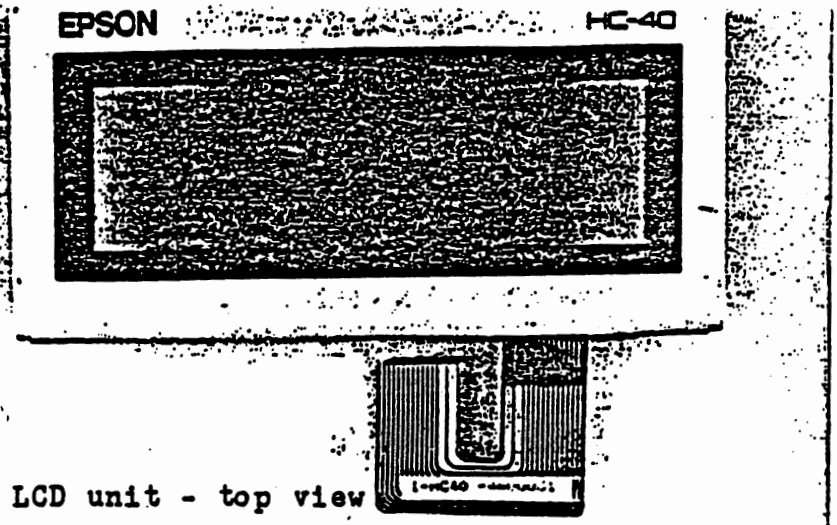

Fig. 2-11 LCD unit - top view

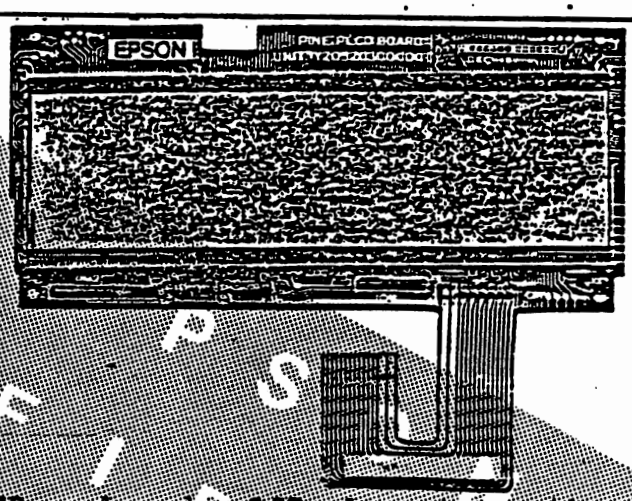

Fig. 2-12. LCD pc board - LCD element mounting side as covered with the panel plate

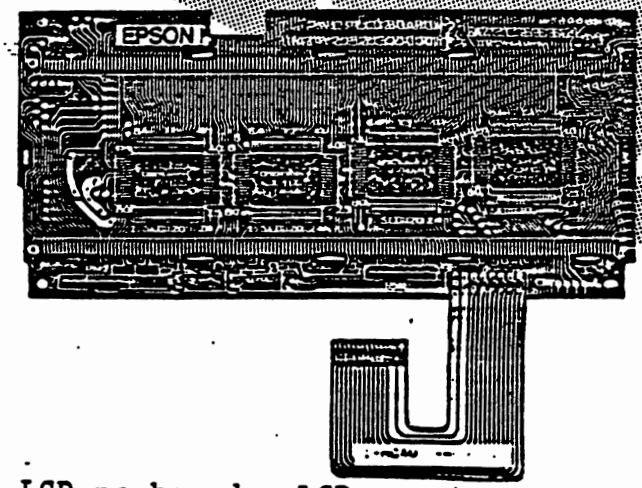

Fig. 2-13. LCD pc board - LCD mounting side as the panel - plate removed

Note: Metalic LCD panel clamps are removed in fig. 2-12.

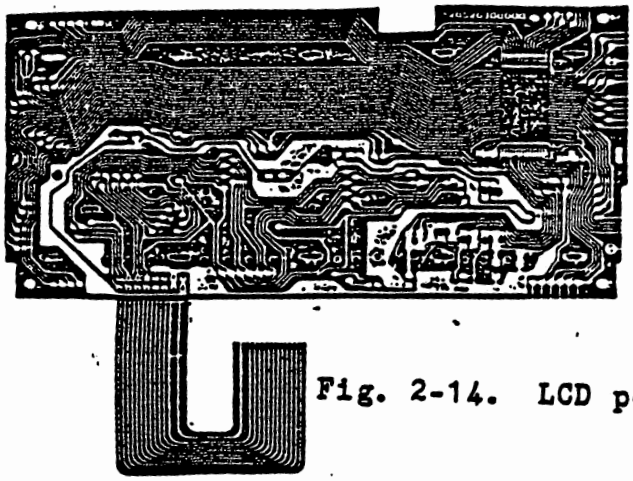

Fig. 2-14. LCD pc board - wiring side

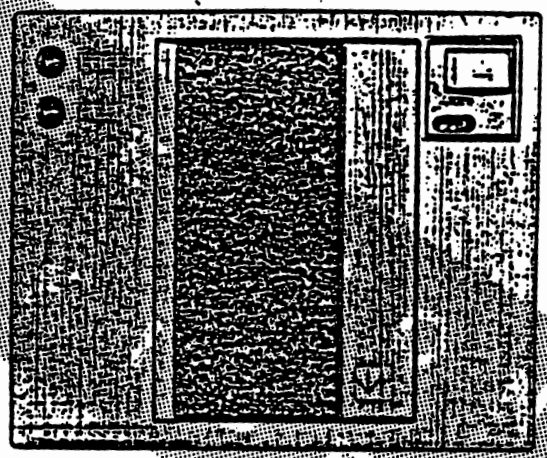

Fig. 2-15. Microcassette drive unit

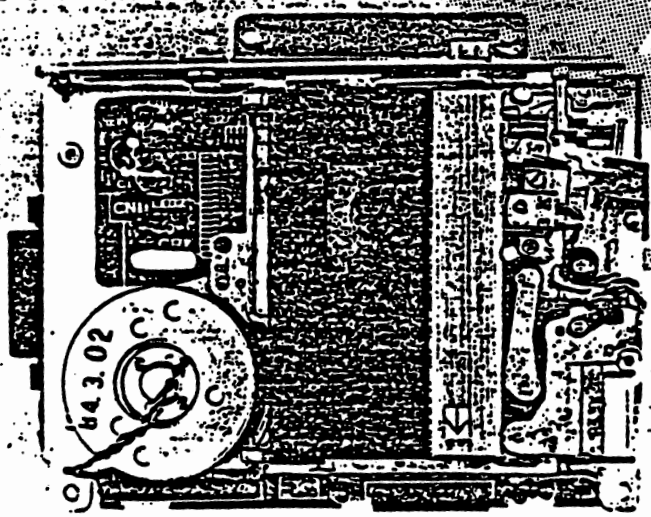

Fig. 2-16. Microcassette dirve mechanism

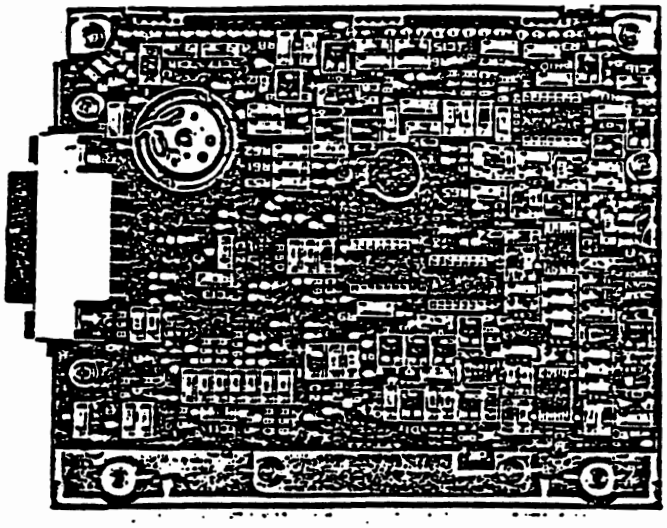

Fig. 2-17. Microcassette drive board - wiring side

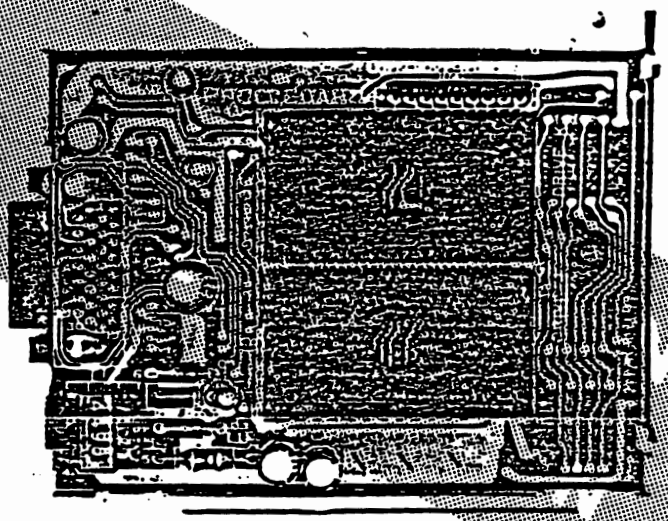

Fig. 2-18. ROM cartridge board - wiring side

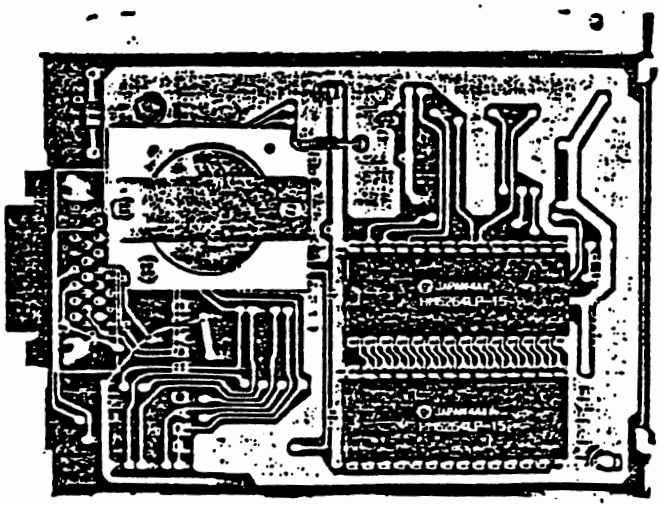

Fig. 2-19. RAM cartridge board - wiring side

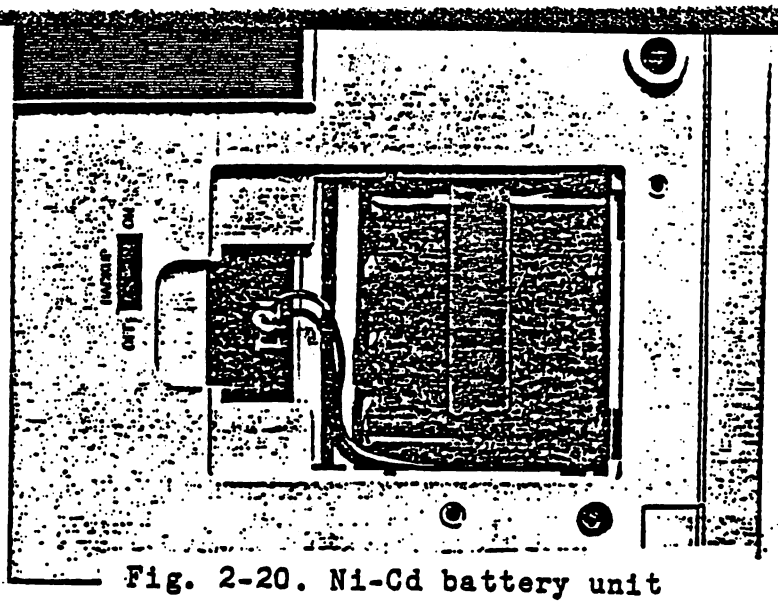

Fig. 2-20. Ni-Cd battery unit

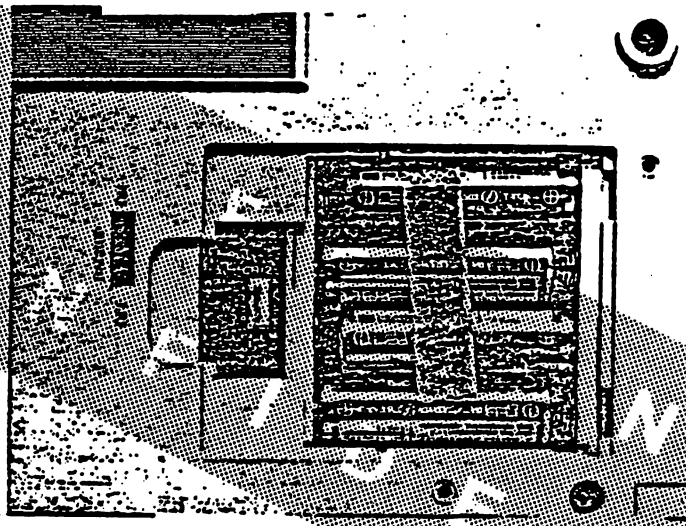

Fig. 2-21. Manganese batteries

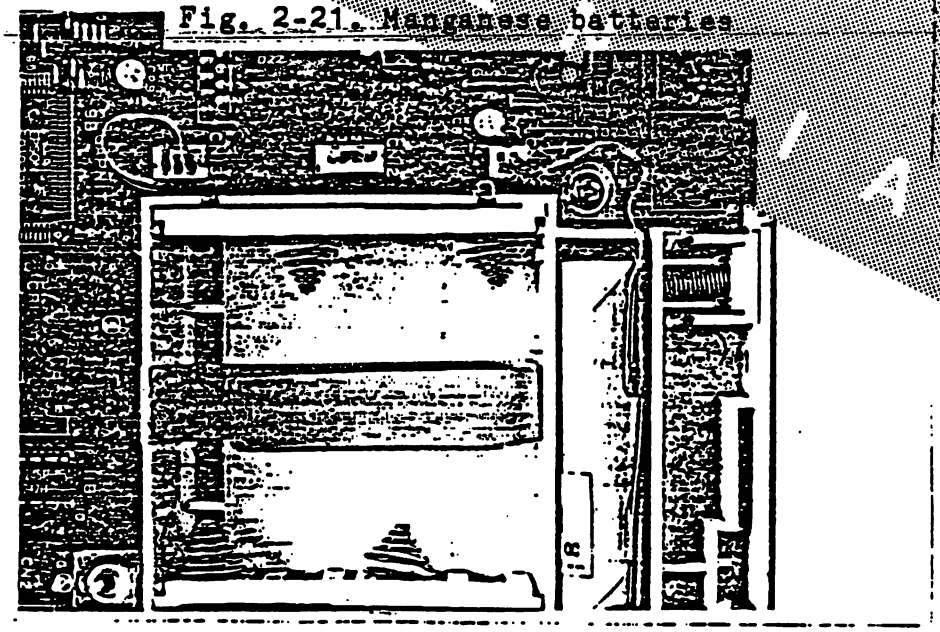

Fig. 2-22. Auxiliary battery

2.2 PINE Board

This section describes the individual circuits on the PINE board.

Fig. 2-25 is a block diagram of the maximum PX-4 hardware configuration. Most of the basic PX-4 functions are implemented by three custom IC elements (gates) and their surrounding circuits.

Fig. 26 is a circuit diagram of the PINE board. The subsequent descriptions are made according to this diagram.

Each circuit terminal, junction, or element is referred to by the coordinate on the diagram. The PINE board circuits are classified as follow for description:

1. Connectors
2. Switches
3. CPU, ROM, and RAM
4. Gate arrays
5. Clock oscillator circuits
6. 7508 CPU
7. 7508 surroudning circuits
8. Power supplies
9. Check terminals
10. Jumper plugs
11. Variable resistors

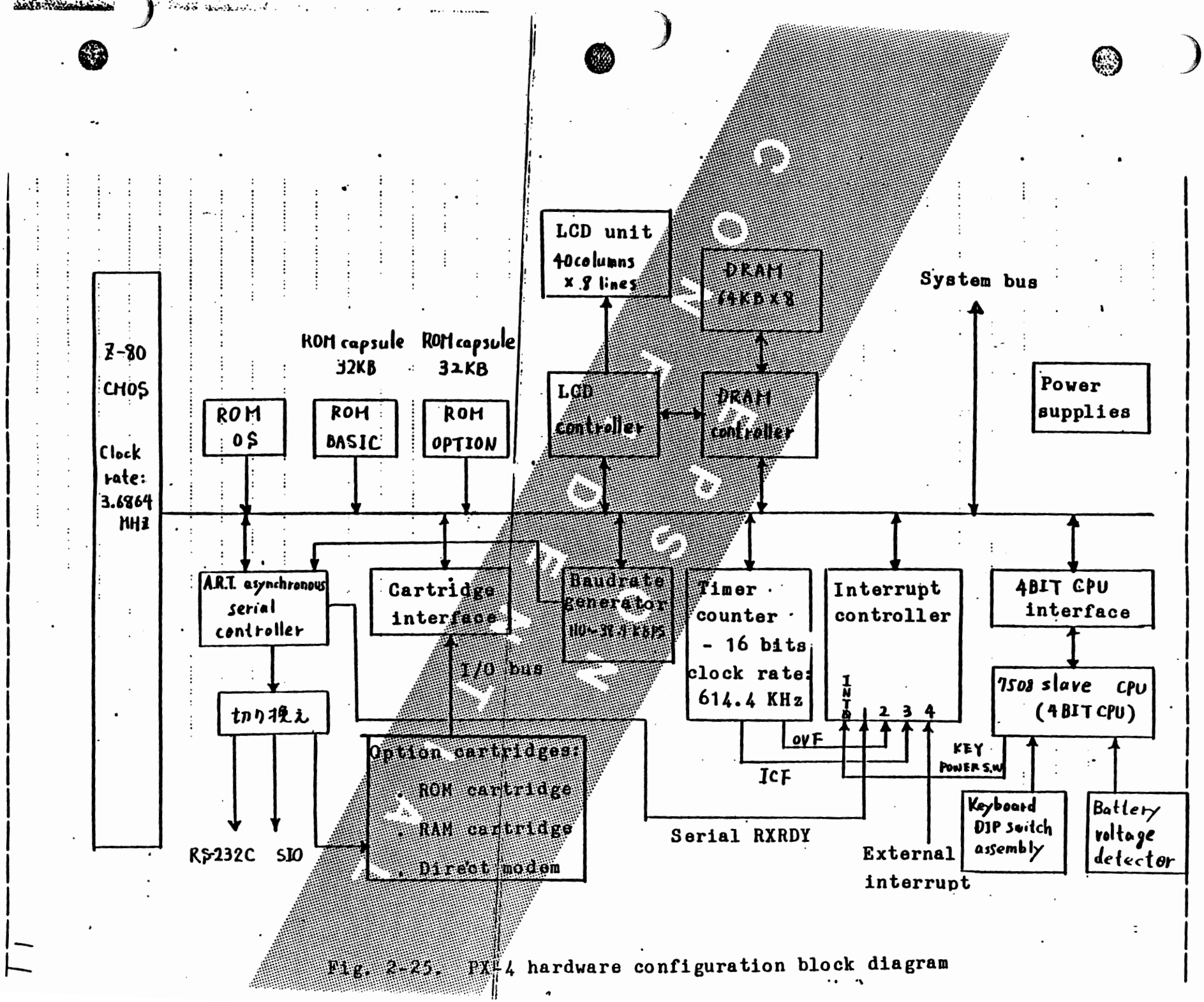

Fig. 2-25. PX-4 hardware configuration block diagram

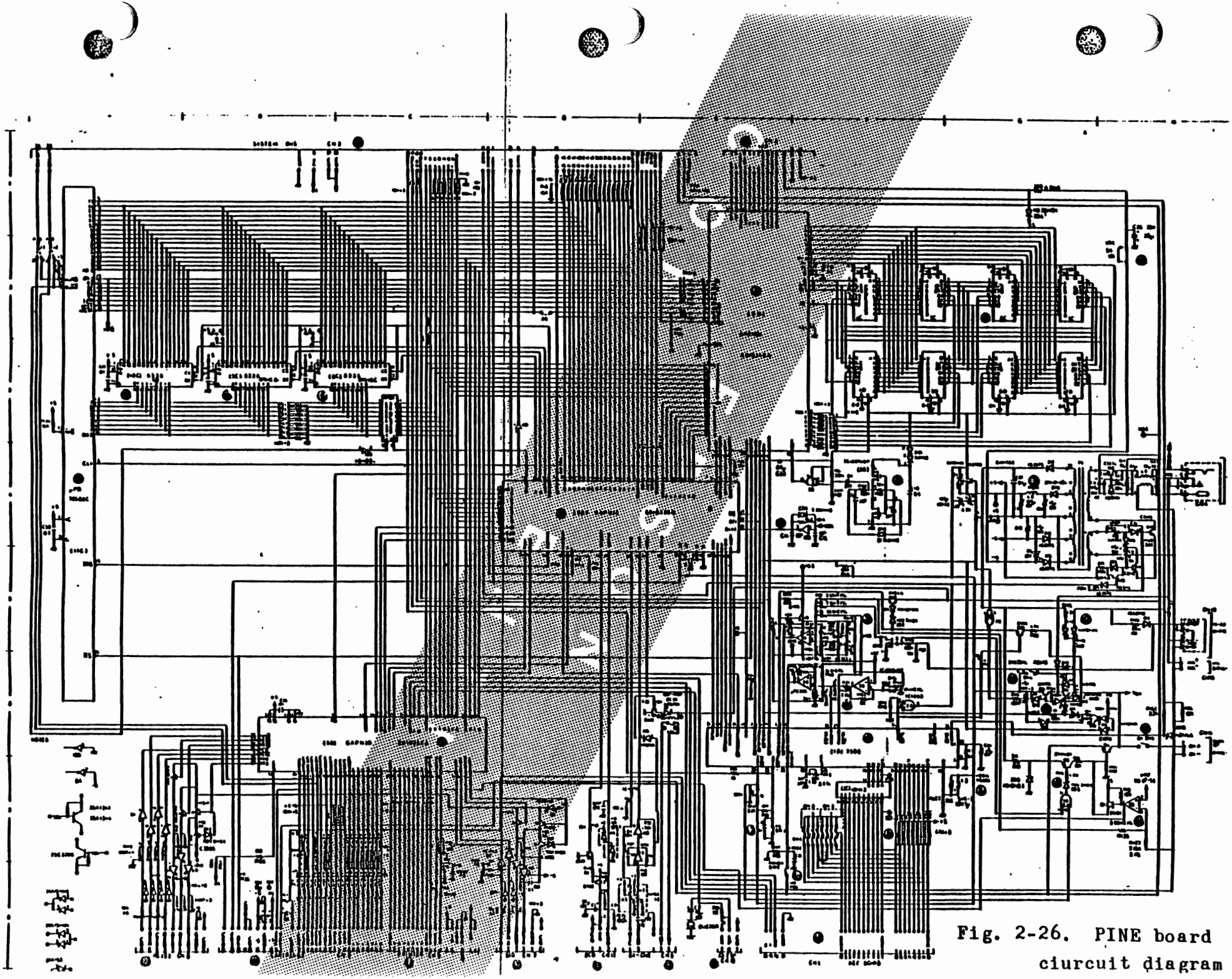

Fig. 2-26. PINE board
ciurcuit diagram

2.2.1 Connectors

(C-1) System Bus connector CN2

Connects the external RAM disk unit.

(E-1) LCD connector CN3

Connects the LCD unit.

(H-4) AC Adaptor connector CN4

Connects the AC adaptor.

(H-5) Main Battery connectors CN12 and CN13

Respectively connect manganese batteries or the Ni-Cd battery unit.

(H-6) Sub-Battery connector CN14

Connects the sub-battery unit incorporated in the computer.

(F-8) Keyboard connector CN1

Connects the standard or item keyboard.

An international character set is specified with the keyboard DIP switch assembly.

Either keyboard type (standard or item) is automatically set.

(A-8) RS-232C connector CN6

Connects the RS-232C cable.

(B-8) Cartridge connector CN9

Connects an option cartridge.

(C-8) Centronics Interface connector CN5

Connects a Centronics-compatible printer.

(D-8) Serial Interface connector CN7

Provides simplified RS-232C interface signals.

(D-8) Barcode Reader connector CN11

Connects a barcode reader.

The barcode reader interface is not supported by the operating system; an application program is required when using the bar-code reader.

(E-8) External cassette Recorder connector CN8

Connects an external cassette tape recorder.

(E-8) External Speaker connector CN10

This connector output is used for microcassette drive azimuth adjustment.

2.2.2 Switches

(F-8) POWER switch SW1

Turns the PX-4 on and off.

(E-7) Reset switch SW2

Resets the main PCU.

(G-6) Initial Reset switch SW4
(G-7)

Initializes the PX-4 system; it also resets 7508.

(H-6) Back-Up switch SW6

Prevents discharge of the sub-battery. This switch is set OFF for shipment. It should be set OFF when the PX-4 is stored for a long time or re-shipped.

(F-7) Keyboard DIP switch assembly SW5

Selects an international character set and a device to which data are directed. When either setting of this switch assembly is changed, the Reset switch needs to be pushed.

2.2.3 CPUs, ROM and DRAM Elements

(A-4) Main CPU

A Z-80 compatible CMOS CPU which operates at a clock rate of 3.6864 KHz. It is provided with a stand-by feature which can minimizes power consumption.

(A-3) Operating System (OS) ROM

This is a 32K byte CMOS mask ROM element which contains the PX-4 operating system. It is inserted into an IC socket for easy replacement.

(B-3) ROM Capsule (9C)

This capsule can ~~entirely~~ contain a CMOS ROM element. Because of its capsule structure, the ROM element can be easily installed and removed.

Normally BASIC ROM is installed in the capsule. It is assigned a drive name B; key in or write "DRIVE B:" when accessing the ROM element.

(B-3) ROM Capsule (8C)

Same as the above capsule (9C).

Normally an application ROM element is installed in this capsule. It is assigned a drive name B; key in or write "DRIVE C:" when accessing the ROM element.

Notes:

CMOS ROM elements should be installed in the capsules. NMOS ROM elements consume more power and are less preferable. An 8K, 16K, or 32K byte mask ROM element can be used. An 8K or 32K CMOS E-ROM element can also be used.

The setting of the jumper plugs J4 and/or J5 must be changed according to the element type whenever the current one is repaced as follows:

32K and 16K byte ROM: Jumper B and open A.

8K byte ROM: Open B and jumper A.

When writing programs in ROM elements, special care must be taken of addresses.

(G-2) 64K byte DRAM

Eight 65,536-byte dynamic RAM IC elements are used here. Since each IC corresponds to a bit of one byte, the eight ICs are accessed at the same time.

The ICs are backed up by the sub-battery; they are self-refreshed while the POWER switch is OFF.

The ICs are NMOS.

2.2.4 Gate Arrays

(E-2) GAPNDL (Gate Array for PINE DRAM and LCD Controller)

This gate array controls the PINE DRAM and LCD unit.

The IC is backed up by battery, the internal states are maintained unchanged if the POWER switch is set OFF.

The internal gate array circuit is made up of approximately 800 CMOS cells.

(D-4) GAPNIT (Gate Array for PINE Interrupt and Timer Controller)

GAPNIT is also one of the PINE gate arrays and incorporates the following circuits:

* Address decoder
* Address multiplexer
* Interrupt controller
* Timer and baudrate generator
* 7508 interface
* I/O ports

This IC is backed up by battery.

(C-6) GAPNIO (Gate Array for PINE Input/Output Controller)

This is another PINE gate array which controls the I/O devices. It is not backed up by battery.

2.2.5 Clock Oscillator Circuits

(E-4) System Clock Oscillator circuit

This is a 7.3728 MHz crystal oscillator circuit. The system clock signal is generated by halving this signal.

The oscillator starts oscillating when PX-4 is turned on.

(F-4) Calendar Clock Oscillator circuit

This is a 32.768 KHz crystal oscillator circuit. A calendar clock built in the computer is driven by the output of this oscillator.

The oscillator is maintained oscillating by the back-up battery if PX-4 is turned off.

2.2.6 7508 CPU

(F-6) 7508 Slave CPU

This is a 4-bit CMOS CPU which has control programs in its ROM.

The CPU is backed up by battery and operates in a stand-by mode to minimize power consumption while the POWER switch is OFF.

It operates by a clock signal of approximately 270 KHz generated by a built-in oscillator.

The features and functions of the slave CPU are summarized:

(1) Calendar clock

7508 internal memory provides a calendar clock feature

regardless whether the POWER switch is ON or OFF.

(2) Temperature sensing DRAM control

While PX-4 is turned off, this feature senses DRAM temperature and provides an optimum DRAM refresh control.

(3) Keyboard control

7508 controls the keyboard as long as the the POWER switch is ON.

(4) Turning PX-4 on/off

7508 turn PX-4 on by sensing that the POWER switch is set ON. It turns PX-4 off by a command received from the main CPU.

P/20

(5) Reset signal output

7508 detects the change of the Reset switch state and outputs a reset signal to the main CPU.

(6) Low voltage detection and switching to sub-battery

7508 always monitors the main battery voltage. When the voltage goes below a certain limit, it connect the sub-battery to the battery power line.

(7) Interrupt signal output

7508 outputs an interrupt signal to the main CPU when:

* Power fails,
* A key is pressed,
* The POWER switch is set ON/OFF,
* The alarm signal is generated, or
* An 1-second interval signal occurs.

(8) Serial data transfer

Serially exchanges data and commands with the main CPU.

(9) Timing alarm detection

7508 detects an timing alarm which is programmed to occur at a specified time and provides the following system start-up functions:

* Turns PX-4 on when it has been off.
* Outputs an interrupt signal when PX-4 has been on.

2.2.7 Circuits Surrounding 7508

(F-7) Keyboard Control circuit

The keyboard key switches are wired in a matrix. 7508 scans the switches in blocks to read any key pressed. The keyboard DIP switch is also read as a key block.

The LEDs on the keyboard are controlled via GAPNIO.

(F-6) Temperature Sensing circuit

This circuit detects temperature changes across 25°C and 45°C in DRAM ambience. From these results, 7508 selects a DRAM self-refresh mode which optimizes power consumption.

The circuit operates at an interval of 10 seconds while the POWER switch is OFF.

(F-5) Low Battery Voltage Detection circuit

This circuit detects a low voltage condition of the main battery through comparison with a reference voltage (V_{RF}) of 1.6 V.

When the low voltage condition is detected, 7508 outputs a Power Failure signal to the main CPU.

The low voltage varies depending on battery as follow:

* Manganese battery: Approx. 4.0 V

* Ni-Cd battery: Approx. 4.8 V

Like the Temperature Sensing circuit, this circuit operates at a 10-second interval for minimum power consumption while the POWER switch is OFF. 7508 controls power supply to these circuits. Both the circuits remain powered as long as the POWER switch is ON.

P/22 2.2.8 DC Power Circuits

(G-4) DC-DC converter

This is a self-oscillating DC-DC converter circuit which uses the stabilized input +5V supply from the main battery or AC adaptor.

7508 can control the oscillation of this circuit which turns on and off the power supply to the main CPU. That is, the main battery always stays connected to the main CPU; the POWER switch does not directly cut and connect the supply current.

(G-5) Auxiliary Battery Charging circuit

The auxiliary battery is a re-chargeable Ni-Cd battery and charged when:

* The AC adaptor is connected,
* The PINE board is powered from the AC adaptor - the sub-battery is charged from either teh AC adaptor or DC-DC converter output.
* The PINE bosrd is powered from the main battery - the sub-battery is charged from the DC-DC converter

When the Ni-Cd main battery unit is used, it can be chrged from the AC adaptor by connecting the battery connector to receptacle CN12.

(G-7) Auxiliary ~~Sub~~-Battery Connecting circuit 1

The PINE board is normally powered by the main battery. When the main battery voltage goes below a certain limit, however, this circuit connect the auxiliary-battery to the main battery ~~with the sub-battery~~ to allow the main CPU to accomplish power failure handling.

(H-7) Auxiliary ~~Sub~~-Battery Connecting circuit 2

This circuit connects the auxiliary ~~sub~~-battery to the main battery to prevent voltage fluctuation on the battery line when the main battery voltage temporarily drops to 3.6V or below due to overload. Power failure is not detected at this voltage drop.

P/23 (G-6) VB2 Switching circuit

This circuit controls connection of the back-up battery (main or sub-battery) to the back-up power line VB2 as follows:

* Connects the back-up battery to VB2 when the POWER switch is OFF.
* Disconnect the back-up battery from VB2 when the POWER switch is ON because the +5V power is connected to the line.

The circuit is ~~fairly complicated~~ somewhat elaborated in order to suppress abrupt voltage change at VB2 line switching.

(H-4) AC adaptor

When plugged in CN4, the AC adaptor is connected in parallel with the main battery.

The adaptor output is stabilized through a noise filter and constant voltage regulator circuit.

Because the constant voltage regulator output is selected higher (6.5V) than the main battery voltage so that the battery is prevented from discharging when the AC adaptor is used.

The AC adaptor charges the Ni-Cd battery as well as supplies power to the PX-4 circuits. The battery is charged directly from the adaptor output; an adaptor which does not meet the specification may result in a problem, if used. The output rating is:

DC 6V, 600mA

(H-5) Ni-Cd Battery unit (CN12)

This is a battery assembly which contains four Ni-Cd batteries (size: AA, IEC: R6) connected in parallel and has a lead connector attached. This connector also serves as a short plug which allows charge to the battery.

Because of its lower internal impedance, the Ni-Cd battery unit is ideal when using the cartridge printer or microcassette drive. The cartridge printer is especially designed for use with the Ni-Cd battery unit. The battery unit can support the standard PINE circuit for four hours after charged for eight hours.

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It is rated as follows:

Output voltage:	4.8 V
Capacity:	450 mAH
Charge current:	Approx. 70 mA
Charge time:	8 hours
Life:	500 cycles

(H-5) Manganese Batteries (CN13)

Four unit-3 manganese batteries (size: AA, IEC: R6) connected in series can be used as main battery in place of the Ni-Cd battery unit.

Because the output voltage of the batteries (6 V) is higher than that of the sub-battery, the back-up current is mainly supplied from these batteries.

The manganese batteries have a higher internal resistance and their output voltage is more affected by load current fluctuation.

~~Two types of manganese batteries are available which have~~ the following lives for the standard PINE circuit:

* Manganese battery: 5.5 hours
* Alkali manganese battery: 11.5 hours

(H-6) Auxiliary ~~Sub~~-Battery (Back-up Battery)

This battery is incorporated in the computer for the purpose of memory back-up. It provides a capacity which can back up memory for about one week. When manganese batteries are used as main battery, the back-up current is supplied from them. When the Ni-Cd battery unit is used whose output voltage is lower, the back-up current is supplied from the Auxiliary ~~sub~~-battery.

The battery is rated as follows:

Output voltage:	4.8 V
Capacity:	90 mAH
Charge current:	3 mA

P/25 2.2.9 Check Terminals ..... Test Points???

(H-3) VB1: Battery voltage

(F-5) VB2: Back-up voltage

(G-4) +5: +5 V output voltage

(F-5) GND: Signal ground

(E-5) X1: Calendar clock signal (1 KHz)

(F-5) VRF: Reference voltage for low ~~battery~~ voltage detection

(F-7) PJ0: 7508 oscillator frequency adjustment

(F-7) SCN: Keyboard scan signal

(A-2) MRQ: Mmeory request signal

2.2.10 Jumper Plugs

(E-7) J1: Normally open, jumpered for testing 7508.

(A-2) J2 - A: Jumpered (BUAK), B: Open

(A-2) J3 - A: Jumpered (BURQ), B: Open

(B-2) J4 - A: Open, B: Jumpered (32KROM)

(B-2) J5 - A: Open, B: Jumpered (32KROM)

(D-2) J6: Normally jumpered, open for using CPU other than 70008C.

2.2.11 Variable Resistors

(H-2) VR1: Adjusts LCD contrast.

(F-7) VR2: Selects the 7508 oscillator frequency.

Reset the POWER switch OFF, jumper J1, and push the Initial Reset switch. Then, adjust the signal cycle to 50 ms with this variable resistor - observe the signal at check terminal P30.

(F-5) VR3: Adjusts the low battery voltage reference voltage.

Adjust the voltage at check terminal VRF to 1.6 V with this variable resistor.

2.3 Outline of Circuit Operations

2.3.1 Circuit Operating Principles

(1) The PINE board contains the two CPUs: main and slave (7508) which respectively control the following devices:

* Main CPU: RS-232C, SIO, printers, cartridges, external RAM disk, buzzer, external cassette recorder, and barcode reader
* Slave CPU (7508): Keyboard, calendar clock, and batteries

The main CPU issues commands to the slave CPU which sends interrupt and reset signals to the main CPU to control each other.

(2) Part of the PINE board circuit continues operating while PX-4 is off. The rest operates only while PX-4 is on. That is, 7508 is always powered which controls power supply to the main CPU by sensing the change of the POWER switch setting.

(3) To continue the previous processing by turning PX-4 on after an interruption (in a Continue mode), memory data and various control circuit status need to be maintained as they are while power is off.

The PINE board implement this Continue mode by backing up

DRAM, two gate arrays, and 7508 from battery.

(4) 7508 maintains the calendar clock and controls the power supply. The POWER switch does not directly shut off or supply the current but it only supplies a low/high level signal to 7508 which controls turning power on/off.

The calendar clock and power controlling backed up by battery on the PINE board are combined to provide useful features such as Time Alarm, Wake, and Auto Power Off.

P/27 (5) The following considerations are implemented on the PINE board to minimize battery consumption:

* CMOS IS elements are used.
* The main and slave CPUs operate in a Stand-by mode until they start operating after "woken" by an interrupt.
* 7508 provides a DRAM refresh control, which optimizes the refreshing current, by sensing the ambient temperature.
* Programs can be executed in ROM instead of RAM so that power consumption can be reduced.
* The Auto Power Off feature automatically turns PX-4 off in five minutes if the POWER switch is left ON.
* Option cartridges are operated only when required.
* The LCD unit minimizes current requirement for display.

(6) The rechargeable sub-battery is used in addition to the main battery in order to allow main battery replacement without destroying memory data. The sub-battery is mainly used for memory back-up.

(7) Either manganese batteries or a Ni-Cd battery unit can be

used as main battery.

By combining main battery and AC adaptor, PX-4 can operate uninterruptedly.

(8) Main memory consisting of RAM and ROM elements which are arranged in different backs are linked to common address lines, and is addressed by selecting either bank.

RAM is DRAM elements and refreshed at an interval.

(9) Display data are written in a specific DRAM area as a bit image and output to the LCD unit under the control of gate array GAPNDL. The LCD panel electrodes are arranged in a 240 x 64 dot matrix and dynamically driven at a duty cycle of 1/64.

(10) PX-4 is desinged to be able to use either the standard or item keyboard.

P/28 2.3.2 Circuit Block Diagram

The data and command transfer (paths) between the main CPU, ROM and RAM, slave CPU (7508), and gate arrays are summarized in fig. 2-27. (GAPNIT, GAPNIO, GAPNDL)

* The main CPU output signals are sent to 7508, GAPNIO, and GAPNDL via GAPNIT.
* The signal to RAM is sent via two arrays GAPNIT and GAPNDL.
* The signals from the switches and keyboard are sent to the main CPU via 7508.
* The I/O devices are controlled by GAPNIO.
* The external RAM disk is directly controlled by the main CPU.

2.3.3 Basic Operations

The basic PINE board operations are explained below ~~according~~ in the

the order numbered on the figure.

(1) PX-4 is turned on by 7508.

When the POWER switch is set ON, 7508 turns the main CPU on. While the POWER switch is OFF, 7508 internal RAM functions as the calendar clock. If an alarm time is set, PX-4 is automatically turned on when the alarm occurs.

(2) While power is off, 7508 keeps activating the Reset signal to the main CPU. When turned on, 7508 removes this reset signal. Pushing the Reset switch while power is on causes the main CPU to be reset.

(3) When the Reset signal is removed, the main CPU reads and executes the ROM program from the beginning. After this, PX-4 is put under the control of the ROM program.

P/29 (4) The main CPU initializes the gate array registers.

(5) The main CPU sends commands to 7508 and reads status from 7508 which tells to the CPU what started it. This allows the main CPU to select the program to be excuted next.

The main CPU may be started when:

* The POWER switch is set ON,
* The time alarm is activated,
* The Initial Reset switch is pushed, or
* The Reset switch is pushed.

(6) The main CPU accesses RAM whenever requested. A part of RAM is reserved for display whose contents are incessantly read by gate array GAPNDL.

(7) When a display enabling command is sent from the main CPU

to GAPNDL, the DRAM contents are displayed on the LCD panel.

(8) The keyboard is controlled by 7508 which reads the type of the keyboard unit and converts key codes according to the type. Each key stroke is detected by 7508 which outputs an interrupt signal to the main CPU. In turn, the main CPU returns a command to 7508 as an acknowledgement. Receiving the command, 7508 sends the key code to the main CPU.

(9) GAPNIO serves as an interface between the main CPU and various I/O devices. Thus, the main CPU exchanges data with the devices via GAPNIO.

(10) When a cartridge is attached, the main CPU reads the type of the carteidge and selects the program which processes the cartridge. When transferring serial data, the main CPU set a data which indicates the I/O connector to be used because the RS-232C, SIO, and cartridge connectors cannot be simultaneously used.

When outputting data to an I/O device, the main CPU has no way to know to which connector to direct the data. Thus, the user assembly sets a connector to the keyboard DIP switch which is read by the main CPU to determine the proper output connector.

P/30 (11) When the POWER switch is reset OFF, 7508 interrupts the main CPU. The interrupted main CPU sends a command to 7508 to read the status from 7508 which tells that the main CPU was interrupted for power off, Then, the main CPU performs a power off procedure.

The main CPU is interrupted for power off when:

* The POWER switch is reset OFF.
* A power failure is detected.

(12) PX-4 is turned off by 7508. After completing a procedure required before turning PX-4, the main CPU sends a power off command to 7508 which, receiving this command, turn PX-4 off.

This is a normal procedure. The main CPU, however, can turn PX-4 off at any time.

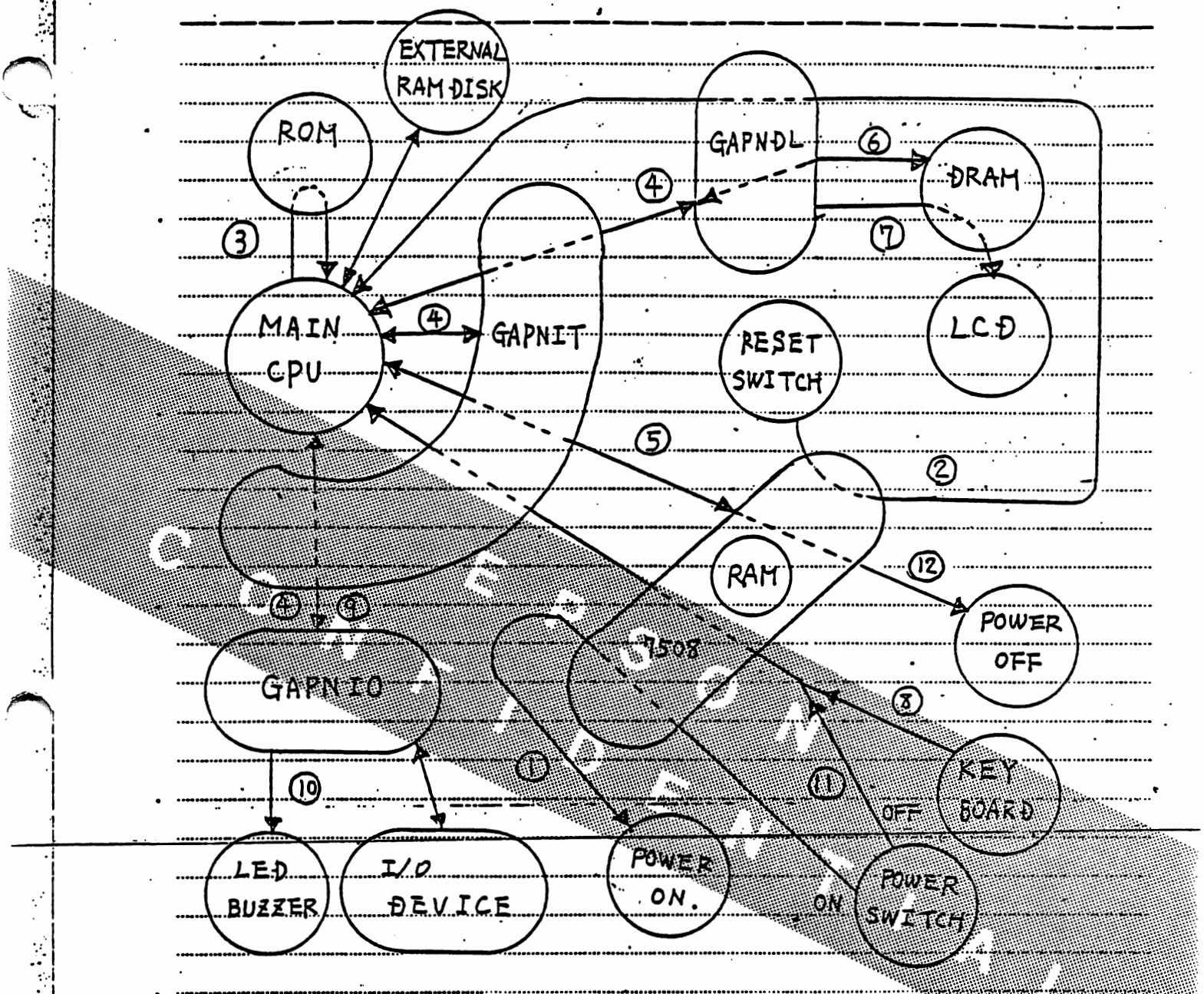

Fig. 2-27. PINE board circuit block diagram

① Power-off signal
② Reset signal
③ ROM read
④ Gate array initialization
⑤ Command/status code
⑥ DRAM access
⑦ Display enabling
⑧ Interrupt signal (key entry)
⑨ I/O register access
⑩ I/O device control
⑪ Interrupt signal (power off)
⑫ Power-off command

2.4 Circuit Operation Synopses

2.4.1 Power Off

(1) The back-up (main or sub-) battery supplies power to the following circuits through the VB2 switching circuit (Q16):

* DRAM
* GAPNDL
* GAPNIT
* 7508
* Calendar clock oscillator circuit (3D)
* POWER switch control circuit (2B)

(2) During this time, the Reset and OFF signals are applied to the two gate arrays to protect the data stored in their registers. The contents of 7508's internal memory are also maintained by uninterrupted power supply from the back-up battery.

(3) DRAM is internally refreshed.

(4) 7508 keeps sensing the ambient temperature at a 10-second interval and selecting the optimum refresh mode to minimize DRAM power consumption.

(5) 7508 keeps counting the calendar clock up every 10 seconds.

(6) 7508 maintains the set alarm time. When the Wake alarm occurs, turns PX-4 on and tarts up the main CPU. All these 7508 actions are starded at a 10-second interval from the Stand-by mode in order to minimize battery power consumption.

(7) When the POWER switch is set ON, 7508 detects this status change and turn the main CPU on.

(8) The above actions continue until memory contents are destroyed due to back-up battery exhaustion and the circuits cannot be normally operate.

Contents of DRAM are destroyed when VB2 drops to 4.2 V or below:

* ~~Minimum~~ Lowest guaranteed VB2 voltage: 4.5 V

* Critical VB2 voltage: 4.2 V

(9) Destruction of memory contents while backed up is indicated by a system initialization image appearing on the CRT screen when PX-4 is turned on. This indicates that the previous data in memory are all lost.

(10) The sub-battery is charged if the AC adaptor is used in addition to the main battery.

2.4.2 Power Off to Power On

(1) When the POWER switch is set ON, 7508 enables the DC-DC converter to supply power to the main CPU. However, power is not turned on if 7508 detects a power failure at this time because of main battery voltage drop. When this occurs, reset the POWER switch OFF and replace the main battery or use the AC adaptor.

(2) 7508 starts up teh main CPU through thefollowing control sequence:

* Turns power (+5) on - this starts system clock oscillation.
* Removes the OFF signal - this causes the gate arrays to be powered leaving from the previous backed-up memory state: the deactivation of the OFF signal causes the VB2 switching circuit to disconnect the sub-battery from the VB2 line.
* Removes the Reset signal - this enables the main CPU and gate arrays to start operating. In addition, teh DRAM refresh mode changes from self- to memory refreshing via GAPNDL.

(3) After the Reset signal is removed, the main CPU runs the operating system program which accomplishes the following:

* Reads the status from 7508 - the main CPU knows from this status data that the POWER switch is set ON and performs necessary procedure: the main CPU examines here what started it. The main CPU may be started when:
  * The Reset switch is pushed,
  * The Initial Reset switch is pushed,
  * PX-4 is turned on by the time alarm feature, or

The POWER switch is set ON.

* Initializes the gate arrays.
* Examines the memory check sum to see if memory contents are destroyed. If the check sum is incorrect, the system initialization image appears on screen, indicating that memory contents may be destroyed due to battery voltage drop, etc.
* Examines the capacity of the ROM capsule (32K, 16K, or 8K bytes) if it is installed.
* Examines the capacity of the internal RAM disk.
* Examines the capacity of the external RAM disk (128K or 64K bytes) if attached.
* Examines what is connected to the cartridge connector.
* If a RAM cartridge is connected, examines its capacity (64K, 32K, or 16K bytes).
* If a ROM cartridge is connected, examines its capacity (32K, 16K, or 8K bytes).
* If a microcassette drive is connected, examines whether the previous operation has been interrupted by the power off. If interrupted, continue the operation. That is, the microcassette drive can also operate in the Continue mode.

(4) Depending on how PX-4 was turned off, the initial menu or BASIC initialization image appears on the screen.

If it was turned off in the Continue mode, the main CPU resumes the previous program.

2.4.3 While PX-4 Is On

(1) When power is on, the PX-4 circuits are powered by the DC-DC

converter and the auxiliary battery is charged.

The DC-DC converter ensures a stable +5 V supply if the battery voltage fjuctuates. The converter is powered by the main battery or AC adaptor. When both are connected, the AC adaptor is given priority.

(2) When the battery voltage drops and 7508 detects power failure, the main CPU turns PX-4 off. Even after power fails, however, the DC-DC converter output voltage is still stabilized. Thus, the +5 V supply is stable whenever the main CPU is operating.

(3) As long as power is on, 7508 keeps controlling the keyboard; it does not enter the Stand-by mode. After PX-4 is turned on, DRAM is refreshed by GAPNDL and 7508 needs not provide the relf-refresh mode. Thus, the ambient temperature sensing circuit is not used.

However, the low battery voltage detection and temperature sensing circuits remain powered.

(4) When power is on, the calendar clock is counted every 10 seconds.

When the time alarm occurs, 7508 interrupts the main CPU. The interrupted main CPU issues a command to 7508 to read the 7508 status. After knowing that the tiem alarm occurred, the main CPU takes the following actions:

* Interrupt the program currently being executed.
* Generates an alarm sound and displays an alarm image.
* Returns to the previous (interrupted) program if the ESC key is pressed.

* If no key is pressed, returns the previous program 50 seconds after the alarm occurs.

/36 (5) The main CPU operates in the Stand-by mode. This feature is specific to the CMOS version of Z-80. It is not available with original version.

The main CPU enters the Stand-by mode whenever it waits for key entry in order to minimize battery consumption. Once an interrupt such as key entry, etc. occurs, the main CPU is started up and takes requested actions and then returns to the Stand-by mode. If no key is pressed for five minutes or more, the main CPU turns power off.

The current Auto Power-Off time can be reset with a BASIC Power command.

(6) When a key is pressed, 7508 detects the key stroke and translates it to a key code. This code is none of the ASCII codes but an internal code specific to PX-4.

Whenever a key is pressed, 7508 interrupts the main CPU. The main CPU then issues a command to 7508 to read its status which tells the currently pressed key.

A status code is stored in 7508 only when an interrupt occurs or after the Reset signal is deactivated, and a BFH code is normally stored. Pressing a key causes the current status code to be replaced with the key code.

(7) Once the Reset signal is removed, GAPNDL is released from the tie with the main CPU and starts the DRAM and LCD control.

RAM has a capacity of 64K bytes and each of the eight DRAM

IC elements corresponds to a bit of onebyte.

GAPNDL generates a RAM address and a timing signal in response to a memory access request from the main CPU.

In PX-4, a 2K byte RAM area is reserved for display. GAPNDL keeps reading this area to output the data to the LCD unit. This memory read effectively serves to refresh memory while power is on. The data are displayed on the LCD panel when the unit is enabled by a command sent from the main CPU to GAPNDL.

(8) Command and data exchanges between the main CPU and 7508 are accomplished as serial data data transfers between 7508 and GAPNIT. This method minimizes the required signal lines.

(9) This computer uses five interrupt signals. GAPNIT assigns a priority to each of these interrupts controls the interrupt signals to the main CPU, under wich the gate array

(10) GAPNIT contains a timer circuit and a baudrate generator which are controlled by programs.

The timer circuit is used to determine a buzzer sound scale and interval, and a cursor blink interval, etc.

The RS-232C and SIO interfaces operate based on the baudrate generator output signal.

(11) This computer uses the CP/M operating system. The operating system only affects how to use the computer (i.e., programming) and no special hardware structure is employed. Only the contents of ROM are associated with CP/M.

2.4.4 Power On to Off

(1) When the POWER switch is set ON, 7508 detects that switch setting change and interrupts the main PCU.

(2) The interrupted main CPU reads th status from 7508 and examines what interrupted it.

Knowing that it was interrupted by the POWER switch set ON, the main PCU proceeds with thecurrent processing to an appropriate point and then starts a power-off procedure.

* If the floppy disk was in the course of output operation when the interrupt occurred the main CPU writes all the data in the floppy disk buffer to the diskette.
* If the microcassette was being used, the main CPU saves data in RAM which is necessary to resume the interrupted operation when power is restored.
* When power was removed in the Continue mode, the main CPU saves data in RAM which is necessary to resume the interrupted operation when PX-4 is turned on again.

(3) Then, the main CPU sends a Power-Off command to 7508.

(4) Receiving this command, 7508 turns PX-4 off by the following sequence control:

* Issues the Reset signal to the main CPU - this signal stops and freezes the main CPU and the gate arrays, and RAM starts self-refreshing.
* Issues an OFF signal - this signal causes the gate arrays to be backed up by memory leaving the normal powered state. The signal also connects the sub-battery to the VB2 line (via Q16).

... * Stops the oscilation of the DC-DC converter and then turn power off.

P/39 2.4.5 When Power Fails

(1) When the battery voltage drops to a certain limit or below, 7508 detects it as a power failure and interrupts the main CPU.

... (2) 7508 connects the auxiliary ~~sub~~-battery to the main battery (via Q12).

(3) The interrupted main CPU reads the status from 7508 and examine what interrupted it.

Knowing that it was interrupted by a power failure, the main CPU continues the current processing to an appropriate point and then performs a power-off procedure (Continue mode). After this procedure, the main CPU displays a message "CHARGE BATTERY" for 30 seconds and then issues the Power-Off command to 7508. If the POWER switch is reset OFF while the above message is displayed, the main CPU issues the Power-Off command to 7508 at that time.

(4) On the other hand, 7508 keeps interrupting the main CPU for power failure. If no Power-Off command can be received within 50 seconds, 7508 forcibly turns PX-4 off.

2 to 3 seconds are required to handle the power failure interrupt at the most. Thus, the main CPU can normally turn power off within 33 seconds after power failed.

(5) Once a power failure is detected by 7508, PX-4 cannot be turned on unless the AC adaptor is used or the battery is replaced. When "CHARGE BATTERY" is displayed, charge the battery(s) or replace it with a new one(s) as soon as possible. If PX-4 is

left as it is, however, memory contents are not immediately lost.

P/40 2.4.6 When The Initial Reset Switch Is Pushed

(1) If the Initial Reset switch is pushed when the POWER switch is OFF, 7508 is initialized. All data including the calendar clock and time alarm values are lost because 7508 internal RAM is cleared.

(2) When the POWER switch is set ON, the main CPU reads the status from 7508 which tells to the main CPU that the Initial Reset switch has already been pushed. Thus, it initializes the system via the operating system which performs the following:

* Takes the actions listed in 2.4.2, (3), then
* Reformst the internal RAM disk,
* Reads the keyboard DIP switch setting, and
* Clears its RAM.

..... (3) The system intialization image is displayed.

The main CPU waits for an entry of the DATE/TIME and WEEK . When the data are keyed in, the main CPU stores them in 7508 RAM.

After this, the main CPU reads the time from 7508.

P/41 2.4.7 When The Reset Switch Is Pushed

(1) If the Reset switch is pushed when power is on, 7508 detects it and issues the Reset signal to the main CPU.

(2) After the Reset signal is deactivated, the main CPU reads the status from 7508 which tells to the main CPU that the Reset switch

was pushed. The main CPU performs the following system reset procedure via the operating system:

* Takes the actions listed in 2.4.2, (3), then
* Rests 7508 via a command - 7508 RAM is not cleared,
* Clears a particular main RAM area, and
* Reads the keyboard DIP switch setting.

Whenever the keyboard DIP switch setting is changed, the Reset switch must be pushed.

(3) Depending on the condition before the Reset switch is pushed, either the initial menu image or the BASIC initialization image is displayed.

3.1.3 Environemental Requirements

(1) Temperature

* Operating: 5 - 35°C
* Storage: -20 - 60°C (Up to 30°C for long term storage)
* Data storage: 0 - 40°C

(2) Humidity (relative)

* Operating: 10 - 80% (no condensation.)
* Storage: 10 - 80% (no condensation.)

The allowable vibration and shock limits are the same as for the HC-40/41 computer.

3.1.4 Principles of Operations

A. Circuit Structure

The following is a block diagram of the RAM cartridge

CHAPTER 3 OPTION DEVICES

3.1 RAM Cartridge

3.1.1 Introduction

The RAM cartridge is an external storage device which can be read and written and connected to the PX-4 computer via the HC-40 series cartridge interface incorporated in the ~~computer~~ PX-4.

The RAM cartridge contains two 64K bit static RAM IC elements (8K 8-bit words) providing a capacity of 16K bytes and can be accessed for read and write as a disk device (device name: I) from the computer.

Because it contains a data back-up lithium battery, the cartridge data can be maintained as detached from the computer.

The cartridge is also provided with a back-up battery exhaustion warning feature (an LED indicator) for extra insurance.

3.1.2 Basic Specifications

(1) RAM

* Element: 64K bit static RAM (HM6264LP)
* Capacity: 16K bytes - 64K bits x 2

(2) Back-up battery

* Element: Lithium battery - CR2032 (Sanyo)
* Capacity: 120 mAH

(3) Power requirements

* Operating: 3 mA (typ.)
* Stand~~by~~-by: 3 uA (typ.)
* Storage: Max. 1 uA (typ.)

EPSON CORPORATION	TITLE	SHEET REVISION	NO. 1
			NEXT SHEET

3.1.3 Environemental Requirements

(1) Temperature

* Operating: 5 - 35°C
* Storage: -20 - 60°C (Up to 30°C for long term storage)
* Data storage: 0 - 40°C

(2) Humidity (relative)

* Operating: 10 - 80% (no condensation.)
* Storage: 10 - 80% (no condensation.)

The allowable vibration and shock limits are the same as for the HC-40/41 computer.

3.1.4 Principles of Operations

A. Circuit Structure

The following is a block diagram of the RAM cartridge

B. System configuration

* RAM cartridge I/O address space

Table 3.1 RAM cartridge I/O address space

I/O Address	bit 7 READ bit 0	bit 7 WRITE bit 0
10 H		Lower address
11 H		Uper address
12 H	Read data	Write data
13 H	ID port (*)	

(*) The type of the attached cartridge can be known by reading this port. RAM cartridge is 20H

* Memory map

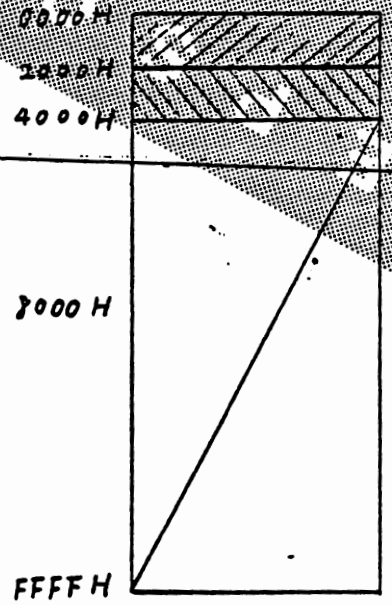

Fig. 3.2 RAM cartridge memory map

EPSON EPSON CORPORATION	TITLE	SHEET REVISION	NO. 4
		NEXT	SHEET

* RAM cartridge read/write procedure

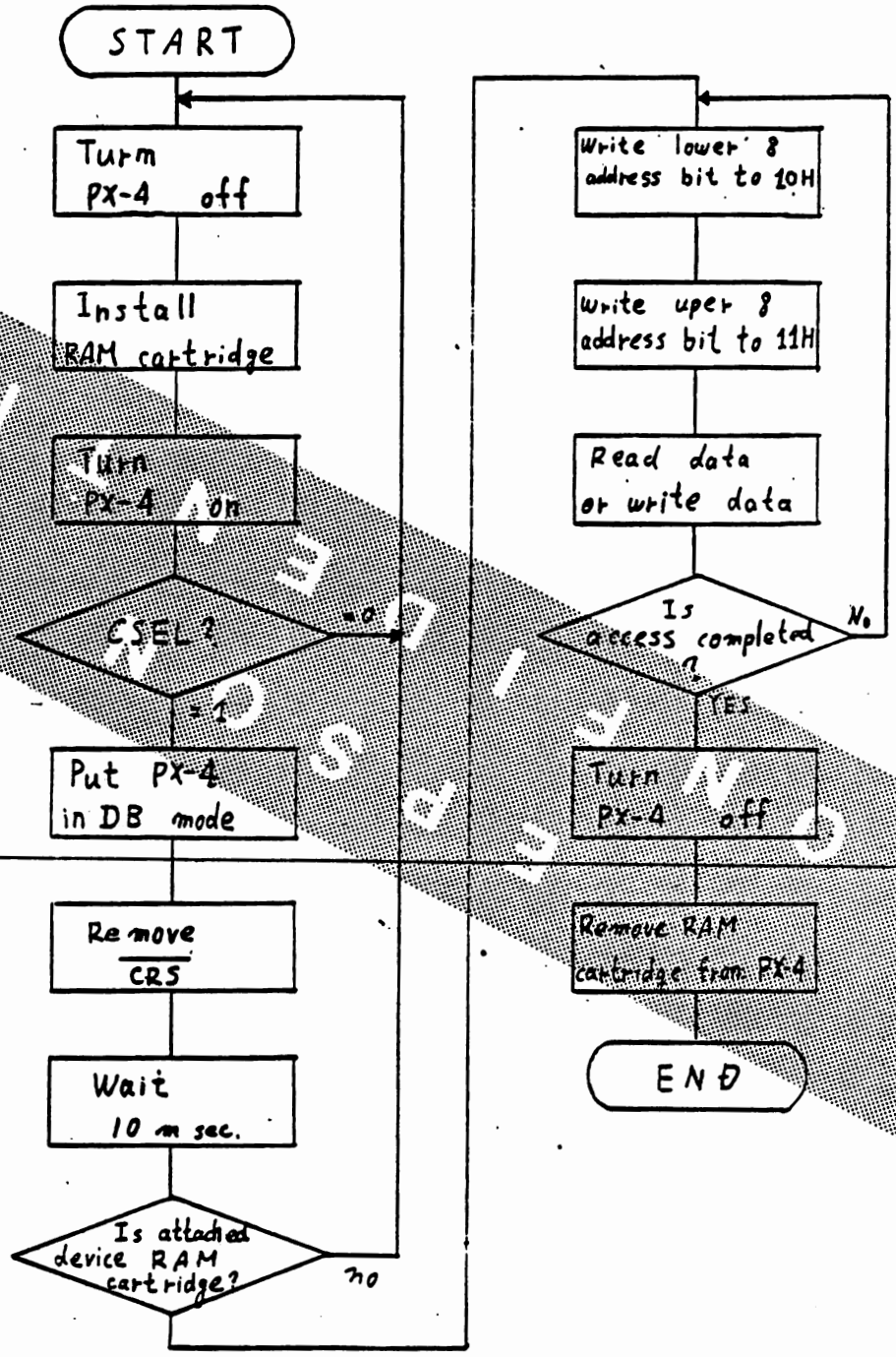

Fig. 3.3 RAM cartridge read/write procedure

EPSON EPSON CORPORATION	TITLE	SHEET REVISION	NO. 5
		NEXT	SHEET

C. Circuit Operations

(1) Reset signals

The following two reset signals are supplied to the RAM cartridge:

Signal		Function
$\overline{RS}$	Reset	Same as the reset signal supplied to the PX-4 CPU.
$\overline{CRS}$	Cartridge Reset	This reset signal is directed only to the RAM cartridge. It is generated at the I/O port by three bits which are set to three H bit in the port from the computer

Table 3.2 RAM cartridge reset signals

When either of the above reset signals is activated (goes low), the RAM address latches (1C and 1D) are cleared, resetting the RAM cartridge.

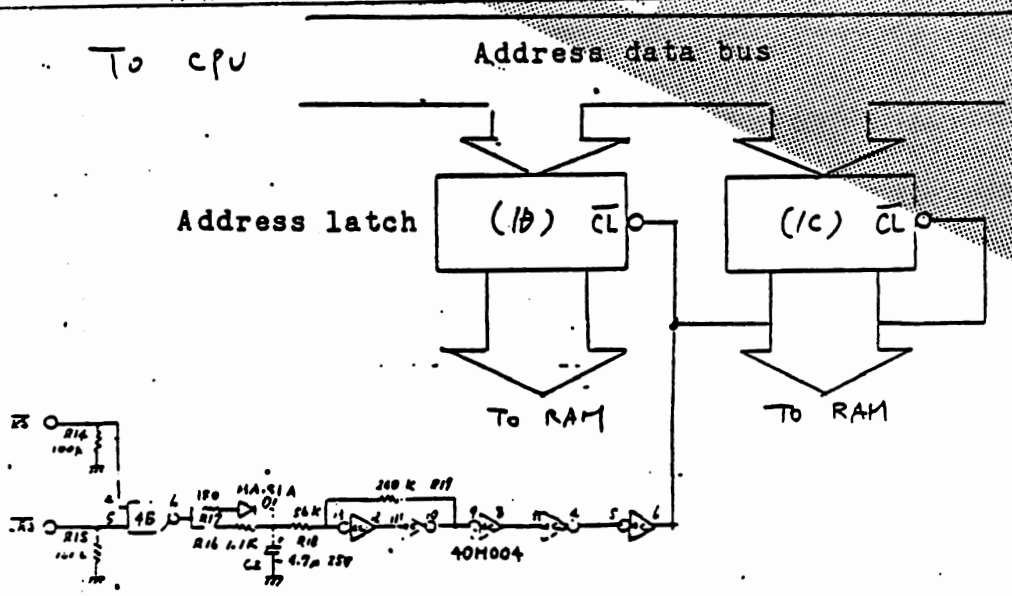

Fig. 3.4 RAM cartridge reset circuit

(2) ROM cartridge identification

The PX-4 computer reads the status from the I/O port 13H which tells what option cartridge is connected to its cartridge interface. When the RAM cartridge is connected, the status (code) is 20H.

Fig. 3.5 shows the RAM cartridge identification (ID) check circuit.

The RAM cartridge address data bus (line) CDB5 is connected with the reset signal ($\overline{CRS}$ + $\overline{RS}$) line through the resistor R3 (20K ohms). This reset signal is normally high, pulling the CDB5 line high. This gives status code 20H when ID is read which identifies the RAM cartridge.

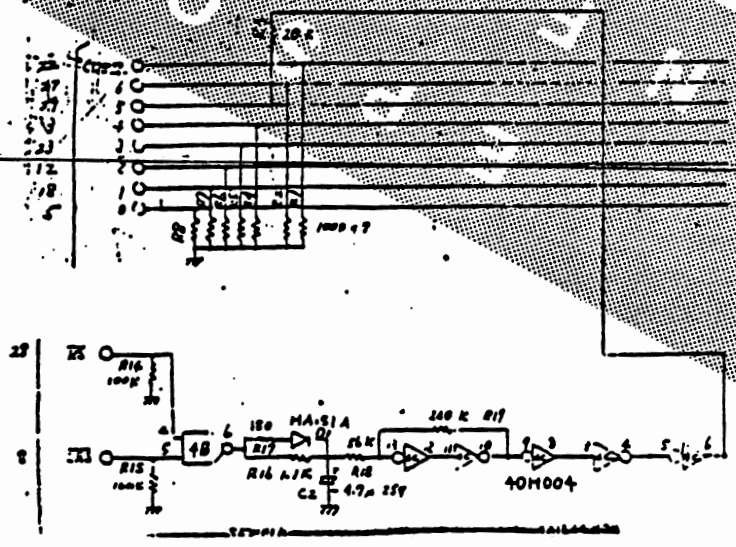

Fig. 3.5 ID generatin circuit.

EPSON CORPORATION	TITLE	SHEET REVISION	NO. 7
			NEXT SHEET

(3) RAM addressing circuit

The RAM cartridge is addressed for read/write by writing an address to the I/O ports 10H (lower address byte) and 11H (upper address byte).

Table 3.3 I/O port address 10H (Write access)

bit	Signal name	Note
7	RAA7	RAM address bit 7
6	6	6
5	5	5
4	4	4
3	3	3
2	2	2
1	1	1
0	0	0

Table 3.4 I/O port address 11H (Write access)

bit	Signal name	Note
7	RACS1	RAM chip selection (CS) access is enabled when RACS0=0 and RACS1=0
6	RACS0	
5	RAA13	RAM address bit 13
4	12	12
3	11	11
2	10	10
1	9	9
0	8	8

The RAM write signal $\overline{CWR}$ is applied to the clock terminal CK (pin 11) of the address latches (1C and 1D) by addressing the I/O ports as summarized in the following table. This low-active signal enables the upper and lower address bytes to be latched.

Table 3.5 I/O port addressing

$\overline{CWR}$	$\overline{CAB1}$	$\overline{CAB2}$	I/O address	Address latch clock	Function
0	0	0	10H	IC 1D ck ↑	Latch lower address byte
0	0	1	11H	IC 1C ck ↑	Latch uper address byte

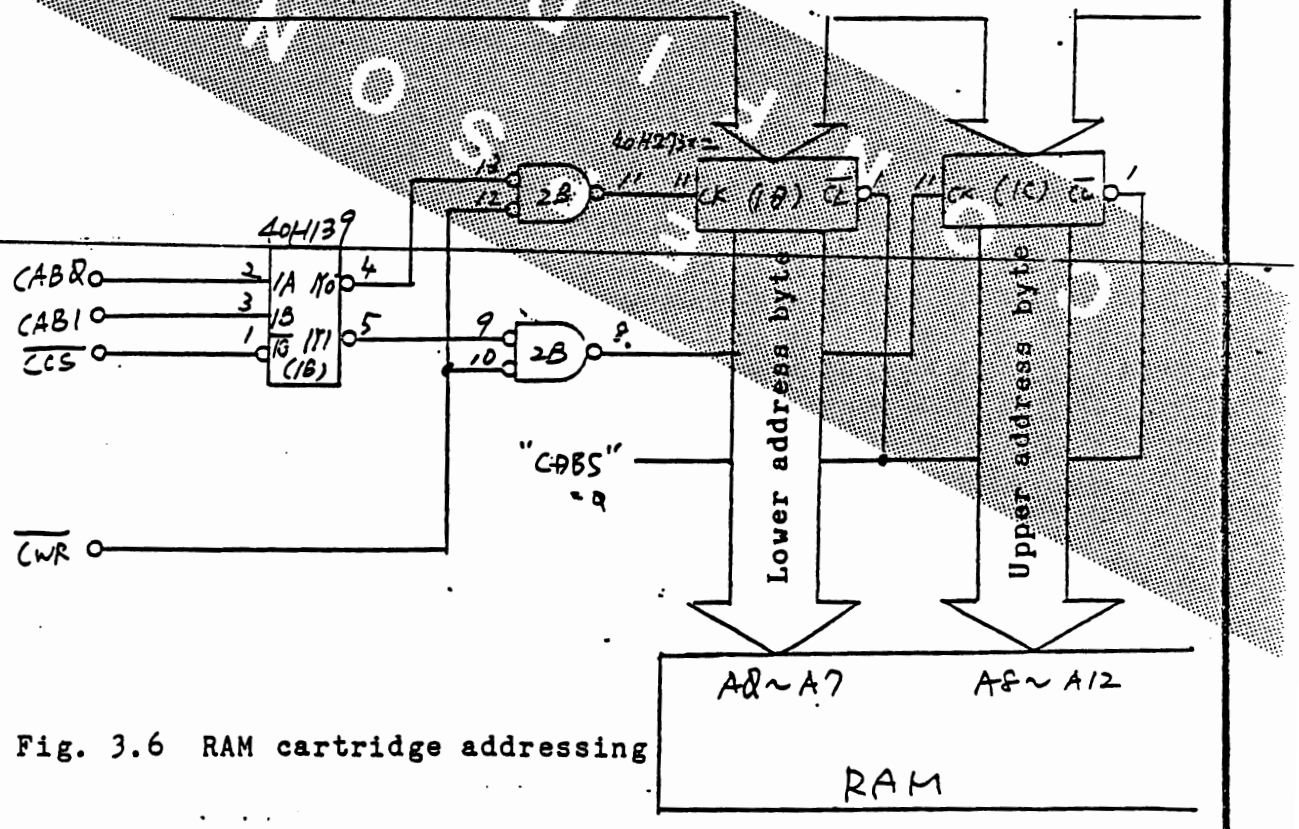

Fig. 3.6 RAM cartridge addressing

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(4) $\overline{CE1}$ signal

The low-active RAM Chip Enable (CE) signal is applied to the $\overline{CE1}$ terminal (pin 21) of the two RAM ICs as shown in the circuit diagram below. One RAM IC element is enabled at a time by the output from 6Q (A13) of the ~~lower~~ upper address latch.

Table 3.6 RAM chip selection

A13	ROM address	Selected RAM chip
0	0000H ~ 1FFFH	2D
1	2000H ~ 3FFFH	2C

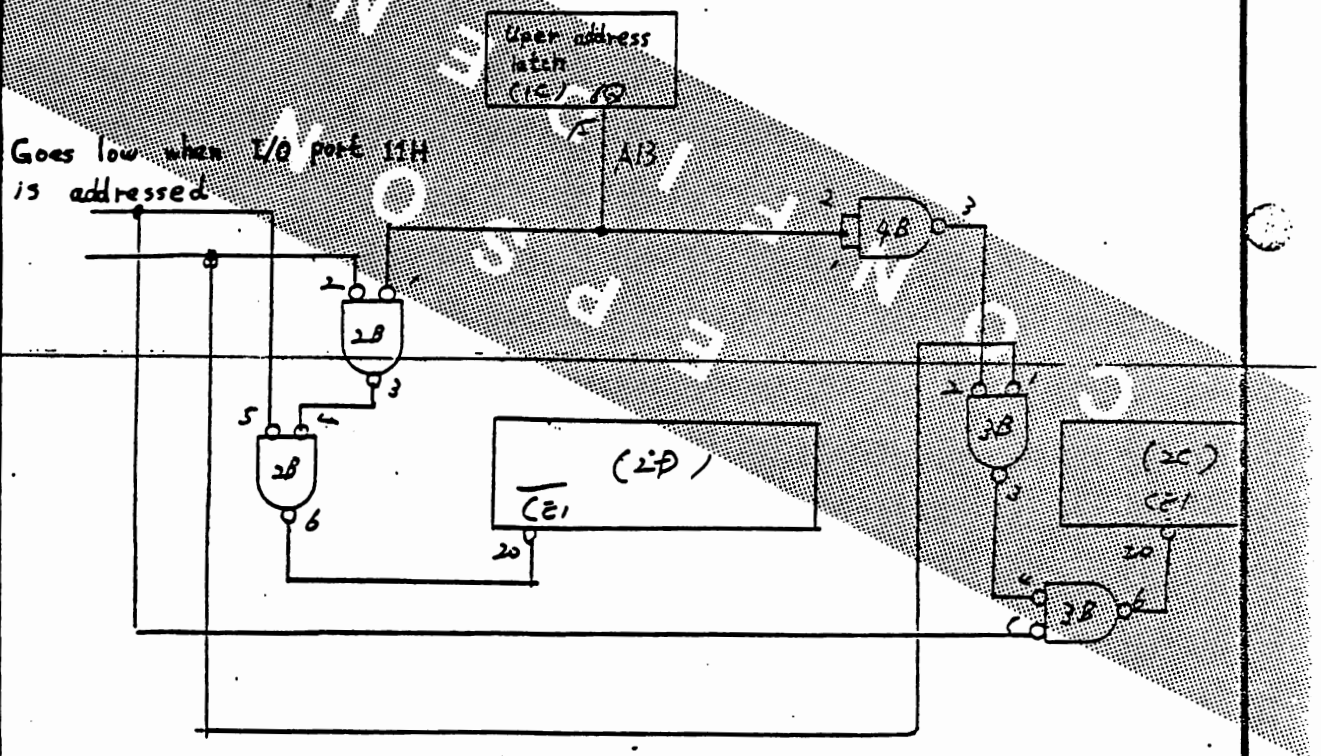

Fig. 3.7 RAM chip enable (selection) circuit

APPENDIX

EPSON EPSON CORPORATION	TITLE	SHEET REVISION	NO.	
			NEXT	SHEET

EPSON
EPSON CORPORATION
80 Hirooka, Shiowa-shi, Nagano, 399-07 Japan
Phone:02635-2-2552 Telex.3342-214 (EPSON J) Cable EPSON MATSUMOTO

CONFIDENTIAL

TITLE

PINE MTOS SPECIFICATIONS
(Microcassette Tape Operating System)

ISSUED SECT.	R.Q NO.	NO.
Technical Publishing Dept.	R353	

REVISIONS					SHEET REVISION STATUS							
REV	CHANGE DOCUMENT	BY	DATE	CHECK	SH	REV	SH	REV	SH	REV	SH	REV
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COVER SHEET 1	TOTAL SHEET 92		NEXT SHEET /		SHEET NO C-1	

Pine Microcassette Tape Operation System

(MTOS)

CONFIDENTIAL

CONTENTS

Chapter 1 SCOPE

These specifications apply to the PINE microcassette tape operating system.

Chapter 2 OUTLINE

This chapter describes the features of microcassette tape operating system (MTOS) and explains the system in outline.

2.1 Features

1) Tape based file management system

MTOS manages data on microcassette tapes as files, allowing the user to easily access data in file units. This makes it possible to use microcassette files for many applications.

2) Use

MTOS is a standalone operating system, but it can be built into another operating systems through the addition of a software interface. The functions of MTOS are generally utilized via the CP/M file management functions. However, they can also be utilized by application programs or other operating systems.

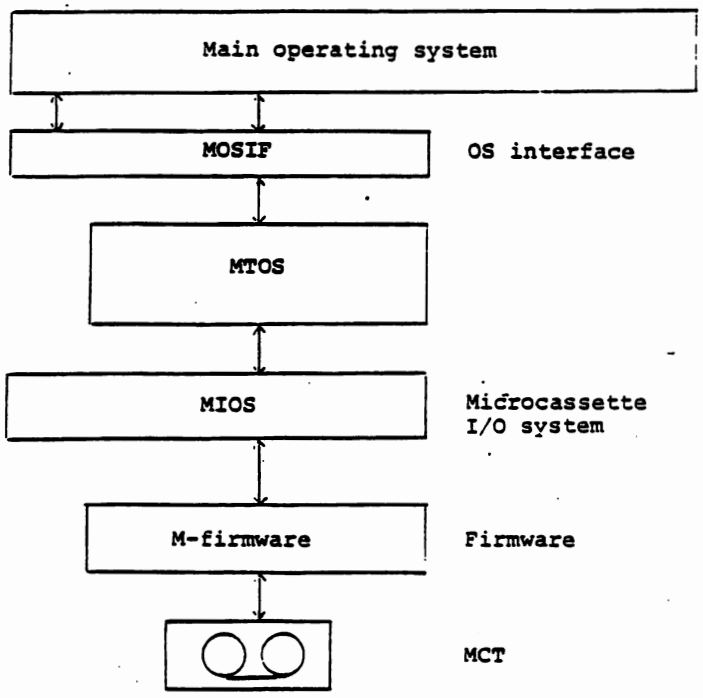
MTOS can also easily be built into machines other than PINE, provided they have the required hardware function.

These specifications are designed with consideration for building MTOS into the CP/M operating system.

2.2 Outline

1) Environment

In order to add the tape file management functions of MTOS to a computer system, it must have software modules for interfacing between (1) the main system and MTOS and (2) between the MCT firmware and MTOS. A typical system configuration is shown below.



2) Operation

MTOS first reads the directory which is at the beginning of the tape to obtain the file location, then locates the object file on the tape. Files are divided into blocks, and are accessed in block units; blocks are sequentially numbered.
Each file has a file name; however files are internally distinguished by file numbers.
File number is set to 0000H at Make Directory and incremented by 1 up to FFFEH every time the file is created, allowing it possible to differentiate from other files.

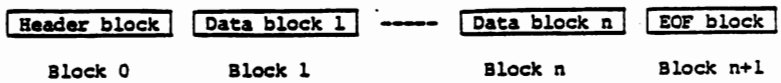
Chapter 3 FILE MANAGEMENT

This chapter describes the configuration of files on tape and procedures for accessing the directory file.

3.1 File Configuration

Under MTOS, a microcassette tape may contain up to 12 files (however, the maximum number of files can be changed at the assembler level). Each file consists of a header block, data blocks and an EOF block. The header block contains information on the file configuration. Data blocks contain data, and the EOF block indicates the end of file.

Each block has an identification field which indicates its block number.



1) Block configuration

Field	Explanation
Sync field	80 zero bits
Preamble	0FFH, 0AAH (2 bytes)
Block ID field	Consists of 4 bytes. Byte 0: Block identifier "H": Header block "D": Data block "E": End of file Bytes 1 and 2: Block number (2 bytes: 0000H to 0FFFFH) Byte 3: Block ID number When individual blocks are written repeatedly, indicates the block's repetition number.
Data field	Contains data. Length is 256 bytes.
BCC (Block Check Character) field	Contains the BCC value calculated for CRC (cyclic redundancy check). The CRC system used is CRC-CCITT, and fields which are subject to CRC range is from the beginning of the block number to the BCC field.
Postamble	0FFH, 0AAH (2 bytes)

2) Header block configuration

	Column From	to	Size	Item	Explanation
	0	3	4	ID field	HDR1 identifying the header field(ASCII)
	4	11	8	File name	File name
	12	19	8	File type	File type
	20		1	Record type	F: Fixed length record V: Variable length record n: Fixed length record which has been written n times. (ASCII)
	21		1	Block mode	Blank: Indicates the space provided following a block to allow the tape to stop before the next block is reached. S: Short gap. The length of this space is not sufficient to allow the tape to stop before the next block is reached.
	22	26	5	Block length	Indicates the length of one block in ASCII code (00000 to 65535).
*	27	28	2	Counter value	Indicates the tape count at which a write to the file is started.
*	29		1		Empty
	30		2	File attribute	File attribute
	31		1		Empty
	32	37	6	Date of file creation	2 bytes each of ASCII code for the year, month and date
	38	43	6	Time of file creation	2 bytes each of ASCII code for the hour, date and second (00~11)
	44	49	6		Empty
	50	51	2	Volume No.	Tape volume number, starting with 01
*	52	59	8	System name	Name of the system used to create the file
*	60	61	2	System file name	File number cataloged in the file directory 0001 to FFFE
*	62	67	8	Password	System password
	68	255		Empty	

* "System name" is the OS name which this MTOS is built in.

3) EOF block

Column from	to	Size	Item	Explanation
0	3	4	ID field	Contains "EOF␣".
4	11	8	File name	Contains the file name.
12	19	8	File type	Contains the file type.
20	21	2	File No.	File number from 0000 to FFFE.
22	23	2	Counter	Counter value of the last block.
24 ∿ 255				Empty

4) Data block length

The length of each block is 256 bytes.

3.2 Directory

MTOS writes the tape directory at the beginning of each tape to manage tape ID and file access.

The tape directory can be mounted from the tape into RAM by the Mount function. The directory in RAM is referred to as RAM directory.

The RAM directory is updated each time the tape is accessed. The contents of the RAM file are written to the tape by the Remove function.

1) Directory configuration

a) First block (directory ID)

Tape and directory ID

Column	Size	Item	Explanation
0 to 7	8	Tape name	Tape name
8 to 9	2	Volume No.	Tape volume number
10 to 17	8	Password	System password
18 to 23	6	Date of creation	Date of directory creation is entered in the order of month, day and year. (ASCII)
24 to 29	6	Time of creation	Time of directory creation is entered in the order of hour, minutes, and second.
30 to 35	6	Date of last remove	Date when the last remove is made. (ASCII)
36 to 41	6	Time of last remove	Time when the last remove is made. (ASCII)
42 to 43	2	Number of times mounted	Number of times the tape has been mounted.
44 to 45	2	Total No. of blocks	Total number of blocks in the tape
46 to 47	2	Total No. of records	Total number of records in the tape
48	1	Total No. of files	Total number of files in the tape
49	1	System flag 1	Tape ID flag
50	1	System flag 2	TOS controller
51 to 52	2	Last file No.	Last file number of the tape

b) Second and third blocks (directory)

These blocks contain file location and other file information. 32 bytes are used for each file, and 1 block is used for 8 files.

Location	Size	Item	Explanation
0 to 1	2	File No.	Number used for managing files on the tape
2	1	File present flag	Indicates that the file is present in the tape.
3	1	File attribute 1	File attribute 1
4	1	File attribute 2	File attribute 2
5 to 6	2	No. of blocks	Number of blocks in the file (High-Low)
7 to 8	2	No. of records	Number of records in the file (High-Low)
9 to 10	2	Starting count	Starting counter value of the file (High-Low)
11 to 12	2	Ending count	Ending counter value of the file (High-Low)
13 to 14	2	No. of times opened	Number of times the file has been opened (High-Low)
15	1	User No.	User number
16 to 23	8	File name	File name
24 to 31	8	File type	File type

2) RAM directory configuration

The file directory is loaded into RAM by the Mount function to enable file access.
The file directory in RAM is referred to as the RAM directory.
The configuration of the RAM directory is shown below.

Location	Size	Item	Explanation
0 to 1	2	File No.	Number used for managing files on the tape
2	1	File present flag	Indicates that the file is present in the tape.
3	1	File attribute 1	File attribute 1
4	1	File attribute 2	File attribute 2
5 to 6	2	No. of blocks	Number of blocks in the file (High-Low)
7 to 8	2	No. of records	Number of records in the file (High-Low)
9 to 10	2	Starting count	Starting counter value of the file (High-Low)
11 to 12	2	Ending count	Ending counter value of the file (High-Low)
13 to 14	2	No. of times opened	Number of times the file has been opened. (High-Low)
15	1	User No.	User number
16 to 23	8	File name	File name
24 to 31	8	File type	File type

3) Explanation of individual fields

a) Directory ID

(1) Tape name and volume number

These fields contain the tape name and volume number specified when the directory was created. These fields are not used by MTOS.
Tape name is specified as "EPSON␣SD" in the system display when the directory is initialized.

(2) Password

The password specified is written into this area when the directory is created. These fields are not used by MTOS.

(3) Date and time fields

These field contain the date and time of directory creation and the last Remove operation.

(4) Number of times of Mount operation

This field initially contains zero; its contents are incremented by 1 each time the directory is mounted.

(5) Number of blocks

This field contains the number of blocks (excluding directory file blocks) on the tape.

(6) Number of records

This field contains the number of records (excluding directory file records) on the tape.

(7) Number of files

This field contains the number of files on the tape.

(8) System flags 1 and 2

These flags are used by the system.

(9) Last file number

This field contains the last file number.

b) Directory block

(1) File number

This field contains the number used for file management. MTOS manages files based not on file names, but on file numbers. (This makes it easy to support the RENAME function.)

(2) File present flag

This flag indicates the validity of the corresponding file on the tape.

00H: Valid (present)
0FFH: Invalid (not present)

(3) File attribute 1

This field indicates the logical attributes of the file and contains information on file read access as follows.

Bit	Contents
7	0: Non-stop mode access 1: Stop mode access
6 5 4	Unused
3 2 1 0	Number of read retries made (0-15)

The contents of bits 7 and 3 to 0 are determined by the access attribute specified when the file is created.

(4) File attribute 2

Not used.

(5) Number of blocks

This field contains the number of blocks in the file (0000 for the header block).

(6) Number of records

This field contains the number of records in the file (0000 for the first 128 bytes of the first block). Records are not present in header and EOF.

(7) Number of times opened

This field indicates how many times the file has been opened.

(8) File starting count

This field contains the tape counter value when processing to write the file header begins at the time of file creation.

(9) File ending count

This field contains the tape counter value after the EOF block has been written at the time of file creation.

(10) User number

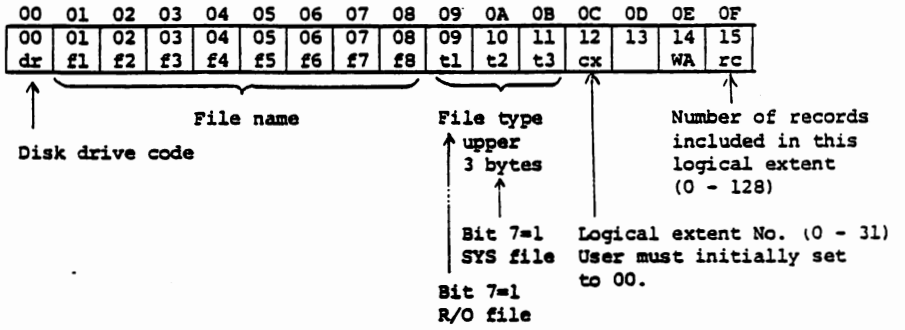
The CP/M user number specified when the file was created.

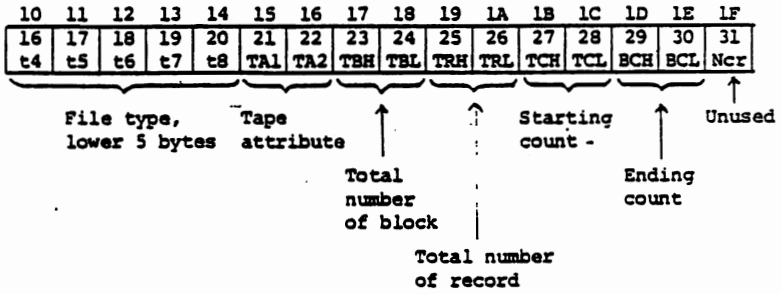
(11) File name, File type

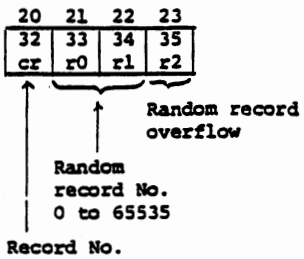
This field contains the file name and the file type after the file was created or RENAMEd.
The upper 3 bytes are used as file type.

3.3 TFCB

A packet called the TFCB (tape file control block) is used for communication with MTOS. This TFCB corresponds to the FCB of CP/M. The TFCB configuration is shown below.







3.4 File Access/Record Access

1) File access

MTOS has the basic rules for file access.

1. More than 2 files cannot be OPENed at the same time.
2. If the file was OPENed to write, other files cannot be opened until it is CLOSEd.
3. If the file was OPENed to read, other files can be also opened. However, the current file will be closed.

2) Record access

MTOS make an access to MCT in 256-byte (1 block) unit, while it makes an access in 128-byte (1 record) unit as an OS interface. It performs blocking/deblocking to compose the block or the record.
Also because of the sequential access the following must be considered.

<u>At Write</u>

1. Once one record is written and the block containing that record is not full, the record in the next block cannot be written.
2. Write cannot be performed except the record in the current block or the next block.

<u>At Read</u>

1. Record other than those in the current block or the next block cannot be accessed.

<u>Read at Write</u>

1. It is possible to read the record in the current block.

Chapter 4 MTOS FUNCTIONS

This chapter explains functions used for file management.
The functions which are supported by MTOS are listed below.

(Directory related functions)

- MMKDIR
- MTAPID

(Tape opening/closing functions)

- MMOUNT
- MRMOVE

(File access and directory search functions)

- MOPEN
- MCLOSE
- MSRDIR
- MSRNXT
- MDLFIL
- MSREAD
- MSWRTE
- MMKFIL
- MRENAM
- MGTLVA
- MSTFAT
- MRREAD
- MRWRTE
- MCPLEN
- MVERFY

4.1 Explanation of Functions

This section describes the name, parameters, and purpose of each function.

As for the return code, see 6.3 Return Codes.

1) MMKDIR (Creating directory file)

a) Entry parameters

Register DE = TFCB address

Contents of TFCB

Column	Size	Contents
0 to 7	8	Tape name (ASCII)
8 to 9	2	Volume No. (ASCII)

b) Purpose

This function rewind the tape and creates the directory file at the beginning of the tape. The contents of the first 10 bytes of the directory file are the same as those of TFCB.
The number of files of the directory is set to zero.
The RAM directory is also created at the same time.
Therefore, it is not necessary to mount the directory after this function has been completed unless a different tape is used.
If the system password is specified, it is specified in the directory.

2) MTAPID (Reading tape ID)

a) Entry parameters

None

b) Return code

Register A≠00H - Directory file has been mounted.
=00H - Directory file has not been mounted.

The contents of columns 0 to 53 of the first block of the directory file are loaded into the DMA buffer and control is returned to the caller only when register A contains other than 00H.

c) Purpose

This function returns the currently mounted tape ID information to the DMA buffer. No information is returned if no directory file is mounted.

3) MMOUNT (Opening tape)

a) Entry parameters

None

b) Purpose

This function reads the directory file from the tape and load it into the RAM directory. This function cannot be used if the directory has not been removed. (Set by flag).

All other MTOS functions can be used after this function has been completed.

This function also turns on the microcassette LED.

4) MRMOVE (Closing tape)

a) Entry parameters

None

b) Purpose

This function writes the contents of the RAM directory to the tape directory file. After this function has been completed, directory functions other than MAKEDIR and MOUNT cannot be used.

If the RAM directory has not been updated, it is not actually written to the tape directory file.
(The RAM directory file contents are changed when a file is written, deleted or renamed.)

This function also turns off the microcassette LED.

5) MOPEN (Opening file)

a) Entry parameters

Register DE = TFCB address
TFCB = Name of file to be opened and file type

b) Purpose

This function searches the RAM directory for the file specified in the TFCB and, if it is found, reads its header block and sets relevant information in the TFCB. (Columns t1, t2 and t3 are significant for the file type.)

If the header block cannot be found, an open error results. An open error also results if the file is already open in the write mode. However, a file can be opened again even if it is already open in the read mode. Whether the non-stop or stop mode of access is used for reads is determined by the file attribute.

Either write attribute or the specified attribute is set as a file attribute.

6) MCLOSE (Closing file)

a) Entry parameters

Register DE = TFCB address

b) Purpose

This function closes a file which is open; it need not be used with files which are opened for reads. After a file is written, this function writes the EOF block, updates the RAM directory and, if the verify flag is on, automatically verifies the write. If any error is detected during verification, a verify error results and the file is not cataloged in the directory.

7) MSRDIR (Searching the directory for the first file)

a) Entry parameters

Register DE = TFCB starting address, file name and file type (3 bytes)

b) Return code

Register A = Directory code (00H) or 0FFH
Register H = 00H
DMA buffer = If the file is detected, file directory information is entered in the first 32 bytes, and the remaining bytes are padded with 0E5H.

c) Purpose

This function searches the RAM directory for the file specified in the TFCB and loads its directory information into the DMA buffer, and returns.

The file match symbol (3FH) may be used.

The directory pointer is updated for the next search.

If the specified file is not found, 0FFH is returned to register A.

8) MSRNXT (Searching the directory for the next file)

a) Entry parameters

None

b) Return code

Register A = Directory code (00H) or 0FFH
Register H = 03H
DMA buffer = Directory information on the file specified in the TFCB

c) Purpose

This function searches the portion of the directory file following the directory pointer for the file specified in the TFCB, then loads the corresponding directory information into the beginning of the DMA.

This function is the same as MSRDIR except that it starts searching at the position indicated by the directory pointer.

9) MDLFIL (Deleting files)

a) Entry parameters

Register DE = TFCB address

b) Purpose

This function deletes the specified file from the RAM directory.

Directory code 00H is returned to register A when the specified file is deleted. If the specified file cannot be found, 0FFH is returned to register A.

10) MSREAD

a) Entry parameters

Register DE = TFCB top address

b) Purpose

This function sequentially reads the file specified in the TFCB. If the record specified in the cr and ex columns cannot be found in the current block or the next block, an error results.

See 3.4 File access/Record access for the reading records.

11) MSWRTE (Writing sequential files)

a) Entry parameters

Register DE = TFCB address

b) Purpose

This function writes the records specified by the TFCB. Since the DMA buffer size is 128 bytes and the block size is 256 bytes, blocking is performed automatically.
A block is actually written to the tape when the block is created and the record of the next block is tried to be written, or at CLOSE.
Therefore, blocked records to be written can be read before the write is actually made.

An error results if the file is not open.

12) MMKFIL

a) Entry parameters

Register DE = TFCB address

b) Purpose

This function writes the file header specified by the TFCB into a free area on the tape and opens that file. If the directory already includes the specified file name or is full, the file cannot be created. If any other file has been opened in the write mode, this function results in an open error.

Whether the stop or non-stop mode of access is used for the write is determined by the TOS attribute area.

13) MRENAM

a) Entry parameters

Register DE = TFCB address

b) Purpose

This function changes the file name specified by columns f1 through t3 of the TFCB to that specified by columns t4 through SRNH. The upper 3 bytes of file type are significant.

14) MGTLVA (Returning logged-in vector address)

a) Entry parameters

None

b) Return information

Register HL = Allocation vector address

c) Purpose

This function returns the MTOS allocation vector address.

The bit(s) corresponding to the quotient of (total number of record) ÷ 1024 in MTOS allocation vector are padded with 1 from left.

1 byte	8 KB
8 bytes	64 KB

15) MSTFAT (Setting file attribute)

a) Entry parameters

Register DE = FCB address

b) Return information

Register A = Directory code (00H, 01H, 02H, or 03H)
= 0FFH: File not found.

c) Purpose

This function sets the attributes of the file specified by the TFCB. The attributes are set by the MSBs of columns t1 and t2. These settings are written both to the directory and file attribute of MTOS.

File attributes

t1 bit 7=0: R/W file
=1: R/O file
t2 bit 7=0: SYS file
=1: DIR file

16) MRREAD (Random read)

a) Entry parameters

Register DE = TFCB address

b) Purpose

This function reads the record specified by PRNH and PRNL of the file FCB. The contents of columns r0 and r1 are converted into an internal record number and a sequential read is performed.

17) MRWRTE

a) Entry parameters

Register DE = TFCB address

b) Purpose

This function writes data to the record specified by columns r0 and r1 of the file FCB.
Operation is the same as for a sequential write.

18) MCPLEN (Calculating file size)

a) Entry parameters

Register DE = FCB address

b) Purpose

This function sets the record size of the file specified by the FCB into r0, r1 and r2, and returns.

19) MVERFY

a) Entry parameters

Register DE = TFCB address

b) Purpose

This function is used to verify the contents of the file specified by the FCB.

4.2 Auto-mount Function

When an attempt is made to access a tape before it has been mounted, mounting is performed automatically, followed by the access operation. This function is referred to as the auto-mount function, and supporting functions are as follows.

MTAPID
MOPEN
MSRDIR
MDLFIL
MSREAD
MSWRTE
MMKFIL
MRENAM
MVERFY

Chapter 5 MICROCASSETTE INPUT/OUTPUT SYSTEM (MIOS)

The interface between the MCT firmware and MTOS is provided by the microcassette input/output system (MIOS). MIOS provides 18 functions which are required by MTOS, as well as two functions which are used for maintaining compatibility with CP/M. This functions are as listed below.

MIOS Functions

0	MIRDST	-- (read tape status)
1	MIRDCT	-- (read tape count)
2	MISTCT	-- (set tape count)
3	MISTOP	-- (stop motor)
4	MIPLAY	-- (rotate motor in play mode)
5	MIREC	-- (rotate motor in record mode)
6	MIFF	---- (rotate motor for fast feed)
7	MISREW	-- (rotate motor for slow rewind)
8	MIREW	--- (rotate motor for rewind)
9	MIFFTE	-- (fast feed to end of tape)
10	MIRWTT	-- (rewind to beginning of tape)
11	MIHDON	-- (load head)
12	MIHDOF	-- (unload head)
13	MISKTP	-- (tape seek)
14	MISTMP	-- (set tape move protect count)
15	MIRSMP	-- (reset tape move protect count)
16	MIRDBL	-- (read one block)
17	MIWTBL	-- (write one block)
18	MIGTWP	-- (read write protect pin)
19	MILEDON	-- (turn on LED)
20	MILEDOF	-- (turn off LED)
21	MISDAT	-- (save data)
22	MILDAT	-- (load data)
23	MIERS	-- (erase the specified area)

5.1 Explanations of Functions

This section explains the functions of the microcassette input/output system.
Input is the parameter passed to the routine, and output is the return code or the value received from the routine.

1) MIRDST

Entry parameters: None.

Return information: Register H - Microcassette status

Purpose: Reads the status of the microcassette drive. The configuration of the microcassette status code is as follows.

Bit 7	Head position	(0: Unloaded	1: Loaded)
Bit 6	Motor	(0: Stopped	1: Moving)
Bit 5	Winding	(0: Non-winding	1: Winding)
Bit 4	Fast feed	(0: Non-fast feed	1: Fast feed)
Bit 3	Play	(0: Not playing	1: Playing)
Bit 2	Record	(0: Not recording	1: Recording)

2) MIRDCT

Entry parameters: None.

Return information: Register HL = Counter value

Purpose: Reads the value of the microcassette counter. The microcassette counter is composed of 16 bits; the value in this counter is increased as the tape is moved in the forward direction, and vice versa.

3) MISTCT

Entry parameters: Register DE = Counter value

Return information: None

Purpose: Sets the value of the tape counter.

4) MISTOP

Entry parameters: None.

Return information: None.

Purpose: Stops the motor of the microcassette drive.

5) MIPLAY

Entry parameters: None.

Return information: None.

Purpose: Turns the microcassette drive motor in the play mode. (The read signal is produced if the head is loaded.)

6) MIREC

Entry parameters: None.

Return information: None.

Purpose: Turns the microcassette drive motor in the record mode. (The tape is erased if the head is loaded.)

(Intentionally blank)

7) MIFF

Entry parameters: None.

Return information: None.

Purpose: Turns the microcassette drive motor in the fast feed mode.

8) MISREW

Entry parameters: None.

Return information: None.

Purpose: Turns the microcassette drive motor in the slow rewind mode. (The tape is automatically unloaded.)

9)

(Intentionally blank)

10) MIFFTE

Entry parameters: None.

Return information: Register A = 00H or 0FFH

Purpose: Turns the microcassette drive motor in the fast feed direction until the end of the tape is reached. When A=0FFH, the brake flag has gone up to indicate that the motor has stopped turning.

11) MIRWTT

Entry parameters: None.

Return information: See 6.3 Return Codes.

Purpose: Turns the microcassette drive motor in the rewind direction until the beginning of the tape is reached. When A=0FFH, the brake flag has gone up to indicate that the motor has stopped turning.

12) MIHDON

Entry parameters: None.

Return information: See 6.3 Return Codes.

Purpose: Loads the head of the microcassette drive (lowers it to the tape).

13) MIHDOF

Entry parameters: None.

Return information: See 6.3 Return Codes.

Purpose: Unloads the head (moves it away from the tape).

14) MISKTP

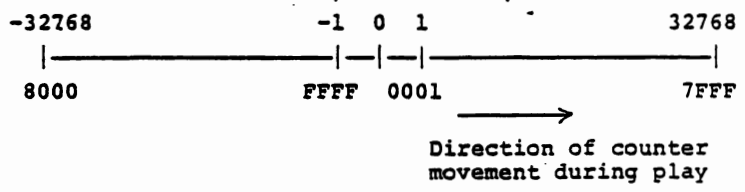
Entry parameters: Register DE = Object count value

Return information: See 6.3 Return Codes.

Purpose: Unloads the head and winds the tape until the value of the counter reaches the value set in register DE. When register A=0FFH, the tape has been braked to a stop.

Note: When the current tape count is C0 and the object count is CT such that C0 is less than CT, and tape is wound in the forward direction until CT is reached.
When CT is less than C0, the tape is wound in the reverse direction until CT is reached.
If C0 and CT are equal, the tape is not wound.

The figure below shows relates the actual tape image to the counter values.



15) MISTMP

Entry parameters: Register DE = No. of counts (B for high, C for low)

Return information: None.

Purpose: Sets the tape movement protect count. The tape movement protect count is the number of counts the tape can be moved (wound) in either direction. If an attempt is made to move the tape beyond this distance, the tape is stopped automatically. For example, when the current count is 500 and the tape movement protect count is 300, rewinding the tape to 400 reduces the tape movement protect count to 200. Afterwards, the tape will stop at 600 (when the tape movement protect count reaches 0) if an attempt is made to advance it to 700.

16) NIRSMP

Entry parameters: None.

Return information: None.

Purpose: Resets the tape movement protect count.

17) MIRDBL

Entry parameters: Register C = Read mode
DE = No. of bytes to be read
HL = Block number
TOSDMA = Starting address of the buffer in which the data read is to be stored (block number pointer)

Return information: See 6.3 Return Codes.

Purpose: Reads the number of bytes of data specified in register DE into the buffer whose starting address is specified in TOSDMA. Data is read in the mode specified in register C. This function makes it possible to retry a read if the first two bytes specified by the start of the buffer are not the same as the block number specified in register HL; however, it returns without doing anything if the number of retries is 0.

Read mode

Bit 7	
Bit 6	0 = Non-stop mode, 1 = Stop mode
Bit 5	
Bit 4	
Bit 3	No. of retries (0 to 15)
Bit 2	
Bit 1	
Bit 0	

18) MIWTBL

Entry parameters: Register DE = No. of bytes to be written
Register C = Write mode
TOSDMA = Starting address of the buffer containing the data to be written

Return information: See 6.3 Return Codes.

Purpose: Writes the number of bytes of data specified in register DE to the tape from the buffer whose starting address is specified in TOSDMA. The write mode which becomes applicable to this data is determined by the setting of bit 7 of the C register.

Write mode

Bit 7 0 = Non-stop mode, 1 = Stop mode
Bit 6
Bit 5
Bit 4
Bit 3
Bit 2
Bit 1
Bit 0

19) MIGTWP

Entry parameters: None.

Return information: Register A = 00 Non protect
A = 03 Protect

Purpose: Reads the status of write protect pin of MCT tape.

20) MILEDON

Entry parameters: None.

Return information: None.

Purpose: Turns on the microcassette drive LED.

21) MILEDOF

Entry parameters: None.

Return information: None.

Purpose: Turns off the microcassette drive LED.

23) MISDAT

Entry parameters: None.

Return information: None.

Purpose: Saves the contents of the system data area to the microcassette tape data area. This function is used during power-up processing.

24) MILDAT

Entry parameters: None.

Return information: None.

Purpose: Loads microcassette data into the system data area. This function is used during power-off processing.

24) MIERS

Entry parameters: Register DE = Tape count

Return information: See 6.3 Return Codes.

Purpose: Erase the length of tape corresponding to the tape count specified in register pair DE.

Chapter 6 MOSIF

MTOS (the microcassette tape operating system) and MIOS (the microcassette input/output system) are interfaced with CP/M via the microcassette operating system interface (MOSIF).

6.1 MTOS Calls

The procedures for making MTOS calls are compatible with those for making BDOS calls. Whether operation is performed by MTOS or BDOS when a call is made is determined according to the following rules.

Rule 1
Functions which are not supported by MTOS are performed by BDOS.

Rule 2
When the FCB is used as a function parameter, the function is performed by MTOS or BDOS according to the disk drive code contained in the FCB.

Rule 3
Other MTOS functions are performed only when the currently logged in drive is the MCT.

A list of the MTOS system calls is shown in the table 2.

6.2 MIOS Calls

The 18 basic MIOS functions are used as a single, multiple-function BIOS call. These functions are called by setting the function number in register B and calling MIOS entry MCTX. The numbers set in register B for each function are as follows.

Register B	Function
0	MIRDST
1	MIRDCT
2	MISTCT
3	MISTOP
4	MIPLAY
5	MIREC
6	MIFF
7	MISREW
8	MIREW
9	MIFFTE
10	MIRWTT
11	MIHDON
12	MIHDOF
13	MISKTP
14	MISTMP
15	MIRSMP
16	MIRDBL
17	MIWTBL
18	None
19	None
20	MIGTWP
21	MILEDON
22	MILEDOF
23	MISDAT
24	MILDAT

6.3 Return Codes

Each function of MTOS or MIOS has some return codes. The return codes of MTOS are set in the A and H registers, and TOSRCD. Those of MIOS are set in the A and C registers, IOSRCD, and BIOSERROR.

MTOS reports 4 errors of CP/M and corresponding error codes are set in the A and H registers.

1) Return codes of MTOS

Return codes of MTOS are set in TOSRCD.
The value to be set in A and H registers is decided by the error code in TOSRCD at the end of MTOS.

a) BDOS level error reports

While CP/M reports 4 errors, MTOS reports the errors as follows:

① When error return is made from MIOS,
BAD SECTOR

② Error during MOUT
BAD SELECT

③ Irregular access of R/O drive
R/O

④ Irregular access of R/O file
R/O FILE

If the each error report is suppressed, error code for each error is set in A and H registers and a return is made.

	A	H
Bad Sector	FF	1
R/O	FF	2
R/O File	FF	3
Bad Select	FF	4

b) Return code in TOSRCD

There are 18 return codes in TOSRCD.
Return codes in TOSRCD, A and H registers, and its explanations are shown in Table 1.
If the value of H register is 5, the error is unique to MTOS, while 0, it may correspond to the CP/M error.
Table 2 shows the error codes which may be reported in MTOS functions.

2) Return codes of MIOS

Return codes of MIOS are set in A and C registers. Also these values are set in BIOSERROR and IOSRCD and a return is made. BIOSERROR is the error code as BIOS, while IOSRCD includes the error information of firmware.
Table 3 shows the error code and its result.
Table 4 shows the each MIOS function and possible error results.

Table 1 MTOS return codes

TOSRCD return value	A	H	Description
0	0	0	Normal completion
1	FF	5	Not removed.
2	FF	5	Not mounted.
3	FF	5	Cannot remove.
4	FF	5	Cannot mount.
5	FF	0	Directory is full.
6	FF	0	R/O file
7	FF	5	File already exists.
8	FF	0	File not found.
9	FF	5	File already open.
A	1	0	File not open.
B	FF	5	Record No. error
C	1	0	Reaches EOF.
D	4	0	Random access error
F	FF	0	R/O drive
10	FF	0	Verify error
11	FF	5	File No. error
12	FF	5	Auto remove check error

Table 2 MTOS System Calls and return codes (I)

Function No.	Function	Parameter \ Return code	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	10	11	12
12	Get version No.																			
13	Reset disk system																			
14	Select disk drive		○			○														
15	Open file	DE ← FCB address				○				○	○					○			○	
16	Close file	DE ← FCB address		○						○	◉					◉		◉	◉	
17	Search for first file	DE ← FCB address				○														
18	Search for next file																			
19	Delete file	DE ← FCB address				○		○									○			
20	Sequential read	DE ← FCB address				○					○	○		○						
21	Sequential write	DE ← FCB address				○		○			○	○	○				○			
22	Create file	DE ← FCB address				○	○		○		○						○			
23	Change file name	DE ← FCB address				○		○		○							○			
24	Get log-in vector																			
25	Get log-in disk number																			
26	Set DMA address																			
27	Get allocation address					○														
28	Set write protect flag																			
29	Get R/O vector																			
30	Set file attribute					○				○										
31	Get disk parameter address																			
32	Set/get user code																			
33	Random read	DE ← FCB address				○					○	○		○	○					
34	Random write	DE ← FCB address				○		○			○	○	○				○			
35	Calculate file size	DE ← FCB address																		
36	Set random record	DE ← FCB address																		

(Continued)

Function No.	Function	Return code / Parameter	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	10	11	12
37	Reset disk drive	DE ← Drive vector																		
38	Not used																			
39	Not used																			
40	Random write with zero fill																			

Table 2 MTOS System Calls (II)

Function No.	Function	Return code / Parameter	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	10	11	12
251	Verify	DE ← TFCB address				○				○	○					○		○	○	
252	Remove			○	○															○
253	Mount		○			○														
254	Read tape ID																			
255	Make tape directory	DE ← FCB address																		

Notes: 1. "○" indicates it is not supported by MTOS.
2. See the explanation of each function.
3. * indicates that verify is specified after CLOSE.

Table 3 BIOSERROR and IOSRCD

BIOSERROR code	Meaning
0	Normal completion
1	Read error
2	Write error
3	Write protect error
4	Time over error
5	Seek error
6	Break error (Break key pressed)
7	Power off error (Power turned off)
FE	Others

TOSRCD code	Meaning
1	Head error (Abnormality on the head)
2	Motor stop error (Motor stop)
3	Write protect error
4	Data error (Bit 0, 1 undiscriminable)
5	CRC error
6	Block mode error (Block mode different)
7	Tape error (Tape not mounted)

Table 4 MIOS functions and return codes

MIOS function No.	Function \ Category / Code	BIOSERROR 1	2	3	4	5	6	7	FE	IOSRCD 1	2	3	4	5	6	7	Remarks
0	Read MCT status																
1	Read counter																
2	Counter set								O								Parameter error
3	Motor stop																
4	Motor play																
5	Motor record																
6	Motor fast feed																
7	Motor slow rewind								O	O							Automatically head unloaded
8	Motor rewind								O	O							
9	Fast feed to end of tape				O	O	O	O		O						O	
10	Rewind to top of tape				O	O	O	O		O						O	
11	Head ON								O	O							
12	Head OFF								O	O							
13	Seek tape					O	O	O		O		O				O	
14	Set move protect area																
15	Reset move protect area																
16	Read 1 block	O					O			O	O		O	O	O		
17	Write 1 block		O	O			O			O	O	O					
18	None																
19	None																
20	Get write protect pin status																
21	LED ON																
22	LED OFF																
23	Save data																
24	Load data																
25	Erase specified area						O	O									

Chapter 7 OTHER NOTES

This chapter describes the relationship between MTOS and MIOS and the Pine operating environment. Items discussed are as follows.

1) Limitations on the buffer used by MIOS
2) Foced termination and power-off of MTOS and MIOS
3) Auto remove checks
4) STOP mode and NONSTOP mode
5) Auto mount checks

7.1 Limitations on the Buffer used by MIOS

The buffer address specified in TOSDMA for use by MIOS must be located in the from 8000H to FFFFH. If not specified, a certain address in the system becomes effective by default.

7.2 Forced Termination and Power-Off of MTOS and MIOS

There are two events which can result in interruption of MCT operation; these are (1) Forced termination (CNT-STOP) and (2) Power-off. MIOS and MTOS processing for both of these is as indicated below.

(1) Forced termination

< MIOS >

When processing currently being performed is a seek, write, or read, that processing is discontinued, the motor is stopped. the head is unloaded, and the return code 0FFH is placed in register A.

< MTOS >

When processing currently being performed is a read or write, a Bad Sector is posted to CP/M, processing is discontinued, and the file is closed. If termination occurs during a write, the file is not cataloged in the directory.

(2) Power-off

< MIOS >

When processing currently being performed is a read or write, the motor is stopped, the head is unloaded, and the return information is set after access to the current block has been completed. In the seeking the motor is immediately stopped.

< MTOS >

The power goes off after control is returned from MIOS. Read access will be continued the next time the power goes on (if power-off is in the continue mode). With other than the continue mode, the file is closed upon power-off because a cold start is made when the power goes back on. If a write is being performed when the power goes off, the file is not cataloged in the directory.

7.3

(Intentionally blank)

7.4 Auto Remove Check

MTOS performs auto remove check by reading the directory ID. If the directory information of created date and time in the tape is same as that in the RAM, remove is performed automatically.
This check is performed by setting a flag.

7.5 STOP Mode and NON-STOP Mode

This section explains use of the STOP and NON-STOP modes of tape access and the types of control which are used with the two modes.

1) Procedures for use

1-1) STOP mode

1-1-1) Writes

In the STOP mode, the motor is stopped after each block is written, then is started again to write the next block. Writes in this mode take longer because the motor is started and stopped for each block. However, since the motor is stopped after writing each block, it doesn't matter how much time passes before each block is written.

1-1-2) Reads

In the STOP mode, the motor is stopped after each block is read, then is started again to read the next block. Since each block is written twice, the motor must be started and stopped two times in order to read one block. Since the motor is stopped after reading each block, it doesn't matter how much time passes before read operation starts for each block.

1-2) NON-STOP mode

1-2-1) Writes

In the NON-STOP mode, the motor is not stopped at the end of each block write; since this eliminates the time which is required to start and stop the motor, it is faster to use the NON-STOP mode to write to tape. However, unless blocks are written in uninterrupted succession, tape will be wasted because there will be longer gaps between blocks. This has the potential disadvantage of making read operation more time consuming.

1-2-2) Read

In the NON-STOP mode, the motor is not stopped after reading each block. This eliminates the time which is required in the STOP mode for starting and stopping the motor. However, read errors will occur in this mode unless the read operation for each block begins before the beginning of the block is reached on tape.

1-3) Comparison of the STOP and NON-STOP modes

This section compares the amount time required for write and read access in the STOP and NON-STOP modes.
This comparison assumes the following conditions.

1) That no errors occur
2) That access is continuous (that no other processing is performed between access to each block)

The number of blocks per file is given as BN.

Symbols:

T_{WS}: Time required to write BN blocks in the STOP mode

T_{RS}: Time required to read BN blocks in the STOP mode

T_{WN}: Time required to write BN blocks in the NON-STOP mode

T_{RN}: Time required to read BN blocks in the NON-STOP mode

T_{BA}: Access time per block

T_{STOP}: Amount of time motor is stopped

T_{START}: Motor speed stabilization time

T_{CNS}: Amount of time which is required regardless of mode (to find and access the header and to write the EOF code to tape)

$T_{WS} = BN * (2 * T_{BA} + T_{STOP} + T_{START}) * T_{CNS}$

$T_{RS} = (2 * BN - 1) * (T_{BA} + T_{STOP} + T_{START}) T_{CNS}$

$T_{WN} = 2 * BN * T_{BA} + T_{CNS}$

$T_{RN} = (2 * BN - 1) * T_{BA} + T_{CNS}$

$T_{WS} - T_{WN} = BN * (T_{STOP} + T_{START})$

$T_{RS} - T_{RN} = (2 * BN - 1) * (T_{STOP} + T_{START})$

Tested values obtained are as follows.

$T_{BA} = (2 + 4 + 256 + 2 + 2) * (4 \times 500 + 5 \times 1000) + \alpha$

$= 266 \times 7000 + \alpha$

$= 1862000 + \alpha$ (μsec)

$= 1.862 + \alpha$ (sec)

$\alpha = (500 + 270 + 270) / 2$

$= 520$ (msec)

Therefore, $T_{BA} = 1.862 + 0.52 = 2.382$ (sec)

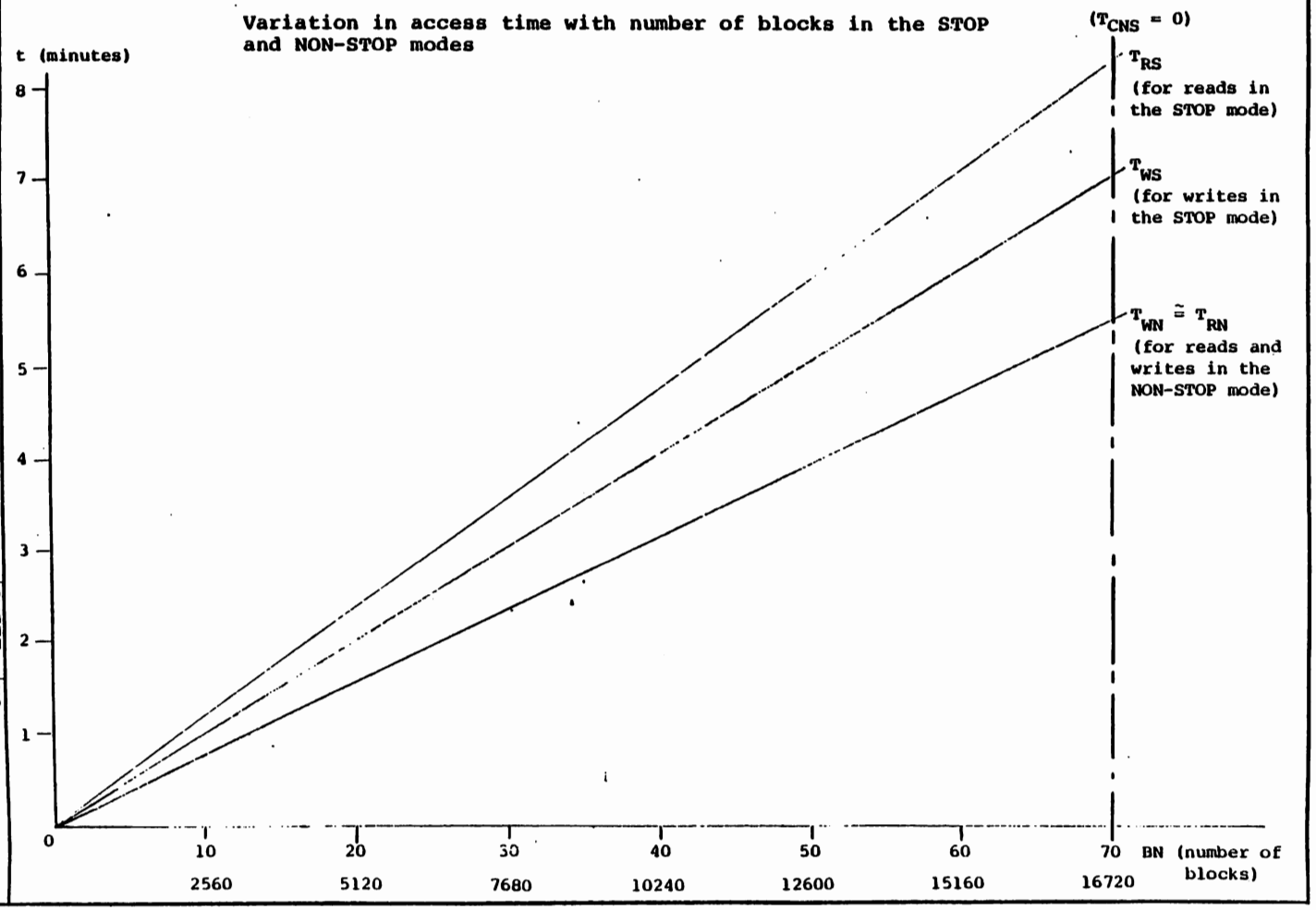
$T_{STOP} = 1$ sec

$T_{START} = 0.2$ sec

Following from the above (in second units):

$T_{WS} = 5.964 \times BN + T_{CNS}$ $\quad T_{RS} = 7.162 \times BN - 3.582 - T_{CNS}$

$T_{WN} = 4.764 \times BN + T_{CNS}$ $\quad T_{RS} = 4.764 \times BN - 2.382 - T_{CNS}$


Variation in access time with number of blocks in the STOP and NON-STOP modes
t (minutes)
8
7
6
5
4
3
2
1
0
10
2560
20
5120
30
7680
40
10240
50
12600
60
15160
70
16720
BN (number of blocks)
(T_{CNS} = 0)
T_{RS} (for reads in the STOP mode)
T_{WS} (for writes in the STOP mode)
$T_{WN} \cong T_{RN}$ (for reads and writes in the NON-STOP mode)

2) Control

This section explains the flags used for access control. The procedure for selecting between the STOP and NON-STOP modes is explained later.

1) TAPMOD
   Bit 7: 1 for the STOP mode, 0 for the NON-STOP mode
   Bits 3 - 0: Number of retries

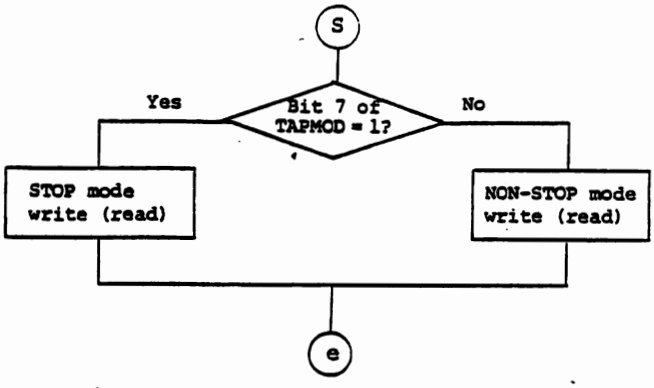
2) TACATR
   Same bit configuration as TAPMOD.

3) DFTATR
   Contains the default value for TACATR; initialized upon reset.

4) TOSCTL
   Bit 5: TCSLAT 0: Access mode is determined from the directory.
   1: Access mode is determined from TACATR.

5) dirtam (i)
   TAPMOD setting at the time of creation of file i (recorded in the directory).

Write (Read)



- TAPMOD is set when a file is created or opened.

  When a file is created, the value of TACATR is set unconditionally.

  When a file is opened, the value of dirtam (i) is set if TCSLAT of TOSCTL is 1, and the value of TACATR is set if its value is 0.

- When a warm boot is made, TACATR is set with the value of DFTATR.

- Bit 5 of TOSCTL is set to 0 when a warm boot is made.

- DFTATR is set with the default value upon reset.

o Relationship between the system display and the (N or S) option of BASIC

Either the STOP or NON-STOP is used for tape reads and writes in BASIC. Procedures for specifying the mode are as follows.

Writes (file creation)

Bit 7 of TACATR is set to 1 for the STOP mode, and to 0 for the NON-STOP mode. Unless otherwise specified, the NON-STOP mode is used.

Reads (file opening)

Bit 5 of TACATR is set to 1 for the STOP mode, and to 0 for the NON-STOP mode. Unless otherwise specified, the bit 5 is set to 0.

Whether or not "STOP" or "NON-STOP" is displayed on the system screen is determined by the setting of bit 7 of TACATR.

Note: The STOP mode can be used for access from BASIC regardless of whether the NON-STOP mode is specified from the system screen. The mode is determined when the file is opened or created.

7.6 Setting the MTOS Controller

MTOS copies system flag 1 to TOSCTL, if MSB of system flag 2 is 1 at MOUNT.
TOSCTL is composed of the flags to control MTOS so that it can decide the MTOS operation for the tape at MOUNT.

TOSCTL configuration

Bit 7	Unused	Always 0.
Bit 6	TCCTCR	1: Adjust the counter. 0: Not adjust the counter.
Bit 5	TCSLAT	1: Access mode unselect. 0: Access mode set by directory.
Bit 4	TCAMFG	1: Performs auto mount. 0: Not perform auto mount.
Bit 3	TCRCFG	1: Check auto remove 0: Not check auto remove.
Bit 2	Unused	
Bit 1	Unused	
Bit 0	TCIGTS	1: MTOS detached from system. 0: MTOS not detached.

Copy Cover & Front
Dave C
Copy Cover Spec
to Dave S.

EPSON AMERICA INC

MEMO

DATE: 5/4/84
REF NO: 978

TO: MR. DAVE CHRISTOPHERSON LOCATION: MS2-4
FROM: E. IDE LOCATION: MS2-1

SUBJ: PINE SPEC

ATTACHED ARE THE FOLLOWING SPECS FOR "PINE":

PINE SYSTEM REV. "B"
MICRO CASSETTE DRIVE (PINE OPTION) REV. "A"

THANK YOU.

EPSON
EPSON CORPORATION
80 Hirooka, shiojiri-shi, Nagano. 399-07 Japan
Phone: 02635-2-2552 Telex: 3342-214 (EPSON J) Cable: EPSON MATSUMOTO

TITLE

PINE OPTION, Micro-Cassette Drive Specifications

ISSUED SECT.	R.Q NO.	NO.

REVISIONS

REV	CHANGE DOCUMENT	DATE		CHECK
A	1st Edition	'84 1/31		

SHEET REVISION STATUS

SH	REV	SH	REV	SH	REV	SH	REV
1	A	15	A				
2	A	16	A				
3	A	17	A				
4	A	18	A				
5	A						
6	A						
7	A						
8	A						
9	A						
10	A						
11	A						
12	A						
13	A						
14	A						

MODEL PINE	DRAWN BY	DATE '84/1/31	CHECKED	DATE	MGR	DATE
COVER SHEET	TOTAL SHEET		NEXT SHEET		SHEET NO.	

Specifications of the Pine Micro-Cassette Option

Contents

1. Application

These specifications apply to the Pine Micro-Cassette Option (abbreviated as PMCT in the following).

2. General Outline

i) The PMCT is an intelligent micro-cassette controller containing a control CMOSMCU6301V.
The PMCT is connected to the Pine cartridge interface and used in handshake mode.
The Pine main unit sends commands or commands and parameters (data) to the micro-cassette option via handshake interface, thus making control of the microcassette drive possible. After completion of operation, or during operation, an ACK in response to the command, or data and ACK, are returned to the main unit.
When some continuous operations are interrupted, the break command is effective.

ii) The PMCT consists of the following elements.

* Frame
* Micro-cassette tape transport mechanism
* Printed circuit board (including MCU)

This specification manual deals with the electric circuits of the printed circuit board including the MCU which contains firmware, and methods of use. For further details on the frame and the mechanism, please consult the following material.

* Pine external design drawing
* Spec sheet for the micro-cassette tape transport mechanism (Olympus Optical Electronics , Ltd.)

iii) As a rule, installation and removal of the PMCT should only be performed with power to the main unit turned off. If it is installed or removed with the power turned on, we cannot be held responsible for any resulting trouble.
When power to the main unit is turned on after the PMCT has been installed, auto-reset of the PMCT is performed and the device as well as the internal RAM are initialized.

3. Hardware Specifications

Pine Micro-Cassette Hardware

Contents

Pine micro-cassette option

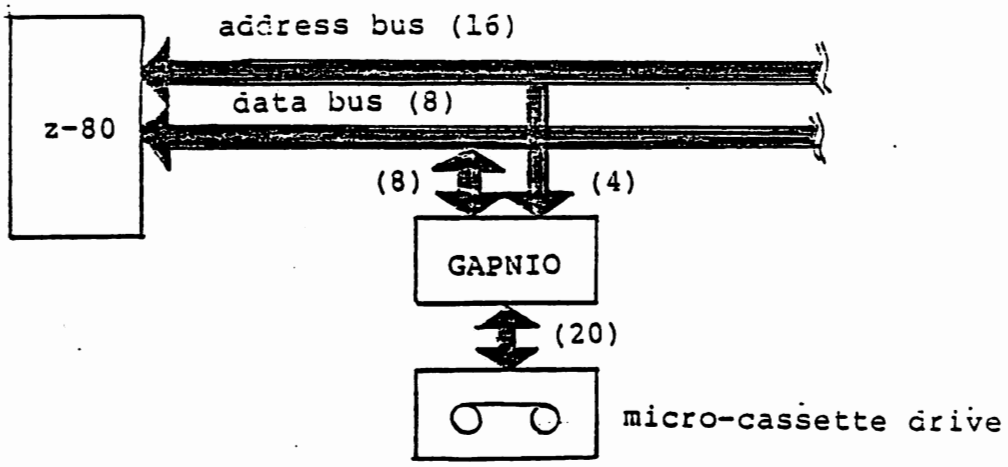
&0 General outline of the system

In the case of Pine, the micro-cassette drive is regarded as one of the options to be connected to the cartridge interface. Various other options can be connected to the cartridge interface (called CTG-IF in the following) connecter, such as ROM cartridges, RAM cartridges, a D-Modem universal cartridge, etc. However, the use of the interface differs for each of these options. As for the micro-cassette option, it is used in handshake (HS) mode.

&&0.1 Cartridge interface (CTG-IF)

The following is a schematic drawing of the system.

Fig. 1 Schematic of the Pine CTG-IF



The micro-cassette option performs in- and output of data to the main CPU (Z80) through the output and input buffers in GAPN10. Control is performed by flags OBF and IBF. When the main CPU writes data or commands to the output buffer, OBF becomes 1 and an interrupt signal (CITO=0) is simultaneously output to the option. When the micro-cassette option reads the data or commands, the interrupt request ceases.

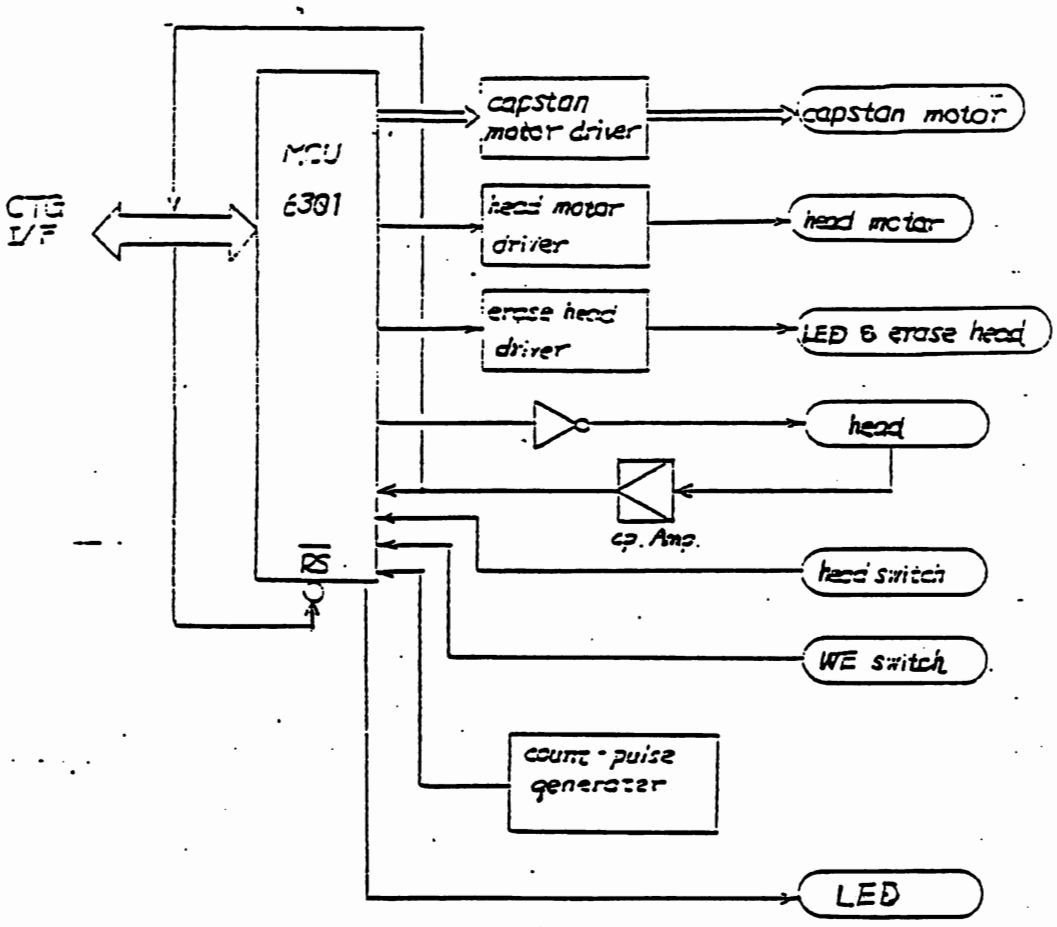
In order to decide whether the information transmitted during communication between main CPU and slave MCU are data or commands, CAB1 and F0 in the status flag register are used. The second bit (CAB1) of the CHSSR assigned to the I/O address $11 is read from the main CPU. If CAB1=0, then the information is data. If CAB1=1, it is a command. Bit 3 (F0) of OPSR assigned to address $101 (in actual practice, any address that fulfils the conditions IOS=0 ($100 - $1FF) and CAB0=1 will do) is read from the slave MCU. If F0=0, then the information is data, if F0=1, then it is a command.

The Pine micro-cassette system has no RAM besides the internal RAM in the MCU6301, and the MCU is not backed up. Therefore, it will sometimes be necessary to send the values in the internal RAM to the main unit and thus save this data if power is turned off.

&&0.2 Configuration of the micro-cassette option

The configuration of the micro-cassette option is shown below.

Fig. 2 Diagram of the micro-cassette option



Pine micro-cassette option

&1 Cartridge interface (CTG-IF)

&&1.1 Names and functions of the 20 CTG connecter terminals

The names and functions of the cartridge connecter terminals in handshake mode are shown below.

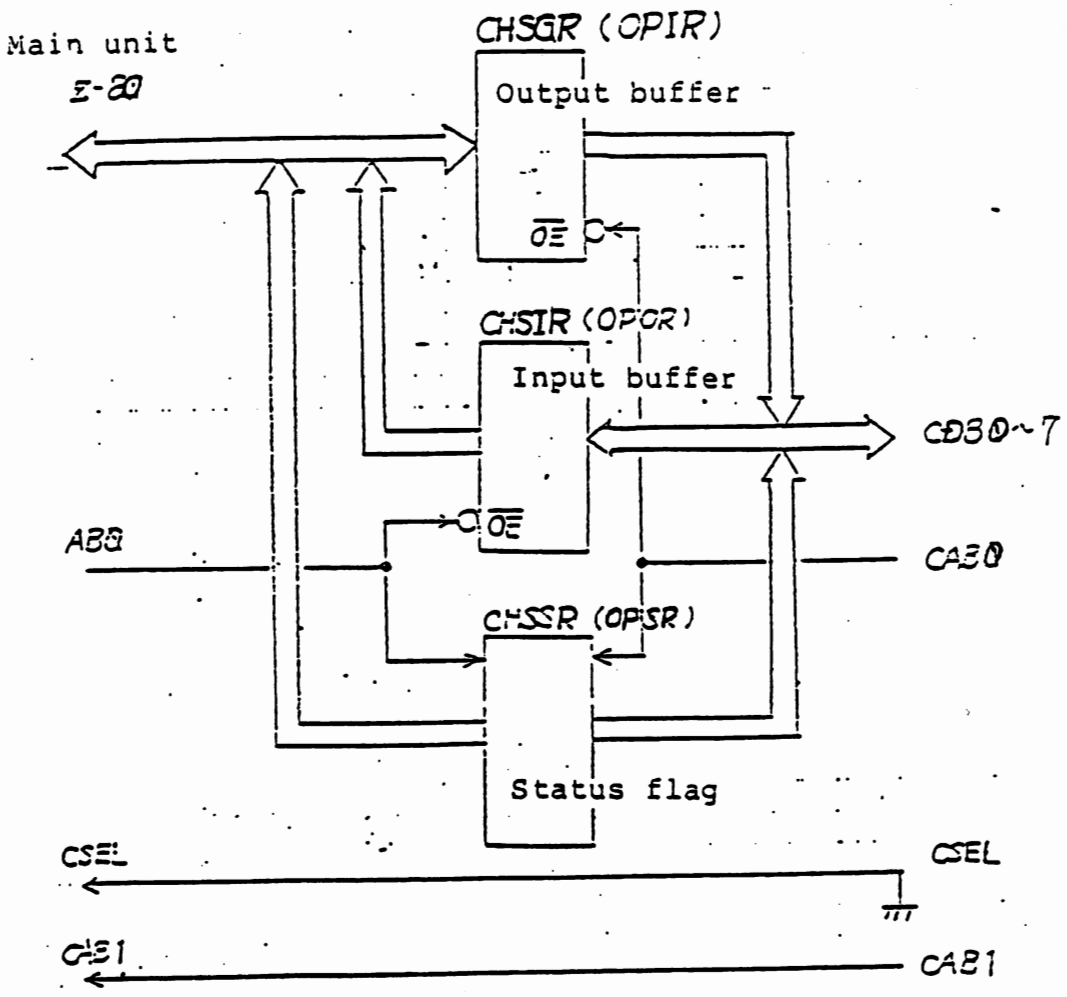
Table 1 Names and functions of the CTG-connecter terminals

Symbol	I/O	Function
$\overline{CCS}$	I	Chip select input from the micro-cassette option. This line is connected to the IOS (SC_1) of 6301. When 6301 accesses the addresses 0100H to 01FFH, it goes to "L" (Mode 5).
CAB1	I	General purpose input line from the micro-cassette option. This line is connected to the 6301 port 1 bit 0(P10). It is set before the 6301 writes data to the output buffer. "L" indicates that the information is data, "H" that it is a command.
CAB0	I	Address input from the micro-cassette option. This line is connected to the LSB (A0; P40) of the 6301 address bus.
$\overline{CRD}$, $\overline{CWR}$	I	Read/write pulse input from the micro-cassette option.
CDB7-0	I/O	Data bus input/output from the micro-cassette option.
CSEL	I	Option select signal input. Pulled down in the micro-cassette option. Can be read from the main CPU as bit 6 of IOSTR.
$\overline{CITO}$	O	Interruption request output to the micro-cassette option. When the main unit has output data or commands to the output buffer, OBF (seen from the main unit) = 1, $\overline{CITO}$=0. When the micro-cassette option reads the data or commands, the interrupt request ceases.
CAVD	I	Input for digital audio signal connected to the speaker. Also used as a general purpose input. In that case, can be read as IOSTR bit 7.
$\overline{CRS}$	O	Reset signal for the cartridge. When 0 is written to the IOCTLR bit 3, the $\overline{CRS}$ terminal becomes 0. When 1 is written, it becomes 1. However, it is not used in the micro-cassette option.
$\overline{CEN}$	I	Enable signal input to 6301.
$\overline{RS}$	O	System reset signal.

&&1.2 Cartridge interface in handshake mode

The structure of the cartridge interface in handshake mode is shown below.

Fig. 3 Diagram of CTG-IF (HS) structure



&&1.3 I/O address space in HS mode

Seen from the main CPU (Z80)

R/W	I/O address	Register name	b7	b6	b5	b4	b3	b2	b1	b0	Flag change
Read	10H	CHSIR	command/data								IBF reset
	11H	CHSSR						OAB1	IBF	IBF	
	12H	Not used (access prohibited)									
	13H										
Write	10H	CHSOR	data								OBF set, F0=0
	11H	CHSOR	command								OBF set, F0=1
	12H	Not used (access prohibited)									
	13H										

CHSIR : Cartridge HS mode input register (CAB1=0 indicates data, CAB=1 commands)
CHSSR : Cartridge HS mode status register
CHSOR : Cartridge HS mode output register

Seen from the CTG option

R/W	Address	CAB0	Register name	b7	b6	b5	b4	b3	b2	b1	b0	Flag change
Read	100H	0	OPIR	command/data								OPIBF reset (OBF reset)
	101H	1	OPSR					F0		OPIBF	OPOBF	
Write	100H	0	OPOR	command/data								OPOBF set (IBF set)
	101H	1	Not used (access prohibited)									

OPIR : Option input register (identical with CHSOR; F0=0 indicates data, 1 connands)
OPOR : Option output register (identical with CHSIR; CAB1=0 indicates data, 1 commands)
OPSR : Option status register (Differs in some points from CHSSR.)
When the slave NCU reads OPIR, the interrupt request ceases.

3.2.4 HS mode operation

In handshake mode (HS), Pine's main CPU Z80 communicates with the cartridge (CTG) option through the output buffer (CHSOR), the input buffer (CHSIR) and the status register (CHSSR). When the main unit writes commands (data) to the output buffers, the option reads it; when the option writes data (commands) into the input buffer (seen from the main unit), the main unit reads it. This handshake is controlled by the flags IBF (OPOBF) and OBF (OPIBF) of the status registers (CHSSR on the main unit side, OPSR for the option side).

When the main unit is writing to the output buffer, AB0=1 (selection of address 11H) indicates commands, AB0=0 (selection of address 10H) data. The value of AB0 at this time is entered into F0 (one of the status flags). This is read as bit 3 of OPSR from the option side. When the main unit writes data or commands to the output buffer, OBF becomes 1 and a interrupt request is simultaneously output to the option ($\overline{CITO}$=0). The value of OBF can be read from both the main unit as well as from the option. However, the meaning is opposite for the main unit and the option, the OBF on the main unit side being the OPIBF on the option side. The same holds true for IBF as well. On the option side, the fact that writing into the output buffer has been performed from the main unit is known due to interrupt or status read. That information is read together with command/data flag F0. When the option reads the output buffer, OBF returns to 0 and $\overline{CITO}$ to 1. The option reads the data (when F0=0) or command (when F0=1) in the output buffer when CAB0=0 (selecting address 100H), or else reads the status when CAB0=1 (selecting address 101H).

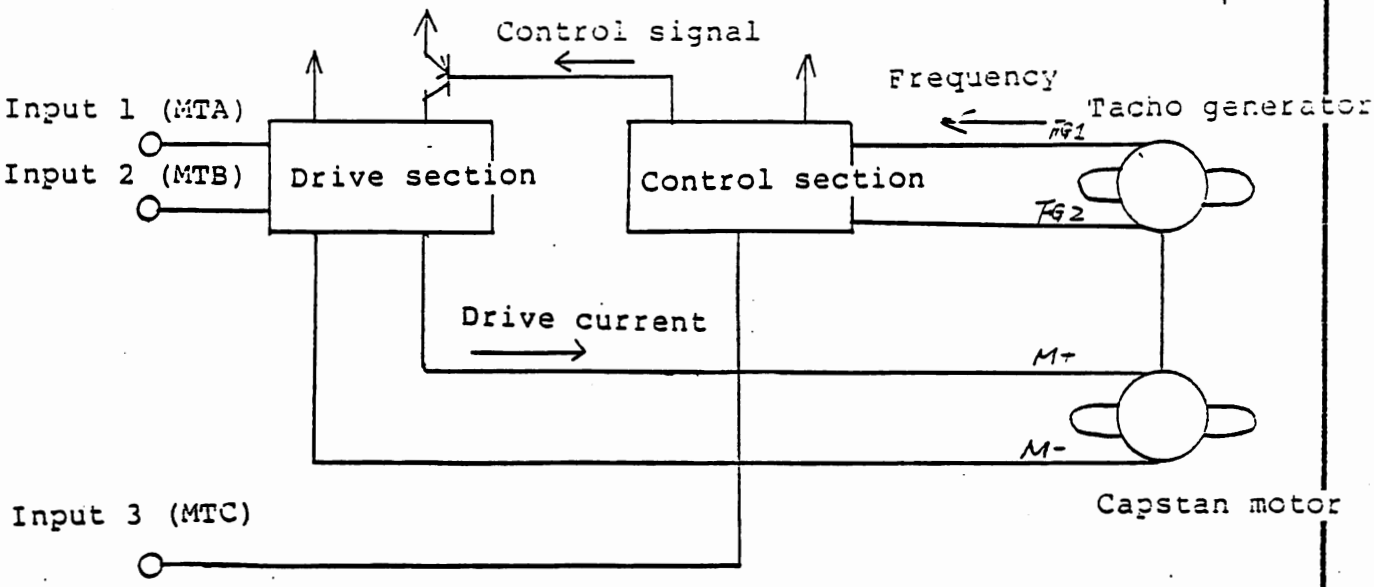
When the option is writing into the input buffer (seen from the main unit), CAB1=0 indicates data, while CAB1=1 means a command. This CAB1 value is entered into bit 2 of the status register CHSSR. When writing to the input buffer is performed, IBF becomes 1, but when the main unit reads the input buffer, IBF returns to 0.

Pine micro-cassette option
&2 Micro-cassette option hardware
&&2.1 General outline of the hardware

The micro-cassette option is an intelligent type containing an MCU 6301. It is interfaced with the main unit's CPU Z80 through the gate assembly GAPIO in the main unit. Details on the interface are given in &1.
In order to secure an I/O port, the slave MCU6301 is used in mode 5. The difference between this and the Maple's micro-cassette drive, besides this difference in modes, is that the counter must be realized in the firmware. Therefore, the hardware counter system consists only of the photo-reflector parts and the waveform generating parts.
All other design factors are practically the same as for the Maple micro-cassette drive. In other words, the capstan motor drive system consists of the 2 ICs M54546L and M51970L. The head motor drive system and brake system are discrete parts, while the signal reading part consists of the operational amp 2904 and a CMOS linear amp.
When creating firmware, attention has to be paid to the following two points: that no RAM is provided on the option, and that the MCU is not backed up.

&&2.2 Design and constants of the various systems

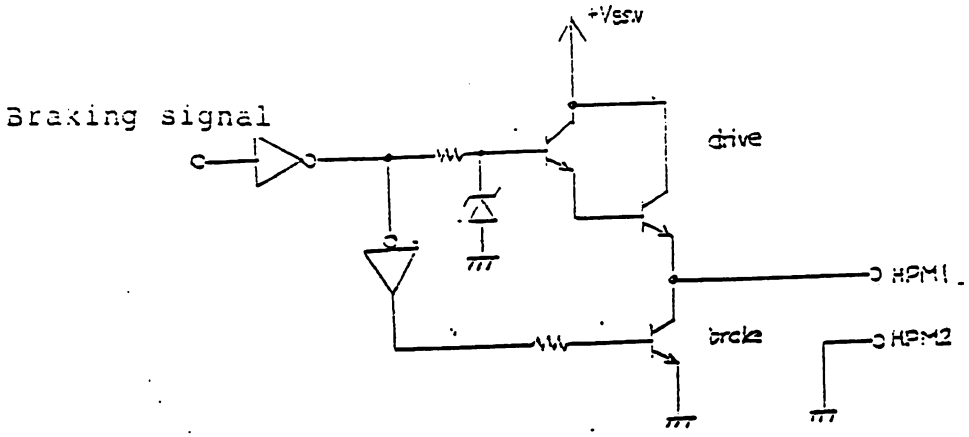
&&&2.2.1 Capstan motor drive system



Input signals and capstan motor operation

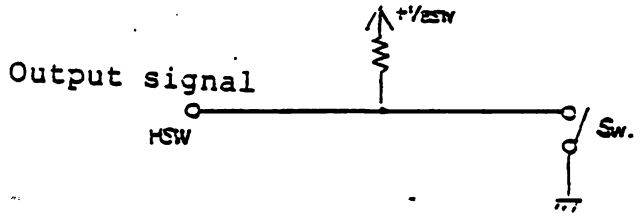
MTA	MTB	MTC	OPERATION
H	L	L	slow feed forward
L	H	L	slow feed backward
H	H	L	brake
L	L	H	don't use
H	L	H	fast feed forward
L	H	H	fast feed backward
H	H	H	don't use

&&&2.2.2 Head motor drive system and braking system



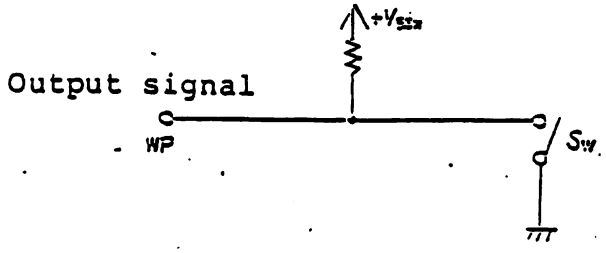
Braking signal	Operation
H	Head motor braking
L	Head motor driven

&&&2.2.3 Head switch section



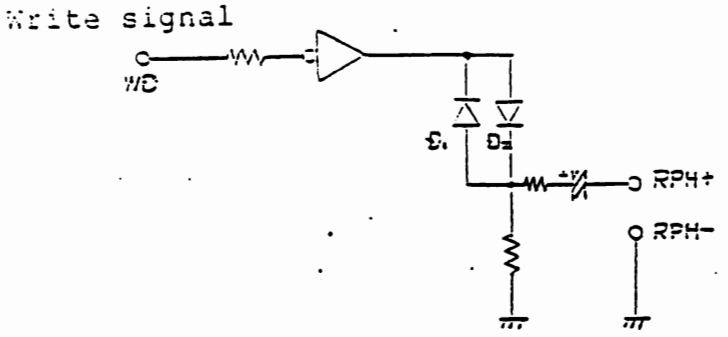
Head condition	Switch condition	Output signal
on	off	H
off	on	L

&&&2.2.4 Mistaken erasure prevention switch section



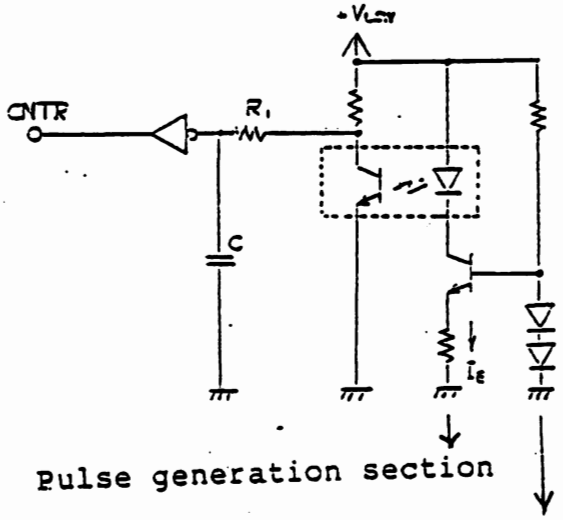
Mistaken erasure prevention pin condition	Switch condition	Output signal
Loss	on	L
No loss	off	H

&&&2.2.5 Write signal output system



Except during writing, ???="H" and D1, D2 are turned off, switching? input and output.

&&&2.2.6 Counter system

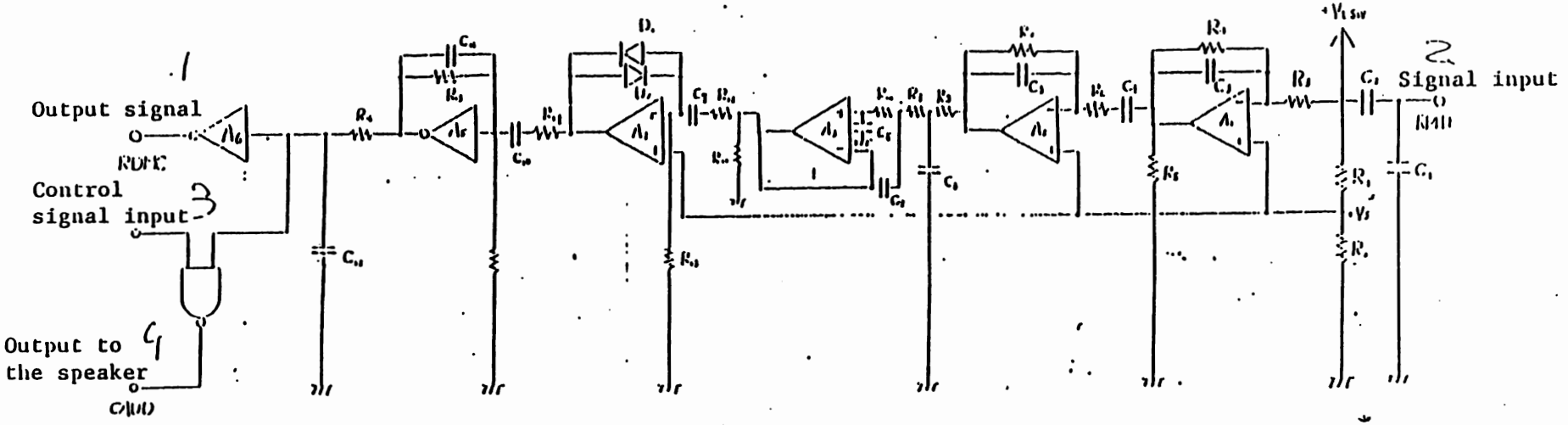


IE=constant

Pulse generation section

Constant current section

§§§ 2.2.7 Amplifier channel for the reading signal



·comparator ·linear amplifier ·peak detector

Third LPF Band Pass 0.5dB ripple Chebyshev characteristics

fc = 3kHz

Inverting amplifier

$G = R_7/R_6$

$B = \frac{\pi}{2} f_c$

$f = \frac{1}{2\pi C_5 R_7}$

Inverting amplifier

gain : $G = -R_4/R_3$

band width: $B = \frac{\pi}{2} f_c$

cut off frequency:

$f = \frac{1}{2\pi C_3 R_4}$

A1, A2 and A3 bias the non-inverted input terminals to VLSWR2/(R1+R2) SO that they operate with a single power source.

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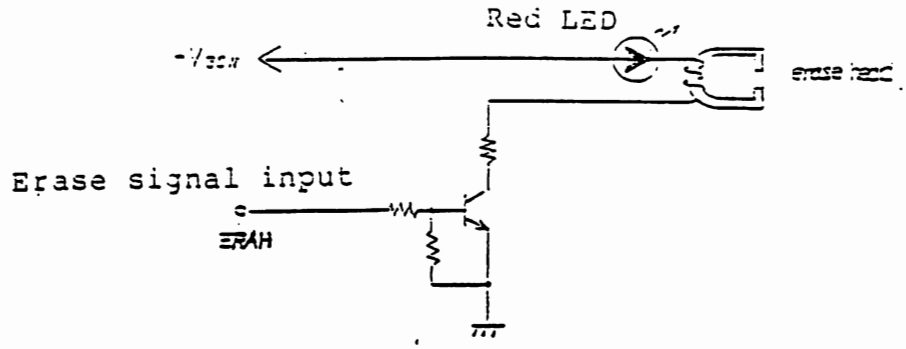
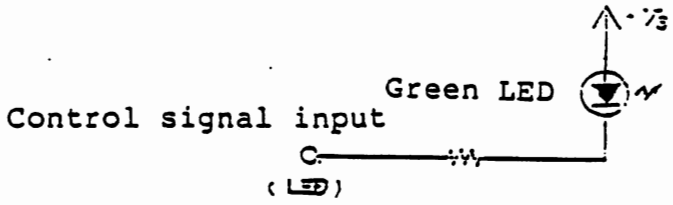
&&&2.2.3 Erase signal generation system



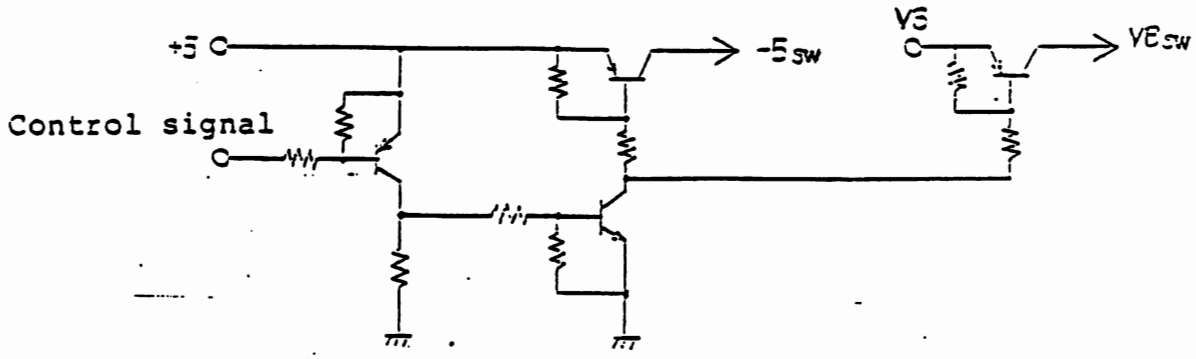
Erase signal	Operation
"H"	Erasure
"L"	-

&&&2.2.9 LED for indicating that tape can be removed



Control signal	LED
H	off
L	on

&&&2.2.10 Power source control system



Control signal	+5SW	VBSW
H	off	off
L	on	on

Pine micro-cassette option

&3. Assignment of the MCU6301 input/output pins

&&3.1 General outline

The MCU 6301 contained in the Pine micro-cassette option is used in mode 5. The inputs/outputs of each port during use in mode 5 are shown below.

Functions of each terminal in mode 5 (mode 6: Cak)

Mode	Part1 (8 lines)	Part2 (8 lines)	Part3 (8 lines)	Part4 (8 lines)	SC1	SC2
6 expan-ded MUX	I/O	I/O	address bus (A0-A7) data bus (D0-D7)	address bus (A8-A13)	AS (O)	R/$\overline{W}$ (O)
5 expan-ded MUX	I/O	I/O	data bus (D0-D7)	address bus (A0-A7)	$\overline{IOS}$ (O)	R/$\overline{W}$ (O)

I=input, O=output, AS=address strobe, R/W=read/write, $\overline{IOS}$=I/O select

* These terminals can be used as I/O terminals (for input only) in order of precedence when they are not needed as address lines.

Since Pine is used in mode 5 and Oak in mode 6, the condition of the mode setting ports (P20, P21, P22) must be established during reset.

&&3.2 Assignment of the input/output pins

The following shows the assignment of the input/output pins for the MCU6301.

Pin No.	Name	I/O	Function	Connection to CTG-IF
1	V_{SS}	I	Ground	GND
2	XTAL	I	Quartz connection terminal - 4MHz	
3	EXTAL	I	Quartz connection terminal (ground side)	
4	$\overline{NMI}$	I	Non-maskable interrupt input terminal (pulls up)	
5	$\overline{IRQ_1}$	I	Interrupt request 1 input terminal	$\overline{CITO}$
6	$\overline{RES}$	I	Reset signal input terminal	$\overline{RS}$
7	$\overline{STBY}$	I	Standby signal input terminal (pulls up)	
8	P20	I	Mode setting terminal (H at reset). Read signal input terminal.	
9	P21	O	Mode setting terminal (L at reset). Write signal output terminal.	
10	P22	O	Mode setting terminal (H at reset). LED control terminal (L:on, H:off)	
11	P23	I	Serial input terminal	
12	P24	O	Serial output terminal	
13	P10	O	HS mode control signal (H: command, L: data) output terminal)	CAB1
14	P11	O	Erase head control signal (H: erasure) output terminal	
15	P12	O	Head motor control signal (H:brake, L:drive) output terminal and speaker output switch (L:off)	
16	P13	O	Capstan motor control signal (MTA) output terminal	
17	P14	O	Capstan motor control signal (MTB) output terminal	
18	P15	O	Capstan motor control signal (MTC) output terminal	
19	P16	O	Operational amp etc. logic side power control signal output terminal	
20	P17	O	$\overline{IRQ}$ mask set (L: mask)	

21	Vcc	I	Power (+5V) input terminal	Vcc
22	P47	I	Head switch signal input terminal	
23	P46	I	Erasure prevention pin detection switch signal input terminal	
24	P45	I	Counter pulse input terminal	
25	P44.....P41	I		
29	P40	O	A0, HS mode control signal (H: status read, L: c/d read)	CAB0
30	P37	I/O	Data bus	
31	P36	I/O	Data bus	
32	P35	I/O	Data bus	
33	P34	I/O	Data bus	
34	P33	I/O	Data bus	
35	P32	I/O	Data bus	
36	P31	I/O	Data bus	
37	P30	I/O	Data bus	

Pin No.	Name	I/O	Function	Connection to CTG-IF
38	SC_2	O	R/W signal output terminal	$\overline{CRD}$, $\overline{CWR}$
39	SC_1	O	I/O select. Active H when MCU accesses $100 - $1FF.	$\overline{CCS}$
40	E	O	Enable signal output terminal	CEN

E01035EA
MB62H114 (FUJITSU)
GAPNIO (Gate Array for PINE Input Output controller)

SPECIFICATION

GAPNIO is Gate Array for PINE and controls Input, Output. It consists of the following blocks.

(1) ART (Asynchronous Receiver Transmitter)
(2) Centro interface
(3) CTG (Cartridge) interface
(4) SIO (Serial IO) interface
(5) RS232C interface
(6) Other IO (LED,Speaker)

A. 58.6.28

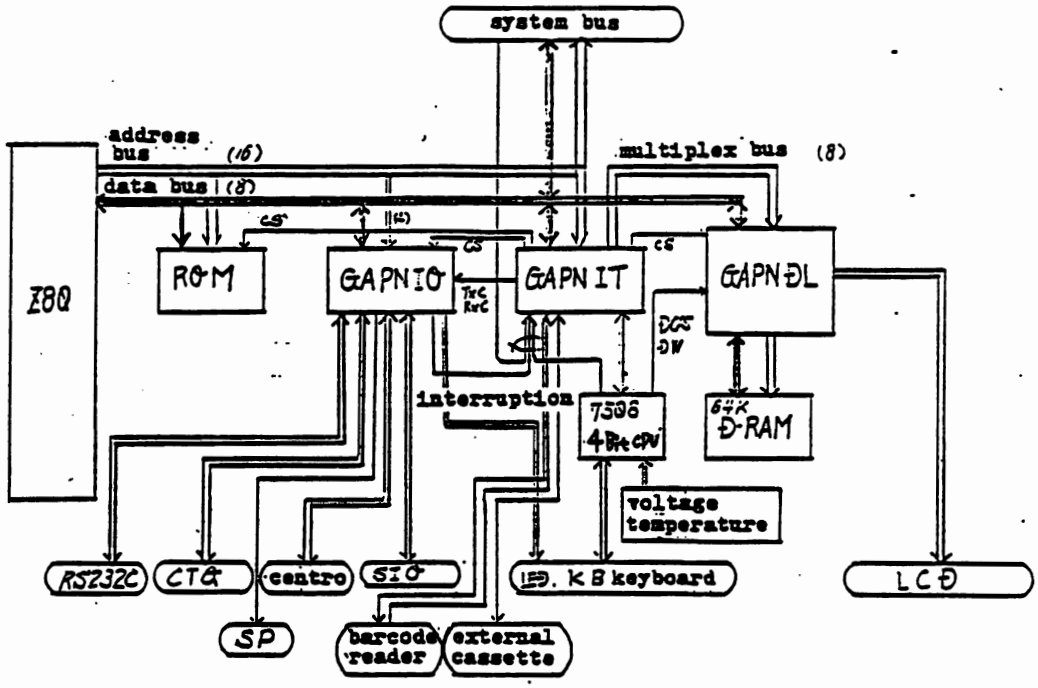
設計 竹田
文責 竹田

EPSON CORPORATION	TITLE	SHEET REVISION	NO.
		0	NEXT / SHEET

1. PINE summary

PINE is made of main CPU Z80, KB-control CPV 7508,64KDRAM, 32K ROM x 3 and 3 gate array (GAPNIO, GAPNIT, GAPNDL). GAPNIO controls main part of IO interface. GAPNIT controls interruption of 7508 interface, timer function, all address space. GAPNDL controls D-RAM and LCD-controller.

1.1 PINE structure



GAPNIO	gate array
GAPNIT	gate array
GAPNDL	gate array(D-RAM,LCD-control)
SIO	serial IO connector
CTG	cartridge connector
7508	4 bit CPU KB control

CS - chip select
DW,DCAS -DRAM control signal when standing by
T x C,R x C -Serial IO clock

19		IOCTLR	IO Control register (8)						
		SP	LED2	LED1	LED0	$\overline{CRS}$	SOUT	$\overline{PINI}$	PSTB
1A~1F									
20 ; FF	release to external								

note 1. Access to unused address within 00~1F in the above list is prohibited.If access is being done really,normal action is not guaranted.(Probably other address data will be broken.)

note 2. *: that is EDU (External developement unit), EXA (Exchange address) is used in the development board. It is useful only when is developed.

(Q5W) BANKR - Bankswitch,timer base clock switch

bit 7 4	BANK 3~Q	BANK switch
bit 3	EDU	switch for development board
bit 2	EXA	switch for development board
bit 1,Q	CKSW 1,Q	clockswitch set fit for 2.45 MHZ, 3.07 MHz,3.68 MHz

(Q6W) SIOR - SIO register for 7508 interface

(2) GAPNDL register

(Q8W) VADR - specify VRAM status in DRAM

(Q9W) YOFF - Y offset register

bit 7	DSP Display ON/OFF
bit 5~Q	Y5~Q scroll specification

(QAW) FR - decide frame frequency of LCD

(QBW) SPUR - control impedance of LCD power

(3) GAPNIO register

(1Q~13R) CTG IF - input for cartridge interface

(14R) ARTDIR - received buffer compatibility for 8251

(15R) ARTSR - status register compatibility for 8251 (subset)

(16R) IOSTR - status input

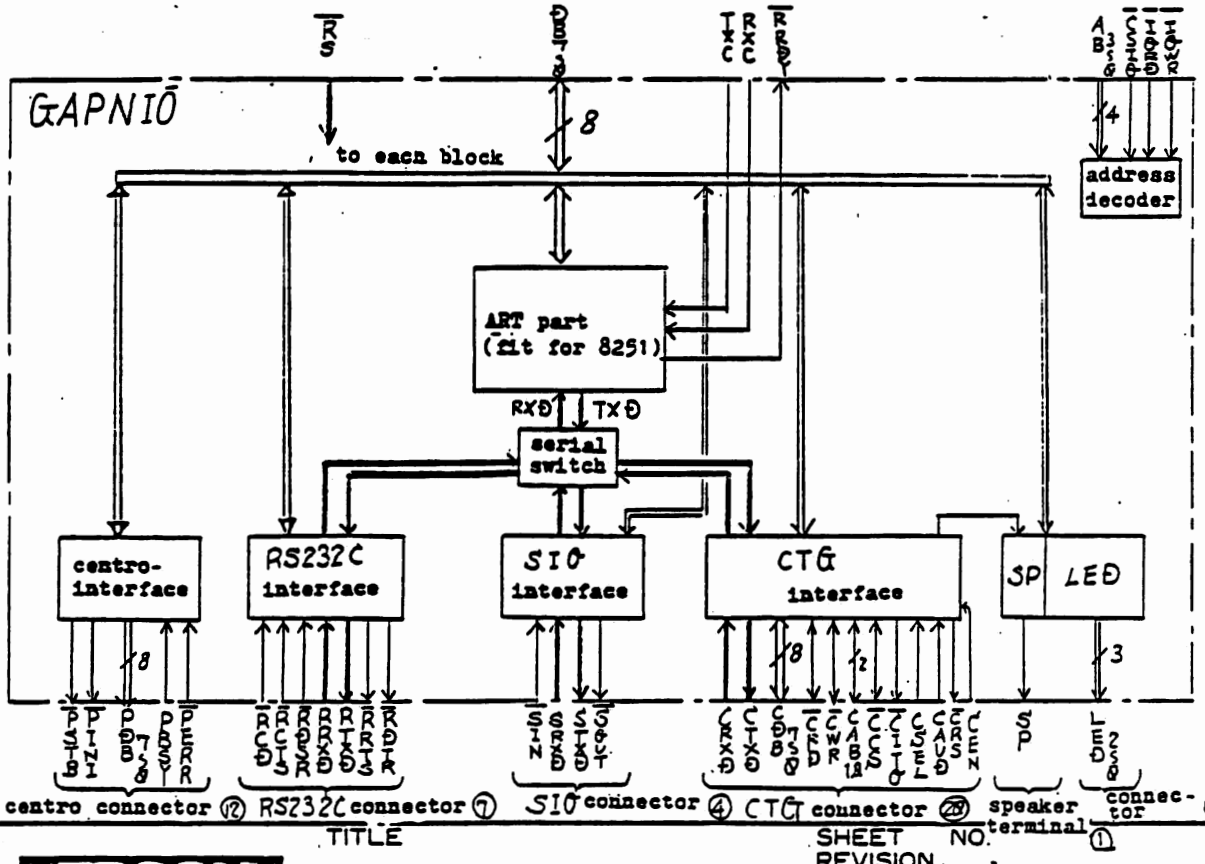
bit 7	CAUD	audio input from cartridge connector
bit 6	CSEL	option input to connection with cartridge connector
bit 5	RCTS	clear to send input
bit 3	RXD	serial data input
bit 2	SIN	SIN input from SIO interface
bit 1	PERR	error input from centro interface(printer)
bit Q	PBSY	busy input from centro interface (printer)

(1Q~13W) CTG IF - output for cartridge interface

2. GAPNIO summary

This chapter aims at understanding the GAPNIO structure. As all matters which it is necessary to make programming by GAPNIO is put on this chapter, it is enough for the persons concerned to software to read this chapter only. Harware contents ex. circuit is explained minimum necessarily in this chapter,butit is detailed in the chapter 3. The persons concerned to hardware have to be reffered to the chpter 3 also. Diagram in this chapter is little different from real diagram for easy understanding, but as it is correct logically,it is no problem to programming.

2.1 GAPNIO block diagram



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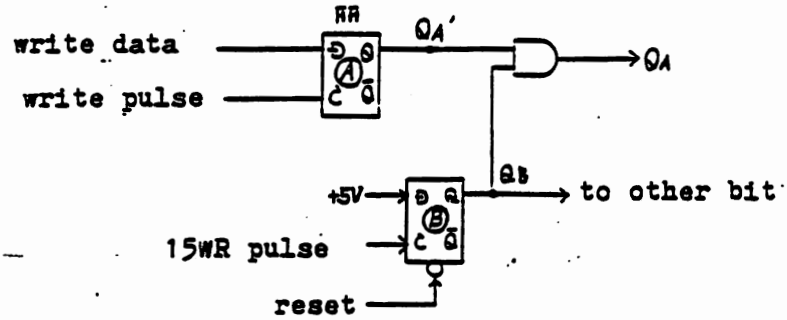
2.2 Register initial reset

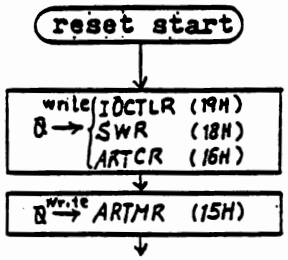
In the element composing of circuit, memory element value of flip flop, latch etc. does not be fixed uniquely when power is on. But these memory elements in the circuit are used as status control, port output and those value is significant when power is on or reset and those value must be fixed uniquely for the most part. In this case, memory element with reset terminal is used generally and external reset input connects to memory reset terminal.
Memory element usage in GAPNIO divides 3 following items.

(1) register, initial reset is not necessary(register to write data from CPU, ARTDOR etc.)
(2) register, initial reset is necessary (register to write data from CPU, ARTCR etc.)
(3) flag control system, initial reset is necessary (not write directly data from CPU, TxRDY etc.)

In the above (2),(3), initial reset is necessary and about (3) flip flop with reset terminal is used and about (2), it is the following special usage for hardware economy.



Register belonging to (2), is 3 register i.e. ARTCR (address 16H), SWR (address 18H), IOCTLR (address 19H) and the above flip flop A shows these bits. As A has no reset terminal, Q_A' initial value is indefinite. On the other thing, flip flop B is for masking output from A and it is reset initially and initial value is 0. Accordingly, Q_A initial value is 0 also. So in the programming it is good to write data as $Q_A' = 0$ during $Q_B = 0$. After, by setting $Q_B = 1$, then initialization is comleted. Q_B is set to 1 by write command to address 15H and then, by resetting again, Q_B remains 1. By the above initialized routine, Q_A seems to be same output from FF with reset terminal.
Initialzation routine summary is as follows.

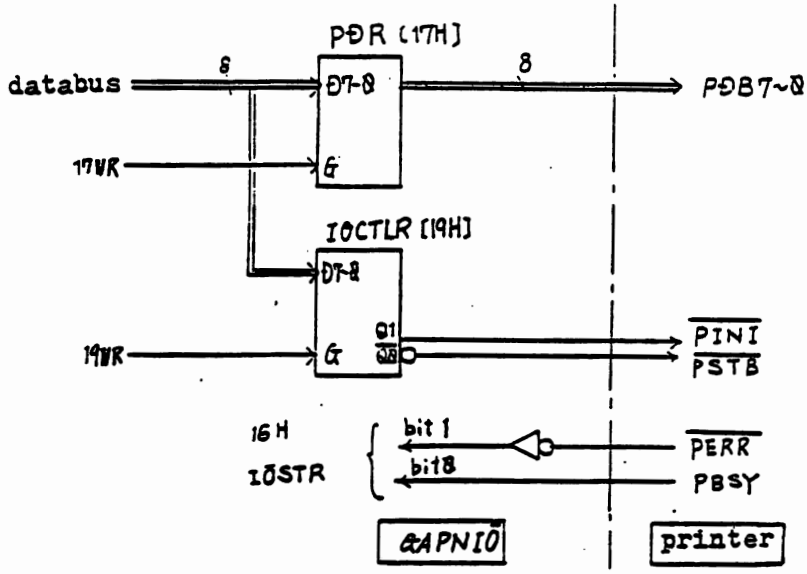


--- any write data is good to ARTMR

note: Hereafter, initial reset for ARTCR, SWR, IOCTLR means initialization routine to be explained here.

2.3.1 Centro interface

Centro interface is 8 bit parallel interface and connects to standard printer. Data strobe signal PSTB is supplied from main part and it does handshake by busy signal PBSY from printer. In addition to PSTB, PBSY, there are PERR which shows printer error status and PINT which initializes printer from main part. Totally, interface is done by 12 signal.



centro interface block diagramm

☐ Terminal name and relation to register

Terminal name	Main Part ⟷ Printer	Logical	Function (terminal)	Corresponding register	Description(register)
PDB7 ~ 0	⟶	posi.	parallel 8 bit data	(17H) PDR	write 1 to register, PDB i terminal becomes 1. PDR is not reset initial.
$\overline{PSTB}$	⟶	nega.	data strove signal. pulse width is min 0.5 μs generally High, active Low	(19H) IO CTLR bit 0 PSTB	write 1 to register, $\overline{PSTB}$ terminal becomes 0. PSTB bit is reset initially PSTB terminal becomes 1.
$\overline{PINI}$	⟶	nega.	initial reset for printer controller Pulse width is min 50 μs. Generally High reset by Low.	(19H) IO CTLR bit 1 $\overline{PINI}$	write 0 to register, $\overline{PINI}$ terminal becomes 0. By initial reset, $\overline{PINI}$ terminal becomes 0.
PBSY	⟵	posi.	High is, printer cannot accept data	(16H) IO STR bit 0 PBSY	when PBSY is 1, 1 is input value.
$\overline{PERR}$	⟵	nega.	Low is, printer is error status	(16H) IO STR bit 1 PERR	when $\overline{PERR}$ is 0, 1 is input value.

note : In this case, initial reset means initialization routine by programming described 2.2 chapter.

2.3.2 CTG IF (cartridge interface)

PINE CTG interface connector can connect with option equipments such as Micro cassette, ROM cartridge, RAM cartridge, D-MODEM, universal cartridge, CTG IF works with these option equipments. According to connecting option equipments, how to work as interface is different in each case and CTG IF copes with by mode switch. CTG IF has 4 modes and mode is decided by option. Each mode is as follows.

(1) HS mode (handshake mode)
As micro cassette , it is CPU to CPU interface with device having CPU at option side and it is similar to 8255 Handshake mode. It exchanges data through output buffer,input buffer. Control of data exchange is done by flag (JBF,OBF).

(2) IO mode (input output port mode)
It takes interface in the form of 4 bit input port or 4 bit output port. D-MODEM is this mode.(Higher 4 bit output,Lower 4 bit output)

(3) DB mode, option looks like ordinary IO device in view of main part. CTG IF connects directly data bus at the main part to cartridge data bus. Cartridge option has 4 address space 10H 13H. ROM, RAM cartridges are connected by this mode.

(4) OT mode (output port mode) .
This takes interface in the form of 8 bit output port.

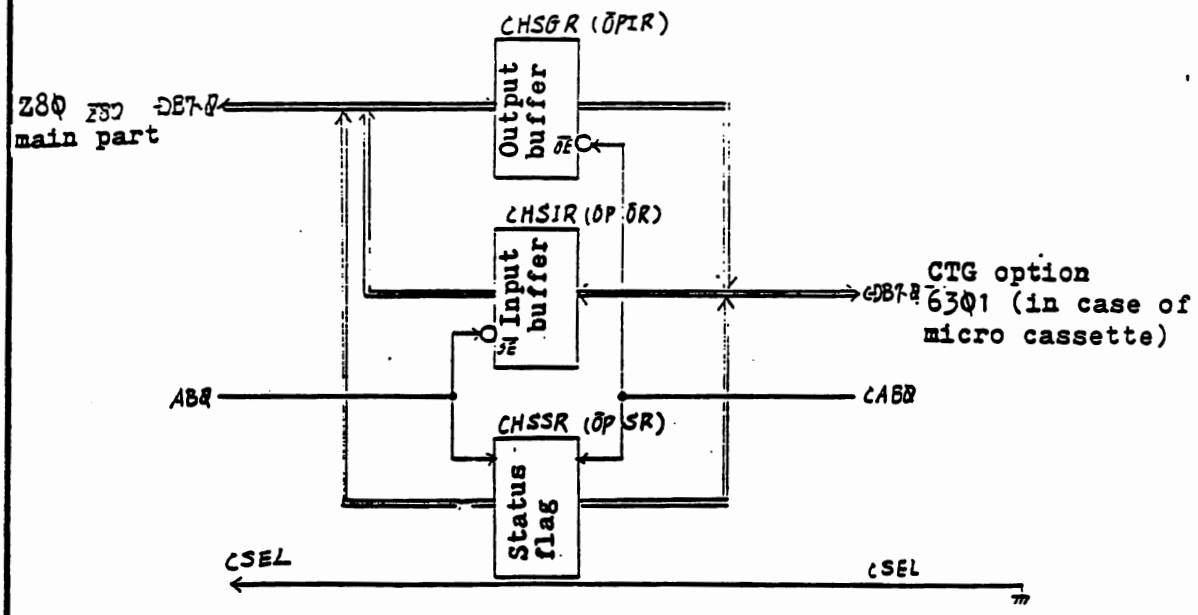
☐ Mode setting

CTG IF mode is done by cartridge switch CSW 1,CSW0 (bit 1,0) in switch register (SWR, address 18H)
CSW 1.0 is set to HS mode (i.e. CSW 1=0,CSW 0=0) by initialization routine at GAPNIO.

CSW1	CSW0	mode
0	0	HS mode
0	1	IO mode
1	0	DB mode
1	1	OT mode

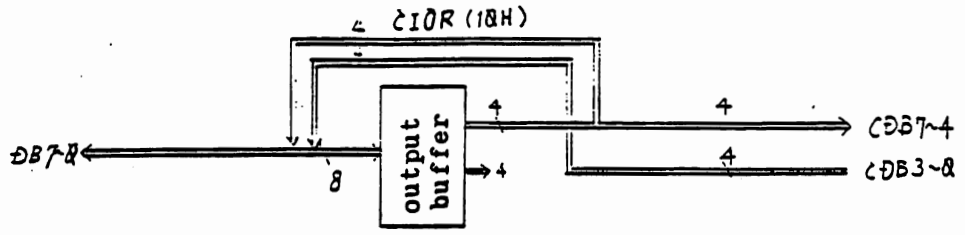
---(Higher 4 bit out,Lower 4 bit in)

☐ HS mode (CSW1=Q, CSW0=0)



At HS mode, main part works by interface with CTG option through output buffer, input buffer. When main part writes data to output buffer, option reads it and oppositely , when option writes data to input buffer, main-part reads it. The handshake is done by OBF(output buffer full), IBF (input buffer full).
CDB7~Q, CABQ, $\overline{CRD}$, $\overline{CWR}$, $\overline{CCS}$ etc. are sent from option side. When main part writes data to output buffer, it becomes a command in case of ABQ=1, a data in case of AB0=Q. Then ABQ value is taken by FQ, one of status flag and this is seen by status read from option side. In spite of OBF=1, $\overline{CITO}$=Q at the same time and then, interrupt request to option generates. About OBF value, it can be seen by status read in both main part and option part.(But in the main part and option part, OBF, IBF is opposite each other and OBF in view of main part is IBF to the option part). On the option side, it can be known that data is written from main part to buffer by interrupt or status read. The data is readable with command/data flag FQ. When option reads output buffer, it returns OBF=Q, $\overline{CITO}$=1. Option reads data of output buffer in case of CABQ=1.
Oppositely, when option writes data to input buffer (no distinction between command and data about write from option. So, CABQ value is considered as Q and it is promised to be Q) then it becomes IBF=1, main part reads input buffer after investigating the value by status read. After readeing input buffer,it returns IBF=Q. It reads data (input buffer) from main part in case of IBF=Q and reads status in case of ABQ=1. At HS mode, CAB1 is not address, it's general input from option. This CAB1 value is readable as a part of status from main part. Further, at HS mode option, CSEL must be pulled down as it becomes Q.

☐ IO mode (CSW1=0, CSW0=1)

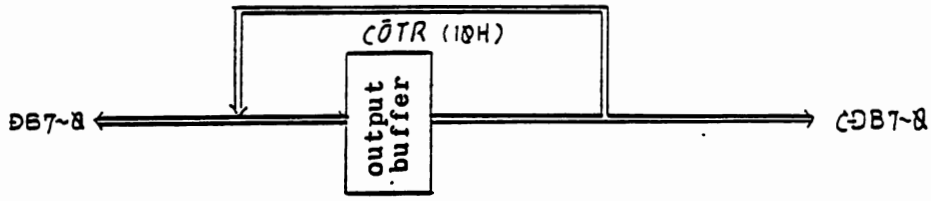


IO mode consists of 4 bit output port (CDB7~4) and 4 bit input port (CDB3~0). Output side consists of 8 bit latch (CIOR, cartridge IO mode register) and to the input side without latch, value of CDB3~0 terminal is entered as it is. IO address is 10H.
When data is written 10H address, content of data bus 8 bit is written to CIOR. Higher 4 bit output from CIOR connects to CDB 7~4 directly, but lower 4 bit output does not connect to anywhere. When data is read from 10H address, value of CDB3~0 terminal enters directly as data bus lower 4 bit and value of higher 4 bit from output buffer enters as higher 4 bit. That is, output port value of higher 4 bit is readable by 10H Read.
At IO mode, it is CSEL=1. Further, $\overline{CCS}$, CAB1, CAB0, $\overline{CWR}$, $\overline{CRD}$ etc. are high-impedance and besides they are input. Accordingly, they must be pull-up or pull-down as they becomes inactive . $\overline{CITO}$ output is 1.Flag is not usable at all.

IO mode IO address space

R/W	IO address	register name	D7 6 5 4	3 2 1 0
READ	10	CIOR	content of output port	CDB3~0
	11	unused (access prohibited)		
	12			
	13			
WRITE	10	CIOR	4bits data	don't care
	11	unused (access prohibited)		
	12			
	13			

☐ OT mode (CSW=1, CSWQ=1)



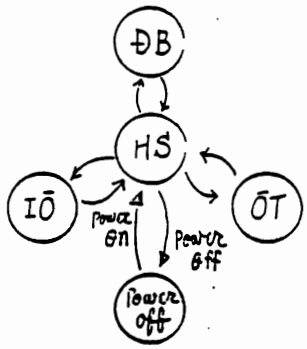
OT mode consists of 8 bit output ratch. Output buffer address (COTR, cartridge OT mode register) is 10H and when data is written to 10H ,content of bus DB7~0 transmitts to COTR and simultaneously, it becomes to output CDB7~0. When reading 10H address, COTR contents is read. At OT mode, it must be CSEL 1.Further, $\overline{CCS}$, CAB1, CAB0, $\overline{CWR}$, $\overline{CRD}$ etc are high-impedance and besides they are input. Accordingly, they must be pull-up or pull-down as they becomes inactive. CITO output is 1. Flag is not usable at all.

OT mode OT address space

R/W	IO address	register name	D7 6 5 4 3 2 1 0
READ	10	COTR	(content of output port)
	11	unused (access prohibited)	
	12		
	13		
WRITE	10	COTR	8bits data
	11	unused (access prohibited)	
	12		
	13		

note: Register, CHSOR, CIOR etc are the same thing physically.

A mode must be selected always through HS mode as stated above. The relation among each mode can be described like the figure on the right. Initial set values of output port of IO, OT mode option are described in the specification of each option, but they are generaly considered equal to the value acquired when 13H is read in DB mode. (refer to the specification of D-MODEM option for PINE.)

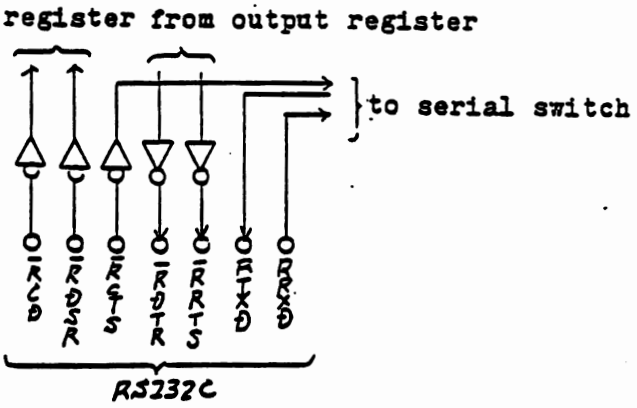


☐ Flag (IBF,OBF)

IBF, OBF enter a reset state by a reset input. For example, when power is applicated, IBF-0, OBF-0. Set and reset conditions are already described. IBF and OBF are always in a reset state in a mode other than HS mode. Therefore, when HS mode is established from another mode, IBF, OBF-0.

2.3.3 RS232 interface

RS232 interface is a serial interface and it is composed of 7 signal lines; RRXD, RTXD (transmit-receive lines) $\overline{RCD}$, $\overline{RCTS}$, $\overline{RDSR}$ (control input) $\overline{RRTS}$, $\overline{RDTR}$ (control output). RRXD, RTXD can be connected to ART through the serial switch. To get detail informations on RRXD, RTXD, refer to 2.3.5 (serial switch), 2.3.6 (ART). $\overline{RCD}$, $\overline{RCTS}$, $\overline{RDSR}$ can be read respectively as bit 4, bit 5 of IOSTR, bit 7 of ARTSR. The negative logic is applied to these pins while the input of data read in the main device is based on the positive logic. So the value reverses. i.e. if the value of a pin is 0, 1 is input in the bit of the corresponding register. As far as $\overline{RCTS}$ concerned, this rule is not necessarily valid, depending on the values of SSW1, SSW0 (serial switch). Refer to 2.3.5 to get detail information on this matter.(If SSW 1, the rule is valid for RCTS like the other pins. If SSW1=0, the value of the bit of the corresponding register is 1 independent of the pin value of $\overline{RCTS}$.)
The output pins $\overline{RDTR}$, $\overline{RRTS}$ are respectively the reverse of the bit 5 and of the bit 5 of ARTCR. If 1 is written in these bits, the pin value becomes 0. The pin values becomes 1 by initial reset.



☐ Polarity of RS232C

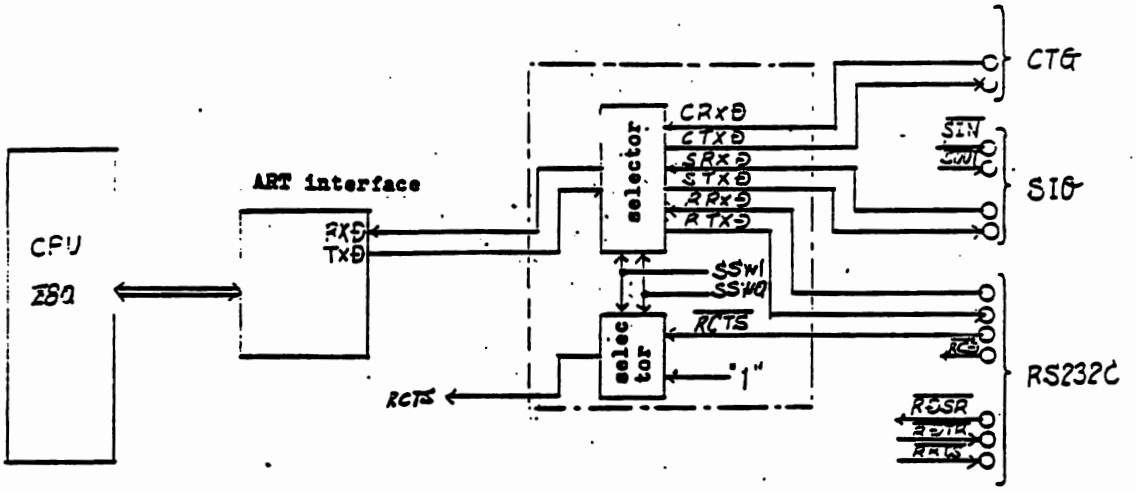
The polarity of each signal of RS232C varies among the read from a register in the main device, the pin value of the gate array and the value in the connector. The following table is put in order to make this confusing matter clearer.

signal	corresponding register bit polarity	pin of GAPNIO polarity	connector polarity	value of a initial reset, corresponding bit, corresponding pin
RRXD Receive Data		RRXD Positive	$\overline{RRXD}$ Negative	
RTXD Transmit Data		RTXD Positive	$\overline{RTXD}$ Negative	
RRTS Request To Send	ARTCR 5 Positive	$\overline{RRTS}$ Negative	RRTS Positive	0 , 1
RDTR Data Terminal Ready	ARTCR 1 Positive	$\overline{RDTR}$ Negative	RDTR Positive.	0 , 1
RCTS Clear To Send	IOSTR 5 Positive	$\overline{RCTS}$ Negative	RCTS Positive	
RDSR Data Set Ready	ARTSR 7 Positive	$\overline{RDSR}$ Negative	RDSR Positive	
RCD Carrier Detect	IOSTR 4 Positive	$\overline{RCD}$ Negative	RCD Positive	

note: RRXD can be read as bit 3 of IOSTR if SSW1=1, refer to 2.3.6

2.3.5 serial switch (serial selection circuit)

PINE has 3 serial interface; RS232C, SIO (serial IO), SIO of SIO (serial IO of the cartridge). The serial selection circuit has function of selecting one interface among these three and connecting it to ART (8251 compatible) the selection is performed through the selection bit SSW1,0 (serial switch 1,0 SWR bit 3,2). The following figure and table summarizes respectively the block chart of the serial system and the relation between SSW1,0 and signals.

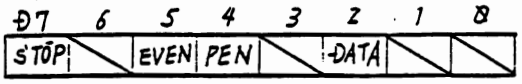


serial mode	SSW1	SSW0	RXD	TXD	RCTS
0	0	0	(CTG) CRXD	(CTG) CTXD	1
1	0	1	(SIO) SRXD	(SIO) STXD	1
2	1	0	(RS232C) RRXD	(RS232C) RTXD	$\overline{RCTS}$ terminal reverse.
3	1	1	(RS232C) RRXD	(SIO) STXD	$\overline{RCTS}$ terminal reverse

Serial mode 4 is a special mode which is intended for receiving from RS232C and transmitting to SIO.
Each signalof CTXD, STXD and RTXD is in a High state (Mark signal) when no selection is being made.
When power is applied, the select bits SSW1,0 does not enter a reset state. i.e. they are unsettled. So it is necessary to set the select bits correctly before use. (The serial mode 0 is set by the initialization routine described in 2.2)

Register descriptions

(1) ARTMR ART mode register (15H) .... corresponds to 8251 mode instruction don't care



don't care

STOP------Number of bit
{=1 2 bits
{=0 1 bit

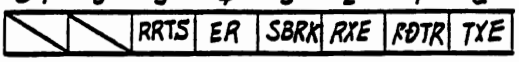
EVEN----- Parity Even or Odd . . . valid only when PEN 1
{=1 Even
{=0 Odd

PEN------ Presence or absente of tne parity
{=1 Presence
{=0 Absence

DATA----- Data length (parity bits escluded)
{=1 8 bits
{=0 7 bits

(Different from 8251) 8251 has 3 stop bits (1,1 ½ ,2) and 4 data lengths (5,6,7,8). 8251 has 2 modes (synchronous and asynchronous modes) while ART has only one mode (asynchronous mode). As for the baud rate facter, 8251 has 1,1/16,1/64 while ART has only 1/16 fixed.

(2) ARTCR ART command register (16H) .... corresponds to 8251 command



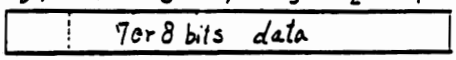
instruction compatible with the correspondent bits of 8251 command register

RRTS,RDTR .... When $\overline{\text{RRTS}}$,$\overline{\text{RDTR}}$ are nigh, output pin valve becomes 0 (refer to 2.3.3)
ER .... Error reset. It resets OE,FE,PE. When RXE=1, Let ER be 1,too.
SBRK .... Break output. This charges TXD forcibly to 0. Valid when TXE=1.
RXE .... This makes ready to receive
TXE .... This makes ready to transmit. TXD=1 as long as TXE=0

note: Only ER is pulse signal. When ER 1 is written, the pulse is transmitted only during writing. Therefore, it is not necessary to return ER=0

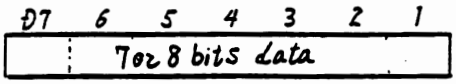
(different from 8251) Bit 7,EH of 8251 is for synchronous mode. So ART has not it. ART has not bit 6,IR (internal reset),neitner. This is applied in 8251 in order to convert mode instruction into command instruction, but ART has no need of it because different addresses were assigned to the command register and mode register. Remember to let TXE and RXE be both 0 before rewriting mode register.

(4) ARTDOR ART data output register (14H) .... corresponds to 8251 transmitter



buffer. Data will be transmitted from TXD after parallel-serial conversion. If the data length is 7 bits (DATA=0), don't care bit 7.

(5) ARTDIR ART data input register (14) .... correspond to 8251 receiver

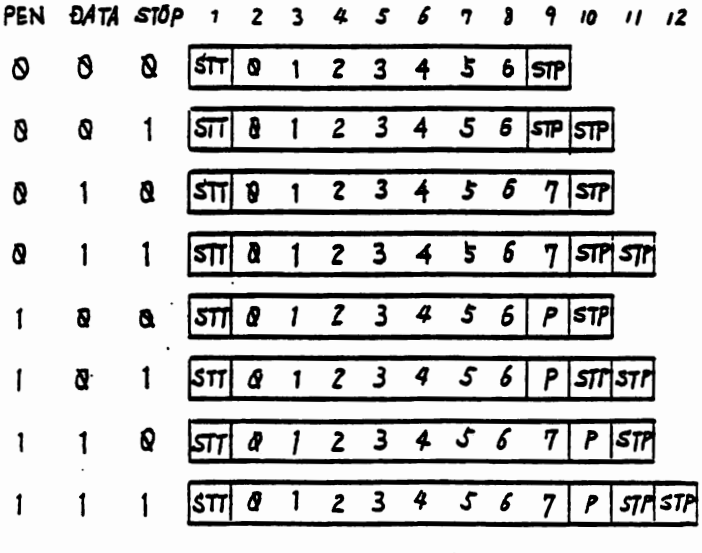


buffer. Data from RXD will be taken in after parallel-serial conversion. If the data length is 7 bits, bit 7=0.

☐ Transmit-receive format

The transmit-receive baud rate of ART is 1/16 of the clock signal TXC,RXC generated by the baud rate generater in GAPNIT. The maximum frequency of TXC, RXC is 614.4 KHZ (38.4K x 16). i.e. the bauds can be extended until 38.4K bauds. 100 baud for ART only. Transmit-receive data are transmitted and received in the follwing order. start bit Data(LSB MSB) Parity bit Stop bit PEN, DATA, STOP values and data format are as follows.

Format



STT - Start bit
STP - Stop bit
P- Parity bit
0~7 - Data, bit 0~7

3 Hardware

This chapter describes the circuits and input-output pins in the gate array GAPNIO as well as input-output AC characteristics.

3.2 GAPNIO input output pins

GAPNIO has 66 input output pins mounted in a 80 pins flat package. The function of each pin is as follws. (Total number of the pins is 70, 4 power lines included

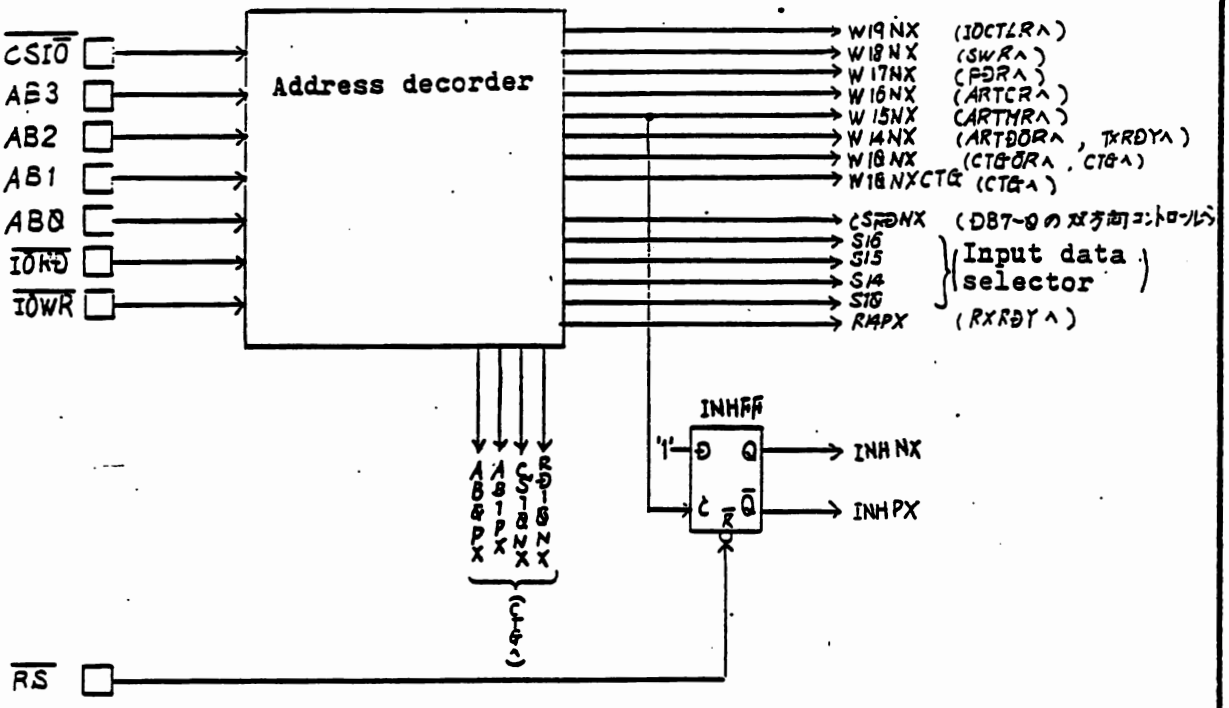
PIN	PIN No	DIRECTION	FUNCTION
AB 3~0	4	input	Address bus lines. Lower 4 bits of Z80 address bus. For decode of IO instructions
$\overline{CSIO}$	1	input	Chip select. GAPNIT generates after decording addresses. It is selected in case of 10H~1FH. Active low
DB7~0	8	bidirectional	Data bus lines. Data bus lines of Z80
$\overline{IORD}$	1	input	Read pulse. Transmitted from GAPNIT. IORQ of Z80 and NAND of RD. Negative logic.
$\overline{IOWR}$	1	input	Write pulse. Transmitted from GAPNIT. WR pulse of Z80 is cut in a part of edge within GAPNIO and it becomes thin and then it becomes $\overline{IOWR}$ with IORQ, NAND. Negative logic.
$\overline{RE}$	1	input	Reset input
RRDY	1	output	Receive ready. This becomes Low when data is set in the receive buffer of ART.
TXC	1	input	Clock for serial transmitter. Used in ART.
RXC	1	input	Clock for serial receiver. Used in ART.
LED2~0	3	output	Output for LED
SP	1	output	Output for speaker
PDB7~0	8	output	Data output for printer (centro-interface)
$\overline{PSTB}$	1	output	Strobe signal for printer. Negative pulse
$\overline{PINI}$	1	output	Initialization signal for printer. Negative pulse.
$\overline{PERR}$	1	input	Signal which indicates error state of printer.If PERR=0, it means error state.
PBSY	1	input	Signal which indicates busy state of printer. If PBSY=1, it means busy state.
CDB7~0	8	bidirectional	Data bus lines of cartridge interface.
$\overline{CCS}$	1	bidirectional	Chip select signal to cartridge. Input in HS mo: Output in DB mode. In DB mode, it becomes low fo. 10H~13H.
CAB1	1	bidirectional	Address lines of cartridge. Address output in DB mode. General input in HS mode.
CAB0	1	bidirectional	Address lines of cartridge. Address output in DB mode. Address input in HS mode.
$\overline{CWR}$	1	bidirectional	Write pulse of cartridge. output in DB mode input in HS mode.
$\overline{CRD}$	1	bidirectional	Read pulse of cartridge. Output in DB mode input in HS mode.
$\overline{CRS}$	1	input	Reset signal to cartridge.
CSEL	1	output	Judge input of cartridge. 0 means HS mode option. 1 means any other option exept HS mode option or no option.
CITO	1	output	Interrupt request to cartridge. When it is written to output register in HS mode, it becomes Low.
CAUD	1	input	Audio input from cartridge . When AUSW of SWR is set to 1 and SP of IOCTLR is set to 0, CAUD signal is output from SP terminal.
CTXD	1	output	Serial data output to cartridge.
CRXD	1	input	Serial data input from cartridge.
SRXD	1	input	Serial data input from SIC.

3.3 Descriptions of the circuit block & AC characteristics.

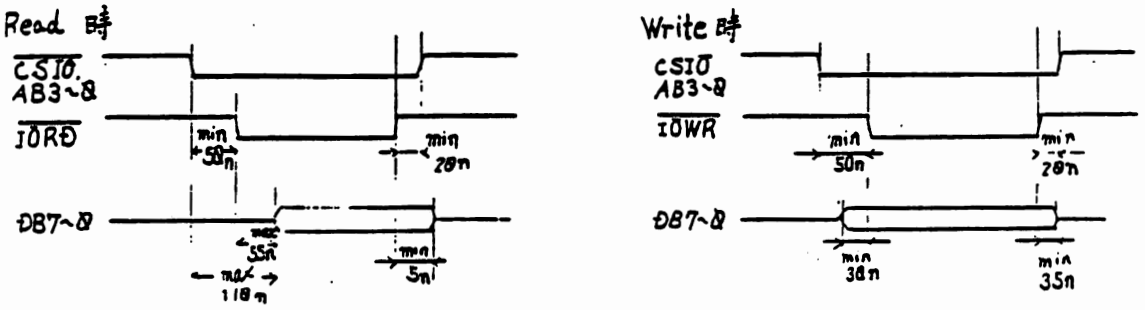
As the block functions are already illustrated in the chapter 2, the circuits and AC characteristics are described in this section.

3.3.1 Address decorder.

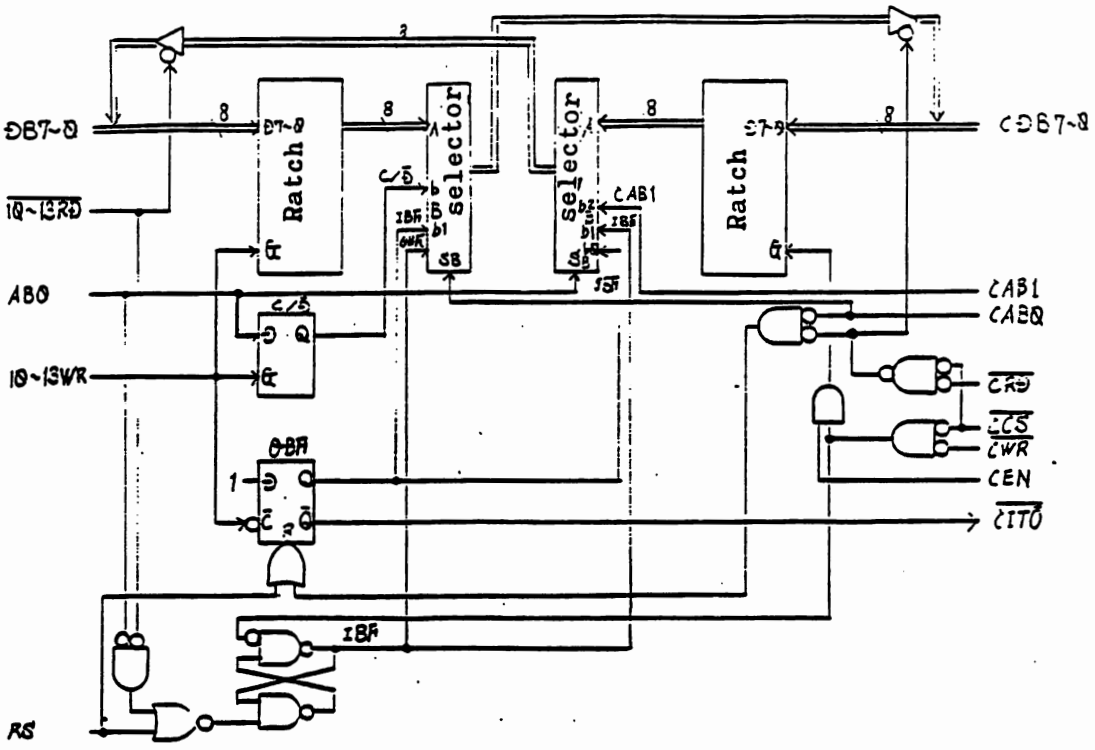
The address decorder decords CSIO, AB3~0 and generates write pulse and read signal. INHFF in the following figure is FF for an initial reset. (Refer to 2.2)



- The following figures show the timing which allows data to be read and written correctly.



(1) HS mode (CSW1=0, CSW0=0)

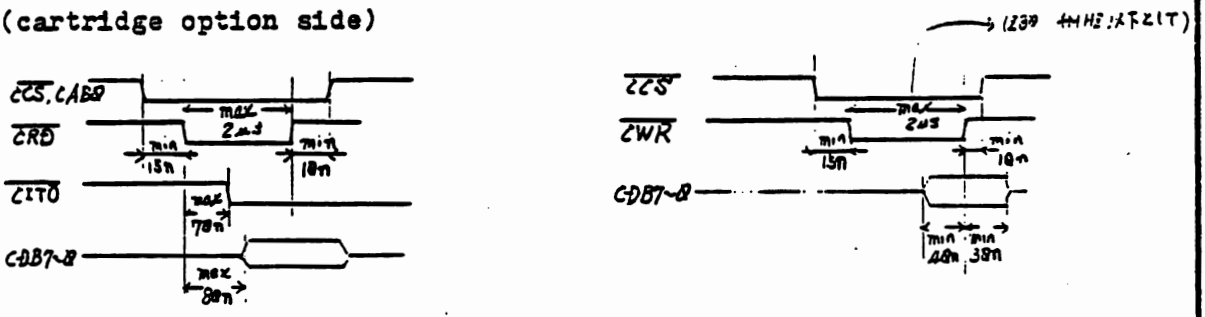


* OBF, IBF are expressed as seen from the main part side.

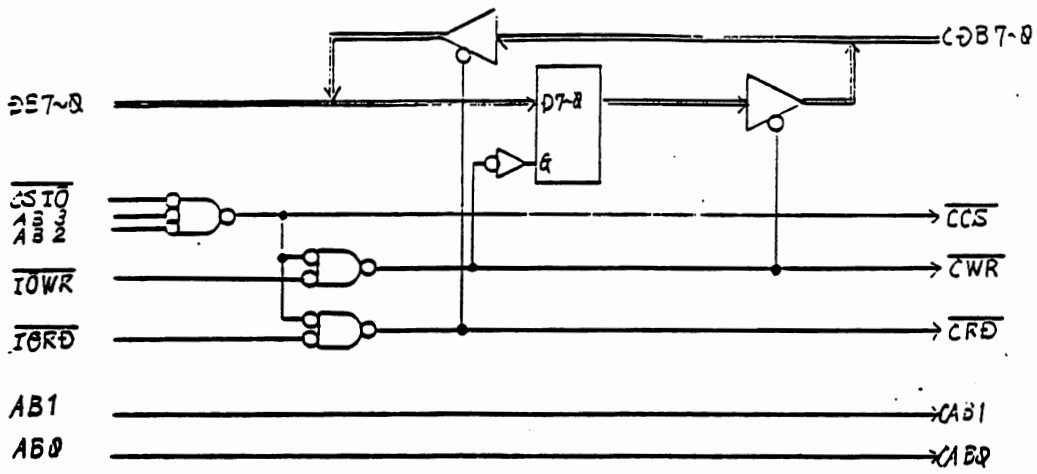
AC characteristics

(CPU side)

(cartridge option side)

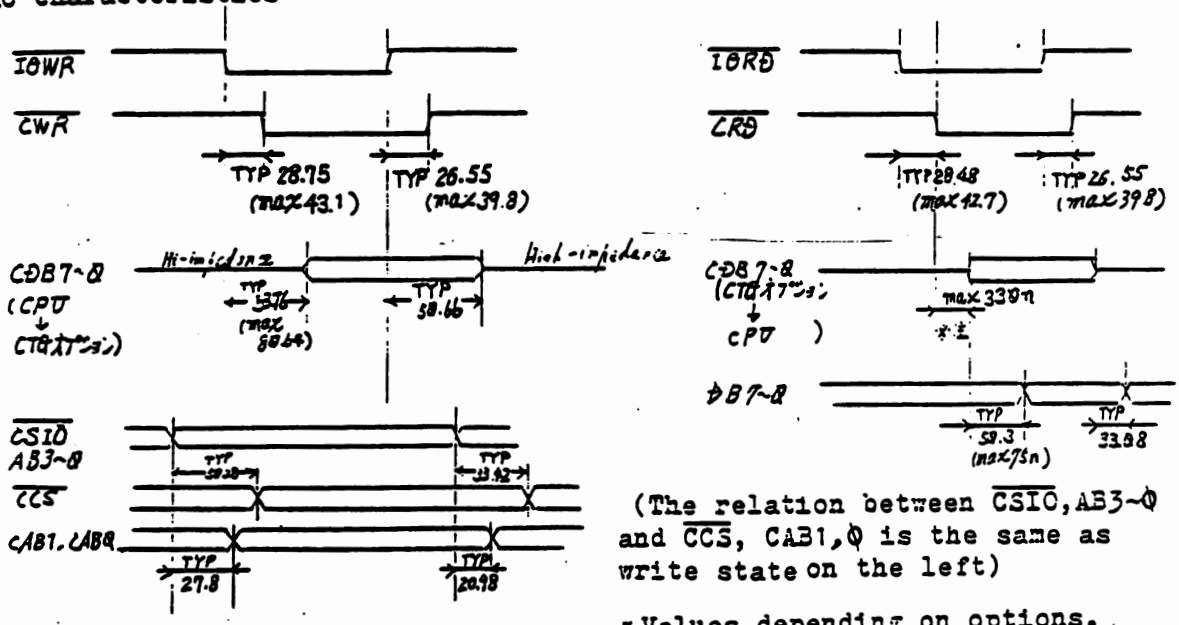


(3) DB mode (CSW1=1, CSW0=0)



* $\overline{CITO}$ is High
* OBF and IBF are in a reset state.

AC characteristics

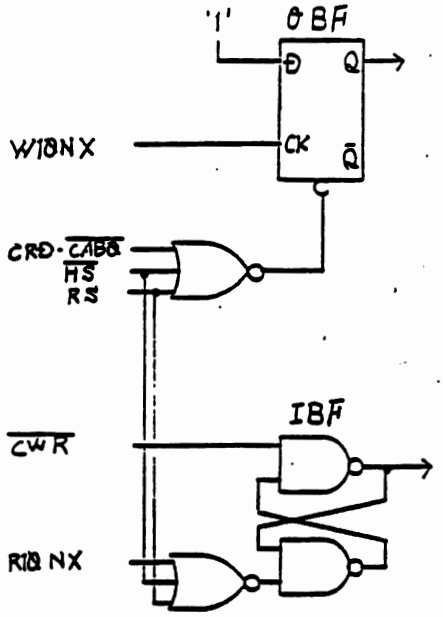


(The relation between $\overline{CSIO}$, AB3~0 and $\overline{CCS}$, CAB1, 0 is the same as write state on the left)

* Values depending on options. Max 330n when Z80 3.68 MHZ

(5) Flag

Set reset conditions of IBF (output buffer full flag) and IBF (input buffer full flag) are shown in the following figure.



WIONX .... Write pulse to address number 1Q. Negative pulse
RIONX .... Read pulse to address number 1Q. Negative pulse
HS .... HS 1 in any mode other than handsnake mode. Both OBF and IBF are reset.
CWR .... Write pulse from cartridge
CRD.CABQ.. Read pulse to address number Q from cartridge (CABQ-Q)

(6) Equipment address setting on CTG option side

In case of a option otner than HS mode option, it is necessary to set the equipment address of each option in CDB7 4 according to 13H Read made by the main part, after setting DB mode. As for IO mode and OT mode option, CDB7~4 are output ports. When 13H is read, the value is decided by pull-up or pull-down of CDB7~4. (Pull-up 1, Pull-down Q). On the main boad, however, CDB7~Q are all pulled down by 1MΩ. So, without any treatment, CDB7~Q will be all QQQQ. That is why it is necessary to treat the option pulling up or down with a resistance of about 100KΩ according to the equipment address.
Such is valid also for DB mode option. The address number 13H cannot be used as data input.

(2) Transmitter circuit (transmitter buffer, parallel-serial converter, parity generater)

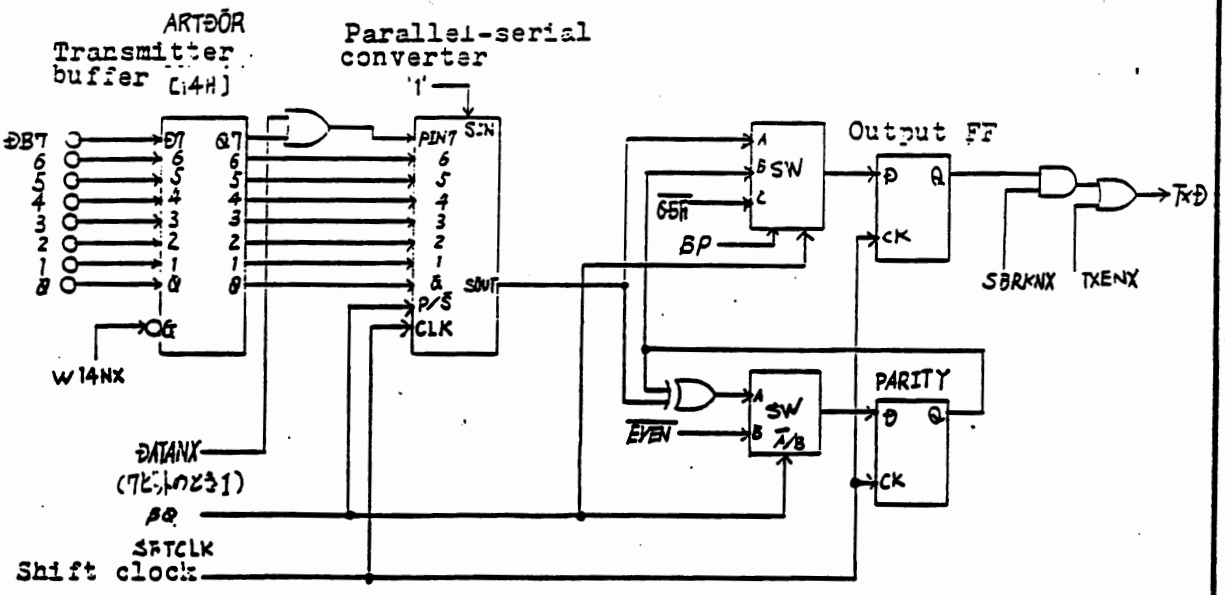


Figure 1

The transmitter circuit is composed of transmitter buffer (ARTDOR,14H), parallel-serial converter and parity generater. The transmitter is 8 bit ratch. Data is written in the buffer by written to 14H. It is necessary to confirm by checking TxRDY that the buffer is empty, before writing. When data is written in ARTDOR, TxRDY becomes Q, OBF becomes 1. Thus, if the bit counter is in BQ state, the transmission starts. If the bit counter is in a state other than BQ state,i.e. if it is transmitting precedent data, the buffer begins to transmit the data newly written only when the transmission of precedent data is ended and the bit counter enter BQ state.

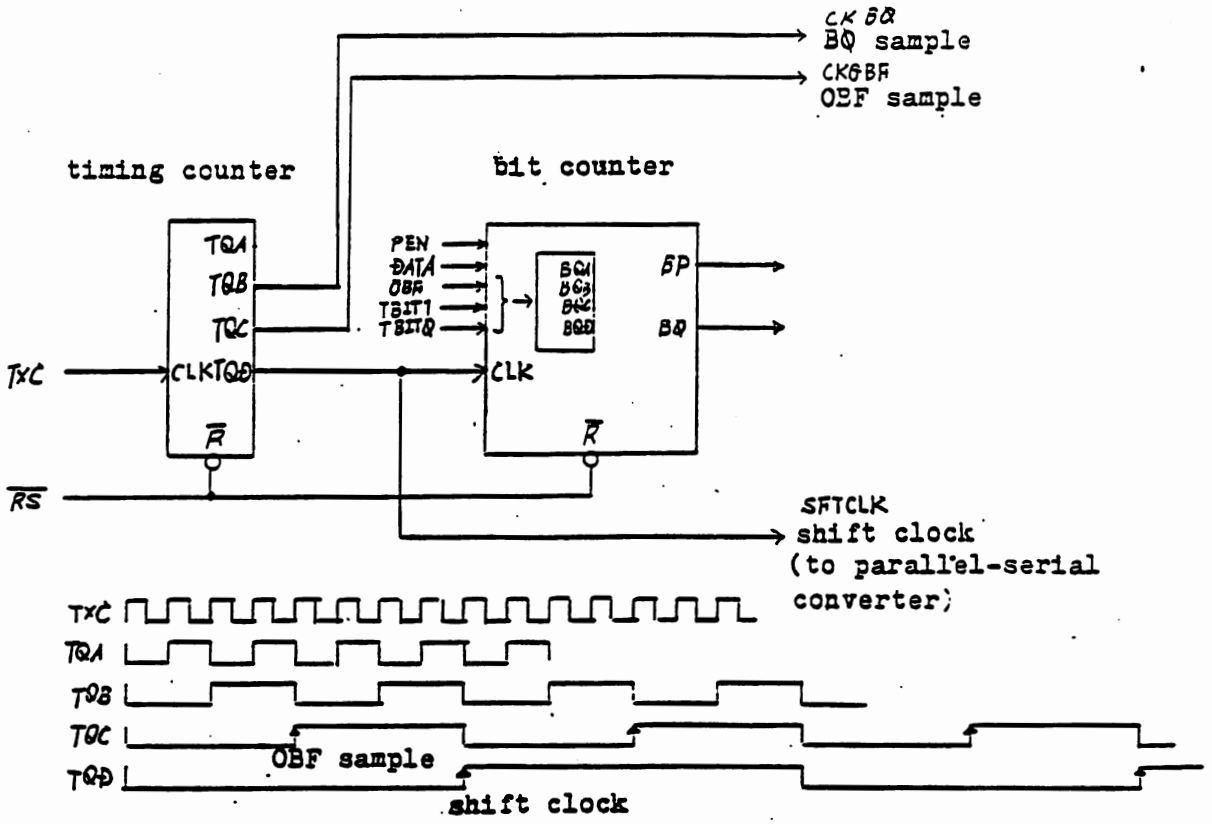
(A) First of all, the contents of ARTDOR are loaded in parallel-serial convert. The initial value is set in the parity generater and start bit (Q) is output from output FF. At this moment, TxRDY becomes 1, which means that a new data can be written to the transmitter buffer. In case that the data length is specified to be 7 bits, MSB of ARTDOR changes to 1 at the OR gate and is loaded to prallel-serial converter. The initial parity value is Q with even parity and 1 with odd parity (BQ→B1)

(B) When the next shift clock starts,parallel-serial converter will be shifted and the SOUT value (DQ) is output from output FF. In the parity generater, the initial parity value (DQ) is calculated (B1→B2)

(C) D1, D2, D3, D4, D5, D6 and D7 will be shifted out one after another (untill D6 in case of 7 bits), at the same time initial parity value⊕DQ⊕ D1⊕D2⊕D3⊕D4.... D7 is calculated in the parity generater. Parity bit means the result of this calculation.

(3) Transmitter control circuit (timing counter, bit counter)

図2



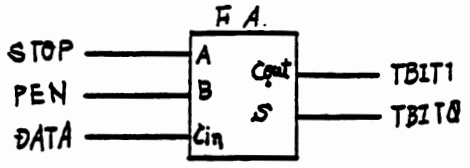
The timing conter is used to generate timing signals which serve to control each section of the transmitter part and is 4 bits hexadecimal free running counter. This counter is also reset by a reset. The clock signal which is 16 tinmes quicker than the baud rate is suppied to TXC. The baud rate is generated in the counter and is output as MSB output (TQD). This baudrate signal serves as standard clock for the transmission (shift clock for the parallel-serial converter). The role of the bit counter is to count transmission bit. It is renewed every 1 bit shift-out. This counter is composed of 4 bits FF, but not free running counter like the timing counter. It counts from (0000) to (Total transmission bit number -1) and returns to 0. For example, let's think of a unit of transmission bits whose components are; data length 8, parity present stop bit 2. The total bit number is ; start (1) + Data (8)+ Parity (1)+ Stop(2)= 12 bits. In this case, the counter counts up till (1011) and return back (0000). When the counter has no transmission data, it remains (0000) even if the clock signal arrives at it. It starts counting up just when data is written to ARTDOR from the main part. i.e. a(0000) state created by a reset input till when data will will be written in ARTDOR. From now on, we'll use an abbreviation like the following example, (0000): B0, (0001): B1, (1011): B11. Three distinct signals (OBF, TBIT1, TBITQ) serve to control the up-date of the bit counter. OBF (output buffer full) is the signal that indicates the presence of data to be transmitted within the transmitter buffer (ARTDOR). Every time a transmitter is over and the bit counter returns back to B0, OBF is checked If OBF=1, transmissions continue. If OBF=0, BQ remains till OBQ turns to 1. TBIT1 and TBIT0 are the signals that indicate the total transmission bit number. These signals control the return timing to B0 after transmitting how many bits.

☐ Relation between mode register values and total transmission bit number

STOP (Stop bit number)	PEN (Parity)	DATA (Data length)	Total bit number	TBIT1	TBIT0
0 (1)	0	0 (7)	9	0	0
0 (1)	0	1 (8)	10	0	1
0 (1)	1	0 (7)	10	0	1
0 (1)	1	1 (8)	11	1	0
1 (2)	0	0 (7)	10	0	1
1 (2)	0	1 (8)	11	1	0
1 (2)	1	0 (7)	11	1	0
1 (2)	1	1 (8)	12	1	1

TBIT1 and TBIT0 can tell how many 1 numbers are there among STOP, PEN and DATA indicating it in binary scale (Full Adder).

$$\begin{cases} TBIT\,1 = STOP \cdot PEN + DATA \cdot \overline{STOP} + DATA \cdot PEN \\ TBIT\,0 = STOP \oplus PEN \oplus DATA \end{cases}$$



That is; TBIT1 and TBIT0 occupy the lower two bits of (total bit number -1). i.e. the bit counter increase from (0,0,0,0) to (1,0,TBIT1,TBIT0) and return back to (0,0,0,0).

☐ Relation between mode register value and parity output timing (Refer to figure-4, too)

PEN	DATA	Parity output
0	0	Nothing
0	1	Nothing
1	0	B9
1	1	B10

As serial output TXD is delayed of one stage by FF, the output timing BP is;

$$BP = PEN \cdot (\overline{DATA} \cdot B8 + DATA \cdot B9)$$
$$= PEN \cdot Q_D \cdot \overline{Q_B} \cdot (\overline{DATA} \cdot \overline{Q_A} + DATA \cdot Q_A)$$

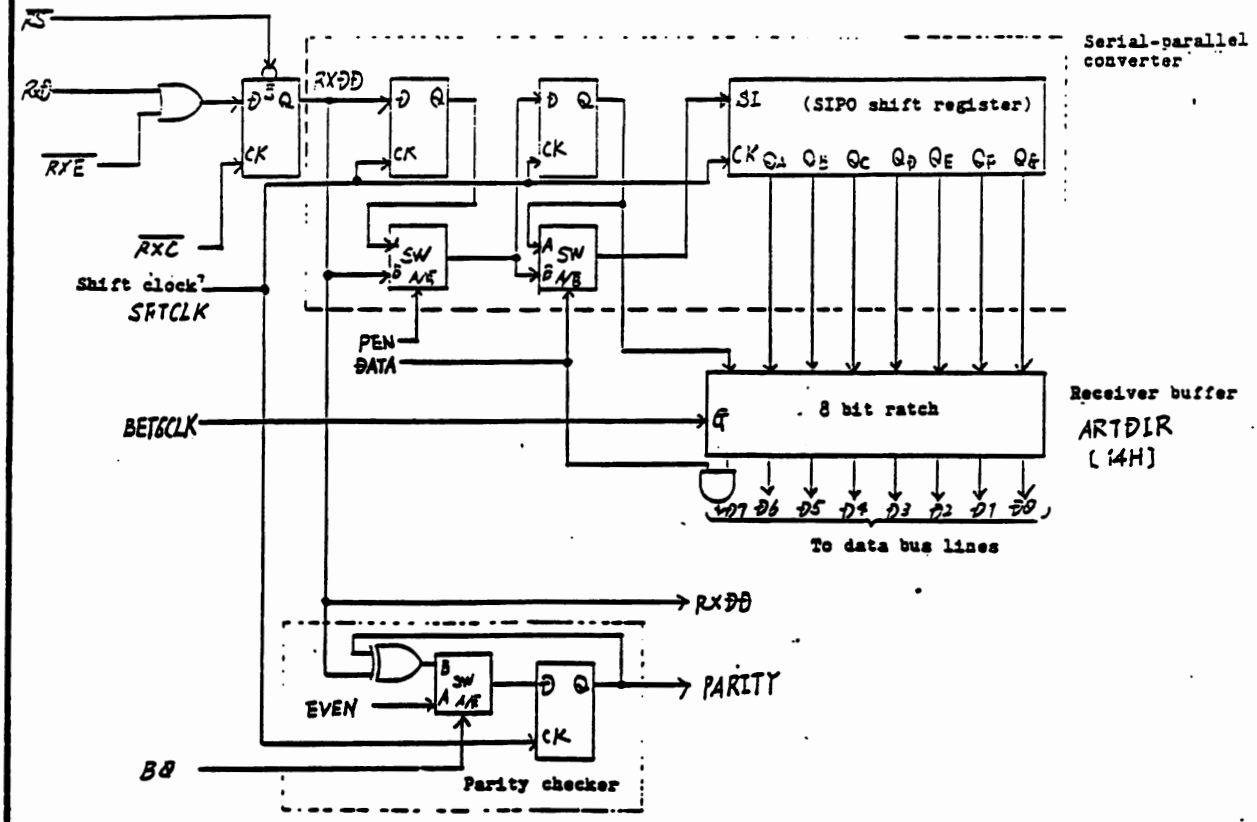
Transmission timing in each mode

Mode / Bit counter		(9)	(10)	(10)	(11)	(11)	(11)	(11)	(12)
Mode	STOP	0	0	0	0	1	1	1	1
	PEN	0	0	1	1	0	0	1	1
Bit counter	DATA	0	1	0	1	0	1	0	1
B0		Stop	Stop	Stop	Stop	Stop	Stop	Stop	Stop
B1		Start	Start	Start	Start	Start	Start	Start	Start
B2		D0	D0	D0	D0	D0	D0	D0	D0
B3		D1	D1	D1	D1	D1	D1	D1	D1
B4		D2	D2	D2	D2	D2	D2	D2	D2
B5		D3	D3	D3	D3	D3	D3	D3	D3
B6		D4	D4	D4	D4	D4	D4	D4	D4
B7		D5	D5	D5	D5	D5	D5	D5	D5
B8		D6	D6	D6	D6	D6	D6	D6	D6
B9			D7	P	D7	Stop	D7	P	D7
B10					P		Stop	Stop	P
B11									Stop

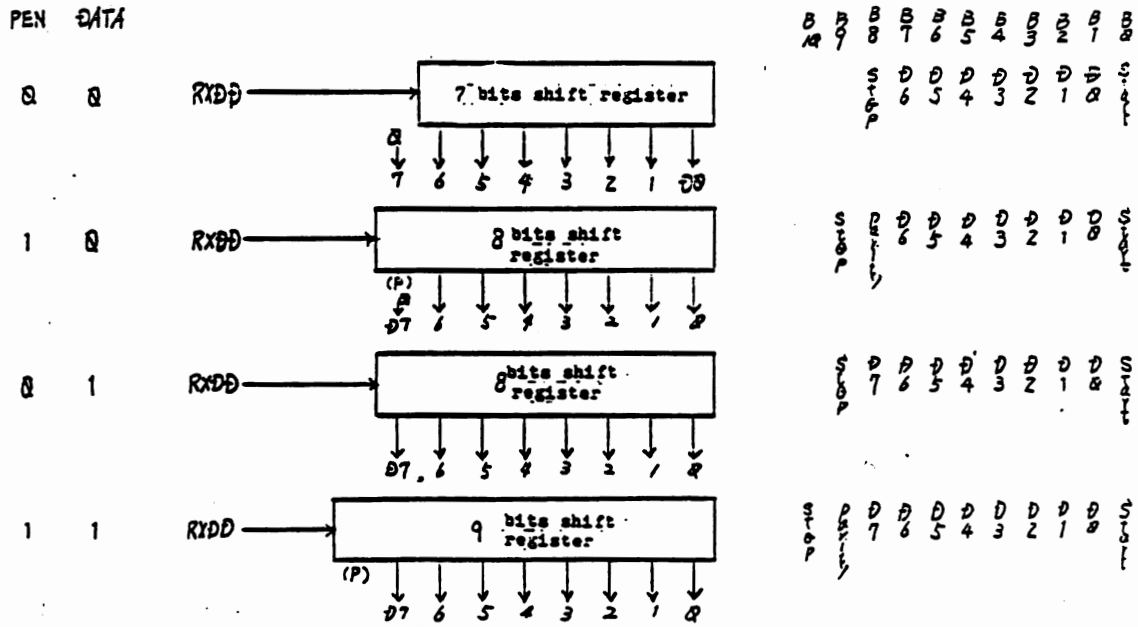
Start ... start bit
Stop .... stop bit
D0 7 .... data
P .... parity

Figure -4

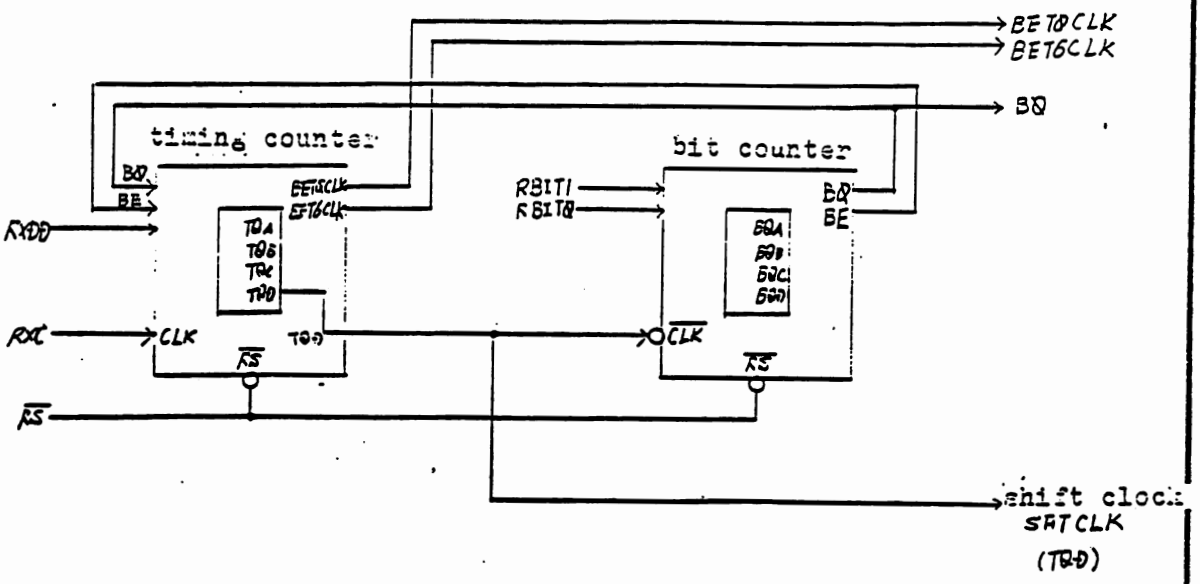
(5) Receiver circuit (Serial-parallel converter, Parity checker and Receiver buffer).



(Serial-parallel converter)



(6) Receiver control circuit (timing counter , bit counter)



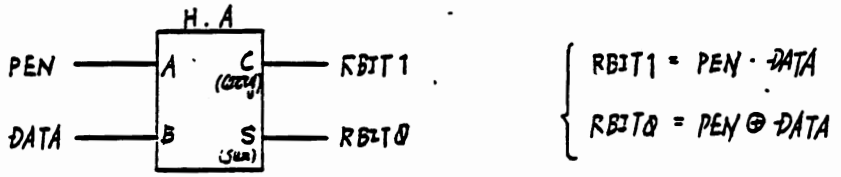
Timing counter inspects a start bit of receiver data and makes a center timing signal for data sampling. If receiving data becomes Ø by noise, after half a bit, it checks a start bit once again and it has function to ignore a illegal startbit. Further, it makes necessary timing signal at other receiver parts. Timing counter is made of 4 pieces of FF and generally it returns to Ø after counting Ø~15 . (but exept start bit, stop bit). Accordingly, TQ of MSB output becomes baud rate. Bit counter is a counter to count receiving bits of received data and it counts up at TQ output start of timing counter. Starting up of TQ becomes a center of bit and then it becomes a shift clock of se-pa converter. Bit counter is made of 4 pieces FF and it counts up from Ø every starting down of TQ and when it amounts to (total receiving bits-1), it returns to Ø. Before structure of receiver control is explained, it is described about total number of receiving bits. Originally, total number of received bits means (start bit 1) + (data, 7 or 8) + (parity bit, 0 or 1) + (stop bit, 1 or 2) but here above formula. That is , in case of stop bit = 1 or 2, it is always considered as 1 and therefore in case of stop bit 2, the 2nd bit is ignored. Receiver control circuit works on the premise that stop bit is always 1. Framing error is checked at the first stop bit only and then it enters to the mode to wait the start bit of next data. Here, the stop bit of the 2nd bit is ignored and then can be synchronized by the start bit of next data and it is received correctly.Thus, if the stop bit is considered as 1, the received action works correctly and the circuit become simple in this way.
RBIT1, RBIT0, input to bit counter means total bits number as the above and it decides the timing that the bit counter returns to Ø. RBIT1,Ø is calculated by PEN, DATA of mode register and it becomes like Table 5. Hereafter, it is expresse as BØ when the bit counter is Ø and then it's expressed as the B1 ....B1Ø. Timing counter also is expressed as the TØ, T1 .... T15.

☐ Relation between register and total received bit number

Figure -5

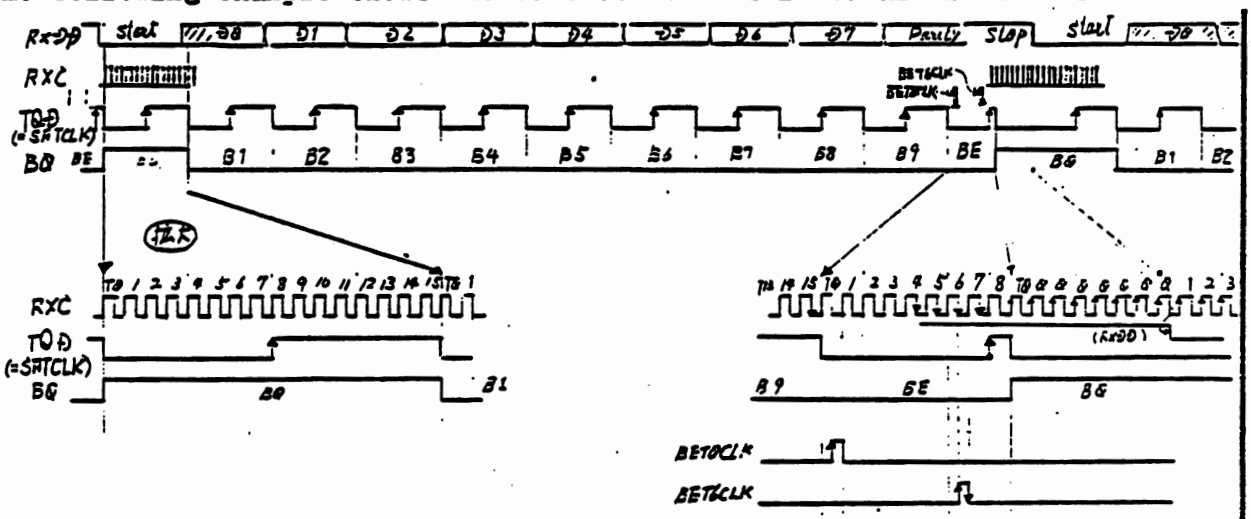
PEN	DATA	Bit number	RBIT1	RBIT0
0	0 (7)	9	0	0
0	1 (8)	10	0	1
1	0 (7)	10	0	1
1	1 (8)	11	1	0

RBIT1 and RBIT0 are calculated through HA (Half Adder). Notice that (1, 0, RBIT1, RBIT0) is a binary scale of (total bit number -1).

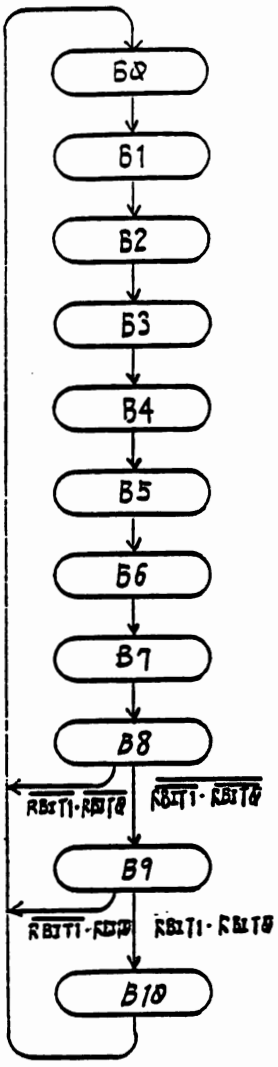


☐ Timing signals transmitted by the timing and bit counter (SFTCLK, B0, BET0CLK, BET6CLK)

※ The following example shows the case of 11 bits in total bit number.



Structure of the bit counter



Data input of each FF which composes the bit counter can be found on this chart

$$\begin{cases} D_A = \overline{Q_A} \cdot \overline{BE} \\ D_B = (Q_A \oplus Q_B) \cdot \overline{BE} \\ D_C = (Q_A \cdot Q_B \oplus Q_C) \cdot \overline{BE} \\ D_D = (Q_A \cdot Q_B \cdot Q_C \oplus Q_D) \cdot \overline{BE} \end{cases}$$

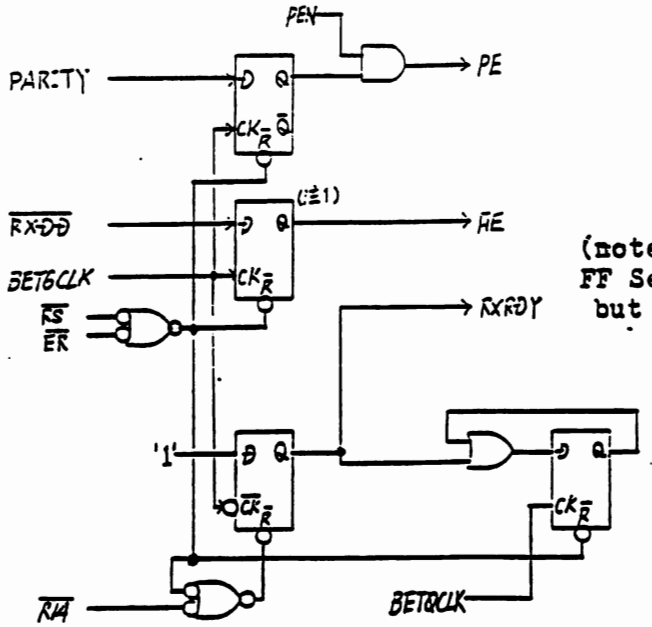
---Asynchronous structure permitted; $DC = QA \cdot QB \oplus QC$

上式において

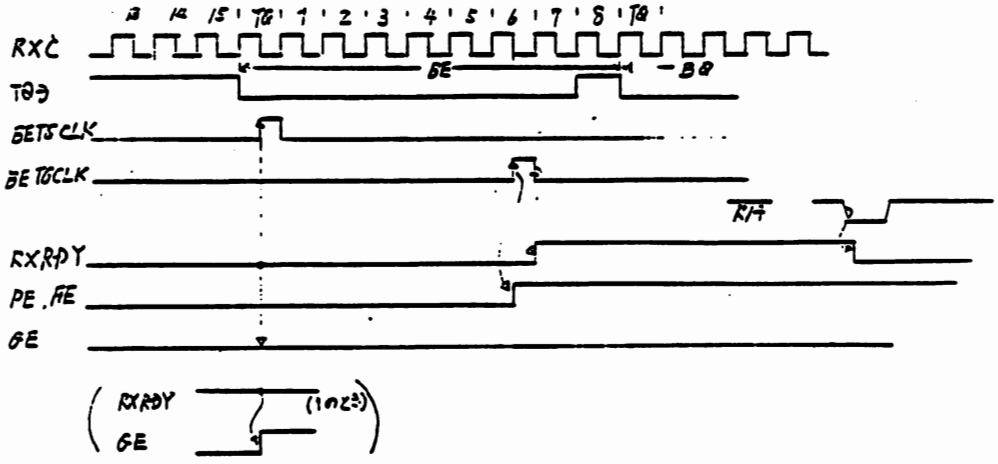
$$BE = (\overline{Q_A \cdot RBIT0}) \cdot (\overline{Q_B \cdot RBIT1}) \cdot Q_D$$

Figure -7

(7) Receiver control flag (RXRDY,FE,OE,PE)



(note 1)
FF Set-up and Hold of FE is not assured but it makes no difference.



All the flags of FE, PE, OE and RXRDY can be reset by a reset input or ER (error reset) command.
When1byte data is input, parity error and framing error are checked according to the T6 center timing of the end cycle of the bit counter BE. (It is with this timing that the data is taken in the receiver buffer). RXRDY is reset according to the T6 end timing.
This lag of set timings between PE,FE and RXRDY is designed intentionally in order that FE and OE values be guaranteed when RXRDY=1. If they are set at the same time, a race will be produced between them. CPU reads ARTDIR of 14H after having confirmed that RXRDY=1. RXRDY is reset by this. In case that the receiver buffer ARTDIR is not read since RXRDY passes to 1 by the time when the stop bit of the next data will be input, a overrun error flag is to be set. FE and PE are renewed every time data is received while OE, once set, is not reset until ER command reacnes it.

4.Specifications of Gate-Array devices

(1) DC specifications

(2) Logic circuit diagram

(3) Seal diagram

(4) Outword form design

(5) Pins disposition diagram

DC characteristic

VDD=4.0～6.3V, VSS=0V
TOP=0～70°C

ITEM		SIMBOL	CONDITION	STANDARD			UNIT
				MIN	AVERAGE	MAX	
POWER CURRENT		IDDS	note 3 STATIC STATE	0		0.01	mA
OUTPUT TENSION	H LEVEL	VOH	mA IOH=-0.4	3.7		VDD	V
	L LEVEL	VOL	IOL=2mA	VSS		0.4	V
INPUT TENSION	H LEVEL	VIH		2.6			V
	L LEVEL	VIL				0.7	V
INPUT LEAK CURRENT		ILI	VI= 0V～VDD	-10		10	μA
INPUT LEAK CURRENT		ILZ		-10		10	μA

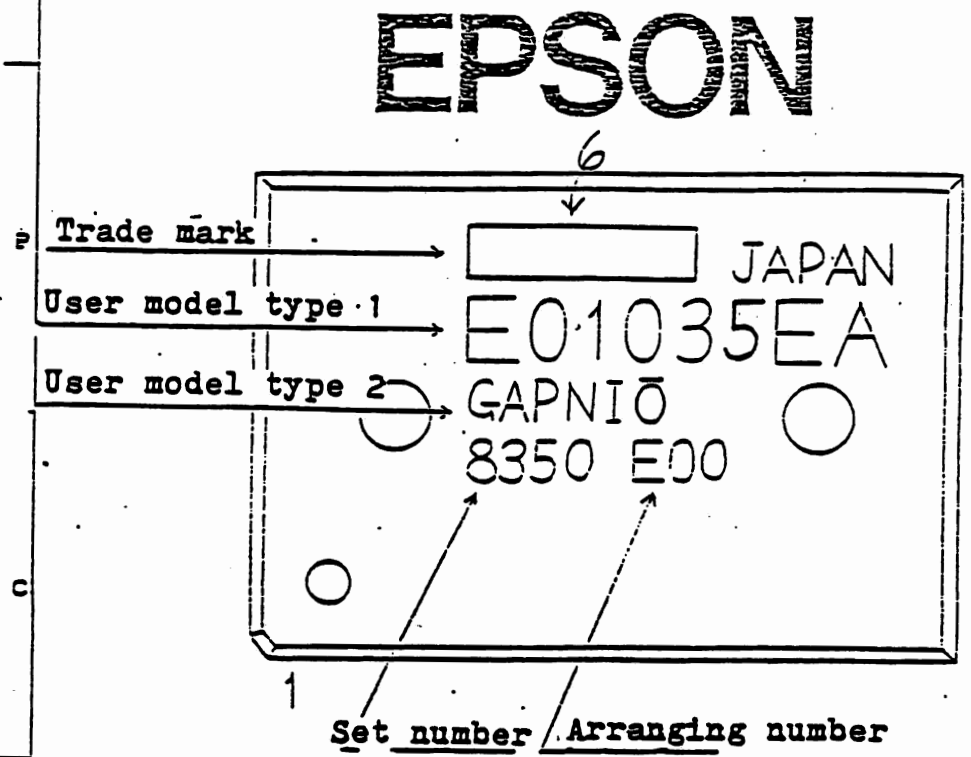
note 3: VIH VDD-0.3V, VIL=VSS 0.3V
On the condition that TOP=0~50°C

note 4: In case of try-state input.

(4-2) Logic circuit diagram

Annexed design (MB62H114 Logic circuit diagram DRAW DATE 830526)
23rd June 1983
EMISSION NUMBER 833049

Seal format diagram for MB62H SERIES (EPSON)



F64 / 80ピン

1. Trade mark : Height 1.5mm
2. User model type 1 : Height 1.2mm Round gothic type
3. User model type 2 : Height 1.2mm Round gothic type
4. Other character : Height 1.2mm Round gothic type

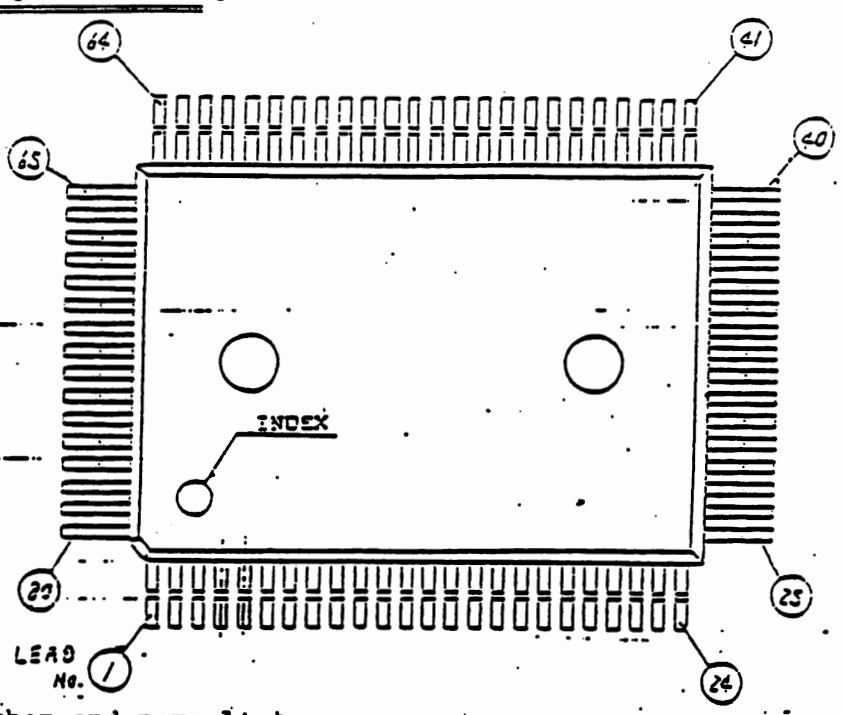
Model type	User model type 1	User model type 2
MB62H113	E01033EA	GAPNIT
MB62H113	E01034EA	GAPNDL
MB62H113	E01035EA	GAPNIO

(4-5) Pins disposition diagram

MB62H114 (FPT-80)

GAPNIŌ

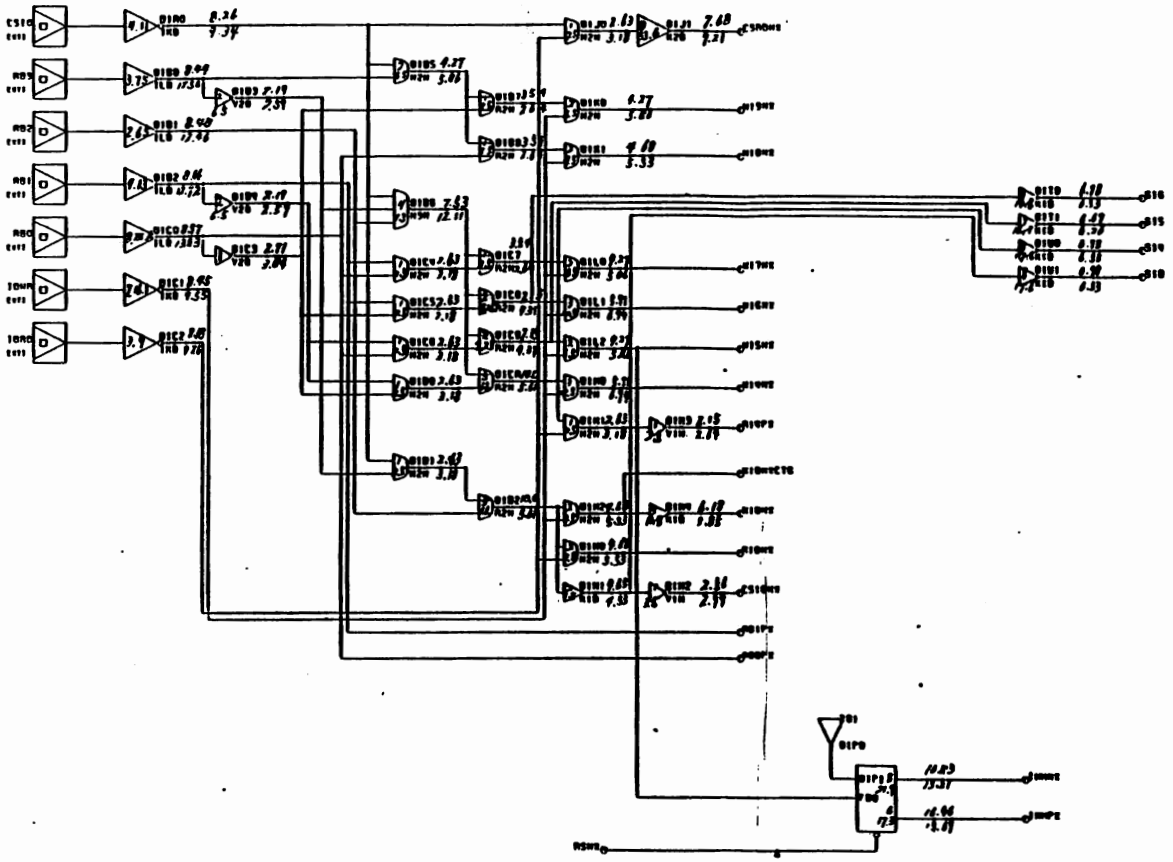
Pins disposition diagram



Pin number and name list

PIN No.	I/O	Name	PIN No.	I/O	Name	PIN No.	I/O	Name	PIN No.	I/O	Name
1	I	RCTS	21	I	CSIŌ	41	O	RRĐY	61	O	CRS
2	—	N.C	22	I	TXC	42	O	PĐB7	62	I/O	CCS
3	—	N.C	23	/	N.C	43	O	PĐB3	63	/	N.C
4	O	STXĐ	24	I	RXC	44	O	PĐB0	64	O	CITO
5	—	N.C	25	I/O	ĐB5	45	O	PST3	65	I/O	C
6	O	CTXE	26	I/O	ĐB2	46	O	FINI	66	I/O	CRĐ
7	—	N.C	27	I/O	ĐB3	47	O	PDB2	67	I/O	CĐB4
8	—	N.C	28	—	N.C	48	O	PĐB6	68	I	CAUĐ
9	I	RS	29	I/O	ĐB1	49	O	PĐB4	69	I/O	CĐB1
10	I	RĐSR	30	I/O	ĐB0	50	I	FERR	70	I/O	CAB1
11	O	SŌUT	31	I/O	ĐB6	51	I	FBSY	71	—	N.C
12	Power	VSS	32	I/O	ĐB7	52	Power	VSS	72	I/O	CĐB7
13	I	CEN	33	Power	VDD	53	I/O	CĐB3	73	Power	VDD
14	O	SP	34	I/O	ĐB4	54	I/O	CWR	74	I	SIN
15	O	LEĐ0	35	I	AB1	55	I/O	CĐB6	75	I	RCĐ
16	O	LEĐ2	36	I	AB0	56	I/O	CĐB5	76	I	SRXĐ
17	—	N.C	37	O	PĐB7	57	I	CRXĐ	77	O	RĐTR
18	O	LEĐ1	38	O	PĐB1	58	I/O	CĐB2	78	O	RRTS
19	I	IŌRĐ	39	I	AE3	59	I	CSEL	79	I	RRXĐ
20	I	IŌWR	40	I	AB2	60	I/O	CAB0	80	O	RTXĐ

ENĐ



*ABOP3	05	/A2	*WIONE	05	/B2		
*ABIP3	05	/A2	*WIOWEC16	05	/B2		
*CSIONE	05	/A2	*WIWRE	03	/B2		
*CSIOWE	05	/A2		03	/B2		
*INWRE	02	/C3		02	/C8		
*INWP3	03	/C3	*WISRE	02	/C8		
*RSWE	03	/C3	*WISWE	02	/C7		
	04	/C11	*WIERE	02	/C8		
	03	/C2	*WIEWE	02	/C7		

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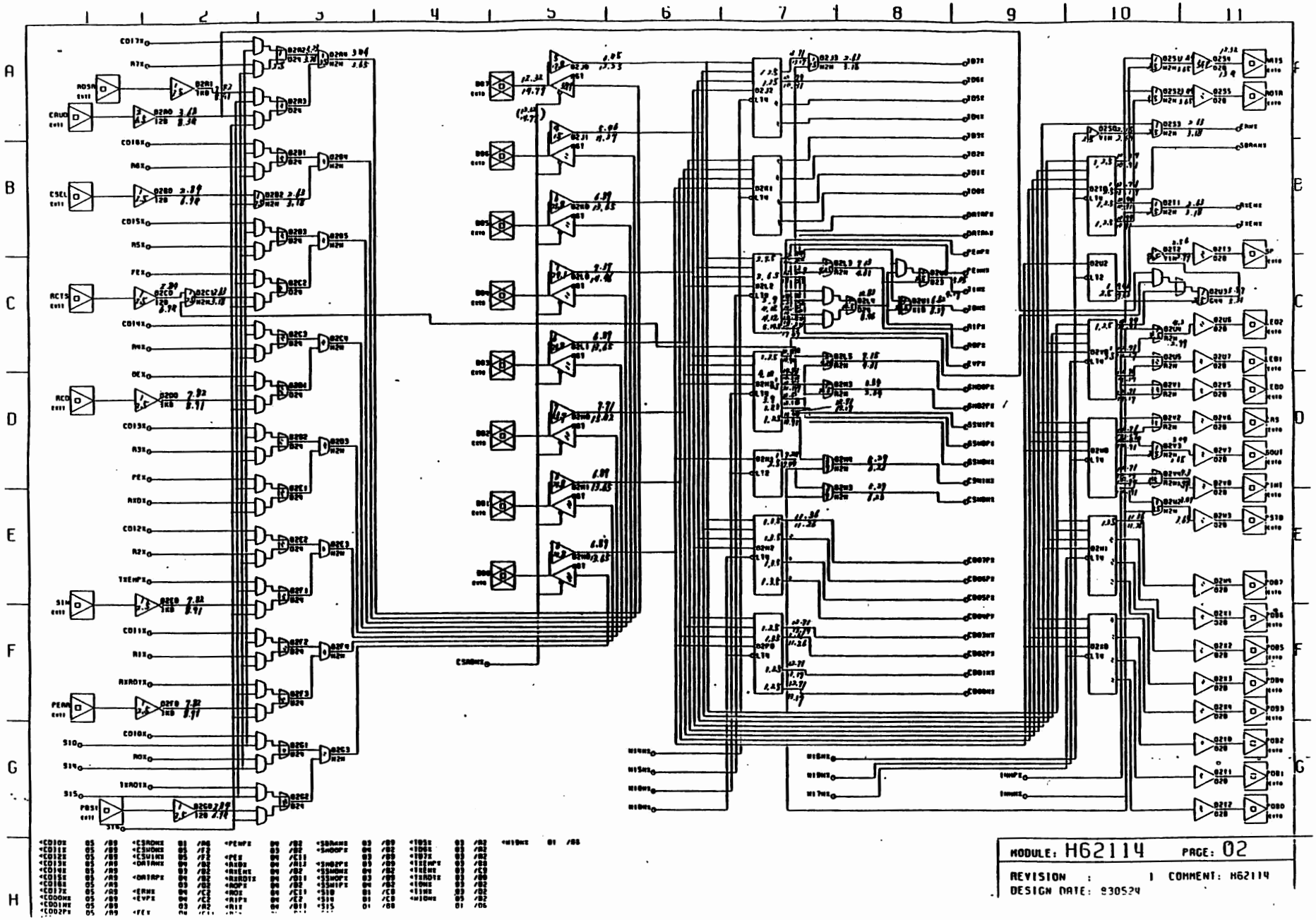
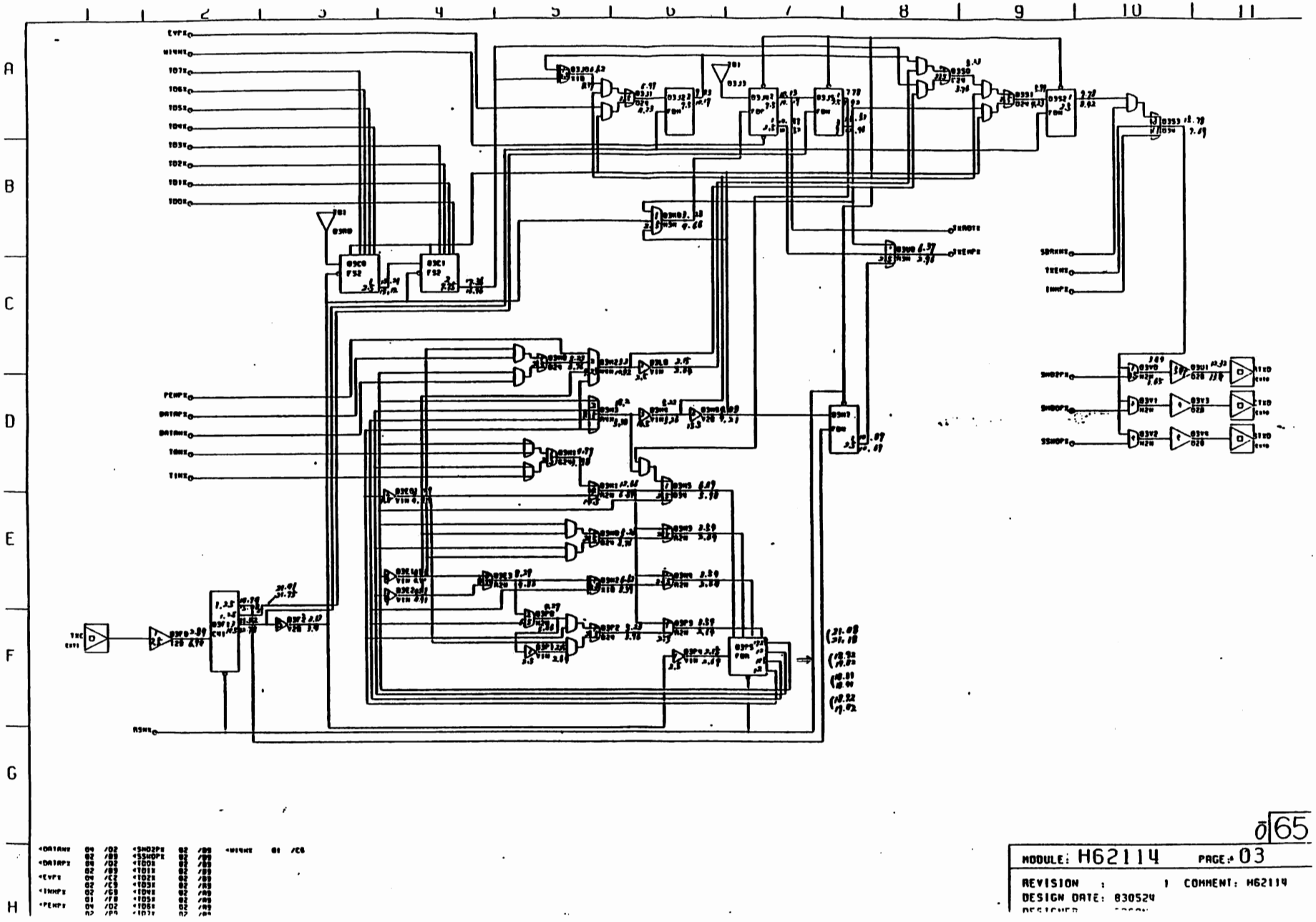
REVISION :	COMMENT: H62114
DESIGN DATE: 830524	
DESIGNER : EPSON	

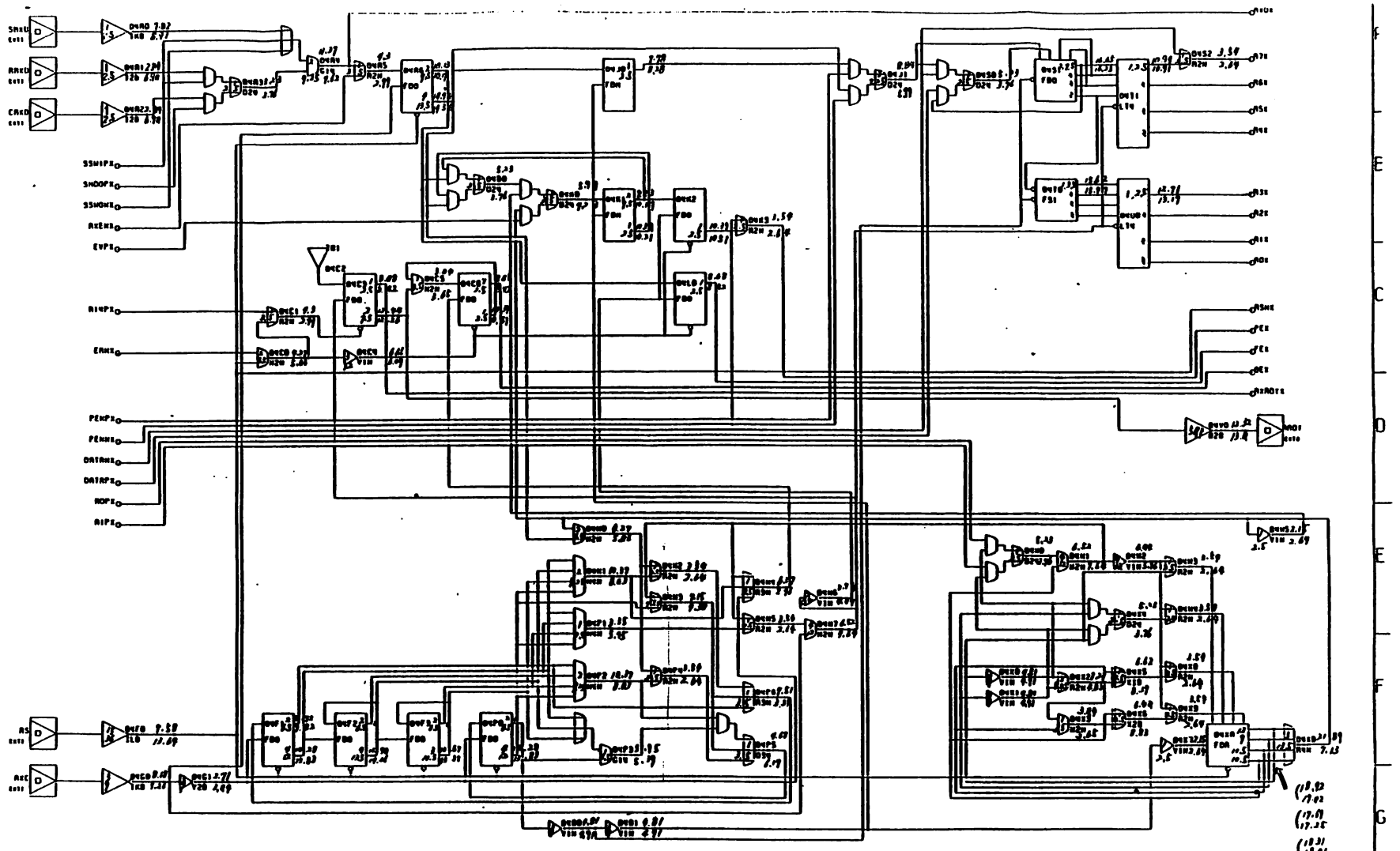


MODULE: H62114 PAGE: 02

REVISION : 1 COMMENT: H62114

DESIGN DATE: 930524





*DATAMX	03	/D2	*AXDX	02	/E0	*33MDMX	02 /D0
*DATAPX	03	/D2	*AXEMX	02	/E1	*SSWIPX	02 /D0
			*AXRADIX	02	/F2		
*ERMX	02	/D0	*AOPX	02	/E0		
*LVPX	03	/D2	*MOX	02	/E2		
			*AIPX	02	/E0		
*FEX	02	/C2	*AIX	02	/F2		
*DEX	02	/C2	*AIWPX	03	/D6		
*PENMX	02	/C2	*AZX	02	/E2		
*PENPX	03	/D2	*A3X	02	/D2		
	02	/D0	*AWX	02	/C2		
*PEX	02	/D2	*A5X	02	/D2		
*RSWX	05	/C2	*A6X	02	/D2		
	03	/C2	*A7X	02	/E2		
	01	/F5	*SHOOPX	03	/D9		
				02	/D9		

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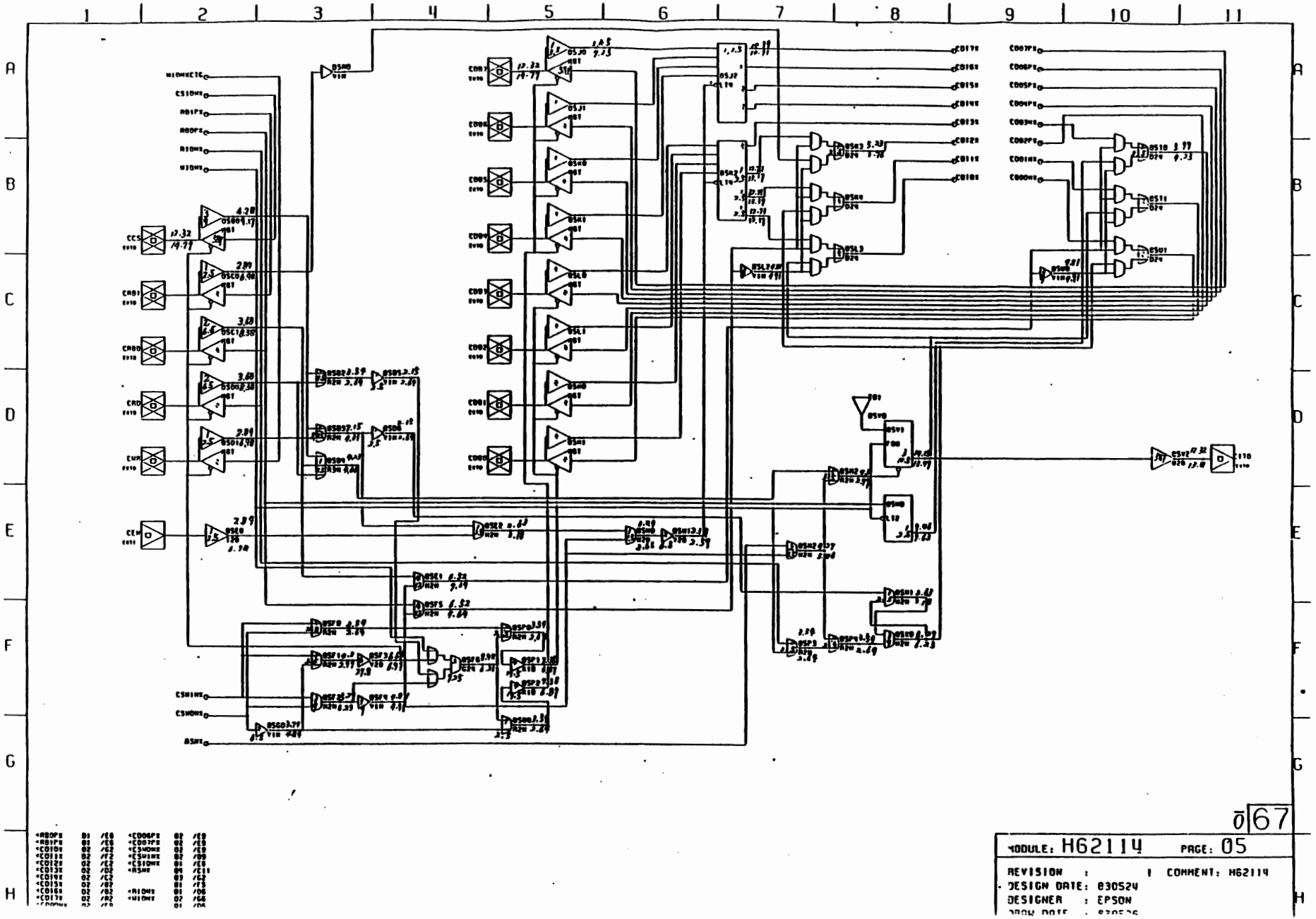
DESIGNER : EPSON	
DRAW DATE : 830526	
DRAWER : FUJITSU	



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DESIGN DATE: 830524

DESIGNER : EPSON

PINE OPTIONAL CARTRIDGE

Universal Cartridge Specifications Booklet

1. Applications

This specifications booklet is to be used for the universal cartridge which is an optional cartridge for the Pine.

Contents

2. Outline

The Universal Cartridge is a multi-purpose cartridge for use with the Pine. Through use of this cartridge the user free to install other electronic equipment. This cartridge is to be used for creating trial versions of optional cartridges according to wiring arrangements.
This specifications booklet specifies the necessary interfaces with the Pine mainframe and exterior dimensions when the Universal Cartridge is being used.

3. Connector Pin Arrangement

(?) Nihon Koku Denshi Sei PICL30S-LT

1	GND	+/-5V ground	16	+5V	+5V power supply
2	CAUD	Audio input	17	CG	Case ground
3	NDB4	Data bus no. 4	18	CDB1	Data bus no. 1
4	CDB4	Read signal	19	CG	Case ground
5	CDB0	Data bus no. 0	20	CAB1	Address bus no. 1
6	CITO	Interrupt signal	21	FPOF	Overcurrent detection
7	CCS	Chip select			
8	CRS	Cartridge reset	22	CDB7	Data bus no. 7
9	CAB0	Address bus no. 0	23	CDB3	Data bus no. 3
10	CSEL	Mode select input	24	CEN	6301 EN signal
11	GND	VB1 ground	25	CWR	Write signal
12	CDB2	Data bus no. 2	26	CTXD	Serial receiving line
13	VB1	Non-stabilized power supply	27	CDB6	Data bus no. 6
14	CRXD	Serial transmission line	28	RS	Hardware reset
			29	CDB5	Data bus no. 5
15	-5V	-5V power supply	30	VB2	Backup power supply

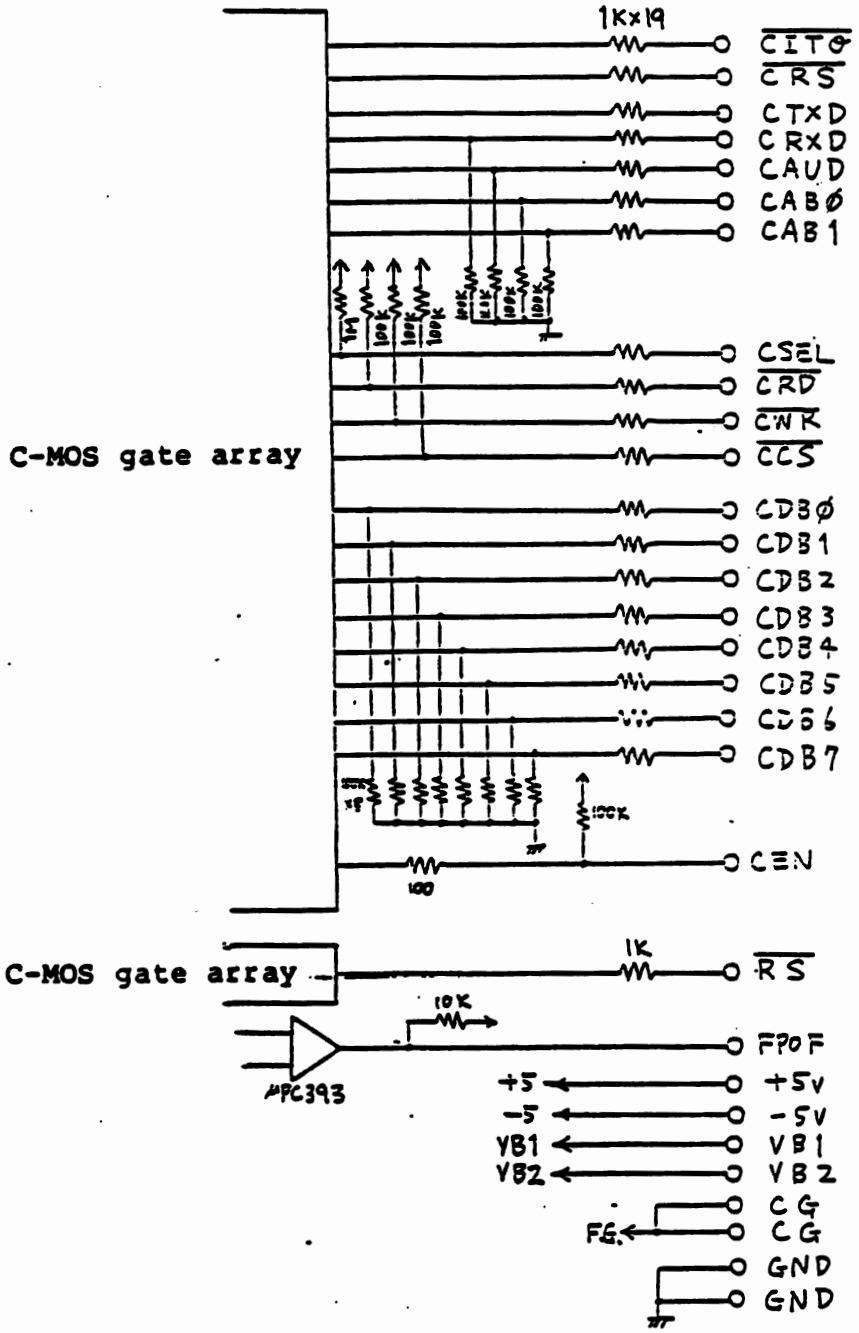
4. Explanations of Various Pins

GND:	Pin 1	This is the +/-5V ground.
CAUD:	Pin 2	This is digital audio signal output which is connected to a piezoelectric beeper. It can be used for general purpose output and can be used for reading as bit 7 of I/O Port 16H.
CDB0:	Pin 5	When in the Hand Shake mode (will be referred to as HS mode) these function as data bus input output on the cartridge side. When in the Data Bus mode (will be referred to as DB mode) will function as data bus input output for mainframe side. When in the Output mode (will be referred to as OT mode) will function as input for 8 bit port input. When in the Input output mode (will be referred to as IO mode) CDB 7 - 4 will function as input ports and CDB 3 - 0 as output ports.
" 1:	18	
" 2:	12	
" 3:	23	
" 4:	3	
" 5:	29	
" 6:	27	
" 7:	22	
$\overline{\text{CRD}}$:	Pin 4	Outputs read pulse to the mainframe when in the HS mode. Inputs read pulse from mainframe when in DB mode.
$\overline{\text{CITO}}$:	Pin 6	This is only used in the HS mode. It becomes 0 when the mainframe outputs data or commands to the output buffer and transmits an interrupt request to the cartridge. It changes to 1 when data is read by the cartridge.
$\overline{\text{CCS}}$:	Pin 7	When in the HS mode, this is used for chip select output from the cartridge. When in the DB mode, this is used for chip select input to the cartridge. It is not used in the OT and IO modes.
$\overline{\text{CRS}}$:	Pin 8	This is responsible for preset input from the mainframe. By outputting data to bit 3 of I/O port 19H those values are output from the mainframe. This can also be used for general purpose input.

CAB0: Pin 9	When in the HS mode, this outputs the mainframe's address. When in the DB mode, this inputs the mainframes address. It is not used in the OT and IO modes.
CAB1: Pin 20	When in the HS mode, this is used for general purpose output from the mainframe. When the DB mode, this inputs the address from the mainframe. It is not used in the OT and IO modes.
CSEL: Pin 10	Used for output to the mainframe. Is 0 in the HS mode and 1 in all other modes. Can perform read as bit 6 of I/O Port 16H of the mainframe.
GND: Pin 11	Return ground for non-stabilized power supply VB1.
VB1: Pin 13	Non-stabilized power supply. Batteries or an AC adapter are connected directly. This is used when a large current is required. (4 - 7V)
CRXD: Pin 14	For serial data transmission line. Can also be used for general purpose output. This sets bits 2 and 3 of I/O Port 18H to 0 and reads from bit 3 of I/O Port 16H.
CTXD: Pin 26	Receiving line for serial data.
-5V: Pin 15	-5V power supply. Can handle up to approximately 30mA.
+5V: Pin 16	+5V power supply. Can handle up to approximately 70mA. (5V+/- 5%)
CG: Pins 17,19	This is for the case ground.
FPOF: Pin 21	Overcurrent detection input. For options uses which require large current, when this signal is 1, current levels must be reduced immediately.
CEN: Pin 24	This is used for E signal output when 6301 is used in the cartridge. At all other times it is pulled up.

$\overline{\text{CWR}}$:	Pin 25	When in the HS mode this is used for write pulse output to the mainframe. When in the DB mode, this is used for write pulse input from the mainframe.
$\overline{\text{RS}}$:	Pin 28	Simultaneous to being supplied to the CPU of the mainframe this is used for reset signal input.
VB2:	Pin 30	This is used for the backup power supply. Power is supplied from +5V when the mainframe's power supply is on and from batteries or an AC adapter when the power supply is off. When power supply is on, up to approximately 15mA can be supplied. When power supply is off, up to approximately 0.5mA can be supplied.

The diagram below shows the interface of the various signals in the mainframe's circuit board.



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5. Explanation of Modes

The cartridge interface can have up to 4 different modes depending on the types of optional equipment connected.

(1) HS Mode (Hand Shake Mode)
This is the CPU to CPU interface mode, used with optional equipment containing CPUs and is similar to the 8255 Hand Shake mode. It handles data through the input and output buffers. Control flags (IBF, OBF) are used for control during data transmission.

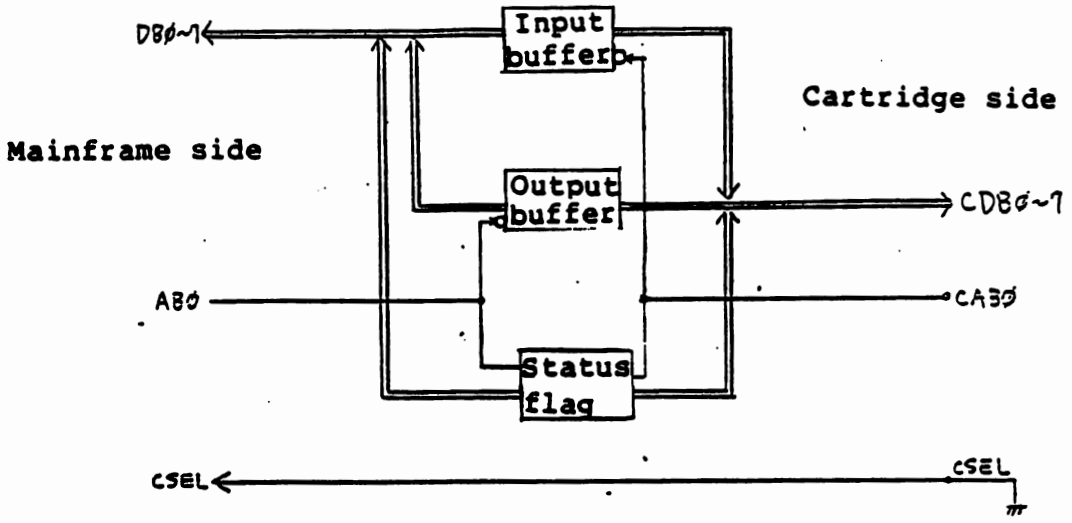
(2) DB Mode (Data Bus Mode)
This is the mode in which optional equipment is viewed by the mainframe as normal input output devices. Optional equipment is directly connected to the mainframe's data bus and is alloted an address area composed of I/O ports 10 - 13H.

(3) IO Mode (Input Output Mode)
This mode uses a 4 bit input port and 4 bit output port system.

(4) OT Mode (Output Mode)
In this mode an 8 bit output port system is used.

In the following section we will explain in detail the various modes.

5-1 HS Mode



When in the HS mode, the cartridge is interfaced to the mainframe through the input and output buffers. When the cartridge writes data to the output buffer, it is read by the mainframe which in turn writes data or commands to the input buffer which is then read by the cartridge. This hand shaking is carried out using the IBF and OBF status flags.
When the mainframe writes to the input buffer, if AB0 =1 it is a command and if AB0 = 0 it is data. AB0 values at this point are read into F0 of the status flags and can be detected through the status read on the cartridge side. When writing to the input buffer is carried out, IBF = 1 and CITO = 0, and an interrupt request is sent to the cartridge side. (Please note that IBF is reversed on the mainframe and cartridge sides. The names shown here are as seen from the cartridge side.)
When the presence of an interrupt (request) or status read notifies the cartridge side that the mainframe is writing to the buffer, it reads that data together with the F0. When the cartridge side reads from the input buffer, IBF returns to 0 and CITO returns to 1. When CAB0 = 0 the cartridge side can read data from the input buffer and when CAB0 = 1 it reads the status.

In addition, when the cartridge side writes to the output buffer, OBF = 1, the mainframe checks the values through status read and then reads the output buffer. When the output buffer is read OBF returns to 0. The mainframe is able to read the output buffer when AB0 = 0 the status flag when AB0 = 1. (Because the cartridge side does not distinguish between commands/data when writing to the output buffer, CAB0 = 0 is used.)
When in the HS mode, CAB1 can be used for general purpose output from the cartridge side and can also be used for reading as part of status function on the mainframe side.

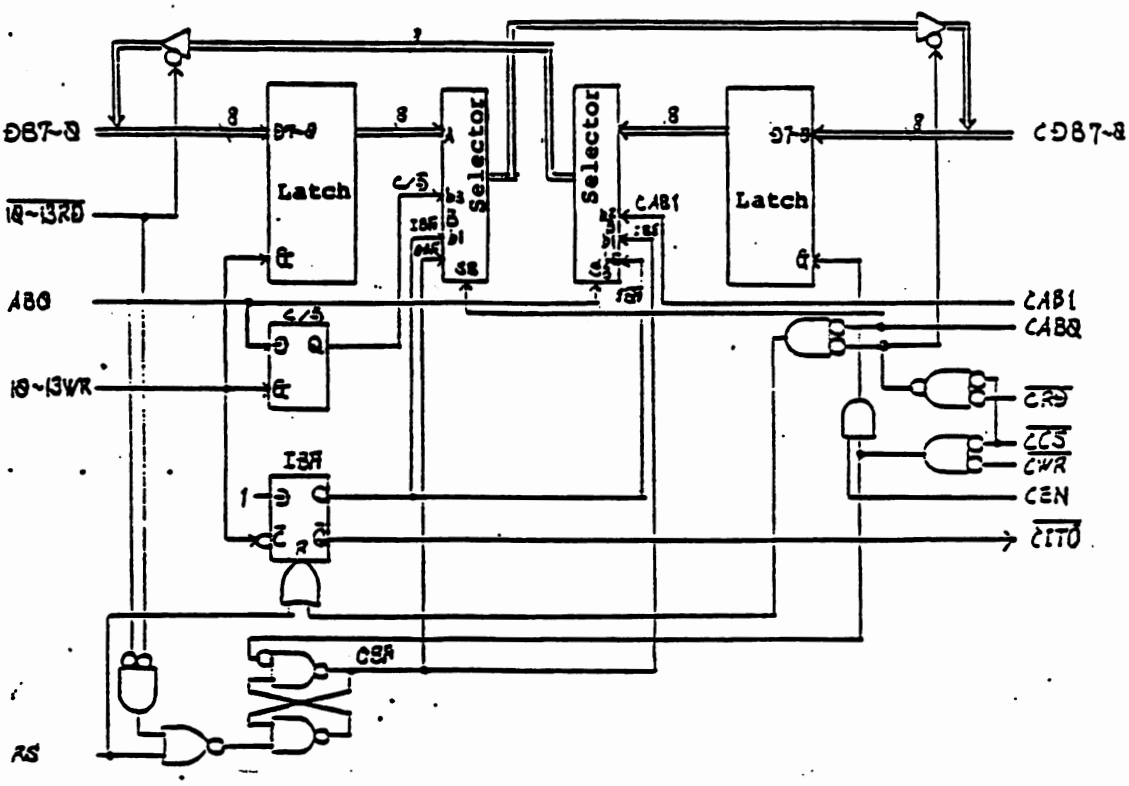
IO Address Space

R/W	CAB0	D7 6 5 4 3 2 1 0	
READ	0	8 bit input data	IFB=0, CITO=1
	1	\ \ F0 \ \ IBF OBF	
WRITE	0	8 bit data output	OBF=1
	1	Unused	

Address Area Mainframe Side

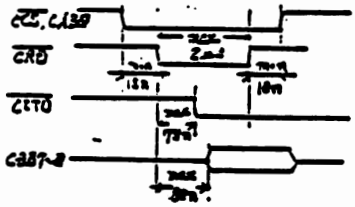
R/W	IO address	D7 6 5 4 3 2 1 0	
READ	10	8 bit output data	OBF=0
	11	\ CAB1 Mainframe IBF Mainframe OBF	
	12	Unused	
	13	"	
WRITE	10	8 bit input data	IBF=1, F0=0, CITO=0
	11	8 bit input commands	IBF=1, F0=1, CITO=0
	12	Unused	
	13	"	

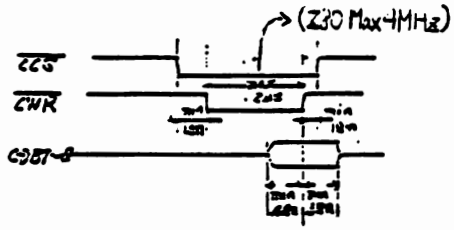
Illustration of Cartridge Interface Circuits and Timing Charts



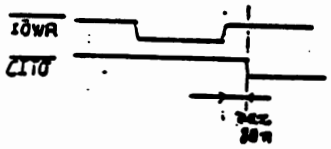
The OBF and IBF are shown as they would be seen on the cartridge side.

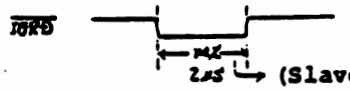
(Cartridge Option Side)





(CPU side)





(Slave 6301; less than 6MHz)

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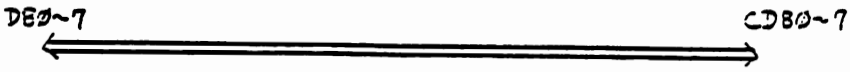
5-2 DB Mode

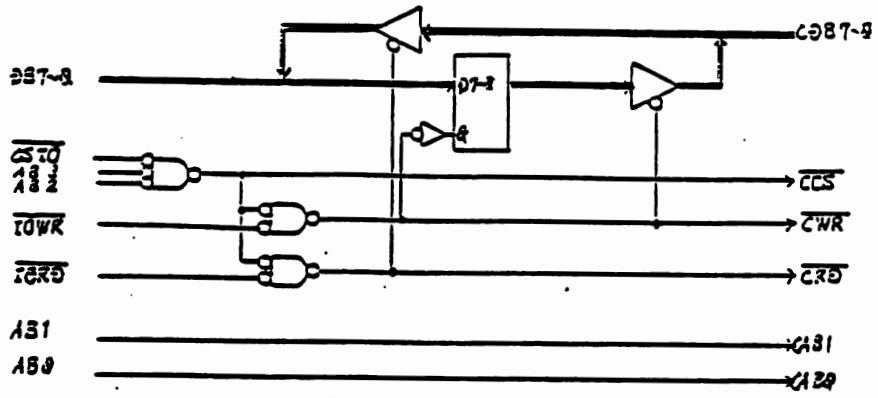


In the DB mode the cartridge is used as a normal I/O device and is viewed as a I/O device with a 4 address area by the mainframe. Therefore, CDB0 - 7 is directly connected to system devices 0 - 7 and, $\overline{CCS}$, $\overline{CRD}$, $\overline{CWR}$, CAB0 and CAB1 are all supplied from the mainframe. CCS is 0 for all mainframe I/O addresses 10 - 13H and CAV1 and $\overline{CAB0}$ correspond to the lower 2 bits of the address. $\overline{CRD}$ and $\overline{CWR}$ are the mainframe's I/O write pulses. At this time $\overline{CITO}$ is 1.
CSEL is 1 in DB mode.

I/O address space as viewed from mainframe side.

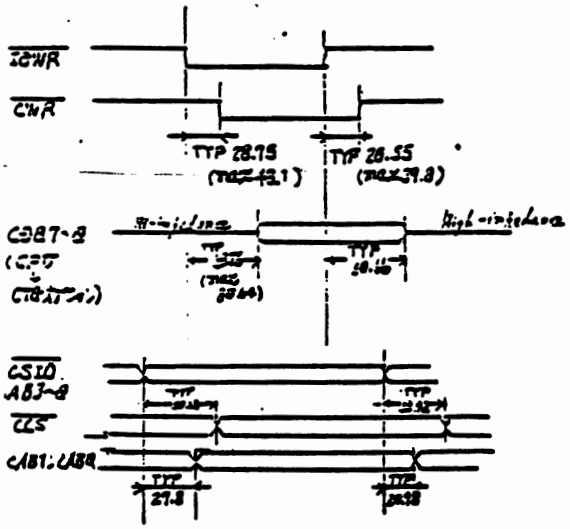
R/W	I/O address	D7 6 5 4 3 2 1 0
READ	10	
	11	
	12	
	13	Device address
WRITE	10	
	11	
	12	
	13	

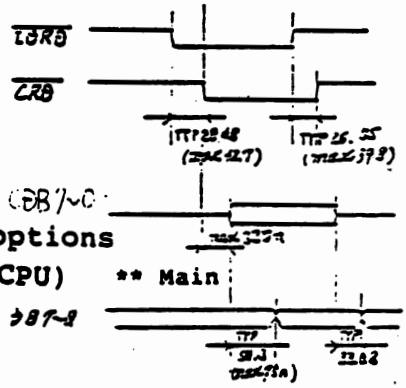
Illustration of Cartridge Interface Circuits and Timing Charts.



** CITO is high
** OBF and IBF are reset

AC characteristics





($\overline{CSIO}$, AB3 - 0 and $\overline{CCS}$, CAB1.0 are the same during write as shown to the left.)

** Values determined by options: when Z80 is 3.68MHz, maximum is 330m.

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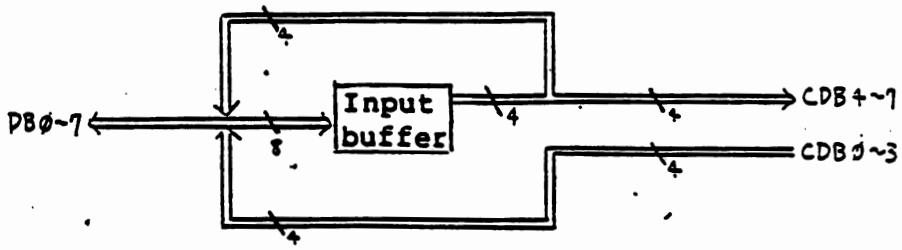
5-3 IO Mode



The IO mode is composed of 4 bit input ports, CDB4 - 7 and 4 bit output ports CDB0 - 3. The input side is composed of an 8 bit latch while the output side has no latch. Instead, values of pins CDB0 - 3 are output as they are. The IO address is 10H.

When the mainframe side writes to 10H, data in the data bus is written to the input buffer and the upper 4 bits enter CDB4 - 7.

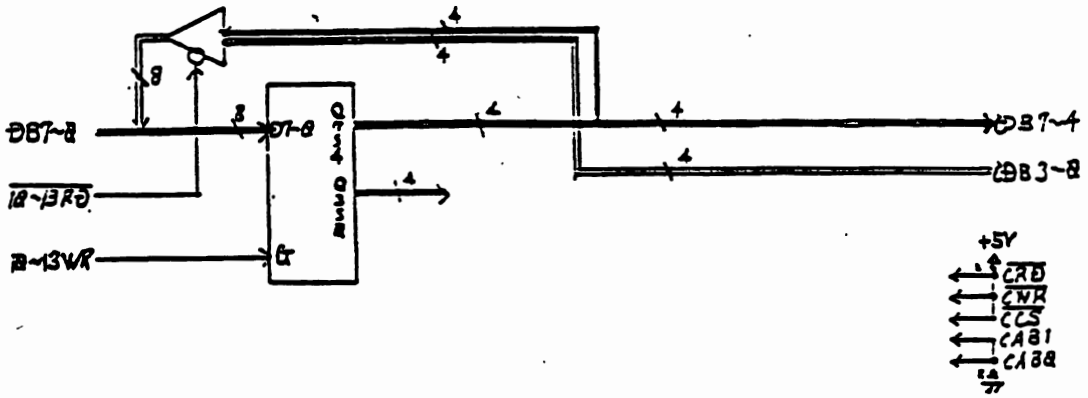
When the mainframe reads from 10H the values of pins CDB0 - 3 are output directly to the data bus lower 4 bits, DB0 - 3, and the upper 4 bits from the input buffer enter the upper 4 bits of DB4 - 7.

CSEL must be 1 in the IO mode. Also $\overline{CCS}$, $\overline{CRD}$, $\overline{CWR}$, CAB1 and CAB0 must be pulled up or down. $\overline{CITO}$ is 1 and no flags are used.

IO Address Base As Viewed From Mainframe Side.

R/W	IO address	D7 6 5 4 3 2 1 0	
READ	10	(content of input buffer)	CDB3-0
	11	Unused	
	12	"	
	13	"	
WRITE	10	CDB4-7	
	11	Unused	
	12	"	
	13	"	

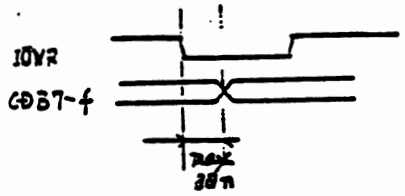
Illustration of Cartridge Interface Circuit and Time Charts.



(Or 100K)

** $\overline{CRD}$, $\overline{CWR}$, $\overline{CCS}$, CAB1 and CAB0 have high impedance and are used as input for the gate array so must be pulled up and down in an inactive state.
** $\overline{CITO}$ is high.
** $\overline{OBF}$ and IBF are reset.

AC Characteristics



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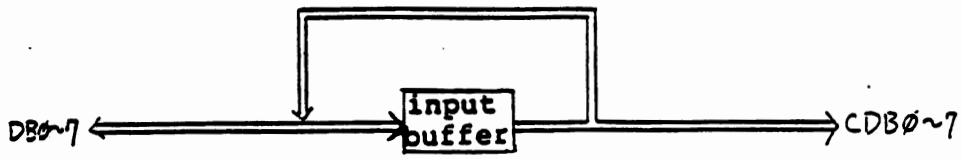
5-4 OT Mode



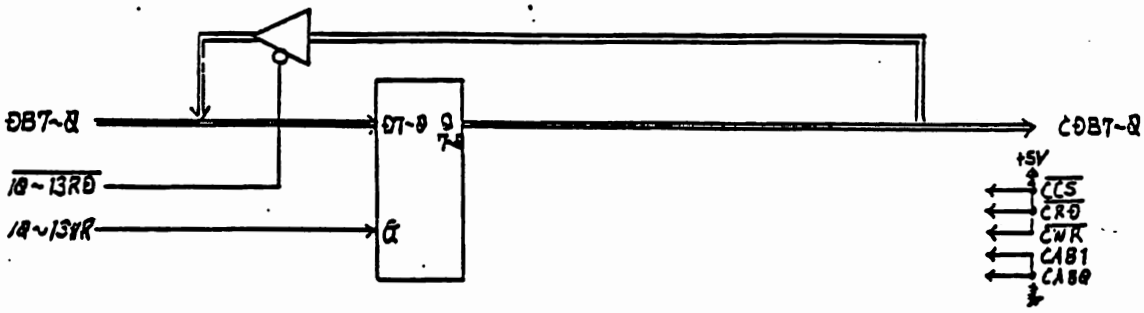
The OT mode is composed of an 8 bit input port with latch. The input port address as viewed from the mainframe side is 10H, and when writing to 10H, the data in data bus DB0 - 7 is latched in the input buffer and entered to CDB0 - 7 simultaneously. Also, when reading from 10H, it is possible to read the data in the input buffer.

CSEL must be 1 in the OT mode and because $\overline{CCS}$, CAB0, CAB1, $\overline{CRD}$ and $\overline{CWR}$ have high impedance they must be pulled up and down. $\overline{CITO}$ is 1 and no flags are used.

IO Address Base as Viewed From The Mainframe Side.

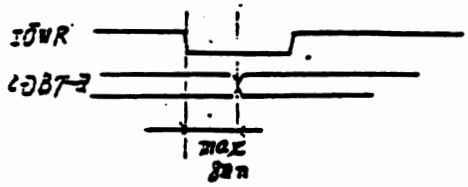
R/W	IO address	D7 6 5 4 3 2 1 Ø
READ	10	Content of input buffer
	11	Unused
	12	"
	13	"
WRITE	10	8 bit data CDBØ - 7
	11	Unused
	12	"
	13	"

Illustration Of Cartridge Interface Circuits and Timing Charts

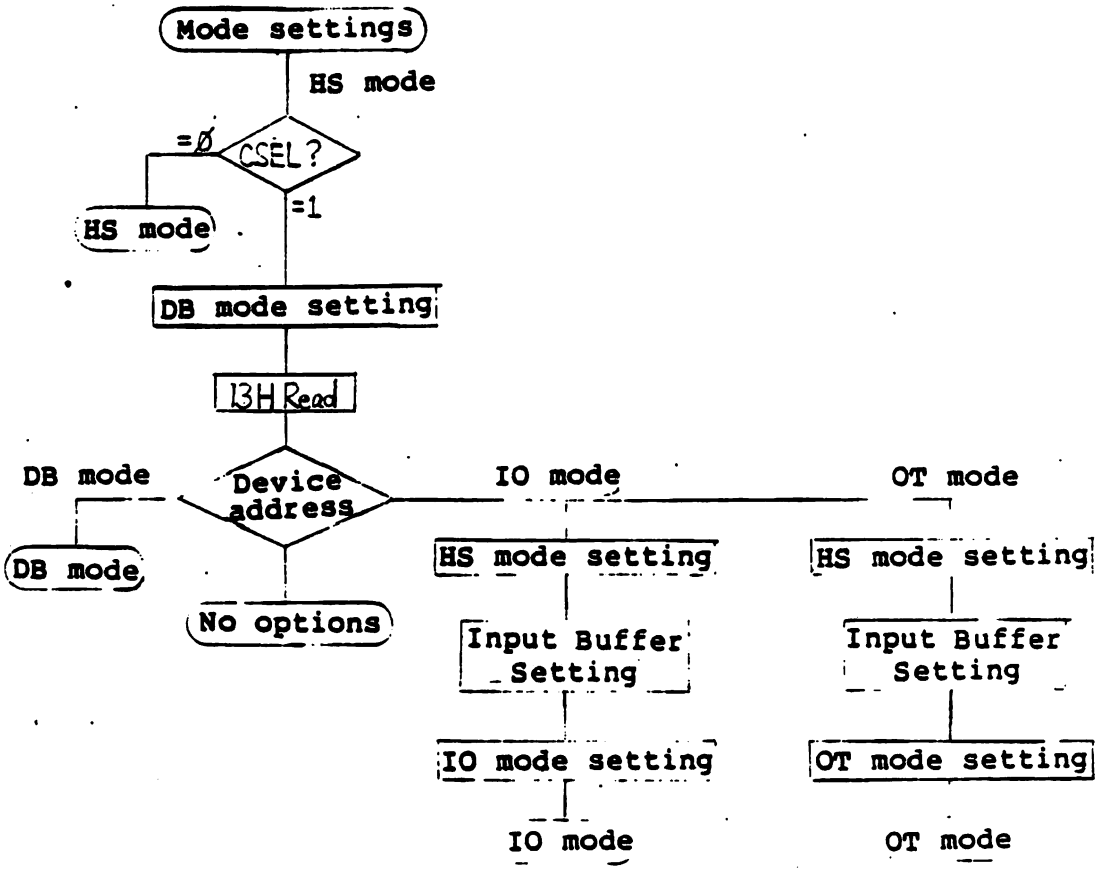


** $\overline{CITO}$ is high.
** $\overline{CCS}$, $\overline{CRG}$, $\overline{CWR}$, CAB1 and CAB0 are same as in the HS mode.
** OBF and IBF are reset.

AC Characteristics



A flow chart for mode selection is shown below . The device addresses established so far are also shown below.



Device Address

CSEL	13H 7 6 5 4	Mode option
Ø	————	HS microcassette
1	0 0 0 1	DB ROM cartridge
1	0 0 1 0	DB RAM cartridge
1	1 - - 1	IO modem
1	1 1 1 1	Nothing

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7. Explanation of Serial Ports

The cartridge has serial transmission lines CTXG and CRXT which are connected through the ART (asynchronous receiver transmitter) in the mainframe and also through the serial switch. Serial ports CTXD and CRXT are unaffected by mode setting explained in the previous section and are used for all modes.

7-1 About The Serial Switch.

In addition to the serial ports, the mainframe has 3 types serial interfaces which include the ISO and RS232C. It is the serial switch's function to select one of these three and connect it to the ART. To select cartridge serial ports, change bits 2 and 3 (SSW0, SSW1) of I/O port 18H to 0. (I/O port 18H is also used in mode setting.)

7-2 Outline Of ART Specifications.

- Baud rate : 110 - 38.4Kbps
- Data length: 7 or 8 bits
- Parity : No, even,odd
- Stop bit : Bit 1 or 2
- Error check: Parity error, framing error, over-running
- Sound break: Output possible
- Flags : TX ready, TX empty and RX ready
- Interrupt : Interruption by RX ready
- Posseses illegal start bit check function
- IXD can read directly
- Non-synchronized transmission only
- Complete double buffer transmitting and receiving

7-3 Explanations of Register

	D7	6	5	4	3	2	1	0
15H write	STP	x	EVN	PEN	x	DAT	x	x

STP: No. of stop bits
- 0: 1 stop bit
- 1: 2 stop bit

EVN: Types of Parity (PEN = 1 can be used)
- 0: Odd parity
- 1: Even parity

PEN: Presence of Parity
- 0: No Parity
- 1: Parity

DAT: Data Length
- 0: 7 bit
- 1: 8 bit

	D7	6	5	4	3	2	1	0
16H write	x	x	RPTS	ER	SBRK	RXE	RDTR	TXE

RRTS: Not used with the cartridge
RDTR:
ER : Error reset. OE,FE ,PE are reset
SBRK: Break output, TXT = 0.
RXE : Receiving possible
TXE : Transmission possible

In the case of ER only, during pulse output when ER has become 1 it is not necessary to return ER to 0.

	D7	6	5	4	3	2	1	0
15H Read	RDSR	0	FE	OE	PE	TXEM	RXRD	TXRD

RDSR: Not used for cartridges.

FE: Framing Error. Even if framing error occurs, data receiving operations will be unaffected and if the next stop bit of data is correct FE will be reset.

OE: Overrun Error. Even if overrun error occurs, data receiving operations will not be affected, however, even if the following data is received properly OE will not be reset.

PE: Parity Error. Resetting conditions for parity error are the same as those for FE. PE will be reset when PEN = 0.

TXEM: This indicates that there is no data in the transmitting section. This is set regardless of TXE.

RXRD: Receiving Ready. When RXRD = 1 interruption INT1 occurs. This is reset by receiving buffer read or error reset commands.

TXRD: Transmitter Ready. This is set when the transmission buffer is empty. It is reset when data is written into the transmission buffer.

	D7	6	5	4	3	2	1	0
14H Write	TX Data							

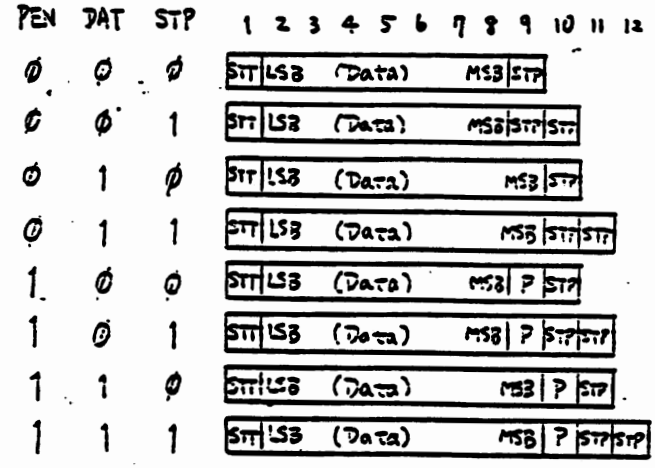
This is data that is output by TXD. When data length is 7 bits, the 7th bit is a don't care.

	D7	6	5	4	3	2	1	0
14H Read	RX Data							

This is data received from RXD. When data length is 7 bits, the 7th bit becomes 0.

7-4 Transmitting and Receiving Format

Transmitting and receiving data is transmitted and received in the order of start bit, data (LSB-NSB), parity bits and stop bit.
Data format and PEN, DAT and STP values are shown below.



STT: Start Bit
P : Parity Bit
STP: Stop Bit

Data flow

8. Precautions For Interface Creation

Please be careful of the following points when creating option cartridges.

(1) Pull Up and Pull Down
When setting device addresses in the OT and IO modes, the device address is set by applying pull up or pull down to input connectors CDB4 - 7, however, because 1M ohm of pull down is applied on the mainframe side, pull up or pull down amounting to several tens of K ohms of resistance will be necessary.

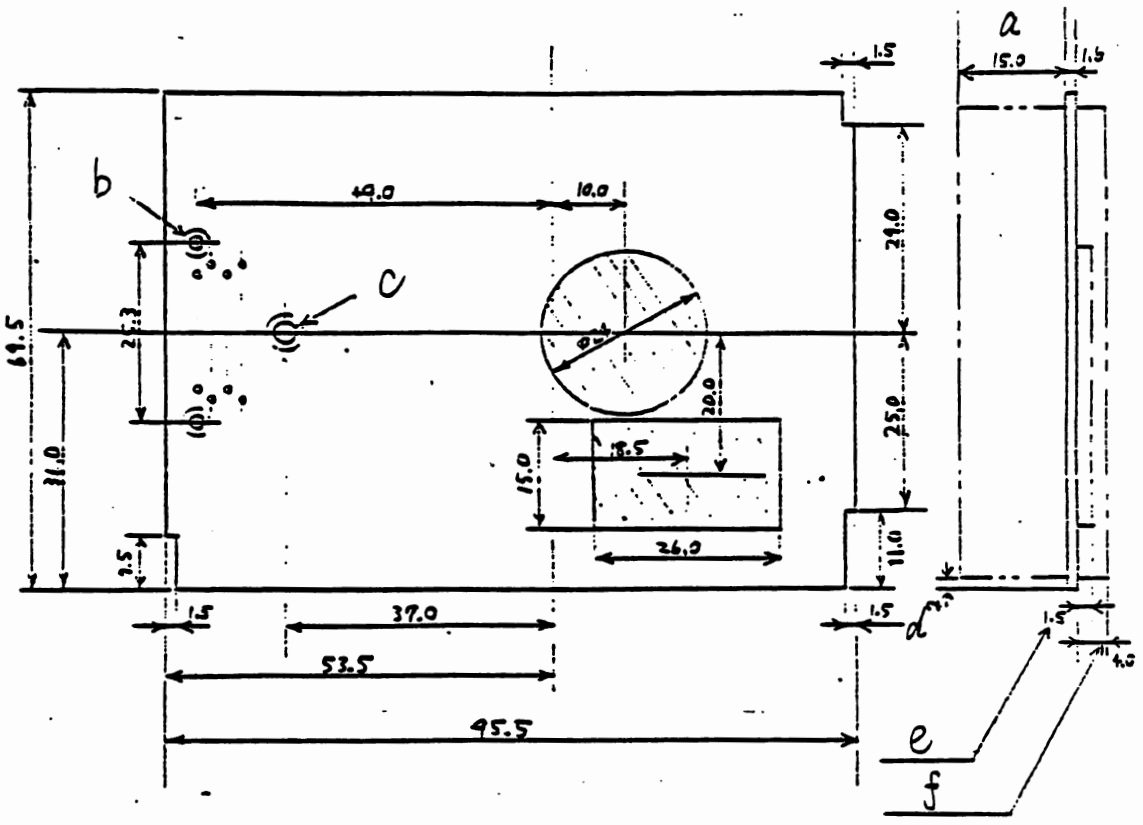
(2) Precautions For Using HS Mode.
Of options used in the HS mode, there are those that are some that are supported by the mainframe's operating system. It is important to be aware of this when creating other options. The reason for this is that when the power supply to the mainframe is on, the operating system checks to see what is connected to the option cartridge (it checks the CSEL). And because it makes an ID check of the option cartridge when an HS mode cartridge is connected, an ID check command (00) is output. The cartridge receives this command and responds with CAB1 = 1 as the response code (00). At the same time it must also respond by transmitting CAB1 = 0 as the ID number. Not following the foregoing procedures would hang the operating system up and it would not be able to start up. Therefore, cartridges used in the HS mode must observe sequence of procedures. The ID numbers which the operating system presently supports are,
08: Microcassette
09: Printer
Users who wish to create other options should apply ID numbers other than these two.

(3) About Device Addresses

When the power supply to the mainframe is turned on, its operating system checks to see what kind of options are connected and establishes which options will need supporting and carries out the necessary processing. This is why it is necessary to use 2 device addresses, one for devices which require support of the mainframe's operating system and one for those that don't. At present there are 3 types of device addresses. They are

01: ROM cartridge
02: RAM cartridge
0F: Modem

9. PCB Dimensions



a. Available mounting space

b. OCG pattern, 2-ϕ2 through whole

c. ϕ.43 pattern is not permitted, 2-ϕ2.3

d. Mounting of total circumference not permitted

e. Height restriction on slanted line sections

f. Height restriction

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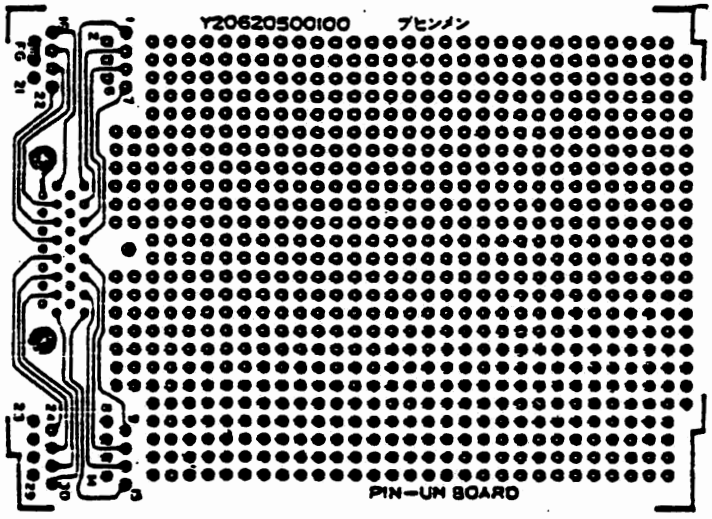

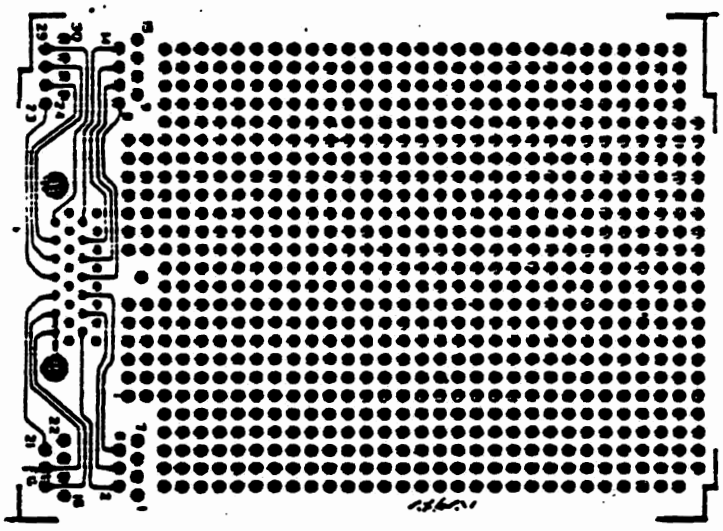

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10. Precautions Concerning FCC (including FTZ) Regulations (United States and Europe)

1. FCC regulations require that all options to conform to regulation values when they are installed in the system.
Therefore, it is necessary to obtain FCC approval each time option cartridges are created.
It is for these reasons that we have samples presented before hand of EPSON brand option cartridges to obtain approval from our equipment design section. Any applications to the FCC (FTZ) will be deliberated on before hand and actual applications will be made by EPSON Co. Ltd. or an overseas corporate entity.

2. Precautionary points regarding option cartridge design to make clearing FCC (FTZ) regulations easier.
   (1) Use C-MOS IC wherever possible in option cartridges.
   (2) Use thick power supply and ground patterns and sufficiently reduce power supply impedance.
   (3) Keep clock frequency as low as possible and use a wave form that provides as slow a start up and slow down as possible.
   (4) If external connectors are used be sure that they have metal cases and connect frame guards to the frame guard of the mainframe.

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TITLE

Pine Digital Multimeter Specifications

ISSUED SECT.	R.Q NO.	NO.

REVISIONS					SHEET REVISION STATUS							
REV	CHANGE DOCUMENT	BY	DATE	CHECK	SH	REV	SH	REV	SH	REV	SH	REV
A	First Issue				1	A			15	A		
					2	A			16	A		
					3	A			17	A		
					4	A			18	A		
					5	A			19	A		
					6	A			20	A		
					7	A			21	A		
					8	A						
					9	A						
					10	A						
					11	A						
					12	A						
					13	A						
					14	A						

MODEL	DRAWN BY	DATE	CHECKED	DATE	MGR	DATE

COVER SHEET	TOTAL SHEET	NEXT SHEET	SHEET NO

CONFIDENTIAL

Pine Digital Multimeter Specifications

Contents

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1. Application

This specifications manual applies to the Pine Digital Multimeter. (Hereon referred to as D.M.M.)

2. General Outline

i) The D.M.M. is an intelligent measuring instrument that incorporates an A/D converter IC (9775 - Suwa Seikosha), and a 4 bit CMOS CPU (M50760L). The D.M.M. is connected to the Pine cartridge interface and transfers data and commands through a 600 baud asynchronous serial communications system. Also, the cartridge interface can be set to an I/O data bus mode and used as a control signal line (Power ON/OFF, RDY). With the programming language available on the Pine main unit, a program can be made to readily control the D.M.M. and an automatic measuring system can be set up.

ii) The D.M.M. is composed of the following:
. Case
. Size AAA batteries x 2
. Substrate (circuit board)
This specifications manual applies to the use of the CPU including firmware, and the electronic circuit board on which it is integrated.

iii) Installation and removal of the D.M.M. unit should only be carried out when the power of the main unit is turned OFF. If the unit is connected or disconnected while power is still ON, proper operations of the unit cannot be guaranteed. Additionally, the D.M.M. unit should not be connected or disconnected while the input terminal is connected to an object being measured.

Pine D.M.M. Hardware Specifications

Contents

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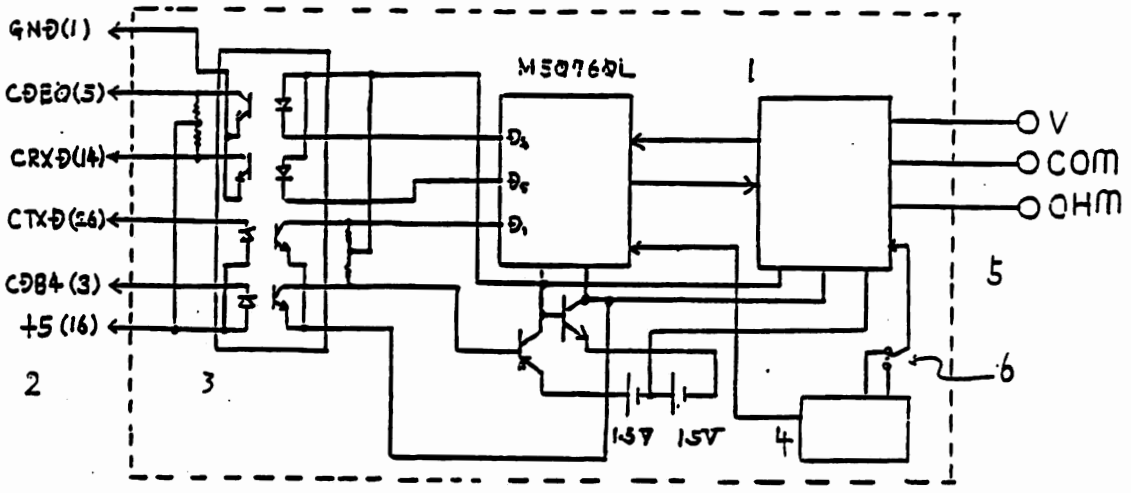
1-2 D.M.M. Configuration

A general configuration diagram of the D.M.M. is shown below.

1. A/D converter IC
2. Pine connector
3. Photo coupler PC-817
4. Oscillator
5. Measuring terminal
6. Integral time selection switch

Fig 2



- The Pine main unit and the D.M.M. is completely insulated by the photo coupler.
- The measuring terminals are V, OHM, and COM terminals and the resistance measurement terminals are OHM and COM, while the terminals used for voltage measurement are V and COM.
- The power is supplied with 21.5V AAA sized batteries.
- An integral timing switch is included and can be found by opening the battery box.

1. System Description
The Pine is designed for the D.M.M. to be one of the options to be connected to the cartridge interface. The D.M.M. is designed to communicate by the cartridge serial interface or the I/O data bus mode.

1-1 Cartridge Interface (CTG-IF)
A general diagram of the system is shown below.

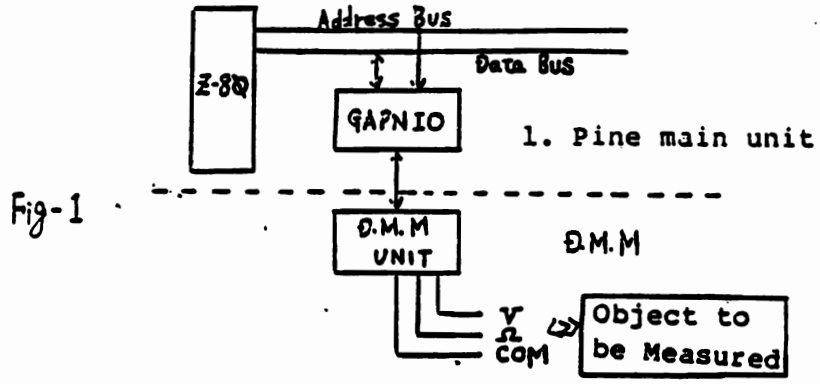


Fig-1

Data and commands are transferred by communications between the D.M.M. and the GAPNIO (the Pine cartridge interface IC).

Signal line
CTXD (connector pin 26) : Command output line from Pine
DRXD (connector pin 14) : Data and ACK output line from D.M.M.

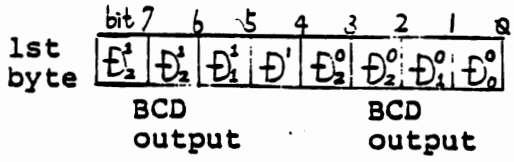
Control line
CDB0 (connector pin 5) : Command (range selection command) RDY signal
CDB4 (connector pin 3) : Power ON/OFF control signal

Signal line : Asynchronous serial communications line
. 600 baud
. 1 start bit
. 8 bit data
. No parity
* It is necessary to set the Pine serial communications mode to CIG serial communications mode.

Control line : By setting to the I/O data bus mode, the Pine can control CDB0, which in turn can control the ON/OFF of CDB4, the input line to the Pine.
* I/O port set bits 1 and 0 at address 18 to bit 1 = "0" and bit 0 = "1".

2. Outline of Measuring Functions
The types of measurements include DCV, ACV, OHM and low power OHM. Data are 3 1/2 digits and maximum digit is 2999.

2-1 General Specifications
Data Output : Data 3 1/2 digits max equals 2999, Output is BCD format, 3 byte overflow display, 10^3 columns (most significant digit) is 3. Automatic sign selection, "-" bit is set.



10^1 column
10^0 column
10^3 column (overflow display)
10^2 column

3rd byte
Auto Range display
Millivolt Units
K ohm units
Battery Low

$P_{1,2,3}$ { Decimal point position designation

Symbol
mV, V, Ω, kΩ, Auto, Batt

Data BCD format output

* Decimal point position designation (one position of P3-P1 set to 1 or all set to 0). This is combined with the BCD output to display the actual value.
When measuring resistance, the existence of K ohm units (K=1:K ohm units, K=0:ohm units) is shown by the presence of this bit. For voltage measurements, millivolts are expressed with the presence of this bit (M=1:millivolts, M=0:V).
* Auto : displays if is set to Auto Range with "1".
* Batt : displays if the battery is low witn "1". When this bit is set to "1", the battery must be replaced.

Case resistance : 1 KV
Measuring method : double integral system
Range selection : Auto range and fixed range
Sample rate : Approx 4/sec (60 Hz area integral time)
: Approx 5/sec (50 Hz " " ")
Precision guaranteed temperature and humidity :
18 ℃ - 28 ℃, less than 80% R.H. (with no condensation)
Optional temperature and humidity :
5 ℃ - 35 ℃, less than 80% R.H. (with no condensation)
Storage temperature and humidity :
-20 ℃ - 60 ℃, less than 70% R.H. (with no condensation)
Power supply : +/-1.5 V, size AAA batteries x 2.
Battery low : 1.32 +/- 0.8 V sets Batt signal bit to "1".
Power consumption : 9 mw (3 mA)

Down range : When the count results is less than 179 :
Example : When measuring within the 30.00 K ohm range and the resistance drops below 1.79 K ohm, this becomes 0.179 K ohm and the range is set to 3.000 K ohm.

2-3 Input impedance
DCV : greater than 100 M ohm, 300.0 mV range
approx. 10 M ohm, excluding 300.0 mV range
ACV : approx. 10 M ohm

2-4 OHM opening voltage
OHM : 1.5V+/-0.2V, 300.0 onm range
: 0.65V+/-0.7V excluding 300.0 ohm range
LP ohm : less than 0.4V
(low power)

2-5 Precision
Allowable deviation : refer to appendix 1,
Temperature characteristics :
sld lift : +/-0.3 digit/°C
gain lift : +/-400 ppm/°C.fs

2-6 Circuit overload protection
V terminal : 500VDC or DC+AC peak
Ohm terminal : 250VAC 1 minute

3. Integral time switching
This is set to match the power supply (AC) in the area that the D.M.M. is being used. (50Hz/60Hz) By setting the integral time, it is possible to suppress AC noise. The integral time selection switch can be found by opening the cover of the battery box. In terms of software, as described in the section on commands, it is set up so that bit 5 of ACKO receives this information. Through software, it is possible for the Pine to detect this setting.

Pine D.M.M. Command Specifications

Contents

4. Command Specifications (corresponds to BASIC)

4-1 Activation

(1) Connect the D.M.M. to the Pine cartridge unit.

(2) Turn the Pine ON.

(3) Set the Pine cartridge interface to I/O mode. Set the cartridge switches in the switch register (SWR, address 18H) CSW1, CSW0 (bit 1,0) to CSW1="0" and CSW0="1".

```
OUT &H18, 1
```

(4) Power ON the D.M.M. and reset
CDB4 is the D.M.M. power ON/OFF control line.

```
OUT &H10, &HF0
```

It is necessary to wait at least 5 seconds between these 2 commands because of power ON and reset.

```
OUT &H10, &H00
```

(5) Open the communications line between the Pine and the D.M.M. The cartridge serial communications port is used (600 baud, 8 bit data, no parity).

```
OPEN "I", #1, "COM3: (88N1FNN)"
OPEN "O", #2, "COM3: (88N1FNN)"
```

(6) Set measuring mode

```
PRINT #2 CHR$ (&Hnn)
```

bit7	6	5	4	3	2	1	0
1	n6	*	n4	n3	n2	n1	n0

1 byte command

↑ Fixed ↑ Unused

(i) Range set

Range signifies Auto range set

R2-R6 are the Range numbers as described in the section on measurement ranges.

n2	n1	n0	Range
0	0	0	R0
0	0	1	Cannot be used
0	1	0	R2
0	1	1	R3
1	0	0	R4
1	0	1	R5
1	1	0	R6

(ii) DCV <-> ACV; ohm <-> LP ohm selection n3

n3 1 : ACV or LP ohm
0 : DCV or ohm

(iii) Voltage measurement <-> resistance selection n4

n4 1 : resistance measurement
0 : voltage measurement

The combination of (ii) and (iii) will determine what is being measured.
Example : n3=1, n4=0 designates LP ohm

(iv) OUTPUT System n6

n6 1 : output mode 1 (In this periodic mode, the D.M.M. remains in idle status, until the D.M.M. receives ACK1 from the PINE,. When ACK1 is received, the next A/D conversion data is sent to the PINE)

0 : output mode 0 (This is a free run mode where the next set of A/D data is sent when a certain amount of time has clasped, even when ACK1 is not sent from the Pine.)

(7) ACK0 judgement

In order to judge if the measuring mode as described in (6) has been properly set in the D.M.M., ACK0, the acknowledge signal is sent back from the D.M.M. ACK0, with the exception of bit 5, should be have the same contents as the measuring mode set command. If the there is a discrepancy, the power ON/reset is executed as described in (4).
The contents of bit 5 expresses the contents of the integral time setting switch attached to the D.M.M. bit 5="0" : 50 Hz and bit 5="0" : 60 Hz. The reason this is included is for the purpose of suppression the effects of AC noise. It is not vital for this to be set to the frequency of the environment, however if set, this will increase accuracy. Please take note that the sample rate will differ from the 50 Hz and 60 Hz settings.

A=ASC(INPUT$(1,#1)) The value of A is compared to nn <1> value of (6)

(8) RUN command

This command is instructed to D.M.M. in order to send the next set of A/D conversion data. This will execute only if ACK0 is correct.

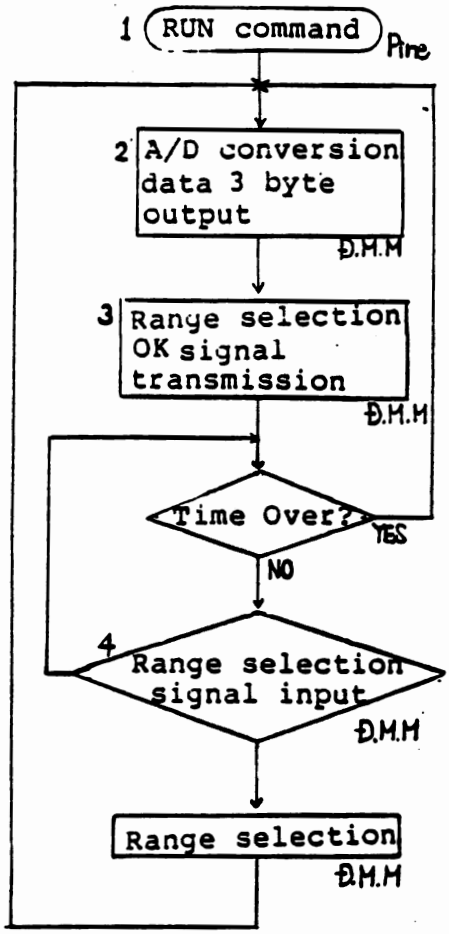
PRINT #2,CHR$(XX)

XX is not used and the contents does not matter

4-2 Data input

The way data is input depends on the OUTPUT system setting. (n6)

(i) For OUTPUT mode 0



(D.M.M. Operation)

When the RUN command is received by the D.M.M., 3 bytes of A/D conversion data is output then the Range selection OK signal is transmitted. After transmission, the D.M.M. waits for the Range selection signal and when this signal is receives, the Range is selected and switched and then output of A/D conversion data is resumed.

If the Range selection command is not sent in the set interval of time, TIME OVER results and output of A/D conversion data is resumed.

(1) A/D data input

```
D0 = ADC(INPUT$(1,#1))
D1 = ADC(INPUT$(1,#1))
D2 = ADC(INPUT$(1,#1))
```

(2) Confirmation of Range selection OK signal

```
R=INP(&H10)
```

bit 0 of R is tested

"0" = Range selection OK signal active

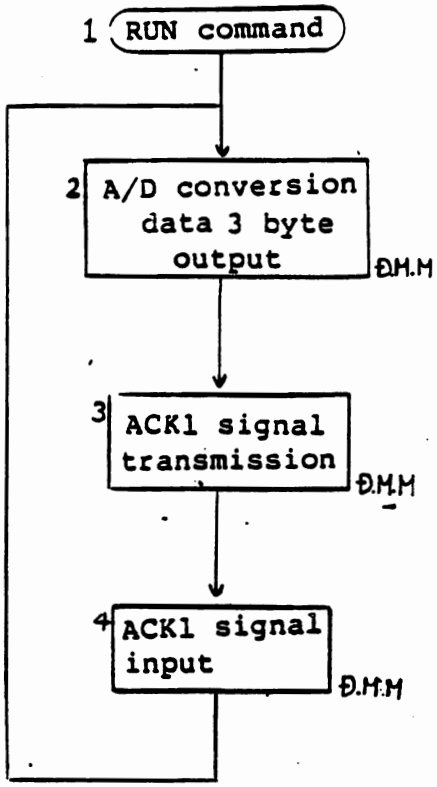
"1" = Range selection OK signal inactive

Range selection is necessary after A/D data input (manual Range). Range selection OK is confirmed to be active then the Range selection command is transmitted.

(3) Range selection command
PRINT #2,CHR$(0n) n=0-6
This corresponds to R9-R6 as described in the section on functions.

When operated in this OUTPUT mode 0, A/D conversion data will be entered in the TIME OVER interval and the sample rate as described in the general specifications can be obtained.

(ii) For OUTPUT mode 1



(D.M.M. operation)

When the RUN command is received by the D.M.M., 3 bytes of A/D conversion data is output then the ACK1 RDY signal is transmitted. The D.M.M. waits until the ACK1 signal is received the resumes A/D conversion data output.

(1) A/D data input

```
D0=ASC(INPUT$(1,#1))
D1=ASC(INPUT$(1,#1))
D2=ASC(INPUT$(1,#1))
```

(2) ACK1 RDY signal confirmation

```
R=INP (&H10)
```

bit 0 of R is tested
"0" = ACK1 RDY active
"1" = ACK1 RDY inactive
When the ACK1 RDY = signal becomes active, ACK1 is transmitted.

(3) ACK1 signal transmission

```
PRINT #2,CHR$(m,m)
```

bit7	6	5	4	3	2	1	0	m.m
m7	m6	m5	m4	m3	m2	m1	m0	
1	x	x	x	x	x	x	x	: Range is not selected (switched) and A/D conversion data is requested.
0	0	0	0	0	m2	m1	m0	: As expressed by m2-m0 (base 2), 0-6 corresponds to R0-R6 Range and selects the Range. R1 is reserved.

x : Unused

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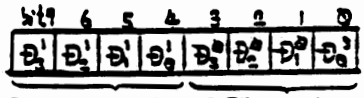
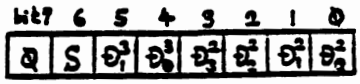
4-3 A/D conversion data 3 bytes

1st byte



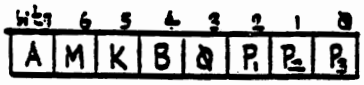
(BCD output 10^1 column (BCD output 10^0 column

2nd byte



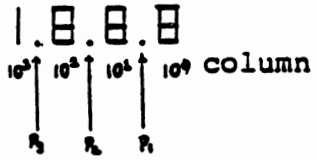
Sign
BCD output 10^3 column
BCD output 10^2 column

3rd byte



Auto Range
M units
K units
Battery Low
point

S: sign bit
"1" : minus
"0" : plus
P1-P3: point designation



The value is express with the point and BCD.
B: Battery Low bit
"1" : Battery Low
"0" : Battery O.K.
When the battery is low, the internal batteries should be replaced.
K: K units
"1" : Expresses K ohms
"0" : No K ohms (ohms or voltage measurement)
M: M units
"1" : Expresses mV
"0" : not mV (V or resistance measurement)
AUTO: AUTO Range
"1" : Expresses AUTO Range
"0" : Expresses Manual Range

4-4 Power OFF

OUT &H10, &HFO

With this, the power of the D.M.M. is turned OFF.

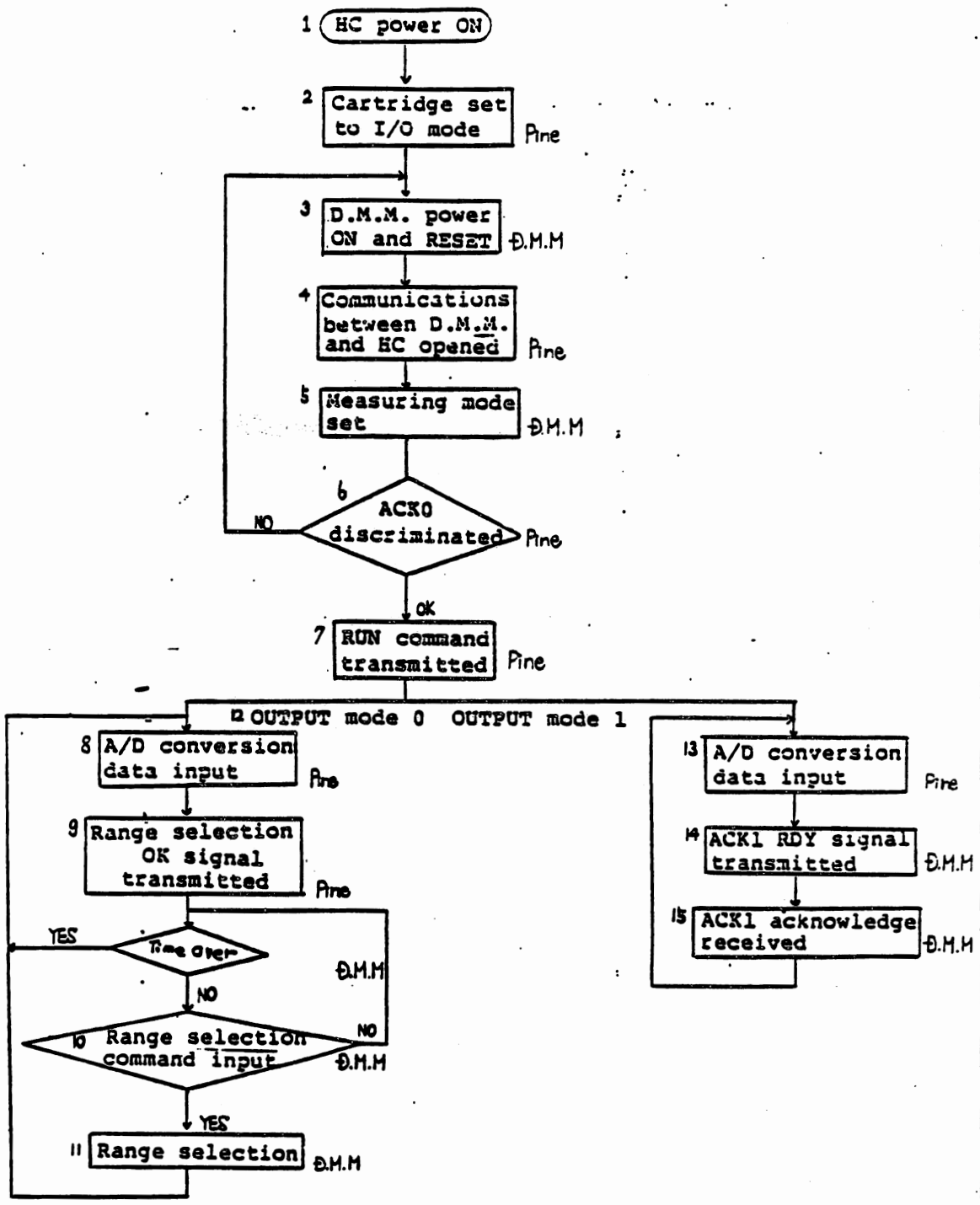
* The power is not turned OFF when the BREAK key is pressed, thus the power OFF command must be executed. (If this is not done, the D.M.M. batteries will be depleted.)

4-5 Table of Commands

Command	Basic	Binary data value							
D.M.M. power ON & RESET	OUT &H10, &HF0 OUT &H10, &H00	1 0	1 0	1 0	1 0	0 0	0 0	0 0	0 0
D.M.M. power OFF	OUT &H10, &HF0	1	1	1	1	0	0	0	0
HC set to I/O mode	OUT &H18, 1	0	0	0	0	0	0	0	1
Communications between D.M.M. and HC open	OPEN <input mode>, <file number>, "COM3:(88N1FF)"								
Measuring mode setting	PRINT#-, CHR$ (&Hnn)	n7	n6	*	n4	n3	n2	n1	n0
ACK0 descrimination	A=ASC(INPUT$ (1,#-))	n7	n6	n5	n4	n3	n2	n1	n0
RUN command	PRINT#-, CHR$ (x, x)	*	*	*	*	*	*	*	*
A/D data input	D=ASC(INPUT$ (1, #))	D7	D6	D5	D4	D3	D2	D1	D0
ACK1 RDY, Range selection OK	R=INP(&H10)	*	*	*	*	*	*	*	R
Range selection command	PRINT#-, CHR$ (0n)	0	0	0	0	0	n2	n1	n0
ACK1 acknowledge (Range not selected (switched))	PRINT#-, CHR$ (80)	1	*	*	*	*	*	*	*

- : file no. * : unused

5. Operation Flow



EPSON CORPORATION	TITLE	SHEET REVISION	NO.
	CONFIDENTIAL	A	NEXT 20 / SHEET 19

Appendix 1

Allowable Deviation 23 C +/-5°C
80% R.H. without condensation.

Function	Range	Allowable deviation	
DCV	300.0 mV	+/-(0.5% rdg + 2 dgt)	
	3.000 V	"	
	30.00 V	"	
	300.0 V	"	
	500 V	+/-(0.8% rdg + 2 dgt)	
ACV	3.000 V	+/-)0.8% rdg + 4 dgt)	40-500Hz
	30.00 V	"	"
	300.0 V	"	"
	350 V	+/-(10% rdg + 4 dgt)	"
OHM	300.0	+/-(0.5% rdg + 4 dgt)	
	3.000 K	"	
	30.00 K	"	
	300.0 K	"	
	3000 K	+/-(1.5% rdg + 4 dgt)	
LP	3.000 K	+/-(0.8% rdg + 8 dgt)	
	30.00 K	"	
	300.0 K	"	
	3000 K	+/-(2.0% rdg + 8 dgt)	
Remainder		less than 4 dgts	

Appendix 2 D.M.M. Power Supply

The D.M.M. is designed to obtain it's power from batteries (size AAA internal batteries). This insulates it from the Pine main unit and serves to protect the Pine from the object being measured. However, if the object to be measured is less than 7 volts then there is no danger of the Pine being damaged. Only under these conditions, should the option to supply power from the Pine main unit to the D.M.M. be considered.
When power is supplied from the pine main unit, if an AC adapter is used, checking and replacing batteries will no longer be necessary and is ideal for using over extended periods of time. However, note that there is a limit to the range that this method can be used and caution should be taken.

Copy
Cover to
Frank
Dave C.
cc'd to Dave S.
Thanks

EPSON AMERICA INC

MEMO

DATE: 4/26/84
REF NO: 966

TO: MR. FRANK TIRIMACCO LOCATION: MS2-4
FROM: E. IDE LOCATION: MS2-1

SUBJ: SPEC OF THE PINE MODEM UNIT HARDWARE

ATTACHED IS A COPY OF THE MODEM UNIT HARDWARE SPEC. REV. "A" FOR THE PINE.

A SAMPLE IS SUPPOSED TO BE AVAILABLE TO SERVICE DIV BY END MAY.

THANK YOU.

CC: MR. DAVE CHRISTOPHERSON