June 1995

M68MPBF333

MCU PERSONALITY BOARD

SCHEMATIC DIAGRAMS

This package contains the M68MPBF333 MCU Personality Board (MPB) schematic diagrams. These schematic diagrams are for reference only and may deviate slightly from the circuits on your MPB.

TABLE OF CONTENTS

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED
	0	ORIGINAL RELEASE	10/15/93	R.G.
	A	CHANGE XFC CAP VALUE/PKG SIZE		

DRAWN BY: R. G.	DATE: 10/15/93
DESIGN ENGINEER: R. G.	DATE:
PROJECT LEADER: R. G.	DATE:

MOTOROLA INC.

MICROPROCESSOR AND MEMORY TECHNOLOGIES GROUP

6501 WILLIAM CANNON DRIVE WEST AUSTIN, TEXAS 78735 USA

TITLE: SCHEMATIC - MPBF333C

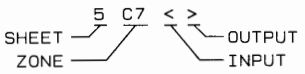
SIZE		DWG. NO.	REV:
A	GEDTTL: BOARD GEDABV: MPBF333C	63ASE90427W	A

LAST_MODIFIED=Tue Jun 21 18:36:32 1994 SHEET 1 OF 8

DWG. NO. 63ASE90427W REV: A

NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTORS ARE IN OHMS, 5%, 1/8 WATT.
   ALL CAPACITORS ARE IN UF. 50V.
   ALL VOLTAGES ARE DC.
2. INTERRUPTED LINES CODED WITH THE SAME LETTER OR LETTER COMBINATIONS ARE ELECTRICALLY CONNECTED.
3. DEVICE TYPE NUMBER IS FOR REFERENCE ONLY. THE NUMBER VARIES WITH THE MANUFACTURER.
4. SPECIAL SYMBOL USAGE:
   * DENOTES - ACTIVE LOW SIGNAL.
   <> DENOTES - VECTORED SIGNALS.
5. INTERPRET DIAGRAM IN ACCORDANCE WITH AMERICAN NATIONAL STANDARDS INSTITUTE SPECIFICATIONS, CURRENT REVISION, WITH THE EXCEPTION OF LOGIC BLOCK SYMBOLOGY.
6. CODE FOR SHEET TO SHEET REFERENCES IS AS FOLLOWS:



7. VCC LOCATIONS
   UNLESS OTHERWISE SPECIFIED, VCC IS APPLIED TO:
   PIN 8 OF ALL 8-PIN ICS
   PIN 14 OF ALL 14-PIN ICS
   PIN 16 OF ALL 16-PIN ICS
   PIN 20 OF ALL 20-PIN ICS, ETC.
8. GROUND LOCATIONS
   UNLESS OTHERWISE SPECIFIED, GROUND IS APPLIED TO:
   PIN 4 OF ALL 8-PIN ICS
   PIN 7 OF ALL 14-PIN ICS
   PIN 8 OF ALL 16-PIN ICS
   PIN 10 OF ALL 20-PIN ICS, ETC.

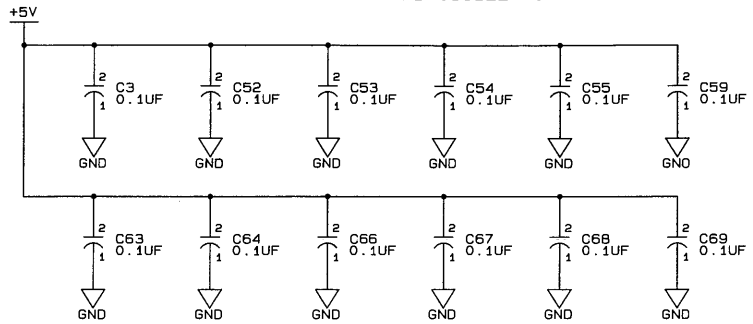
NOTES

DWG. NO. 63ASE90427W

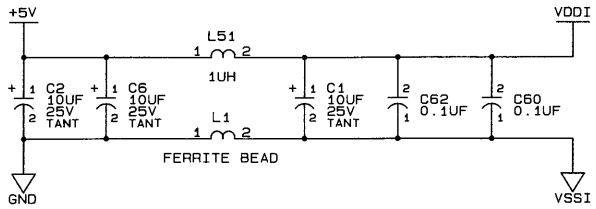
REV: A

SIZE	GEDTTL: BOARD	DWG. NO.	REV:
A	GEDABV: MPBF333C	63ASE90427W	A
LAST_MODIFIED=Tue Jun 21 18:36:47 1994		SHEET 2 OF 8	

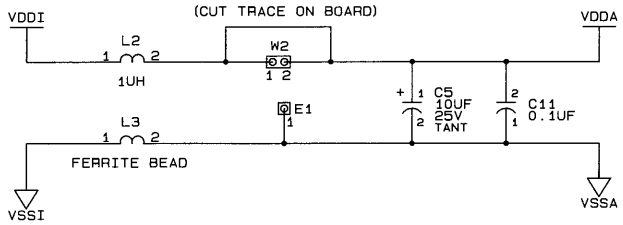
+5V AND GND DECOUPLING
FOR VDDE OF MCU AND OSCILLATOR



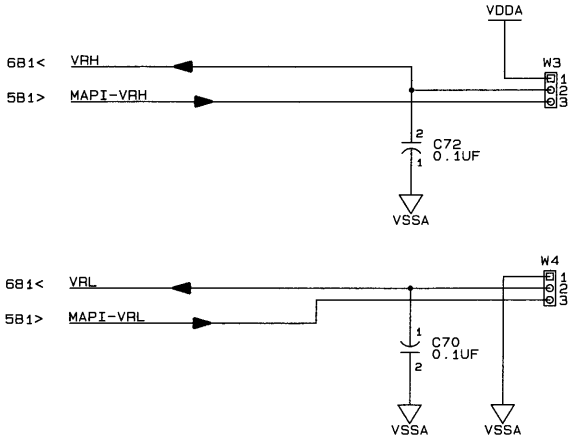
VDDI/VSSI GENERATION



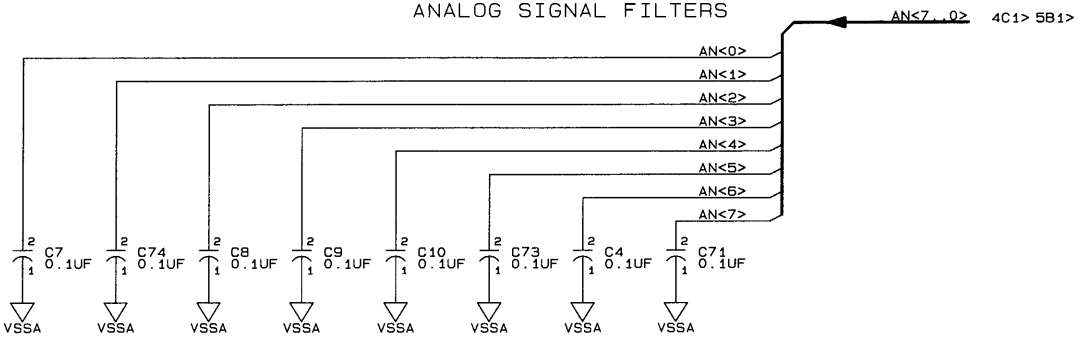
ADC MODULE
VDDA/VSSA GENERATION



ADC MODULE
VRH & VRL SELECTION



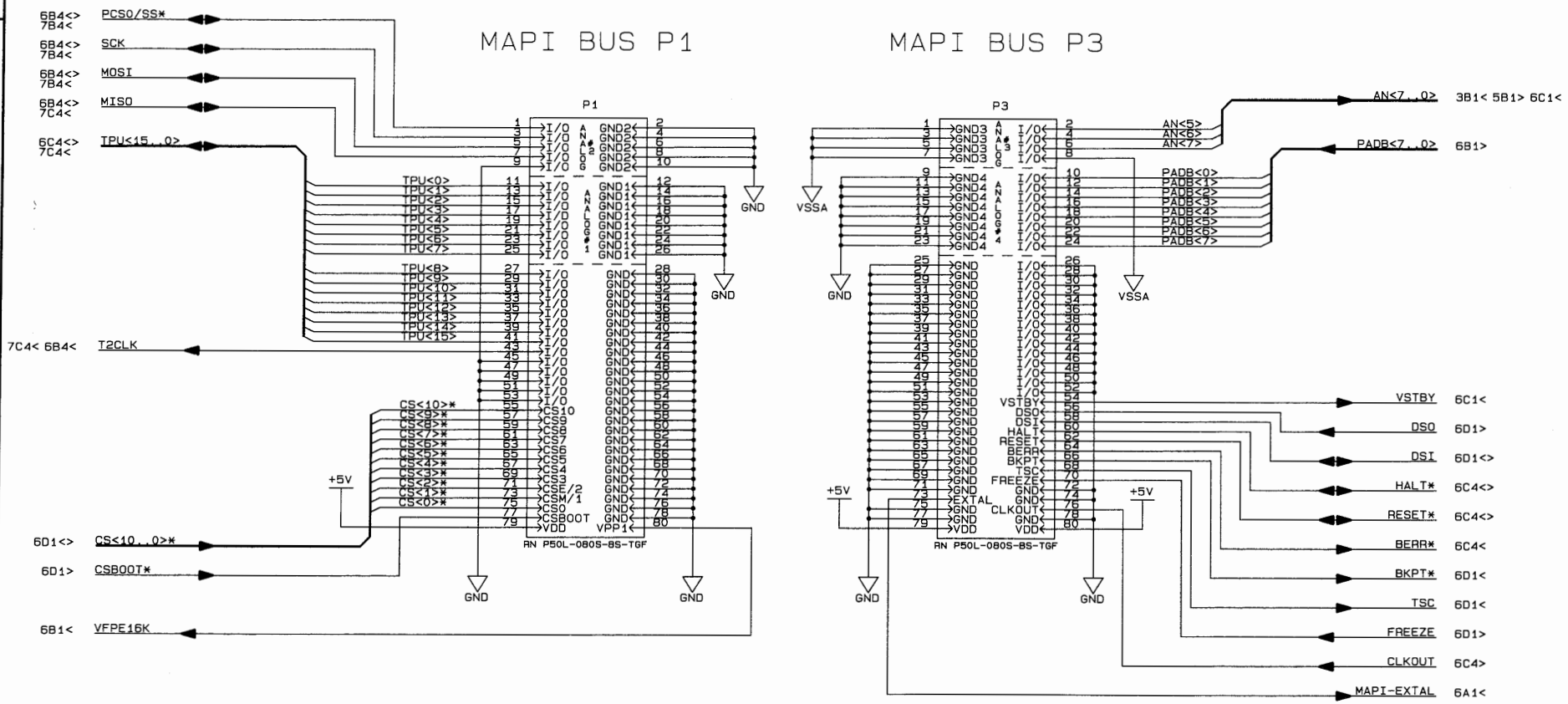
ADC MODULE
ANALOG SIGNAL FILTERS



BYPASS CAPACITORS, CLEAN POWER & SIGNAL FILTERS

SIZE	GEDTTL: BOARD	DWG. NO.	REV:
A	GEDABV: MPBF333C	63ASE90427W	A
LAST_MODIFIED=Tue Jun 21 19:31:54 1994		SHEET 3 OF 8	

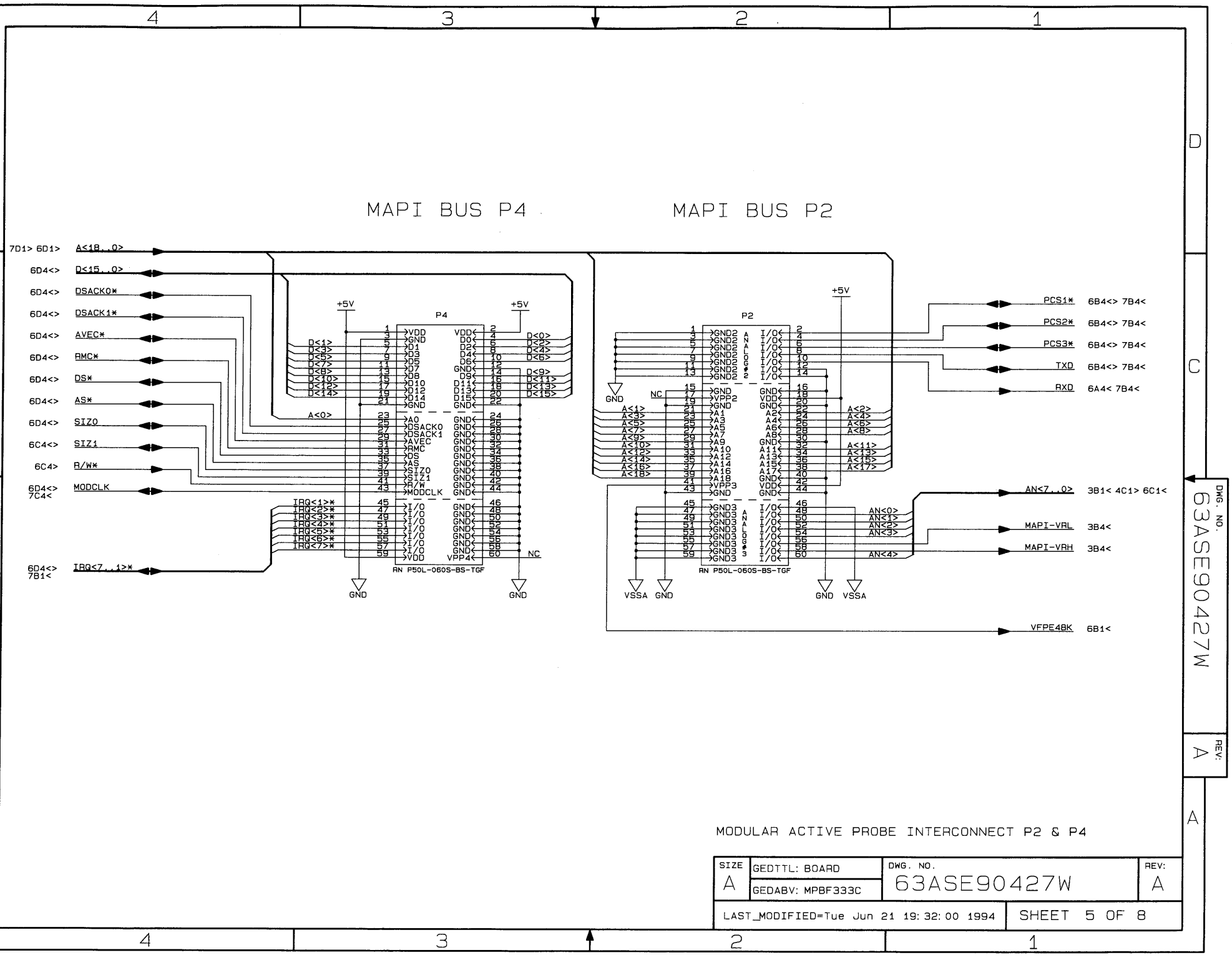
DWG. NO. 63ASE90427W REV: A



MODULAR ACTIVE PROBE INTERCONNECT P1 & P3

SIZE		DWG. NO.	REV:
A	GEDTTL: BOARD GEDABV: MPBF333C	63ASE90427W	A
LAST_MODIFIED=Tue Jun 21 19:31:58 1994		SHEET 4 OF 8	

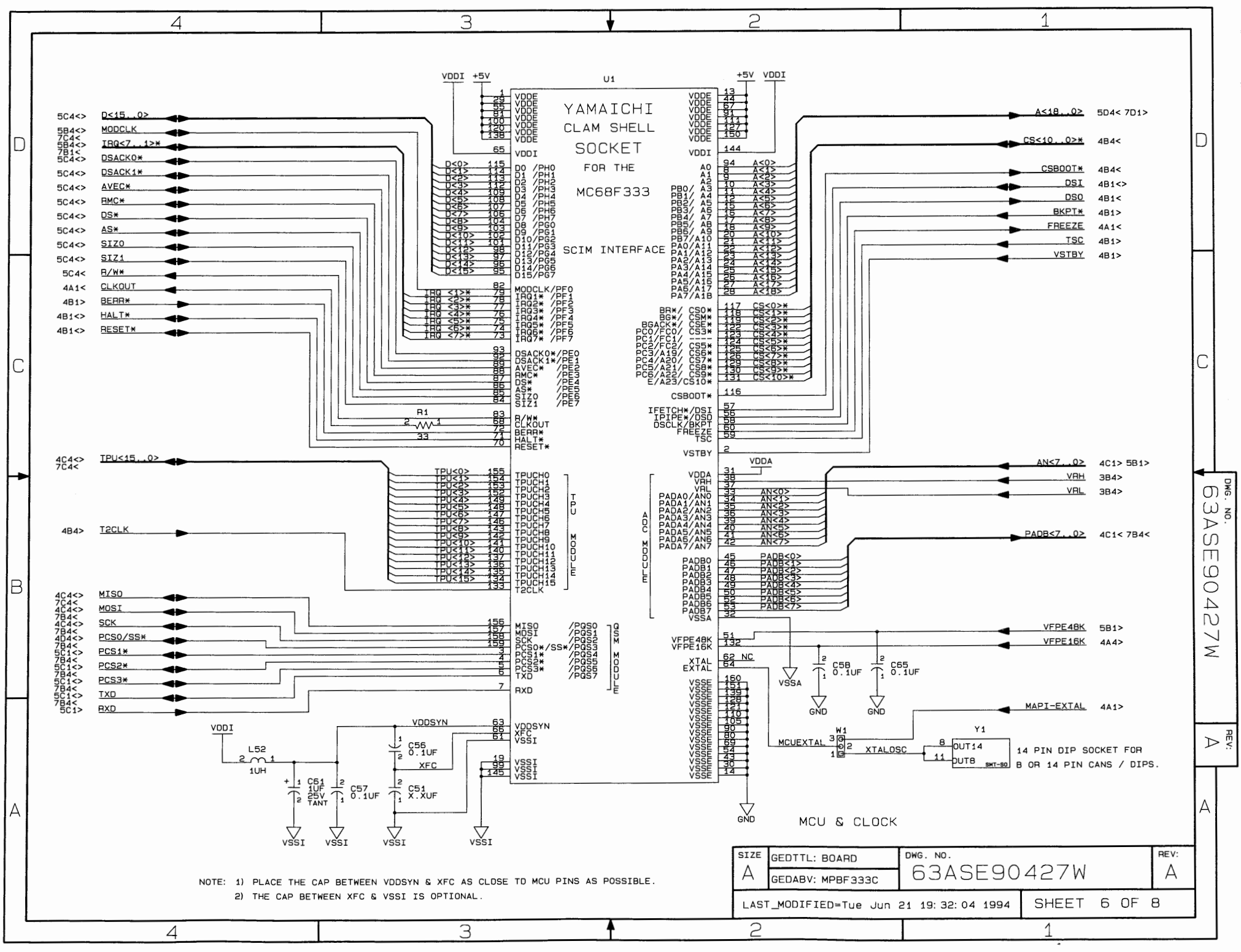
DWG. NO. 63ASE90427W REV: A



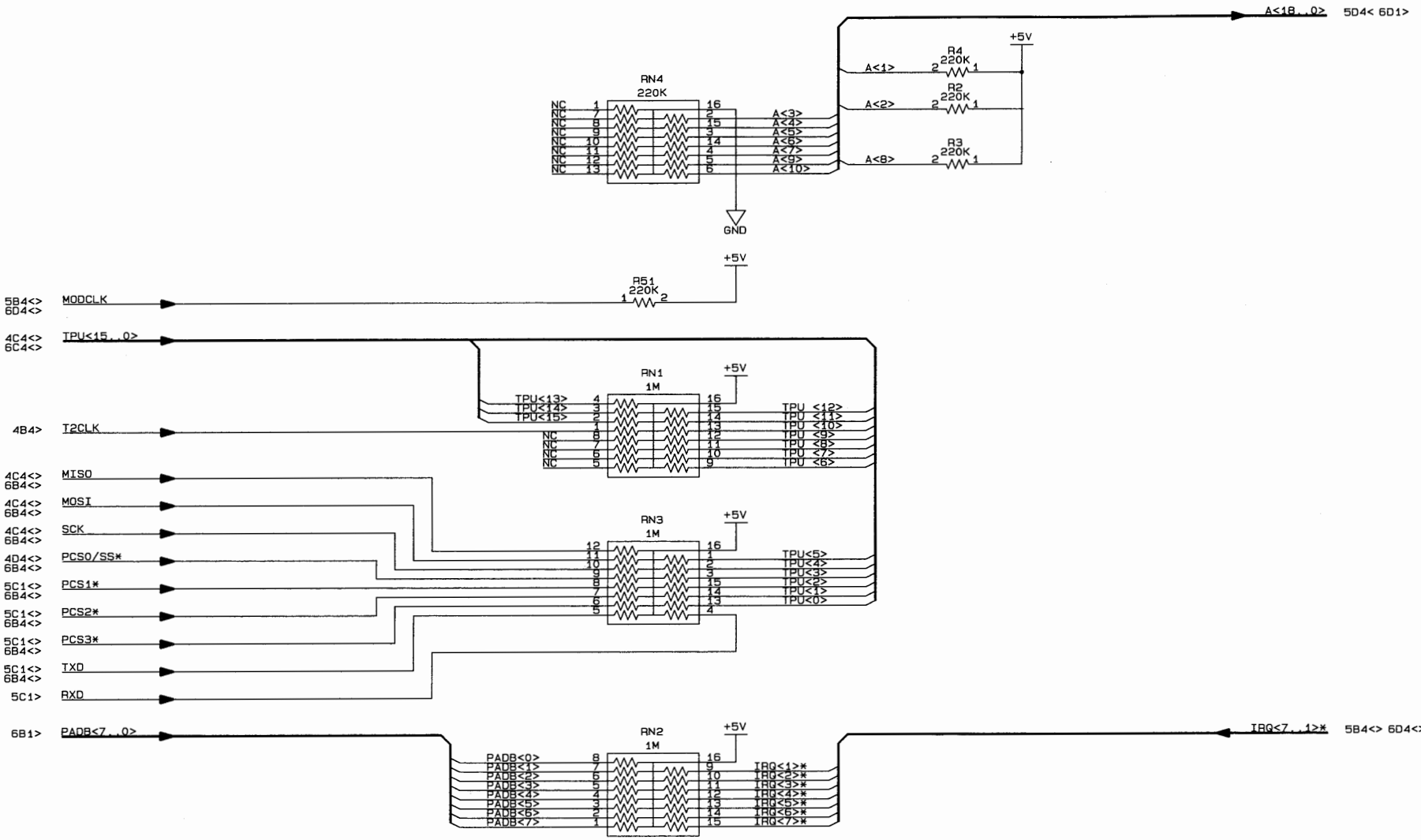
MODULAR ACTIVE PROBE INTERCONNECT P2 & P4

SIZE		DWG. NO.	REV:
A	GEDTTL: BOARD GEDABV: MPBF333C	63ASE90427W	A
LAST_MODIFIED=Tue Jun 21 19:32:00 1994		SHEET 5 OF 8	

DWG. NO. 63ASE90427W REV: A


U1
YAMAICHI
CLAM SHELL
SOCKET
FOR THE
MC68F333
SCIM INTERFACE
MCU & CLOCK
D<15..0>
MODCLK
IRQ<7..1>*
DSACK0*
DSACK1*
AVEC*
RMC*
DS*
AS*
SIZ0
SIZ1
R/W*
CLKOUT
BERR*
HALT*
RESET*
TPU<15..0>
T2CLK
MISO
MOSI
SCK
PCS0/SS*
PCS1*
PCS2*
PCS3*
TXD
RXD
A<18..0>
CS<10..0>*
CSBOOT*
DSI
DSO
BKPT*
FREEZE
TSC
VSTBY
AN<7..0>
VRH
VRL
PADB<7..0>
VFPE48K
VFPE16K
MAPI-EXTAL
MCUEXTAL
XTALOSC
14 PIN DIP SOCKET FOR
8 OR 14 PIN CANS / DIPS.
L52
1UH
C56 0.1UF
C61 1UF 25V TANT
C57 0.1UF
C51 X.XUF
C58 0.1UF
C65 0.1UF
R1
33
NOTE: 1) PLACE THE CAP BETWEEN VDDSYN & XFC AS CLOSE TO MCU PINS AS POSSIBLE.
2) THE CAP BETWEEN XFC & VSSI IS OPTIONAL.
SIZE A
GEDTTL: BOARD
GEDABV: MPBF333C
DWG. NO. 63ASE90427W
REV: A
LAST_MODIFIED=Tue Jun 21 19:32:04 1994
SHEET 6 OF 8

MC68HCF333 MCU PERSONALITY CODE = 083HEX
(USING A<10..1>)



PULL-UPS / PULL-DOWNS / PERSONALITY ID

SIZE		DWG. NO.	REV:
A	GEDTTL: BOARD GEDABV: MPBF333C	63ASE90427W	A
LAST_MODIFIED=Tue Jun 21 19:32:06 1994		SHEET 7 OF 8	

DWG. NO. 63ASE90427W REV: A

*** Signal Cross-Reference ***
--- for the entire design --

A <18..0>	5D4< 6D1> 7D1>
AN <7..0>	3B1< 4C1> 5B1> 6C1<
AS *	5C4<> 6D4<>
AVEC *	5C4<> 6D4<>
BERR *	4B1> 6C4<
BKPT *	4B1> 6D1<
CLKOUT	4A1< 6C4>
CS <10..0> *	4B4< 6D1<>
CSBOOT *	4B4< 6D1>
D <15..0>	5C4<> 6D4<>
DS *	5C4<> 6D4<>
DSACK0 *	5C4<> 6D4<>
DSACK1 *	5C4<> 6D4<>
DSI	4B1<> 6D1<>
DSO	4B1< 6D1>
FREEZE	4A1< 6D1>
HALT *	4B1<> 6C4<>
IRQ <7..1> *	5B4<> 6D4<> 7B1<
MAPI-EXTAL	4A1> 6A1<
MAPI-VRH	3B4< 5B1>
MAPI-VRL	3B4< 5B1>
MISO	4C4<> 6B4<> 7C4<
MODCLK	5B4<> 6D4<> 7C4<
MOSI	4C4<> 6B4<> 7B4<
PADB <7..0>	4C1< 6B1> 7B4<
PCS0/SS *	4D4<> 6B4<> 7B4<
PCS1 *	5C1<> 6B4<> 7B4<
PCS2 *	5C1<> 6B4<> 7B4<
PCS3 *	5C1<> 6B4<> 7B4<
R/W *	5C4< 6C4>
RESET *	4B1<> 6C4<>
RMC *	5C4<> 6D4<>
RXD	5C1> 6A4< 7B4<
SCK	4C4<> 6B4<> 7B4<
SIZ0	5C4<> 6D4<>
SIZ1	5C4<> 6C4<>
T2CLK	4B4> 6B4< 7C4<
TPU <15..0>	4C4<> 6C4<> 7C4<
TSC	4B1> 6D1<
TXD	5C1<> 6B4<> 7B4<
VFPE16K	4A4> 6B1<
VFPE48K	5B1> 6B1<
VRH	3B4> 6B1<
VRL	3B4> 6B1<
VSTBY	4B1> 6C1<

DWG. NO. 63ASE90427W

REV: A

SIGNAL CROSS REFERENCES

SIZE		DWG. NO.	REV:
A	GEDTTL: BOARD GEDABV: MPBF333C	63ASE90427W	A
LAST_MODIFIED=Tue Jun 21 18:40:01 1994		SHEET 8 OF 8	