Tracy Losh

SYSTEMS
ENGINEERING LABORATORIES

TECHNICAL MANUAL

Synchronous Communications Modem Interface Unit

Volume 1 of 2

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Synchronous Communications Modem Interface Unit

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LIST OF EFFECTIVE PAGES

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LIST OF RELATED PUBLICATIONS

The following publications contain information not included in this manual but necessary for a complete understanding of the Synchronous Communications Modem Interface. Only those manuals pertaining to the type of computer used in the system are applicable.

Publication Title	Publication Number
Technical Manual - SYSTEMS 810A Purpose Computer	303-095000
Design Manual - Input/Output Interface SYSTEMS 810A Computer	310-095003
Reference Manual - SYSTEMS 810A General Purpose Computer	301-095049
Operator Manual - SYSTEMS 810A/810B Computer/Peripheral	302-095064
Technical Manual - SYSTEMS 810B General Purpose Computer	303-095019
Design Manual - SYSTEMS 810B Input/Output Interface	310-095117
Reference Manual - SYSTEMS 810B General Purpose Computer	301-095118
Operator Manual - SYSTEMS 840A/840MP Computer/Peripheral	302-095051
Technical Manual - SYSTEMS 840 Multiprocessor Computer System	303-095017
Design Manual - SYSTEMS 840MP Input/ Output Interface	310-095097
Reference Manual - SYSTEMS 840 Multiprocessor Computer System	301-095098

SECTION I

GENERAL DESCRIPTION

1-1 INTRODUCTION

1-2 This manual contains information pertaining to the installation, operation and maintenance of the SYSTEMS Synchronous Communications Modern Interface Unit designed and manufactured by SYSTEMS Engineering Laboratories, Fort Lauderdale, Florida. The unit and its associated equipment are shown in figure 1-1.

1-3 This manual contains or references all information required to install, checkout, operate, calibrate, adjust and repair the unit, and consists of the following sections:

Volume 1

a. Section I - General Description

b. Section II - Operation and Programming

c. Section III - Theory of Operation

d. Section IV - Installation and Maintenance

e. Section V - Performance Testing and Failure Analysis

Volume 2

a. Section VI - Assemblies and Circuit Cards

b. Section VII - Drawings

1-4 The manuals listed in the List of Related Publications in the front matter support the information contained in this manual.

1-5 PHYSICAL DESCRIPTION

1-6 The SYSTEMS Synchronous Communications Interface Unit (SCMIU) may, depending upon options, be packaged in a single or double micrologic swing plane assembly.

1-7 Card/cable connectors are used to connect all external signal cables to the interface unit. All interconnections with the computer and data modem are made through the I/O connector panel.

1-8 Solid state circuitry is employed throughout the unit. All circuits are assembled on printed circuit cards made of epoxy glass fiber. Several circuits are generally included on each printed circuit card. All circuit wiring to the mating connector is accomplished by using wire-wrap techniques. The circuit cards plug into the connectors on the swing plane and require no special tools or extractors for removal.

1-9 FUNCTIONAL DESCRIPTION

1-10 The SYSTEMS Synchronous Communications Modem Interface Unit contains the logic circuits required to interface a SYSTEMS 800 Series Computer (SYSTEMS 810A, 810B, 840A, or 840MP) with a synchronous data moderm designed to meet EIA (Electronic Industries Association) Standard RS-232-B. Figure I-2 shows a simplified block diagram of a typical system utilizing a communications modem interface unit.

1-11 The communications modem interface unit performs three basic functions in the system illustrated:

a. I/O Control- The interface unit contains the unit I/O sync and unit decode logic circuits which control the flow of data between the computer and the data modem. Also included are timing and control circuits which are directly related to the operation and control of the data modem.

b. Format Conversion - The interface unit contains serial-to-parallel converter for converting data being transferred to the computer, and a parallel-to-serial converter for converting the data output from the computer.

c. Logic Level Conversion - The interface unit contains transmit circuits which convert the micrologic levels used by the computer to the bipolar levels used by the data modem, (current switch is offered as an optional feature). Similarly, receive circutis are employed to convert the bipolar signals from the data modem to the micrologic levels for the computer.

1-12 POWER SUPPLY

1-13 The SYSTEMS 240-000-00 power supply chassis is designed to accommodate from one to four power supply modules. Depending on the overall system requirements, either the 240-000-03 or 240-000-04 power supply modules may be used. These power supply modules are adjustable from 3.2 to 7.0 volts.

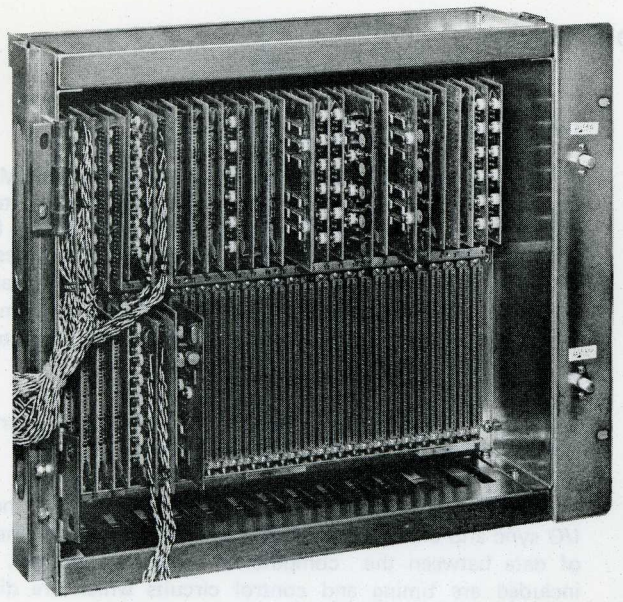
1-14 Refer to the Specifications and Leading Particulars for additional details, and to Section IV for power supply adjustment procedures.

1-15 OPTIONS

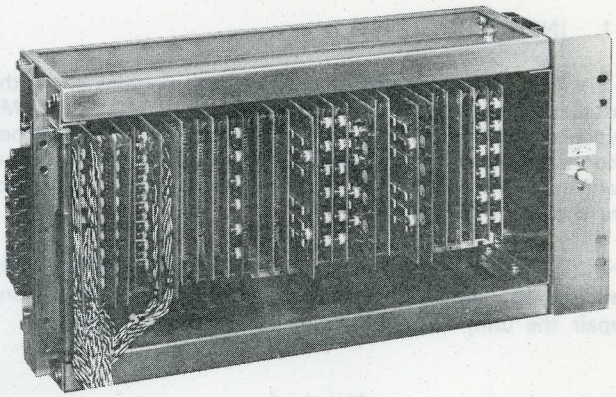
1-16 Table 1-1 lists the options that are available for the Synchronous Communications Modern Interface Unit.

1-17 SPECIFICATIONS AND LEADING PARTICULARS

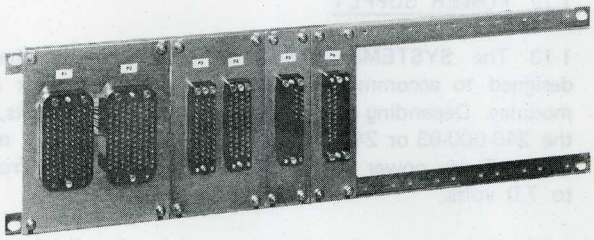
1-18 Refer to Tables 1-2, 1-3, and 1-4 for specifications and leading particulars concerning the SCMIU, 240-000-04 Power Supply and 240-000-03 Power Supply, respectively.



N6370



N6372



N6371

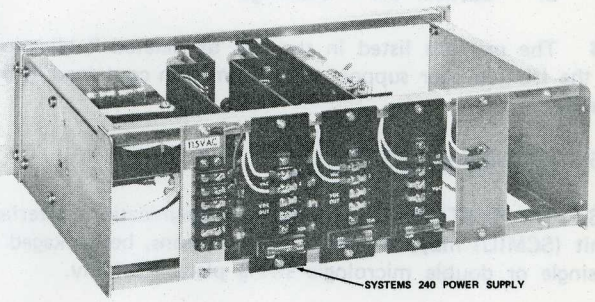


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Figure 1-1 Synchronous Communications Modem Interface

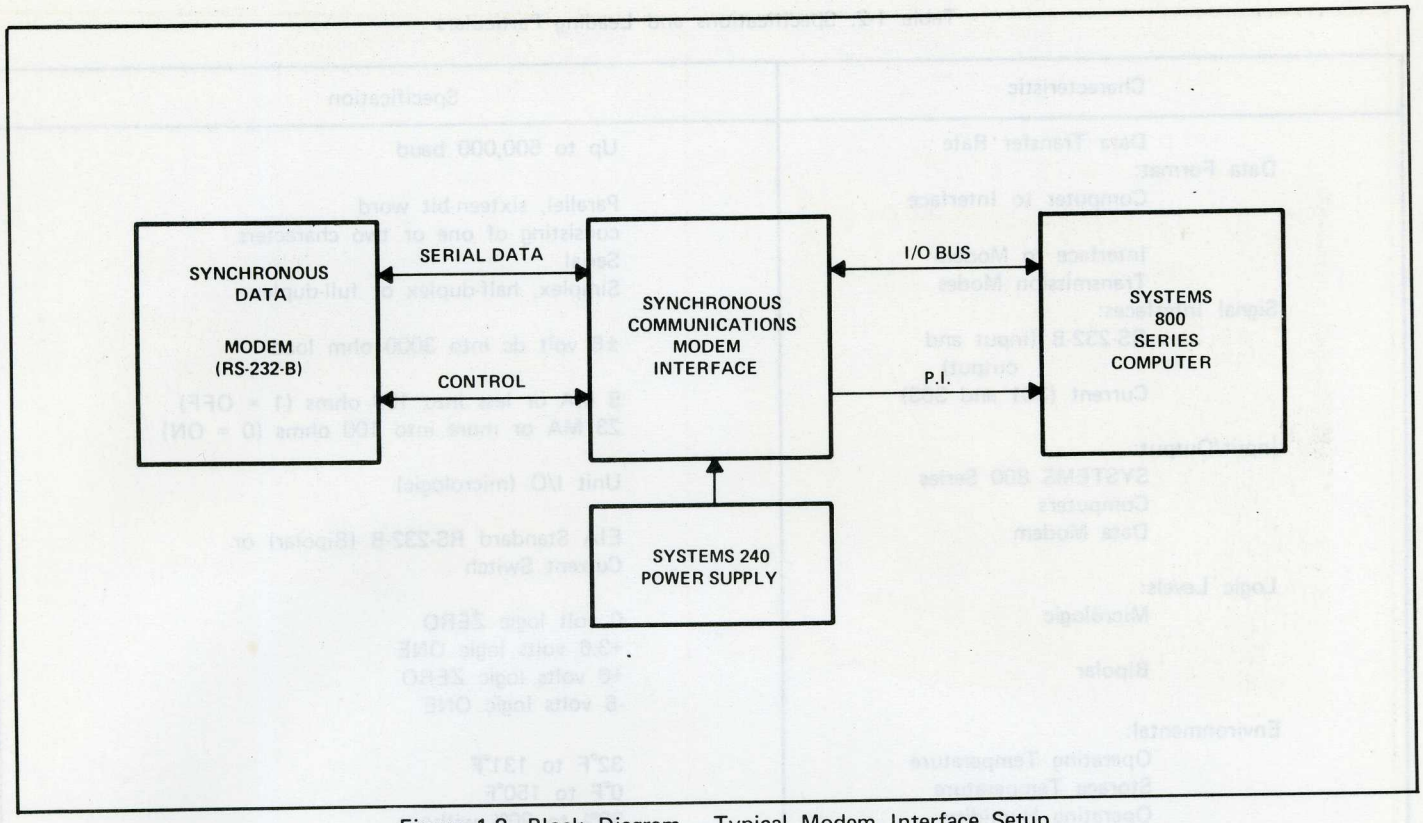


Figure 1-2. Block Diagram - Typical Modem Interface Setup

Table 1-1. Model Numbers and Options

Model #'s Options	Description
711631	Simplex transmission unit for 810A/B
711632	Simplex Receive Unit for 810A/B
711633	Duplex Unit for 810A/B
741631	Simplex transmission unit for 840MP
741632	Simplex Receive Unit for 840MP
741633	Duplex Unit for 840MP
* 7x163x-001	Even Block Parity Generation & checking
* 7x163x-002	Odd Block Parity Generation & checking
** 7x163x-010	LSB first transmission & reception
** 7x163x-020	MSB first transmission & reception
* 7x163x-100	Block Transfer Control Interface (BTCI)
* 7x163x-200	Current Output for Bell 300 Series Modems
* 7x163x-004	Auto-Dial Option, requires Model 711610, 711612, 741610 or 741612 as prerequisite
* 7x162x-040	Clock Option - For Modems requiring External
* 7x163x-400	Clock for synchronous operation
	Special
	* These options may be combined by adding the suffixes, that is Odd Block Parity, LSB first transmission with BTCI would be 7x161x-112
	** One of these two options must be specified in all cases

Table 1-2. Specifications and Leading Particulars

Characteristic	Specification
Data Transfer Rate	Up to 500,000 baud
Data Format:	
Computer to Interface	Parallel, sixteen-bit word consisting of one or two characters
Interface to Modem	Serial
Transmission Modes	Simplex, half-duplex or full-duplex
Signal Interfaces:	
RS-232-B (input and output)	±6 volt dc into 3000 ohm load
Current (301 and 303)	5 MA or less into 100 ohms (1 = OFF) 23 MA or more into 100 ohms (0 = ON)
Input/Output:	
SYSTEMS 800 Series Computers	Unit I/O (micrologic)
Data Modem	EIA Standard RS-232-B (Bipolar) or Current Switch
Logic Levels:	
Micrologic	0 volt logic ZERO +3.6 volts logic ONE
Bipolar	+6 volts logic ZERO -6 volts logic ONE
Environmental:	
Operating Temperature	32°F to 131°F
Storage Temperature	0°F to 150°F
Operating Humidity	30% to 90% without condensation
Storage Humidity	5% to 05% without condensation
AC Power Requirements	150 watts
Heat Dissipation	6000 BTU/HR
Physical Dimensions:	
Interface	
1 Row	9.0 Inches high, 19.0 inches wide, 7.5 inches deep
2 Row	15.5 inches high, 19.0 inches wide, 7.5 inches deep
Power Supply	5.25 inches high, 19.0 inches wide, 14.0 inches deep
I/O Panel	5.25 inches high, 19.0 inches wide 4.0 inches deep

Table 1-3. Specifications and Leading Particulars - SYSTEMS Model 240-000-04 Power Supply

Characteristic	Specification
Output Voltage	Variable, 3.2 to 7 volts
Output Current	10 amperes maximum
Load Regulation	50 mv maximum; 0 to 10 amperes at 5 volts output, nominal line
Line Regulation	100 millivolts total maximum from 100 to 135 volts ac, 10 amperes at 5 volts
Ripple	80 millivolts peak-to-peak; 120 Hz maximum at 10 amperes, 5 volts, nominal line
Overload Protection	Current limited at 14 amperes; protection for short circuit with adequate cooling
Overvoltage Protection	Crowbar protection at 7.5 volts nominal
Remote Sensing	None

Table 1-4. Specifications and Leading Particulars - SYSTEMS Model 240-000-03 Power Supply

Characteristic	Specification
Output Voltage	Variable, 3.2 volts to 7.0 volts
Output Current	5 amperes maximum
Load Regulation	30 millivolts maximum; 0 to 5 amperes at 5 volts output, nominal line
Line Regulation	100 millivolts total maximum from 100 to 135 volts ac, 5 amperes at 5 volts
Ripple	80 millivolts, peak-to-peak; 120 Hz maximum at 5 amperes, 5 volts nominal line
Overload Protection	Current limited at 8 amperes; protection for short circuit with adequate cooling
Overvoltage Protection	Crowbar protection at 7.5 volts nominal
Remote Sensing	None

SECTION II

OPERATION AND PROGRAMMING

2-1 INTRODUCTION

2-2 This section contains or references information pertaining to the operation and programming of the SYSTEMS Synchronous Communications Modem Interface Unit (SCMIU).

2-3 OPERATION

2-4 The communications moderm interface unit has no controls or indicators and is operated strictly under software control. The unit connects to the I/O bus of a SYSTEMS 800 Series Computer and operates in a manner similar to other peripheral units. A block transfer control interface (BTC) option is provided such that data transfers can be accomplished under BTC control without program intervention. Full duplex capability is available as an option provided that a suitable communications facility is available.

2-5 The SYSTEMS 800 Series Computer controls the unit through execution of the standard I/O instructions (CEU, TEU, AIP, AOP, MIP, MOP).

2-6 PROGRAMMING

2-7 All of the information required to program the Synchronous Communications Modem Interface Unit may be found in the applicable computer reference manual referenced in the list of related publications.

2-8 The following information is unique to the communications modem interface unit and is provided as a supplement to the referenced manuals.

2-9 In order to program the Synchronous Communications Modem Interface Unit (SCMIU) effectively, a basic understanding of the unit hardware is required. The following discussion is included to fulfill this requirement.

2-10 The SCMIU consists of three major assemblies; the computer interface unit, the transmit logic and the receive logic. The computer interface unit provides all the necessary timing and formatting to allow the computer to communicate with either the transmit logic or the receive logic. The transmit logic, on the other hand, provides the necessary timing and formatting to supply computer output data to the data modem unit. The receive logic receives timing and data from the data modem and converts it to a form compatible to the computer.

2-11 To establish a transmission path from the computer to the remote device, the computer program must first raise the Request To Send line to the modem and test the Clear To Send line until it is raised by the modem. This delay is normally 7.9 to 10.5 seconds in the 203A, the Request To Send line should be held in the raised state at all times to bypass this delay period for each transmission.

2-12 For synchronization purposes, the first two characters of each incoming message (after any period of nontransmission by the remote device) are assumed to be sync characters. The SCMIU is commanded to enter the sync mode by execution of a CEU instruction with bit 6 (BSM) of the CEU second word set. In the sync mode, the serial-to-parallel converter operates as an open-ended shift register. Incoming bits are shifted in and compared to the first of the two sync characters. When a comparison occurs, the unit assembles the next 8-bit character and compares it to the second sync character. If the characters compare, the unit switches automatically to the input mode and remains in this mode unitl again commanded to enter the sync mode, or commanded by execution of a CEU with bit 6 reset in the second word to turn the receive section off. This instruction is used in conjunction with receive parity. A priority interrupt signal, also generated, may be utilized by the program, provided an external interrupt level is available. If the second character does not compare with the second sync character, the unit switches back and begins looking for the first sync character again. Definition of the two sync characters is accomplished by connecting jumpers on the printed circuit boards. This permits selection of any desired sync pattern.

2-13 In the input mode, incoming data bits are assembled into 8-bit characters in the serial-to-parallel converter under control of the modem Receiver Signal Timing Element line and transferred to the input buffer. From the input buffer the character is transferred to the character assembly buffer where input words are assembled, either one or two characters per word as selected. Data input may be either by BTC control or by programmed input.

2-14 If the BTC transfer mode is utilized, the input word will be transferred directly into the SYSTEMS 800 Series Computer memory and will be stored in the computer memory location specified by the BTC current word address register.

2-15 Priority interrupt logic may be utilized for programmed single-word transfers if desired. This might be useful, for example, to input data if the BTC is being utilized for data output. When an input word has been assembled in the assembly buffer, a priority interrupt signal is generated. When this signal is connected to the input interrupt level (either the standard input level or an external level), the interrupt signal will notify the computer that a word is ready for input. Execution of an input instruction (AIP/MIP), addressing the unit by the computer program, will cause the word to be transferred into the computer.

2-16 In the receive mode with BTC operation,(after input of the final word in the block) the word count complete from

the BTC automatically will turn off the data receive section after the next character(parity) has been received. The parity character and parity status will be held until either an input of the parity character, performing a test of the parity condition, or an enter-sync mode command is received. In the receive mode of operation, after the final word in the block has been input , a CEU command with bit 6 reset will turn off the data receive section and allow the next input interrupt to signal the computer that the parity character has been received. This interrupt will be reset by either inputting the parity character, testing for its error condition using a TEU with bit 5 set; or an enter-sync mode command is received.

2-17 As each incoming character is transferred into the input buffer, all ONE bits in the character cause the flip-flops in the corresponding positions in the parity character register to toggle (switch states). ZERO's do not affect the register flip flop. For example, even parity would be as follows:

11101001 Previous state of parity character register
10110111 New incoming character
01011110 New state of parity character register

This is equivalent to a logical exclusive OR of the two characters.

2-18 If the transmitting device transmitted a block parity character at the end of the message, then the state of the parity character register flip-flops should all be reset (ZERO's) after this character is received. If this is not the case, then a transmission error has occurred. The reset state of the register can be tested at any time by execution of a TEU instruction with bit 5 set. The TEU will skip if no error occurred. For devices that transmit the ONE's complement of the exclusive OR parity check character, the parity character register flip-flops should all be set (ONE's) after this character is received.

2-19 Data output from the SYSTEMS 800 Series Computer to the remote device through the data modem is accomplished by either programmed single-word transfer or under BTC control. Under programmed transfers, execution of an output instruction (AOP/MOP) addressing the unit by the computer program will cause one word to be transferred from the computer into the character disassembly buffer. For BTC transfers, the word is transferred by the BTC and BTCI logic.

2-20 The word is disassembled according to the selected mode (one or two characters per word) and the character is transferred to the parallel-to-serial converter when the converter is ready. The character is shifted out of the converter serially to the modem transmitter under control of the Transmitter Signal Element Timing line from the modem.

2-21 If BTC is utilized for the output block transfer, the BTC and BTCI logic fetches another word from the computer memory when the character disassembly buffer is emptied. If program trasfers are utilized, a priority interrupt signal is generated when the buffer is emptied. When this signal has been connected to the output interrupt level (either the standard output level or an external level), the interrupt signal will notify the computer that the buffer is ready for another character. As output characters are transferred into the parallel-to-serial converter, a block parity character is generated in a manner identical to that previously described under character input. If block parity transmission is enabled, and the BTC is utilized for block output, then this character will be transmitted after both characters in the last word have been transmitted.

2-22 Provisions are made for data block parity error generation on an output. A block parity character is formed on each data block (including each of the two sync character) in a manner identical to the LRCC character on magnetic tape systems. This amounts to a column-wise parity generation on each of the eight bits of the characters in the output data block. This parity character is formed in a 8-bit flip-flop register, which is cleared to ZERO (reset) for even parity or (set) for odd parity when the unit switches to the sync mode. The following are some brief programs which can be used as examples for typical routines.

2-23 TRANSMIT PROGRAM

2-24 This program, as shown in table 2-I, will transmit six 8-bit characters in the word mode with parity generation.

2-25 RECEIVE PROGRAM

2-26 This program will receive six 8-bit characters in a word mode and check parity. If parity error is received, it will halt at location X; if no parity error is received, it will halt at location Y. (Refer to table 2-2).

2-27 TRANSMIT AND RECEIVE DATA FORMAT

2-28 The data format used for the serial transmit and receive data is illustrated in figure 2-1. Two 8-bit sync words are used to mark the start of a data frame. These sync words are followed by a specific number of data characters, each containing 8 bits. The length of the data frame is specified by the user. Refer to figures 2-2, 2-3, 2-4, and 2-5.

2-29 SYNC WORDS

2-30 The communications modem interface is normally provided with the jumper card (4A) wired to detect the following sync patterns:

Sync Word #I 01010101
Sync Word #2 00110010

2-31 However, the sync patterns may be rewired to meet the user's specification by changing the jumpers on the two jumper cards.

2-32 CEU SECOND WORD FORMAT

2-33 The function codes for the communications modem interface unit are defined in table 2-3. These codes are contained in the second word of the CEU instruction. Refer to the appropriate computer reference manual for the SYSTEMS 800 Series Computer first word format for all I/O instructions.

2-34 TEU SECOND WORD FORMAT

2-35 The test codes for the communications modem interface unit are defined in table 2-4. These test codes are contained in the second word of the TEU instruction. Refer to the appropriate computer reference manual for the SYSTEMS 800 Series Computer first word format for all I/O instructions.

Table 2-1. Transmit Program

Instruction	Address	Remarks
CEU	'43,W	
DATA	'4460	Set Request to Send, Terminal Ready, Word Mode and Parity
TEU	'43	
DATA	'40000	Wait for Clear to Send
BRU	*-2	
MOP	'43,W	
DATA		First and Second Sync Character
MOP	'43,W	
DATA		First 2 Data Characters
MOP	'43,W	
DATA		Second 2 Data Characters
MOP	'43,W	
DATA		Third Set of 2 Data Characters
HLT		
Parity is automatically generated and transmitted after the last data character.		

Table 2-2. Receive Program

Instruction	Address	Remarks
CEU	'43,W	
DATA	'1460	
MIP	'43,W	
DATA		First 2 Data Characters
MIP	'43,W	
DATA		Second 2 Data Characters
MIP	'43,W	
DATA		Third Set of 2 Data Characters
CEU	'43,W	
DATA	0	Stop Receive
AIP	'43,W	Input Parity Character
TEU	'43	
DATA	'2000	
X HLT		Error
Y HLT		No Error

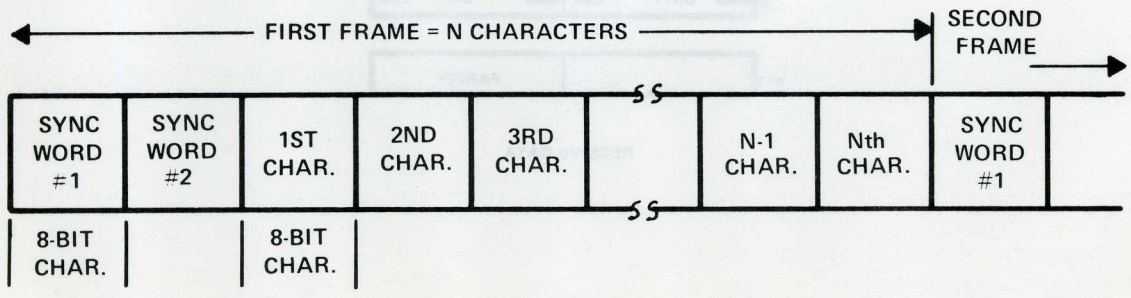


Figure 2-1. Data Format Transmit and Receive

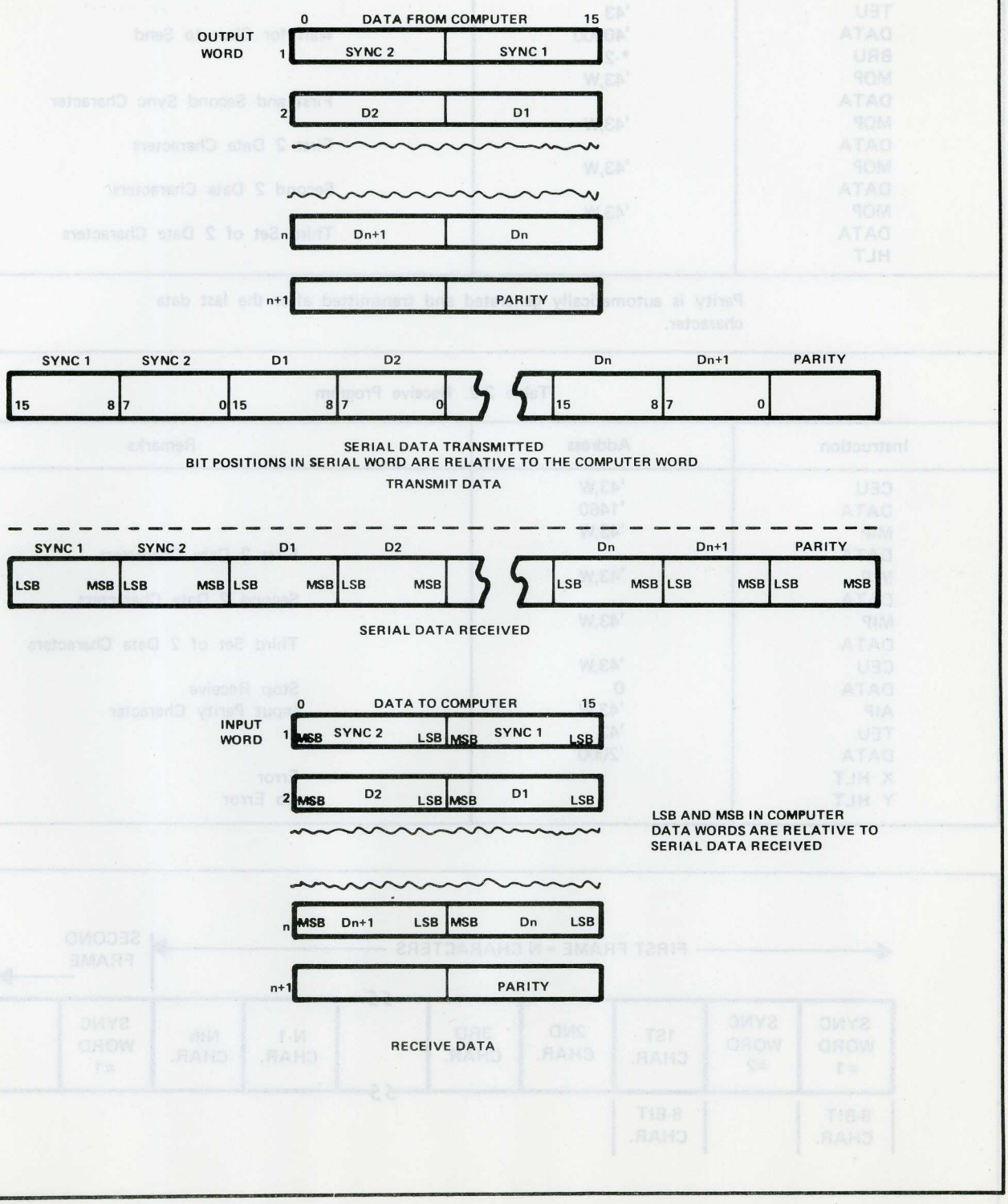


Figure 2-2. DATA FORMAT Word Mode LSB Transmitted/Recieved First

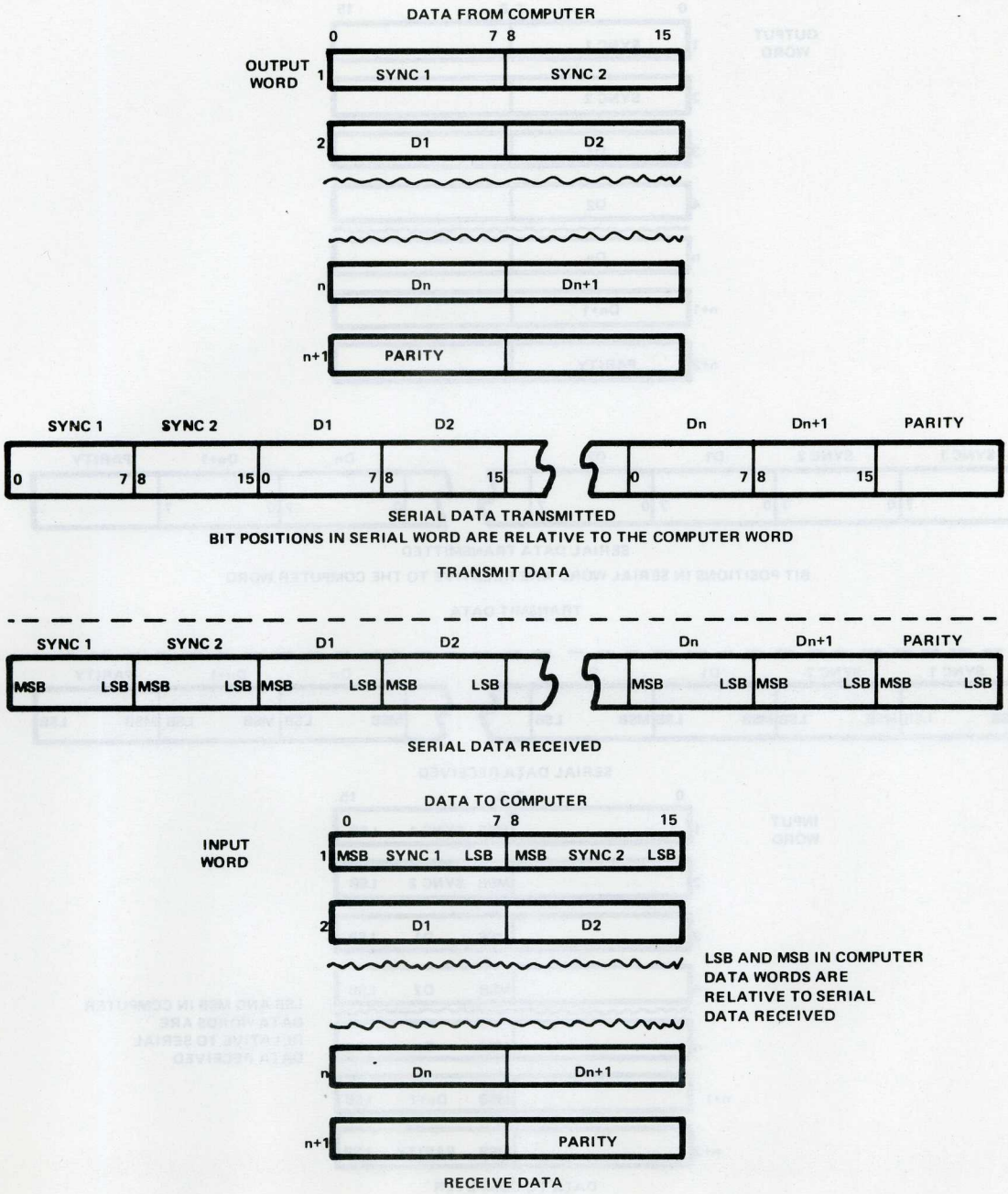


Figure 2-3. DATA FORMAT Word Mode MSB Transmitted/Received First

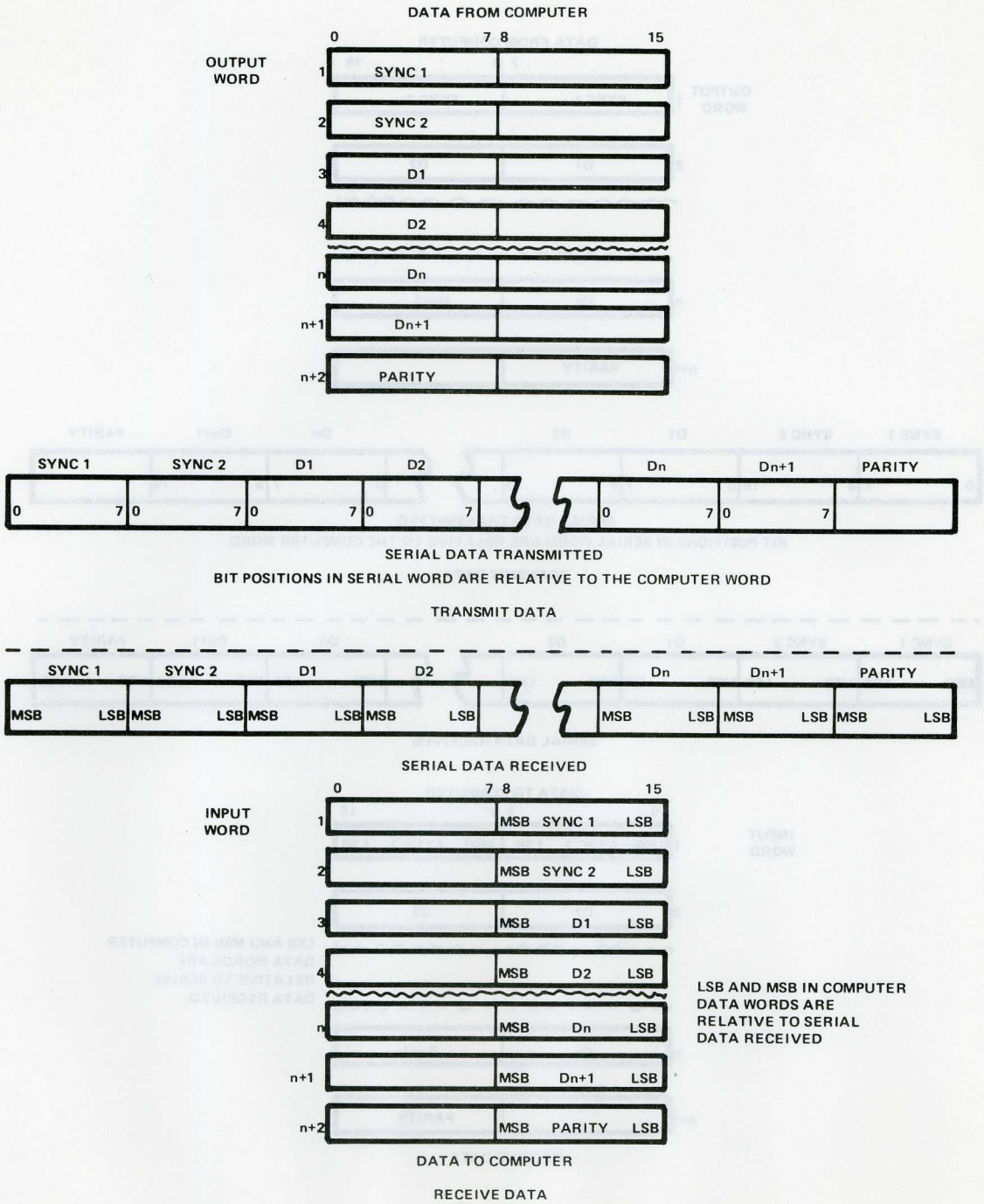


Figure 2-4. DATA FORMAT Character Mode MSB Transmitted/Received First

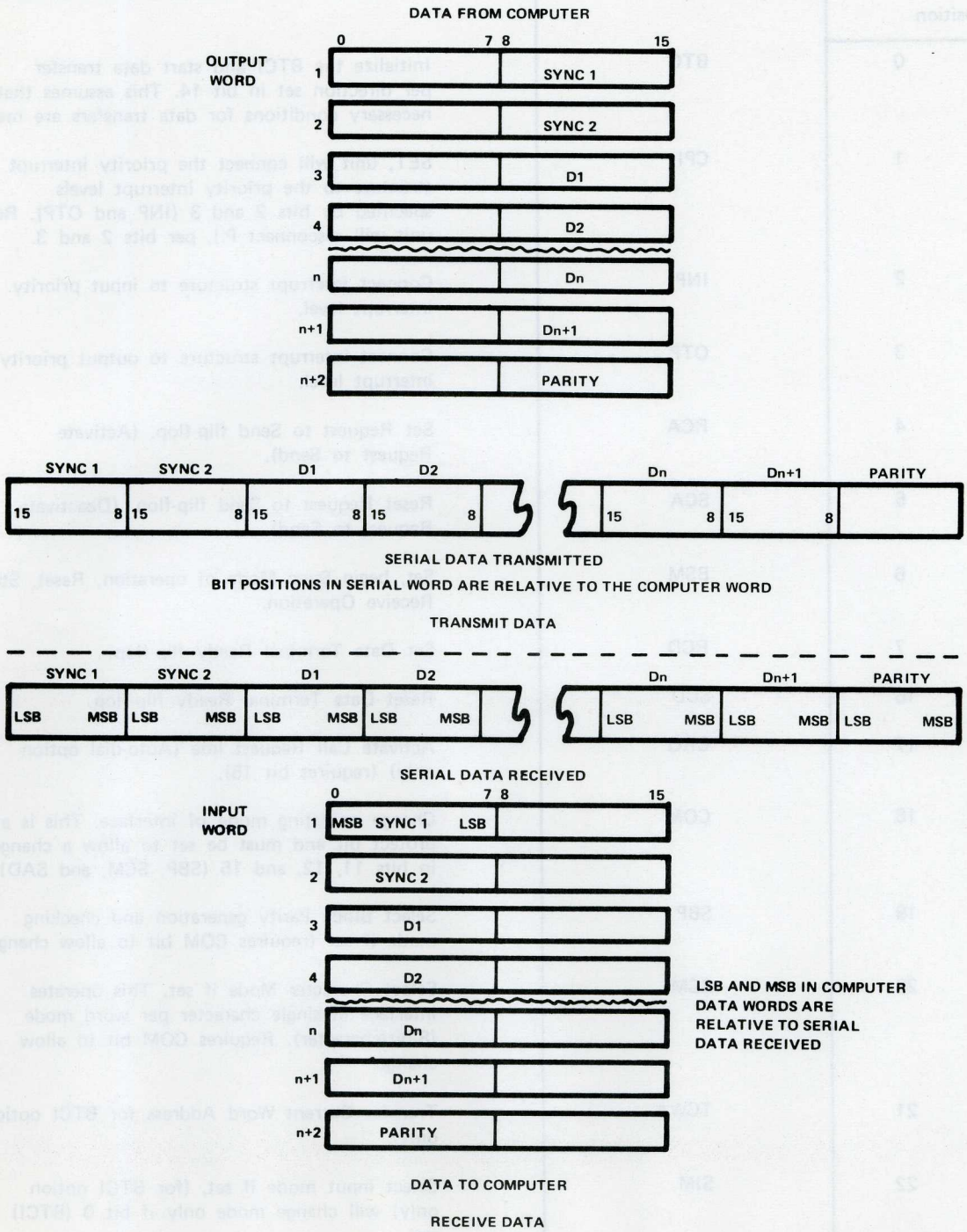


Figure 2-5. DATA FORMAT Character Mode LSB Transmitted/Recieved First

Table 2-3. CEU Second Word Format (SYSTEMS 810/840 Series Computer)

810/840 Bit Position		Mnemonic	Function
0	0	BTC	Initialize the BTCI and start data transfer per direction set in bit 14. This assumes that necessary conditions for data transfers are met.
1	1	CPI	SET, unit will connect the priority interrupt structure to the priority interrupt levels specified by bits 2 and 3 (INP and OTP). Reset, unit will disconnect P.I. per bits 2 and 3.
2	2	INP	Connect interrupt structure to input priority interrupt level.
3	3	OTP	Connect interrupt structure to output priority interrupt level.
4	4	RCA	Set Request to Send flip-flop. (Activate Request to Send).
5	5	SCA	Reset Request to Send flip-flop. (Deactivate Request to Send).
6	6	BSM	Set, begin Sync Mode of operation, Reset, Stop Receive Operation.
7	7	RCD	Set Data Terminal Ready flip-flop.
8	16	SCD	Reset Data Terminal Ready flip-flop.
9	17	CRQ	Activate Call Request line (Auto-dial option only) (requires bit 15).
10	18	COM	Change operating mode of interface. This is a protect bit and must be set to allow a change in bits 11, 12, and 15 (SBP, SCM, and SAD).
11	19	SBP	Select Block Parity generation and checking mode if set (requires COM bit to allow change).
12	20	SCM	Select Character Mode if set. This operates interface in single character per word mode (8-bit/character). Requires COM bit to allow change.
13	21	TCWA	Transfer Current Word Address for BTCI option only.
14	22	SIM	Select input mode if set, (for BTCI option only) will change mode only if bit 0 (BTCI) is set.
15	23	SAD	Select Auto-Dial Mode if set. (Requires COM bit to allow change). This places interface in Auto-Dial mode to allow communication to dialing mechanism.

2-36 PRIORITY INTERRUPT

2-37 The Communications Synchronous Modem Interface Unit is equipped with the standard input and output interrupt lines. However, there are several other interrupt lines that are utilized in special cases (refer to table 2-5).

2-38 The CSMIU has provisions for generating priority interrupts from souces other than the standard I/O signals. These priority interrupts are as follows:

a. Unit in Sync.

b. Data Set Ready (SCC)

c. Data Set is Clear to Send (SCB)

d. Data Carrier Detector (SCF)

e. Data Modulation Detector (SCG)

f. Ring Indicator

2-39 The four lines SCC, SCB, SCF AND SCG are combined in a logical inclusive OR function so that loss of any condition by the data modem will cause a priority interrupt signal to be generated.

2-40 The Sync signal from the data modem is connected to a special priority interrupt level as is the Ringing Indicator signal.

Table 2-4. TEU Second Word Format (SYSTEMS 810/840 Series Computer)

810/840 Bit Position		Mnemonic	Function
0	0	SCC	Skip if Data Set Ready
1	1	SCB	Skip if Data Set is clear to Send
2	2	SCF	Skip if Data Carrier Detector line is true.
3	3	SCG	Skip if Data Modulation Detector line is true.
4	4	SCE	Skip if Ring Indicator line is true.
5	5	SNE	Skip if no block error was detected in last transmission.
6	6	SPWI	Skip if Power Indicator line in Auto-Dial is true. (Auto-Dial option).
7	7	SDSS	Skip if Data Set is in Data Mode (Auto-Dial option).
8	16	SDLR	Skip if Data line is unoccupied (Auto-Dial option).
9	17	SAC	Skip if Abandon Call and Reentry line is in off condition. (Auto-Dial option).

Table 2-5. Priority Interrupt

Connector P5 Pin Number	Standard	Non-Standard
101	Input — Incorporated in the Standard	Input (Note 1).
102	Output — I/O cable	Output (Note 1).
103		Unit in Sync signal.
104	Interrupt will occur if any of these conditions are not true	a. Data Set Ready (SCC).
		b. Data Set is Clear to Send (SCB).
		c. Data Carrier Detector line (SCF).
		d. Data Modulation Detector line (SCG).
105		Ring Indicator
106		e. BTC End of Block

Note 1. The input and output interrupts (standard) are controlled by the CEU instruction. The non-standards are not.

SECTION III

THEORY OF OPERATION

3-1 INTRODUCTION

3-2 This section contains a general and a detailed theory of operation for the SYSTEMS Synchronous Communications Modem Interface Unit. Refer to Section VII for the logic diagrams referenced in the detailed theory of operation and to Section VI for schematic and assembly drawings of the individual circuit cards. Functional descriptions of each circuit card may be found in Section VI. A thorough understanding of the circuit card operation is necessary for a complete understanding of the detailed theory presented in this section.

3-3 A complete list of primary signals pertaining to the detailed logic in this manual is provided at the end of this section in a signal glossary. It would be advantageous for the reader to familiarize himself with the signal mnemonics and descriptions of these signals before advancing into the detailed theory.

3-4 GENERAL THEORY

3-5 The Synchronous Communications Modem Interface Unit is used to provide a link between the computer and the data modem. The unit consists of 1-or 2-row logic module, I/O panel, power supply and associated cables.

3-6 The data transfer rate is determined by the modem, since both the transmit and receive clock are supplied by the modem, (except when employing the external clock option).

3-7 High-speed logic elements are utilized throughout in the construction of the unit so that transmission rates up to 500,000 baud are possible with the unit.

3-8 The interface unit contains transmit circuits that convert the micrologic levels used by the computer to the bipolar levels used by the data modem. Similarly, receive circuits are employed to convert the bipolar signals from the data modem to the micrologic levels for the computer. Refer to programming, in Section II, for additional operational characteristics.

3-9 MODEM INTERFACE SIGNALS

3-10 The following paragraphs provide a brief functional description of the signal lines between the communications modem interface and the data modem as defined by EIA standard RS-232-B as application to the unit.

3-11 Transmitted Data (Circuit BA)

3-12 Signals on the Transmitted Data lines are generated by the communication modem interface. This line is connected to the transmit section of the data modem to transmit data to the remote data processing terminal equipment. The communications modem interface holds the Transmitted Data line in a marking condition during any time interval between characters or words, or at such times that no signals are being transmitted.

3-13 Received Data (Circuit BB)

3-14 The signals on the Receive Data line are generated by the receive section of the data modem in response to data signals from the remote data processing terminal equipment. The signal condition, either mark or space, is held for the total duration of the signal element.

3-15 Request To Send (Circuit CA)

3-16 The signals on the Request To Send line are generated by the communications modem interface unit to condition the local data modem to transmit. For example: if the data modem has a modulator, the carrier signal is turned on when the CA signal is on. The on condition of this circuit is maintained as long as the interface unit has data ready or is actually transmitting data to the data modem, and is controlled by a CEU instruction from the computer.

3-17 Clear To Send (Circuit CB)

3-18 The signals on the Clear To Send line are generated by the local data modem to indicate that it is prepared to transmit data. The on condition of this signal is the response to the Request To Send signal from the communications modem interface. When the Request To Send signal is turned off, the Clear To Send signal is removed.

3-19 Data Set Ready (Circuit CC)

3-20 The signals on the Data Set Ready line are generated by the local data modem to indicate that it is ready to operate. The off condition indicates one of the following:

a. Any abnormal or test condition that disables or impairs any normal function associated with the class of service being furnished.

b. That the communications channel is switched to an alternate means of communication (for example, alternate voice telephone).

c. That the local data modem is not connected to a communications channel(that is, that data set is "on hook").

3-21 The Data Set Ready line is normally in the on condition except as noted above. This circuit is used to indicate the status of the local data modem. The on condition of this circuit is not to be interpreted either as an indication that the

communication channel has been established to a remote station or the status of any remote station or equipment.

3-22 Data Terminal Ready (Circuit CD)

3-23 The signals on the Data Terminal Ready line are generated by the SCMIU. The on condition of this circuit causes the data modem to be connected to the communications channel and is generated by a CEU instruction.

3-24 Ring Indicator (Circuit CE)

3-25 Signals on this circuit indicate that a ringing singnal is being received from a remote station. This circuit is required for automatic answering of received calls. The ON condition indicates that a ringing signal is being received. The OFF condition is maintained at all other times.

3-26 Data Carrier Detector (Circuit CF)

3-27 The signals on the Data Carrier Detector line are generated by the local data modem as an indication that the data carrier is being received from the remote data modem. When the data carrier is lost because the transmitting signal is turned off or because of a fault condition, the off condition of the Data Carrier Detector will follow after an appropriate guard time delay.

3-28 Data Modulation Detector (Circuit CG)

3-29 The signals on the Data Modulation Detector line are generated by the local data modem and are used as an indication of proper demodulation of the data carrier in the signal converter.

3-30 An on condition is maintained only when the data carrier is being properly demodulated. When the demodulated data signal indicates that the degree of modulation has been reduced to a point below a reasonable preset threshold, the off condition occurs before the next signal element.

3-31 The on condition indicates proper demodulation of the received data carrier signal. The off condition indicates that a possible error has been detected in the data communication equipment. It may, in some instances, be used to call automatically for a retransmission of the previously transmitted data signal.

3-32 Transmitted Signal Element Timing (Circuit DB)

3-33 The Transmitted Signal Element Timing signals are generated by the data modem to provide the modem interface with signal element timing information. This waveform has a 50/50 duty cycle and is used to define the transmit data bit rate. The transitions between signal elements on the Transmitted Data line nominally occur at the same time as the transitions on the circuit DB.

3-34 Receiver Signal Element Timing (Circuit DD)

3-35 The Receiver Signal Element Timing signals are generaged by the data modem to provide the modem interface with signal element timing information. This waveform has a 50/50 duty cycle and is used to define the receive data bit rate. The transitions nominally indicate the center of each signal element on the Receive Data line.

3-36 Signal Ground (Circuit AB)

3-37 The signal ground conductor is connected to the ground bus in the communications modem interface and establishes a commom ground reference potential for all circuits in the interface unit except circuit AA (protective ground).

3-38 Protective Ground (Circuit AA)

3-39 The protective ground conductor is bounded to the frame of the 2-row micrologic swing plane assembly containing the communications modem interface logic.

3-40 AUTO DIAL INTERFACE SIGNALS

3-41 The following paragraphs provide brief functional descriptions of the signal lines between the SCMIU and the auto-dial mechanism as applicable to the unit.

3-42 Call Request (CRQ)

3-43 The ON condition indicates that the SCMIU is initiating a call.

3-44 Digit Leads (NBI, NB2, NB4, NB8)

3-45 Signals are presented by the interface on the four leads in parallel giving a 4-bit binary representation of the digit to be dialed. NB8 is the most significant bit in the binary coded digit.

3-46 Digit Present (DPR)

3-47 The ON condition indicates that the states of the digit leads may be read by the Automatic Calling Unit (ACU).

3-48 Present Next Digit (PND)

3-49 The ON condition indicates that the ACU is ready to receive a digit from the interface. (This is a signal from the ACU to the business machine).

3-50 Power Indication (PW)

3-51 The power indication lead is ON whenever power is available within the ACU. The ACU should be considered inoperative if the PWI lead is OFF. This is a signal from the ACU to the SCMIU.

3-52 Data Set Status (DSS)

3-53 This circuit is ON whenever the data set is in the data mode. This is a signal from the ACU to the SCMIU.

3-54 Data Line Occupied (DLO)

3-55 An ON indication is given whenever the telephone line associated with the ACU is in use. This is an indication that the ACU will ignore any request for service presented at a time when this lead is already ON. The lead will also be ON when

the ACU is in the test mode. This is a signal from the ACU to the SCMIU.

3-56 Abandon Call and Retry (ACR)

3-57 This circuit is associated with a timer that times out whenever a preset interval has elapsed between successive events in the calling procedure. When this lead comes ON it indicates that an event has not occurred within the desired time. This is a signal from the ACU to the SCMIU.

3-58 COMPUTER INSTRUCTIONS

3-59 The modem interface unit responds to three types of instructions from the computer. These instructions are: Test External Unit (TEU), Command External Unit (CEU), and Data Transfer Instructions (AIP, AOP, MIP, and MOP).

3-60 Command External Unit

3-61 The CEU instructions are used by the computer to command the SCMIU to perform specific functions. These functions are determined by specific function codes listed in Section II, table 2-3.

3-62 Test External Unit

3-63 The TEU instruction is used by the computer to test the status of the modem. The test functions are determined by the function codes listed in the table 2-4 Section II of this manual.

3-64 Data Transfer Instructions

3-65 The data transfer instructions are used by the computer to either input data from, or output date to the data modem through the communications modem interface.

3-66 Output Data. When the computer executes an output instruction (AOP or MOP), 16 bits of data are placed on the computer I/O bus. These 16 bits make up a word of data. The data from the I/O bus is then loaded into the output register under the control of the I/O sync logic. Once the data is loaded into the output buffer, the computer is released to perform other tasks. The transmit logic takes control of the data and generates a signal to load it into the parallel/serial converter. Shift pulses then shift the data from the parallel/serial (S/P) converter to the data modem as a serial wavetrain.

3-67 Input Data. Before the computer can input data from the SCMIU, sync must be established. A CEU instruction is executed by the computer to enable the sync circuits in the modem interface. Two sync words are used to mark the start of a data frame. These sync words each contain eight bits arranged in a unique pattern of ONE's and ZERO's. When the sync circuits are enabled and two sync words are received and recognized, the subsequent 8-bit characters of data are shifted into the serial/parallel (S/P) converter. When a complete 8-bit character has been shifted into the S/P converter, it is transferred to the input buffer.

3-68 The character is transferred from the input buffer to the character assembly buffer where inputs are assembled, either one or two characters. This is dependent on the mode selected, either word mode or character mode. An interrupt is generated to inform the computer that the unit has data ready to be transferred. In response to the interrupt, the computer execites an AIP or MIP instruction that causes the I/O sync logic to generate a Gate Data Out signal. This signal then enables a set of gates and cable drivers to gate the data from the input buffer to the computer by way of the I/O bus. Data input may be either by BTC control or by programmed input. If the BTC transfer mode is utilized the input data will be transferred directly into the computer memory by the BTC and BTCI logic, and will be stored in the computer memory location specified by the BTC current word address.

3-69 DETAILED THEORY

3-70 The SYSTEMS Communications Modem Interface is shown in the detailed block diagram, figure 3-1 and the logic on drawing group 130-100659-000 in Section VII.

3-71 The following is a functional description of commands,signals and responses between the computer and the SCMIU.

3-72 Instruction Sync (313)

3-73 nstruction Sync is used to allow the device to interrogate its device (unit) number lines, and in turn answer via the unit sync return line. The Instruction Sync line is present until the device answers.

3-74 Wait Flag (510)

3-75 This signal signifies that the instruction being executed contains the computer Wait Flag bit. The Wait Flag causes the device to inhibit answering by way of the unit sync return until it is ready to perform the desired instruction. The Wait Flag line is not used during a test instruciton. The line is present until the computer recognizes the unit sync return line and is ready to proceed with the instruction execution.

3-76 Input/Output (509)

3-77 This signal signifies the direction of transfer in conjunction with a data transfer instruction. The line is present for the duration of the instruction. A ONE indicates input, a ZERO indicates output.

3-78 Computer Data Accepted (513)

3-79 This signal signifies that the computer has accepted data from the device as the result of an AIP/MIP instruction. The signal presence is controlled by the mainframe I/O logic.

3-80 Data Transfer Instruction (310)

3-81 This signal signifies that a data transfer instruction (AOP, MOP, AIP, MIP0 is being executed, and is present for the duration of the instruction.

3-82 Command Instruction (312)

3-83 This signal signifies that a Command External Unit (CEU) instruction is being executed and is present for the duration

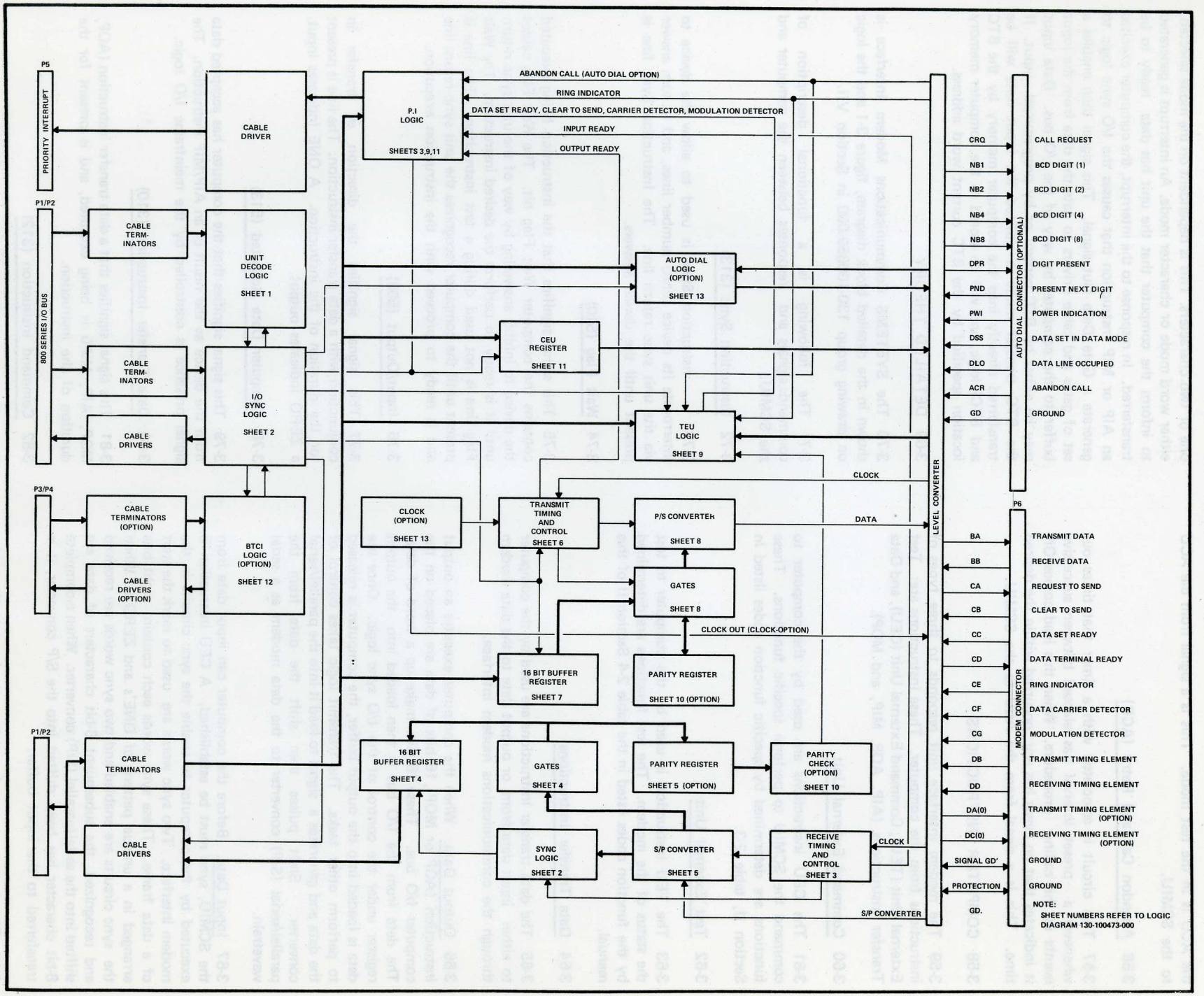


Figure 3-1. Detailed Block Diagram - Synchronous Communications Modem Interface (130-100659-000)

of the instruction. The second word of the instruction contains the function (operation) bits.

3-84 Clock (511)

3-85 The Clock line is formed by ORing the designated timing pulses together from the master computer clock.

3-86 Computer Data Here (512)

3-87 This signal signifies that the computer has recognized the Unit Sync Return line and the Test Return - if applicable and has proceeded into the execution cycle of the instruction. Computer Data Here is used to notify the unit that the data bits are present on the I/O bus and can be interrogated or loaded into the output register. The signal remains until the unit answers on its Unit Data Accepted line.

3-88 Test Instruction (311)

3-89 This signal signifies that a Test External Unit (TEU) instruction is being executed and is present for the duration of the instruction. The second word of the instruction contains the test code.

3-90 Master Clear (709)

3-91 The master clear line is activated by the CLEAR switch on the computer control panel and also by the initial condition buffer (ICB) when power is turned on. In the case of the CLEAR switch, the line is a dc level and remains activated as long as the switch is depressed. The ICB condition enables the master clear line for approximately one second.

3-92 Unit Test Return (710)

3-93 This signal signifies the status of the device after receipt of the Instruction Sync from the computer. If the device is capable of performing the required instruction, the Test Return line is enabled thus allowing the computer program a skip of the next instruction. The Test Return signal remains valid until the Instruction Sync signal is removed.

3-94 Unit Sync Return (711)

3-95 This signal signifies that the device has recognized the Instruction Sync signal. The signal remains until the computer removes the Instruction Sync signal.

3-96 Unit Data Accepted (712)

3-97 This signal signifies that the device has accepted the data word present on the I/O bus. In the case of the test instruction, it notifies the computer that the test return line is valid and can be interrogated. The signal remains until the Computer Date Here signal is removed.

3-98 UNIT DECODE

3-99 The logic for the unit decode is shown on the logic diagram 130-100659-000, sheet 1. The six unit select bits (decoding unit $43_{(8)}$ from the computer I/O bus are received through P1/P2. These bits are applied to a set of cable terminators, inverted and applied to AND gates 21A(1) and 21A(2). The output of both AND gates enables AND gate 22A(1) which generates the This Unit signal. The output of AND gate 22A(1) also pratially enables AND gate, 21A(3) which, when fully enabled through the Instruction Sync and the Data Transfer signals or the Command Instruction signal, generates the Enable (HENS and LENS) signal which is applied to AND gate 22A(7) and 22A(8) on sheet 2 (I/O sync logic). The output from 21A(3) partially enables AND gate 21A(4). This gate is fully enabled by a Low output from AND gate 22A(2) or 22A(3). AND gate 22A(2) is enabled by the Buffer Ready (BRDY) signal from the I/O logic, sheet 9 and the Data Transfer Instruction (DT) signal, while AND gate 22A(3) is enabled by the CI signal from the computer. The output from AND gate 21A(4) is designated Command or Instruction Ready (COMRDY) signal and triggers flip-flop 19A(1) on sheet 2, on its trailing edge.

3-100 I/O SYNC LOGIC

3-101 The detailed logic for the I/O sync logic is shown on drawing 130-100659-000, sheet 2. This logic provides the control gating of signals between the applicable SYSTEMS 800 Series Computer and the Synchronous Communications Modem Interface Unit. Instructions for the I/O system are provided by the following: Command Instructions (CEU), Data Transfer (Input) Instructions (AIP/MIP) and Data Transfer (Output) Instructions (AOP/MOP).

3-102 Command (CEU) and Data Transfer Instructions

3-103 When a CEU Instruction is decoded, the Command Ready (LICOMRDY) signal on sheet 2 provides a trigger input to flip-flop 19A(1). The flip-flop is triggered by the negative-going edge of the pulse. The Enable Sync (HENS) signal from the unit decode logic (sheet 1) supplies the Low dc reset input, while set steering is provided by the High reset output of flip-flop 19A(2). The Low set output of flip-flop 19A(1) is ORed through 22A(9) and generates the Unit Test Return signal through cable driver 28A(5). Flip-flop 19A(2) is triggered by the Computer Clock (T3T) signal and the Enable Sync (HENS) signal which is applied through AND gate 22A(7). The Wait Flag (WFL) signal supplies set steering while dc reset is supplied by the Input Line (LINP) signal, Enable Sync (LENS) signal Computer Data Accepted (LCDA) signal and the Output Line (OTP) signal plus the output from latch 22A(11) and 22A(12). The various signals are ANDed and ORed through AND gate 21A(6) and OR gate 21A(5) to supply the dc reset.

3-104 The setting of flip-flop 19A(2) is dependent on the set steering input provided by the condition of the Wait Flag (WFL) signal. If the signal is Low, the setting of flip-flop 19A(2) is inhibited. The High reset output is applied to the set steering input of flip-flop 19A(1), enabling it and supplying anoutput to AND gate 21A(14), partially enabling this gate. When this gate is fully enabled by the Data Transfer Instruction (HDT) signal and the Output Line (OTP) signal, latch 22A(12) and 22A(11) is set. This generates a Low output signal from latch 22A(11). It is ORed through 22A(13), inverted and constitutes the Gate Data Out (GDO) signal that is supplied to various destinations.

3-105 The computer responds with a Computer data Accepted (CDA) signal ORed through 21A(5), dc resetting flip-flop 19A(2) and simultaneously setting latch 22A(11) and 22A(12)

to its normal state. Whenever the output from latch 22A(11) is Low, gate 21A(6) is inhibited until the Computer Data Accepted signal has set the latch to its normal state. This partially enables the AND gate 21A(6) again.

3-106 The High set output from 19A(1) also partially enables AND gate 22A(10), which is fully enabled whenever the Wait Flag (WFL) signal is Low. This signal is ORed through 21A(15) and generates the Unit Sync Return signal through cable driver 28A(6).

3-107 The Unit Sync Return (USR) is also established whenever the reset output from 19A(2) is Low or a Low reset output signal from flip-flop 19A(5) is ORed through 21A(15).

3-108 This Unit selected (TUN) signal, Command Instruction (CI) signal and the Computer Data Here 1(CDH1) are applied to AND gate 21A(7) and transferred through various inverter and AND gating circuits to the trigger input of flip-flop 19A(3). AND gate 21A(13) is fully enabled whenever the reset output from flip-flop 13A(3) is High. Resetting of the flip-flop occurs with Computer Data Here 1 (CDH1) signal. The Low reset output signal from flip-flop 19A(3) is ORed through 21A(16) and generates the Unit Data Accepted signal through cable driver 28A(7).

3-109 Whenever AND gate 21A(13) is fully enabled, its Low output constitutes the Command to Unit Strobe (CUS) signal, which is applied to sheet 11, drawing 130-100659-000, to trigger the flip-flop 12A(7) and 19A(9). The High Command to Unit Strobe (CUS) signal is taken from the output of inverter 20A(11) and transferred to sheet 3 and 11, drawing 130-100659-000.

3-110 Data Transfer Instruction (DT) signal. This Unit Selected (TUN) signal and Computer Data Here 1 (CDH1) signal are applied to AND gate 21A(8) and transferred to flip-flop 19A(4) in a similar fashion as described in the preceding circuit. Its output is ORed through 21A(16) and also transferred to the computer by cable driver 28A(7). The Register Strobe (RS) signal is generated whenever AND gate 21A(12) is fully enabled. This signal is applied to sheet 11, drawing 130-100659-000.

3-111 AND gate 21A(9) is enabled by Computer Data Here 2 (CDH2) signal, Test Instruction (TIN) signal and This Unit Selected (TUN) signal. The output of this gate is applied to the trigger input of flip-flop 19A(6), through various inverters and through AND gate 21A(11), which is fully enabled by the reset output of this flip-flop. The reset output signal of flip-flop 19A(6) is transferred to OR gate 22A(9). Whenever this signal is Low, it generates the UTR signal to the computer through cable driver 28A(5). The output of AND gate 21A(9) is also ORed through 21A(16) and transferred to the computer (P1/P2) by cable driver 28A(7). Set steering to flip-flop 19A(6) is accomplished with the Test Skip Reply (TESKP) signal from the output of AND gate 22A(19), sheet 9, drawing 130-100659-000. Computer Data Here 2 (CDH2) supplies the dc reset to this flip-flop. This signal, when Low, will reset 19A(6).

3-112 Test Instruction (TIN) signal, Computer Clock 2 (T3T)signal and the High reset output from flip-flop 19A(5) enable AND gate 21A(10). The output is applied to trigger the flip-flop 19A(5). Whenever the reset output of this flip-flop is Low, a signal is generated through OR gate 21A(15) and generates USR to the computer through cable driver 28A(6). The Low Instruction Sync (INS) signal, dc resets flip-flop 19A(5).

3-113 PRIORITY INTERRUPT

3-114 Part of the logic for the priority interrupts is shown on drawing 130-100659-000 sheet 9. These include the following functions:

a. Data Set Ready (SCC) signal

b. Data Set is Clear To Send (SCB) signal

c. Data Carrier Detector (SCF) signal

d. Data Modulation Detector (SCG) signal

3-115 The four lines are combined in a logical inclusive OR function, so that loss of any condition by the modem will cause a priority interrupt signal to be generated. The ringing indicator line from the modem is connected to a special priority interrupt level. Refer to sheets 3 and 11 for additional priority interrupts.

3-116 Standard Interrupt

3-117 When the input and output interrupts are connected as the two standard interrupts, their outputs appear on pin 504 and 503 respectively on the unit I/O bus connector (P1/P2). In this configuration, these interrupts must be enabled by the computer before they can be used. A CEU instruction with bits 1, 2, and 3 of the CEU second word are used for this purpose. Bit 1 designates either a connect or disconnect function, and bits 2 and 3 select either the input and/or the output interrupt.

3-118 RECEIVE TIMING AND CONTROL LOGIC

3-119 The logic diagram for the receive and sync control circuits is shown on drawing 130-100659-000, sheet 3. Figure 3-2 shows a timing diagram of the signals associated with these circuits.

3-120 Begin Sync Mode

3-121 Before the computer can input data from the modem,it must execute a CEU instruction to this unit to enable the sync mode. Bit 6 of the CEU second word is used for this purpose. When the CEU instruction is executed, AND gate 5A(2) is enabled by the DB6 and CUS signals. The output of 5A(2) sets NOR latch 5A(3) - 14A(17) . When the latch is set, AND gate 5A(4) is enabled. The output from AND gate 5A(4) is inverted and applied to AND gate 14A(18).

3-122 Sync Mode

3-123 As the serial data is shifted into the S/P converter from the data modem, the bits are constantly compared to the jumpers on card 4A. This jumper card defines the two unique sync patterns that make up the sync words. When a comparison is made between the data and the jumpers on the card 4A, a true condition is generated at the output of 3A(5) and 3A(6).

DESCRIPTION	LINE SYMBOL	LOCATION
RECEIVE CLOCK	RCLK	5-7A(1)-18
BEGIN SYNC MODE	BSM	3-5A(3)-3
START SYNC LATCH	SSL	3-5A(3)-7
FIRST WORD SYNC	FWS	3-9A(28)-57
COMPARE FIRST WORD STROBE	COM1	3-14A(18)-77
SECOND WORD ENABLE	SWE	3-6A(10)-59
SECOND WORD SYNC	SWS	3-9A(26)-60
COMPARE SECOND WORD STROBE	COM2	3-3A(3)-21
SYNC	SYNC	3-5A(9)-36
RC1 FLIP-FLOP	RC1	3-12A(8)-45
RC2 FLIP-FLOP	RC2	3-12A(9)-61
RC4 FLIP-FLOP	RC4	3-12A(10)-59
RC8 FLIP-FLOP	RC8	3-12A(11)-73
ZERO DETECT	ODET	3-9A(20)-46
LOAD ENABLE	LDEN	3-6A(9)-61
LOAD STROBE	LDR	3-3A(1)-9
PARITY CHECK TEST LINE	PCKT	5-5A(12)-39
INPUT READY	IRDY	3-12A(12)-71
GATE DATA OUT	GDO	2-20A(15)-30
RECEIVE	BB	5-24A(8)-62

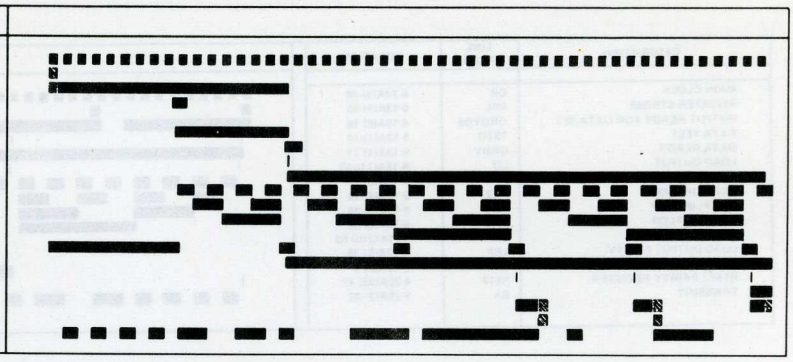


Figure 3-2. Timing Diagram-- Receive and Sync Control

3-124 This is applied to AND gate 14A(18), which was previously enabled by the CEU instruction. A pulse is generated and used to trigger flip-flop 6A(10) to the set state. When the flip-flop is set, the following occurs: (1) AND gate 14A(18) is inhibited, (2) the dc reset signal is removed from the counter register, (3) AND gate 14A(13) is inhibited, (4) and AND gate 3A(3) and 3A(4) are partially enabled.

3-125 When the dc reset signal is removed from the counter register, and AND gate 5A(5) is enabled, the counter is advanced one count for each received pulse. After eight counts, when the counter returns to zero, a ONE is generated on the output of AND gate 14A(14). This output is inverted and applied to AND gate 3A(1), 3A(2), 3A(3) and 3A(4). If, at this time, a comparison is found to exist between the data bits in the S/P converter and the jumper card 4A, then AND gate 3A(7) and 3A(8) will be enabled, the signal will be inverted and applied to AND gate 5A(8). The Second Word Sync(SWS) signal out of inverter 9A(26) is applied to AND gate 3A(3). AND gate 3A(3) is enabled and the timing pulse is gated to set NOR latch 5A(9) and 14A(15). If, however, a match does not exist; AND gate 3A(4) is enabled and resets flip-flop 6A(10). This will cause the unit to go back and search for the first word sync pattern that matches the jumpers on card 4A.

3-126 Assuming that two consecutive words are shifted into the P/S converter, and they match the jumpers on the card 4A,NOR latch 5A(9) and 14B(15) will be set. When this latch is set, the following will happen: (1) the dc reset level is removed from flip-flop 6A(9) and timing pulse RT3 triggers it to the reset state to generate the LDEN-pulse to enable the data from the S/P converter to be loaded into the input register on the next succeeding character, (2) latch 5A(3) and 14A(17) and flip-flop 6A(10) are reset to return the circuits to the initial condition.

3-127 Each time a Compare First Word Strobe (COM1) signal, a Compare Second Word Strobe (CM2) signal or a Load Input Register (LD2R) signal is generated, OR gate 3A(9) generates a Count Parity Register (CPAR) signal. It is applied to the trigger input of the flip-flops in the parity register, sheet 5. The output from gate 3A(2) also triggers flip-flop 12A(12). This generates the Input Ready signal that is transferred to the command register, sheet 11, and ANDed into 22A(22), partially enabling this gate. The reset output of flip-flop 19A(7) will fully enable 22A(22), applying a signal to the output interrupt on the computer bus.

3-128 Resetting of flip-flop 12(A)12 occurs with either the Gate Data Out (GDO) signal, the Reset Receive Parity(RRP) signal, the Begin Sync Mode (BSM) signal, or the Initial Condition signal.

3-129 The Compare Second Word strobe (COM2) signal from AND gate 3A(3) also triggers one-shot 7A(4) to generate a sync signal. This signal is transferred to connector P5, pin 103,203, by the cable driver 28A(16) to provide the In Sync Priority Interrupt Signal.

3-130 TRANSMIT TIMING AND CONTROL LOGIC

3-131 The logic for the transmit and test control is shown on drawing 130-100659-000, sheet 6.

3-132 Transmit Logic

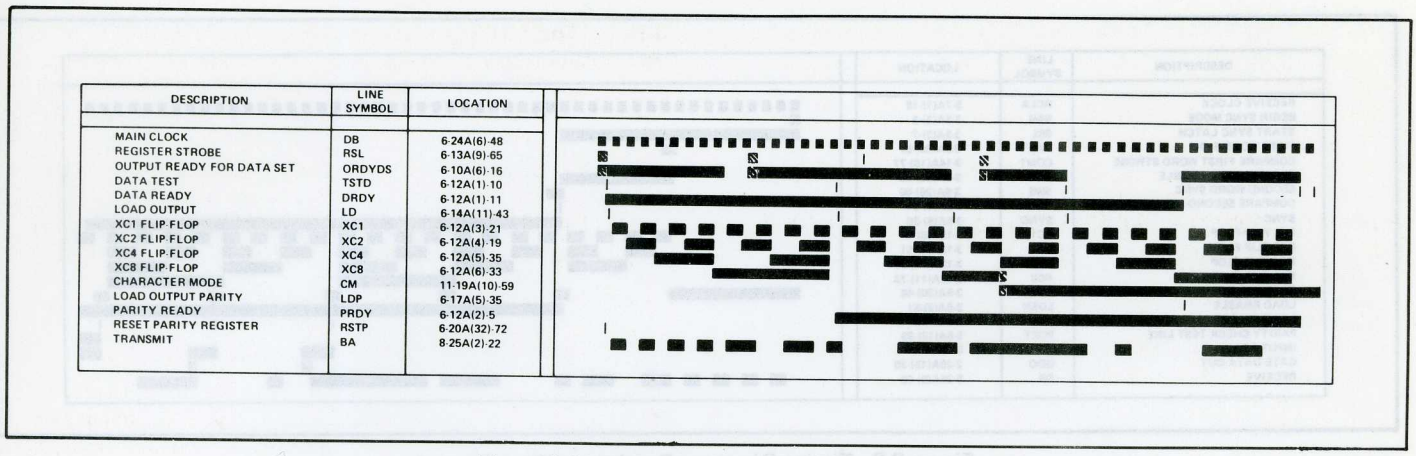
3-133 The transmit logic receives the Transmit Signal Element Timing (DB) signal from the data modem, various control signals from the command register and control logic, and signals from the unit decode logic. It generates the Load Output Register (LD1 and LD2) signal, the Load Output Parity Register (LDP) signal, the Data Ready (DRDY) signal, Shift (SFT) signal, and Output Ready For Data Set (ORDYDS) signal, and the Reset Parity Register (RSTP) signal.

3-134 Timing Circuit

3-135 The transmit section contains a count by eight and count by sixteen circuit. The timing relationships and circuit identifications for these circuits are shown in figure 3-3.

3-136 Busy and Load Data

3-137 When the computer executes an AOP or MOP instruction to this unit, a Register Strobe (RS) signal is generated by the I/O sync logic. This signal is applied to the dc set input of flip-flop 13A(9) causing the Busy signal to go to ONE, and steering applied to flip-flop 12A(1). When a T1 timing pulse is generated, it is gated through AND gate 14A(10) to trigger flip-flop 12A(1) to the set state. When flip-flop 12A(1) is set, it enables the second input to AND gate 14A(11).



DESCRIPTION	LINE SYMBOL	LOCATION
MAIN CLOCK	DB	6-24A(6)-48
REGISTER STROBE	RSL	6-13A(9)-65
OUTPUT READY FOR DATA SET	ORDYDS	6-10A(6)-16
DATA TEST	TSTD	6-12A(1)-10
DATA READY	DRDY	6-12A(1)-11
LOAD OUTPUT	LD	6-14A(11)-43
XC1 FLIP-FLOP	XC1	6-12A(3)-21
XC2 FLIP-FLOP	XC2	6-12A(4)-19
XC4 FLIP-FLOP	XC4	6-12A(5)-35
XC8 FLIP-FLOP	XC8	6-12A(6)-33
CHARACTER MODE	CM	11-19A(10)-59
LOAD OUTPUT PARITY	LDP	6-17A(5)-35
PARITY READY	PRDY	6-12A(2)-5
RESET PARITY REGISTER	RSTP	6-20A(32)-72
TRANSMIT	BA	8-25A(2)-22

Figure 3-3. Timing Diagram - Transmit Control

3-138 The dc voltage is removed from the counter register circuits 12A(3), 12A(4) and 12A(5). These three flip-flops are left in the reset state, and AND gate 14A(9) is fully enabled. This condition partially enables AND gates 14A(11) and 17A(5). When latch 1A(11) is set to a ONE it will enable 14A(11) and 17A(5)and a ONE is generated on the LD signal line. This signal performs two functions: (1) it enables the gate that transfers the data from the output buffer to the parallel-to-serial converter, and (2) LD1 partially enables AND gate 5A(20). When the modem unit is in the character mode (CMH) AND gate 5A(20) is ORed through 5A(18) and triggers flip-flop 13A(9) to the reset state to remove the Busy signal. The absence of the Busy signal informs the computer that another word can be accepted.

3-139 The Output Ready Data Set (ORDYDS) from 20A(31) is transferred to the CEU command register and control logic, sheet 11, and applied to AND gate 22A(23). When the Command to Unit Strobe (CUS) and Data Bit 3 are applied to AND gate 22A(21), and Data Bit 1 is true, the output will trigger flip-flop 19A(8). This fully enables AND gate 22A(23) to generate the Output Priority Interrupt signal through cable driver 28A(2).

3-140 If the computer executes a second AOP or MOP instruction during the time that the counter is being advanced, an RSDS signal will set flip-flop 13A(9). When the counter completes a full cycle and resets itself, AND gate 14A(9) will be fully enabled causing AND gates 14A(10) and 14A(11) to be partially enabled. The first T1 timing pulse after the completion of the counter cycle will be gated through AND-gate 14A(10) to trigger flip-flop 12A(1), but since the flip-flop is already set nothing happens. With latch 1A(11) set to a ONE, AND gate 14A(11) generates an LD signal. The purpose of this is to delay generating a second LD signal until the 8-bits in the parallel-to-serial converter have been shifted out.

3-141 If, however, the computer did not execute a second AOP or MOP instruction, flip-flop 12A(2) would be in the reset state when the counter completed its cycle. Under these conditions the T2 timing signal would trigger flip-flop 12A(1) to the reset state to inhibit the generation of the second LD signal.

3-142 The shift signal is constantly generated by the main input clock. The input clock is inverted by inverters 16A(28) and 16A(25), sheet 6, and applied to the trigger inputs of the P/S converter flip-flops, sheet 8.

3-143 The Parity Enable (PARE) signal from the command register and control logic sheet 11 resets flip-flop 12A(2) through inverter 20A(30) when in the ZERO state. When in the ONE state, and after the second LSTD pulse, flip-flop 12A(2) will assume a set conditon. Upon termination of the data transfers and after flip-flop 12A(1) has been reset, gates 17A(5) and 14A(12) are enabled. 14A(12) inhibits further updating of the parity register while 17A(5) is loading the parity character into P/S converter.

3-144 Command Register and Control Logic (CEU)

3-145 The signals generated in the command register and control logic are applied to various circuits throughout the modem interface.

3-146 The Data Bit 10 after Termination (DB10) signal and Command to Unit Strobe (CUS) signal enable AND gate 22A(24). The output triggers flip-flop 19A(12). Set and reset steering to the flip-flop is supplied by the Data Bit 11 after Termination (DB11) signal. Parity Enable (PARE) signal generated by flip-flop 19A(12) is applied to AND gate 14A(12) on sheet 6, partially enabling this gate. When fully enabled ,this gate will generate the Output Ready for Data Set (ORDYS)signal.

3-147 Also triggered by the output of AND gate 22A(24) are flip-flops 19A(10) and 30B(10). Set and reset steering to 19A(10) is supplied by Data Bit 12 after Termination (DB12) signal. Flip-flop 19A(10) generates the Character Mode (HCM) and (LCM) signal. The LCM signal is applied to AND gate 10A(1) and 6A(19) sheet 6. When this signal is ONE, AND gate 10A(1) and 5A(19) are enabled, intializing a count by sixteen. Refer to the transmit and control logic description for a more detailed discussion of this logic.

3-148 Flip-flop 30B(10) pratially enables AND gate 27B(11) and 17A(4), depending on the state of the set or reset output. Register Strobe (RS) signal or BTCI Register Strobe (BRS) signal fully enables these gates; generating the Register Strobe Auto-Dial (RSAD) signal, Register Strobe Data Set 1 (RSDS1) signal, Register Strobe Data Set 2 (RSDS2) signal and the Register Strobe Data Set (RSDS) signal.

3-149 Data Bit 4 after Termination (DB4) signal supplies set steering to flip-flop 12A(7). The Command to Unit Strobe (CUS) signal triggers the flip-flop, thereby activating the Request to Send signal to the data modem. However, Data Bit 5 after Termination (DB5) signal resets the request to send flip-flop thereby deactivating the Request to Send signal to the data modem. Flip-flop 19A(9) is set or reset by Data Bit 7 after Termination (DB7) signal or Data Bit 8 after Termination (DB8) signal, respectively. The signal activates or deactivates the Data Terminal Ready signal to the data modem.

3-150 The Command to Unit Strobe (CUS) plus the Data Bit 15 After Termination (DB15) signal are ANDed through gate 27B(12) and applied to the trigger input of flip-flop 30B(11). Data Bit 9 After Termination supplies both the set and reset steering to 30B(11). A Master Clear or Low reset output from flip-flop 19A(9) is applied to the dc reset of this flip-flop,(through OR gate 27B(13). The set output of 30B(11) is generated through cable driver 25B(6) to pin 75, connector 26A.

3-151 This signal constitutes the Call Request (CRQ) signal, which activates the call request line (auto-dial). The bit is active only with bit 15 set.

3-152 Test Logic (TEU)

3-153 The TEU instruction is used by the computer to test the status of the data modem. The functions that are tested are listed in the TEU second word format, as shown in table 2-4. The test code, used to determine which function is to be tested, is contained in bits 0 to 9, depending whether the SYSTEMS 810 Series Computer or the SYSTEMS 840 Series Computer is utilized.

3-154 The test control logic monitors the Data Set Ready (CC) signal, Data Set is Clear to Send (CB) signal, Data Carrier Detector line (CF) signal, Data Modulation Detector (CG) signal, Ring Indicator (auto-dial option) (PW1) signal, Data Set in Data Mode (auto-dial option) (DSS) signal, Data Line Unoccupied (auto-dial option) (AC) signal. The status of the data modem is reflected in the condition of these lines, and is tested by the computer by executing a TEU instruction to this unit. The TEU word bit, when set (ONE), performs the tests below. (Skip signifies the next sequential instrction is bypassed when the true condition exists).

3-155 When testing for the CC, bit 0 of the TEU second word is set. If the data set is ready, the CC line will be true and AND gate 22A(14) fully enabled. A ZERO is applied to OR gate 17A(2) which in turn applies a ONE to AND gate 22A(19). The other input to AND gate 22A(19) is supplied by the Test Unit Condition (TEST) signal, which also partially enables AND gate 5A(14). The Test signal originates in the I/O sync logic from the ONE levels of the Computer Data Here (CDH2) signal, the Test Instruction (TIN) signal and the This Unit Selected (TUN) signal. With AND gate 22A(19) fully enabled, a Test Skip Reply (TESKP) signal is generated, and gated to the computer through OR gate 22A(9) shown on sheet 2.

3-156 The received data sets the steering of the received parity register (sheet 5). The set output of the parity register is ANDed by 3A(11) and 3A(10), then inverted and ANDed together with HDB5. The AND gate output is ORed at 17A(3) to cable 22A(19) with a TEU command.

3-157 The TEST signal and the NE signal are applied to AND gate 5A(14), generating the Reset Receive Parity (RRP) signal, which supplies a reset pulse to the receive ready flip-flop 12A(12), sheet 3.

3-158 S/P CONVERTER AND INPUT BUFFER REGISTER

3-159 The serial-to-parallel converter and input buffer register logic circuits are shown on drawing 130-100659-000, sheets 4 and 5.

3-160 Serial-to-Parallel Converter

3-161 The serial data is shifted into the serial-to-parallel converter by the receive clock pulses. The incoming data together with CF enables AND gate 15A(1), delivering both set and reset steering to flip-flop 6A(1). The receive clock then triggers the register and shifts the data into the register. After eight successive signals, a complete 8-bit data word is stored in the S/P converter register.

3-162 Input Buffer Register

3-163 When the S/P register is triggered, the data contained in it is transferred into the input buffer register through the steering inputs. The Load Input Register 2 (HD2R) signal triggers the flip-flop. The output of the buffer register partially enables the AND gates.

3-164 In response to the Input Interrupt, the computer executes an AIP or MIP instruction. This causes a GDO signal to be generated by the I/O sync logic. The GDO signal then fully enables the AND gates, placing the data on the drivers, and enabling the transfer of the data through the I/O bus to the computer.

3-165 OUTPUT BUFFER AND P/S CONVERTER

3-166 The logic for the output buffer register and the parallel-to-serial converter is shown on drawing 130-100659-000, sheets 7 and 8.

3-167 Output Buffer Register

3-168 Data bits 0 through 15 from the computer I/O bus are applied to the output buffer register through a set of cable terminators and inverters. When a data bit is present on the I/O bus, set steering is applied to the associated flip-flop in the buffer register. Conversely, when the bit is ZERO, reset steering is applied. A Register Strobe (RS) signal is generated by the I/O sync logic when an AOP or MOP instruction is being executed. This strobe simultaneously triggers the 16 flip-flops in the register to load the data from the I/O bus into the output buffer. A Master Clear may be initiated from the control panel of the computer, if so desired, or is initiated when power is first applied to the systme to clear the register.

3-169 Parallel-to-Serial Converter

3-170 Initially the P/S converter is reset by the Master Clear signal (ICB1). After the data from the I/O bus is stored in the output buffer, the Load Output (LD) signal is generated by the transmit logic. This signal enables a set of gates that apply the dc set signal to the flip-flop in the P/S converter

when a ZERO is stored in the corresponding flip-flop in the output buffer register. After the data is loaded into the P/S converter, the transmit logic, shown on sheet 6, generates the Shift Pulse (SFT) signal that triggers the register.

3-171 The SFT pulses are derived directly from the data modem main clock. Each time an SFT is received, the data is shifted one bit. At the end of eight consecutive shift pulses, the eight data bits are shifted to the data modem through transmit circuit 25A(2).

3-172 OPTIONS

3-173 Parity Register and Load Gates (Option)

3-174 Provisions are made for block parity error generation and input checking. A block parity character is formed on each block input in a manner identical to the LRCC character on magnetic tape systems. This amounts to a column-wise parity generation on each of the 8-bits in each of the characters in the input block. This parity signal is formed in an 8-bit flip-flop register. It is set for even parity when the unit switches to the sync mode.

3-175 As each incoming character is transferred to the input buffer, sheet 8, all ONE bits in the character cause the flip-flops 2A(1) through 1A(10) on sheet 10 (parity register and load gates) to switch states. ZERO's do not affect the register flip-flops.

3-176 For example even parity would be as follows:

11101001 Previous state of parity character register
10110111 New incoming character
01011110 New state of parity character register

Note

This is equivalent to a logical exclusive OR function of the two characters.

3-177 When Latch 1A(11) is set to a ONE AND gate 14A(11) is enabled for an output. This output is inverted, ANDed with T3, inverted again and used to Strobe the output parity register. Generation of a ONE from the reset output of the parity register flip-flops partially enables the AND load gates. The Load Output Parity Register (LDP) signal generated when AND gate 17A(5) on sheet 6 is enabled, fully enables the load gate, sheet 10, applying a parity bit to the set inputs of the flip-flops of the P/S converters, sheet 8.

3-178 Block Transfer Control Interface (Option)

3-179 The BTC interface logic, drawing 130-100659-000 sheet 12, is an integral part of the data terminal used with a unit operating with the BTC. The units data terminal connects both the standard I/O bus and the block transfer control. Signal lines,applied through cable terminators and cable drivers, interface with the BTC through the BTC cable. All other signals are derived from either the data terminal or the unit control logic. Additional information concerninc BTCI operation is located in the I/O Design Manual for the specific 800 Series Computer being used.

3-180 The basic signal flow is sequenced in the following manner:

a. The command function bit (bit 0) sent to the unit causes the device to raise the Initialize signal to the BTC.

b. The function bits also enable the device to raise the I/O signal depending on direction of transfer.

c. The Unit Disconnected signal form the computer is sent to all devices causing them to disconnect from the BTC.

d. The BTC recognizes that the device is disconnected by the presence of Unit Connected signal.

e. The BTC then removes the Unit Disconnect signal. The device logic generates the signal Unit Data Accepted, indicating the command second word is processed and sends this signal to the mainframe control unit which terminats the I/O instruction and removes the function bits. The device recognizes the removal of the function bits and generates the Unit Connected signal to the BTC.

f. The BTC then receives the Data Transfer Request signal from the device logic.

g. The device receives either one of two signals along with a data word transfer; BTC Data Here to Unit signal,if the device is inputting data; Gate Data Out signal, if the device is outputting data.

h. The device sends either one of two signals with each data word transfer. Unit Data Here signal is sent to the BTC if the device is inputting data; and Unit Data Accepted signal is sent to the BTC if the device is outputting data.

i. When the value of the word count is decremented to zero and termination reached, the BTC sends out the End of Block signal and the Units Disconnect signal.

3-181 External Clock (Option)

3-182 An external clock is available as an option. A crystall oscillator 22B(1) on drawing 130-100659-000 sheet 13 supplies a specific frequency to the steering and trigger input of flip-flop 23B(1). The 11 additional flip- flops act as dividers. Frequency requirements can be obtained by wiring to specific flip-flop output points. In addition, the crystal may be selected to meet specific frequency requirements.

3-183 One of the clock output leads is connected to the transmit timing lead through driver 25A(4) sheet 13. The other is connected to the receive timing lead through driver 25A(5).

3-184 Auto-Dial (Option)

3-185 The SYSTEMS 800 Series Computer controls the SCMIU through execution of the standard input/output instructions. Whenever auto-dial logic is utilized, bit SAD in the CEU second word is applied to the auto-dial mode to allow communication to the dialing mechanism. Refer to tables 2-3, and 2-4 for CEU and TEU second word formats.

3-186 Data bits 0 through 4 After Termination (DBO) signal supplies steering to flip-flops 30B(1) through 30B(4). These bits are received from the inverters 16A(1) through 16A(4) on sheet 7. Triggering to the flip-flop is supplied by the Register Strobe (Auto-Dial) (RSAD) signal from sheet 11 The set output of each flip-flop is transmitted through cable drivers 25B(2), 25B(3), 25B(4), and 25B(5), pin numbers 71,72,73 and 74, on connector 26A.

3-187 The instruction Present Next Digit (PND) signal is applied to the trigger input of flip-flop 23B(11) by receiver 24B(1) to reset the flip-flop. The Register Strobe (auto-dial) (RSAD) signal dc sets flip-flop 23B(11). The Master Clear (ICB) signal is applied to the dc input of this flip-flop as well as the other flip-flops in the auto-dial logic. The set output is transferred through cable driver 25B(1) to pin 70, connector 26, indicating the Digit Present (DPR) signal. The Present Next Digit (PND) signal is inverted and ANDed together with the reset output of flip-flop 23B(11) plus the Output Line (OTP) signal and the Enable Auto Dial (EAD) signal through AND gate 26B(5). The output of this AND gate constitutes the Out Ready for Auto-dial (RDYAD) signal and is applied to OR gate 21A(17), sheet 9, initiating the Buffer Ready signal to AND gate 22A(2), sheet 1.

3-188 SYSTEMS MODEL 240-000-04 POWER SUPPLY

3-189 Figure 3-4 is the block diagram of the 240 series power supply, (Refer to the specifications and leading particular tables in Section I for specifics). The following is a detailed description of the power supply.

3-190 Under normal conditions, the feedback voltage from the supplies' output is constantly compared to the reference voltage to generate an error correction input signal to the output driver. As long as the current demand remains within the supplies' limits, the error correction signal will maintain a constant output voltage by varying the amount of current flowing through the output transistor Q2. Shorting the output terminals together causes the current overload detection circuit to turn OFF the constant current generator. The resulting error signal generated by the voltage comparator limits the amount of current flowing through the output transistor. When the short is removed, and if the fuse (F1) has not opened, the output voltage will return to normal if the output voltage rises above seven volts, the overvoltage detection circuitry protects the logic connected to the supply by turning ON the silicon rectifier's output together and causes the fuse to open.

3-191 SIGNAL GLOSSARY

3-192 Table 3-1 provides a list of primary signals used in the logic pertaining to Section III.

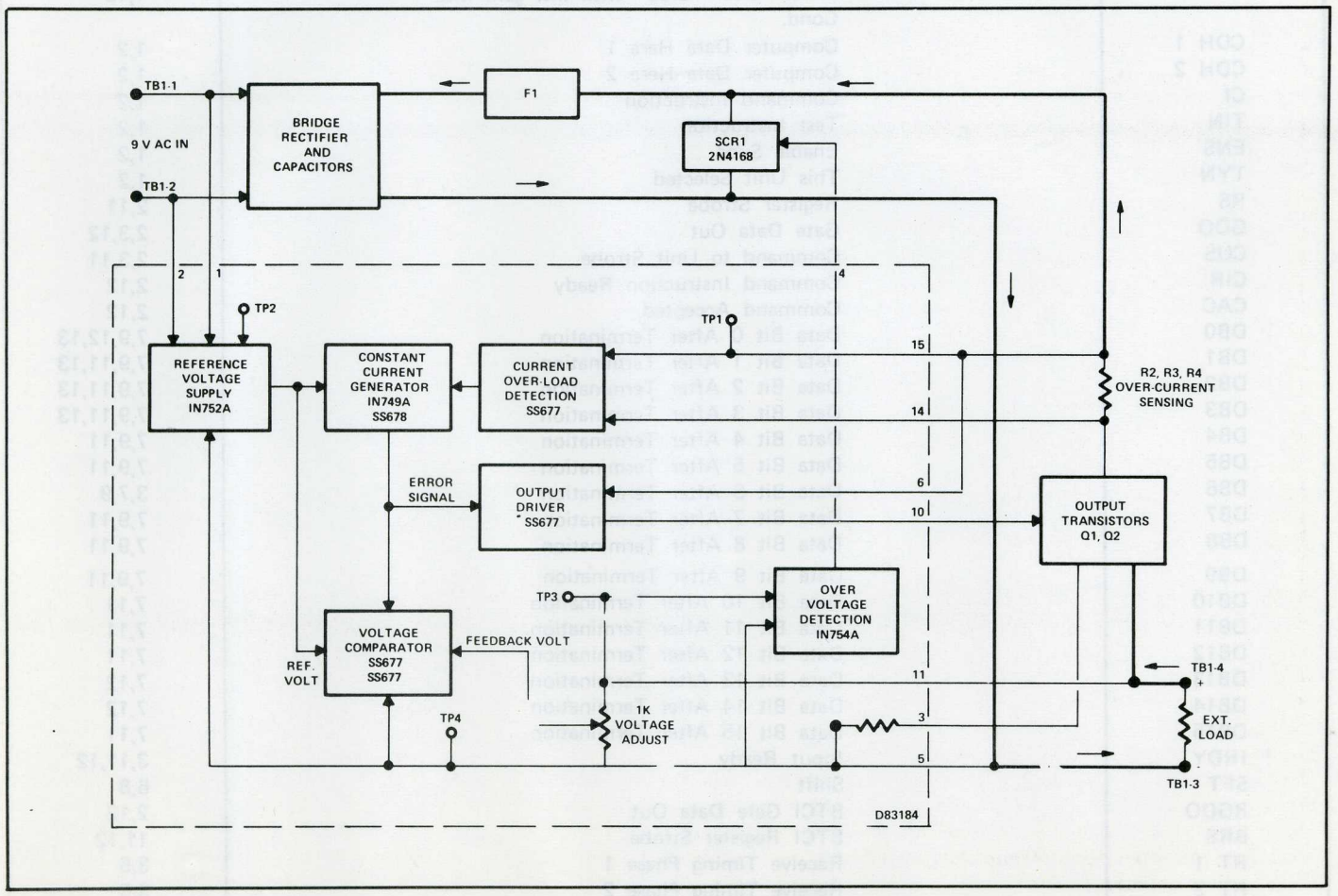


Figure 3-4. Block Diagram - SYSTEMS 240 Power Supply

Table 3-1. Synchronous Data Set, Mnemonic Reference

Mnemonic	Description	Sheets
INP	Input Line	1,2,3
OTP	Output Line	1,2,9,13
CDA	Computer Data Accepted	1,2
WFL	Wait Flag	1,2
T3T	Computer Clock #1	1,2
DTI	Data Transfer Instruction	1,2
INS	Instruction Sync	1,2
ICB 1	Master Clear "ored" with int. gen. Init. Cond.	1,8
ICB 2	Master Clear "ored" with int. gen. Init. Cond.	1,7
ICB 3	Master Clear "ored" with int. gen. Init. Cond.	1,7
ICB 4	Master Clear "ored" with int. gen. Init. Cond.	1,3,6
ICB 5	Master Clear "ored" with int. gen. Init. Cond.	1,5
ICB 6	Master Clear "ored" with int. gen. Init. Cond.	1,4
ICB 7	Master Clear "ored" with int. gen. Init. Cond.	1,4
ICB 8	Master Clear "ored" with int. gen. Init. Cond.	1,11
ICB 9	Master Clear "ored" with int. gen. Init. Cond.	1,13
CDH 1	Computer Data Here 1	1,2
CDH 2	Computer Data Here 2	1,2
CI	Command Instruction	1,2
TIN	Test Instruction	1,2
ENS	Enable Sync	1,2
TYN	This Unit Selected	1,2
RS	Register Strobe	2,11
GDO	Gate Data Out	2,3,12
CUS	Command to Unit Strobe	2,3,11
CIR	Command Instruction Ready	2,12
CAC	Command Accepted	2,12
DB0	Data Bit 0 After Termination	7,9,12,13
DB1	Data Bit 1 After Termination	7,9,11,13
DB2	Data Bit 2 After Termination	7,9,11,13
DB3	Data Bit 3 After Termination	7,9,11,13
DB4	Data Bit 4 After Termination	7,9,11
DB5	Data Bit 5 After Termination	7,9,11
DB6	Data Bit 6 After Termination	3,7,9
DB7	Data Bit 7 After Termination	7,9,11
DB8	Data Bit 8 After Termination	7,9,11
DB9	Data Bit 9 After Termination	7,9,11
DB10	Data Bit 10 After Termination	7,11
DB11	Data Bit 11 After Termination	7,11
DB12	Data Bit 12 After Termination	7,11
DB13	Data Bit 13 After Termination	7,12
DB14	Data Bit 14 After Termination	7,12
DB15	Data Bit 15 After Termination	7,11
IRDY	Input Ready	3,11,12
SFT	Shift	6,8
BGDO	BTCI Gate Data Out	2,12
BRS	BTCI Register Strobe	11,12
RT 1	Receive Timing Phase 1	3,5
RT 2	Receive Timing Phase 2	3,5

Table 3-1. Synchronous Data Set, Mnemonic Reference (Cont'd)

Mnemonic	Description	Sheets
RT 3	Receive Timing Phase 3	3,5
CM	Character Mode	3,6,11
RSDS 1	Register Strobe (Data Set) 1	7,11
RSDS 2	Register Strobe (Data Set) 2	7,11
COMRDY	Command "or" Instruction Ready	1,2
T3T2	Computer Clock #2	1,2
BRDY	Buffer Ready	1,9
TESKP	Test Skip Reply	2,9
GDO 1	Gate Data Out #1 w/BTCI	2,4
GDO 2	Gate Data Out #2 w/BTCI	2,4
TEST	Test Unit Condition	2,9
I0	Data Bit 0 Before Termination	4,7
I1	Data Bit 1 Before Termination	4,7
I2	Data Bit 2 Before Termination	4,7
I3	Data Bit 3 Before Termination	4,7
I4	Data Bit 4 Before Termination	4,7
I5	Data Bit 5 Before Termination	4,7
I6	Data Bit 6 Before Termination	4,7
I7	Data Bit 7 Before Termination	4,7
I8	Data Bit 8 Before Termination	4,7
I9	Data Bit 9 Before Termination	4,7
I10	Data Bit 10 Before Termination	4,7
I11	Data Bit 11 Before Termination	4,7
I12	Data Bit 12 Before Termination	4,7
I13	Data Bit 13 Before Termination	4,7
I14	Data Bit 14 Before Termination	4,7
I15	Data Bit 15 Before Termination	4,7
ORDYDS	Output Ready for Data Set	6,9,11,12
ORDYAD	Output Ready for Auto Dial	9,13
IRDYDS	Input Ready for Data Set	3,9
CNTEN	Counter Enable (Transmit)	6,11
RSAD	Register Strobe (Auto-Dial)	11,13
RSTP	Reset Parity Register (Transmit)	6,10
PARE	Parity Enable	5,6,11
LD1	Load Output Register #1	6,8
LD2	Load Output Register #2	6,8
LDP	Load Output Parity Register	6,10
PB1	Parity Bit 1 to Parity Register (Transmit)	8,10
PB2	Parity Bit 2 to Parity Register (Transmit)	8,10
PB3	Parity Bit 3 to Parity Register (Transmit)	8,10
PB4	Parity Bit 4 to Parity Register (Transmit)	8,10
PB5	Parity Bit 5 to Parity Register (Transmit)	8,10
PB6	Parity Bit 6 to Parity Register (Transmit)	8,10
PB7	Parity Bit 7 to Parity Register (Transmit)	8,10
PB8	Parity Bit 8 to Parity Register (Transmit)	8,10
DRDY	Strobe Parity Register	6,10
BTCRS	Input End of Block Reset Sync	12,3
SPB1	Parity Bit 1 to Transmit Register	8,10
SPB2	Parity Bit 2 to Transmit Register	8,10
SPB3	Parity Bit 3 to Transmit Register	8,10
SPB4	Parity Bit 4 to Transmit Register	8,10
SPB5	Parity Bit 5 to Transmit Register	8,10
SPB6	Parity Bit 6 to Transmit Register	8,10
SPB7	Parity Bit 7 to Transmit Register	8,10
SPB8	Parity Bit 8 to Transmit Register	8,10
RCLIC	Receive Clock	3,5
CPAR	Count Parity Register (Receive)	3,5
LDIR	Load Input Register 1 (Receive)	3,4

Table 3-1. Synchronous Data Set, Mnemonic Reference (Cont'd)

Mnemonic	Description	Sheets
LDZR	Load Input Register 1 (Receive)	3,4
SNG	Sync No Good	3,5
ODB0	Output Register Data Bit 0	7,8
ODB1	Output Register Data Bit 1	7,8
ODB2	Output Register Data Bit 2	7,8
ODB3	Output Register Data Bit 3	7,8
ODB4	Output Register Data Bit 4	7,8
ODB5	Output Register Data Bit 5	7,8
ODB6	Output Register Data Bit 6	7,8
ODB7	Output Register Data Bit 7	7,8
ODB8	Output Register Data Bit 8	7,8
ODB9	Output Register Data Bit 9	7,8
ODB10	Output Register Data Bit 10	7,8
ODB11	Output Register Data Bit 11	7,8
ODB12	Output Register Data Bit 12	7,8
ODB13	Output Register Data Bit 13	7,8
ODB14	Output Register Data Bit 14	7,8
ODB15	Output Register Data Bit 15	7,8
RB1	1st Received Bit	3,4,5
RB2	2nd Received Bit	3,4,5
RB3	3rd Received Bit	3,4,5
RB4	4th Received Bit	3,4,5
RB5	5th Received Bit	3,4,5
RB6	6th Received Bit	3,4,5
RB7	7th Received Bit	3,4,5
RB8	8th Received Bit	3,4,5
BSM	Begin Sync Mode	3,5
RRP	Reset Receive Parity	3,9
EAD	Enable Auto-Dial	9,11,13
PCKT	Parity Check Test Line	5,9
RSDS	Register Strobe (Data Set)	6,11,12

SECTION IV

INSTALLATION AND MAINTENANCE

4-1 INTRODUCTION

4-2 This section contains information pertaining to the installation and maintenance of the SYSTEMS Synchronous Communications Modem Interface.

4-3 INSTALLATION

4-4 The communications modem interface is normally provided as part of a system and is installed in one of the system cabinets at the factory. However, if the unit is provided separately, the following installation procedures are recommended.

4-5 INSTALLATION REQUIREMENTS

4-6 The room in which the unit is to be operated should be climatically controlled to provide the necessary environmental requirements specified in Section I, Specifications and Leading Particulars. The cabinet space requirements may be determined by referring to the assembly drawings in Section VI.

4-7 When selecting a location for the installation of the communications modem interface, consideration should be given to the distance between the unit and the data modem. The cable connecting these two units should be as short as possible and should not exceed 45 feet.

4-8 UNPACKING PROCEDURES

4-9 The following procedure is suggested for unpacking the equipment. The method of packing is dependent upon the mode of transportation for shipment. This unpacking procedure is for equipment packed to meet the most severe manner of transportation.

a. Cut the metal binding straps around the shipping crate.

b. Remove the unit by carefully lifting it from the crate.

c. Remove the surrounding styrofoam padding.

d. Remove the polyethyene bag covering the unit.

e. Remove the tape, supports, paper shims, etc.

f. Remove the external cables and lines if included in the package.

g. Thoroughly inspect the equipment to determins if any damage has occurred during shipment. Should any damage be discovered, a claim should be filed with the carrier. A complete report of damage should be forwarded to SYSTEMS Engineering Laboratories, Incorporated, for advice concerning the disposition of the equipment.

4-10 SETUP

4-11 The following procedures are provided for installing the communications modem interface unit, the I/O connector panel and the SYSTEMS 240 Power Supply, in a standard electronic equipment cabinet.

a. Install the communications modem interface , the I/O connector panel and the SYSTEMS 240 Power Supply using 10-32X1/2 inch bolts to fasten the units to the mounting rail in the equipment cabinet.

b. Fabricate an RS-232-B Interface Cable for the data modem. Refer to table 4-1 for the pin connections.

Note

The RS-232-B Interface Cable length should not exceed 45 feet.

CAUTION

Always remove primary power from the system (and computer) before making any signal cable connections. Otherwise, buffered outputs could become accidentally grounded, thereby damaging system components.

c. Connect all of the external signal cables between the computer communications modem interface, and the data modem per figure 4-1.

d. Terminate the 5.0 volt,±6 volt and ground connections from the SYSTEMS 240 Power Supply to the Jones terminal strip located on the communications modem interface unit.

e. Connect the ac power input on the SYSTEMS 240 Power Supply to the cabinet circuit breaker (not provided).

f. Perform the performance test procedures provided in Section V for checking the operation of the unit.

4-12 MAINTENANCE

4-13 Refer to Section VI for schematic and assembly drawings of the individual circuit cards and to Section VII for the logic drawings of the unit. A thorough understanding of the theory of operation is necessary for effective troubleshooting of the unit.

Invalid due to errors

Table 4-1. Interface Cable Connector

Mnemonic	Description	P6
CRQ	Call Request	305/405
NB1	Digit 1	309/409
NB2	Digit 2	308/408
NB4	Digit 4	307/407
NB8	Digit 8	306/406
DPR	Digit Present	310/411
PND	Present next Digit	305/405
PWI	Power Indicator	301/401
DSS	Data Set in Data Mode	302/402
DLO	Data Line Occupied	303/403
ACR	Abandon Call	304/404
BA	Transmitted Data	101/201
BB	Received Data	102/202
CA	Request to Send	106/206
CB	Clear to Send	108/208
CC	Data Set Ready	107/207
CD	Data Terminal Ready	105/205
CE	Ring Indicator	111/211
CF	Data Carrier Detector	109/209
CG	Data Modulation Detector	110/210
DB	Transmitted Signal Element Timing	103/203
DD	Receiver Signal Element Timing	104/204

4-14 SPECIAL TOOLS AND TEST EQUIPMENT

4-15 Table 4-2 provides a list of special tools and test equipment required to setup and maintain the communications modem interface unit.

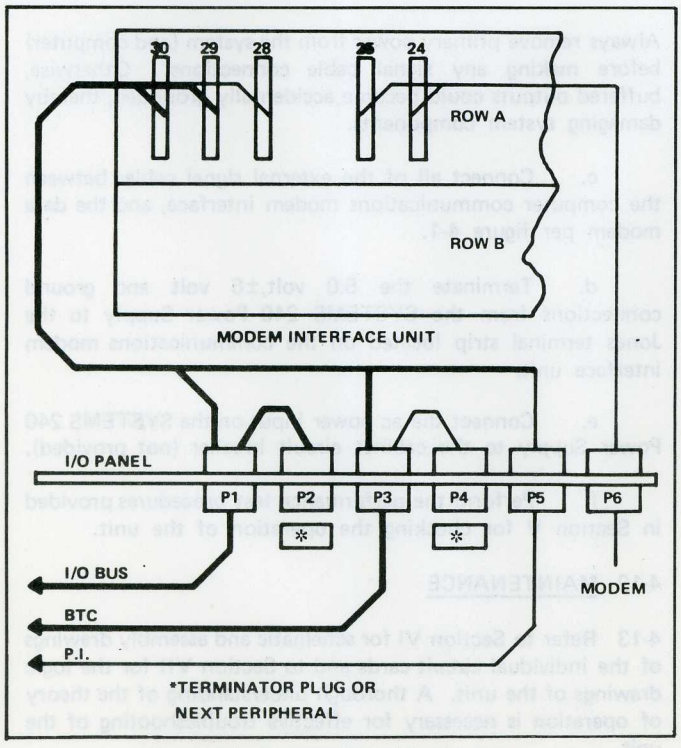


Figure 4-1. External Cabling Diagram

4-16 PREVENTIVE MAINTENANCE

4-17 Schedule

4-18 A preventive maintenance schedule can best be established by the user, who knows the exact conditions under which the system is operating.

4-19 No special maintenance schedule for the digital logic is necessary. It is recommended that an occasional cleaning of the digital logic area be performed, but the primary rule is: Hands off, if the system is functioning properly.

4-20 CORRECTIVE MAINTENANCE

4-21 Adjustment Procedures

4-22 The communications modem interface unit does not contain any circuit cards which require adjustment. However, the regulator card in the SYSTEMS Model 240-000-04 and -03 power supplies are adjustable using the following procedure:

a. Connect a voltmeter to the output of the power supply module.

b. Adjust potentiometer R9 on the regulator assembly card (160-083184) for the desired output reading.

4-23 Removal and Replacement Procedures

4-24 The procedure for removing the communications modem interface from its cabinet is the reverse of the procedure in the setup procedure.

EIA MODEM AND INTERFACE CONNECTOR CABLE

MODEM	MNEMONIC	SIGNAL DESCRIPTION	INTERFACE	
			J1 Signal	Gnd
Pin 1 Wht/Brn	FG	Frame Ground	To All	
Pin 2 Wht/Blu	TD	Transmit Data	102	202
Pin 3 Wht/Yel	BB	Receive Data	106	206
Pin 4 Wht/Grn	CA	Request To Send	101	201
Pin 5 Red/Blk	CB	Clear To Send	108	208
Pin 6 Brn	CC	Data Set Ready	107	207
Pin 7 Blu	SG	Signal Ground	To All	
Pin 8 Red	CF	Data Carrier Detector	109	209
Pin 15 Wht/Slt	DB	Transmitted Signal Timing	104	204
Pin 17 Wht	DD	Receiver Signal Timing	105	205
Pin 20 Org	CD	Data Terminal Ready	103	203
Pin 21 Lht Brn	CG	Data Modulation Detector	110	210
Pin 22 Wht/Blk	CE	Ring Indicator	111	211

7-7-75

Invalid due to errors.

Table 4-2. Special Tools and Test Equipment

Name	Manufacturer	Part No/Model
Oscilloscope	Tektronix	547
Scope Plug-in	Tektronix	1A1
Volt-ohm Meter	Simpson	260
Oscillator	Wavetek	105
Card Tester	SYSTEMS	9066
Extension Card	SYSTEMS	8013
Wire-Wrap and Unwrap Tools	Gardner-Denver	Refer to the wire-wrapping procedure section for part and model number

4-25 Circuit cards are removed simply by pulling the card free from its connector. No special tool is required for extracting the card. All like type cards are interchangeable.

4-26 Replacement Circuit Components

4-27 The following procedures are for removing components from the circuit boards. The only special equipment required is a standard ear syringe and a four-inch length of No. 10 thin-wall Teflon tubing.

a. Insert one end of the Teflon tubing into the syringe.

b. Heat the soldered connection. While the solder is in a molten state, use the syringe and tubing to draw the solder from the connection.

c. Carefully pry the component lead loose from the copper land of the printed circuit board and straighten.

d. Repeat steps a, b, and c for each lead of the component and pull the component from the printed circuit board.

4-28 Wire Wrapping Procedures

4-29 These procedures define the materials and processes recommended for wire wrapped electrical connections which are used in all SYSTEMS products. The typical card connectors illustrated in figure 4-2 establish the terminology relating to these wire wrapping procedures.

4-30 Wire Wrap Guns. The following wire wrap guns are recommended for use in the installation of solid or standed wire:

a. Hand Squeeze (Gardner-Denver 14H-1C or equivalent).

b. Battery Operated (Gardner-Denver 14R2 or equivalent).

c. Air Operated (Standard Pneumatic Model 663 or equivalent).

Note

The hand squeeze gun should not be used for wrapping wire smaller than AWG 28, Battery powered or air operated guns may be used for wrapping, wire sizes AWG 22 through AWG 30.

4-31 AC electric powered wire wrap guns are not recommended for use on SYSTEMS equipment due to the malfunctions which may arise. If guns of this type must be used , care should be taken during the wrapping procedures to eliminate cut or crimped wire, or torn insulation near the connection.

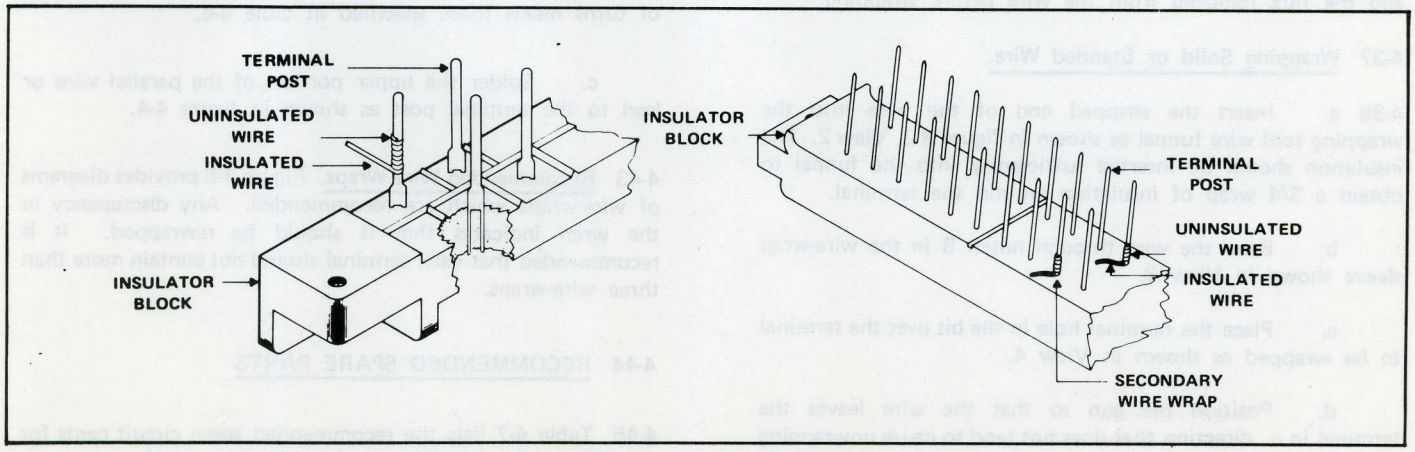


Figure 4-2. Typical Card Connectors

4-32 Wire-Wrap Bits and Sleeves. The bits and sleeves listed in table 4-3 are used for wrapping AWG 22 through AWG 30 solid or standed wire. All of the bits and sleeves listed are manufactured by Gardner-Denver, Inc.

4-33 Wire-Wrap Types. This procedure outlines three types of wire-wraps; solid wire-srap, standed wire-wrap, and secondary wire-wrap. The solid and standard types produce a tightly wrapped spiral of continuous wire around the terminal post.

4-34 The secondary type produces the same type of connection as the solid or standed wrap, with a length of bare wire wrapped around the terminal and a wire or component lead.

4-35 Wire-Preparation. The wire end to be wrapped should be stripped of insulation to the length specified in table 4-4.

Table 4-3. Wire-Wrap Bits and Sleeves

Wire Gauge	Wire Diameter In Inches	Solid Wire		Stranded Wire	
		Bit No.	Sleeve No.	Bit No.	Sleeve No.
30	0.0100	507063	500350	501389	502129
28	0.0126	509278	507100	None	None
26	0.0159	502118	512056	507062	18840
24	0.201	507062	18840	26699	18840
22	0.253	26699	18640	None	None

Table 4-4. Wire Stripping Lengths

Wire Gauge	Strip Length In Inches	
	Minimum	Maximum
30	1 1/16	1 9/64
28	31/32	1 3/16
26	1 7/16	1 11/16
24	1 1/8	1 7/16
22	1 1/8	1 7/16

4-36 Standed wire should be thoroughly tinned with pure tin and the flux removed from the wire before wrapping.

4-37 Wrapping Solid or Standed Wire.

4-38 a. Insert the stripped end of the wire into the wrapping tool wire funnel as shown in figure 4-3, View 2. The insulation should be inserted sufficiently into the funnel to obtain a 3/4 wrap of insulation around the terminal.

b. Bend the wire through notch B in the wire-wrap sleeve shown in View 3.

c. Place the terminal hole in the bit over the terminal to be wrapped as shown in View 4.

d. Position the gun so that the wire leaves the terminal in a direction that does not tend to cause unwrapping after ther termination of both ends of the wire has been made.

e. Squeeze the trigger on the gun, allowing the wire-wrap to be completed as shown in Views 5 and 6.

f. Check the connection to insure that the number of turns are within the specifications provided in table 4-5.

4-39 Secondary Wire-Wrap. This type requires the bits and sleeves shown in table 4-6 for each wire gauge. The table also provides the recommended number of turns for the connection.

4-40 Component Lead of Wire Preparation. Insulted wire should be stripped to a length which does not exceed more than one-sixteenth of an inch above the top turn, or less than one-thirty second of an inch above the top turn, Standed wire should be tinned with solder and the flux removed before the termination is completed.

4-41 Component leads should be sleeved to one-quarter of an inch from the end of the lead. The wire or lead should be bent at a right angle at the point where the insulation or sleeve begins.

4-42 Secondary Wrapping Method

a. The wire or lead to be connected to the post is positioned parallel to the post. Using the correct bit and sleeve listed in table 4-6, a second length of bare wire is wrapped around the post and lead following the same procedures outlined for wrapping solid or standed wire.

b. Check the connection to insure that the number of turns meets those specified in table 4-6.

c. Solder the upper portion of the parallel wire or lead to the terminal post as shown in figure 4-4.

4-43 Recommended Wire Wraps. Figure 4-5 provides diagrams of wire-wraps which are recommended. Any discrepancy in the wrap indicates that it should be rewrapped. It is recommended that each terminal should not contain more than three wire-wraps.

4-44 RECOMMENDED SPARE PARTS

4-45 Table 4-7 lists the recommended spare circuit cards for the Synchronous Communications Modem Interface.

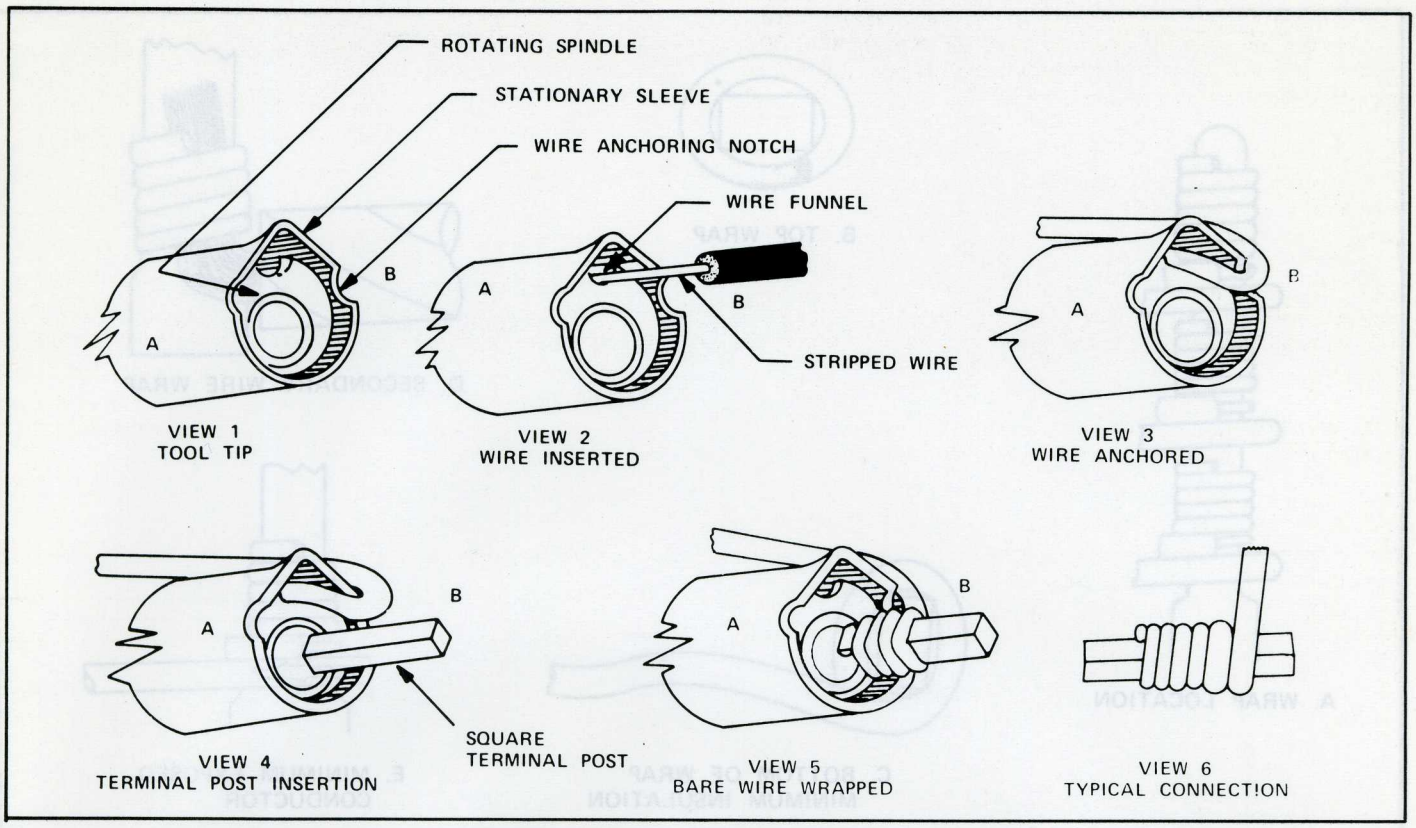


Figure 4-3. Solderless Wrap Connection Process

Table 4-5. Recommended Turns

Wire Gauge	Number of Turns	
	Minimum	Maximum
30	9	11
28	8	10
26	6	7
24	5	6
22	5	6

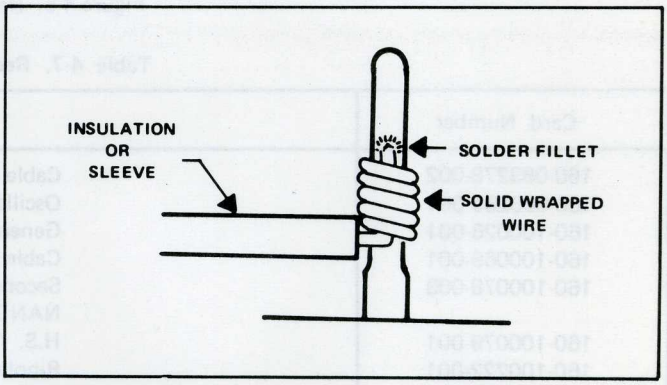


Figure 4-4. Secondary Soldered Wrap Connection

Table 4-6. Secondary Wire-Wrap Bits and Sleeves

Wire Gauge	Bit Number	Sleeve Number	Number of Turns	
			Minimum	Maximum
30	None	None		
28	None	None		
26	507062	18840	6	7
24	507062	18840	4.5	6
22	507062	18840	4.5	6
20	507062	18840	4.5	6
18	20420	17611	4.5	6
16	20420	17611	4.5	6

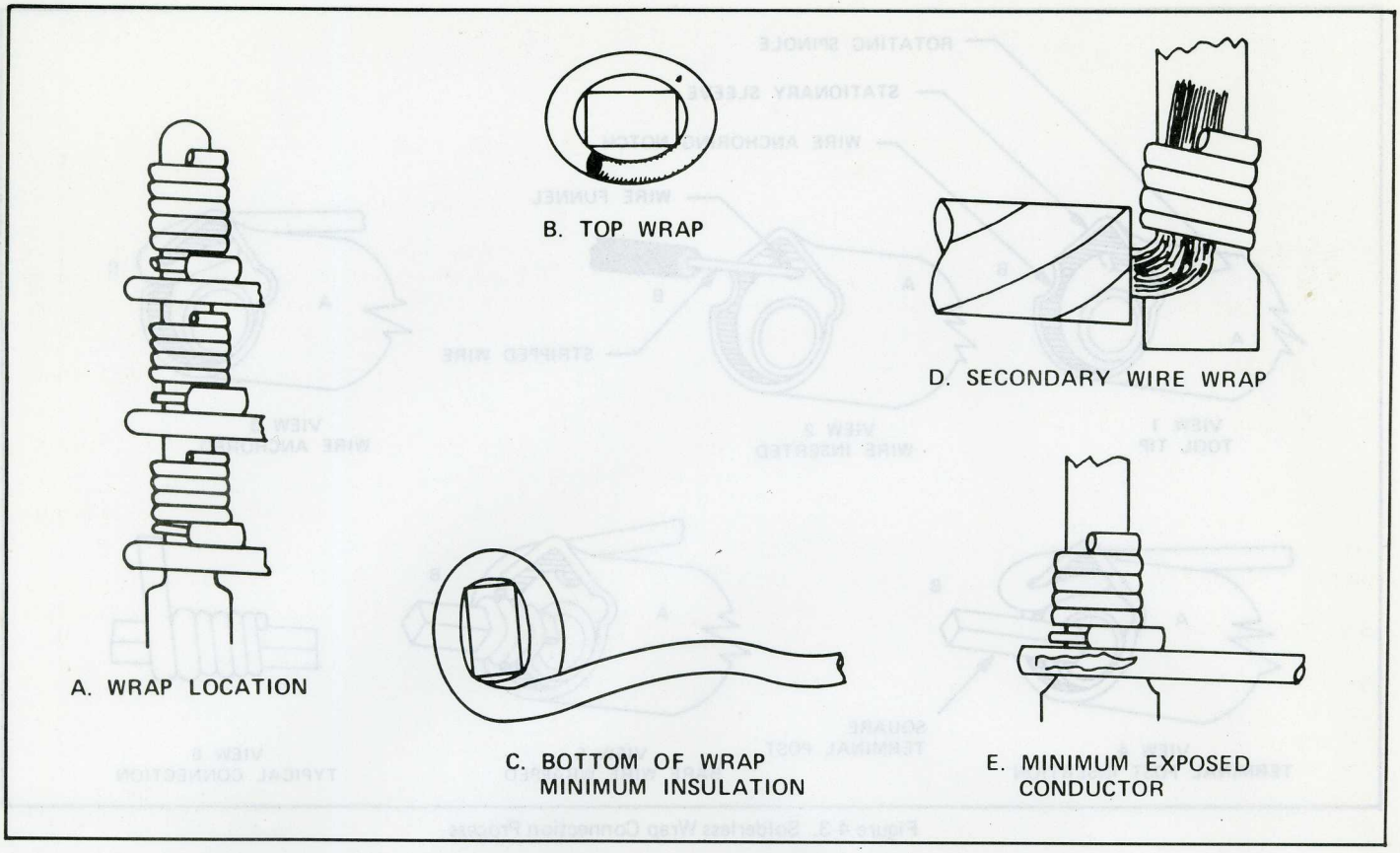


Figure 4-5. Recommended Wire Wraps

Table 4-7. Recommended Spare Parts

Card Number	Description	Quantity
160-083278-002	Cable Driver/Terminator	1
160-083289-001	Oscillator	1
160-100026-001	General Register Even	1
160-100069-001	Cable Terminator	1
160-100078-003	Second TTL Quad Two Input NAND	1
160-100079-001	H.S. One-Shot	1
160-100222-001	Bipolar Receiver	1
160-100223-001	Bipolar Driver	1
160-900020-003	Second Dual Four Input NAND	1
160-900022-003	Second JK Flip-Flop AND Inputs	1
160-900023-003	Second Dual JK Flip-Flop Common Clock	1
160-900024-003	Second Dual JK Flip-Flop Separate Clocks	1
160-900029-003	Second Hex Inverter	1
160-900030-003	Second Triple Three NAND	1
160-083278-003	*Terminator/Driver	1
160-100069-002	*Terminator	1
160-900043-000	Mixed Logic No. 7	1

*Current Mode Option Only

SECTION V

PERFORMANCE TESTING AND FAILURE ANALYSIS

5-1 INTRODUCTION

5-2 This seciton contians information pertianing to the performance testing and failure analysis of the SYSTESM Communications Modem Interface.

5-3 PERFORMANCE TESTING

5-4 The following test procedures are provided for checking the operation of the communications modem interface unit. The first procedure tests the operation of the interface unit with the data modem and the second procedure tests the operation of the unit by itself.

5-5 TEST ONE

5-6 The following procedure tests the operation of the communications modem interface and the data modem. This procedure may be used for the initial checkout of the interface unit, or any time that a problem is suspected in either the interface unit or the data modem. Figure 5-1A is a simplified block diagram of the test setup.

a. Connect a jumper from the transmit output to the receive input on the communication link side of the data modem. Refer to the technical manual provided with the data modem for details and circuit loading information.

b. Apply power to the computer, the interface unit, and the data modem.

c. Manually load the program provided in table 5-1 into the computer.

d. Depress the START switch on the computer control panel.

e. Manually load data bits into the computer using the entry toggle switches and observe the bits being displayed in the B-Register.

f. Remove the jumper from step a.

5-7 TEST TWO

5-8 The following procedure is provided to test the operation of the communications modem by itself. This procudure is

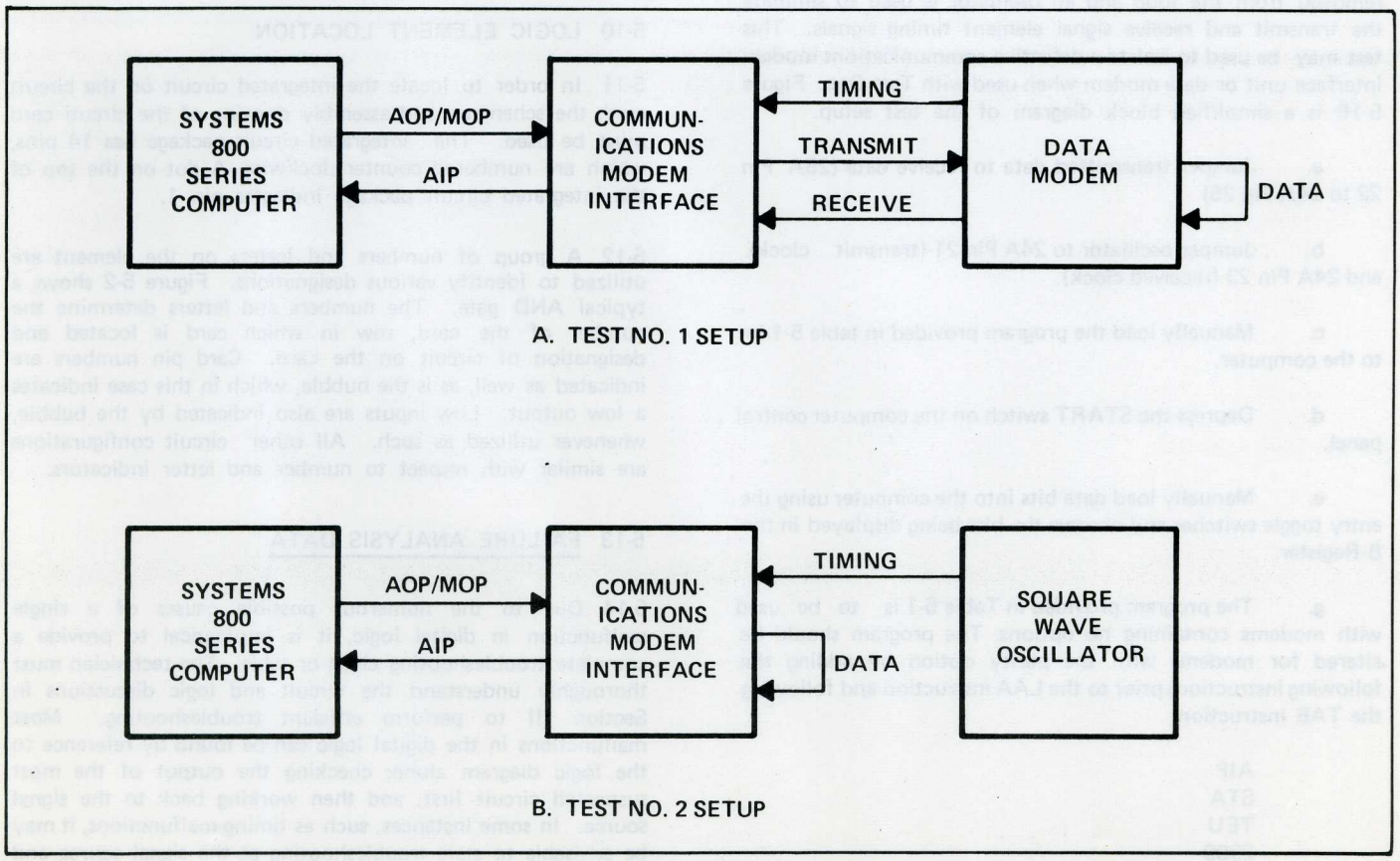


Figure 5-1. Performance Test Setup

Table 5-1. Communications Modem Interface Test Program

Instruction	Address	Remarks
STRT CEU	'43,W	
DATA	'4460	
TEU	'43	Use this TEU only if using a data set otherwise
DATA	'40000	No op this TEU.
BRU	*-2	
MOP	'43,W	
DATA	——	First and Second Sync Words
LCS		
AOP	'43,W	
AIP	'43,W	
TAB		
LAA	X	
STA	Y	
IMS	Y	
BRU	*-1	
BRU	START	
X DATA	'170000	
Y DATA	0	

similar to that of Test One except that the data modem is removed from the loop and an oscillator is used to simulate the transmit and receive signal element timing signals. This test may be used to isolate a defective communications modem interface unit or data modem when used with Test One. Figure 5-1B is a simplified block diagram of the test setup.

a. Jumper transmitted data to receive data (25A Pin 22 to 24A Pin 25)

b. Jumper oscillator to 24A Pin 21 (transmit clock) and 24A Pin 23 (received clock).

c. Manually load the program provided in table 5-1 into the computer.

d. Depress the START switch on the computer control panel.

e. Manually load data bits into the computer using the entry toggle switches and observe the bits being displayed in the B-Register.

g. The program provided in Table 5-1 is to be used with modems containing no options. The program should be altered for modems with the parity option by adding the following instructions prior to the LAA instruction and following the TAB instruction.

```
AIP
STA
TEU
2000
HLT
```

5-9 CIRCUIT ANALYSIS

5-10 LOGIC ELEMENT LOCATION

5-11 In order to locate the integrated circuit on the circuit card, the schematic and assembly drawing of the circuti card must be used. The integrated circuit package has 14 pins, which are numbered counter-clockwise. A dot on the top of the integrated circuit package indicates pin 1.

5-12 A group of numbers and letters on the element are utilized to identify various designations. Figure 5-2 shows a typical AND gate. The numbers and letters determine the number of the card, row in which card is located and designation of circuit on the card. Card pin numbers are indicated as well, as is the bubble, which in this case indicates a low output. Low inputs are also indicated by the bubble, whenever utilized as such. All other circuit configurations are similar with respect to number and letter indicators.

5-13 FAILURE ANALYSIS DATA

5-14 Due to the numerous possible causes of a single malfunction in digital logic, it is impractical to provide a complete troubleshooting chart or table. The technician must thoroughly understand the circuit and logic discussions in Section III to perform efficient troubleshooting. Most malfunctions in the digital logic can be found by reference to the logic diagram alone; checking the output of the most suspected circuit first, and then working back to the signal source. In some instances, such as timing malfunctions, it may be advisable to start troubleshooting at the signal source and then proceed toward the output.

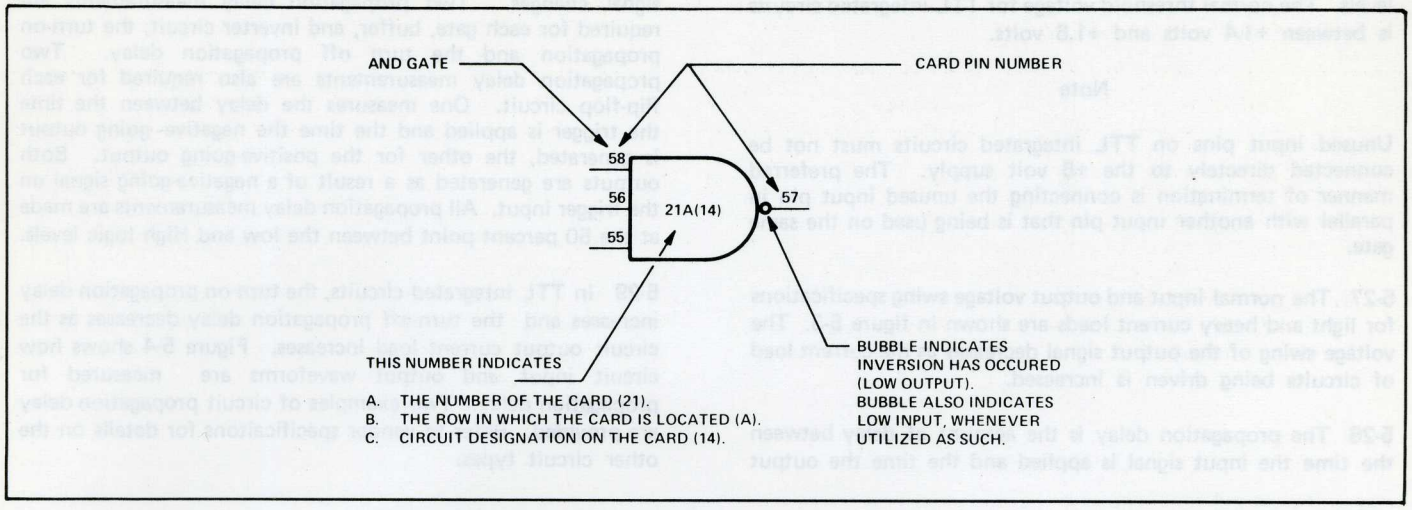


Figure 5-2. Card and Element Location

5-15 The following steps often correct malfunctions before it becomes necessary to check circuit waveforms:

a. Insure that the circuit cards are firmly installed in the swing plane connectors.

b. Check the input and output connectors.

c. Check the output voltages of the power supplies.

d. Check the fuses.

e. Check circuit card locations.

5-16 If the malfunction has not been corrected after the above steps have been performed, a faulty circuit card must be located.

5-17 It is often helpful to disable a circuit when troubleshooting digital logic. A typical example is a flip-flop that is normally changing state and is bothersome when tracing a signal. The flip-flop circuits can be disabled by grounding the output.

5-18 It is safe to assume that nearly all malfunctions of a digital circuit card are due to the failure of an integrated circuit.Once the faulty circuit card has been located, a unit may be returned to normal operation by replacing the faulty card with one from the supply of spare cards.

5-19 DIGITAL CIRCUIT COMPONENT TESTING

5-20 To prevent erroneous indications of a malfunction, and to properly view a valid malfunction, it is imperative that all test equipment is properly connected. In addition, due to the low current requirements of digital logic circuits, improperly connected test equipment may cause malfunctions.

5-21 Whenever possible, the circuit components should be tested with component mounted on the card, and the card installed in its normal operating position in the unit. For ease of troubleshooting the digital circuits, a circuit card extender may be used to extend the card beyond the adjoining circuit card. This makes the circuit card components easily accessible to the technician.

5-22 The card involved is removed from the circuit card connector. A card extender (part number 160-100005-001) is inserted into the circuit card connector and the card is then inserted into the card extender. Signals on the integrated circuit packages may now be monitored.

CAUTION

Before removing or inserting a circuit card, the power must be turned off. If a circuit card is removed or inserted with power on, the components on the card may be damaged.

5-23 Due to the close proximity of the circuit cards, care should be taken not to allow the cards to touch one another while the power is on. Care should also be taken when placing probes on the integrated circuit pins so that the pins are not shorted together.

5-24 The circuits are comprised primarily of transistor-transistor logic (TTL) integrated circuit packages. Voltage tests can be performed on the circuits using either a voltmeter or an oscilloscope. Caution must be taken to prevent the application of excissive current to the circuits from the test equipment.

5-25 CIRCUIT LOADING AND PROPAGATION DELAY

5-26 The intergrated circuits can be tested for voltage swing and propagation delay. The output voltage swing for all TTL integrated circuits should be from 0 (+0.25 to +0.5) volts to +5 (+35 to +4.5) volts. The two logic levels are normally referred to as High level and Low level or ONE level and ZERO

levels. The normal threshold voltage for TTL integrated circuits is between +1.4 volts and +1.8 volts.

Note

Unused input pins on TTL integrated circuits must not be connected directely to the +5 volt supply. The preferred manner of termination is connecting the unused input pin in parallel with another input pin that is being used on the same gate.

5-27 The normal input and output voltage swing specifications for light and heavy current loads are shown in figure 5-3. The voltage swing of the output signal decreases as the current load of circuits being driven is increased.

5-28 The propagation delay is the amount of delay between the time the input signal is applied and the time the output signal changes. Two propagation delay measurements are required for each gate, buffer, and inverter circuit; the turn-on propagation and the turn off propagation delay. Two propagation delay measurements are also required for each flip-flop circuit. One measures the delay between the time the trigger is applied and the time the negative- going output is generated, the other for the positive-going output. Both outputs are generated as a result of a negative-going signal on the trigger input. All propagation delay measurements are made at the 50 percent point between the low and High logic levels.

5-29 In TTL integrated circuits, the turn-on propagation delay increases and the turn-off propagation delay decreases as the circuit output current load increases. Figure 5-4 shows how circuit input and output waveforms are measured for propagation delay. Two examples of circuit propagation delay are provided. Refer to vendor specificaitons for details on the other circuit types.

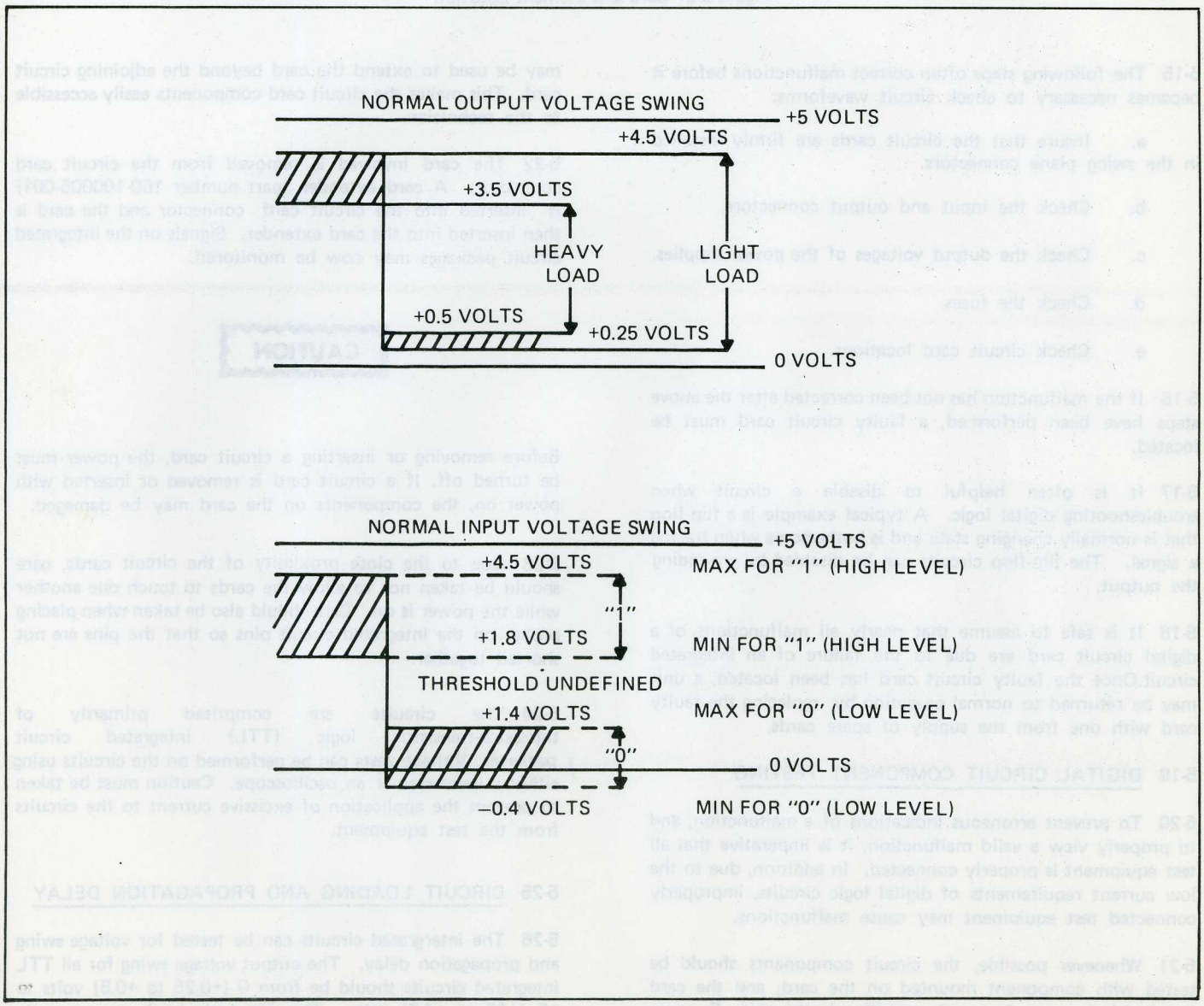
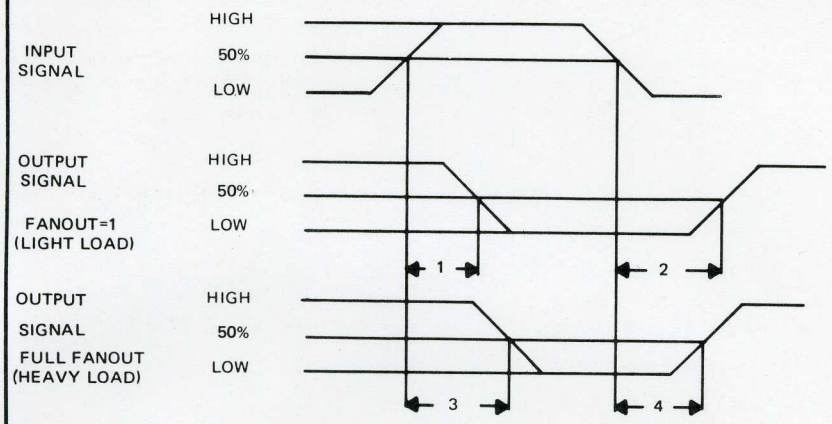


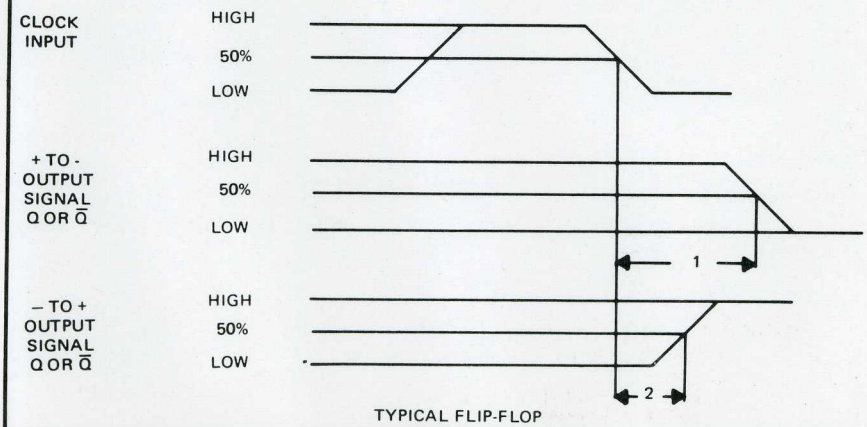
Figure 5-3. Normal Input and Output Voltage Swing Specifications

TYPE CIRCUIT	CAP. LOAD	TEMP.	TEST 1	TEST 2	TEST 3	TEST 4
SG 132 BUFFER	500 PF	+50 C	18 NSEC.	21 NSEC.	20 NSEC.	20 NSEC.
SC 133 BUFFER	500 PF	+50° C	18 NSEC.	21 NSEC.	21 NSEC.	20 NSEC.



BUFFER CIRCUIT

TYPE CIRCUIT	CAP. LOAD	TEMP.	TEST 1	TEST 2
SF 52/53 FLIP-FLOP	200 PF	+25 C	40 NSEC.	22 NSEC.



TYPICAL FLIP-FLOP

Figure 5-4. Integrated Circuit Propagation Delay (TTL Logic)

SEL SYNCHRONOUS MODEM INTERFACE I/C AND TRANSISTOR CROSS REFERENCE

INTEGRATED CIRCUITS

SEL PART NO.	IC PART NO.	MOTOROLA SUBSTITUTE PART NO.
252-115413-201	RF132D	MC2024L
252-115420-201	RF202D	MC2011L
252-115008-201	RG82D	MC426L
252-115412-301	RG123D	MC456L
252-115022-201	RG222D	MC2001L
	TG222J	
252-115022-301	RG223D	MC2051L
252-115024-201	RG242D	MC2003L
	TG242J	
252-115038-201	RG382D	
252-115412-201	TG122D	MC2023L
252-115032-201	TG322J	MC2007L

IC Letter Designation RF, RG, TF, TG, etc. First letter indicates manufacturer, R = Raytheon, T = Transitron. Second letter indicates type of I/C, F = FlipFlop, G = Gate.

TRANSISTORS

SEL PART NO.	TRANSISTOR NO.
250-122369-002	2N2369A
	2N3227
250-123251-001	2N3251
250-123947-001	2N3947

5/28/75