SYSTEMS
ENGINEERING LABORATORIES

TECHNICAL MANUAL

Synchronous Communications
Modem Interface Unit

August 17

306-701630-000
Volume 2 of 2

6901 West Sunrise Blvd., Fort Lauderdale, Florida 33313
Area Code 305 587-2900

SPECIFICATION SHEET

Publication Cut Off Data August 11, 1971

Wire List Information				
Description	Drawing Number	Wire List Number	Revision Level	ECO Change Level
Synchronous Modem Interface	130-100659	411-100659	000	B

Engineering Change Orders Incorporated
None

SYSTEMS Form No. 667

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SECTION VI

ASSEMBLIES AND CIRCUIT CARDS

6-1 INTRODUCTION

6-2 This section contains information pertaining to the major assemblies, circuit cards, and components used in the system. Included are Systems Engineering Laboratories designation conventions, major assembly drawings, circuit card schematic and assembly drawings, parts lists, and circuit card descriptions, specifications, and adjustment procedures where applicable.

6-3 DESIGNATION CONVENTIONS

6-4 CABINETS AND MAJOR ASSEMBLIES

6-5 The methods used in designating major units in Systems Engineering Laboratories systems provide for easy location and identification of components within the system from the logic drawings. Typical designations are illustrated in figure 6-1. Cabinets are numbered 1, 2, 3, etc., from left to right when facing the front. The major units, such as control panels, power supplies, patch panels, and card files are lettered F or R depending upon whether the unit is accessible from the front or rear of the cabinet. The major units are also numbered from top to bottom. The major unit designation is always preceded by the cabinet designation number. A major unit designation of 2F5 indicates that the unit is located in the second cabinet, the fifth unit from the top, in the front of the cabinet. Units located in the middle of the cabinet are further designated with the letter A. The designation of 2F1A indicates that the unit is located behind unit 2F1.

6-6 Vertically mounted card trays are numbered from left to right. As an example, unit 1F3 would be located in the first cabinet, the third unit over, counting from the left. Units below a vertical tray continue the sequence.

6-7 Circuit Cards

6-8 The circuit cards are mounted vertically in parallel files in the card trays. The circuit cards are numbered from front to rear within each card file. The card files are lettered alphabetically from left to right in horizontally mounted card trays and from top to bottom in vertically mounted card trays. The rows are designated by letters (A, B, C, etc.) from top to bottom. The mounting connections in each row are numbered (1, 2, 3, etc.) from left to right, as viewed from the wiring side of the plane. A designation number of 9C indicates the card in the ninth connector from the left, in the third row of connectors from the top.

6-9 Circuit Card Test Points

6-10 Most circuits on the general purpose circuit cards are provided with at least one test point. The test points are located on the component side of the card and are numbered (1, 2, 3, etc.) from top to bottom when the card is installed. A designation numbe 9C(3) on the logic diagram indicates the circuit associated with the third test point on the card in connector 9C.

6-11 All interconnections between the circuit cards are made at the card mounting connectors. Each connector is equipped with 29 pins, which are numbered 1 through 29 from the bottom to the top when the card is installed. A designation number of 6C5 indicates the fifth pin from the bottom on the sixth card in the third file of cards from the top.

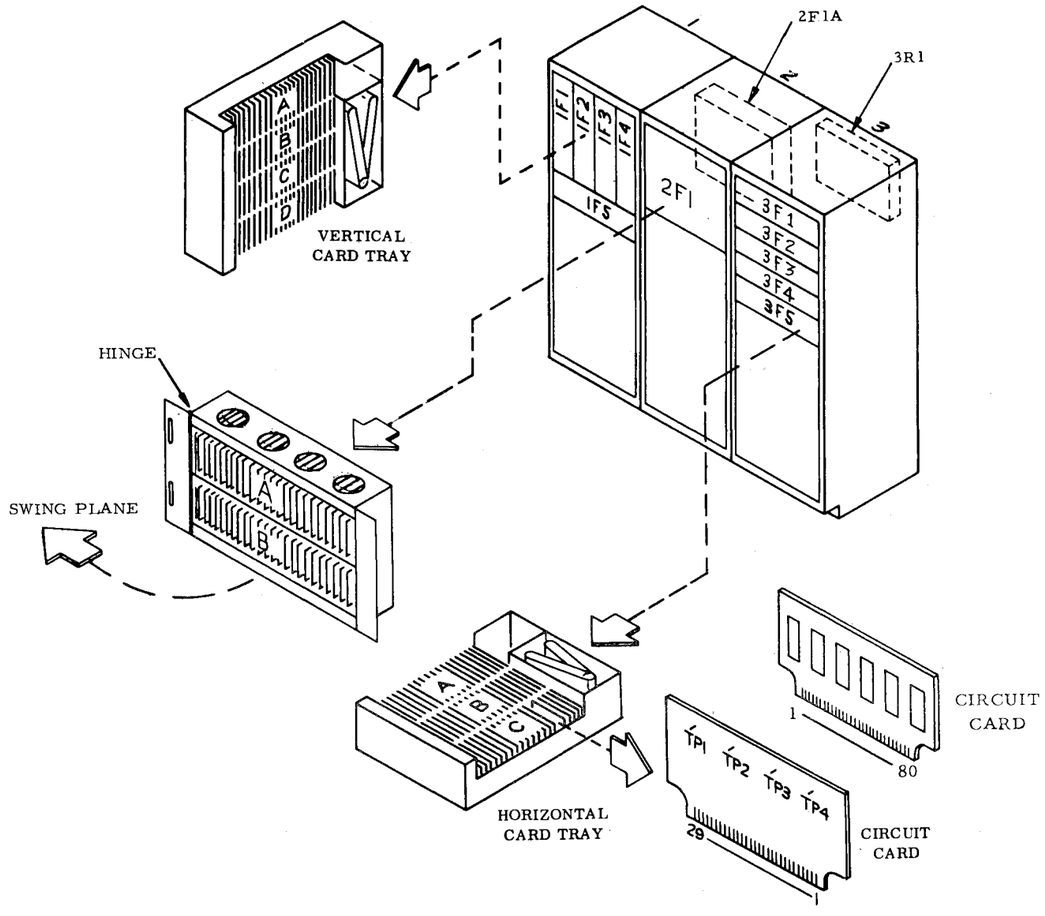
6-12 In systems which contain circuit cards that require 80 pin connectors, each connector contains 80 pins, which are numbered 1 through 80 from the top to the bottom when the card is installed. A designation number of 6C5 indicates the fifty pin from the top on the sixth card in the third file of cards from the top.

6-13 Connectors

6-14 The connectors, consisting of a plug and a receptacle, are designated by the capital letter P followed by a number. Normally, the plug portion of the connector is mounted on the back of the card tray and is identified as P1, P2, P3, etc., and the receptacle is part of the interconnecting cable assembly between the card trays.

6-15 All I/O cables attach to a connector panel located at the bottom rear of the cabinet. The computer I/O bus extension cable is attached to the peripheral device using a 104-pin connector. The male half of the connector (designated P1) provides for connecting the cable from the computer I/O bus. The female half of the connector (designated P2) provides for connecting a cable which extends the I/O bus to the next peripheral device.

6-16 If the peripheral device contains block transfer control (BTC) logic or priority interrupt (PI) circuits in addition to the standard I/O interrupts, 50-pin connectors (designated P3, P4, etc., as required) are used to connect the cables for this logic. The 50-pin cables connect in the same fashion as the 104-pin I/O bus extension cables.



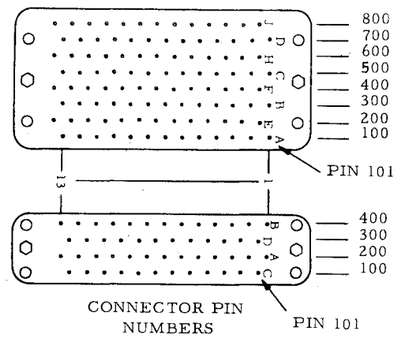


Figure 6-1. Designation Conventions (Typical)

A 3003

6-17 Connector Pin Numbers

6-18 The pins on the 50-pin and 104-pin connectors are lettered alphabetically. However, to eliminate the necessity of having to read a letter to locate a particular pin, the pins are designated by numbers. The pins are arranged in rows of 12 and 13 pins each and are designated 1 through 12 or 1 through 13, respectively. The 50-pin connectors contain four rows which are assigned 100, 200, 300, and 400 series numbers. The 104-pin connectors contain eight rows which are assigned 100 through 800 series numbers. On the 50-pin connectors, pins C, A, D, and B are designated 101, 201, 301, and 401, respectively. On the 104-pin connectors, pins A, E, B, F, C, H, D, and J are designated 101, 201, 301, 401, 501, 601, 701, and 801 respectively.

6-19 ASSEMBLIES AND CIRCUIT CARDS

6-20 A complete set of assembly drawings, with parts lists is provided in this section for all major assemblies and circuit cards contained in the system. The drawings are grouped and presented in the following order:

- Final Assembly
- Major Assemblies
- Circuit Cards

6-21 FINAL ASSEMBLY AND MAJOR ASSEMBLY DRAWINGS

6-22 The first mechanical assembly drawing presented in this section is the final assembly. This is followed by the major assembly drawings, which are arranged in numerical order. Included here are the drawings which show the card location and complement of each logic plane.

6-23 CIRCUIT CARDS

6-24 The third group of drawings in this section is the circuit cards. These drawings are arranged in numerical order and include the following information:

- Circuit Card Schematic
- Circuit Card Assembly
- Parts List
- Circuit Description
- Specifications
- Adjustment Procedures (if applicable)

6-25 Dash numbers are used to distinguish between variations of a basic type of assembly or circuit card (for example: 8501-1, -2). The variations are reflected in the parts lists, which indicate the quantity of a particular component for the different dash numbers. Refer to the card location drawings to determine the dash number of a circuit card used for a particular application.

6-26 Unless noted otherwise, circuit card resistors are carbon composition and are rated at 5 percent, 1/4 watt.

6-27 ABBREVIATIONS

6-28 Abbreviations for reference designators and descriptions used in the parts lists are as follows:

6-29 Reference Designators

C#	-	Capacitor
CR#	-	Diode
R#	-	Potentiometer and Fixed Resistor
Q#	-	Transistor
IC#	-	Integrated Circuit

6-30 Descriptions

A/R	-	As Required
N/R	-	Not Used or Required
S.S.	-	Stainless Steel
MF	-	Metal Film
DC	-	Deposit Carbon
MG	-	Metal Glaze
W/W	-	Wire Wound

ERN 123-2 DATE 10-8-70 REV –

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			Fort Lauderdale, Florida 33310	CODE IDENT	SHEET 1 OF 2 SHEETS	REV
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ENGR	[illegible]	10-8-70				
APPD	[illegible]	10-9-70	USED ON: 701620			

LTR	REVISION DESCRIPTION	DATE	APPD	LTR	REVISION DESCRIPTION	DATE	APPD

RECORD OF REVISION STATUS OF EACH SHEET

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LM 105-100063

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LIST of MATERIAL	Systems Engineering Laboratories	20886	LM 105-100063	
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1	X	1	107-100299-002	SWINGPLANE ASS'Y		2 ROW
2	X	1	107-100349-003	MODULE ASSEMBLY		2 ROW
3	REF	REF	141-100231-000	CARD LOCATION		
4	REF	REF	411-100473-001	WIRE LIST		
5	X	1	144-100210-001	CABLE ASSEMBLY		
6	1	1	107-015939-002	P/S CHASSIS ASS'Y		
7	2	2	107-015929-001	LOW VOLT. VAR. P/S CHAS. ASSY		
8	1	1	107-015929-002	LOW VOLT. VAR. P/S CHAS. ASSY		
9	2	2	110-100019-001	PLATE, WIRING TIE OFF		
10	2	2	110-100319-001	ANGLE, I/O MTG.		
11	1	1	110-100414-002	I/O PANEL, (2) 104 PIN CONN		
12	1	1	110-100411-004	I/O PANEL, (2) 50 PIN CONN		
13	1	1	110-100410-004	I/O PANEL, (2) 50 PIN CONN		
14	1	1	116-016676-003	LABEL		
15	22	22	201-300001-009	WASHER, FLAT #6		
16	10	10	201-300003-003	WASHER, SPLIT LOCK #6		
17	10	10	201-200011-003	NUT, PLAIN HEX #6-32		
18	12	12	201-100017-018	SCREW, #6 TAPPING		
19	1	X	107-100300-001	SWINGPLANE ASS'Y		1 ROW
20	1	X	107-100349-001	MODULE ASSEMBLY		1 ROW
21	1	X	144-100210-002	CABLE ASSEMBLY		

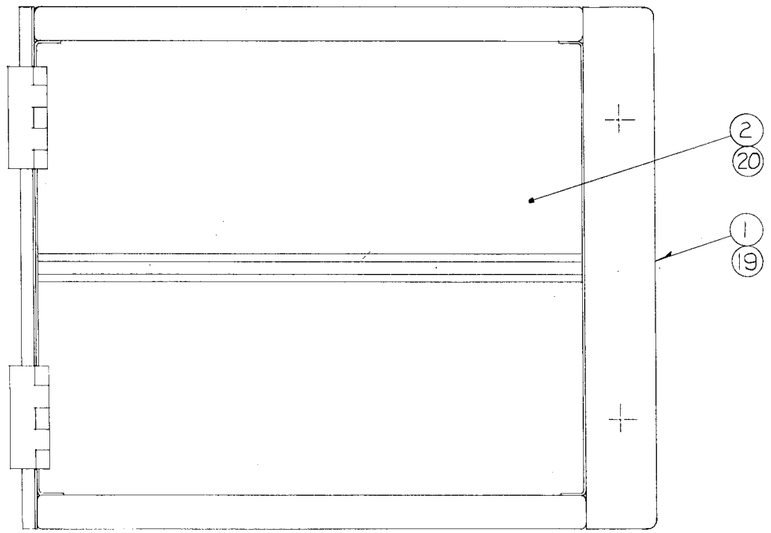
LM 105-100063

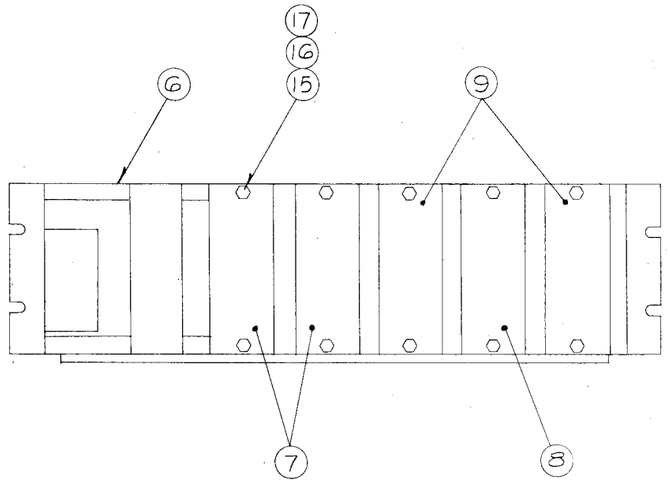
S.E.L. Form 365-2A

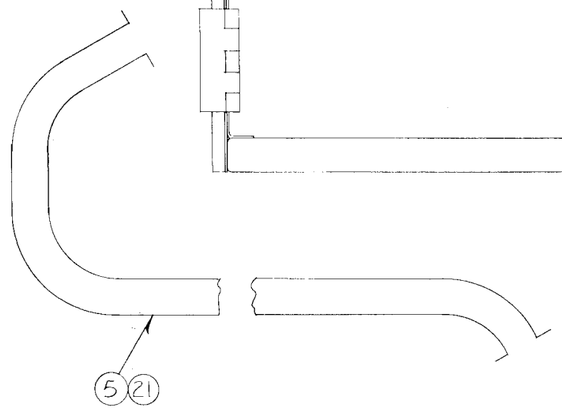
ERN 123-2
DATE 10-8-70 REV- 1

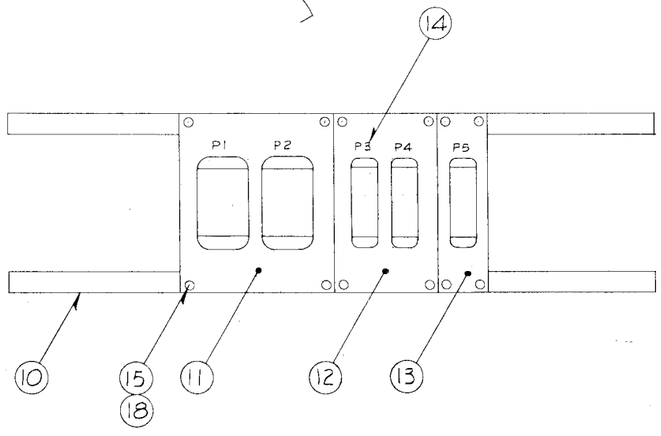
REVISIONS

LTR	DESCRIPTION	DATE	APPROVED









APPLICABLE DOCUMENT
LM-105-100063

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UNLESS OTHERWISE SPECIFIED
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TOLERANCES ON

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12 TO 24	± .03	± .010
OVER 24	± .06	± .015
ANGLES ± 0° 30'		

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FINISH: H

		DATE
DRAWN	Schmandrak	9-11-70
CHECKED		
ENGR		10.8.70
PROJ ENGR		11/6/70
APPROVED		10.8.70
APPROVED		

Systems Engineering Laboratories
Fort Lauderdale, Florida

SYN. DATA MODEM ASS'Y

SIZE	CODE IDENT NO.	DWG NO.
D	20886	105-100063

SCALE H | 768010 | SHEET 1 OF 1

LIST of MATERIAL			Systems Engineering Laboratories	ERN	DATE	REV
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ENGR	R. BALDWIN	9-15-67		ITEM NOMENCLATURE: LOW VOLTAGE VARIABLE POWER SUPPLY CHASSIS ASS'Y		
APPD	M.R. ZUBER	9-15-67	USED ON:			

LTR	REVISION DESCRIPTION	DATE	APPD	LTR	REVISION DESCRIPTION	DATE	APPD
L	71-437; LM ADDED N.NERO	6-21-71	AB				

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LM107-015929

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LIST of MATERIAL	Systems Engineering Laboratories	20886	LM107-015929	L
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1	1	1	160-083184	REGULATOR ASS'Y		
2	1	1	110-015844	CHASSIS		
3	X	1	110-016016	HEAT SINK		
4	1	1	110-016017	HEAT SINK		
5	1	1	110-016018	HEAT SINK		
6	1	1	116-012027-001	IDENTIFICATION TAG PART MODEL & SERIAL NO.		
7	REF	REF	D53280	WIRING DIAGRAM, LOW VOLTAGE VARIABLE		
8	1	1	223-100001-004	CLAMP CABLE (BIRNBACH)		
9	1	2	223-200002-001	CLIP COMPONENT (AUGUT)		
10	1	1	264-300005-001	FUSE BLOCK HOLDER		
11	1	1	259-700008-007	BLOCK TERM. (E.T.C. INC)		
12	1	1	259-700002-008	STRIP TERM. (H.H. SMITH)		
13	4	4	223-500001-016	TERMINAL INSUL. (AMP)		
14	2	6	223-500001-019	TERMINAL INSUL. (AMP)		
15						
16	2	2	223-500001-008	TERMINAL INSUL. (AMP)		
17	13	13	223-300001-001	TIE CABLE (PANDUIT)		
18	1	1	259-300007-004	CONNECTOR, RECEPTACLE (AMPHENOL)		
19	X	4	6549B-8	INSULATOR FLANGED (BIRNBACH)		
20	2	2	201-300004-003	WASHER INTERNAL TOOTHED CRES. No. 6		
21	14	10	201-300006-001	WASHER SHOULDER NYLON (DABURN)		

LM107-015929

S.E.L. Form 365-2A

LIST of MATERIAL	Systems Engineering Laboratories	20886	LM107-015929	L
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22	18	24	201-300002-005	WASHER FLAT CRES NO 6		
23	10	12	201-200017-002	NUT HEX CRES NO 6		
24						
25						
26						
27	4	1	201-100010-032	SCREW PAN HEAD 6X32 X 3/4		
28	1	3	201-100010-033	SCREW PAN HEAD 6X32 X 7/8		
29	6	8	201-100010-029	SCREW PAN HEAD 6X32 X 7/16		
30	2	4	201-100010-030	SCREW PAN HEAD 6X32 X 1/2		
31	8	8	201-300002-003	WASHER FLAT CRES NO 4		
32	X	1	116-016691-005	LABEL (15A)		
33	2	2	201-100010-031	SCREW PAN HEAD CRES 4-40 X 9/16		
34	AR	AR	223-300002-003	GROMMET STRIP		
35	AR	AR	258-500001-061	WIRE-INSUL. ELEC. SINGLE STRANDED		
36	AR	AR	258-500001-082	WIRE-INSUL. ELEC. SINGLE STRANDED		
37	AR	AR	258-500001-083	WIRE-INSUL. ELEC. SINGLE STRANDED		
38	AR	AR	265-400001-009	INSULATION SLEEVING TEFLON		
39	AR	AR	265-600002-004	INSULATION SLEEVING POLYOLEFIN		
40	AR	AR	209-200001-001	COMPOUND HEAT SINK		
41	1	1	253-100010-103	RESISTOR 18K 1/4W 5%		
42	6	6	201-200018-002	4-40 PLAIN NUT HEX CRES		

LM107-015929

S.E.L. Form 365-2A

LIST of MATERIAL	Systems Engineering Laboratories	20886	LM107-015929	L
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ITEM NO.	QTY REQ'D PER DASH NO. 002	001	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	REFERENCE DESIGNATION	REMARKS
43	X	1	264-100001-016	FUSE GLASS TUBE		
44	1	X	264-100001-002	FUSE GLASS TUBE		
45	4	4	251-100080-001	RECTIFIER SILICONE		
46	1	1	251-124168-001	RECTIFIER SILICON		
47	1	1	254-100440-039	CAPACITOR-SOLID ELEC.-TANT.		
48	2	1	250-123772-001	TRANSISTOR SILICON		
49	1	2	254-100010-114	CAPACITOR 13,000 MFD SPRAGUE		
50	2	3	253-100190-002	RESISTOR POWER		
51	1	1	253-1000190-001	RESISTOR POWER		
53	X	1	116-016676-081	LABLE BLACK ON WHITE		
54	5	5	201-300002-009	WASHER FLAT #10 CRES		
55	REF	REF	D53159	SCHEMATIC LOW VOLTAGE PWR. SUP.		
56	X	1	250-123771-001	TRANSISTOR		
57	2	2	201-300002-015	SCREW PAN HEAD CRES 4-40 X 3/8		
58	2	2	201-300002-016	SCREW PAN HEAD CRES 4-40 X 7/16		
59	1		116-016691-016	LABLE (10 AMP)		
60	4	4	201-300002-003	WASHER FLAT CRES NO 4		
61	12	14	201-300014-136	WASHER LOCK-SPLIT NO 6		
62	6	6	201-300014-135	WASHER LOCK-SPLIT NO 4		

LM107-015929

S.E.L. Form 365-2A

ERN
DATE REV 1

REVISIONS

ZONE	LTR	DESCRIPTION	DATE	APPROVED
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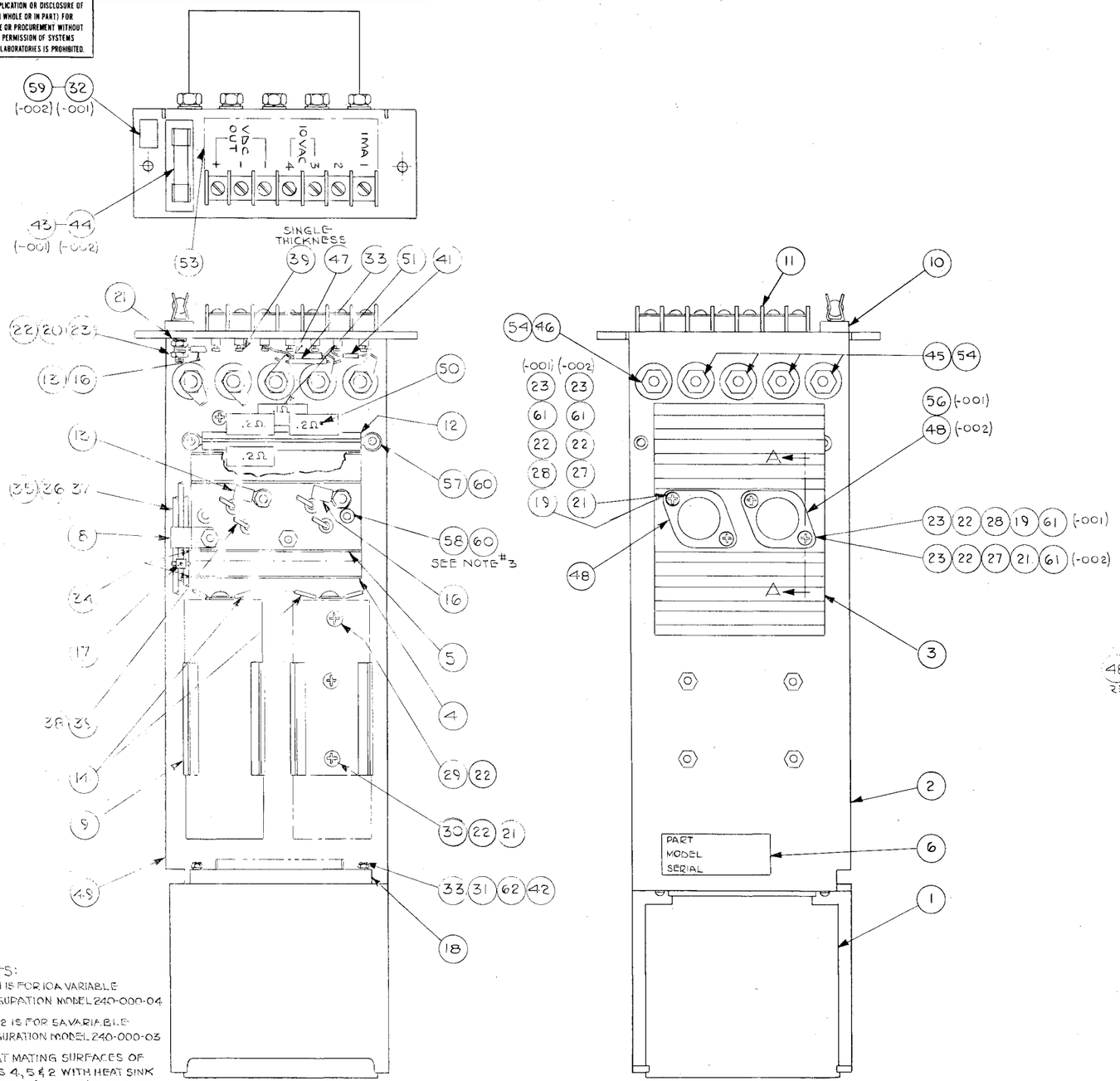
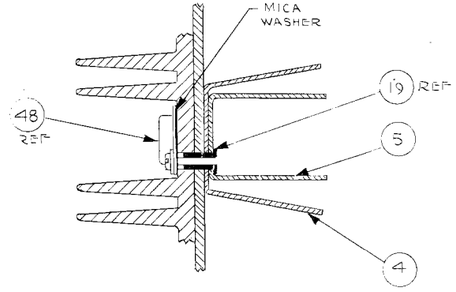


NOTES:
1. -001 IS FOR 10A VARIABLE CONFIGURATION MODEL 240-000-04
2. -002 IS FOR 5A VARIABLE CONFIGURATION MODEL 240-000-03
3. COAT MATING SURFACES OF ITEMS 4, 5 & 2 WITH HEAT SINK COMPOUND (ITEM 40) BEFORE ASSEMBLY.
4. COAT MATING SURFACES OF ITEMS 48, 47, (MICA WASHERS INCLUDED); 3, 2 BEFORE ASS'Y.

-001 SHOWN



SECTION A A
-001 ONLY

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON:		
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UNDER 12	± .02	± .005
12 TO 24	± .03	± .010
OVER 24	± .06	± .015
ANGLES ± 0° 30'		

MATERIAL:

FINISH:

NEXT ASSY	USED ON
APPLICATION	

		DATE
DRAWN	IGLEHEART	8-29-67
CHECKED	CRAWLEY	9-14-67
ENGR		
PROJ ENGR	R. BALDWIN	9-15-67
APPROVED	M. R. ZUBER	9-15-67
APPROVED		

Systems Engineering Laboratories
Fort Lauderdale, Florida

LOW VOLTAGE VARIABLE POWER SUPPLY CHASSIS ASSEMBLY

SIZE	CODE IDENT NO.	DWG NO.
D	20886	107-015929

SCALE | REV LTR L | SHEET

LIST of MATERIAL			Systems Engineering Laboratories	20886	LM107-015939	H
PREP	IGLEHEART	DATE 9-8-67	Fort Lauderdale, Florida 33310	CODE IDENT	SHEET 1 OF 7 SHEETS	REV
CHK	E.W. PICARD	9-11-67	ITEM NOMENCLATURE: POWER SUPPLY CHASSIS ASSY			
ENGR	R. BALDWIN	9-12-67				
APPD	M.R. ZUBER	9-12-67	USED ON: MDL 240			

LTR	REVISION DESCRIPTION	DATE	APPD	LTR	REVISION DESCRIPTION	DATE	APPD
H	INC ECO 71-579 MRV 8-16-71 (CREATED LM)	8/16/71					

RECORD OF REVISION STATUS OF EACH SHEET

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42
H	H	H	H	H	H	H																																				

LM107-015939

S.E.L. Form 365-1

LIST of MATERIAL	Systems Engineering Laboratories	20886	LM107-015939	H
ITEM NOMENCLATURE: POWER SUPPLY CHASSIS ASSY		CODE IDENT	SHEET 2 OF SHEETS	REV

ITEM NO.	QTY REQ'D PER DASH NO. 005	004	003	002	001	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	REFERENCE DESIGNATION	REMARKS
1	1	1	1	1	1	107-015746-001	CHASSIS - P/S		
2	1	1	1	1	1	110-015790-001	BRACKET, LEFT		
3	X	X	1	X	1	110-016025-001	PLENUM		
4	X	X	1	X	1	110-016026-001	COVER, PLENUM		
5	1	1	1	1	1	110-016052-001	PLATE - TERM. MTG.		
6	X	X	1	X	1	110-016027-001	BRACKET - FAN		
7	1	1	1	1	1	223-100001-007	CABLE CLAMP, NYLON		
8	1	1	1	1	1	285-300013-001	EDGE TRIM, PLASTIC GRUMMET 2.19 LONG		BASKETWEAVE
9	X	X	2	X	2	201-700023-022	SPACER #6, 1/4 X 1/2 LONG		
10	1	1	1	1	1	110-015790-002	BRACKET, RIGHT		
11	1	1	1	1	1	259-700017-005	COVER, TERM. BLOCK		
12	15	15	12	10	17	223-500001-016	TERMINAL - INSUL		
13	AR	AR	AR	AR	AR	258-500001-091	WIRE INSUL, 1/C, STRANDED		
14	AR	AR	X	X	AR	265-600002-004	INSUL. SLEEVING POLYOLEFIN		SHRINKABLE
15	AR	AR	AR	AR	AR	223-300001-001	CABLE TIE		
16	X	X	AR	X	AR	203-200003-001	SPRING TAPE, 3/8 X 1/4		RHOPAC
17	X	X	AR	X	AR	203-200005-004	TAPE, PRESSURE SENSITIVE		
18	1	1	1	1	1	116-016691-020	LABEL		
19	1	1	1	1	1	259-700005-005	MARKER STRIP, TERM. BLOCK		
20	1	1	1	1	1	256-000160-001	TRANSFORMER		
21	1	1	X	X	1	256-100006-001	LINE FILTER		

LM107-015939

S.E.L. Form 365-2A

LIST of MATERIAL	Systems Engineering Laboratories	20886	LM107-015939	H
ITEM NOMENCLATURE: POWER SUPPLY CHASSIS ASSY		CODE IDENT	SHEET 3 OF SHEETS	REV

ITEM NO.	QTY REQ'D PER DASH NO. 007	006	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	REFERENCE DESIGNATION	REMARKS
1	1	1	107-015746-001	CHASSIS - P/S		
2	1	1	110-015790-001	BRACKET, LEFT		
3	X	X	110-016025-001	PLENUM		
4	X	X	110-016026-001	COVER, PLENUM		
5	1	1	110-016052-001	PLATE - TERM. MTG.		
6	X	X	110-016027-001	BRACKET - FAN		
7	1	1	223-100001-007	CABLE CLAMP, NYLON		
8	1	1	285-300013-001	EDGE TRIM, PLASTIC GRUMMET 2.19 LONG		BASKETWEAVE
9	X	X	201-700023-022	SPACER #6, 1/4 X 1/2 LONG		
10	1	1	110-015790-002	BRACKET, RIGHT		
11	1	1	259-700017-005	COVER, TERM. BLOCK		
12	12	15	223-500001-016	TERMINAL - INSUL		
13	AR	AR	258-500001-091	WIRE INSUL, 1/C, STRANDED		
14	X	AR	265-600002-004	INSUL. SLEEVING POLYOLEFIN		SHRINKABLE
15	AR	AR	223-300001-001	CABLE TIE		
16	X	X	203-200003-001	SPRING TAPE, 3/8 X 1/4		
17	X	X	203-200005-004	TAPE, PRESSURE SENSITIVE		
18	1	1	116-016691-020	LABEL		
19	1	1	259-700005-005	MARKER STRIP, TERM. BLOCK		
20	1	X	256-000160-001	TRANSFORMER		
21	X	1	256-100006-001	LINE FILTER		

LM107-015939

S.E.L. Form 365-2A

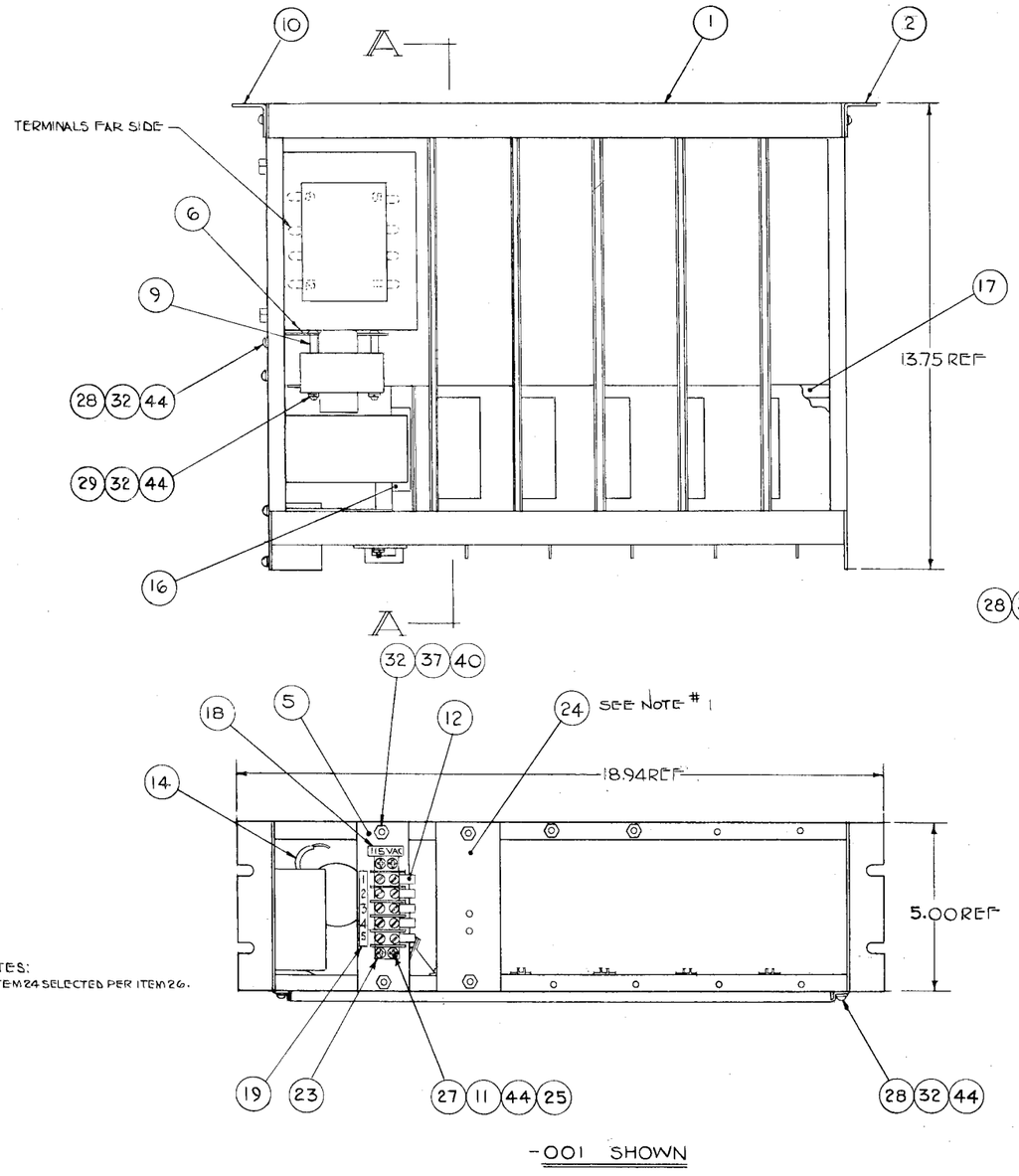
LIST of MATERIAL	Systems Engineering Laboratories	20886	LM 107-015939	H
ITEM NOMENCLATURE: POWER SUPPLY CHASSIS ASSY		CODE IDENT	SHEET 4 OF SHEETS	REV

ITEM NO.	QTY REQ'D PER DASH NO. 005	004	003	002	001	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	REFERENCE DESIGNATION	REMARKS
22	X	X	1	X	1	207-100007-001	BLOWER		
23	1	1	1	1	1	259-700011-005	TERMINAL BLOCK		
24	REF	REF	REF	REF	REF	110-100019-001	TIE OFF PLATE		
25	2	2	2	2	2	259-700018-002	SPRING CLIP		
26	REF	REF	REF	REF	REF	101-100005	240 POWER SUPPLY CONFIG: CONT.		
27	4	4	4	4	4	201-100010-030	SCREW PAN HD 6-32 X 1/2		
28	4	4	10	4	10	201-100010-028	" 6-32 X .38		
29	2	2	2	X	4	201-100010-037	" 6-32 X 1 3/4		
30	4	4	4	4	4	201-100010-045	" 8-32 X .50		
31	X	X	X	4	4	201-100011-063	SCREW PAN HD 10-32 X .50		
32	5	5	15	3	17	201-300002-005	WASHER - FLAT # 6		
33									
34	4	4	4	4	4	201-300002-010	WASHER - FLAT # 10		
35									
36	4	4	4	4	4	201-300014-009	WASHER SPLIT-LOCK # 10		
37	2	2	2	2	2	201-200018-003	NUT - HEX 6-32		
38	4	4	4	4	4	201-200017-003	NUT - HEX 8-32		
39	4	4	4	4	4	201-200016-005	NUT - HEX 10-32		
40	2	2	2	2	2	201-300014-007	WASHER SLIT-LOCK #6		
41	X	REF	REF	REF	REF	134-100115	WIRING DIAGRAM		
42	REF	X	X	X	X	134-100116	WIRING DIAGRAM		

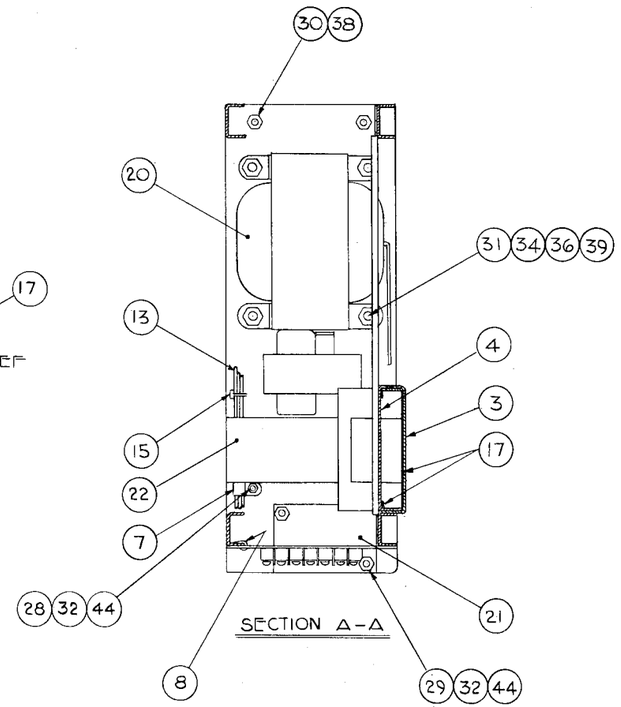
LM107-015939

S.E.L. Form 365-2A

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
H	INC ECO 71-579 PER 8-14-71 (REMOVED LIST OF MATERIAL)	8/15/71	



-001 SHOWN



SECTION A-A

NOTES:
1. ITEM 24 SELECTED PER ITEM 26.

APPLICABLE DOCUMENT
L/M 107-015939

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON		
BASIC DIMENSION	DECIMAL PLACES .XX	.XXX
UNDER 12	± .02	± .005
12 TO 24	± .03	± .010
OVER 24	± .06	± .015
ANGLES ± 0° 30'		

MATERIAL:

FINISH:

DRAWN IGLEHEART	DATE 9-8-67
CHECKED E.W. PICARD	9-11-67
ENGR	
PROJ ENGR R. BALDWIN	9-12-67
APPROVED M.R. ZUBER	9-12-67
APPROVED	

101-100005	
NEXT ASSY	USED ON
APPLICATION	

Systems Engineering Laboratories
Fort Lauderdale, Florida

POWER SUPPLY CHASSIS ASSEMBLY

SIZE	CODE IDENT NO.	DWG NO.	REV
D	20886	107-015939	H

SCALE | SHEET 1 of 1

B 107-015939 H

A

LIST of MATERIAL	Systems Engineering Laboratories	20886	LM107-015939	H
ITEM NOMENCLATURE: POWER SUPPLY CHASSIS ASSY		CODE IDENT	SHEET 5 OF SHEETS	REV

ITEM NO.	QTY REQ'D PER DASH NO. 007	006	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	REFERENCE DESIGNATION	REMARKS
22	X	X	207-100007-001	BLOWER		
23	1	1	259-700011-005	TERMINAL BLOCK		
24	X	REF	110-100019-001	TIE OFF PLATE		
25	2	2	259-700018-002	SPRING CLIP		
26	REF	REF	101-100005	240 POWER SUPPLY CONFIG. CONT.		
27	4	4	201-100010-030	SCREW PAN HD 6-32 X 1/2		
28	3	4	201-100010-028	" 6-32 X .38		
29	X	2	201-100010-037	" 6-32 X 1 3/4		
30	4	4	201-100010-045	" 8-32 X .50		
31	4	X	201-100011-063	SCREW PAN HD 10-32 X .50		
32	3	5	201-300002-005	WASHER-FLAT #6		
33						
34	4	X	201-300002-010	WASHER-FLAT #10		
35						
36	4	X	201-300014-009	WASHER SPLIT-LOCK #10		
37	3	2	201-200018-003	NUT-HEX 6-32		
38	4	4	201-200017-003	NUT- HEX 8-32		
39	4	X	201-200016-005	NUT- HEX 10-32		
40	3	2	201-300014-007	WASHER SLIT-LOCK #6		
41	X	X	134-100115	WIRING DIAGRAM		
42	X	X	134-100116	WIRING DIAGRAM		

LM107-015939

S.E.L. Form 365-2A

LIST of MATERIAL	Systems Engineering Laboratories	20886	LM107-015939	H
ITEM NOMENCLATURE: POWER SUPPLY		CODE IDENT	SHEET 6 OF SHEETS	REV

ITEM NO.	QTY REQ'D PER DASH NO. 005	004	003	002	001	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	REFERENCE DESIGNATION	REMARKS
43	X	X	X	X	X	134-100117	WIRING DIAGRAM		
44	7	7	13	5	15	201-200017-002	NUT, HEX SELF-LOCK 6-32		
45	X	1	1	1	1	118-100018-001	MOUNTING KIT (HDW)		
46	X	X	X	X	X	134-100261-000	WIRING DIAGRAM		

LM107-015939

S.E.L. Form 365-2A

LIST of MATERIAL	Systems Engineering Laboratories	20886	LM107-015939	H
ITEM NOMENCLATURE: POWER SUPPLY CHASSIS ASSY		CODE IDENT	SHEET 7 OF SHEETS	REV

ITEM NO.	QTY REQ'D PER DASH NO. 007	006	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	REFERENCE DESIGNATION	REMARKS
43	X	REF	134-100117	WIRING DIAGRAM		
44	5	7	201-200017-002	NUT, HEX SELF-LOCK 6-32		
45	1	X	118-100018-001	MOUNTING KIT (HDW)		
46	REF	X	134-100261-000	WIRING DIAGRAM		

LM107-015939

S.E.L. Form 365-2A

ERN/74-1 DATE 8-4-71 REV –

LIST of MATERIAL			Systems Engineering Laboratories	20886	LM 141-100312	–
PREP	E. PEREZ-CUBAS	DATE 8-3-71	Fort Lauderdale, Florida 33310	CODE IDENT	SHEET 1 OF 2 SHEETS	REV
CHK				ITEM NOMENCLATURE: CARD LOCATION & COMPLEMENT LIST SYNC MODEM		
ENGR	C.M. Owen	8/10/71				
APPD	C.M. Owen	8/10/71	USED ON: 554102 (704004)			

LTR	REVISION DESCRIPTION	DATE	APPD	LTR	REVISION DESCRIPTION	DATE	APPD

RECORD OF REVISION STATUS OF EACH SHEET

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42

LM 141-100312

S.E.L. Form 365-1A

LIST of MATERIAL	Systems Engineering Laboratories	20886	LM 141-100312	–
ITEM NOMENCLATURE: CARD LOCATION & COMPLEMENT LIST		CODE IDENT	SHEET 2 OF 2 SHEETS	REV

ITEM NO.	QTY REQ'D PER DASH NO.	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	REFERENCE DESIGNATION	REMARKS
1	1	144-100210	CABLE ASSEMBLY		
2	1	160-083289-001	OSCILLATOR		
3	2	160-100026-001	GEN REG EVEN		
4	2	160-100069-001	CABLE TERMINATOR		
5	5	160-100078-003	2 NAND		
6	2	160-100079-001	ONE SHOT		
7	1	144-100294	CABLE ASSEMBLY		SEE NOTE 1.
8	1	144-100293	CABLE ASSEMBLY		
9	3	160-900020-003	4 NAND		
10	1	160-900022-003	JK-AND		
11	3	160-900023-003	JK-CC		
12	4	160-900024-003	JK-SC		
13	5	160-900029-003	HEX INV		
14	3	160-900030-003	3 NAND		
15	1	160-900043-001	LOGIC MIX #7		
16	1	160-083251-000	JUMPER CARD		

LM 141-100312

S.E.L. Form 365-2A

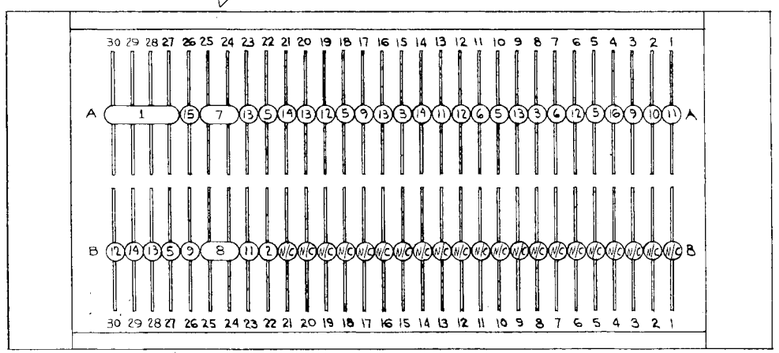
ERN 174-1
DATE 8-4-71 REV- 1

NOTES:
1. FOR CURRENT MODE OPTION (-200) REPLACE THIS CABLE ASS'Y WITH 144-100295-001

SIZE	141-100312	REV.
D		-

REV.	DESCRIPTION	DATE	APPD

(1)



TRAY LOGIC & OR WIRING DIAGRAM LISTING CHART	
15	130-100659-000
No. SHEETS	DRAWING NUMBER

APPLICABLE DOCUMENT
LM 141-100312

LEGEND

- (C/10) CONNECTOR - 104 PIN "AMP" CONNECTOR OCCUPYING CARD POSITION
- (C/50) CONNECTOR - 50 PIN "AMP" CONNECTOR OCCUPYING CARD POSITION
- (N/C) NO CARD - "ELCO" CONNECTOR PRESENT AS SPARE FOR FUTURE CARD EXPANSION
- (U) UN-OCCUPIED, NO CARD OR "ELCO" CONNECTOR PRESENT
- (S) SET BACK - CARD & CONNECTOR REMOVED FOR CLEARANCE OF FRONT PANEL COMPONENTS

Systems Engineering Laboratories
6901 West Sunrise Blvd., Fort Lauderdale, Florida 33310

DR RLW	5/12/71	CARD LOCATION AND COMPLEMENT LIST SYNC MODEM
CHK		
ENGR CMM	8/2/71	
PROJ MM	8/4/71	
APPD		

554102(704004)

CODE IDENT NO.	SIZE		REV.
20886	D	141-100312	

SHEET 1 of 1

ERN 123-1 DATE 9-17-70 REV.

LIST of MATERIAL | **Systems Engineering Laboratories**, Fort Lauderdale, Florida 33310 | 20886 | LM 144-100210 | A

PREP	RENE G.	DATE 7-8-70
CHK	N H	9/17/70
ENGR	A Holm	9/17/70
APPD	Swanson MH	9/17/70

CODE IDENT | SHEET 1 OF 3 SHEETS | REV

ITEM NOMENCLATURE: CABLE ASSY. I/O & BTC SYNC. DATA MODEM INTFC.

USED ON: 772926

LTR	REVISION DESCRIPTION	DATE	APPD
A	71-362 NR 6 5-13-71 E.P.C	5/13/71	ob

RECORD OF REVISION STATUS OF EACH SHEET

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42
A	A	A																																							

LM 144-100210

S.E.L. Form 365-1

LIST of MATERIAL | **Systems Engineering Laboratories** | 20886 | LM 144-100210

ITEM NOMENCLATURE: C.A. I/O & BTC-SYNC. DATA MODEM INTFC. | CODE IDENT | SHEET 2 OF 3 SHEETS | REV

ITEM NO.	QTY REQ'D PER DASH NO. 005	004	003	002	001	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	REFERENCE DESIGNATION	REMARKS
1	1	1	1	1	1	259-500003-002	CONN. 104 PIN F		AMP
2	1	1	1	1	1	259-500003-003	CONN. 104 PIN M		AMP
3	X	1	1	1	1	259-500001-002	CONN. 50 PIN F		AMP
4	X	1	1	1	1	259-500001-003	CONN. 50 PIN M		AMP
5	104	154	154	5	15	259-900010-030	SOCKET, 24-26		AMP
6	116	166	166	166	166	259-900010-029	PIN 24-26		AMP
7	2	2	2	2	2	160-100069-001	CONN. CARD		
8	1	1	1	1	1	160-083278-002	CONN. CARD		
9	AR	AR	AR	AR	AR	258-000940-001	WIRE, # 26 AWG T W/P BLACK/WHITE		W. L. GORE ASS.
10	6	6	6	6	6	223-300008-002	MOUSE TAIL		
11	1	1	1	1	1	259-500001-003	CONN. 50 PIN M		AMP

LM 144-100210

S.E.L. Form 365-2A

LIST of MATERIAL | **Systems Engineering Laboratories** | 20886 | LM 144-100210

ITEM NOMENCLATURE: C.A. I/O & BTC-SYNC. DATA MODEM INTFC. | CODE IDENT | SHEET 3 OF 3 SHEETS | REV

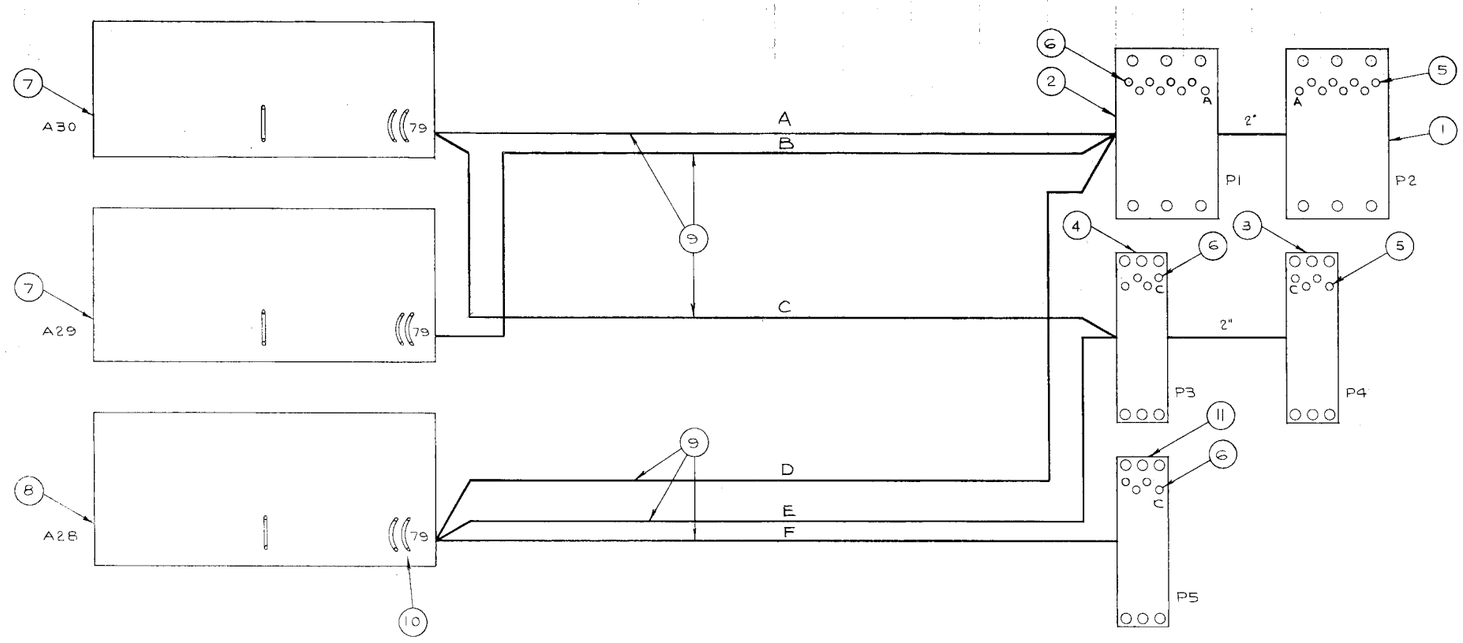
ITEM NO.			QTY REQ'D PER DASH NO. 005	007	006	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	REFERENCE DESIGNATION	REMARKS
1			1	1	1	259-500003-002	CONN 104 PIN F		AMP
2			1	1	1	259-500003-003	CONN 104 PIN M		AMP
3			X	X	X	259-500001-002	CONN 50 PIN F		AMP
4			X	X	X	259-500001-003	CONN 50 PIN M		AMP
5			104	104	104	259-900010-030	SOCKET 24-26		AMP
6			116	116	116	259-900010-029	PIN 24-26		AMP
7			2	2	2	160-100069-001	CONN CARD		
8			1	1	1	160-083278-002	CONN CARD		
9			AR	AR	AR	258-000940-001	WIRE # 26 AWG T W/P BLAK/WHITE		W.L.GORE ASSY
10			6	6	6	223-300008-002	MOUSE TAIL		
11			1	1	1	259-500001-003	CONN 50 PIN M		AMP

LM 144-100210

S.E.L. Form 365-2A

ERN 123-1
DATE 9-17-70 REV- 1

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	71-362 NR. 5-13-71 EP-C	5/13/71	aB



DASH NO. CHART						
DASH NO.	CABLE LENGTH (IN.)					
	A	B	C	D	E	F
-001	26.00	28.00	29.00	30.00	32.00	34.00
-002	50.00	52.00	53.00	54.00	56.00	58.00
-003	74.00	76.00	77.00	78.00	80.00	82.00
-004	98.00	100.00	101.00	102.00	104.00	106.00
-005	26.00	26.00	26.00	26.00	26.00	26.00
-006	50.00	50.00	50.00	50.00	50.00	50.00
-007	74.00	74.00	74.00	74.00	74.00	74.00
-008	78.00	78.00	78.00	78.00	78.00	78.00

FROM	TO	COLOR	AWG	REMARKS
P1/P2-101	A29-1	WHT	26	TWIST
201	2	BLK		
102	3	WHT		
202	4	BLK		
103	5	WHT		
203	6	BLK		
104	7	WHT		
204	8	BLK		
105	9	WHT		
205	10	BLK		
106	11	WHT		
206	12	BLK		
107	13	WHT		
207	14	BLK		
108	15	WHT		
208	A29-16	BLK		
109	A30-1	WHT		
209	2	BLK		
110	3	WHT		
210	4	BLK		
111	5	WHT		
211	6	BLK		
112	7	WHT		
212	8	BLK		
113	9	WHT		
213	A30-10	BLK		
301	A29-17	WHT		
401	18	BLK		
302	19	WHT		
402	20	BLK		
303	21	WHT		
P1/P2-403	A29-22	BLK	26	TWIST

FROM	TO	COLOR	AWG	REMARKS
P1/P2-304	A29-23	WHT	26	TWIST
404	24	BLK		
305	25	WHT		
405	26	BLK		
306	27	WHT		
406	28	BLK		
307	29	WHT		
407	30	BLK		
308	31	WHT		
408	A29-32	BLK		
309	A30-11	WHT		
409	12	BLK		
310	13	WHT		
410	14	BLK		
311	15	WHT		
411	16	BLK		
312	17	WHT		
412	18	BLK		
313	19	WHT		
413	A30-20	BLK		
503	A28-2	WHT		
603	1	BLK		
504	4	WHT		
P1/P2-604	3	BLK		
P5 104	8	WHT		
204	7	BLK		
105	10	WHT		
P5 205	A28-9	BLK		
P1/P2-509	A30-21	WHT		
609	22	BLK		
510	23	WHT		
P1/P2-610	A30-24	BLK	26	TWIST

FROM	TO	COLOR	AWG	REMARKS
P1/P2-511	A30-25	WHT	26	TWIST
611	26	BLK		
512	27	WHT		
612	28	BLK		
513	29	WHT		
613	A30-30	BLK		
701	A29-33	WHT		
801	34	BLK		
702	35	WHT		
802	36	BLK		
703	37	WHT		
803	38	BLK		
704	39	WHT		
804	40	BLK		
705	41	WHT		
805	42	BLK		
706	43	WHT		
806	44	BLK		
707	45	WHT		
807	46	BLK		
708	47	WHT		
808	A29-48	BLK		
709	A30-31	WHT		
809	A30-32	BLK		
710	A28-14	WHT		
810	13	BLK		
711	16	WHT		
811	15	BLK		
712	20	WHT		
P1/P2-812	19	BLK		
P3/P4-101	22	WHT		TWIST
P3/P4-201	A28-21	BLK	26	

FROM	TO	COLOR	AWG	REMARKS
P3/P4-102	A28-26	WHT	26	TWIST
202	25	BLK		
103	28	WHT		
203	27	BLK		
104	32	WHT		
204	31	BLK		
105	34	WHT		
205	33	BLK		
106	38	WHT		
206	37	BLK		
107	40	WHT		
P3/P4-207	39	BLK		
P5-102	41	WHT		
P5-202	A28-42	BLK		
P3/P4-109	A30-33	WHT		
P3/P4-209	A30-34	BLK		
P5-103	A28-43	WHT		
P5-203	A28-44	BLK		
P3/P4-301	A30-35	WHT		
401	36	BLK		
302	37	WHT		
402	38	BLK		
303	39	WHT		
403	40	BLK		
304	41	WHT		
404	42	BLK		
305	43	WHT		
P3/P4-405	A30-44	BLK		
P5-101	A28-45	WHT		
P5-201	A28-46	BLK		
P5-106	A27-45	WHT		
P5-206	A27-46	BLK	26	TWIST

APPLICABLE DOCUMENT
LM 144-100210

	772926
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON

BASIC DIMENSION	DECIMAL PLACES .XX	.XXX
UNDER 12	± .02	± .005
12 TO 24	± .03	± .010
OVER 24	± .06	± .015
ANGLES ± 0° 30'		

MATERIAL:
FINISH:

DRAWN	RENE GONZALEZ	DATE 7-3-70
CHECKED		9/17/70
ENGR		9/17/70
PROJ ENGR		9/17/70
APPROVED		9/17/70
APPROVED		

Systems Engineering Laboratories
Fort Lauderdale, Florida

CABLE ASSEMBLY I/O & BTC SYNC DATA MODEM INTFC

SIZE	CODE IDENT NO.	DWG NO.
D	20886	144-100210

SCALE | SHEET 1 OF 1

ERN / 74-1 DATE 8-4-71 REV -

LIST of MATERIAL			Systems Engineering Laboratories	20886	LM 144-100293	-
PREP	E. PEREZ-CUBAS	DATE 6-9-71	Fort Lauderdale, Florida 33310	CODE IDENT	SHEET 1 OF 2 SHEETS	REV
CHK				ITEM NOMENCLATURE: CABLE ASSEMBLY STANDARD AUTO-DIAL		
ENGR	[signature]	8/3/71				
APPD			USED ON: 554102 (704002)			

LTR	REVISION DESCRIPTION	DATE	APPD	LTR	REVISION DESCRIPTION	DATE	APPD

RECORD OF REVISION STATUS OF EACH SHEET

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42

LM 144-100293

S.E.L. Form 365-1A

LIST of MATERIAL	Systems Engineering Laboratories	20886	LM 144-100293	
ITEM NOMENCLATURE: CABLE ASS'Y STANDARD AUTO-DIAL		CODE IDENT	SHEET 2 OF 2 SHEETS	REV

ITEM NO.	QTY REQ'D PER DASH NO. 001	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	REFERENCE DESIGNATION	REMARKS
1	22	259-900010-030	24-26 AMP SOCKETS		
2	2	259-800002-023	CORNER GUIDE PIN		
3	1	259-100410-002	FIXED JACK SCREW FEMALE		
4	2	259-800002-024	CORNER GUIDE SOCKET		
5	1	110-100410-004	50 PIN MOUNTING PLATE		
6	1	259-500001-002	CONN. 50PIN FEMALE		
7	1	259-800001-001	FIXED JACK SCREW MALE		
8	AR	258-000940-001	WIRE #26 AWG TWISTED/PR		
9	1	160-100223-001	BIPOLAR DRIVER		
10	1	160-100306-001	BIPOLAR RECEIVER		
11	4	223-300008-006	MOUSE TAIL		

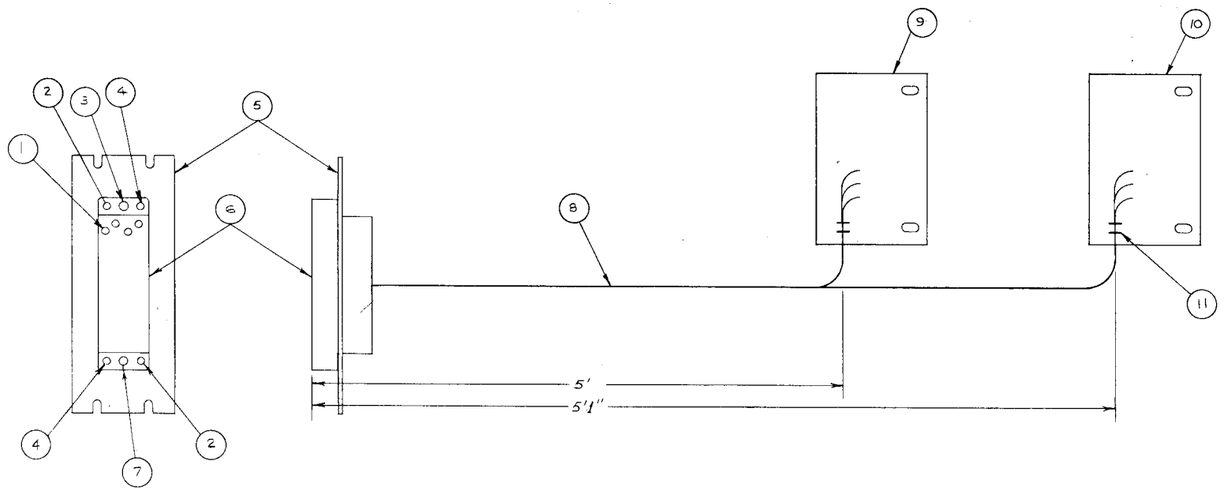
LM 144-100293

S.E.L. Form 365-2A

ERN 174-1
DATE 8-4-71 REV- 1

REVISIONS

ZONE	LTR	DESCRIPTION	DATE	APPROVED



FROM	TO	COLOR	AWG	REMARKS
P7-101	24B-E3	WHITE	26	TWISTED PAIR
-201	-E4	BLACK		
-102	-E5	WHITE		
-202	-E6	BLACK		
-103	-E7	WHITE		
-203	-E8	BLACK		
-104	-E9	WHITE		
-204	24B-E10	BLACK		
-105	25B-E12	WHITE		
-205	-E11	BLACK		
-106	-E1	WHITE		
-206	-E2	BLACK		
-107	-E4	WHITE		
-207	-E3	BLACK		
-108	-E6	WHITE		
-208	-E5	BLACK		
-109	-E8	WHITE		
-209	-E7	BLACK		
-110	-E10	WHITE		
-210	-E9	BLACK		
-111	-E2	WHITE		TWISTED PAIR
P7-211	25B-E1	BLACK	26	

APPLICABLE DOCUMENT
LM 144-100293

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ON

BASIC DIMENSION	DECIMAL PLACES .XX	.XXX
UNDER 12	± .02	± .005
12 TO 24	± .03	± .010
OVER 24	± .06	± .015
ANGLES ± 0° 30'		

MATERIAL:
FINISH:

554102	704004
PROJ.	SPCL SYS.
APPLICATION	

DRAWN E. PEREZ-CUBAS 5-25-71
CHECKED
ENGR 8/3/71
PROJ ENGR 8/3/71
APPROVED
APPROVED

Systems Engineering Laboratories
Fort Lauderdale, Florida

CABLE ASSEMBLY
STANDARD AUTO-DIAL

SIZE	CODE IDENT NO.	DWG NO.
D	20886	144-100293

SCALE | REV LTR | SHEET 1 OF 1

ERN 174-1 DATE 8-4-71 REV –

LIST of MATERIAL			Systems Engineering Laboratories	20886	LM 144-100294	–
PREP	E. PEREZ-CUBAS	DATE 6-9-71	Fort Lauderdale, Florida 33310	CODE IDENT	SHEET 1 OF 2 SHEETS	REV
CHK				ITEM NOMENCLATURE: CABLE ASSEMBLY STANDARD MODEM		
ENGR	C. McClinton	8/3/71				
APPD			USED ON: 554102 (704002)			

LTR	REVISION DESCRIPTION	DATE	APPD	LTR	REVISION DESCRIPTION	DATE	APPD

RECORD OF REVISION STATUS OF EACH SHEET

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42

LM 144-100294

S.E.L. Form 365-1A

LIST of MATERIAL	Systems Engineering Laboratories	20886	LM 144-100294	–
ITEM NOMENCLATURE: CABLE ASSY STANDARD MODEM		CODE IDENT	SHEET 2 OF 2 SHEETS	REV

ITEM NO.	QTY REQ'D PER DASH NO. 001	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	REFERENCE DESIGNATION	REMARKS
1	22	259-900010-030	24-26 AMP SOCKETS		
2	2	259-800002-023	CORNER GUIDE PIN		
3	1	259-100410-002	FIXED JACK SCREW FEMALE		
4	1	110-100410-004	50 PIN MOUNTING PLATE		
5	1	259-500001-002	CONN, 50 PIN FEMALE		
6	2	259-800002-024	CORNER GUIDE SOCKET		
7	1	259-800001-001	FIXED JACK SCREW MALE		
8	AR	258-000940-001	WIRE #26 AWG TWISTED/PR		
9	1	160-100223-001	BIPOLAR DRIVER		
10	1	160-100306-001	BIPOLAR RECEIVER		
11	4	223-300008-006	MOUSE TAIL		

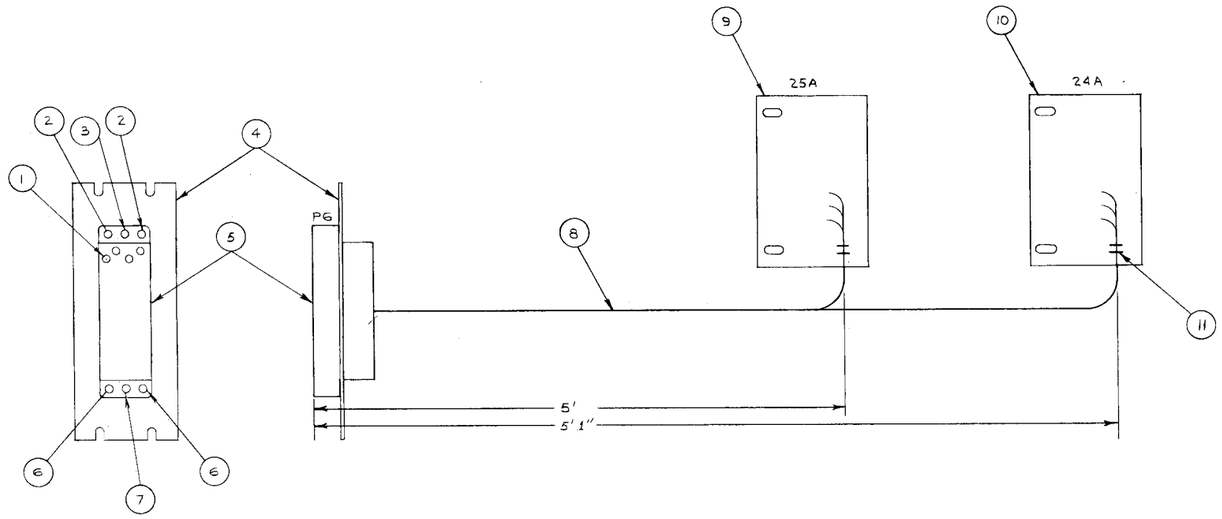
LM 144-100294

S.E.L. Form 365-2A

ERN 174-1
DATE 8-4-71 REV - 1

REVISIONS

ZONE	LTR	DESCRIPTION	DATE	APPROVED



FROM	TO	COLOR	AWG	REMARKS
P6-101	25A-E2	WHITE	26	TWIST
" -201	" -E1	BLACK	"	
" -102	" -E4	WHITE	"	
" -202	" -E3	BLACK	"	
" -103	" -E6	WHITE	"	
" -203	25A -E5	BLACK	"	
" -104	24A -E11	WHITE	"	
" -204	" -E12	BLACK	"	
" -105	" -E13	WHITE	"	
" -205	" -E14	BLACK	"	
" -106	" -E15	WHITE	"	
" -206	" -E16	BLACK	"	
" -107	" -E1	WHITE	"	
" -207	" -E2	BLACK	"	
" -108	" -E3	WHITE	"	
" -208	" -E4	BLACK	"	
" -109	" -E5	WHITE	"	
" -209	" -E6	BLACK	"	
" -110	" -E7	WHITE	"	
" -210	" -E8	BLACK	"	
" -111	" -E9	WHITE	"	TWIST
P6-211	24A-E10	BLACK	26	

APPLICABLE DOCUMENT
LM 144-100294

554102	704004
PROJ	SPCL SYS.
APPLICATION	

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ON

BASIC DIMENSION	DECIMAL PLACES .XX	.XXX
UNDER 12	± .02	± .005
12 TO 24	± .03	± .010
OVER 24	± .06	± .015

ANGLES ± 0° 30'

MATERIAL:
FINISH:

		DATE
DRAWN	E. PEREZ-CUBAS	5-26-71
CHECKED		
ENGR		8/3/71
PROJ ENGR		8/3/71
APPROVED		
APPROVED		

Systems Engineering Laboratories
Fort Lauderdale, Florida

CABLE ASSEMBLY
STANDARD MODEM

SIZE	CODE IDENT NO.	DWG NO.
D	20886	144-100294

SCALE | REV LTR | SHEET 1 OF 1

ERN 174-1 DATE 8-4-71 REV –

LIST of MATERIAL			Systems Engineering Laboratories Fort Lauderdale, Florida 33310	20886	LM 144-100295	–
PREP	E. PEREZ-CUBAS	DATE 6-9-71		CODE IDENT	SHEET 1 OF 2 SHEETS	REV
CHK				ITEM NOMENCLATURE: CABLE ASSEMBLY OPTIONAL MODEM		
ENGR	[signature]	8/5/71				
APPD			USED ON: 554102 (704004)			

LTR	REVISION DESCRIPTION	DATE	APPD	LTR	REVISION DESCRIPTION	DATE	APPD

RECORD OF REVISION STATUS OF EACH SHEET

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42

LM 144-100295

S.E.L. Form 365-1A

LIST of MATERIAL	Systems Engineering Laboratories	20886	LM 144-100295	–
ITEM NOMENCLATURE: CABLE ASSY OPTIONAL MODEM		CODE IDENT	SHEET 2 OF 2 SHEETS	REV

ITEM NO.	QTY REQ'D PER DASH NO. 001	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	REFERENCE DESIGNATION	REMARKS
1	1	110-100410-004	50PIN MOUNTING PLATE		
2	1		FIXED JACK SCREW MALE		
3	1		FIXED JACK SCREW FEMALE		
4	4		SCREW		
5	48"		COAX		RG 195/U
6	AR	258-000940-001	WIRE #26AWG BLK. STRANDED		
7	1	YOC120	FERRULES BURNDY		
8	1	YOC109	FERRULES BURNDY		
9	1	160-083278-003	CABLE DRIVER		
10	1	160-100069-002	CABLE TERMINATOR		
11	4	223-300008-002	MOUSE TAIL		
			RELATED ITEM		
12	1		12 POSITION BURNDY		MD12 MXR-8T
			COAX CONN. KIT INCLUDES		
			ITEMS 2 THRU 4		

LM 144-100295

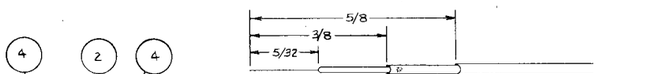
S.E.L. Form 365-2A

ERN 174-1
DATE 8-4-71 REV – 1

REVISIONS

ZONE	LTR	DESCRIPTION	DATE	APPROVED

FIGURE 1.



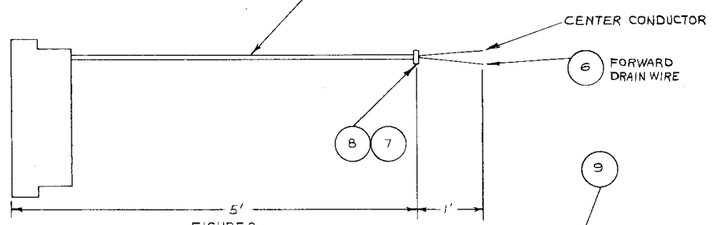


FIGURE 2

FIGURE 3

	FROM PG	TO	WIRE TYPE
C	CENTER CONDUCTOR	24A3	RG195/U
	OUTER CONDUCTOR	24A4	
D	CENTER CONDUCTOR	25A20	
	OUTER CONDUCTOR	25A19	
E	CENTER CONDUCTOR	25A14	
	OUTER CONDUCTOR	25A13	
F	CENTER CONDUCTOR	24A1	
	OUTER CONDUCTOR	24A9	
J	CENTER CONDUCTOR	24A11	
	OUTER CONDUCTOR	24A12	
K	CENTER CONDUCTOR	24A15	
	OUTER CONDUCTOR	24A16	
L	CENTER CONDUCTOR	24A13	
	OUTER CONDUCTOR	24A14	
M	CENTER CONDUCTOR	24A5	RG195/U
	OUTER CONDUCTOR	25A2	

APPLICABLE DOCUMENT
LM 144-100295

NOTES: 1) CUT 8 WIRES 6 FEET LONG.
2) STRIP & CRIMP BURNDY COAX CONNECTORS AS PER BURNDY INSTRUCTIONS WITH BURNDY CRIMPER M8ND/N22RVMT REFERENCE FIGURE 1 FOR STRIP LENGTH
3) INSERT CONTACT INTO BLOCK
4) STRIP COAX & INSTALL FERRULES WITH FORWARD DRAIN WIRE EXACTLY 5 FEET FROM CONNECTOR. USE BURNDY CRIMPER MR8PVIS. SEE FIGURE 2.
5) FOR FURTHER INFORMATION REFER TO BURNDY ASSY PROCEDURE SD51447.

554102	704004
PROJ.	SPCL SYS
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON

BASIC DIMENSION	DECIMAL PLACES .XX	.XXX
UNDER 12	± .02	± .005
12 TO 24	± .03	± .010
OVER 24	± .06	± .015
ANGLES ± 0° 30'		

MATERIAL:
FINISH:

		DATE
DRAWN	E.PEREZ-CUBAS	5-28-71
CHECKED		
ENGR		8/3/71
PROJ ENGR		8/4/71
APPROVED		
APPROVED		

Systems Engineering Laboratories
Fort Lauderdale, Florida

CABLE ASSEMBLY
OPTIONAL MODEM

SIZE	CODE IDENT NO.	DWG NO.
D	20886	144-100295

SCALE | REV LTR | SHEET 1 OF 1

160-083278 SCHEMATIC AND ASSEMBLY
CABLE DRIVER/TERMINATOR

DESCRIPTION

This circuit card contains 17 discrete component inverting stages designed to drive and terminate twisted pair cables and reduce crosstalk between cables. The cable driver and terminator is used in conjunction with the positive (0-+3.6v) micrologic circuits and is capable of driving 100 feed twisted pair cable.

SPECIFICATION

Logic levels:

0 volts = logic ZERO
+3.3 volts = logic ONE

Power requirements:

0 volts - pins 1 and 79
+5 volts - pins 2 and 80

LIST of MATERIAL			Systems Engineering Laboratories	ERN	DATE	REV
PREP	J.MAGINNESS	5-17-68	Fort Lauderdale, Florida 33310	20886	LM160-083278	D
CHK	RKM	5-24-68		CODE IDENT	SHEET 1 OF 2 SHEETS	REV
ENGR	MR	7-16-68		ITEM NOMENCLATURE: SCHEMATIC & ASSEMBLY CABLE DRIVER/TERMINATOR		
APPD	L KLINGLER	7-16-68	USED ON: FIXED HEAD DISC			

LTR	REVISION DESCRIPTION	DATE	APPD
D	REF 71-168, REVISED LM 160-083278 NR6	3-9-71	RDW

LTR	REVISION DESCRIPTION	DATE	APPD

RECORD OF REVISION STATUS OF EACH SHEET

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42
D	D																																							

LM160-083278

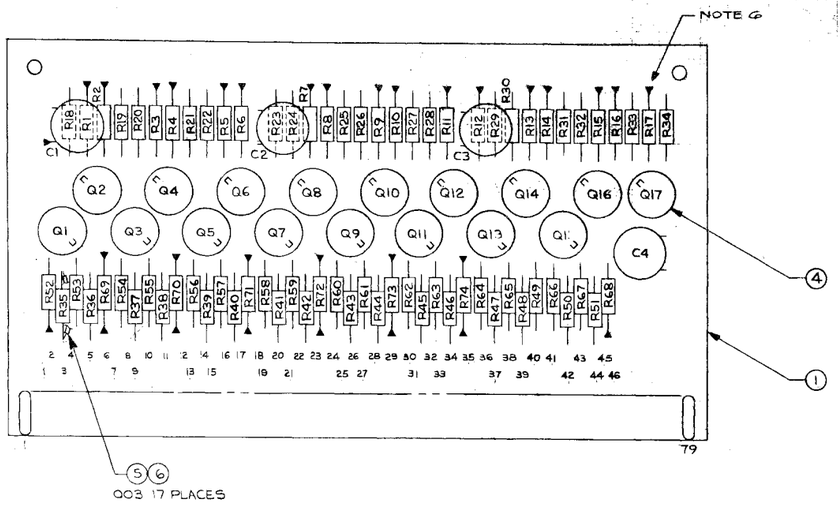
S.E.L. Form 365-1A

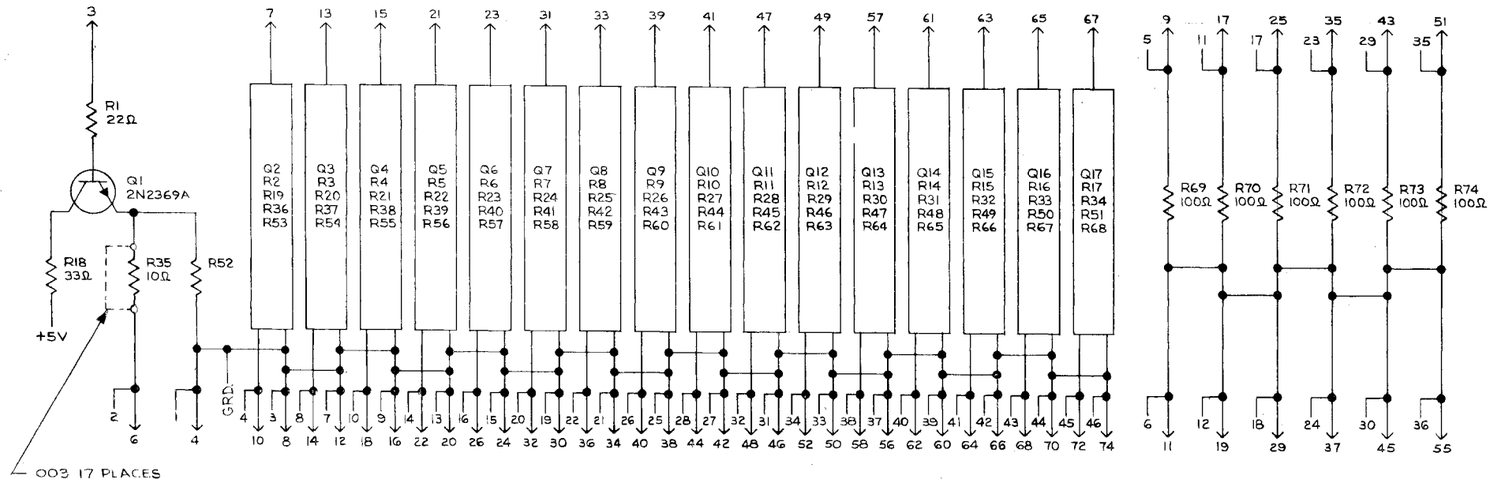
LIST of MATERIAL	Systems Engineering Laboratories	20886	LM160-083278	D
ITEM NOMENCLATURE: SCHEMEASSY CABLE DRVR/TERMINATOR		CODE IDENT	SHEET 2 OF SHEETS	REV

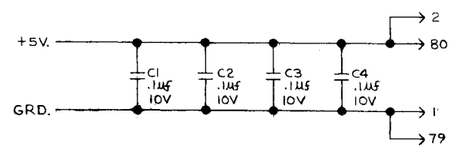
ITEM NO.	QTY REQ'D PER DASH NO. 002	001	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	REFERENCE DESIGNATION	REMARKS
1	1	1	164-003278-001	PRINTED WIRING BOARD		FOR REF SEE 149-053107-000
2	REF	REF	168-003278-001	DRILLING DRAWING		
3	REF	REF	172-016322-001	DIMENSIONAL DRAWING		
4	17	17	110-010369-001	UNIPAD		
5						
6						
7						
8						
9	4	4	254-100700-002	CAP. 1UF +80-20% 10VCER	C1-C4	
10	17	17	253-100010-033	RES 22Ω ± 5% 1/4W CMPSN	R1-R17	
11	17	17	253-100010-037	RES 33Ω ± 5% 1/4W CMPSN	R18-R34	
12	17	17	253-100010-025	RES 10Ω ± 5% 1/4W CMPSN	R35-R51	
13	6	23	253-100010-049	RES 100Ω ± 5% 1/4W CMPSN	R52-R74	
14	17	17	250-122369-002	TRANSISTOR	Q1-Q17	

LM160-083278

S.E.L. Form 365-2A







NOTES:
1. ALL ITEMS AS SPECIFIED IN LIST OF MATERIAL OR APPROVED EQUIVALENT.
2. UNLESS OTHERWISE SPECIFIED RESISTORS ARE ±5%, 1/4W.

~~4. PRINTED WIRING BOARD SHALL MEET THE REQUIREMENTS OF 160-001050-001.~~
~~5. TEST PER SEL 950924-1.~~
6. INDICATES TOP SIDE SOLDER (QTY 32) NOT REQUIRED WHEN PLATED THRU.

SIZE	160-083278	REV.
D		E

REV.	DESCRIPTION	DATE	APPD
A	68-1651; RELEASED ~~10-9-68~~ RKM	6/9/68	
B	68-829; 69-058; ADDED CABLE DESIGNATIONS E-002 FLP 5-2-69 RKM	5/2/69	
C	69-1113; UPDATED TO LATEST NO. SYSTEM; ADDED NOTES 4, 5, 6 & TOP SIDE SOLDER SYM; DELETED ITEM #3 RSK 2-19-70	2/20/70	
D	REF 71-168, REVISED LM 160-083278 NR	3/3/71	
E	71-299 LM 5-19-71 RKM	5-21-71	

APPLICABLE DOCUMENTS:
LM 160-083278

ITEM	DWG. OR PART NO.	DESCRIPTION

THIS DOCUMENT AND THE INFORMATION CONTAINED HEREIN ARE THE PROPERTY OF SYSTEMS ENGINEERING LABORATORIES. IN CONSIDERATION OF THE RECEIPT OF THIS DOCUMENT, THE RECIPIENT AGREES NOT TO REPRODUCE, COPY, USE OR TRANSMIT THIS DOCUMENT IN WHOLE OR IN PART, FOR ANY PURPOSE, EXCEPT WITH APPROPRIATE APPROVAL OF SYSTEMS ENGINEERING LABORATORIES.

Systems Engineering Laboratories
6901 West Sunrise Blvd., Fort Lauderdale, Florida 33310

DR J. MAGINNESS	5-17-68	SCHEMATIC & ASSEMBLY CABLE DRIVER/TERMINATOR
CHK RKM	5-24-68	
ENGR	7-16-68	
PROJ	7-15-68	
APPD	7/16/68	
NEXT ASSY		

CODE IDENT NO.	SIZE		REV
20886	D	160-083278	E

SHEET 1 OF 1

160-083289 SCHEMATIC AND ASSEMBLY
OSCILLATOR (Sheet 1 of 2)

DESCRIPTION:

This circuit card contains one quad 2-input NAND/NOR gate circuit, one 50mHz dual JK flip-flop circuit with separate clock inputs, and a 2.6667 mHz crystal controlled oscillator.

The NAND/NOR gate circuit consists of a multiple emitter input AND gate followed by an inverting amplifier with a cascode pull-up network. Each gate functions as a NAND element in positive logic or as a NOR element in negative logic.

The dual JK flip-flop circuit has separate clock input terminals for each flip-flop and separate dc set input terminals.

Information is applied to the J and/or K terminals while the clock is low. This new information is ANDed with the present state of the flip-flop and stored in the depletion region of a diode when the clock goes high. When the clock returns low, the stored information is ANDed with the inverted clock, causing the cross-coupled buffered NAND gates to be set accordingly.

SPECIFICATIONS:

Speed	Designed to operate at 20 mHz, propagation delay time typically 18 nsec.			
Logic Levels	Logic 0 is typically 0.26 volts; logic 1 is typically 3.3 volts at 25° C.			
Ratings	Voltage			
	Supply voltage (D° C°)			7.0v Max.
	Supply voltage (surge, 1 sec.)			12.0v Max.
	Supply voltage (operating)	4.5v Min.	5.0v Typ.	6.0v Max.
	Input voltage			5.5v Max.
	Output voltage			5.5 v Max.

160-083289 SCHEMATIC AND ASSEMBLY
OSCILLATOR (Sheet 2 of 2)

Temperature

Operating	0 Min.		+ 75° C Max.
Shorage	-65 Min.		+200° C Max.
Power dissipation (50% duty cycle, Vcc = +5v)		50 Typ.	MW Max.

LIST of MATERIAL	Systems Engineering Laboratories	ERN 20886	DATE LM160-083289	REV F
PREP [illegible] DATE 3-19-68	Fort Lauderdale, Florida 33310	CODE IDENT	SHEET 1 OF 4 SHEETS	REV
CHK [illegible] 3-20-68		ITEM NOMENCLATURE: SCHEMATIC & ASSEMBLY OSCILLATOR		
ENGR R. EALEY 4-16-68				
APPD C. KLINGER 4-16-68	USED ON:			

LTR	REVISION DESCRIPTION	DATE	APPD	LTR	REVISION DESCRIPTION	DATE	APPD
F	71-162: HRC 3-4-71 RKM	3-5-71	[illegible]				

RECORD OF REVISION STATUS OF EACH SHEET

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42
F	-	-	F																																					

LM 160-083289

S.E.L. Form 365-1A

LIST of MATERIAL	Systems Engineering Laboratories	20886	LM 160-083289	F
ITEM NOMENCLATURE: SCHEMATIC & ASSEMBLY OSCILLATOR		CODE IDENT	SHEET 2 OF 4 SHEETS	REV

ITEM NO.	QTY REQ'D PER DASH NO. 005	004	003	002	001	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	REFERENCE DESIGNATION	REMARKS
1	1	1	1	1	1	164-003289-001	PRINTED WIRING BOARD		FOR REV SEE 149-053107-000
2	REF	REF	REF	REF	REF	168-083289-001	DRILLING DWG		
3	REF	REF	REF	REF	REF	172-016322-001	DIMENSIONAL DWG		
4	4	4	4	4	4	110-010369-001	UNIPAD		
5	1	1	1	1	1	223-300008-006	STRAP, RUBBER		
6									
7									
8									
9									
10									
11									
12									
13									
14									
15									
16									
17	1	1	1	—	1	254-100980-015	CAP 15-60 PF 500V CER	C1	
18	1	1	1	—	1	254-100500-019	CAP 47PF ±10% 1000V CER	C2	
19	1	1	1	1	1	254-100500-012	CAP 22 PF ±10% 1000V CER	C3	
20	2	2	2	2	2	254-100500-027	CAP 100 PF ±10% 1000V CER	C4,6	
21	1	1	1	1	1	254-100550-001	CAP.005UF+60-40% 150V CER	C5	

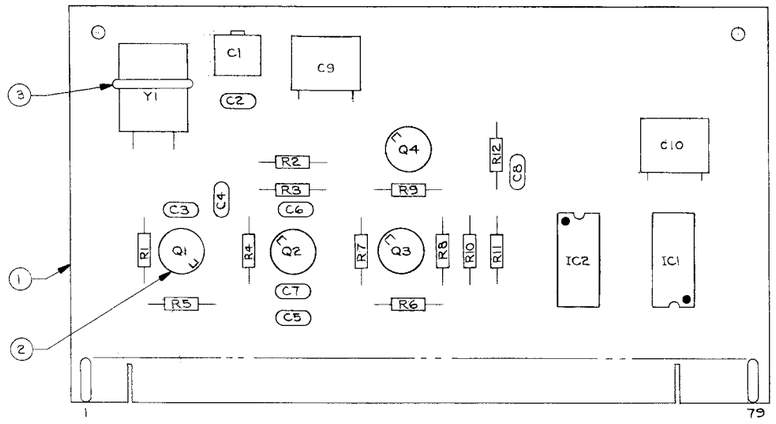
LM 160-083289

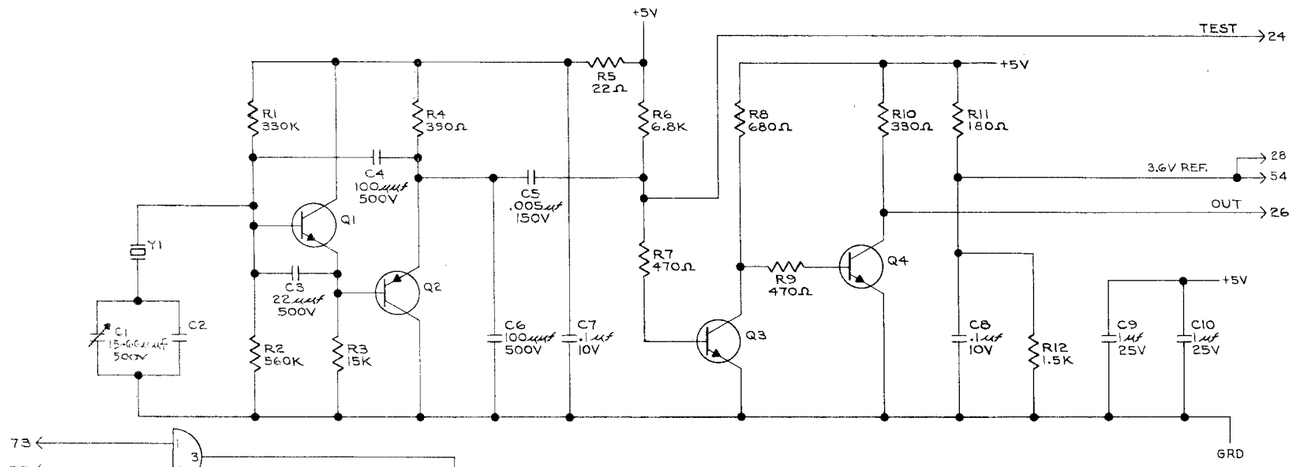
S.E.L. Form 365-2A

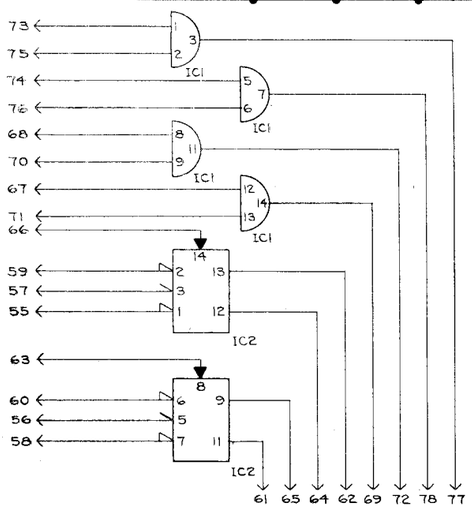
NOTES:
1. ALL ITEMS AS SPECIFIED IN LIST OF MATERIAL OR APPROVED EQUIVALENT
2. UNLESS OTHERWISE SPECIFIED RESISTORS ARE ±5%, 1/4W

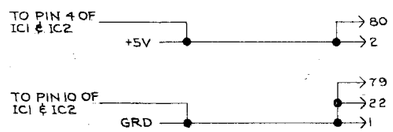
SIZE		REV.
D	160-083289	F

REV.	DESCRIPTION	DATE	APPD
A	68-440; IC1 WAS SG220; Y1 WAS 908, SAVOY. RKM 3-1-68	3/1/68	
B	68-465; RELEASED RKM 8-9-68	8/9/68	
C	69-1129; ADDED 002 B.E. 2-3-70 RKM	2/3/70	
D	70-424, ARH 5-20-70 RKM	5/26/70	
E	71-038; H.R.C. 2-5-71 RKM	2-8-71	
F	71-162; H.R.C. 3-4-71 RKM	3-5-71	









APPLICABLE DOCUMENTS:
LM 160-083289

ITEM	DWG. OR PART NO.	DESCRIPTION

Systems Engineering Laboratories
6901 West Sunrise Blvd., Fort Lauderdale, Florida 33310

DR	H.R.C. Brink	3-19-68
CHK	RKM	3-20-68
ENGR	R. Baldwin	4-16-68
PROJ	H.R.C. Brink	4-16-68
APPD	R.K. Mueller	4-16-68
NEXT ASSY		

SCHEMATIC & ASSEMBLY
OSCILLATOR

CODE IDENT NO.	SIZE		REV.
20886	D	160-083289	F

SHEET 1

D 160-083289 F

LIST of MATERIAL	Systems Engineering Laboratories	20886	LM 160-083289	F
ITEM NOMENCLATURE: SCHEMATIC & ASSEMBLY OSCILLATOR		CODE IDENT	SHEET 3 OF 4 SHEETS	REV

ITEM NO.	QTY REQ'D PER DASH NO. 005	004	003	002	001	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	REFERENCE DESIGNATION	REMARKS
22	4	2	2	2	2	254-100700-002	CAP .1UF+80-20% 10V CER	C7,8	
23	2	2	2	2	2	254-100870-013	CAP 1UF±20% 25V CER	C9,10	
24	1	1	1	1	1	252-115022-201	INTEGRATED CIRCUIT	IC1	
25	1	1	1	1	1	252-115412-301	INTEGRATED CIRCUIT	IC2	
26	1	1	1	1	1	250-123947-001	TRANSISTOR	Q1	
27	1	1	1	1	1	250-123251-001	TRANSISTOR	Q2	
28	2	2	2	2	2	250-122369-002	TRANSISTOR	Q3,4	
29	1	1	1	1	1	253-100010-133	RES 330K±5% 1/4W CMPSN	R1	
30	1	1	1	1	1	253-100010-139	RES 560K±5% 1/4W CMPSN	R2	
31	1	1	1	1	1	253-100010-101	RES 15K±5% 1/4W CMPSN	R3	
32	1	1	1	1	1	253-100010-063	RES 390Ω±5% 1/4W CMPSN	R4	
33	1	1	1	1	1	253-100010-033	RES 22Ω±5% 1/4W CMPSN	R5	
34	1	1	1	1	1	253-100010-021	RES 6.8K±5% 1/4W CMPSN	R6	
35	2	2	2	2	2	253-100010-065	RES 470Ω±5% 1/4W CMPSN	R7,9	
36	1	1	1	1	1	253-100010-069	RES 680Ω±5% 1/4W CMPSN	R8	
37	1	1	1	1	1	253-100010-061	RES 330Ω±5% 1/4W CMPSN	R10	
38	1	1	1	1	1	253-100010-055	RES 180Ω±5% 1/4W CMPSN	R11	
39	1	1	1	1	1	253-100010-077	RES 1.5K±5% 1/4W CMPSN	R12	
40	—	—	—	1	1	260-100001-001	CRYSTAL 2.6667 MHZ	Y1	
41	—	—	—	1	—	254-100500-027	CAP 100PF±10% 1000V CER	C2	
42	—	—	1	—	—	260-100001-004	CRYSTAL 10 MHZ	Y1	

LM 160-083289

S.E.L. Form 365-2A

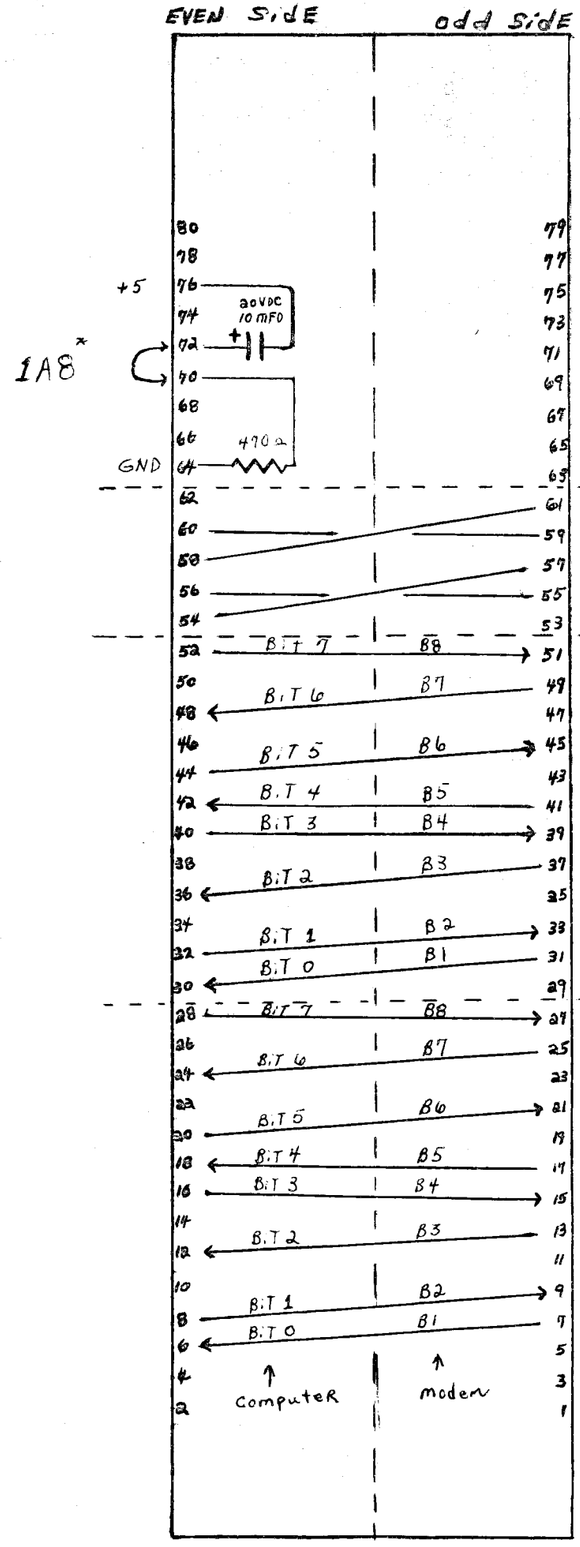
LIST of MATERIAL	Systems Engineering Laboratories	20886	LM 160-083289	F
ITEM NOMENCLATURE: SCHEMATIC & ASSEMBLY OSCILLATOR		CODE IDENT	SHEET 4 OF 4 SHEETS	REV

ITEM NO.	QTY REQ'D PER DASH NO. 005	004	003	002	001	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	REFERENCE DESIGNATION	REMARKS
43	—	1	—	—	—	260-100001-005	CRYSTAL 5.0 MHZ	Y1	
44	1	—	—	—	—	260-100001-007	CRYSTAL 4.9152	Y1	

LM 160-083289

S.E.L. Form 365-2A

CARD



ALL JUMPERS AND COMPONENTS LOCATED ON odd SIDE.

* REFER TO LOCATION ON LOGIC DIAGRAM AND TIMING PRINTS

FOR THE PROPER SYNC CODE, THE JUMPERS ARE TIED TO A HIGH FROM THE RECEIVE REGISTER

JUMPER CARD
83251

160-100026 GENERAL REGISTER EVEN

DESCRIPTION

This module contains a 16-bit register. Each stage has a steering input and a dc set input. The common clock and common reset circuits are split in half and connected to eight stages each.

SPECIFICATIONS

Input Power Requirements:

Voltage Tolerance:	±10%
Voltage, Nominal:	+5V
Current, Maximum:	435mA
Current, Typical:	248mA

888600 pjr

ERN 011-2
DATE 11/14/69 REV B

LIST of MATERIAL			Systems Engineering Laboratories	20886	LM 160-100026	E
PREP	RKM	DATE 9-18-68	Fort Lauderdale, Florida 33310	CODE IDENT	SHEET 1 OF 3 SHEETS	REV
CHK	GJW	9-24-68		ITEM NOMENCLATURE: GENERAL REGISTER EVEN		
ENGR	W RF	9-25-68				
APPD		11/12	USED ON: SYS 86			

LTR	REVISION DESCRIPTION	DATE	APPD
A	ITEM 12 WAS 1K; ITEM 13 WAS 120Ω. RKM 10-14-68 UC WRF	10/14/68	WRF
B	UPDATED TO LATEST STANDARDS BJC 11/6/69 RKM	11-11-69	WRF
C	ECO 70-511 N.L.A 6-1-70 RKM	6/2/70	WRF
D	70-1009 M.P. 9-17-70 RKM	9-21-70	JB
E	71-001 WKS 3-10-71 RKM	3-10-71	RKM

RECORD OF REVISION STATUS OF EACH SHEET

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42
B	B																																							
C	C	C																																						
D	D	C																																						
E	E	E																																						

LM 160-100026

S.E.L. Form 365-1

LIST of MATERIAL	Systems Engineering Laboratories	20886	LM 160-100026	E
ITEM NOMENCLATURE: GENERAL REGISTER EVEN		CODE IDENT	SHEET 2 OF SHEETS	REV

ITEM NO.	QTY REQD PER DASH NO. 003	002	001	PART OR IDENTIFYING NO.	DRAWING OR SPECIFICATION NO.	NOMENCLATURE OR DESCRIPTION	REF DES	REMARKS
1	1	1	1	164-100026-001		PRINTED CIRCUIT		FOR REV SEE 149-100001-000
2	REF	REF	REF	172-016322-001		DIMENSIONAL DWG		
3	REF	REF	REF	168-100026-001		DRILLING DWG		
4								
5	2	1	2	110-010369-001		UNIPAD		
6								
7								
8	X	2	2	254-100700-002		CAP. .1μF +80-20% 10V CER	C1 C2	
9	4	X	4	252-115022-301		INTEGRATED CIRCUIT	IC1 IC2	
							IC7 IC8	
10	8	X	8	252-115413-201		INTEGRATED CIRCUIT	IC3-IC6	
							IC9-IC12	
11	2	X	2	250-122369-002		TRANSISTOR	Q1 Q2	
12	2	X	2	253-100010-071		RES. 820Ω ±5% 1/4W CMPSN	R1 R5	
13	2	X	2	253-100010-053		RES. 150Ω ±5% 1/4W CMPSN	R2 R6	
14	1	1	1	253-100010-077		RES. 1.5K ±5% 1/4W CMPSN	R3	
15	1	1	1	253-100010-055		RES. 180Ω ±5% 1/4W CMPSN	R4	
16	X	2	X	252-115022-301		INTEGRATED CIRCUIT	IC1 IC2	
17	X	4	X	252-115413-201		INTEGRATED CIRCUIT	IC3-IC6	
18	X	1	X	250-122369-002		TRANSISTOR	Q1	

LM 160-100026

S.E.L. Form 365-2

LIST of MATERIAL	Systems Engineering Laboratories	20886	LM 160-100026	E
ITEM NOMENCLATURE: GENERAL REGISTER EVEN		CODE IDENT	SHEET 3 OF SHEETS	REV

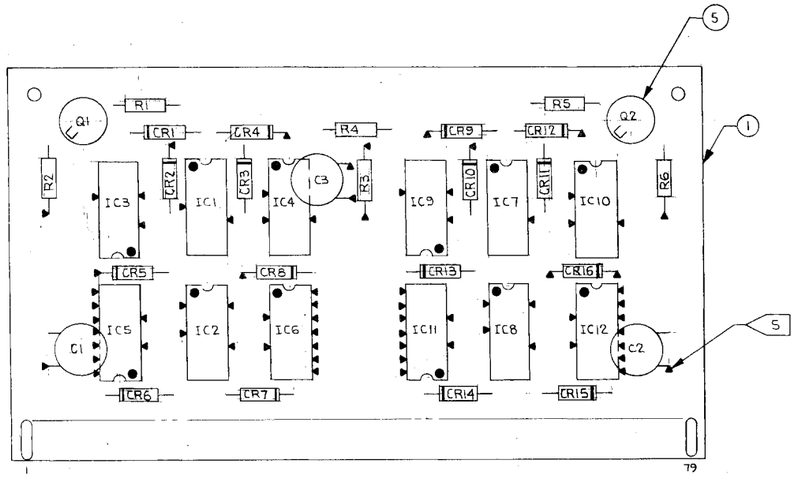
ITEM NO.	QTY REQ'D PER DASH NO. 003	002	001	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	REFERENCE DESIGNATION	REMARKS
19	X	1	X	253-100010-071	RES 820Ω ± 5% 1/4W CMPSN	R1	
20	X	1	X	253-100010-053	RES 150Ω ± 5% 1/4W CMPSN	R2	
21	3	X	X	254-100700-002	CAP .1UF +80-20% 10V CER	C1,2,3	
22	16	X	X	251-100040-001	DIODE	CR1-16	

LM 160-100026

S.E.L. Form 365-2A

NOTES:
1. ALL ITEMS AS SPECIFIED IN LIST OF MATERIAL OR OR APPROVED EQUIVALENT.
2. PRINTED WIRING BOARD SHALL MEET THE REQUIREMENTS OF 190-001050-001
3.
4. TEST PER SEL 95092A-1
5. INDICATES TOP SOLDER (▶ QTY 65 FOR C01, 35 FOR 002, 76 FOR 003) NOT REQD WHEN PLATED THRU

SIZE	160-100026		REV.
REV.	DESCRIPTION	DATE	APPD
A	R1 & R5 WERE 1K; R2 & R6 WERE 120Ω RKM 10-14-68	10/14/68	
B	UPDATED TO LATEST STANDARDS BJC 11/6/69 RKM	11/11/69	
C	ECO 70-511 N.L.A 6-1-70 RKM	6/2/70	
D	70-1009 M.P. 9-17-70 RKM	9/21/70	
E	71-001 WKS 3-10-71 REM	3-10-71	



REVISION LEVEL OF SHEETS							
SH 1	SH 2	SH 3	SH 4	SH 5	SH 6	SH 7	
E	E	E					

APPLICABLE DOCUMENTS:
LIST OF MATERIAL-LM 160-100026

ITEM	DWG. OR PART NO.	DESCRIPTION

Systems Engineering Laboratories
6901 West Sunrise Blvd., Fort Lauderdale, Florida 33310

DR	RKM	9-18-68
CHK	GFW	9-24-69
ENGR	R Fox	11-12-69
PROJ		11-12-69
APPD		11-12-69

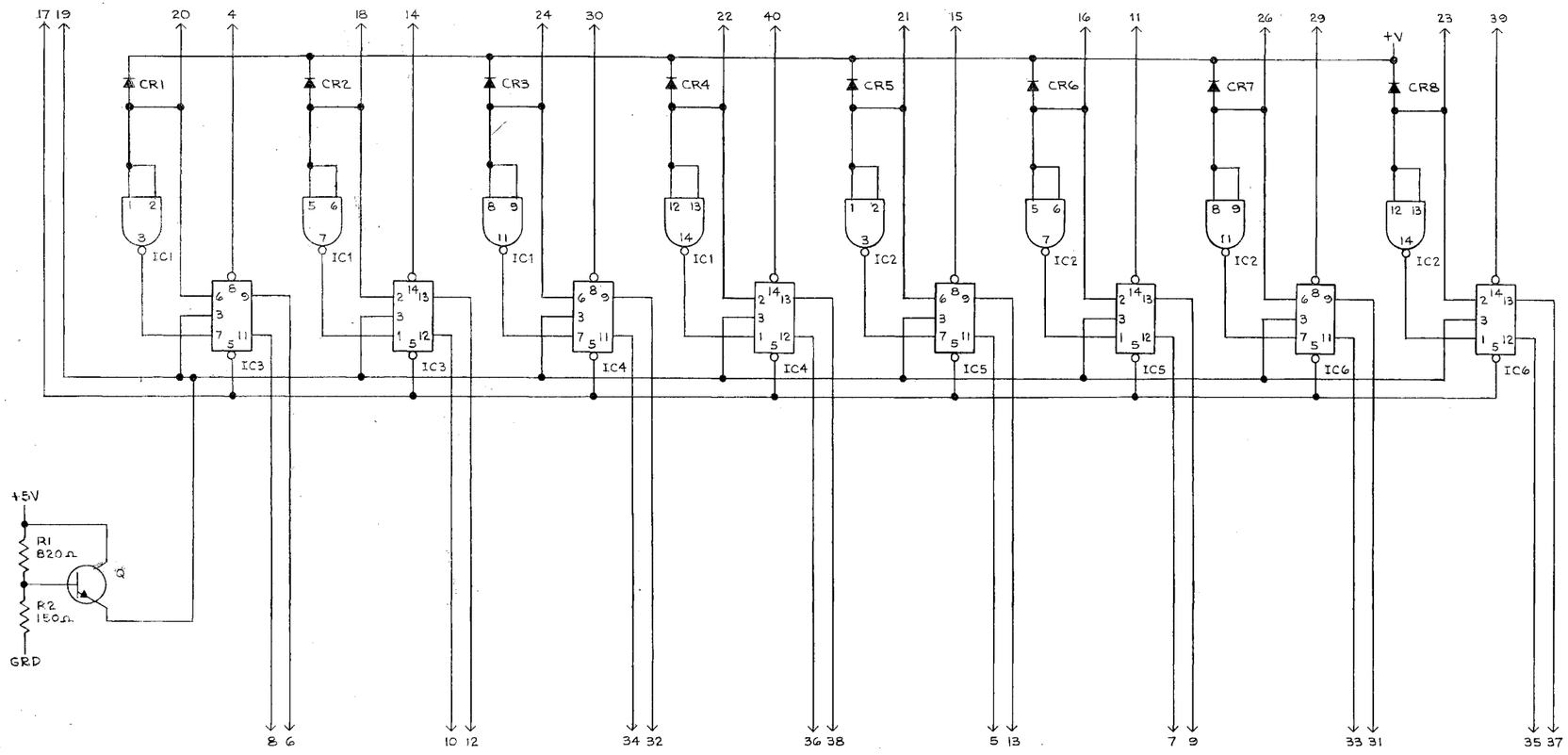
SCHEMATIC & ASSEMBLY
GENERAL REGISTER
EVEN

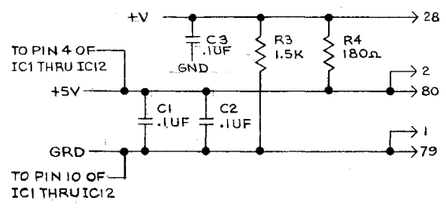
NEXT ASSY 141-100131-001

CODE IDENT NO.	SIZE		REV.
20886	D	160-100026	E

NOTES:
1. SEE SHEET 1

SIZE	160-100026		REV.
D			E
REV.	DESCRIPTION	DATE	APPD
A THRU D	SEE SHEET 1		
E	71-001 WKS 3-10-71 RKM	3-10-71	





ITEM	DWG. OR PART NO.	DESCRIPTION

Systems Engineering Laboratories
6901 West Sunrise Blvd., Fort Lauderdale, Florida 33310

DR C.WILLIAMS	4-23-68
CHK GPW	9-24-68
ENGR R Fox	11-12-69
PROJ E.W.Williams	11-12-69
APPD E.Wm	11-12-69
NEXT ASSY	

SCHEMATIC & ASSEMBLY
GENERAL REGISTER
EVEN

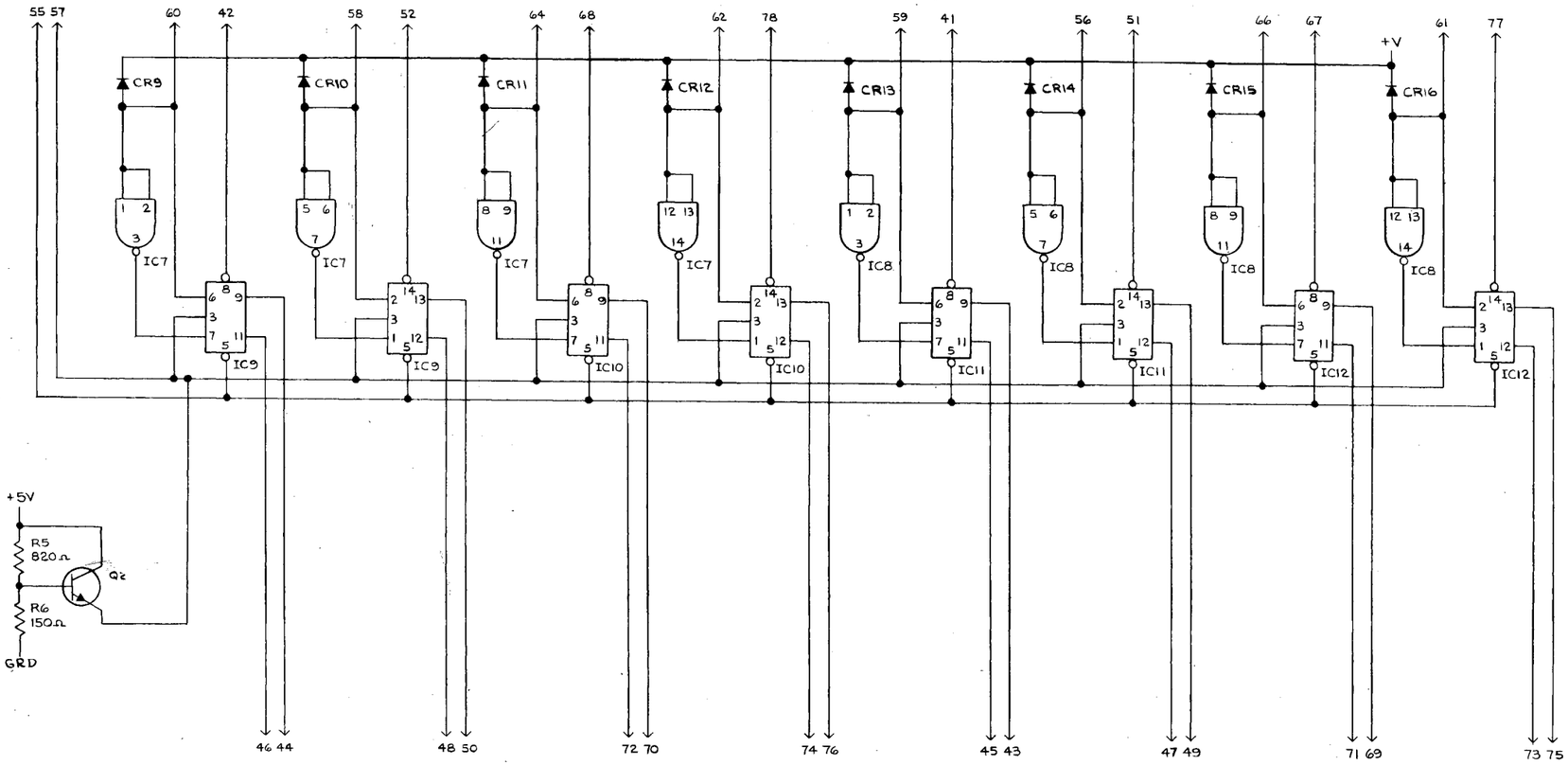
CODE IDENT NO.	SIZE		REV.
20886	D	160-100026	E

SHEET 2

160-100026 E

NOTES:
1. SEE SHEET 1

SIZE	160-100026		REV.
REV.	DESCRIPTION	DATE	APPD
A THRU C	SEE SHEET 1		
E	71-001 WKS 3-10-71 AKM	3-10-71	



ITEM	DWG. OR PART NO.	DESCRIPTION

THIS DOCUMENT AND THE INFORMATION CONTAINED HEREIN ARE THE PROPERTY OF SYSTEMS ENGINEERING LABORATORIES. IN CONSIDERATION OF THE RECEIPT OF THIS DOCUMENT, THE RECIPIENT AGREES NOT TO REPRODUCE, COPY, USE OR TRANSMIT THIS DOCUMENT IN WHOLE OR IN PART, FOR ANY PURPOSE, EXCEPT WITH APPROPRIATE APPROVAL OF SYSTEMS ENGINEERING LABORATORIES.

Systems Engineering Laboratories
6901 West Sunrise Blvd., Fort Lauderdale, Florida 33310

DR C.WILLIAMS	4-23-69	SCHEMATIC & ASSEMBLY GENERAL REGISTER EVEN
CHK GAW	9-24-69	
ENGR R FOR	11-12-69	
PROJ E Williams	11-12-69	
APPD EMU	11-12-69	
NEXT ASSY		

CODE IDENT NO.	SIZE		REV
20886	D	160-100026	E

SHEET 3

D 160-100026 E

160-100069 SCHEMATIC AND ASSEMBLY CABLE TERMINATOR

DESCRIPTION:

This circuit card contains 24 discrete component inverting stages designed to terminate twisted pair cables and reduce crosstalk between cables.

LIST of MATERIAL			Systems Engineering Laboratories	20886	LM160-100069	A
PREP	ERWOLFE	DATE 1-23-69	Fort Lauderdale, Florida 33310	CODE IDENT	SHEET 1 OF 2 SHEETS	REV
CHK	RKM	1-27-69		ITEM NOMENCLATURE: CABLE TERMINATOR		
ENGR		2-5-69				
APPD		2/5	USED ON:			

LTR	REVISION DESCRIPTION	DATE	APPD	LTR	REVISION DESCRIPTION	DATE	APPD
A	70-1012 RB 9-23-70 RKM	9-24-70					

RECORD OF REVISION STATUS OF EACH SHEET

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42
—	—																																							
A	A																																							

LM160-100069

S.E.L. Form 365-1

LIST of MATERIAL	Systems Engineering Laboratories	20886	LM 160-100069	A
ITEM NOMENCLATURE: CABLE TERMINATOR		CODE IDENT	SHEET 2 OF 2 SHEETS	REV

ITEM NO.	QTY REQ'D PER DASH NO. 001	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	REFERENCE DESIGNATION	REMARKS
1	1	164-100069-001	PRINTED CIRCUIT		FOR REV SEE 149-100001-000
2	REF	172-010322-001	DIMENSIONAL DWG		
3	REF	168-100069-001	DRILLING DWG		
4	24	110-010369-001	UNIPAD		
5	AR	258-400001-004	WIRE AWG 24		
6	AR	265-400001-071	SLEEVING		
7					
8					
9					
10	2	254-100700-002	CAP .1uF +80 -20% 10V CERAMIC	C1,2	
11	24	250-122369-002	TRANSISTOR	Q1-24	
12	24	253-100010-073	RES 1K ±5% 1/4W CMPSN	R1-24	
13	24	253-100010-080	RES 2K ±5% 1/4W CMPSN	R25-48	
14	24	253-100010-077	RES 1.5K ±5% 1/4W CMPSN	R49-72	

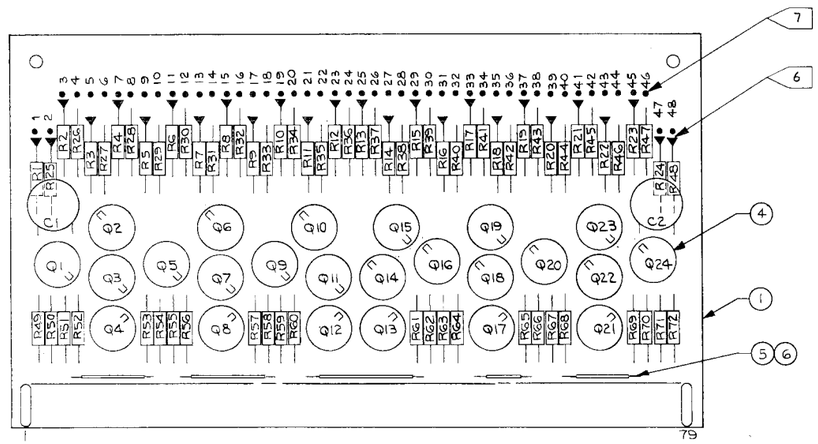
LM160-100069

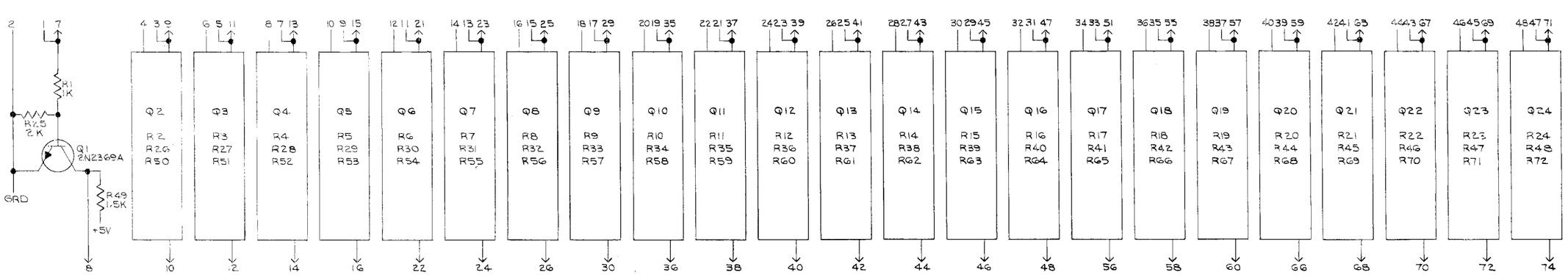
S.E.L. Form 365-2A

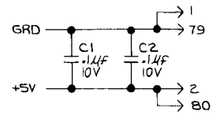
NOTES:
1. ALL ITEMS AS SPECIFIED IN LIST OF MATERIAL OR APPROVED EQUIVALENT.
2. UNLESS OTHERWISE SPECIFIED RESISTORS ARE ±5%, 1/4W.
3.
4. PRINTED WIRING BOARD SHALL MEET THE REQUIREMENTS OF 190-001050-001.
5. TEST PER SEL 95092A-1.
6. INDICATES TOP SOLDER (▶ QTY 26) NOT REQUIRED WHEN PLATED THRU.
7. • INDICATES HOLE TO BE FREE OF SOLDER.

SIZE	160-100069	REV.
D		A

REV.	DESCRIPTION	DATE	APPD
A	70-1012 RB 9-23-70 RKM	9/24/70	







APPLICABLE DOCUMENTS:
LIST OF MATERIAL LM 160-100069

ITEM	DWG. OR PART NO.	DESCRIPTION

Systems Engineering Laboratories
6901 West Sunrise Blvd., Fort Lauderdale, Florida 33310

DR	E R WOLFE	1-24-68
CHK	R K M	1-30-69
ENGR		2-5-69
PROJ		2-5-69
APPD		2/5
NEXT ASSY		

SCHEMATIC & ASSEMBLY
CABLE TERMINATOR

CODE IDENT NO.	SIZE		REV.
20886	D	160-100069	A

SHEET 1

ERN 011-2
DATE 11/14/69 REV A

160-100078 SECOND TTL QUAD TWO INPUT "NAND"

DESCRIPTION

Each gate functions as a NAND element in positive logic (as a NOR element in negative logic).

SPECIFICATIONS

Speed: Typical propagation delay:

10 nsec	(160-100078-005 - 160-100078-008)
6 nsec	(160-100078-001 - 160-100078-004)

Logic swing: typically 0.26 volts to 3.5 volts

Power: Average dissipation per gate;

15 mw	(160-100078-005 - 160-100078-008)
	(160-100078-001 - 160-100078-004)

888600 pjr

LIST of MATERIAL			Systems Engineering Laboratories	20886	LM 160-100078	A
PREP	ERWOLFE	DATE 1-10-69	Fort Lauderdale, Florida 33310	CODE IDENT	SHEET 1 OF 3 SHEETS	REV
CHK	RKM	1-13-69		ITEM NOMENCLATURE: SECOND TTL QUAD TWO INPUT "NAND"		
ENGR	Thomas L. Hughes	1-15-69				
APPD		1/15	USED ON: SYS-86			

LTR	REVISION DESCRIPTION	DATE	APPD
A	69-815; UPDATED TO LATEST NUMBERING SYSTEM. MS 10-3-69 RKM	10/6/69	

LTR	REVISION DESCRIPTION	DATE	APPD

RECORD OF REVISION STATUS OF EACH SHEET

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42
A	A	A																																							

LM 160-100078

S.E.L. Form 365-1

LIST of MATERIAL			Systems Engineering Laboratories	20886	LM 160-100078	A
ITEM NOMENCLATURE: SECOND TTL QUAD TWO INPUT NAND				CODE IDENT	SHEET 2 OF SHEETS	REV

ITEM NO.	QTY REQ'D PER DASH NO. 005	004	003	002	001	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	REFERENCE DESIGNATION	REMARKS
1	1	1	1	1	1	164-100078-001	PRINTED CIRCUIT		FOR REV SEE 149-100001-000
2	REF	REF	REF	REF	REF	172-016323-001	DIMENSIONAL DWG		
3	REF	REF	REF	REF	REF	168-100078-001	DRILLING DWG		
4	AR	AR	AR	AR	AR	258-400001-004	WIRE		
5	AR	AR	AR	AR	AR	265-400001-004	SLEEVING		
6									
7									
8									
9	2	2	2	2	2	254-100700-002	CAP. .1 μf	C1,2	
10	X	X	X	X	6	252-115022-001	INTEGRATED CIRCUIT	IC1-6	
11	X	X	X	6	X	252-115022-101		IC1-6	
12	X	X	6	X	X	252-115022-201		IC1-6	
13	X	6	X	X	X	252-115022-301		IC1-6	
14	6	X	X	X	X	252-115014-001		IC1-6	
15	X	X	X	X	X	252-115014-101		IC1-6	
16	X	X	X	X	X	252-115014-201		IC1-6	
17	X	X	X	X	X	252-115014-301	INTEGRATED CIRCUIT	IC1-6	
18	1	1	1	1	1	253-100010-077	RES. 1.5K	R1	
19	1	1	1	1	1	253-100010-055	RES. 180Ω	R2	

LM 160-100078

S.E.L. Form 365-2A

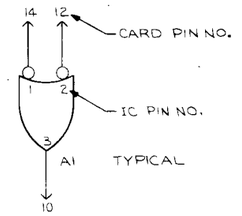
LIST of MATERIAL		Systems Engineering Laboratories	20886	LM 160-100078	A
ITEM NOMENCLATURE: SECOND TTL QUAD TWO INPUT NAND			CODE IDENT	SHEET 3 OF SHEETS	REV

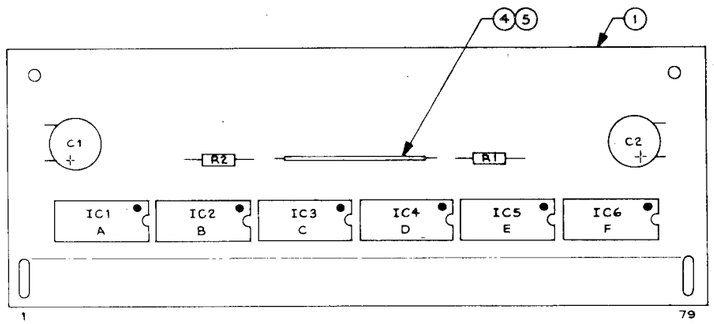
ITEM NO.	QTY REQ'D PER DASH NO. 008	007	006	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	REFERENCE DESIGNATION	REMARKS
1	1	1	1	164-100078-001	PRINTED CIRCUIT		FOR REV SEE 149-100001-000
2	REF	REF	REF	172-016323-001	DIMENSIONAL DWG		
3	REF	REF	REF	168-100078-001	DRILLING DWG		
4	AR	AR	AR	258-400001-004	WIRE		
5	AR	AR	AR	265-400001-004	SLEEVING		
6							
7							
8							
9	2	2	2	254-100700-002	CAP. .1 μf	C1,2	
10	X	X	X	252-115022-001	INTEGRATED CIRCUIT	IC1-6	
11	X	X	X	252-115022-101		IC1-6	
12	X	X	X	252-115022-201		IC1-6	
13	X	X	X	252-115022-301		IC1-6	
14	X	X	X	252-115014-001		IC1-6	
15	X	X	6	252-115014-101		IC1-6	
16	X	6	X	252-115014-201		IC1-6	
17	6	X	X	252-115014-301	INTEGRATED CIRCUIT	IC1-6	
18	1	1	1	253-100010-077	RES. 1.5K	R1	
19	1	1	1	253-100010-055	RES. 180Ω	R2	

LM 160-100078

NOTE

THE LOGIC ELEMENTS ON THIS CARD CAN BE USED TO IMPLEMENT EITHER "AND" OR "OR" FUNCTIONS. THE "AND" IMPLEMENTATION IS SHOWN FOR ALL CIRCUITS WITH AN EXAMPLE OF THE "OR" IMPLEMENTATION SHOWN DIRECTLY BELOW.





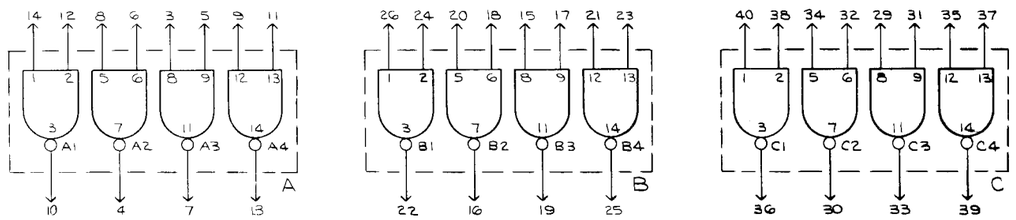
NOTES:
1. ALL ITEMS AS SPECIFIED IN LIST OF MATERIAL OR APPROVED EQUIVALENT.
2. UNLESS OTHERWISE SPECIFIED RESISTORS ARE ±5%.
3. FOR COMPLETE DOCUMENTATION USE PC ASSY MFG PROCESS CONTROL SPEC 149-100008-000 FOR CERTAIN CHANGES IN PROCESSES & COMPONENTS THAT MAY HAVE BEEN REFLECTED TO THE PART DESCRIBED.
4. THE LOGIC SYMBOLS ON THIS SHEET CONFORM TO MIL STD 806.
5. DASH NUMBERS 001-004 ARE SUHL II OR EQUIV. (50 MEGAHERTZ, 6 NANO-SECOND GATE PROPAGATION DELAY)
   DASH NUMBERS 005-008 ARE SUHL I OR EQUIV. (35 MEGAHERTZ, 12 NANO-SECOND GATE PROPAGATION DELAY)
   DASH NUMBERS 009-012 ARE COMBINATIONS OF LOGIC ELEMENTS WITH DIFFERENT FREQUENCY, TEMPERATURE OR FAN-OUT CHARACTERISTICS.
   FAN-OUT IN THE FOLLOWING TABLE IS DEFINED IN TERMS OF SUHL II (APPROX 2 ma SINK CURRENT FROM +V) LOADS.

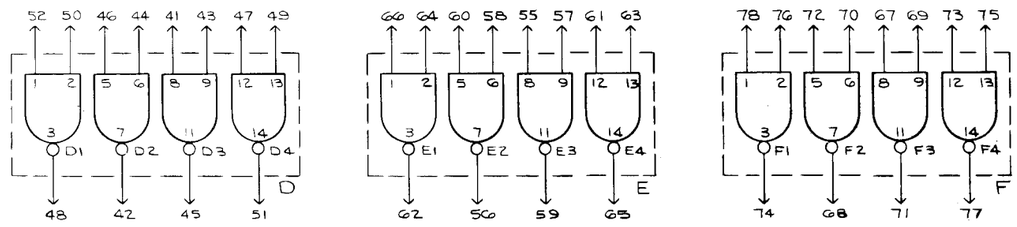
FAN-OUT	MILITARY -55°C TO +125°C	INDUSTRIAL 0°C TO +75°C
11	001	
6	002	008
9		003
5		004
15	005	
7	006	
12		007

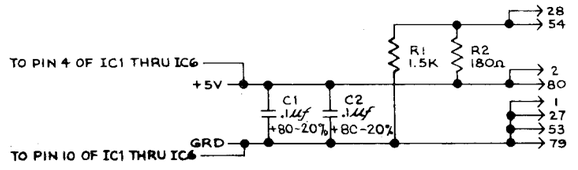
SIZE		REV.
D	160-100078	A

REV.	DESCRIPTION	DATE	APPD
A	69-815; UPDATED TO NEW NUMBERING SYSTEM. MS 10-3-69 RKM	10/6/69	

ERN 011-2
DATE 11/14/69 REV A







APPLICABLE DOCUMENTS:
LIST OF MATERIAL - LM 160-100078

ITEM	DWG. OR PART NO.	DESCRIPTION

Systems Engineering Laboratories
6901 West Sunrise Blvd., Fort Lauderdale, Florida 33310

DR ERWOLFE	1-10-69	LOGIC & ASSEMBLY SECOND TTL QUAD TWO INPUT "NAND"
CHK RKM	1-13-69	
ENGR	1-15-69	
PROJ	1-16-69	
APPD	11/14/69	
NEXT ASSY 141-100131-001	CODE IDENT NO. 20886	SIZE D — 160-100078 — REV. A

SHEET 1

160-100079 SCHEMATIC AND ASSEMBLY
HIGH-SPEED ONE SHOT

DESCRIPTION

This circuit card contains four high-speed one-shot circuits. The circuits are triggered by a positive to negative (+ voltage to ground) signal, producing a negative (+ voltage to ground) output pulse of adjustable duration. With C in microfarads and T (time) in microseconds (C=T/2,500), the value of C1, C2, C3, or C4 is changed to select the pulse duration of the circuit. Potentiometers R4, R7, R10, and R13 provide adjustment of the pulse duration for the range selected by the capacitor.

ERN. 075-1
REV. B DATE 5-20-70

LIST of MATERIAL			Systems Engineering Laboratories	20886	LM160-100079	D
PREP	RKM	DATE 2-5-69	Fort Lauderdale, Florida 33310	CODE IDENT	SHEET 1 OF 5 SHEETS	REV
CHK	F.L. Blatto	2-17-69		ITEM NOMENCLATURE: H.S. ONE SHOT		
ENGR		2-17-69				
APPD			USED ON:			

LTR	REVISION DESCRIPTION	DATE	APPD
A	ADDED ITEM 29; ITEM 15 VALUE WAS 1.5K; ITEM 16 VALUE WAS 180Ω. caw 5-28-69 RKM	6-2-69	
B	ADDED DASH 003 & 004 NC 11-25-69 RKM	12/3/69	MP
C	71-122; JWG 3-22-71	3-29-71	
D	71-504 JH 8-11-71 RKM	8-19-71	

LTR	REVISION DESCRIPTION	DATE	APPD

RECORD OF REVISION STATUS OF EACH SHEET

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42
B	B	B																																						
C	C	C	C	C																																				
D	D	C	D	C																																				

LM 160-100079

S.E.L. Form 365-1

R

LIST of MATERIAL	Systems Engineering Laboratories	20886	LM 160-100079	D
ITEM NOMENCLATURE: H.S. ONE SHOT		CODE IDENT	SHEET 2 OF SHEETS	REV

ITEM NO.	QTY REQ'D PER DASH NO. 005	004	003	002	001	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	REFERENCE DESIGNATION	REMARKS
1	1	1	1	1	1	164-100079-001	PRINTED CIRCUIT		FOR REV SEE 149-100001-000
2	REF	REF	REF	REF	REF	172-016322-001	DIMENSIONAL DWG		
3	REF	REF	REF	REF	REF	168-100079-001	DRILLING DWG		
4	4	4	4	2	4	110-010369-001	UNIPAD		
5									
6									
7									
8					4	S.A.T.	CAP	C1-C4	NOTE 4
9	4	4	4	4	4	254-100700-002	CAP. .1μf + 80-20% 10V CERAMIC	C5-C8	
10	8	8	8		8	251-114009-001	DIODE IN4009	CR1-CR8	
11	2	2	2		2	252-115412-301	INTEGRATED CIRCUIT	IC1, IC4	
12	2	2	2		2	252-115022-201	INTEGRATED CIRCUIT	IC2, IC5	
13	2	2	2		2	252-115008-201	INTEGRATED CIRCUIT	IC3, IC6	
14	4	4	4		4	250-123251-001	TRANSISTOR 2N3251	Q1-Q4	
15	1	1	1	1	1	253-100010-055	RES. 180Ω ±5% 1/4W COMP	R1	
16	1	1	1	1	1	253-100010-077	RES. 1.5K ±5% 1/4W COMP	R2	
17	4	4	4		4	253-100010-063	RES. 390Ω ±5% 1/4W COMP	R3,6,9,12	
18	4	4	4		4	253-100510-008	POT. 2K ±10% 1/2W WW	R4,7,10,13	
19	4	4	4		4	253-100010-097	RES. 10K ±5% 1/4W COMP	R5,8,11,14	
20				2		S.A.T.	CAP.	C1,2	NOTE 4
21				4		251-114009-001	DIODE IN4009	CR1-CR4	

LM 160-100079

S.E.L. Form 365-2A

R

LIST of MATERIAL	Systems Engineering Laboratories	20886	LM 160-100079	C
ITEM NOMENCLATURE: H.S. ONE SHOT		CODE IDENT	SHEET 3 OF SHEETS	REV

ITEM NO.	QTY REQ'D PER DASH NO. 005	004	003	002	001	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	REFERENCE DESIGNATION	REMARKS
22				1		252-115412-301	INTEGRATED CIRCUIT	IC1	
23				1		252-115022-201	INTEGRATED CIRCUIT	IC2	
24				1		252-115008-301	INTEGRATED CIRCUIT	IC3	
25				2		250-123251-001	TRANSISTOR 2N3251	Q1,2	
26				2		253-100010-063	RES. 390Ω ±5% 1/4W COMP	R3,6	
27				2		253-100510-008	POT. 2K ±10% 1/2W WW	R4,7	
28				2		253-100010-097	RES. 10K ±5% 1/4W COMP	R5,8	
29	4	4	4	4	4	253-100010-042	RES. 51Ω ±5% 1/4W COMP	R15-18	
30			1			254-100300-041	CAP 10μf ±10% 20V CER	C1	
31			1			254-100900-001	CAP .01μf ±10% 50V CER	C2	
32			1			254-100300-029	CAP 1.0μf ±10% 20V CER	C3	
33			1			254-100900-003	CAP .033μf ±10% 50V CER	C4	
34	1	1				254-100650-003	CAP .0033μf ±5% 50V CER	C1	
35		1				254-100300-029	CAP 1.0μf ±10% 20V CER	C2	
36	1	1				254-100300-023	CAP .33μf ±10% 20V CER	C3	
37	1	1				254-100620-001	CAP .001μf ± 5% 100V CER	C4	
38	1					254-100410-025	CAP .47UF ±20% 10V PLZD	C2	
39						254-100440-017	CAP .1DF ±20% 35V PLZD	C3	

LM 160-100079

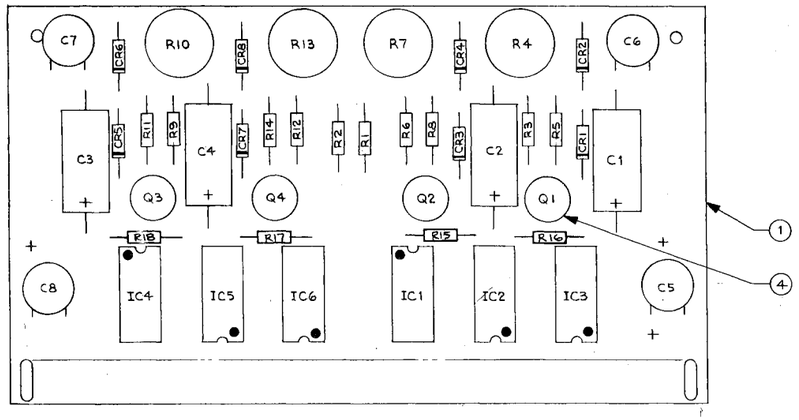
S.E.L. Form 365-2A

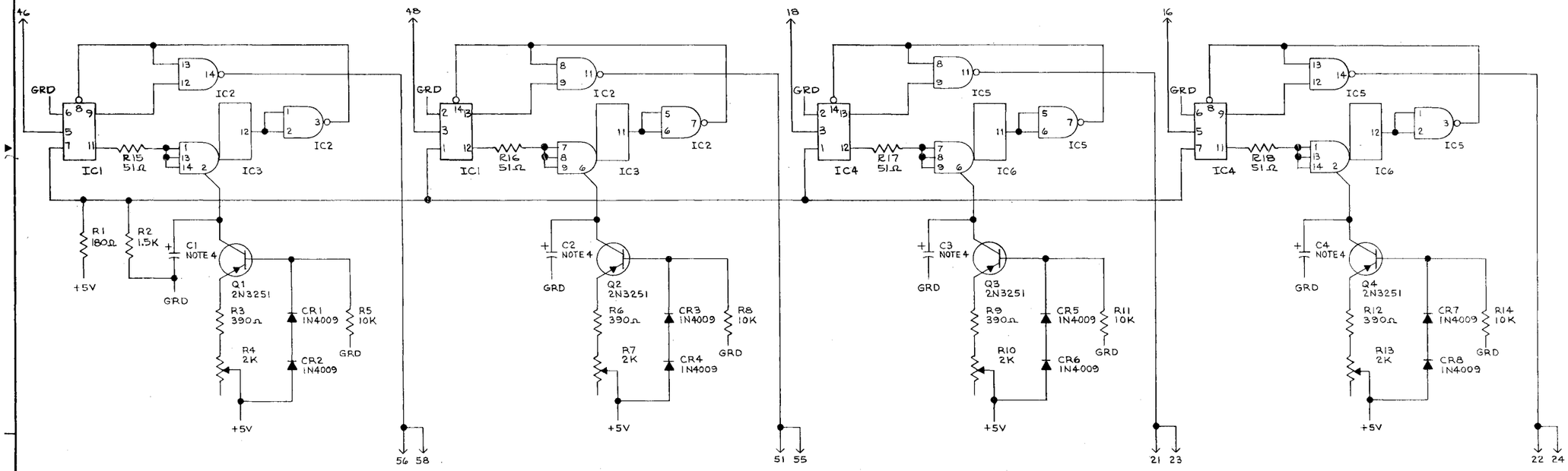
R

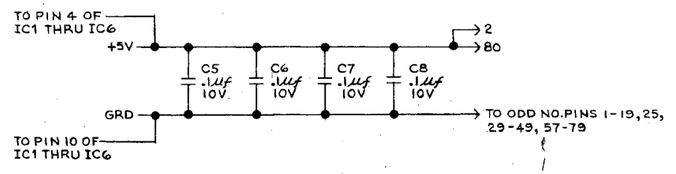
ENG. 013-1
REV. B DATE 5-20-70

NOTES.
1. ALL ITEMS AS SPECIFIED IN LIST OF MATERIAL OR APPROVED EQUIVALENT
2. UNLESS OTHERWISE SPECIFIED RESISTORS ARE ±5%, 1/4 W
3. FOR COMPLETE DOCUMENTATION USE PC ASSY MFG PROCESS CONTROL SPEC 149-100008-000 FOR CERTAIN CHANGES IN PROCESSES & COMPONENTS THAT MAY HAVE BEEN REFLECTED TO THE PART DESCRIBED.
4. C1 THRU C4, SELECT VALUE SUCH THAT C = T/2,500
C = CAPACITOR IN ufd.
T = NOMINAL DELAY (u SEC).

SIZE	160-100079		REV.
D			D
REV.	DESCRIPTION	DATE	APPD
A	ADDED R15-18; R1 WAS 1.5K; R2 WAS 180Ω; CAW 5-28-69 RKM	6/1/69	
B	UPDATED TO LATEST REV. OF LM NR 6 11-25-69 RKM	11/3/69	
C	71-122; JWG 3-22-71 RKM	3/26/71	
D	71-504 JWG 8-11-71 RKM	8-19-71	







APPLICABLE DOCUMENTS:
LIST OF MATERIAL- LM160-100079

ITEM	DWG. OR PART NO.	DESCRIPTION

Systems Engineering Laboratories
6901 West Sunrise Blvd., Fort Lauderdale, Florida 33310

DR	R.K.M	2-5-69
CHK	[illegible]	2-17-69
ENGR	[illegible]	1-28-70
PROJ	[illegible]	[illegible]
APPD	[illegible]	[illegible]
NEXT ASSY		

SCHEMATIC & ASSEMBLY
H.S. ONE SHOT

CODE IDENT NO.	SIZE		REV.
20886	D	160-100079	D

SHEET 1

LIST of MATERIAL	Systems Engineering Laboratories	20886	LM 160-100079	D
ITEM NOMENCLATURE: H.S. ONE SHOT		CODE IDENT	SHEET 4 OF SHEETS	REV

ITEM NO.	QTY REQ'D PER DASH NO. 006	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	REFERENCE DESIGNATION	REMARKS
1	1	164-100079-001	PRINTED CIRCUIT		FOR REV SEE 149-100001-000
2	REF	172-016322-001	DIMENSIONAL DWG		
3	REF	168-100079-001	DRILLING DWG		
4	4	110-010369-001	UNIPAD		
5					
6					
7					
8	X	S.A.T.	CAP	C1-C4	NOTE 4
9	4	254-100700-002	CAP .1UF +80-20% 10V CER	C5-C8	
10	8	251-114009-001	DIODE IN4009	CR1-CR8	
11	2	252-115412-301	INTEGRATED CIRCUIT	IC1, IC4	
12	2	252-115022-201	INTEGRATED CIRCUIT	IC2, IC5	
13	2	252-115008-201	INTEGRATED CIRCUIT	IC3, IC6	
14	4	250-123251-001	TRANSISTOR 2N3251	Q1-Q4	
15	1	253-100010-055	RES 180Ω ±5% 1/4W COMP	R1	
16	1	253-100010-077	RES 1.5K ±5% 1/4W COMP	R2	
17	4	253-100010-063	RES 390Ω ±5% 1/4W COMP	R3,6,9,12	
18	4	253-100510-008	POT 2K ±10% 1/2W WW	R4,7,10,13	
19	4	253-100010-097	RES 10K ±5% 1/4W COMP	R5,8,11,14	
20	X	S.A.T.	CAP	C1, C2	NOTE 4
21	X	251-114009-001	DIODE IN4009	CR1-CR4	

S.E.L. Form 365-2A

LM 160-100079

LIST of MATERIAL	Systems Engineering Laboratories	20886	LM 160-100079	C
ITEM NOMENCLATURE: H.S. ONE SHOT		CODE IDENT	SHEET 5 OF 5 SHEETS	REV

ITEM NO.	QTY REQ'D PER DASH NO. 006	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	REFERENCE DESIGNATION	REMARKS
22	X	252-115412-301	INTEGRATED CIRCUIT	IC1	
23	X	252-115022-201	INTEGRATED CIRCUIT	IC2	
24	X	252-115008-301	INTEGRATED CIRCUIT	IC3	
25	X	250-123251-001	TRANSISTOR 2N3251	Q1,2	
26	X	253-100010-063	RES 390Ω ±5% 1/4W COMP	R3,6	
27	X	253-100510-008	POT 2K ±10% 1/2W WW	R4,7	
28	X	253-100010-097	RES 10K ±5% 1/4W COMP	R5,8	
29	4	253-100010-042	RES 51Ω ±5% 1/4W COMP	R15-18	
30	1	254-100300-041	CAP 10UF ±10% 20V CER	C1	
31	1	254-100900-001	CAP .01UF ±10% 50V CER	C2	
32	X	254-100300-029	CAP 1.0UF ±10% 20V CER	C3	
33	1	254-100900-003	CAP .033UF ±10% 50V CER	C4	
34	X	254-100650-003	CAP .0033UF ±5% 50V CER	C1	
35	X	254-100300-029	CAP 1.0UF ±10% 20V CER	C2	
36	X	254-100300-023	CAP .33UF ±10% 20V CER	C3	
37	X	254-100620-001	CAP .001UF ±5% 100V CER	C4	
38	X	254-100410-025	CAP .47UF ±20% 10V PLZD	C2	
39	1	254-100440-017	CAP .1UF ±20% 35V PLZD	C3	

S.E.L. Form 365-2A

LM 160-100079

160-100222 BIPOLAR RECEIVER

DESCRIPTION

This circuit card consists of nine identical receiving circuits. Each circuit is capable of accepting a plus or minus (±) input voltage. Application of a positive input voltage turns transistor 1Q1 on and provides a zero (0) volt output. Application of a negative input voltage turns transistor 1Q1 off and provides a plus (+v) output.

SPECIFICATION

LOGIC LEVELS	0 volts = Logic ZERO +5 volts = Logic ONE	
POWER REQUIREMENTS	+5 volts	Pins 2 and 80
	Ground	Pins 1 and 70

ERN 123-2 DATE 10-7-70 REV -

LIST of MATERIAL			Systems Engineering Laboratories Fort Lauderdale, Florida 33310	20886	LM 160-100222	—
PREP	BJ CAMPBELL	DATE 5-11-70		CODE IDENT	SHEET 1 OF 2 SHEETS	REV
CHK	M Lazzaro	5-13-70		ITEM NOMENCLATURE: BI-POLAR RECEIVER		
ENGR		10/8/70				
APPD		10/9/70	USED ON:			

LTR	REVISION DESCRIPTION	DATE	APPD	LTR	REVISION DESCRIPTION	DATE	APPD

RECORD OF REVISION STATUS OF EACH SHEET

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42
—	—																																							

LM 160-100222

S.E.L. Form 365-1A

R

LIST of MATERIAL	Systems Engineering Laboratories	20886	LM 160-100222	—
ITEM NOMENCLATURE: BI-POLAR RECEIVER		CODE IDENT	SHEET 2 OF SHEETS	REV

ITEM NO.	QTY REQ'D PER DASH NO. 001	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	REFERENCE DESIGNATION	REMARKS
1	1	168-100222-001	DRILLING DWG		FOR REV SEE 149-100001-000
2	REF	164-100222-000	ART WORK		
3	REF	172-016322-001	DIMENSIONAL DWG		
4	1	110-010369-001	UNIPAD		
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15	2	254-100870-013	CAP 1μf±20%, 25V, CER	C1,2	
16	9	S.A.T.	CAP	1C3-9C3	
17	9	251-114009-001	DIODE	1CR1-9CR1	
18	9	250-122369-002	TRANSISTOR 2N2369	1Q1-9Q1	
19	9	253-100010-089	RES 4.7K±5% 1/4W	1R1-9R1	
20	9	253-100010-069	RES 680Ω±5% 1/4W	1R2-9R2	

LM 160-100222

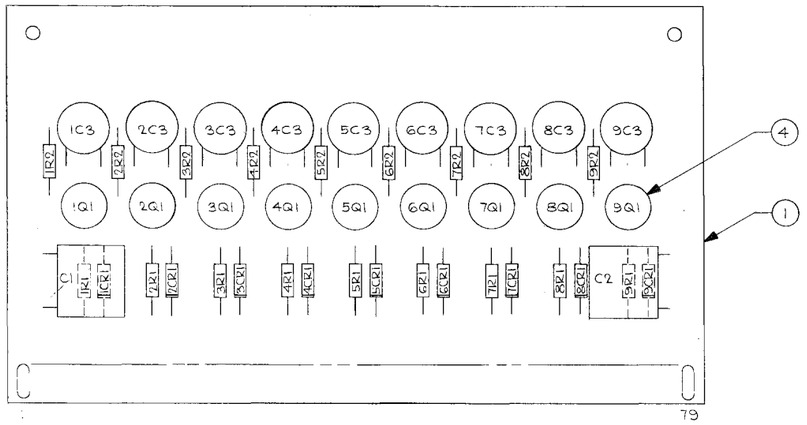
S.E.L. Form 365-2A

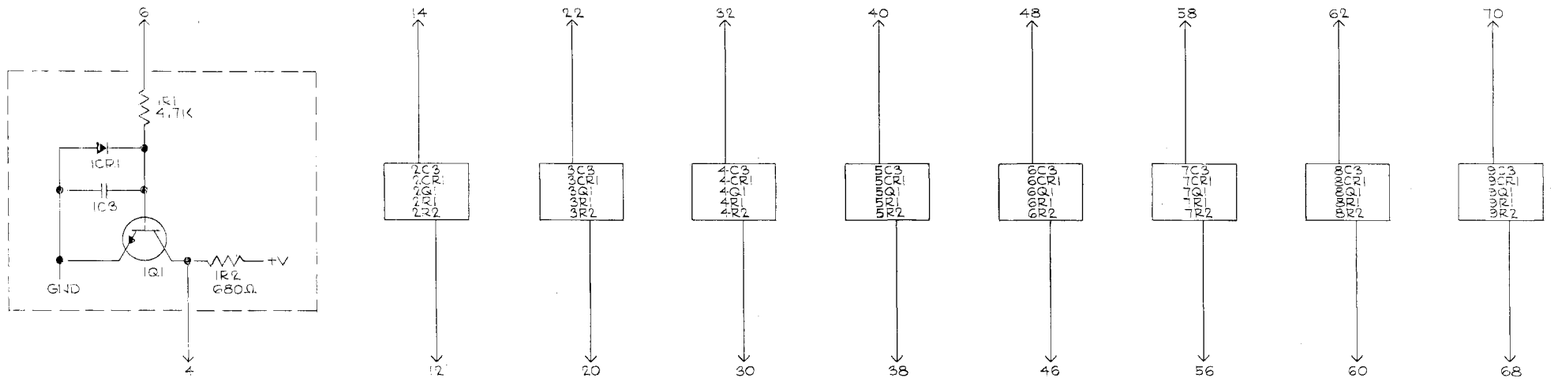
R

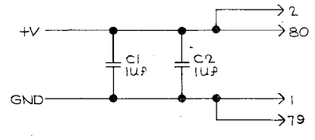
ERN 1205-2
DATE 10-7-70 REV - 1

REVISIONS

ZONE	LTR	DESCRIPTION	DATE	APPROVED







APPLICABLE DOCUMENTS:
LIST OF MATERIAL - LM 160-100222

NOTES:
1. ALL ITEMS AS SPECIFIED IN LIST OF MATERIAL OR APPROVED EQUIVALENT.
2. FOR COMPLETE DOCUMENTATION USE PC ASSY MFG PROCESS CONTROL SPEC 149-100008-000 FOR CERTAIN CHANGES IN PROCESSES & COMPONENTS THAT MAY HAVE BEEN REFLECTED TO THE PART DESCRIBED.

NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ON

BASIC DIMENSION	DECIMAL PLACES .XX	.XXX
UNDER 12	± .02	± .005
12 TO 24	± .03	± .010
OVER 24	± .06	± .015
ANGLES ± 0° 30'		

MATERIAL:
FINISH:

		DATE
DRAWN BJ CAMPBELL		5-6-70
CHECKED MS Fazzaro		5-13-70
ENGR		5/18/70
PROJ ENGR		5/18/70
APPROVED		5/18/70
APPROVED		

Systems Engineering Laboratories
Fort Lauderdale, Florida

BI-POLAR RECEIVER ASSEMBLY

SIZE	CODE IDENT NO.	DWG NO.
D	20886	160-100222

SCALE 2:1 SHEET 1

160-100223 BIPOLAR DRIVER

DESCRIPTION

This circuit card contains seven Bi-Polar Driver assemblies. When a positive potential is applied to pin 3, transistor 1Q1 is turned on. This causes the potential at the base of 1Q2 to become more negative and turn the PNP device on. Pin 6 now reflects a positive 6.3 volt potential. When a negative potential is applied to pin 3, transistor 1Q1 is turned off. This turns transistor 1Q2 off and also causes the potential at the base of 1Q3 to become more positive and turn the NPN device on. Pin 6 now reflects a negative 6.3 volt potential.

ERN 123-2 DATE 10-7-70 REV –

LIST of MATERIAL			Systems Engineering Laboratories	20886	LM160-100223	A
PREP	ARH	DATE 5-15-70	Fort Lauderdale, Florida 33310	CODE IDENT	SHEET 1 OF 2 SHEETS	REV
CHK	M A Fragano	5-22-70		ITEM NOMENCLATURE: BI-POLAR DRIVER		
ENGR		10/2/70				
APPD		10/2/70	USED ON:			

LTR	REVISION DESCRIPTION	DATE	APPD	LTR	REVISION DESCRIPTION	DATE	APPD
A	71-097 K. Dumas 2-17-71	2-23-71					

RECORD OF REVISION STATUS OF EACH SHEET

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42
–	–																																							
A	A																																							

LM160-100223

S.E.L. Form 365-1A

LIST of MATERIAL	Systems Engineering Laboratories	20886	LM160-100223	A
ITEM NOMENCLATURE: BI-POLAR DRIVER		CODE IDENT	SHEET 2 OF SHEETS	REV

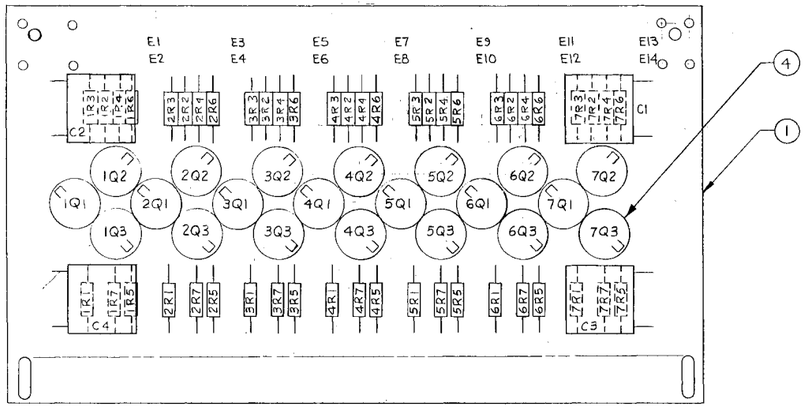
ITEM NO.	QTY REQ'D PER DASH NO. 001	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	REFERENCE DESIGNATION	REMARKS
1	1	168-100223-001	DRILLING DRAWING		FOR REV SEE 149-100001-000
2	REF	164-100223-000	ART WORK		
3	REF	172-016322-000	DIMENSIONAL DRAWING		
4	21	110-010369-001	UNIPAD		
5					
6					
7					
8					
9					
10					
11					
12					
13					
14	4	254-100870-013	CAP 1 UF ±20% 25V CER	C1-C4	
15	7	253-100010-089	RES 4.7K±5% 1/4W, CMPSN	1R6-7R6	
16	14	253-100010-065	RES 470Ω, ±5%, 1/4W, CMPSN	1R1-7R1, 1R7-7R7	
17	7	253-100010-047	RES 82Ω, ±5%, 1/4W, CMPSN	1R2-7R2	
18	7	253-100010-063	RES 390Ω, ±5%, 1/4W, CMPSN	1R3-7R3	
19	14	253-100010-037	RES 33Ω, ±5%, 1/4W, CMPSN	1R4-7R4, 1R5-7R5	
20	14	250-123947-001	TRANSISTORS 2N3947	1Q1-7Q1, 1Q3-7Q3	
21	7	250-123251-001	TRANSISTORS 2N3251	1Q2-7Q2	

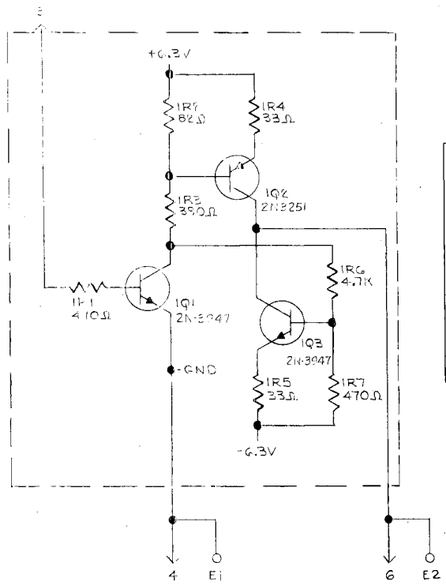
LM160-100223

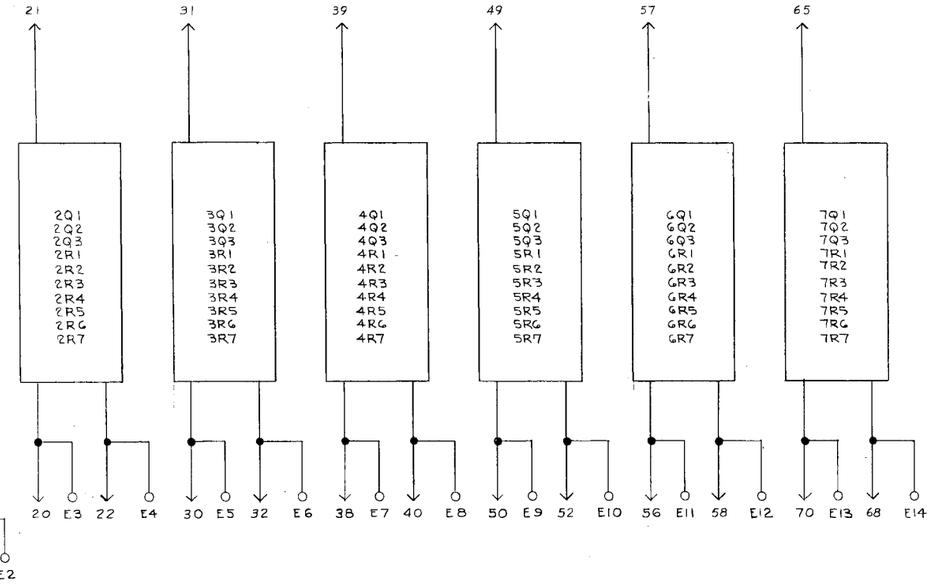
S.E.L. Form 365-2A

ERN 123-2
DATE 10-7-70 REV -

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	71-097 ADD 2N1711	2-23-71	

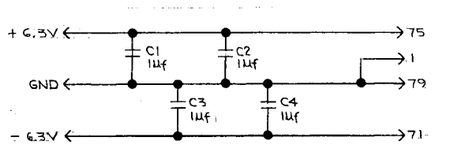






APPLICABLE DOCUMENTS:
LIST OF MATERIAL DWG NO 1123

NOTES:
1. ALL ITEMS AS SPECIFIED IN LIST OF MATERIAL OR APPROVED EQUIVALENT.
2. FOR COMPLETE DOCUMENTATION USE PC ASSY MFG PROCESS CONTROL SPEC 149-100008-000 FOR CERTAIN CHANGES IN PROCESSES & CONTROL THAT MAY HAVE BEEN REFLECTED TO THE PART DESCRIBED
3. SOLDERING AND ASSEMBLY PRACTICES IN ACCORDANCE WITH MFG STD 313-000002-000.



UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON		
BASIC DIMENSION	DECIMAL PLACES XX	XXX
UNDER 12	± .07	± .005
12 TO 24	± .03	± .010
OVER 24	± .06	± .015
ANGLES ± 0° 30'		

MATERIAL:
FINISH:

NEXT ASSY	USED ON
APPLICATION	

		DATE
DRAWN	Maria Sanfilippo	5-6-70
CHECKED	[illegible]	5-22-70
ENGR	[illegible]	6/8/70
PROJ ENGR	[illegible]	6/8/70
APPROVED	[illegible]	6/8/70
APPROVED	[illegible]	

Systems Engineering Laboratories
Fort Lauderdale, Florida

BI-POLAR DRIVER ASSY

SIZE	CODE IDENT NO.	DWG NO.
D	20886	160-100223

SCALE 2/1 NONE | SHEET 1 OF 1

160-100306 PRINTED WIRING BOARD
Bi-POLAR RECEIVER ASSEMBLY

DESCRIPTION

The Bi-Polar Receiver card contains nine identical circuits. The Bi-Polar circuit will accept both positive and negative going inputs and reflects a positive or ground potential at the output. A positive voltage applied to E1 turns transistor 1 Q 1 on and drives pin 8 to ground. A negative voltage applied to E1 turns 1 Q 1 off and places pin 8 to a positive potential. ICR1 and IC 5 form a noise discriminator circuit. With a negative input at E1, ICR1 clamps the base of IQ1 at ground potential, IC5 has two purposes, to react to positive noise spikes and as a time constant in turning 1 Q 1 on.

Circuit Operating Specifications:

INPUT	OUTPUT
+3v to 25v	Ground
0v to -25v	+ Voltage

ERN 174-2 DATE 8-23-71 REV -

LIST of MATERIAL			Systems Engineering Laboratories Fort Lauderdale, Florida 33310	20886	LM 160-100306	-
PREP	E. Lamson	DATE 3-10-71		CODE IDENT	SHEET 1 OF 2 SHEETS	REV
CHK	R. Medley	3-12-71		ITEM NOMENCLATURE: PRINTED WIRING BOARD BI-POLAR RECEIVER ASSEMBLY		
ENGR		8/23/71				
APPD		8/23/71	USED ON: 306-701630			

LTR	REVISION DESCRIPTION	DATE	APPD	LTR	REVISION DESCRIPTION	DATE	APPD

RECORD OF REVISION STATUS OF EACH SHEET

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42
-	-																																							

160-100306

S.E.L. Form 365-1A

LIST of MATERIAL	Systems Engineering Laboratories	20886	LM 160-100306	-
ITEM NOMENCLATURE: PWB BI-POLAR RECEIVER ASSY.		CODE IDENT	SHEET 2 OF 2 SHEETS	REV

ITEM NO.	QTY REQ'D PER DASH NO. 001	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	REFERENCE DESIGNATION	REMARKS
1	1	168-100306-001	PRINTED WIRING BOARD		FOR REV SEE 149-100001-000
2	REF	164-100306-000	PWB ARTWORK		
3	REF	172-016322-001	PWB DIMENSIONAL		
4	9	110-010369-001	UNIPAD		
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15	2	254-100700-002	CAP .1 UF +80-20% 10V CER	C1,2	
16	2	254-100410-041	CAP 10UF ±20% 10V PLZD	C3,4	
17	9	S.A.T.	CAP	IC5-9C5	
18	9	251-114009-001	DIODE 1N4009	ICR1-9CR1	
19	9	250-122369-002	TRANSISTOR 2N2369A	IQ1-9Q1	
20	9	253-100010-089	RES 4.7K ±5% 1/4W CMPSN	IR1-9R1	
21	9	253-100010-069	RES 680Ω ±5% 1/4W CMPSN	IR2-9R2	

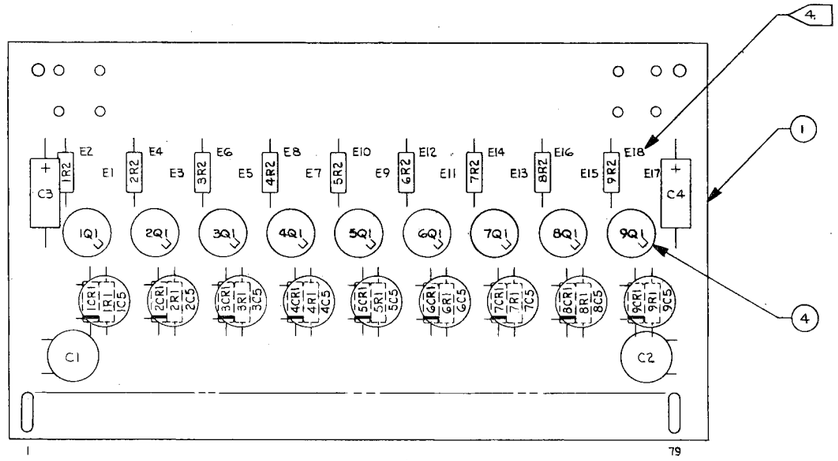
LM160-100306

S.E.L. Form 365-2A

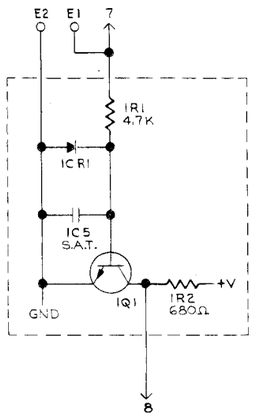
ERN 1149-6
DATE 8-23-71 REV- 1

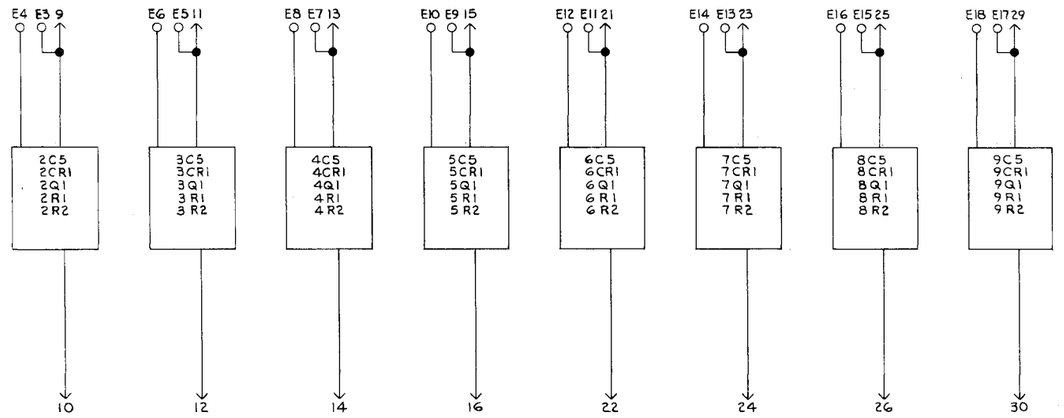
REVISIONS

ZONE	LTR	DESCRIPTION	DATE	APPROVED

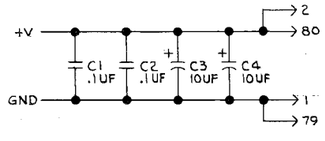


SCALE 2/1





APPLICABLE DOCUMENTS:
LM 160-100306



4. HOLES INDICATED E1 THRU E18 TO BE FREE OF SOLDER.
3. SOLDERING AND ASSEMBLY PRACTICES IN ACCORDANCE WITH MFG STD 318-000002-000.
2. FOR COMPLETE DOCUMENTATION USE PW ASSY MFG PROCESS CONTROL SPEC 149-100008-000 FOR CERTAIN CHANGES IN PROCESSES AND COMPONENTS THAT MAY HAVE BEEN REFLECTED TO THE PART DESCRIBED.
1. ALL ITEMS AS SPECIFIED IN LIST OF MATERIAL OR APPROVED EQUIVALENT.

NOTES:

144-100293	306-701630
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ON

BASIC DIMENSION	DECIMAL PLACES .XX	.XXX
UNDER 12	± .02	± .005
12 TO 24	± .03	± .010
OVER 24	± .06	± .015
ANGLES ± 0° 30'		

MATERIAL:
FINISH:

		DATE
DRAWN	E. Lamson	3-10-71
CHECKED	R. Hedberg	3-12-71
ENGR		4/23/71
PROJ. ENGR		4/23/71
APPROVED		4/23/71
APPROVED		

Systems Engineering Laboratories
Fort Lauderdale, Florida

PRINTED WIRING BOARD
BI-POLAR RECEIVER
ASSEMBLY

SIZE	CODE IDENT NO.	DWG NO.
D	20886	160-100306

SCALE NONE | REV LTR | SHEET 1 OF 1

160-900020 SECOND DUAL FOUR INPUT "NAND"

DESCRIPTION

This circuit card consists of six circuits, each containing two 4-input NAND gates. Each gate in these packages functions as a NAND element in positive logic (as a NOR element in negative logic).

SPECIFICATIONS (Element)

Speed: typical propagation delay;

10 nsec (160-900020-005 - 160-900020-008)
6 nsec (160-190021-001 - 160-900020-004)

Power: Average dissipation per gate

15 mw (160-900020-005 - 160-900020-008)
22 mw (160-900020-001 - 160-900020-004)

888600 pjr

LIST of MATERIAL			Systems Engineering Laboratories	20886	LM 160-900020	A
PREP	ERWOLFE	DATE 12-30-68	Fort Lauderdale, Florida 33310	CODE IDENT	SHEET 1 OF 3 SHEETS	REV
CHK	RKM	1-14-69		ITEM NOMENCLATURE: SECOND DUAL FOUR INPUT "NAND"		
ENGR	Thomas L. Hyde	1/15/69				
APPD		1/16	USED ON: SYS-86			

DATE 11/14/69 REV A

LTR	REVISION DESCRIPTION	DATE	APPD
A	69-826; UPDATED TO THE LATEST NUMBERING SYSTEM M.S. 10-7-69 RKM	10/8/69	JHRE

LTR	REVISION DESCRIPTION	DATE	APPD

RECORD OF REVISION STATUS OF EACH SHEET

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42
A	A	A																																							

LM 160-900020

S.E.L. Form 365-1

LIST of MATERIAL	Systems Engineering Laboratories	20886	LM 160-900020	A
ITEM NOMENCLATURE: SECOND DUAL FOUR "INPUT NAND"		CODE IDENT	SHEET 2 OF SHEETS	REV

ITEM NO.	QTY REQ'D PER DASH NO. 005	004	003	002	001	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	REFERENCE DESIGNATION	REMARKS
1	1	1	1	1	1	164-100078-001	PRINTED CIRCUIT		FOR REV SEE 149-100001-000
2	REF	REF	REF	REF	REF	172-016323-001	DIMENSIONAL DWG		
3	REF	REF	REF	REF	REF	168-100078-001	DRILLING DWG		
4	AR	AR	AR	AR	AR	258-400001-004	WIRE		
5	AR	AR	AR	AR	AR	265-400001-004	SLEEVING		
6									
7									
8									
9	2	2	2	2	2	254-100700-002	CAP. .1µf	C1,2	
10					6	252-115024-001	INTEGRATED CIRCUIT	IC1-6	
11				6		252-115024-101		IC1-6	
12			6			252-115024-201		IC1-6	
13		6				252-115024-301		IC1-6	
14	6					252-115004-001		IC1-6	
15						252-115004-101		IC1-6	
16						252-115004-201		IC1-6	
17						252-115004-301	INTEGRATED CIRCUIT	IC1-6	
18	1	1	1	1	1	253-100010-077	RES. 1.5K	R1	
19	1	1	1	1	1	253-100010-055	RES. 180Ω	R2	

LM 160-900020

S.E.L. Form 365-2A

LIST of MATERIAL	Systems Engineering Laboratories	20886	LM 160-900020	A
ITEM NOMENCLATURE: SECOND DUAL FOUR INPUT "NAND"		CODE IDENT	SHEET 3 OF SHEETS	REV

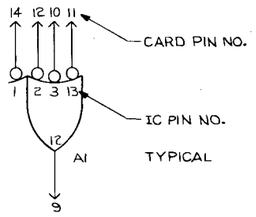
ITEM NO.	QTY REQ'D PER DASH NO. 008	007	006	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	REFERENCE DESIGNATION	REMARKS
1	1	1	1	164-100078-001	PRINTED CIRCUIT		FOR REV SEE 149-100001-000
2	REF	REF	REF	172-016323-001	DIMENSIONAL DWG		
3	REF	REF	REF	168-100078-001	DRILLING DWG		
4	AR	AR	AR	258-400001-004	WIRE		
5	AR	AR	AR	265-400001-004	SLEEVING		
6							
7							
8							
9	2	2	2	254-100700-002	CAP. .1µf	C1,2	
10				252-115024-001	INTEGRATED CIRCUIT	IC1-6	
11				252-115024-101		IC1-6	
12				252-115024-201		IC1-6	
13				252-115024-301		IC1-6	
14				252-115004-001		IC1-6	
15			6	252-115004-101		IC1-6	
16		6		252-115004-201		IC1-6	
17	6			252-115004-301	INTEGRATED CIRCUIT	IC1-6	
18	1	1	1	253-100010-077	RES. 1.5K	R1	
19	1	1	1	253-100010-055	RES. 180Ω	R2	

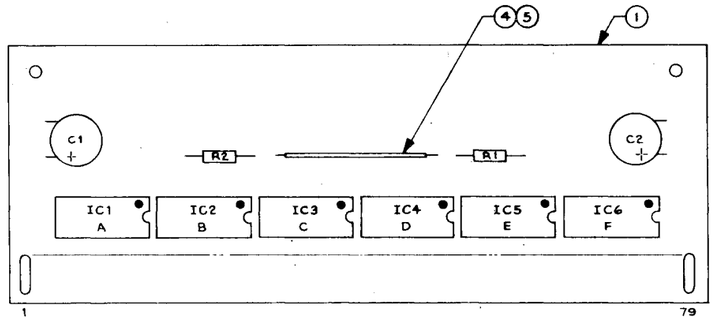
LM 160-900020

S.E.L. Form 365-2A

ECN 011-2
DATE 11/14/69 REV A

NOTE
THE LOGIC ELEMENTS ON THIS CARD CAN BE USED TO IMPLEMENT EITHER "AND" OR "OR" FUNCTIONS. THE "AND" IMPLEMENTATION IS SHOWN FOR ALL CIRCUITS WITH AN EXAMPLE OF THE "OR" IMPLEMENTATION SHOWN DIRECTLY BELOW.



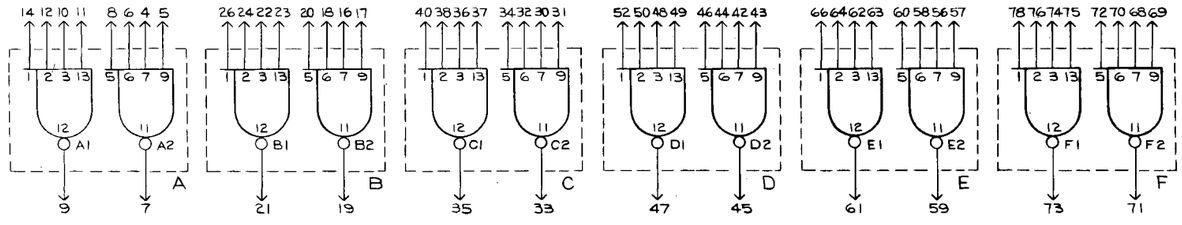


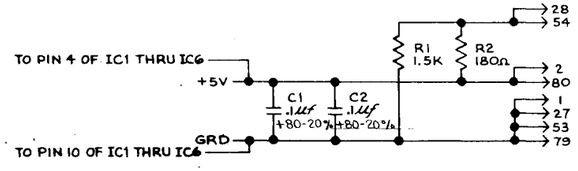
NOTES:
1. ALL ITEMS AS SPECIFIED IN LIST OF MATERIAL OR APPROVED EQUIVALENT.
2. UNLESS OTHERWISE SPECIFIED RESISTORS ARE ±5%.
3. FOR COMPLETE DOCUMENTATION USE PC ASSY MFG PROCESS CONTROL SPEC 149-100008-000 FOR CERTAIN CHANGES IN PROCESSES & COMPONENTS THAT MAY HAVE BEEN REFLECTED TO THE PART DESCRIBED.
4. THE LOGIC SYMBOLS ON THIS SHEET CONFORM TO MIL STD 806.
5. DASH NUMBERS 001-004 ARE SUHL II OR EQUIV. (50 MEGAHERTZ, 6 NANOSECOND GATE PROPAGATION DELAY)
   DASH NUMBERS 005-008 ARE SUHL I OR EQUIV. (35 MEGAHERTZ, 12 NANOSECOND GATE PROPAGATION DELAY)
   DASH NUMBERS 009-012 ARE COMBINATIONS OF LOGIC ELEMENTS WITH DIFFERENT FREQUENCY, TEMPERATURE OR FAN-OUT CHARACTERISTICS. FAN-OUT IN THE FOLLOWING TABLE IS DEFINED IN TERMS OF SUHL II (APPROX 2 ma SINK CURRENT FROM +V) LOADS.

FAN-OUT	MILITARY -55°C TO +125°C	INDUSTRIAL 0°C TO +75°C
11	001	
6	002	008
9		003
5		004
15	005	
7	006	
12		007

SIZE		REV.
D	160-900020	A

REV.	DESCRIPTION	DATE	APPD
A	69-826; UPDATED TO THE LATEST NUMBERING SYSTEM MS 10-7-69 RKM	10/8/69	JRC





APPLICABLE DOCUMENTS:
LIST OF MATERIAL - LM 160-900020

ITEM	DWG. OR PART NO.	DESCRIPTION

Systems Engineering Laboratories
6901 West Sunrise Blvd., Fort Lauderdale, Florida 33310

DR ERWOLFE	12-30-68	LOGIC & ASSEMBLY SECOND DUAL FOUR INPUT "NAND"
CHK RKM	1-14-69	
ENGR	1-15-69	
PROJ	1-16-69	
APPD	1/16/69	
NEXT ASSY 141-100131-001		

CODE IDENT NO.	SIZE		REV.
20886	D	160-900020	A

SHEET 1

D | 160-900020 | A

160-900022 SECOND JK FLIP-FLOP "AND" INPUTS

DESCRIPTION

This circuit card contains six JK flip-flops with two 3-input AND gates in each flip-flop. Refer to A1 TYPICAL on the logic and assembly drawing in regard to the following discussion.

The application of a ONE to IC pins 5, 6, and 7 along with a negative-going clock pulse on IC pin 3, causes the flip-flop to reset. The application of a ONE to IC pins 1, 2, and 14 along with a negative-going clock pulse on IC pin 3, causes the flip-flop to set. IC pins 8, 9, and 13 provide a direct set or reset to the flip-flop. The application of a ZERO to IC pins 8 or 9 resets the flip-flop, causing pin 11 to go High. The application of a ZERO to IC pin 13 sets the flip-flop, causing IC pin 12 to go High.

SPECIFICATIONS (Element)

Speed: Propagation delay times are typically 9 nsec for turn-off and 11 nsec for turn-on.

Logic Swing: Logic ZERO is typically 0.26 volts
Logic ONE is typically 3.2 volts

Power: typically 55 millivolts per flip-flop

Iin (mA) each data input:

1.66 (160-900022-003, -004, -007, -008, -011, and -012)

Iin (mA) clock input:

1.66 (160-900022-003 and -004)
2.5 (160-900022-007, -008, -011, and -012)

Iin (mA) dc set input:

2.8 (160-900022-003 and -004)
1.66 (160-900022-007, -008, -011 and -012)

Iin (mA) dc reset input:

Iin (mA) dc reset input:

2.8 (160-900022-003 and -004)
1.66 (160-900022-007, -008, -011, and -012)

Iout (mA) each output:

22.5 (160-900022-003 and -011)
20 (160-900022-007)
10 (160-900022-008)
12.5 (160-900022-004 and -012)

888600 pir

ERN 011-2
DATE 11/14/69 REV C

LIST of MATERIAL			Systems Engineering Laboratories	20886	LM 160-900022	D
PREP	ER WOLFE	DATE 1-2-69	Fort Lauderdale, Florida 33310	CODE IDENT	SHEET 1 OF 7 SHEETS	REV
CHK	RKM	1-14-69		ITEM NOMENCLATURE: SECOND JK FLIP-FLOP "AND" INPUTS		
ENGR	[signature]	1-15-69				
APPD	[signature]	1/16	USED ON: SYS-86			

LTR	REVISION DESCRIPTION	DATE	APPD
A	69; 433; ADDED ITEMS 6, 24, 25 & 26 08 6-18-69 RKM	7/24/69	[illegible]
B	69-688; ITEM 1 PART NO. WAS 164-100078-001. ITEM 3 PART NO. WAS 168-100078-001 N.J.L. 8-29-69 RKM	9/2/69	[illegible]
C	69-824; UPDATED TO THE LATEST NUMBERING SYSTEM M.S. 10-7-69 RKM	10/7/69	[illegible]
D	69-1005; ITEM 6 QTY WAS 4, ITEM 24 QTY WAS 4, ITEM 25 QTY WAS 2 (R3 & R5) VALUE WAS 820Ω, ITEM 26 QTY WAS 2 (R4 & R6) VALUE WAS 150Ω. BJC 1-26-70 RKM	1/26/70	[illegible]

LTR	REVISION DESCRIPTION	DATE	APPD

RECORD OF REVISION STATUS OF EACH SHEET

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42
D	D	D	D	D	D	D																																			

LM 160-900022

S.E.L. Form 365-1

LIST of MATERIAL						Systems Engineering Laboratories	20886	LM 160-900022	D
ITEM NOMENCLATURE: SECOND JK FLIP-FLOP "AND" INPUTS							CODE IDENT	SHEET 2 OF 7 SHEETS	REV

ITEM NO.	QTY REQ'D PER DASH NO. 005	004	003	002	001	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	REFERENCE DESIGNATION	REMARKS
1	1	1	1	1	1	164-100093-001	PRINTED CIRCUIT		FOR REV SEE 149-100001-000
2	REF	REF	REF	REF	REF	172-016323-001	DIMENSIONAL DWG		
3	REF	REF	REF	REF	REF	168-100093-001	DRILLING DWG		
4	AR	AR	AR	AR	AR	258-400001-004	WIRE		
5	AR	AR	AR	AR	AR	265-400001-004	SLEEVING		
6	6	6	6	6	6	110-010369-001	UNIPAD		
7									
8									
9	2	2	2	2	2	254-100700-002	CAP. .1μF	C1,2	
10	X	X	X	X	6	252-115420-001	INTEGRATED CIRCUIT	IC1-6	
11	X	X	X	6	X	252-115420-101	↕	IC1-6	
12	X	X	6	X	X	252-115420-201	↕	IC1-6	
13	X	6	X	X	X	252-115420-301	↕	IC1-6	
14	6	X	X	X	X	252-115405-001	↕	IC1-6	
15	X	X	X	X	X	252-115405-101	↕	IC1-6	
16	X	X	X	X	X	252-115405-201	↕	IC1-6	
17	X	X	X	X	X	252-115405-301	↕	IC1-6	
18	X	X	X	X	X	252-115425-001	↕	IC1-6	
19	X	X	X	X	X	252-115425-101	↕	IC1-6	
20	X	X	X	X	X	252-115425-201	↕	IC1-6	
21	X	X	X	X	X	252-115425-301	INTEGRATED CIRCUIT	IC1-6	

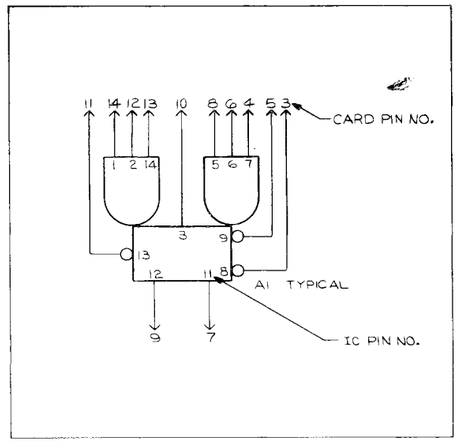
LM 160-900022

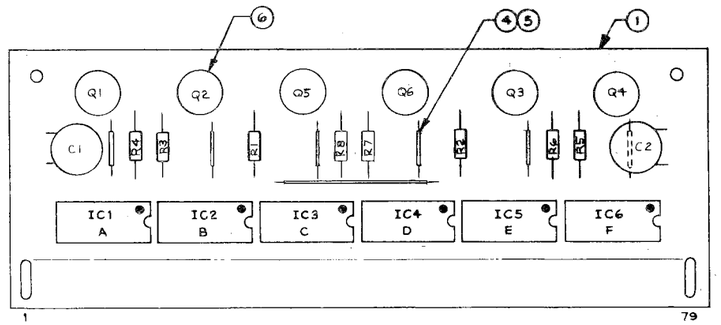
S.E.L. Form 365-2A

LIST of MATERIAL						Systems Engineering Laboratories	20886	LM 160-900022	D
ITEM NOMENCLATURE: SECOND JK FLIP-FLOP "AND" INPUTS							CODE IDENT	SHEET 3 OF 7 SHEETS	REV

ITEM NO.	QTY REQ'D PER DASH NO. 005	004	003	002	001	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	REFERENCE DESIGNATION	REMARKS
22	1	1	1	1	1	253-100010-077	RES. 1.5K ±5% 1/4W CMPSN	R1	
23	1	1	1	1	1	253-100010-055	RES. 180Ω ±5% 1/4W CMPSN	R2	
24	6	6	6	6	6	250-122369-002	TRANSISTOR	Q1-6	
25	3	3	3	3	3	253-100010-067	RES. 560Ω ±5% 1/4W CMPSN	R3,5,7	
26	3	3	3	3	3	253-100010-049	RES. 100Ω ±5% 1/4W CMPSN	R4,6,8	

LM 160-900022



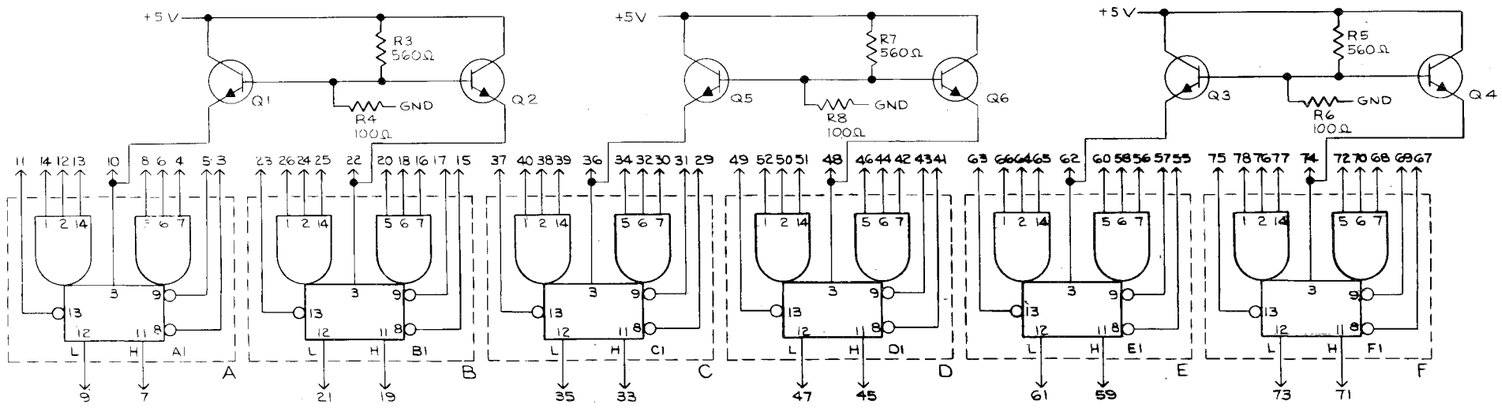


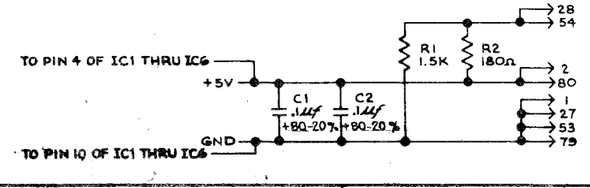
NOTES:
1. ALL ITEMS AS SPECIFIED IN LIST OF MATERIAL OR APPROVED EQUIVALENT.
2. UNLESS OTHERWISE SPECIFIED RESISTORS ARE ±5%.
3. FOR COMPLETE DOCUMENTATION USE PC ASSY MFG PROCESS CONTROL SPEC 149-10008-000 FOR CERTAIN CHANGES IN PROCESSES & COMPONENTS THAT MAY HAVE BEEN REFLECTED TO THE PART DESCRIBED.
4. THE LOGIC SYMBOLS ON THIS SHEET CONFORM TO MIL STD 806.
5. DASH NUMBERS 001-004 ARE SUHL II OR EQUIV.
   (50 MEGAHERTZ, 6 NANO-SECOND GATE PROPAGATION DELAY)
   DASH NUMBERS 005-008 ARE SUHL I OR EQUIV.
   (35 MEGAHERTZ, 12 NANO-SECOND GATE PROPAGATION DELAY)
   DASH NUMBERS 009-012 ARE COMBINATIONS OF LOGIC ELEMENTS WITH DIFFERENT FREQUENCY, TEMPERATURE OR FAN-OUT CHARACTERISTICS. FAN-OUT IN THE FOLLOWING TABLE IS DEFINED IN TERMS OF SUHL II (APPROX 2 ma SINK CURRENT FROM +V) LOADS.

FAN-OUT	MILITARY -55°C TO +125°C	INDUSTRIAL 0°C TO +75°C
15	001, 005, 009	
7	002, 006, 010	
12		003, 007, 011
6		004, 008, 012

SIZE		REV.
D	160-900022	D

REV.	DESCRIPTION	DATE	APPD
A	69-433; ADDED CLAMP CIRCUITS. DB 6-18-69 RKM	7/29/69	
B	69-688; UPDATED TO LATEST REV OF LM NJL 8-29-69 RKM	9/26/69	
C	69-824, UPDATED TO THE LATEST NUMBERING SYSTEM MS 10-7-69 RKM	10/7/69	
D	69-1005; ADDED CLAMP CIRCUIT TO IC3 & IC4; R3 & R5 WERE 820Ω; R4 & R6 WERE 150Ω. BJC 1-26 70 RKM	1/26/70	





APPLICABLE DOCUMENTS:
LIST OF MATERIAL - LM 160-900022

ITEM	DWG. OR PART NO.	DESCRIPTION

Systems Engineering Laboratories
6901 West Sunrise Blvd., Fort Lauderdale, Florida 33310

DR ER WOLFE	1-2-69	LOGIC & ASSEMBLY SECOND JK FLIP-FLOP "AND" INPUTS
CHK RKM	1-14-69	
ENGR	1-15-69	
PROJ	1-16-69	
APP	1/16/69	
NEXT ASSY 141-10013-001		CODE IDENT NO. 20886 / SIZE D / 160-900022 / REV. D

SHEET 1

D 160-900022 D 11

LIST of MATERIAL	Systems Engineering Laboratories	20886	LM 160-900022	D
ITEM NOMENCLATURE: SECOND JK FLIP-FLOP "AND" INPUTS		CODE IDENT	SHEET 4 OF 7 SHEETS	REV

ITEM NO.	QTY REQ'D PER DASH NO. 010	009	008	007	006	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	REFERENCE DESIGNATION	REMARKS
1	1	1	1	1	1	164-100093-001	PRINTED CIRCUIT		FOR REV SEE 149-100001-000
2	REF	REF	REF	REF	REF	172-016323-001	DIMENSIONAL DWG		
3	REF	REF	REF	REF	REF	168-100093-001	DRILLING DWG		
4	AR	AR	AR	AR	AR	258-400001-004	WIRE		
5	AR	AR	AR	AR	AR	265-400001-004	SLEEVING		
6	6	6	6	6	6	110-010369-001	UNIPAD		
7									
8									
9	2	2	2	2	2	254-100700-002	CAP. .1 Mf	C1,2	
10						252-115420-001	INTEGRATED CIRCUIT	IC1-6	
11						252-115420-101		IC1-6	
12						252-115420-201		IC1-6	
13						252-115420-301		IC1-6	
14						252-115405-001		IC1-6	
15					6	252-115405-101		IC1-6	
16				6		252-115405-201		IC1-6	
17			6			252-115405-301		IC1-6	
18		6				252-115425-001		IC1-6	
19	6					252-115425-101		IC1-6	
20						252-115425-201		IC1-6	
21						252-115425-301	INTEGRATED CIRCUIT	IC1-6	

LM 160-900022

S.E.L. Form 365-2A

LIST of MATERIAL	Systems Engineering Laboratories	20886	LM 160-900022	D
ITEM NOMENCLATURE: SECOND JK FLIP-FLOP "AND" INPUTS		CODE IDENT	SHEET 5 OF 7 SHEETS	REV

ITEM NO.	QTY REQ'D PER DASH NO. 010	009	008	007	006	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	REFERENCE DESIGNATION	REMARKS
22	1	1	1	1	1	253-100010-077	RES. 1.5K ±5% 1/4W CMPSN	R1	
23	1	1	1	1	1	253-100010-055	RES. 180Ω ±5% 1/4W CMPSN	R2	
24	6	6	6	6	6	250-122369-002	TRANSISTOR	Q1-6	
25	3	3	3	3	3	253-100010-067	RES. 560Ω ±5% 1/4W CMPSN	R3,5,7	
26	3	3	3	3	3	253-100010-049	RES. 100Ω ±5% 1/4W CMPSN	R4,6,8	

LM 160-900022

S.E.L. Form 365-2A

LIST of MATERIAL	Systems Engineering Laboratories	20886	LM 160-900022	D
ITEM NOMENCLATURE: SECOND JK FLIP-FLOP "AND" INPUTS		CODE IDENT	SHEET 6 OF 7 SHEETS	REV

ITEM NO.	QTY REQ'D PER DASH NO. 012	011	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	REFERENCE DESIGNATION	REMARKS
1	1	1	164-100093-001	PRINTED CIRCUIT		FOR REV SEE 149-100001-000
2	REF	REF	172-016323-001	DIMENSIONAL DWG		
3	REF	REF	168-100093-001	DRILLING DWG		
4	AR	AR	258-400001-004	WIRE		
5	AR	AR	265-400001-004	SLEEVING		
6	6	6	110-010369-001	UNIPAD		
7						
8						
9	2	2	254-100700-002	CAP. .1 Mf	C1,2	
10			252-115420-001	INTEGRATED CIRCUIT	IC1-6	
11			252-115420-101		IC1-6	
12			252-115420-201		IC1-6	
13			252-115420-301		IC1-6	
14			252-115405-001		IC1-6	
15			252-115405-101		IC1-6	
16			252-115405-201		IC1-6	
17			252-115405-301		IC1-6	
18			252-115425-001		IC1-6	
19			252-115425-101		IC1-6	
20		6	252-115425-201		IC1-6	
21	6		252-115425-301	INTEGRATED CIRCUIT	IC1-6	

LM 160-900022

S.E.L. Form 365-2A

LIST of MATERIAL	Systems Engineering Laboratories	20886	LM 160-900022	D
ITEM NOMENCLATURE: SECOND JK FLIP-FLOP "AND" INPUTS		CODE IDENT	SHEET 7 OF 7 SHEETS	REV

ITEM NO.	QTY REQ'D PER DASH NO. 012	011	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	REFERENCE DESIGNATION	REMARKS
22	1	1	253-100010-077	RES. 1.5K ±5% 1/4W CMPSN	R1	
23	1	1	253-100010-055	RES. 180Ω ±5% 1/4W CMPSN	R2	
24	6	6	250-122369-002	TRANSISTOR	Q1-6	
25	3	3	253-100010-067	RES. 560Ω ±5% 1/4W CMPSN	R3,5,7	
26	3	3	253-100010-049	RES. 100Ω ±5% 1/4W CMPSN	R4,6,8	

LM 160-900022

S.E.L. Form 365-2A

160-900023 DUAL JK FLIP-FLOP COMMON CLOCK

DESCRIPTION

This circuit card contains six dual flip-flop circuits. The clock input terminal is common to both flip-flops in the package. The circuits also have a common reset terminal. However, all flip-flops have separate SET input terminals.

Refer to HITYPICAL on the logic schematic in regard to the following discussion. The application of a High to IC pins along with the negative going edge of a clock pulse on IC pin 3 causes the flip-flop to set.

The application of a High to IC pin 1 along with the negative going edge of a clock pulse on IC pin 3 causes the flip-flop to reset. IC pin 14 provides a synchronous (direct) reset or preset to the flip-flop. The application of a Low to IC pin 14 sets the flip-flop, causing IC pin 13 to go High. The application of a Low to IC pin 5 resets the flip-flop, causing IC pin 12 to go iligh

DATE 11/14/69 REV C

LIST of MATERIAL			Systems Engineering Laboratories	20886	LM160-900023	E
PREP	ERWOLFE	DATE 1-3-69	Fort Lauderdale, Florida 33310	CODE IDENT	SHEET 1 OF 3 SHEETS	REV
CHK	RKM	1-14-69		ITEM NOMENCLATURE: SECOND DUAL JK FLIP-FLOP COMMON CLOCK		
ENGR	Thomas L. Taylor	1-15-69				
APPD			USED ON: SYS-86			

LTR	REVISION DESCRIPTION	DATE	APPD
A	69:432; ADDED ITEMS 6,8,20&21 DB 6-18-69 RKM	7/25/69	MRC
B	69:687; ITEM 1 PART NO. WAS 164-100078-001, ITEM 3 PART NO. WAS 168-100078-001 N.J.L. 8-29-69 RKM	9/2/69	MRC
C	69-823; UPDATED TO THE LATEST NUMBERING SYSTEM. M.S. 10-7-69. RKM	10/7/69	MRC
D	69-1007; ITEM 6 QTY WAS 4; ITEM 8 QTY WAS 4; ITEM 20 QTY WAS 2(R3,5) VALUE WAS 820Ω, ITEM 21 QTY WAS 2 (R4,6) VALUE WAS 150Ω. BJC 1-26-70 RKM	1/26/70	MRC
E	70-317; R.A. 7-27-70	7/29/70	RB

RECORD OF REVISION STATUS OF EACH SHEET

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42
D	D	D																																						
E	D	D																																						

LM160-900023

S.E.L. Form 365-1

LIST of MATERIAL	Systems Engineering Laboratories	20886	LM 160-900023	L
ITEM NOMENCLATURE: SECOND DUAL JK FLIP-FLOP COMMON CLOCK		CODE IDENT	SHEET 2 OF 3 SHEETS	REV

ITEM NO.	QTY REQ'D PER DASH NO. 005	004	003	002	001	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	REFERENCE DESIGNATION	REMARKS
1	1	1	1	1	1	164-100093-001	PRINTED CIRCUIT		FOR REV SEE 149-100001-000
2	REF	REF	REF	REF	REF	172-016323-001	DIMENSIONAL DWG		
3	REF	REF	REF	REF	REF	168-100093-001	DRILLING DWG		
4	AR	AR	AR	AR	AR	258-400001-004	WIRE		
5	AR	AR	AR	AR	AR	265-400001-004	SLEEVING		
6	6	6	6	6	6	110-010369-001	UNIPAD		
7									
8	6	6	6	6	6	250-122369-002	TRANSISTOR	Q1-6	
9	2	2	2	2	2	254-100700-002	CAP. .1μf	C1,2	
10	X	X	X	X	6	252-115413-001	INTEGRATED CIRCUIT	IC1-6	
11	X	X	X	6	X	252-115413-101	↕	IC1-6	
12	X	X	6	X	X	252-115413-201	↕	IC1-6	
13	X	6	X	X	X	252-115413-301	↕	IC1-6	
14	6	X	X	X	X	252-115411-001	↕	IC1-6	
15	X	X	X	X	X	252-115411-101	↕	IC1-6	
16	X	X	X	X	X	252-115411-201	↕	IC1-6	
17	X	X	X	X	X	252-115411-301	INTEGRATED CIRCUIT	IC1-6	
18	1	1	1	1	1	253-100010-077	RES. 1.5K ±5% 1/4W CMPSN	R1	
19	1	1	1	1	1	253-100010-055	RES. 180Ω ±5% 1/4W CMPSN	R2	
20	3	3	3	3	3	253-100010-067	RES. 560Ω ±5% 1/4W CMPSN	R3,5,7	
21	3	3	3	3	3	253-100010-049	RES. 100Ω ±5% 1/4W CMPSN	R4,6,8	

LM160-900023

S.E.L. Form 365-2A

LIST of MATERIAL	Systems Engineering Laboratories	20886	LM 160-900023	D
ITEM NOMENCLATURE: SECOND DUAL JK FLIP-FLOP COMMON CLOCK		CODE IDENT	SHEET 3 OF 3 SHEETS	REV

ITEM NO.	QTY REQ'D PER DASH NO. 008	007	006	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	REFERENCE DESIGNATION	REMARKS
1	1	1	1	164-100093-001	PRINTED CIRCUIT		FOR REV SEE 149-100001-000
2	REF	REF	REF	172-016323-001	DIMENSIONAL DWG		
3	REF	REF	REF	168-100093-001	DRILLING DWG		
4	AR	AR	AR	258-400001-004	WIRE		
5	AR	AR	AR	265-400001-004	SLEEVING		
6	6	6	6	110-010369-001	UNIPAD		
7							
8	6	6	6	250-122369-002	TRANSISTOR	Q1-6	
9	2	2	2	254-100700-002	CAP. .1μf	C1,2	
10	X	X	X	252-115413-001	INTEGRATED CIRCUIT	IC1-6	
11	X	X	X	252-115413-101	↕	IC1-6	
12	X	X	X	252-115413-201	↕	IC1-6	
13	X	X	X	252-115413-301	↕	IC1-6	
14	X	X	X	252-115411-001	↕	IC1-6	
15	X	X	6	252-115411-101	↕	IC1-6	
16	X	6	X	252-115411-201	↕	IC1-6	
17	6	X	X	252-115411-301	INTEGRATED CIRCUIT	IC1-6	
18	1	1	1	253-100010-077	RES. 1.5K ±5% 1/4W CMPSN	R1	
19	1	1	1	253-100010-055	RES. 180Ω ±5% 1/4W CMPSN	R2	
20	3	3	3	253-100010-067	RES. 560Ω ±5% 1/4W CMPSN	R3,5,7	
21	3	3	3	253-100010-049	RES. 100Ω ±5% 1/4W CMPSN	R4,6,8	

LM160-900023

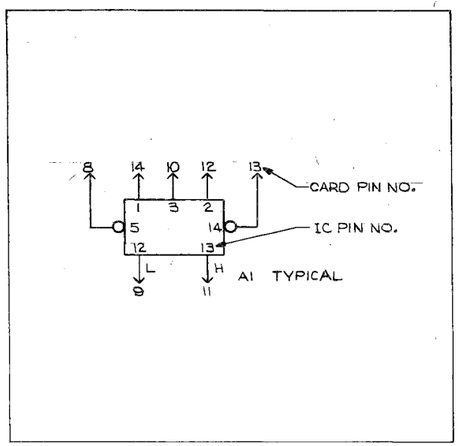
S.E.L. Form 365-2A

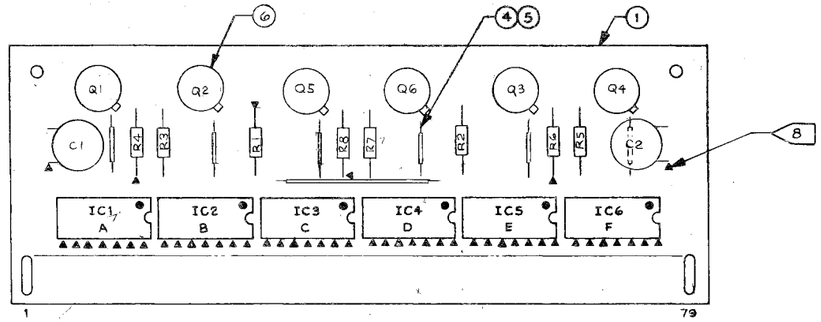
ERN 011
DATE 11/14/69 REV C

SIZE		REV.
D	160-900023	E

REV.	DESCRIPTION	DATE	APPD
A	69-432; ADDED CLAMP CIRCUITS DB 6-18-69 RKM	7/24/69	
B	69-687; UPDATED TO LATEST REV. OF L M N.L. 8-29-69 RKM	9/2/69	
C	69-823; UPDATED TO THE LATEST NUMBERING SYSTEM MS 10-7-69 RKM	10/7/69	
D	69-1007; ADDED CLAMP CIRCUIT TO IC3 & IC4; R3 & R5 WERE 820Ω, R4 & R6 WERE 150Ω. B.J.C 1-23-70 RKM	1/26/70	
E	70-317; R.A. 7-27-70 7-29-70	7/31/70	

NOTES.
1. ALL ITEMS AS SPECIFIED IN LIST OF MATERIAL OR APPROVED EQUIVALENT.
2. UNLESS OTHERWISE SPECIFIED RESISTORS ARE ±5%.
3.

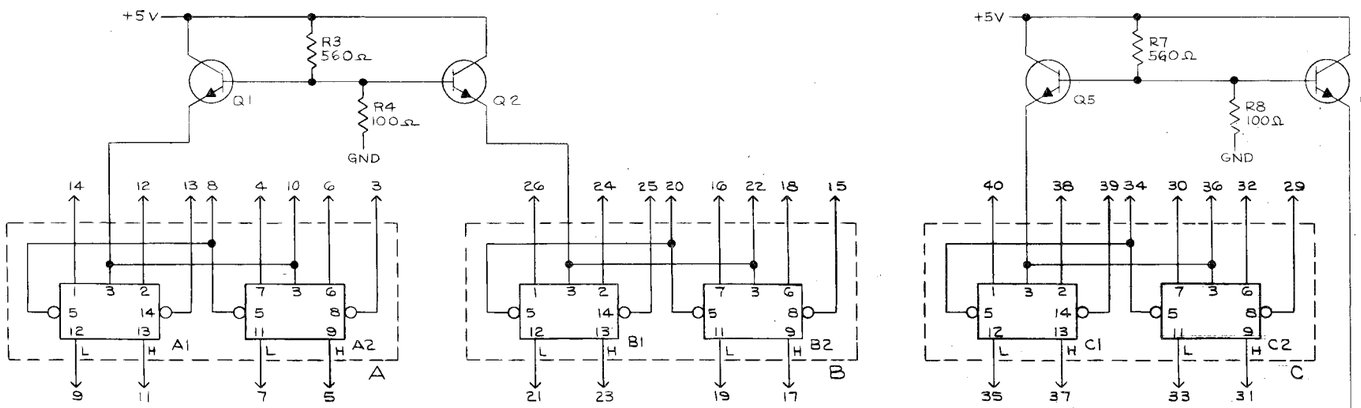


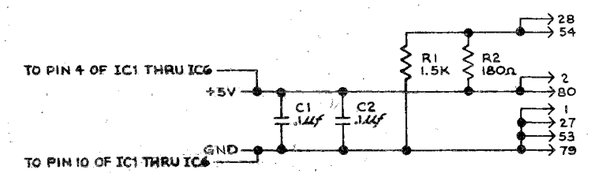


4. THE LOGIC SYMBOLS ON THIS SHEET CONFORM TO MIL STD 806.
5. DASH NUMBERS 001-004 ARE SUHL II OR EQUIV. (50 MEGAHERTZ, 6 NANO-SECOND GATE PROPAGATION DELAY)
   DASH NUMBERS 005-008 ARE SUHL I OR EQUIV. (35 MEGAHERTZ, 12 NANO-SECOND GATE PROPAGATION DELAY)
   DASH NUMBERS 009-012 ARE COMBINATIONS OF LOGIC ELEMENTS WITH DIFFERENT FREQUENCY, TEMPERATURE OR FAN-OUT CHARACTERISTICS. FAN-OUT IN THE FOLLOWING TABLE IS DEFINED IN TERMS OF SUHL II (APPROX 2 ma SINK CURRENT FROM +V) LOADS.

FAN-OUT	MILITARY -55°C TO +125°C	INDUSTRIAL 0°C TO +75°C
11	001, 005	
6	002, 006	
9		003, 007
5		004, 008

6. PRINTED WIRING BOARD SHALL MEET THE REQUIREMENTS OF 190-001050-001.
7. TEST PER SEL 95092A-1.
8. ⊳ INDICATES TOP SOLDER (◂ QTY 48) NOT REQUIRED WHEN PLATED THRU





APPLICABLE DOCUMENTS:
LIST OF MATERIAL - LM 160-900023

ITEM	DWG. OR PART NO.	DESCRIPTION

Systems Engineering Laboratories
6901 West Sunrise Blvd., Fort Lauderdale, Florida 33310

DR ERWOLFE	1-3-69	LOGIC & ASSEMBLY SECOND DUAL JK FLIP-FLOP COMMON CLOCK
CHK RKM	1-14-69	
ENGR	1-15-69	
PROJ E Williams	11-16-69	
APPD		
NEXT ASSY 14-100131-001	CODE IDENT NO. 20886	SIZE D — 160-900023 — REV. E

SHT 1

D 160-900023 E

160-900024 SECOND DUAL JK FLIP-FLOP
SEPARATE CLOCKS

DESCRIPTION

This circuit card contains six dual flip-flop circuits. The clock input is separate to each flip-flop in the package. The circuits have no direct reset. However, all flip-flops have separate set inputs.

Refer to A1 TYPICAL on the logic and assembly drawing in regard to the following discussion. The application of a ONE to IC2 along with a negative going trigger on IC pin 3 causes the flip-flop to set. The application of a ONE to IC pin 1 along with a negative going trigger on IC pin 3 causes the flip-flop to reset. IC pin 14 provides a direct set to the flip-flop. The application of a ZERO to IC pin 14 sets the flip-flop, causing pin 13 to go high.

SPECIFICATION (Element)

Speed:	Propagation delay times are typically 9 n sec turn-off and 11 n sec turn-on.
Noise Immunity:	±700 mv at 25°C and worse case fan-out; ±450 mv from -55°C to ±125°C and worse case fan-out; ±600 mv from 0°C to +75°C at worse case fan-out.
Logic Swing:	Logic ZERO is typically 0.26 volts; logic ONE is typically 3.3 volts at 25°C
Power:	Typically 55 milliwatts (per flip-flop)
I in (ma) each data input:	1.66 (160-900024-003, -004, -007, and -008)
I in (ma) clock input:	1.65 (160-900024-003, -004, -007, and -008)
I in (ma) set input:	2.8 (160-900024-003, -004, -007, and -008)
I out (ma) each output:	22.5 (160-900024-003 and -007) 12.5 (160-900024-004 and -008)

LIST of MATERIAL — Systems Engineering Laboratories — Fort Lauderdale, Florida 33310

		DATE
PREP	ERWOLFE	1-3-69
CHK	RKM	1-14-69
ENGR	[signature]	1-15-69
APPD		

USED ON: SYS-86

20886 | LM 160-900024 | E
CODE IDENT | SHEET 1 OF 3 SHEETS | REV

ITEM NOMENCLATURE: SECOND DUAL JK FLIP-FLOP SEPARATE CLOCKS

LTR	REVISION DESCRIPTION	DATE	APPD
A	69-431; ADDED ITEMS 6,8,20 & 21 DR 6-16-69 RKM	7/24/69	[illegible]
B	69-689; ITEM 1 PART NO. WAS 164-100078-001, ITEM 3 PART NO. WAS 168-100078-001 N.J.L. 8-29-69 RKM	9/2/69	[illegible]
C	69-824; UPDATED TO THE LATEST NUMBERING SYSTEM. MS. 10-16-69 RKM	12/7/69	[illegible]
D	69-1006; ITEM 8 QTY WAS 4 (Q1-4); ITEM 20 WAS 820Ω; QTY WAS 2; ITEM 21 WAS 150Ω; QTY WAS 2. RSK 1-8-70 RKM	1/9/70	[illegible]
E	70-1014 RB 9-22-70 RKM	9-24-70	[illegible]

RECORD OF REVISION STATUS OF EACH SHEET

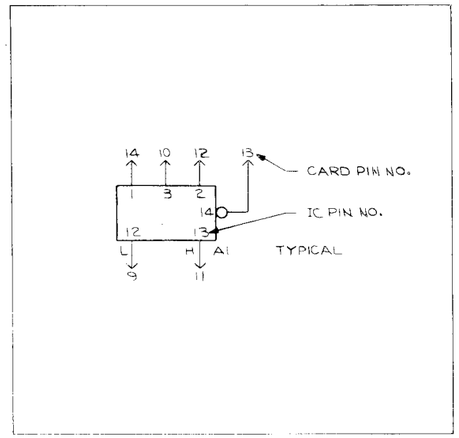
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42
E	E	E																																						

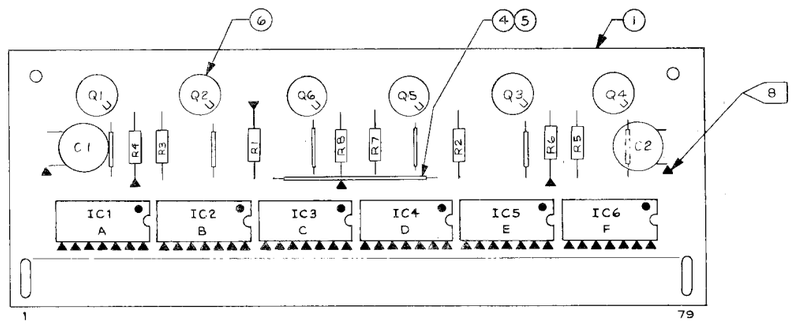
LIST of MATERIAL — Systems Engineering Laboratories — 20886 | LM 160-900024 | E
ITEM NOMENCLATURE: SECOND DUAL JK FLIP-FLOP SEPARATE CLOCKS | CODE IDENT | SHEET 2 OF SHEETS | REV

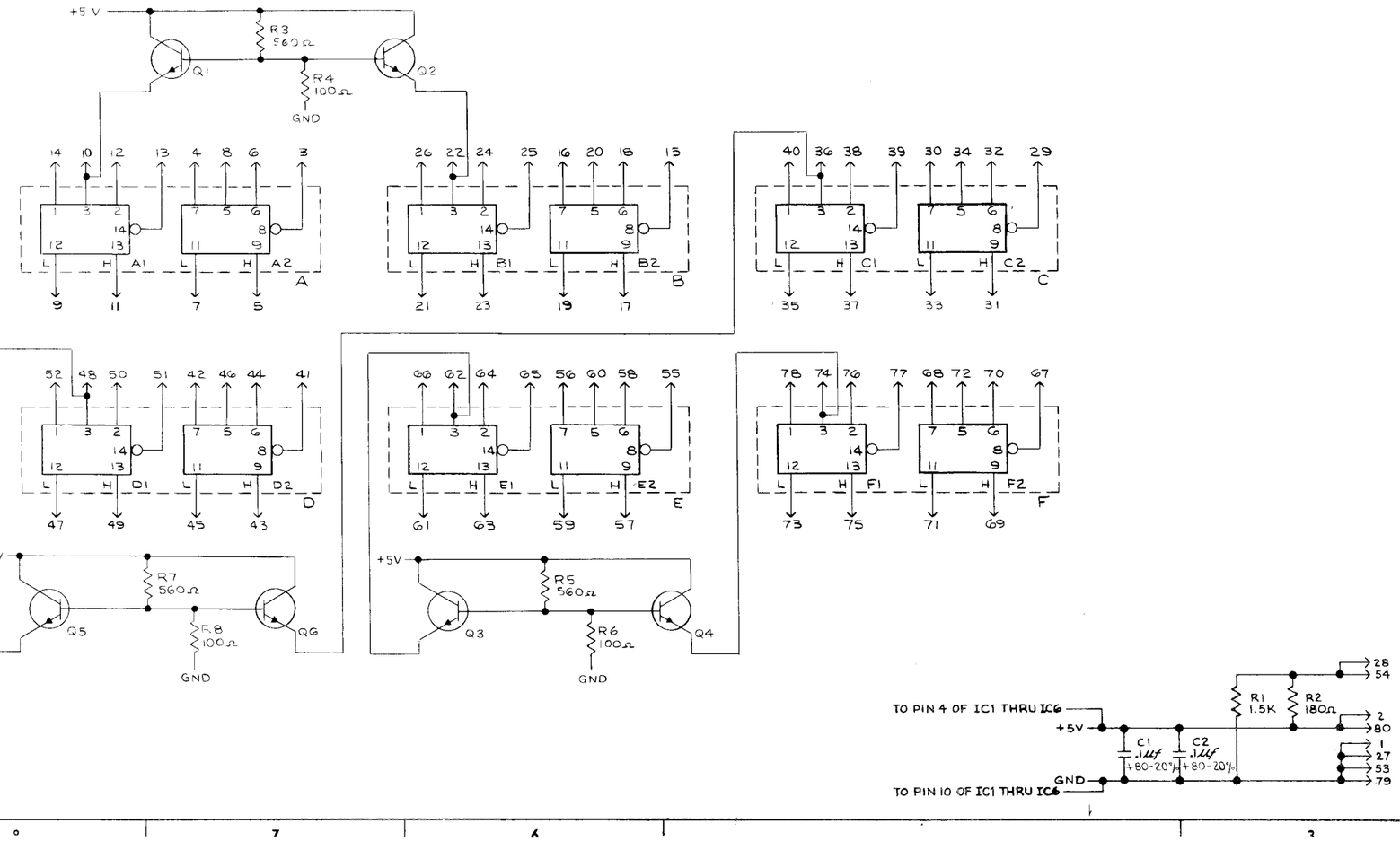
ITEM NO.	QTY REQ'D PER DASH NO. 005	004	003	002	001	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	REFERENCE DESIGNATION	REMARKS
1	1	1	1	1	1	164-100093-001	PRINTED CIRCUIT		FOR REV SEE 149-100001-000
2	REF	REF	REF	REF	REF	172-016323-001	DIMENSIONAL DWG		
3	REF	REF	REF	REF	REF	168-100093-001	DRILLING DWG		
4	AR	AR	AR	AR	AR	258-400001-004	WIRE		
5	AR	AR	AR	AR	AR	265-400001-004	SLEEVING		
6	4	4	4	4	4	110-010369-001	UNIPAD		
7									
8	6	6	6	6	6	250-112369-002	TRANSISTOR	Q1-6	
9	2	2	2	2	2	254-100700-002	CAP. 1μf +80-20% 10V CER	C1, 2	
10	X	X	X	X	6	252-115412-001	INTEGRATED CIRCUIT	IC1-6	
11	X	X	X	6	X	252-115412-101	↑	IC1-6	
12	X	X	6	X	X	252-115412-201		IC1-6	
13	X	6	X	X	X	252-115412-301		IC1-6	
14	6	X	X	X	X	252-115410-001		IC1-6	
15	X	X	X	X	X	252-115410-101		IC1-6	
16	X	X	X	X	X	252-115410-201	↓	IC1-6	
17	X	X	X	X	X	252-115410-301	INTEGRATED CIRCUIT	IC1-6	
18	1	1	1	1	1	253-100010-077	RES. 1.5K ± 5% 1/4 W CMPSN	R1	
19	1	1	1	1	1	253-100010-055	RES. 180Ω ± 5% 1/4 W CMPSN	R2	
20	3	3	3	3	3	253-100010-067	RES. 560Ω ± 5% 1/4 W CMPSN	R3,5,7	
21	3	3	3	3	3	253-100010-049	RES. 100Ω ± 5% 1/4 W CMPSN	R4,6,8	

LIST of MATERIAL — Systems Engineering Laboratories — 20886 | LM 160-900024 | E
ITEM NOMENCLATURE: SECOND DUAL JK FLIP-FLOP SEPARATE CLOCKS | CODE IDENT | SHEET 3 OF SHEETS | REV

ITEM NO.	QTY REQ'D PER DASH NO. 008	007	006	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	REFERENCE DESIGNATION	REMARKS
1	1	1	1	164-100093-001	PRINTED CIRCUIT		FOR REV SEE 149-100001-000
2	REF	REF	REF	172-016323-001	DIMENSIONAL DWG		
3	REF	REF	REF	168-100093-001	DRILLING DWG		
4	AR	AR	AR	258-400001-004	WIRE		
5	AR	AR	AR	265-400001-004	SLEEVING		
6	4	4	4	110-010369-001	UNIPAD		
7							
8	6	6	6	250-112369-002	TRANSISTOR	Q1-6	
9	2	2	2	254-100700-002	CAP. 1μf +80-20% 10V CER	C1, 2	
10	X	X	X	252-115412-001	INTEGRATED CIRCUIT	IC1-6	
11	X	X	X	252-115412-101	↑	IC1-6	
12	X	X	X	252-115412-201		IC1-6	
13	X	X	X	252-115412-301		IC1-6	
14	X	X	X	252-115410-001		IC1-6	
15	X	X	6	252-115410-101		IC1-6	
16	X	6	X	252-115410-201	↓	IC1-6	
17	6	X	X	252-115410-301	INTEGRATED CIRCUIT	IC1-6	
18	1	1	1	253-100010-077	RES. 1.5K ± 5% 1/4 W CMPSN	R1	
19	1	1	1	253-100010-055	RES. 180Ω ± 5% 1/4 W CMPSN	R2	
20	3	3	3	253-100010-067	RES. 560Ω ± 5% 1/4 W CMPSN	R3,5,7	
21	3	3	3	253-100010-049	RES. 100Ω ± 5% 1/4 W CMPSN	R4,6,8	







NOTES:
1. ALL ITEMS AS SPECIFIED IN LIST OF MATERIAL OR APPROVED EQUIVALENT.
2. UNLESS OTHERWISE SPECIFIED RESISTORS ARE ±5%.
3.
4. THE LOGIC SYMBOLS ON THIS SHEET CONFORM TO MIL STD 806.
5. DASH NUMBERS 001-004 ARE SUHL II OR EQUIV. (50 MEGAHERTZ, 6 NANO-SECOND GATE PROPAGATION DELAY)
   DASH NUMBERS 005-008 ARE SUHL I OR EQUIV. (35 MEGAHERTZ, 12 NANO-SECOND GATE PROPAGATION DELAY)
   DASH NUMBERS 009-012 ARE COMBINATIONS OF LOGIC ELEMENTS WITH DIFFERENT FREQUENCY, TEMPERATURE OR FAN-OUT CHARACTERISTICS. FAN-OUT IN THE FOLLOWING TABLE IS DEFINED IN TERMS OF SUHL II (APPROX 2 ma SINK CURRENT FROM +V) LOADS.

FAN-OUT	MILITARY -55°C TO +125°C	INDUSTRIAL 0°C TO +75°C
11	001, 005	
6	002, 006	
9		003, 007
5		004, 008

6. PRINTED WIRING BOARD SHALL MEET THE REQUIREMENTS OF 90-001050-001.
7. TEST PER SEL 450924.
8 > INDICATES TOP SOLDER (▶ QTY 48, NOT REQD WHEN PLATED THRU)

SIZE	160-900024		REV. E
REV.	DESCRIPTION	DATE	APPD
A	69-431; ADDED CLAMP CIRCUITS. DB 6-16-69 RKM	7/24/69	HPC
B	69-689; UPDATED TO LATEST REV. OF LM NJL 8-29-69 RKM	9/6/69	HPC
C	69-822, UPDATED TO LATEST NUMBERING SYSTEM MS 10-6-69 RKM	10/7/69	HPC
D	69-1006; ADDED CLAMP CIRCUIT; R466 WERE 150Ω; R365 WERE 820Ω. RSK 1-8-70 RKM	1/13/70	HPC
E	70-1014 RB 3-22-70 RKM	3-24-70	

APPLICABLE DOCUMENTS:
LIST OF MATERIAL - LM 160-900024

ITEM	DWG. OR PART NO.	DESCRIPTION

Systems Engineering Laboratories
6901 West Sunrise Blvd., Fort Lauderdale, Florida 33310

DRAWN	DR ERWOLFE	1-3-69
CHK	RKM	1-14-69
ENGR		1-15-69
PROJ		1-16-69
APPD		

LOGIC & ASSEMBLY
SECOND DUAL JK
FLIP-FLOP
SEPARATE CLOCKS

NEXT ASSY 141-100131-001 | CODE IDENT NO. 20886 | SIZE D | 160-900024 | REV. E

SHEET 1

160-900029 LOGIC AND ASSEMBLY SECOND HEX INVERTER

DESCRIPTION

This circuit card consists of 36 inverter circuits contained in six integrated circuit packages.

Each Circuit accepts a logical ONE and inverts it to a logical ZERO.

DATE 11/14/69 REV A

LIST of MATERIAL			Systems Engineering Laboratories	20886	LM160-900029	B
PREP	ERWOLFE	DATE 1-7-69	Fort Lauderdale, Florida 33310	CODE IDENT	SHEET 1 OF 3 SHEETS	REV
CHK	RKM	1-13-69		ITEM NOMENCLATURE: SECOND HEX INVERTER		
ENGR	[illegible]	1-15-69				
APPD	[illegible]	1/15/69	USED ON: SYS-86			

LTR	REVISION DESCRIPTION	DATE	APPD
A	69-817; UPDATED TO THE LATEST NUMBERING SYSTEM. MS 10-6-69 RKM	10/6/69	[illegible]
B	70-885; MP 9-3-70 RKM	9-7-70	AB

RECORD OF REVISION STATUS OF EACH SHEET

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42
A	A	A																																						
B	A	A																																						

LM160-900029

S.E.L. Form 365-1

LIST of MATERIAL	Systems Engineering Laboratories	20886	LM 160-900029	A
ITEM NOMENCLATURE: SECOND HEX INVERTER		CODE IDENT	SHEET 2 OF SHEETS	REV

ITEM NO.	QTY REQ'D PER DASH NO. 005	004	003	002	001	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	REFERENCE DESIGNATION	REMARKS
1	1	1	1	1	1	164-100078-001	PRINTED CIRCUIT		FOR REV SEE 149-100001-000
2	REF	REF	REF	REF	REF	172-016323-001	DIMENSIONAL DWG		
3	REF	REF	REF	REF	REF	168-100078-001	DRILLING DWG		
4	AR	AR	AR	AR	AR	258-400001-004	WIRE		
5	AR	AR	AR	AR	AR	265-400001-004	SLEEVING		
6									
7									
8									
9	2	2	2	2	2	254-100700-002	CAP. .1uf	C1,2	
10					6	252-115038-001	INTEGRATED CIRCUIT	IC1-6	
11				6		252-115038-101		IC1-6	
12			6			252-115038-201		IC1-6	
13		6				252-115038-301		IC1-6	
14	6					252-115037-001		IC1-6	
15						252-115037-101		IC1-6	
16						252-115037-201		IC1-6	
17						252-115037-301	INTEGRATED CIRCUIT	IC1-6	
18	1	1	1	1	1	253-100010-077	RES. 1.5K	R1	
19	1	1	1	1	1	253-100010-055	RES. 180Ω	R2	

LM160-900029

S.E.L. Form 365-2A

LIST of MATERIAL	Systems Engineering Laboratories	20886	LM 160-900029	A
ITEM NOMENCLATURE: SECOND HEX INVERTER		CODE IDENT	SHEET 3 OF SHEETS	REV

ITEM NO.	QTY REQ'D PER DASH NO. 008	007	006	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	REFERENCE DESIGNATION	REMARKS
1	1	1	1	164-100078-001	PRINTED CIRCUIT		FOR REV SEE 149-100001-000
2	REF	REF	REF	172-016323-001	DIMENSIONAL DWG		
3	REF	REF	REF	168-100078-001	DRILLING DWG		
4	AR	AR	AR	258-400001-004	WIRE		
5	AR	AR	AR	265-400001-004	SLEEVING		
6							
7							
8							
9	2	2	2	254-100700-002	CAP.	C1,2	
10				252-115038-001	INTEGRATED CIRCUIT	IC1-6	
11				252-115038-101		IC1-6	
12				252-115038-201		IC1-6	
13				252-115038-301		IC1-6	
14				252-115037-001		IC1-6	
15			6	252-115037-101		IC1-6	
16		6		252-115037-201		IC1-6	
17	6			252-115037-301	INTEGRATED CIRCUIT	IC1-6	
18	1	1	1	253-100010-077	RES. 1.5K	R1	
19	1	1	1	253-100010-055	RES. 180Ω	R2	

LM160-900029

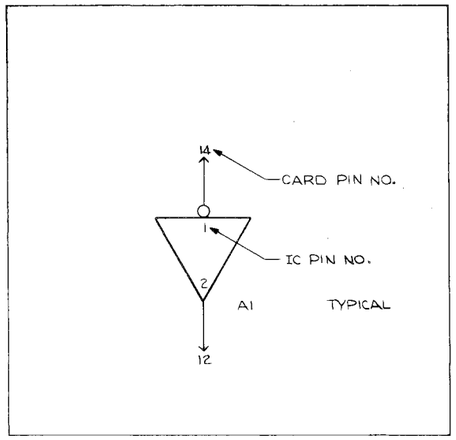
S.E.L. Form 365-2A

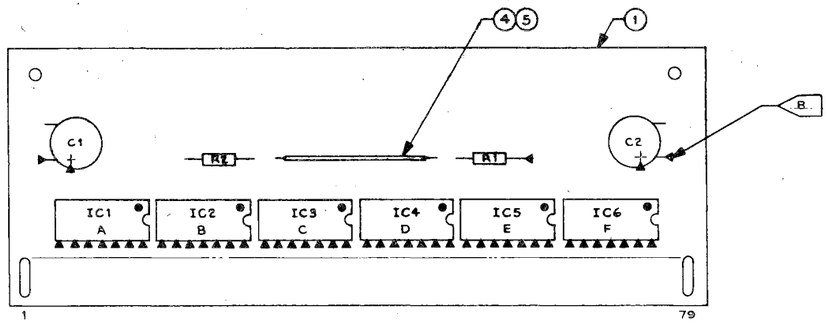
DATE 11/14/69 REV A

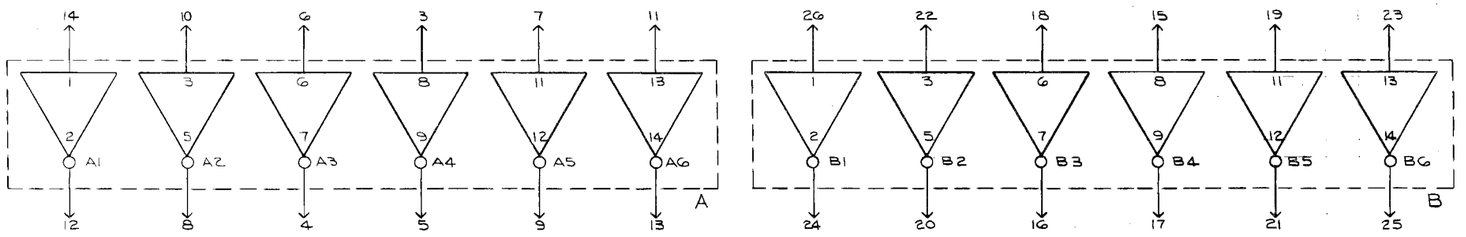
SIZE		REV.
D	160-900029	B

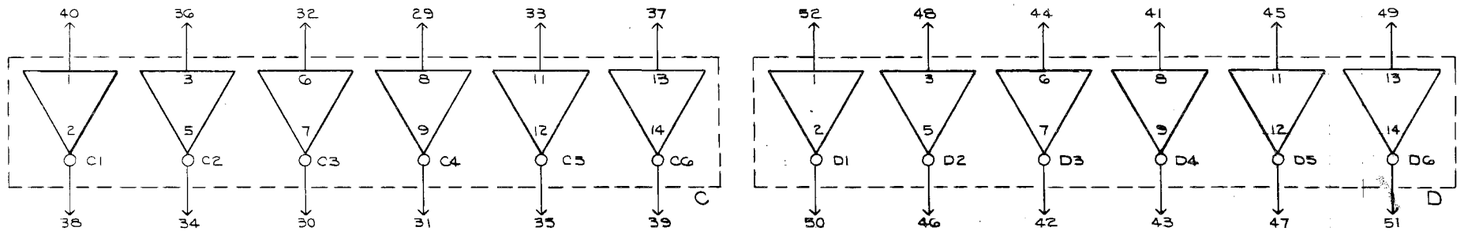
REV.	DESCRIPTION	DATE	APPD
A	69 817; UPDATED TO THE LATEST NUMBERING SYSTEM. MS 10-6-69 RKM		MBE 10/16/69
B	70-885 MP 9-3-70 RKM	9/7/70	

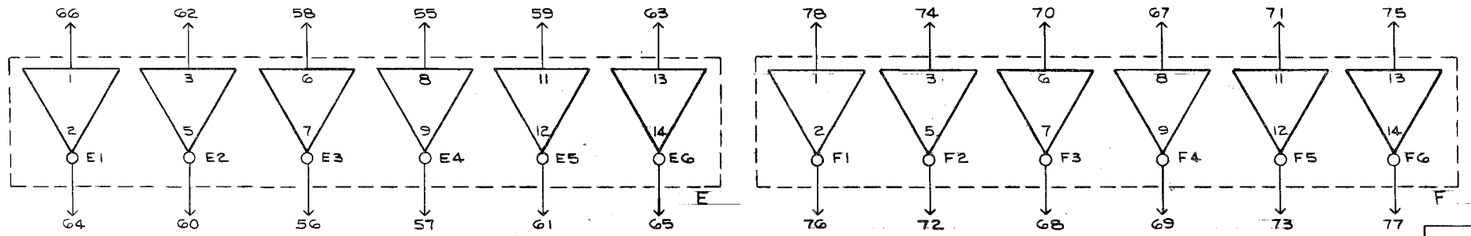
NOTES:
1. ALL ITEMS AS SPECIFIED IN LIST OF MATERIAL OR APPROVED EQUIVALENT.
2. UNLESS OTHERWISE SPECIFIED RESISTORS ARE ±5%
3.

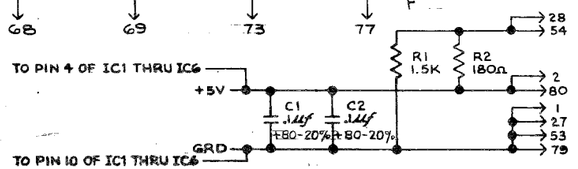












4. THE LOGIC SYMBOLS ON THIS SHEET CONFORM TO MIL STD 806.
5. DASH NUMBERS 001-004 ARE SUHL II OR EQUIV. (50 MEGAHERTZ, 6 NANO-SECOND GATE PROPAGATION DELAY)
   DASH NUMBERS 005-008 ARE SUHL I OR EQUIV. (35 MEGAHERTZ, 12 NANO-SECOND GATE PROPAGATION DELAY)
   DASH NUMBERS 009-012 ARE COMBINATIONS OF LOGIC ELEMENTS WITH DIFFERENT FREQUENCY, TEMPERATURE OR FAN-OUT CHARACTERISTICS. FAN-OUT IN THE FOLLOWING TABLE IS DEFINED IN TERMS OF SUHL II (APPROX 2 MA SINK CURRENT FROM +V) LOADS.

FAN-OUT	MILITARY -55°C TO +125°C	INDUSTRIAL 0°C TO +75°C
11	001,005	
6	002,006	
9		003,007
5		004,008

6. PRINTED WIRING BOARD SHALL MEET THE REQUIREMENTS OF 190-001050-001.
7. TEST PER SEL 95092A-1
8. INDICATES TOP SOLDER (▲ QTY 47) NOT REQD WHEN PLATED THRU

APPLICABLE DOCUMENTS:
LIST OF MATERIAL - LM 160-900029

ITEM	DWG. OR PART NO.	DESCRIPTION

Systems Engineering Laboratories
6901 West Sunrise Blvd., Fort Lauderdale, Florida 33310

DR ERWOLFE	1-7-69	LOGIC & ASSEMBLY SECOND HEX INVERTER
CHK RKM	1-13-69	
ENGR	1-15-69	
PROJ	1-16-69	
APPR	1/16/69	
NEXT ASSY 141-100131-001		CODE IDENT NO. 20886 / SIZE D / 160-900029 / REV. B

SHEET 1

160-900030 SCHEMATIC AND ASSEMBLY SECOND TRIPLE THREE "NAND"

DESCRIPTION

This circuit card consists of six integrated circuit packages.

A logical ONE input is required at the same time on all inputs in order to generate a logical ZERO output.

Any logical ZERO input will produce a logical ONE output.

DATE 11/14/69 REV A

LIST of MATERIAL			Systems Engineering Laboratories	20886	LM 160-900030	B
PREP	E.R WOLFE	DATE 12-30-68	Fort Lauderdale, Florida 33310	CODE IDENT	SHEET 1 OF 3 SHEETS	REV
CHK	RKM	1-14-69		ITEM NOMENCLATURE: SECOND TRIPLE THREE "NAND"		
ENGR	Norman A. Hughes	1-15-69				
APPD			USED ON: SYS-86			

LTR	REVISION DESCRIPTION	DATE	APPD
A	69-816, UPDATED TO LATEST NUMBERING SYSTEM MS 10-3-69 RKM	10/6/69	
B	70-886-JH 8-28-70 RKM	9-3-70	

LTR	REVISION DESCRIPTION	DATE	APPD

RECORD OF REVISION STATUS OF EACH SHEET

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42
A	A	A																																							
B	A	A																																							

LM 160-900030

S.E.L. Form 365-1

LIST of MATERIAL	Systems Engineering Laboratories	20886	LM 160-900030	A
ITEM NOMENCLATURE: SECOND TRIPLE THREE "NAND"		CODE IDENT	SHEET 2 OF SHEETS	REV

ITEM NO.	QTY REQ'D PER DASH NO. 005	004	003	002	001	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	REFERENCE DESIGNATION	REMARKS
1	1	1	1	1	1	164-100078-001	PRINTED CIRCUIT		FOR REV SEE 149-100001-000
2	REF	REF	REF	REF	REF	172-016323-001	DIMENSIONAL DWG		
3	REF	REF	REF	REF	REF	168-100078-001	DRILLING DWG		
4	AR	AR	AR	AR	AR	258-400001-004	WIRE		
5	AR	AR	AR	AR	AR	265-400001-004	SLEEVING		
6									
7									
8									
9	2	2	2	2	2	254-100700-002	CAP .1uf	C1,2	
10					6	252-115032-001	INTEGRATED CIRCUIT	IC1-6	
11				6		252-115032-101		IC1-6	
12			6			252-115032-201		IC1-6	
13		6				252-115032-301		IC1-6	
14	6					252-115019-001		IC1-6	
15						252-115019-101		IC1-6	
16						252-115019-201		IC1-6	
17						252-115019-301	INTEGRATED CIRCUIT	IC1-6	
18	1	1	1	1	1	253-100010-077	RES. 1.5K	R1	
19	1	1	1	1	1	253-100010-055	RES. 180Ω	R2	

LM 160-900030

S.E.L. Form 365-2A

LIST of MATERIAL	Systems Engineering Laboratories	20886	LM 160-900030	A
ITEM NOMENCLATURE: SECOND TRIPLE THREE "NAND"		CODE IDENT	SHEET 3 OF SHEETS	REV

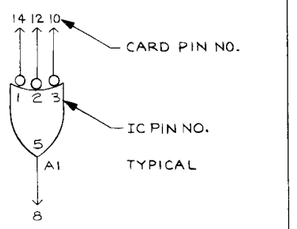
ITEM NO.	QTY REQ'D PER DASH NO. 008	007	006	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	REFERENCE DESIGNATION	REMARKS
1	1	1	1	164-100078-001	PRINTED CIRCUIT		FOR REV SEE 149-100001-000
2	REF	REF	REF	172-016323-001	DIMENSIONAL DWG		
3	REF	REF	REF	168-100078-001	DRILLING DWG		
4	AR	AR	AR	258-400001-004	WIRE		
5	AR	AR	AR	265-400001-004	SLEEVING		
6							
7							
8							
9	2	2	2	254-100700-002	CAP. .1uf	C1,2	
10				252-115032-001	INTEGRATED CIRCUIT	IC1-6	
11				252-115032-101		IC1-6	
12				252-115032-201		IC1-6	
13				252-115032-301		IC1-6	
14				252-115019-001		IC1-6	
15			6	252-115019-101		IC1-6	
16		6		252-115019-201		IC1-6	
17	6			252-115019-301	INTEGRATED CIRCUIT	IC1-6	
18	1	1	1	253-100010-077	RES. 1.5K	R1	
19	1	1	1	253-100010-055	RES. 180Ω	R2	

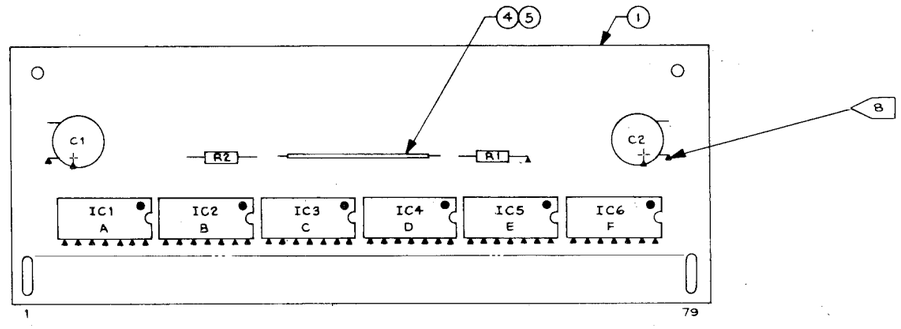
LM 160-900030

S.E.L. Form 365-2A

ERN 011-2
DATE 11/14/69 REV. 1

NOTE
THE LOGIC ELEMENTS ON THIS CARD CAN BE USED TO IMPLEMENT EITHER "AND" OR "OR" FUNCTIONS. THE "AND" IMPLEMENTATION IS SHOWN FOR ALL CIRCUITS WITH AN EXAMPLE OF THE "OR" IMPLEMENTATION SHOWN DIRECTLY BELOW.





NOTES:
1. ALL ITEMS AS SPECIFIED IN LIST OF MATERIAL OR APPROVED EQUIVALENT.
2. UNLESS OTHERWISE SPECIFIED RESISTORS ARE ±5%.
3.

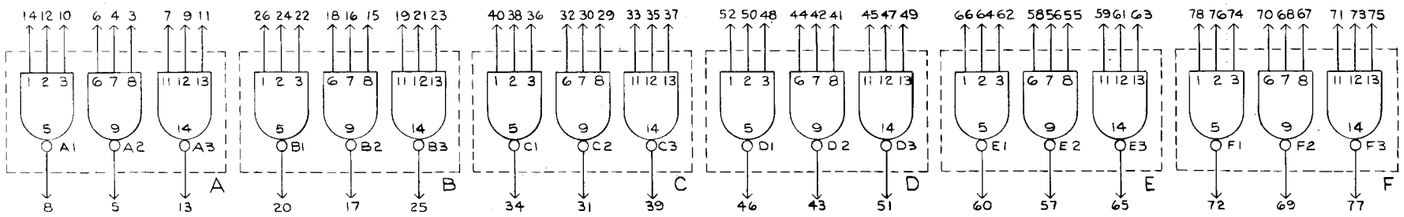
SIZE		REV.
D	160-900030	B

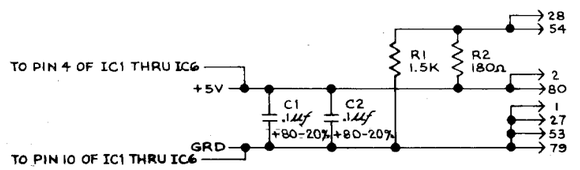
REV.	DESCRIPTION	DATE	APPD
A	69-816; UPDATED TO LATEST NUMBERING SYSTEM. MS 10-3-69 RKM	10/6/69	
B	70-886 JH 8-28-70 RKM	9/3/70	

4. THE LOGIC SYMBOLS ON THIS SHEET CONFORM TO MIL STD 806.
5. DASH NUMBERS 001-004 ARE SUHL II OR EQUIV. (50 MEGAHERTZ, 6 NANO-SECOND GATE PROPAGATION DELAY)
   DASH NUMBERS 005-008 ARE SUHL I OR EQUIV. (35 MEGAHERTZ, 12 NANO-SECOND GATE PROPAGATION DELAY)
   DASH NUMBERS 009-012 ARE COMBINATIONS OF LOGIC ELEMENTS WITH DIFFERENT FREQUENCY, TEMPERATURE OR FAN-OUT CHARACTERISTICS. FAN-OUT IN THE FOLLOWING TABLE IS DEFINED IN TERMS OF SUHL II (APPROX 2 ma SINK CURRENT FROM +V) LOADS.

FAN-OUT	MILITARY -55°C TO +125°C	INDUSTRIAL 0°C TO +75°C
11	001, 005	
6	002, 006	
9		003, 007
5		004, 008

6. PRINTED WIRING BOARD SHALL MEET THE REQUIREMENTS OF 190-001050-001
7. TEST PER SEL 95092A-1
8. > INDICATES TOP SOLDER (QTY 47), NOT REQUIRED .IN PLATED THRU.





APPLICABLE DOCUMENTS:
LIST OF MATERIAL - LM 160-900030

ITEM	DWG. OR PART NO.	DESCRIPTION

Systems Engineering Laboratories
6901 West Sunrise Blvd., Fort Lauderdale, Florida 33310

DR E R WOLFE	12-30-68	LOGIC & ASSEMBLY SECOND TRIPLE THREE "NAND"
CHK RKM	1-14-69	
ENGR	1-15-69	
PROJ E Wilson	1-16-69	
APPD	1/16/69	
NEXT ASSY 141-100131-001		

CODE IDENT NO.	SIZE		REV.
20886	D	160-900030	B

SHEET 1

D 160-900030 B

160-900043 LOGIC & ASSEMBLY SECOND MIXED LOGIC #7

DESCRIPTION

This circuit card contains five quad 2-input NAND/NOR gates and two/four input NAND/NOR gates. Each gate consists of a two/four input AND gate followed by an inverting amplifier. Each of the gates functions as a NAND element in positive logic (as a NOR element in a negative logic). These types are useful where multiple inverting functions are needed or where multiple drivers are needed such as in clock distribution systems.

LIST of MATERIAL			Systems Engineering Laboratories	20886	LM 160-900043	A
PREP	ERWOLFE	DATE 1-14-69	Fort Lauderdale, Florida 33310	CODE IDENT	SHEET 1 OF 2 SHEETS	REV
CHK	RKM	1-15-69		ITEM NOMENCLATURE: SECOND MIXED LOGIC #7		
ENGR	Thomas A. Hughes					
APPD			USED ON:			

LTR	REVISION DESCRIPTION	DATE	APPD	LTR	REVISION DESCRIPTION	DATE	APPD
A	71-385; UPDATED TO LATEST REV OF S&A. EL 6-10-71 RKM	6-10-71					

RECORD OF REVISION STATUS OF EACH SHEET

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42
—	—																																							
A	—																																							

LM160-900043

S.E.L. Form 365-1

LIST of MATERIAL	Systems Engineering Laboratories	20886	LM 160-900043	—
ITEM NOMENCLATURE: SECOND MIXED LOGIC #7		CODE IDENT	SHEET 2 OF 2 SHEETS	REV

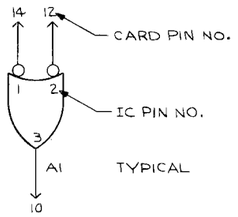
ITEM NO.	QTY REQ'D PER DASH NO. 004	003	002	001	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	REFERENCE DESIGNATION	REMARKS
1	1	1	1	1	164-100078-001	PRINTED CIRCUIT		FOR REV SEE 149-100001-000
2	REF	REF	REF	REF	172-016323-001	DIMENSIONAL DWG		
3	REF	REF	REF	REF	168-100078-001	DRILLING DWG		
4	AR	AR	AR	AR	AWG 24	WIRE SOLID COPPER TINNED		
5	AR	AR	AR	AR	AWG 24	SLEEVING TEFLON THINWALL		
6								
7								
8								
9	2	2	2	2	UK-10-104	CAP. .1μf +80-20% 10V CERAMIC	C1, 2	CRL
10				5	SG220	INTEGRATED CIRCUIT	IC1-5	SYLVANIA
11				1	SG240		IC6	
12			5		SG 221		IC1-5	
13			1		SG 241		IC6	
14		5			SG222		IC1-5	
15		1			SG 242		IC6	
16	5				SG223		IC1-5	
17	1				SG 243	INTEGRATED CIRCUIT	IC6	SYLVANIA
18	1	1	1	1	RC07GF152J	RES. 1.5K±5% 1/4W COMP	R1	AB
19	1	1	1	1	RC07GF181J	RES. 180Ω±5% 1/4W COMP	R2	AB

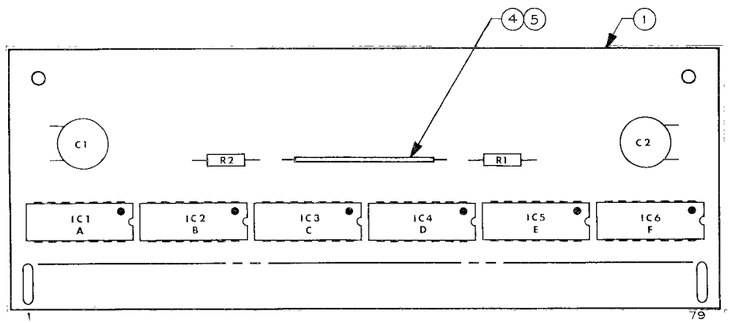
LM160-900043

S.E.L. Form 365-2A

NOTE

THE LOGIC ELEMENTS ON THIS CARD CAN BE USED TO IMPLEMENT EITHER "AND" OR "OR" FUNCTIONS. THE "AND" IMPLEMENTATION IS SHOWN FOR ALL CIRCUITS WITH AN EXAMPLE OF THE "OR" IMPLEMENTATION SHOWN DIRECTLY BELOW.

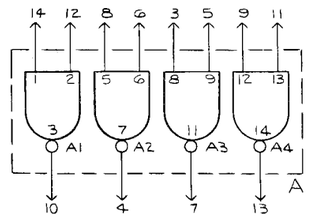


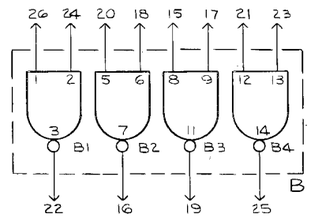


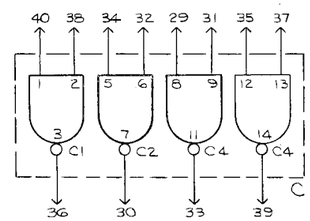
NOTES:
1. ALL ITEMS AS SPECIFIED IN LIST OF MATERIAL OR APPROVED EQUIVALENT.
2. UNLESS OTHERWISE SPECIFIED RESISTORS ARE ±5%, 1/4 W.
3. FOR COMPLETE DOCUMENTATION USE PC ASSY MFG PROCESS CONTROL SPEC 149-100008-000 FOR CERTAIN CHANGES IN PROCESSES & COMPONENTS THAT MAY HAVE BEEN REFLECTED TO THE PART DESCRIBED.
4. THE LOGIC SYMBOLS ON THIS SHEET CONFORM TO MIL STD 806.
5. DASH NUMBERS 001-004 ARE SUHL II OR EQUIV. (50 MEGAHERTZ, 6 NANOSECOND GATE PROPAGATION DELAY)
   DASH NUMBERS 005-008 ARE SUHL I OR EQUIV. (35 MEGAHERTZ, 12 NANOSECOND GATE PROPAGATION DELAY)
   DASH NUMBERS 009-012 ARE COMBINATIONS OF LOGIC ELEMENTS WITH DIFFERENT FREQUENCY, TEMPERATURE OR FAN-OUT CHARACTERISTICS. FAN-OUT IN THE FOLLOWING TABLE IS DEFINED IN TERMS OF SUHL II (APPROX 2 ma SINK CURRENT FROM +V) LOADS.

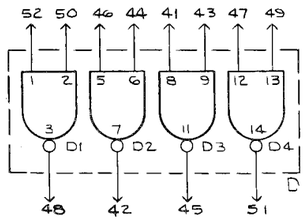
FAN-OUT	MILITARY -55°C TO +125°C	INDUSTRIAL 0°C TO +75°C
11	001	
6	002	
9		003
5		004

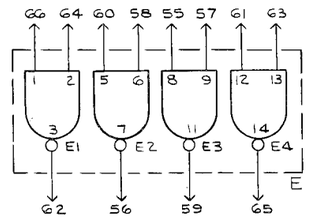
SIZE	160-900043		REV.
D			A
REV.	DESCRIPTION	DATE	APPD
A	71-3886, JWG 6-7-71 RKM	6-7-71	

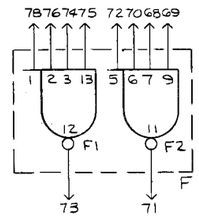


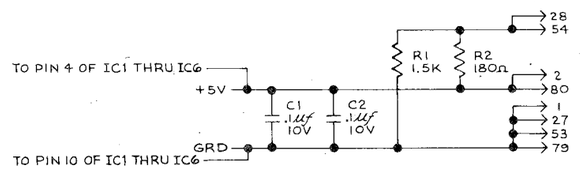












APPLICABLE DOCUMENTS:
LIST OF MATERIAL - LM 160-900043

ITEM	DWG. OR PART NO.	DESCRIPTION

Systems Engineering Laboratories
6901 West Sunrise Blvd., Fort Lauderdale, Florida 33310

DRER WOLFE	1-14-69	LOGIC & ASSEMBLY SECOND MIXED LOGIC #7
CHK RKM	1-15-69	
ENGR	1-15-69	
PROJ	1-16-69	
APPD	1/16/69	
NEXT ASSY		

CODE IDENT NO.	SIZE		REV.
20886	D	160-900043	A

SHEET 1

SECTION VII

DRAWINGS

7-1 INTRODUCTION

7-2 This section contains all of the system logic and wiring diagrams. The logic circuits for each of the functional sections are contained in drawing sets and are identified by an engineering drawing number. These sets are arranged in numerical order, as are the individual sheets within the sets.

7-3 Refer to Volume 1 of this manual for the detailed discussion of the circuits contained on the drawings in this section. Also, refer to Section VI of this manual for schematic and assembly drawings of the individual circuit cards.

7-4 CONVENTIONS

7-5 LOGIC SYMBOLS

7-6 Logic symbols are used to represent the circuits contained on the circuit cards. Figure 7-1 illustrates the symbols used for this purpose.

7-7 The circles on the inputs and outputs of the SEL 806B logic symbols denote a zero volt (0V) condition as the true state of the circuit. For example, an inverter may have a circle on either the input or output depending on how it is being used. The buffer shown in figure 7-1 is a noninverting stage, and as such does not have a circle on either the input or output. However, some buffers do invert and therefore are treated like inverters. To distinguish between a buffer and an inverter, the symbols are labeled either BUF or INV.

7-8 The standard discrete component logic symbols are also shown in figure 7-1. This portion of the figure also provides some pertinent information concerning the logic circuits described.

7-9 LOGIC LEVELS

7-10 The logic levels used by the micrologic circuits in the system are either 0 volts for a logic ZERO or +3.6 volts for a logic ONE. In the discussion of the detailed theory, these levels are referred to as ZERO and ONE, or Low and High, respectively.

7-11 The logic levels used by the standard discrete logic circuits are either 0 volts for a logic ZERO or -6 volts for a logic ONE. In the discussion of the detailed theory, these levels are referred to as ZERO and ONE, or Low and High, respectively.

7-12 WIRE ADDRESSING

7-13 Wire addressing on the logic diagrams permits tracing signals between drawings or individual sheets of a single drawing. When the destination or source of a signal is shown on another sheet of a set of drawings, there are three possible addressing schemes used on Systems Engineering Laboratories drawings.

7-14 The three addressing schemes are presented in the following list.

a. $\overline{3}$ - STXFER

b. $\overline{3}$ - 13B24

c. 26-14A3-ABCH

7-15 Example (a) indicates that the signal could be located in the upper, right-hand quadrant of sheet 3. The mnemonic designator, in some cases is obvious; however, it is not essential that the reader understand what the mnemonic stands for, since it is provided as an aid in tracing signals from one sheet to another.

7-16 Example (b) is similar to example (a) except that, in place of the mnemonic designator, the circuit location is used. In this example, the circuit used is located in card location 13 of row B of the card tray or swing plane and the signal wire is connected to pin 24 of the circuit card receptacle.

7-17 The wire address provided in example (c) is explained in the following discussion.

a. The first two digits of the legend are the last two digits of the drawing number.

1. In some instances, this number may have three digits for the drawing number.

2. When the wire address references a circuit within the same set of logic drawings, these digits are omitted.

b. The second part of the legend gives the sheet number of the drawing set and the vertical and horizontal co-ordinates (zone) of the signal source. For the example - Sheet 14, vertical co-ordinate A, horizontal co-ordinate 3.

c. The third part of the legend is the mnemonic assigned to that signal with an H or L indicating that the signal level logically implemented is either High or Low. For the example - mnemonic ABC, logical signal level High.

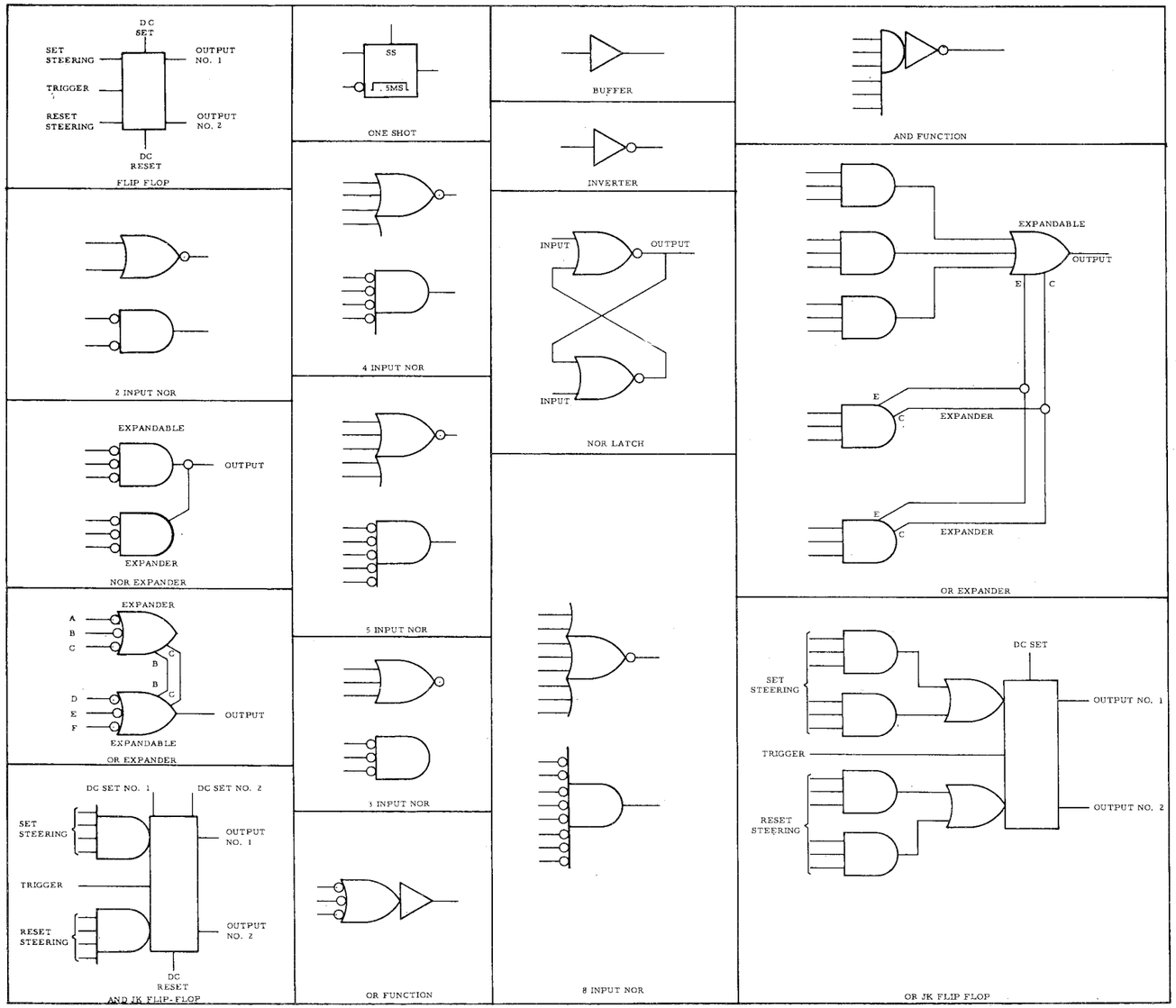
7-18 SIGNAL LINE CALLOUTS

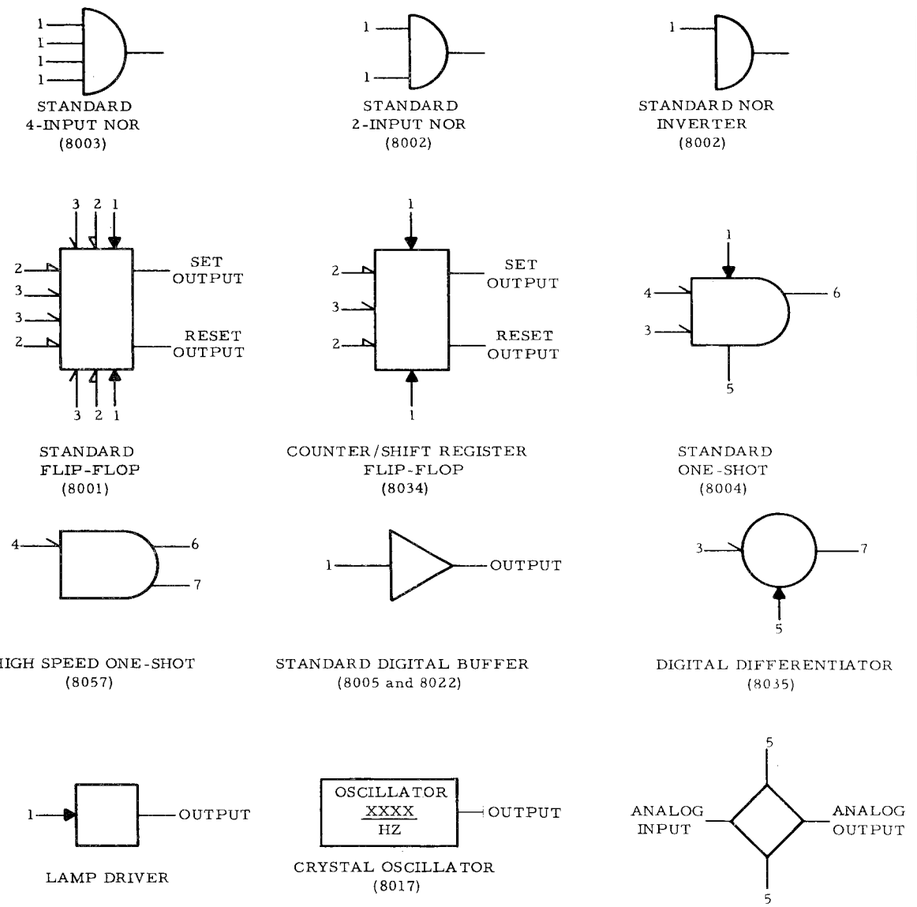
7-19 Most primary signals on the logic diagrams are labeled with the name of the signal being generated. A reference to the voltage level of the signal is indicated in one of the following manners:

a. + or - sign before or after the signal name indicating a high or a low.

b. H or L indicating high or low before or after the signal name.

c. A bar over the signal name ($\overline{\text{XFER}}$) indicates a low and the absence of a bar indicates a high.





NOTES:

1. STANDARD DC INPUT
2. LEVEL INPUT (ZERO VOLTS ENABLES AC COUPLED INPUT)
3. AC COUPLED INPUT (CIRCUIT RESPONDS TO POSITIVE-GOING SIGNALS)
4. AC COUPLED INPUT (CIRCUIT RESPONDS TO NEGATIVE-GOING SIGNALS)
5. CONTROL INPUT
6. POSITIVE-GOING OUTPUT
7. NEGATIVE-GOING OUTPUT
8. ALL OTHER CIRCUITS REPRESENTED BY BLOCKS

Figure 7-1. SYSTEMS 806B and Standardard Discrete Component Logic Symbols

ERN 123-1
DATE 9-17-70 REV – 1

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

PRIORITY INTERRUPT

CABLE DRIVERS

P.I. LOGIC

ABANDON CALL (AUTO DIAL OPTION)
RING INDICATOR
DATA SET RDY, CLR. TO SEND, CARRIER DET, MOD. DET.
INPUT READY

OUTPUT READY

CABLE TERM'S

UNIT DECODE LOGIC

CABLE TERM'S

I/O SYNC LOGIC

CABLE DRIVERS

CABLE (0) TERM'S

BTC1 LOGIC (OPTION)

CABLE (0) DRIVERS

AUTO DIAL LOGIC (OPTION)

CEU. CONTROL REGISTER

TEU TEST LOGIC

TRANSMIT TIMING & CONTROL

CLOCK

P/S CONV.

DATA

GATES

CLOCK (OPTION)

16 BIT BUFFER REG

PARITY REG. (OPTION)

CLOCK OUT (CLOCK OPTION)

CABLE TERM'S

PARITY CHK. (OPTION)

16 BIT BUFFER REG

GATES

PARITY REG. (OPTION)

CABLE DRIVERS

S/P CONV.

DATA

SYNC. LOGIC

RCV. TIMING & CONTROL

CLOCK

CONVERTERS

LEVEL

AUTO DIAL CONNECTOR (OPTION)

CRQ	CALL REQUEST
NB1	BCD DIGIT (1)
NB2	BCD DIGIT (2)
NB4	BCD DIGIT (4)
NB8	BCD DIGIT (8)
DPR	DIGIT PRESENT
PND	PRESENT NEXT DIGIT
PWI	POWER INDICATION
DSS	DATA SET IN DATA MODE
DLO	DATA LINE OCCUPIED
ACR	ABANDON CALL
GD.	GROUND

MODEM CONNECTOR

BA	TRANS. DATA
BB	RECEIVED DATA
CA	REQ. TO SEND.
CB	CLEAR TO SEND
CC	DATA SET READY
CD	DATA TERM. READY
CE	RING INDICATOR
CF	DATA CARRIER DET.
CG	MODULATION DET.
DB	TRANS. TIMING ELEM.
DD	REC. TIMING ELEM.
DA (0)	TRANS. TIM. ELEM. (OPTION)
DC (0)	REC. TIM. ELEM. (OPTION)
SIG. GD.	GROUND
PROT. GD.	GROUND

138-100046-000

9-2-70 AT

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON

BASIC DIMENSION	DECIMAL PLACES .XX	.XXX
UNDER 12	± .02	± .005
12 TO 24	± .03	± .010
OVER 24	± .06	± .015
ANGLES ± 0° 30'		

MATERIAL:
FINISH:

	772926
NEXT ASSY	USED ON
APPLICATION	

DRAWN	RENE GONZALEZ	DATE 6-30-70
CHECKED		9/17/70
ENGR		9/17/70
PROT ENGR		9/17/70
APPROVED		9/17/70
APPROVED		

Systems Engineering Laboratories
Fort Lauderdale, Florida

BLOCK DIAGRAM
SYNC. DATA
MODEM INTERFACE

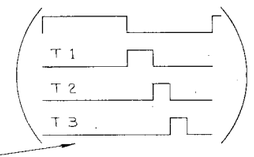
SIZE	CODE IDENT NO.	DWG NO.
D	20886	138-100046-000

SCALE | SHEET 1 OF 1

S.E.L. FORM 063D

ERN 123-1
DATE 9-17-70 REV - 1

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

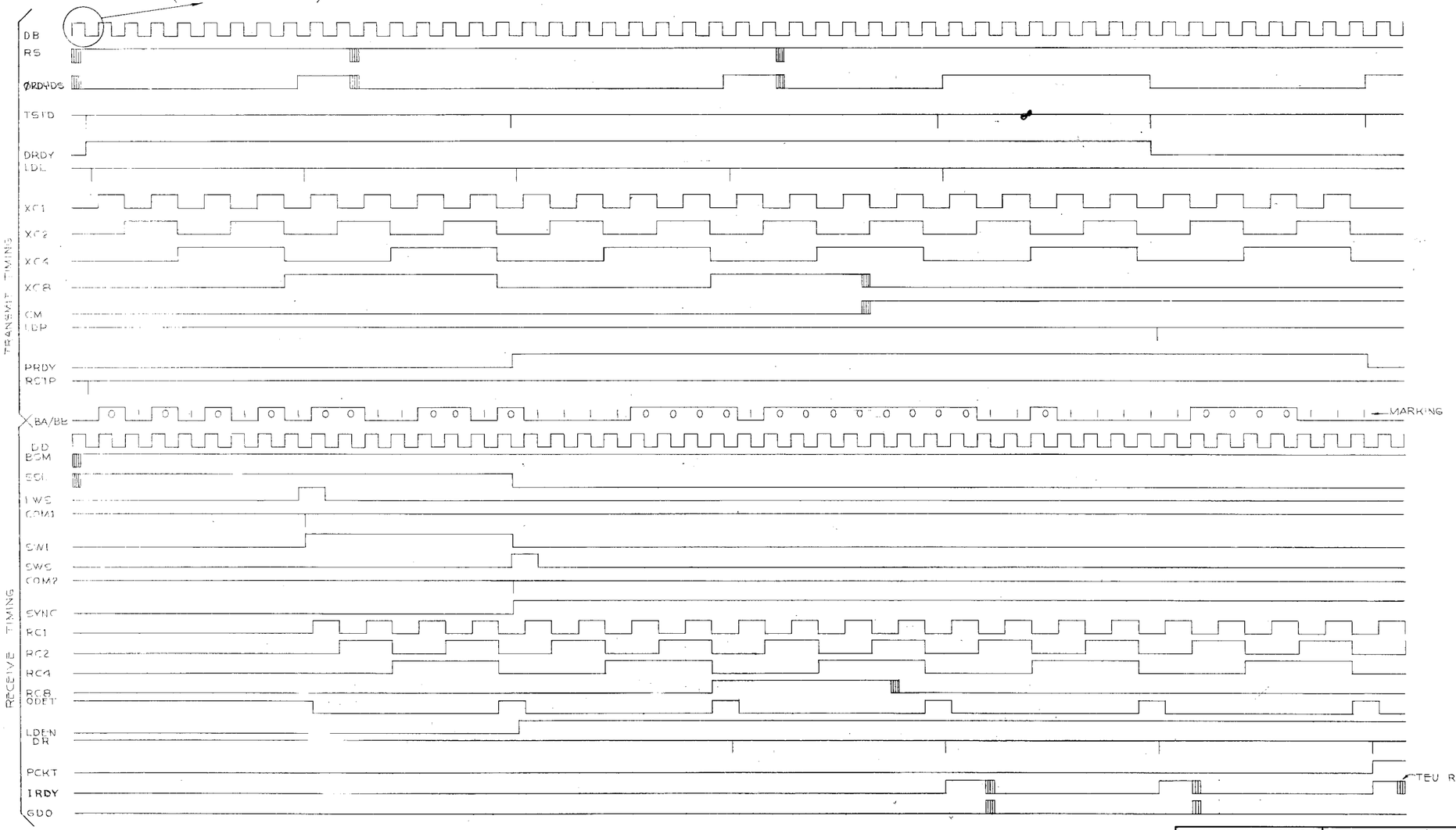


BLOCK FORMAT

SYNC 1	SYNC 2	DATA 1	DATA 2	DATA 3	PARITY

DATA FORMAT (OCTAL)

SYNC 1 - 125 DATA 1 - 360 PARITY ODD -207
SYNC 2 - 062 DATA 2 - 200 OR
DATA 3 - 157 PARITY EVEN-170



NOTES.

1. SYNC & 1ST (2) TWO DATA WORDS LOADED AS 2 CHARACTERS PER WORD, LAST WORD AS ONE CHARACTER PER WORD. SET TO TRANSMIT ODD PARITY.

9-2-70 AB
9-21-70 AB

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON		
BASIC DIMENSION	DECIMAL PLACES .XX	.XXX
UNDER 12	± .02	± .005
12 TO 24	± .03	± .010
OVER 24	± .06	± .015
ANGLES ± 0° 30'		

MATERIAL:
FINISH:

NEXT ASSY	USED ON
	772926
APPLICATION	

		DATE
DRAWN	RENE GONZALEZ	7-1-70
CHECKED		9/17/70
ENGR		9/17/70
PROJ ENGR		9/17/70
APPROVED		9/17/70
APPROVED		

Systems Engineering Laboratories
Fort Lauderdale, Florida

TIMING DIAGRAM SYNC. DATA MODEM INTERFACE UNIT

SIZE	CODE IDENT NO.	DWG NO.
D	20886	147-100010-000
SCALE		SHEET 1 OF 1

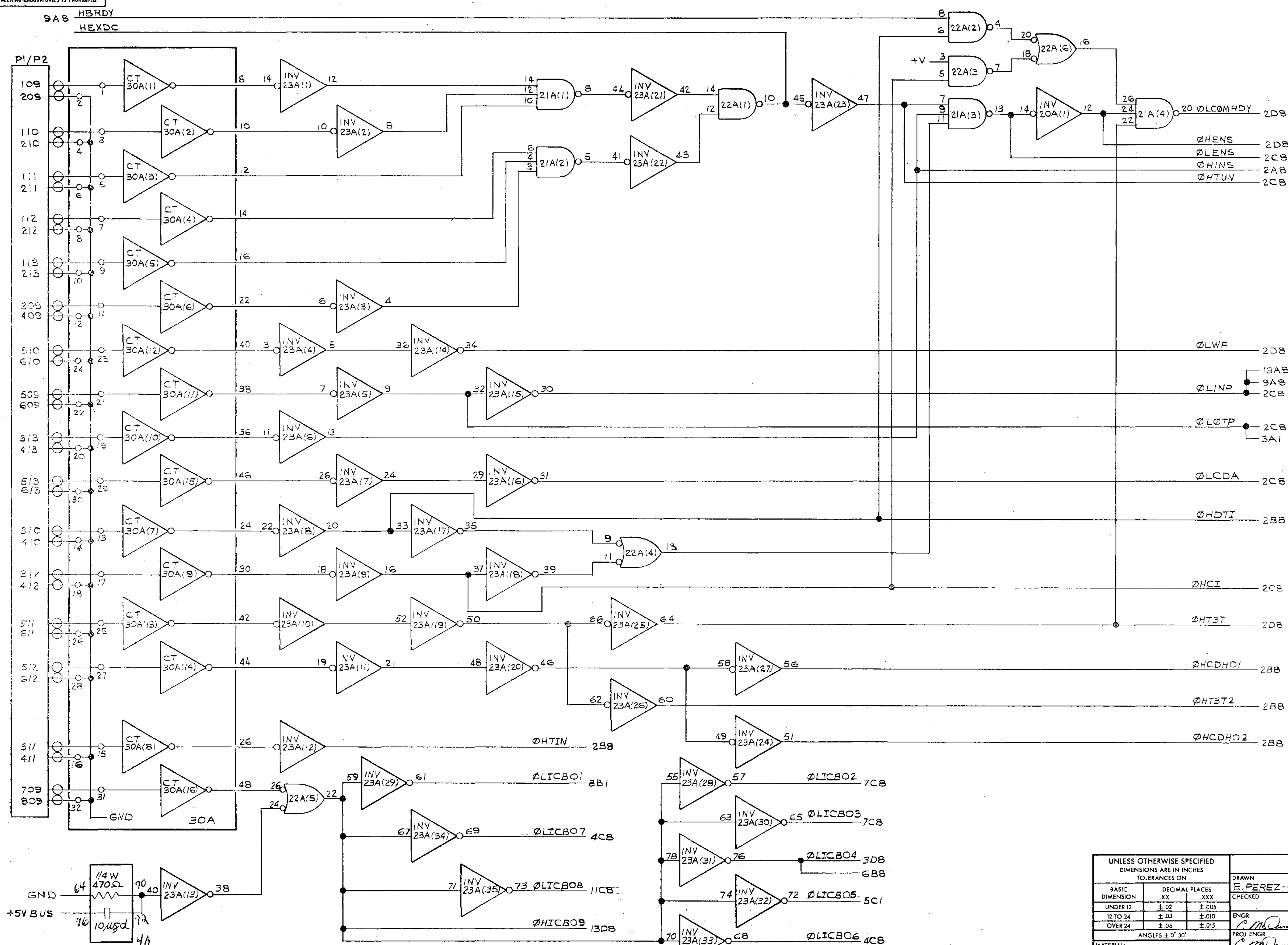
147-100010-000

S.E.L. FORM 063D

THE USE, DUPLICATION OR DISCLOSURE OF THIS DATA (IN WHOLE OR IN PART) FOR MANUFACTURE OR PROCUREMENT WITHOUT THE WRITTEN PERMISSION OF SYSTEMS ENGINEERING LABORATORIES IS PROHIBITED.

ERN 174-1 DATE 8-4-71 REV -

ZONE	LTR	DESCRIPTION	DATE	APPROVED



NOTES:
1. FOR CARD LOCATION SEE DWG 141-100312.

554102	704004
PROJ ASSY	SPCL. SYS.
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON

BASIC DIMENSION	DECIMAL PLACES .XX	.XXX
UNDER 12	± .02	± .005
12 TO 24	± .03	± .010
OVER 24	± .06	± .015

ANGLES ± 0° 30'

MATERIAL:

FINISH:

DRAWN E. PEREZ-CUBAS DATE 6-1-71
CHECKED
ENGR C. McDonald 8/3/71
PROJ ENGR C. McDonald 8/3/71
APPROVED
APPROVED

Systems Engineering Laboratories
Fort Lauderdale, Florida

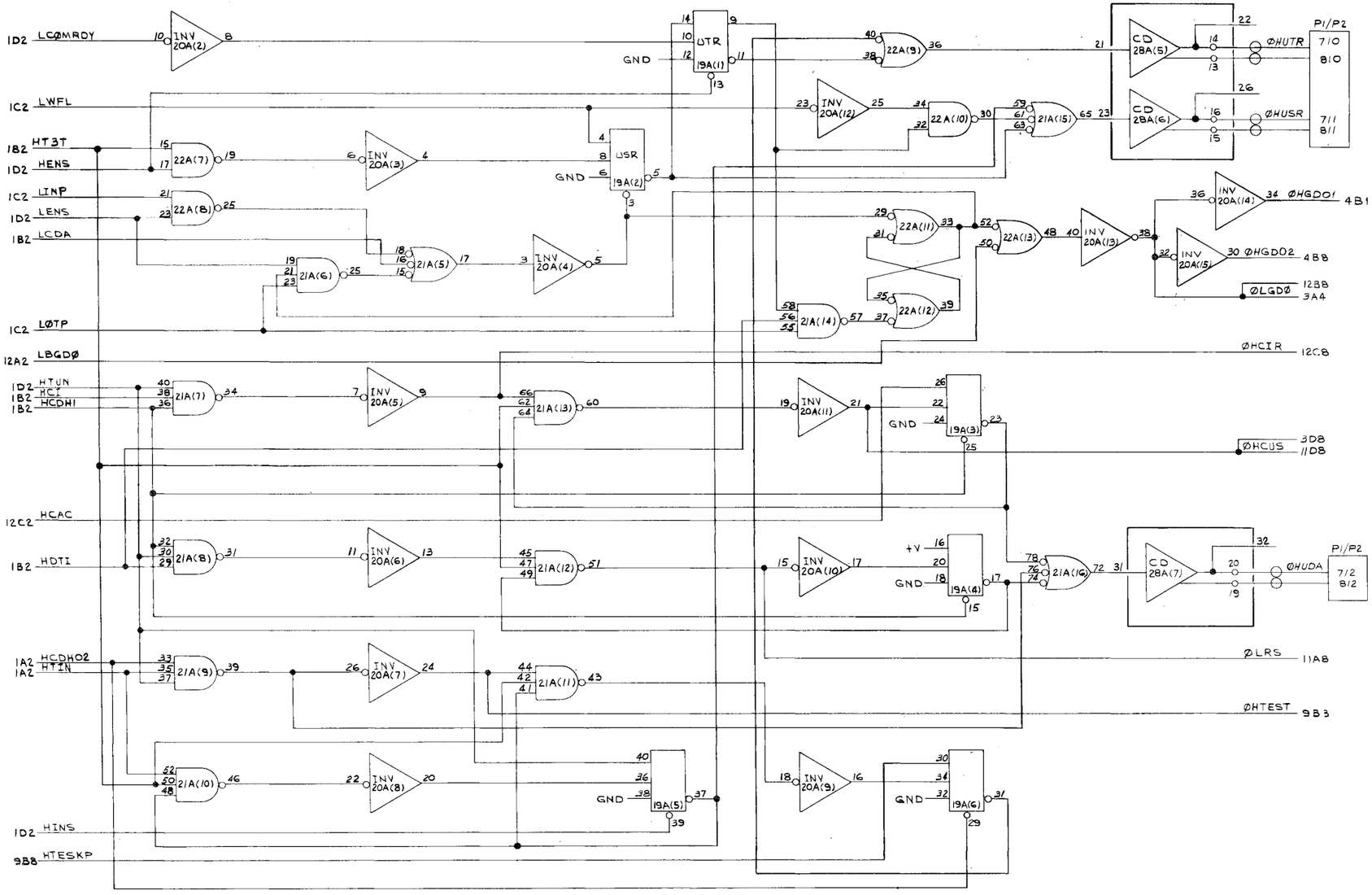
LOGIC DIAGRAM
UNIT DECODE LOGIC

SIZE D CODE IDENT NO. 20886 DWG NO. 130-100659-000
SCALE REV LTR SHEET 1 OF 15

ECN DATE	REV
	1

REVISIONS

ZONE	LTR	DESCRIPTION	DATE	APPROVED



UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON		
BASIC DIMENSION	DECIMAL PLACES .XX	.XXX
UNDER 12	± .02	± .005
12 TO 24	± .03	± .010
OVER 24	± .06	± .015
ANGLES ± 0° 30'		

MATERIAL:

FINISH:

554102	704004
PROJ	SPCL SYS
APPLICATION	

DRAWN	E. PEREZ-CUBAS	DATE 6-3-71
CHECKED		
ENGR		8/2/71
PROJ ENGR		8/2/71
APPROVED		
APPROVED		

Systems Engineering Laboratories
Fort Lauderdale, Florida

LOGIC DIAGRAM
I/O SYNC LOGIC

SIZE	CODE IDENT NO.	DWG NO.
D	20886	130-100659-000

SCALE

SHEET 2

ERN	DATE	REV
		1

REVISIONS

ZONE	LTR	DESCRIPTION	DATE	APPROVED

11A8 LCM
5D3 LRCLK
5D1 HRT3
7C5 HDBOG
2C2 HCUS
1A5 LICBO4
5D2 HRT2
5D2 HRT2
5D6 HRB1
5D6 LRB1
5D6 HRB2
5D6 LRB2
5D5 HRB3
5D5 LRB3
5D5 HRB4
5D5 LRB4
5D4 HRB5
D4 LRB5
D4 HRB6
5D4 LRB6
5D4 HRB7
5D4 LRH7
5D3 HRB8
5D3 LRB8
2C2 LGDØ
9C1 LRRP
1C2 LØTP
12A2 LBTCRS

5A(2) 5A(3) 5A(4) 9A(24) 14A(18) 5A(5) 9A(23) RC1 RC2 RC4 RC8 14A(13) 12A(8) 12A(9) 12A(10) 12A(11) 14A(14) 9A(19) 9A(20) SSL 14A(17) 14A(16) COM1 9A(25) SWE 6A(10) 9A(27) 5A(6) 9A(22) 9A(21) 3A(3) 3A(4) O.S. 7A(4) ØDET 28A(16) CD P5 103 203 ØLSNG 588 ØLBSM 588 5A(9) SYNC 17A(9) LDEL 6A(9) COM2 3A(1) 3A(2) 5A(16) 5A(17) SLIP WIRING ØHLD1R 4D5 ØHLD2R 4D8 3A(9) ØHC PAR 5C8 ØHIRDY 11D6 12B8 ØLIRDYS 9A8 5A(11) 12A(12) DR GND 5A(24) 5A(23) 17A(4) 17A(10) 5A(22) 5A(21) 9A(33) 17A(8) 3A(8) 3A(7) 3A(6) 3A(5) 9A(29) 9A(30) 9A(31) 9A(32) 5A(7) 5A(8) 9A(28) 9A(26) FWS SWS +V GND

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON		
BASIC DIMENSION	DECIMAL PLACES .XX	.XXX
UNDER 12	± .02	± .005
12 TO 24	± .03	± .010
OVER 24	± .06	± .015
ANGLES ± 0° 30'		

MATERIAL:
FINISH:

554102	704004
PROJ	SPCL.SYS.
APPLICATION	

DRAWN	Schmandrat	5-4-71
CHECKED		
ENGR		5/3/71
PROJ ENGR		5/3/71
APPROVED		
APPROVED		

Systems Engineering Laboratories
Fort Lauderdale, Florida

LOGIC DIAGRAM
RECEIVE TIMING
&
CONTROL LOGIC

SIZE	CODE IDENT NO.	DWG NO.
D	20886	130-100659-000

SCALE | SHEET 3

130-100659-000

ZONE	LTR	REVISIONS DESCRIPTION	DATE	APPROVED
		ERN DATE REV 1		

HRB1 5C8 5C1 HRB8 | HRB2 5C1 5C1 HRB7 | HRB3 5C1 5C1 HRB6 | HRB4 5C1 5C1 HRB5 | HRB5 5C1 5C1 HRB4 | HRB6 5C1 5C1 HRB3 | HRB7 5C1 5C1 HRB2 | HRB8 5C1 5C8 HRB1

LTCB06 1A5 HLD1R - 3B1

SUPPLEMENTAL WIRING

1-020 \ -010 -020 \ -010

LTCB07 1A6 HLD2R - 3B1

+V

17 19 20 4 18 14 24 30 22 40 21 15 16 11 26 29 23 39 55 57 60 42 58 52 64 68 62 78 59 41 56 51 66 67 61 77

8A

8 6 10 12 24 32 36 38 5 13 7 9 33 31 35 37 46 44 48 50 72 70 74 76 45 43 47 49 71 69 73 75

2C2 HGD01
2C2 HGD02

23 21 | 38 40 | 32 34 | 31 29 | 37 35 | 50 52 | 44 46 | 43 41 | 49 47 | 64 66 | 58 60 | 57 55 | 63 61 | 76 78 | 70 72 | 69 67

10A(8) | 10A(9) | 10A(10) | 10A(11) | 10A(12) | 10A(13) | 10A(14) | 10A(15) | 10A(16) | 10A(17) | 10A(18) | 10A(19) | 10A(20) | 10A(21) | 10A(22) | 10A(23)

25 | 36 | 30 | 33 | 39 | 48 | 42 | 45 | 51 | 62 | 56 | 59 | 65 | 74 | 68 | 71

14 | 10 | 6 | 3 | 7 | 11 | 26 | 22 | 18 | 15 | 19 | 23 | 40 | 36 | 32 | 29

9A(1) | 9A(2) | 9A(3) | 9A(4) | 9A(5) | 9A(6) | 9A(7) | 9A(8) | 9A(9) | 9A(10) | 9A(11) | 9A(12) | 9A(13) | 9A(14) | 9A(15) | 9A(16)

12 | 8 | 4 | 5 | 9 | 13 | 24 | 20 | 16 | 17 | 21 | 25 | 38 | 34 | 30 | 31

3 7 13 15 21 23 31 33 39 41 47 49 57 61 63 65

CABLE DRIVER 27A

6 ØHI00 7D8 | 10 ØHI01 7D7 | 14 ØHI02 7D7 | 18 ØHI03 7D6 | 22 ØHI04 7D6 | 26 ØHI05 7D5 | 32 ØHI06 7D5 | 36 ØHI07 7D5 | 40 ØHI08 7D4 | 44 ØHI09 7D4 | 48 ØHI10 7D3 | 52 ØHI11 7D3 | 58 ØHI12 7D2 | 62 ØHI13 7D2 | 64 ØHI14 7D1 | 68 ØHI15 7D1

130-100659-000

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON		
BASIC DIMENSION	DECIMAL PLACES .XX	.XXX
UNDER 12	± .02	± .005
12 TO 24	± .03	± .010
OVER 24	± .06	± .015
ANGLES ± 0° 30'		

MATERIAL:

FINISH:

554102	704004
PROJ	SPCL.SYS
APPLICATION	

DRAWN Schmandrak DATE 5-4-71
CHECKED
ENGR
PROJ ENGR
APPROVED
APPROVED

Systems Engineering Laboratories
Fort Lauderdale, Florida

LOGIC DIAGRAM INPUT BUFFER

SIZE	CODE IDENT NO.	DWG NO.
D	20886	130-100659-000

SCALE SHEET 4

ERN	DATE	REV
		1

REVISIONS

ZONE	LTR	DESCRIPTION	DATE	APPROVED

3A7 ØHRB1
4D8 3A7 ØLRB1
3D8 ØLRCLK
3A7 ØHRB2
4D8 3A7 ØLRB2
3A7 ØHRB3
4D7 3A7 ØLRB3
3A7 ØHRB4
3AG 4D7 ØLRB4
3AG ØHRB5
3AG 4D7 ØLRB5
3AG ØHRB6
3AG 4D7 ØLRB6
3A5 ØHRB7
4D7 3A5 ØLRB7
3A5 ØHRB8
4D8 3A5 ØLRB8
3C8 ØHRI2
3B1 ØHRT3
3D8

6A(8) 6A(7) 6A(6) 6A(5) 6A(4) 6A(3) 6A(2) 6A(1)

9A(18) 5A(1) IREC 26

BIPØLAR RECEIVER

RCV 24A(8) GND E-15 E-16 BD 106 206

RCV 24A(7) GND E-13 E-14 DD 105 205

TØ MØDEM PG

9A(17) IRCLK 24

O.S. 7A(1) O.S. 7A(2) O.S 7A(3)

HCF
LICBO5 1A5

001 ØR 002 ØPTIØN

1A(1) 1A(2) 1A(3) 1A(4) 1A(5) 1A(6) 1A(7) 1A(8)

ØDD EVEN ØDD EVEN 4A

9A(34) 3A(12) LSNG LBSM HPARE +V 3B1 3B8 1A8

HCPAR 3B2

1A 54

3A(10) 3A(11)

9A(35) 9A(36)

7C6 HDBO5

14A(15)

9D5 ØLPCKT

NOTES: 1. FØR CURRENT MØDE ØPTIØN (-200) SEE SHEET 14.

554102	704004
PROJ	SPCL. SYS
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON

BASIC DIMENSION	DECIMAL PLACES .XX	.XXX
UNDER 12	± .02	± .005
12 TO 24	± .03	± .010
OVER 24	± .06	± .015

ANGLES ± 0° 30'

MATERIAL:

FINISH:

	DRAWN	DATE
	Schmandrat	5-4-71
CHECKED		
ENGR		8/3/71
PROJ ENGR		8/3/71
APPROVED		
APPROVED		

Systems Engineering Laboratories
Fort Lauderdale, Florida

LOGIC DIAGRAM
S/P CONVERTER
&
PARITY REGISTER

SIZE	CODE IDENT NO.	DWG NO.
D	20886	130-100659-000

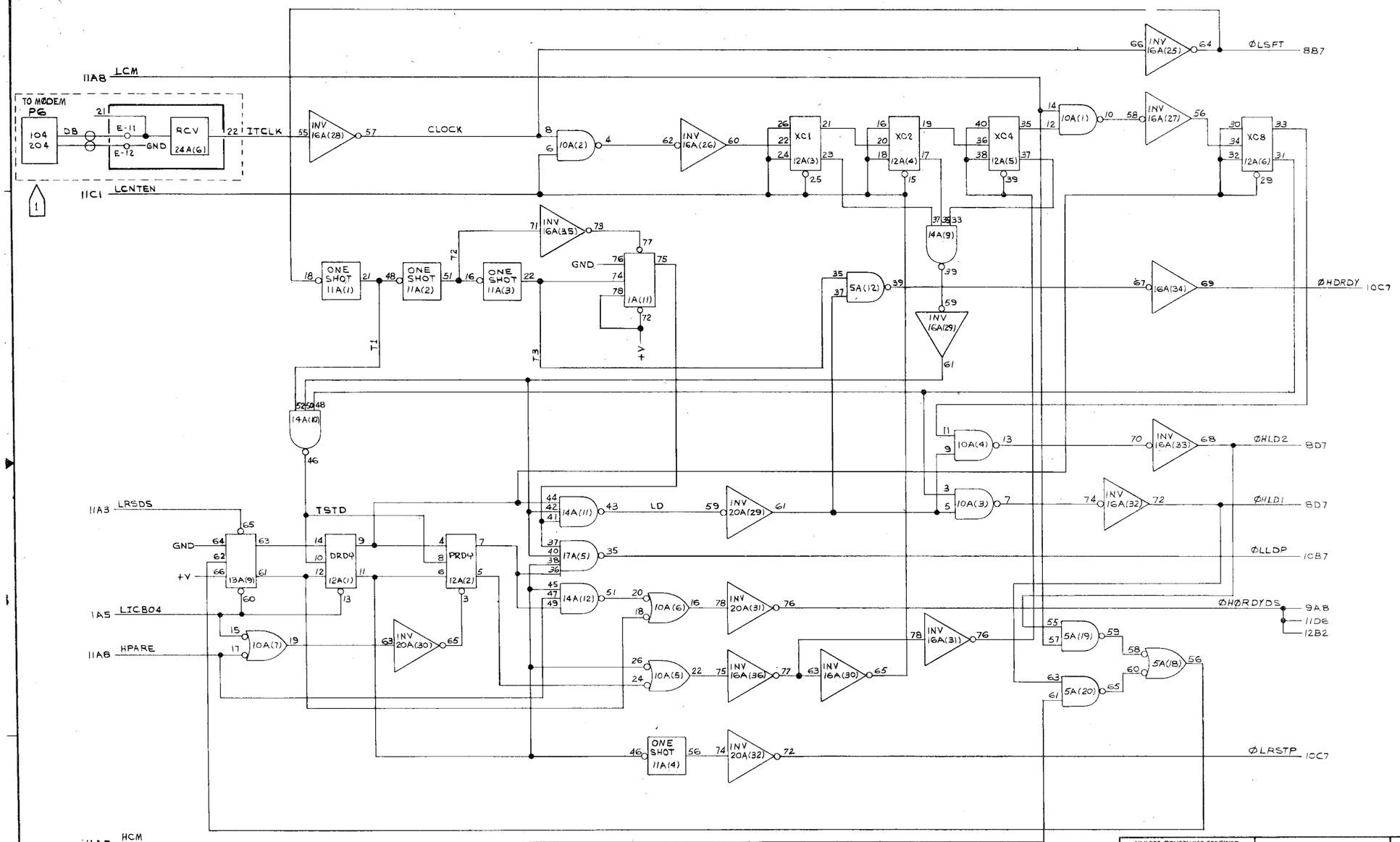
SCALE | SHEET 5

130-100659-000

ERN	DATE	REV
		1

REVISIONS

ZONE	LTR	DESCRIPTION	DATE	APPROVED



1. FOR CURRENT MODE OPTION (-200) SEE SHEET 14

NOTES:

554102	704004
PROJ	SPCL. SYS.
APPLICATION	

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ON

BASIC DIMENSION	DECIMAL PLACES .XX	.XXX
UNDER 12	± .02	± .005
12 TO 24	± .03	± .010
OVER 24	± .06	± .015
ANGLES ± 0° 30'		

MATERIAL:

FINISH:

		DATE
DRAWN	Schmandrak	5-4-71
CHECKED		
ENGR		8/3/71
PROJ ENGR		8/3/71
APPROVED		
APPROVED		

Systems Engineering Laboratories
Fort Lauderdale, Florida

LOGIC DIAGRAM TRANSMIT TIMING & CONTROL LOGIC

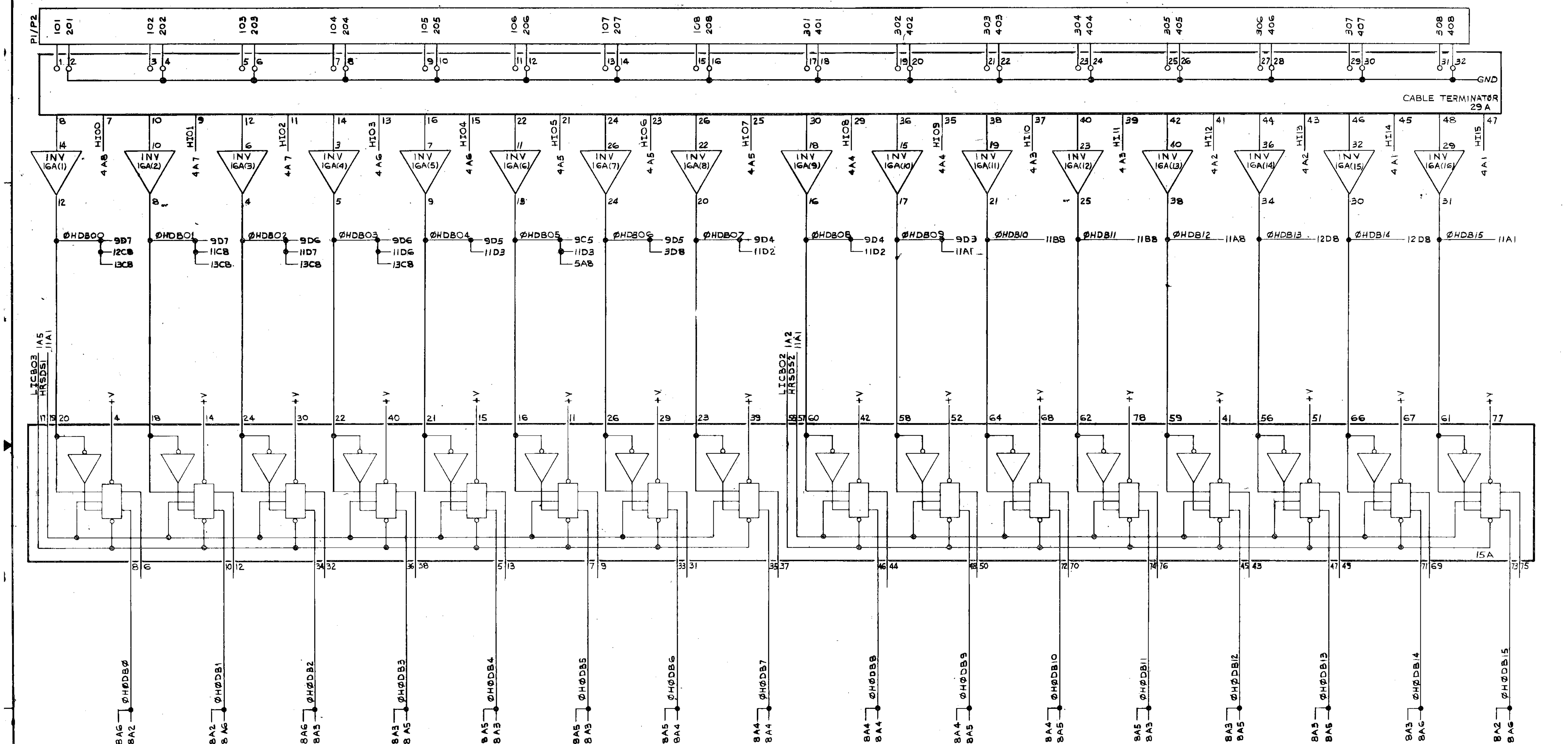
SIZE	CODE IDENT NO.	DWG NO.
D	20886	130-100659-000

SCALE

SHEET 6

130-100659-000-1

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED



UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON		
BASIC DIMENSION	DECIMAL PLACES .XX	.XXX
UNDER 12	±.02	±.005
12 TO 24	±.03	±.010
OVER 24	±.06	±.015
ANGLES ± 0° 30'		

MATERIAL:

FINISH:

554102	704004
PROJ	SPCL SYS
APPLICATION	

DRAWN Schmandrok DATE 5-4-71
CHECKED
ENGR C McD[illegible] 8/3/7
PROJ ENGR C McD[illegible] 8/3/71
APPROVED
APPROVED

Systems Engineering Laboratories
Fort Lauderdale, Florida

LOGIC DIAGRAM
OUTPUT BUFFER

SIZE D | CODE IDENT NO. 20886 | DWG NO. 130-100659-000
SCALE | SHEET 7

130-100659-000

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

ECN DATE REV 1

SUPPLEMENTAL WIRING

HØDB0 7A8 7A1 HØDB15 -020 -010
HØDB8 7A4 7A5 HØDB7
HØDB1 7A7 7A1 HØDB14
HØDB9 7A4 7A5 HØDB6
HØDB2 7A7 7A2 HØDB13
HØDB10 7A3 7A5 HØDB5
HØDB3 7A6 7A2 HØDB12
HØDB11 7A3 7A6 HØDB4
HØDB4 7A6 7A3 HØDB11
HØDB12 7A2 7A6 HØDB3
HØDB5 7A5 7A3 HØDB10
HØDB13 7A2 7A7 HØDB2
HØDB6 7A5 7A4 HØDB9
HØDB14 7A1 7A7 HØDB1
HØDB7 7A5 7A4 HØDB8
HØDB15 7A1 7A8 HØDB0 -020 -010

HXB1H HXB1L HXB2H HXB2L HXB3H HXB3L HXB4H HXB4L HXB5H HXB5L HXB6H HXB6L HXB7H HXB7L HXB8H HXB8L

HLD2 6B2
HLD1 6B2

18A(2) 18A(3) 18A(4) 18A(5) 18A(6) 18A(7) 18A(8) 18A(9) 18A(10) 18A(11) 18A 18A(13) 18A(14) 18A(15) 18A(16) 18A(17)

LSPB1 10A6
LSPB2 10A5
LSPB3 10A5
LSPB4 10A4
LSPB5 10A4
LSPB6 10A4
LSPB7 10A3
LSPB8 10A3

14A(1) 14A(2) 14A(3) 14A(4) 14A(5) 14A(6) 14A(7) 14A(8)

16A(17) 16A(18) 16A(19) 16A(20) 16A(21) 16A(22) 16A(23) 16A(24)

10D6 ØHPB1
10D6 ØHPB2
10D5 ØHPB3
10D5 ØHPB4
10D4 ØHPB5
10D4 ØHPB6
10D3 ØHPB7
10D3 ØHPB8

19A(11) 13A(1) 13A(2) 13A(3) 13A(4) 13A(5) 13A(6) 13A(7) 13A(8)

GND
+V
LICBO1 1A6
LSFT 6D1

IXMIT+

TO MODEM PG

DRIV 25A(2) E-4 E-3 GND BA 102 202

1 FOR CURRENT MODE OPTION (-200) SEE SHEET 14

NOTES:

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON		
BASIC DIMENSION	DECIMAL PLACES .XX	.XXX
UNDER 12	± .02	± .005
12 TO 24	± .03	± .010
OVER 24	± .06	± .015
ANGLES ± 0° 30'		

MATERIAL:
FINISH:

554102	704004
PROJ	SPCL SYS
APPLICATION	

DRAWN	Schmandrak	5-4-71
CHECKED		
ENGR	C. McOmber	8/4/71
PRODUCTION	C. McOmber	8/4/71
APPROVED		
APPROVED		

Systems Engineering Laboratories
Fort Lauderdale, Florida

LOGIC DIAGRAM
DATA GATES
&
P/S CONVERTER

SIZE	CODE IDENT NO.	DWG NO.
D	20886	130-100659-000

SCALE SHEET 8

130-100659-000

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

ERN DATE REV 1

P6 207 107 208 108 209 109 210 110 211 111

CC CB CF CG CE

E-2 E-1 E-4 E-3 E-6 E-5 E-8 E-7 E-10 E-9

GND

RCV 24A(1) RCV 24A(2) RCV 24A(3) RCV 24A(4) RCV 24A(5)

P7 201 101 202 102 203 103 204 104

PWI DSS DLO ACR

E-4 E-3 E-6 E-5 E-8 E-7 E-10 E-9 GND

RCV 24B(2) RCV 24B(3) RCV 24B(4) RCV 24B(5)

-001 ØR -002 ØPTIØN

HDR00 7C8 IDSR HDB01 7C8 ICTS HDB02 7C7 IAGC HDB03 7C7 HDB04 7C6 IRID LPCKT 5A7

HDB06 7C5 HDB07 7C5 HDB08 7C5 HDB09 7C4 HDB05 7C6

ITA(1)

INV 20A(16) INV 20A(17) INV 20A(18) INV 20A(19) INV 20A(20)

INV 28B(20) INV 28B(21)

22A(14) 22A(15) 22A(16) 22A(17) 22A(18)

27B(14) 27B(15) 27B(16) 27B(17)

CD 28A(4) P5 105 205

CD 28A(3)

17A(2) 17A(3) 26B(4)

INV 20A(21) INV 28B(22) INV 20A(22)

22A(19)

5A(14)

HTEST 2B2

P8 204 104

3A1 LTRDYDS

6AB 1C2 HØRDYDS 7/1 LINP LEAD 21A(18) 21A(17)

13AB LØRDYAD

ØHRDY 1D8 ØHTESKP 2A8 ØLRRP 3A4

-004 ØPTIØN

2: FOR CURRENT MODE ØPTIØN (-200) SEE SHEET 14.

NØTES: 1. TIE TO +V IF AUTO DIAL ØPTION IS NØT REQUIRED

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON		
BASIC DIMENSION	DECIMAL PLACES .XX	.XXX
UNDER 12	± .02	± .005
12 TO 24	± .03	± .010
OVER 24	± .06	± .015
ANGLES ± 0° 30'		

MATERIAL:

FINISH:

554102	704004
PROJECT	SPCL SYS.
APPLICATION	

DRAWN	E. PEREZ-CUBAS	DATE 6-7-71
CHECKED		
ENGR		8/2/71
PROJ ENGR		8/2/71
APPROVED		
APPROVED		

Systems Engineering Laboratories
Fort Lauderdale, Florida

LOGIC DIAGRAM (TEU) TEST LOGIC

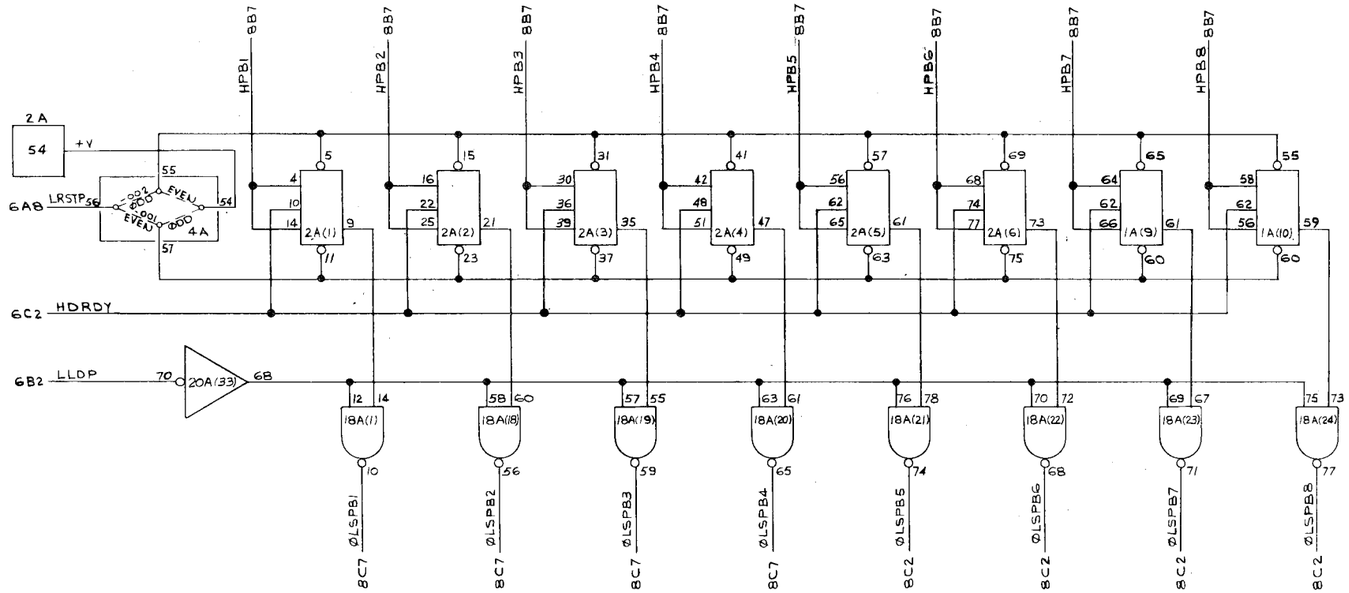
SIZE	CODE IDENT NO.	DWG NO.
D	20886	130-100659-000

SCALE | REV LTR | SHEET 9

ERN		REV	1
DATE			

REVISIONS

ZONE	LTR	DESCRIPTION	DATE	APPROVED



554102	704004
PROJ	SPCL5/6
APPLICATION	

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ON -

BASIC DIMENSION	DECIMAL PLACES .XX	.XXX
UNDER 12	± .02	± .005
12 TO 24	± .03	± .010
OVER 24	± .06	± .015

ANGLES ± 0° 30'

MATERIAL:

FINISH:

DRAWN	Schmandrak	5-4-71
CHECKED		
ENGR	C McDonald	8/2/71
PROJ ENGR	C McDonald	8/2/71
APPROVED		
APPROVED		

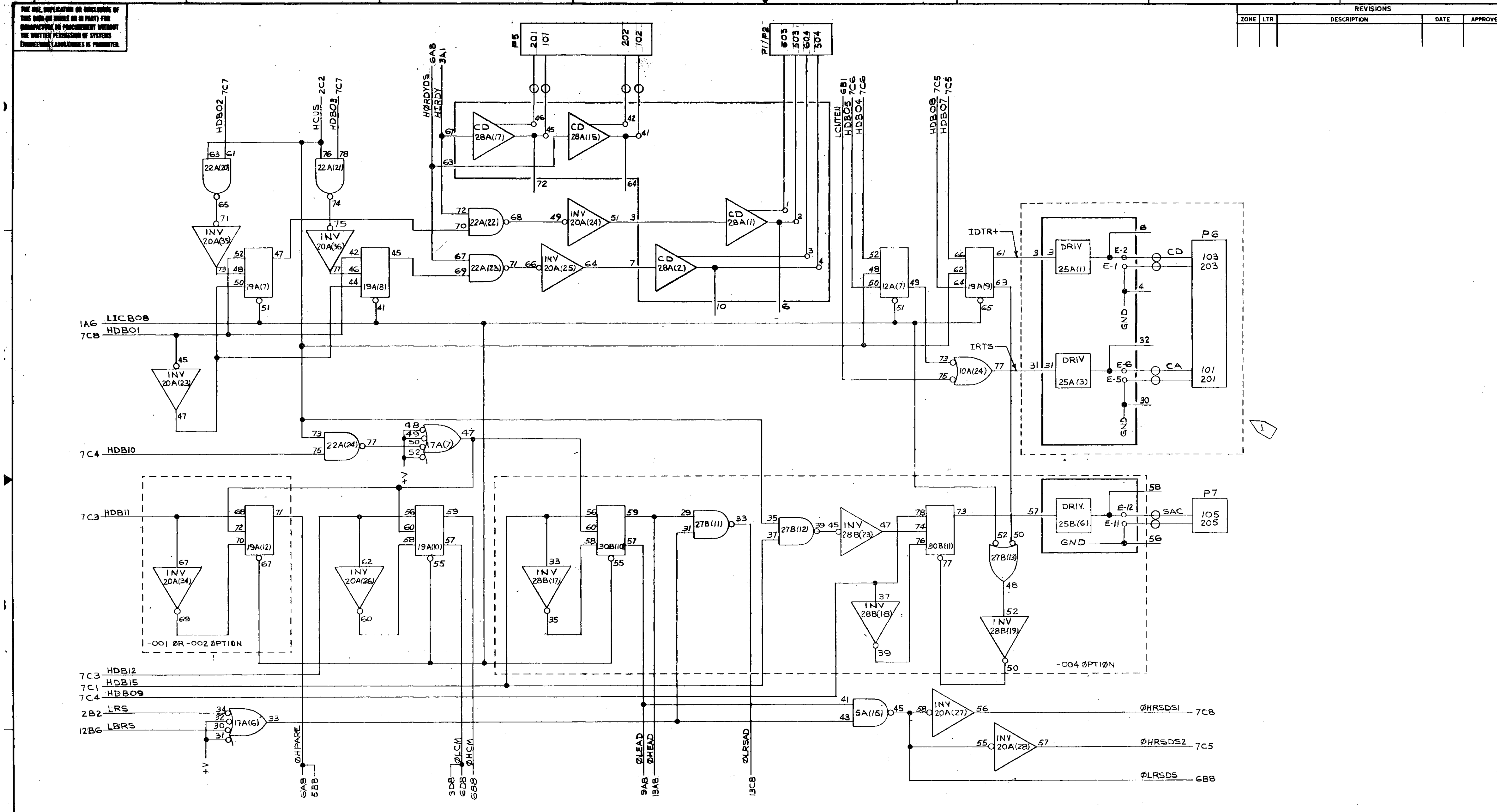
Systems Engineering Laboratories
Fort Lauderdale, Florida

LOGIC DIAGRAM PARITY REGISTER & LOAD GATES OPTION-001 OR-002

SIZE	CODE IDENT NO.	DWG NO.
D	20886	130-100659-000

SCALE | SHEET 10

130-100659-000



1. FØR CURRENT MØDE ØPTIØN (-200) SEE SHEET 14

NØTES:

554102	704004		
PROJ	SPCL. SYS		
APPLICATION			

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ON

BASIC DIMENSION	DECIMAL PLACES .XX	.XXX
UNDER 12	±.02	±.005
12 TO 24	±.03	±.010
OVER 24	±.06	±.015

ANGLES ± 0° 30'

MATERIAL:

FINISH:

DRAWN Schmondrak DATE 5-4-71

CHECKED

ENGR [signature] 8/2/71

PROJ ENGR [signature] 8/2/71

APPROVED

APPROVED

Systems Engineering Laboratories
Fort Lauderdale, Florida

LOGIC DIAGRAM
(CEU) COMMAND REG.
& CONTROL LOGIC

SIZE D | CODE IDENT NO. 20886 | DWG NO. 130-100659-000

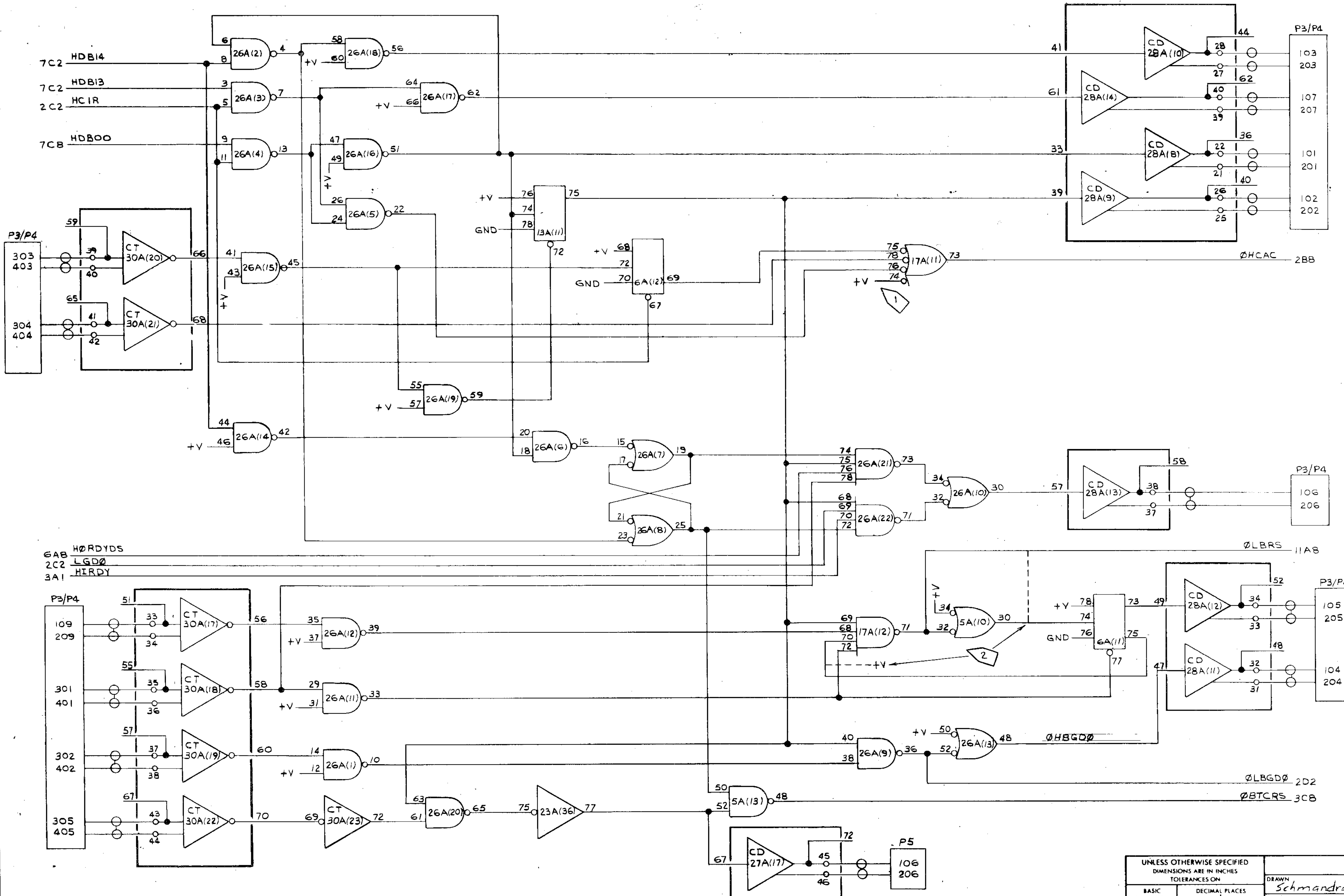
SCALE | SHEET 11

REVISIONS: ZONE | LTR | DESCRIPTION | DATE | APPROVED

ERN DATE REV 1

130-100659-000

ZONE	LTR	REVISIONS DESCRIPTION	DATE	APPROVED



2. WHEN THIS UNIT IS MØUNTED IN THE COMPUTER'S BTC #4 PØSITIØN REMØVE 6A75 FRØM 17A70. TIE 17A70 TØ 17A54(+V), REMØVE 5A30 FRØM 6A74. TIE 6A74 TØ 17A71. 5A30 ØUTPUT WILL NØT BE USED

NØTES: 1. TIE 17A76 TØ GND IF BTCI ØPTIØN IS NØT REQUIERED.

554102	704004
PROJ	SPCL. S/S.
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON

BASIC DIMENSION	DECIMAL PLACES .XX	.XXX
UNDER 12	± .02	± .005
12 TO 24	± .03	± .010
OVER 24	± .06	± .015

ANGLES ± 0° 30'

MATERIAL:

FINISH:

		DATE
DRAWN	Schmandrak	5·4·71
CHECKED		
ENGR	C McDaniel	8/2/71
PROJ ENGR	C McDaniel	8/2/71
APPROVED		
APPROVED		

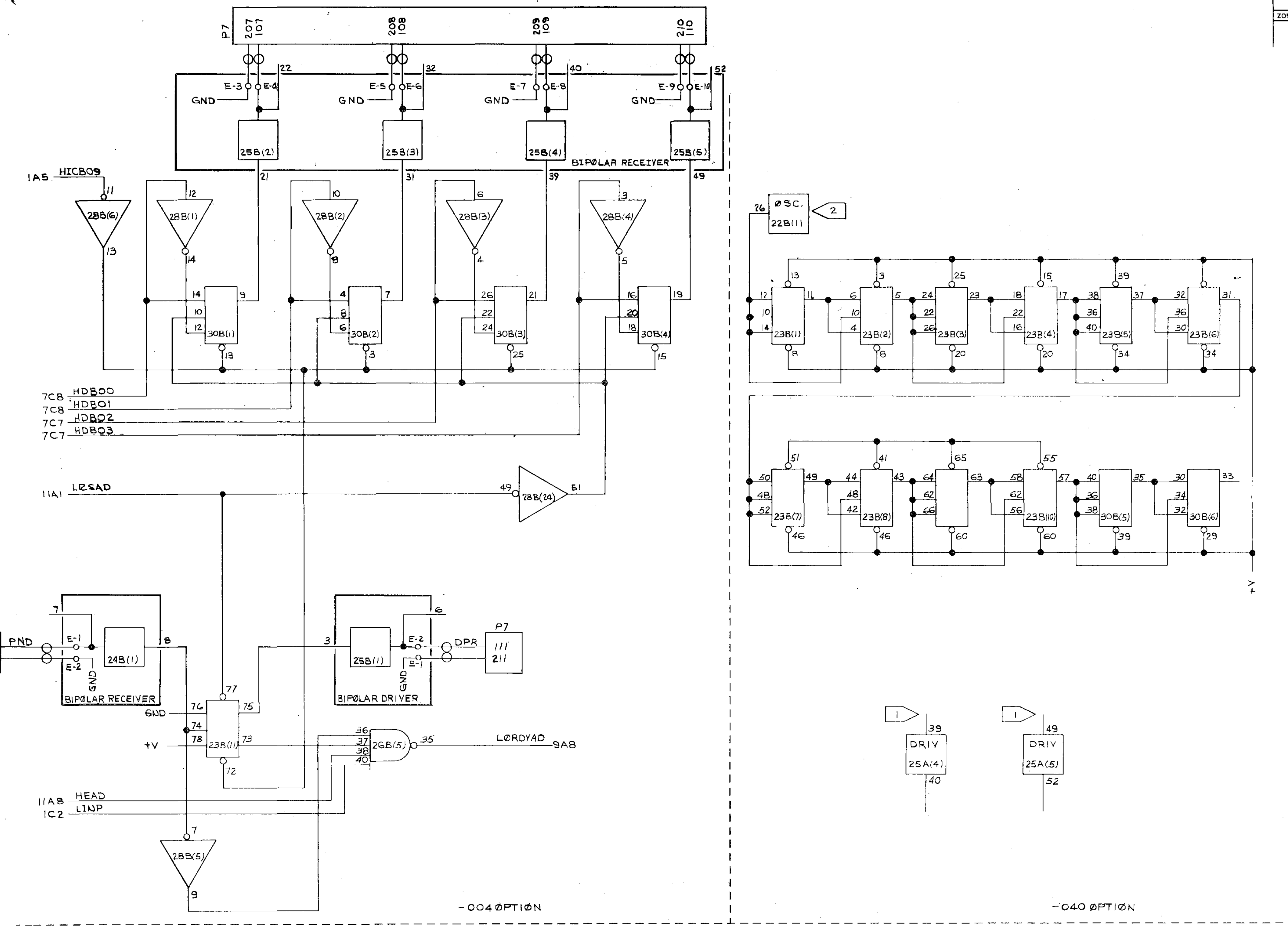
Systems Engineering Laboratories
Fort Lauderdale, Florida

LOGIC DIAGRAM BTCI OPTION

SIZE	CODE IDENT NO.	DWG NO
D	20886	130-100659-000

SCALE | SHEET 12

ZONE	LTR	REVISIONS DESCRIPTION	DATE	APPROVED



NØTES:
1. SUPPLEMENTAL WIRING ØF THESE PØINTS TØ FLIP-FLØP ØUTPUTS DETERMINED BY FREQUENCY REQUIREMENTS.
2. SELECT CRYSTAL TØ MEET FREQUENCY REQUIREMENTS

554102	704004
PROJ	SPCL. SYS.
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON

BASIC DIMENSION	DECIMAL PLACES .XX	.XXX
UNDER 12	± .02	± .005
12 TO 24	± .03	± .010
OVER 24	± .06	± .015

ANGLES ± 0° 30'

MATERIAL:

FINISH:

		DATE
DRAWN	Schmandrak	5-4-71
CHECKED		
ENGR	C McDonald	8/3/71
PROJ ENGR	C McDonald	8/3/71
APPROVED		
APPROVED		

Systems Engineering Laboratories
Fort Lauderdale, Florida

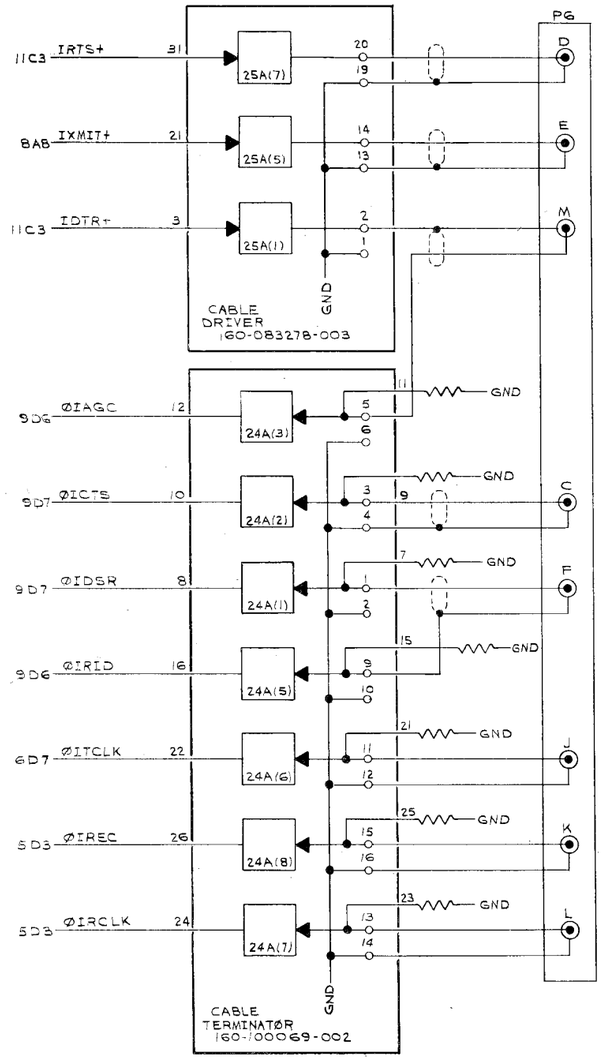
LOGIC DIAGRAM EXTERNAL CLOCK & AUTO DIAL LOGIC OPTIONS

SIZE	CODE IDENT NO.	DWG NO.
D	20886	130-100659-000

SCALE | SHEET 13

ERN
DATE REV 1

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED



P6 FUNCTION TABLE

CONN. POSITION	ELEMENT	FUNCTION
C	CENTER COND	CLEAR TO SEND
	SHIELD	GND
D	CENTER COND	REQUEST TO SEND
	SHIELD	GND
E	CENTER COND	TRANSMIT DATA
	SHIELD	GND
F	CENTER COND	DATA SET READY
	SHIELD	RING INDICATOR
J	CENTER COND	TRANSMIT CLOCK
	SHIELD	GND
K	CENTER COND	RECEIVED DATA
	SHIELD	GND
L	CENTER COND	RECEIVED CLOCK
	SHIELD	GND
M	CENTER COND	AGC LOCK
	SHIELD	DATA TERMINAL READY

NOTES:
1. ALL RESISTORS ARE 120Ω 1/4W

554102	704004
PROJ.	SPC. SYS
APPLICATION	

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ON

BASIC DIMENSION	DECIMAL PLACES .XX	.XXX
UNDER 12	± .02	± .005
12 TO 24	± .03	± .010
OVER 24	± .06	± .015
ANGLES ± 0° 30'		

MATERIAL:
FINISH:

DRAWN	E. PEREZ-CUBAS	DATE 6-9-71
CHECKED		
ENGR		8/4/71
PROJ. ENGR		8/2/71
APPROVED		
APPROVED		

Systems Engineering Laboratories
Fort Lauderdale, Florida

LOGIC DIAGRAM
-200
CURRENT MODE OPTION
DRIVERS & RECEIVERS

SIZE	CODE IDENT NO.	DWG NO.
D	20886	130-100659-000

SCALE | REV LTR | SHEET 14

A

	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
CARD TYPE	CABLE ASSEMBLY				LOGIC MIX #7	CABLE ASS'Y		HEX. INV.	2-NAND	3-NAND	HEX. INV.	JK-SC	2-NAND	4-NAND	HEX. INV.	GEN. REG. EVEN	3-NAND	JK-CC	JK-SC	O. S.	2-NAND	HEX. INV.	GEN. REG. EVEN	O. S.	JK-SC	2-NAND	JUMP CARD	4-NAND	JK-FF "AND"	JK-CC
CARD No	144-100210				900043	144-100294		900029 -003	100078 -003	900030 -003	900029 -003	900024 -003	100078 -003	900020 -003	900029 -003	100026 -001	900030 -003	900023 -003	900024 -003	100079 -001	100078 -003	900029 -003	100026 -001	100079 -001	900024 -003	100078 -003	093251	900020 -003	900022 -003	900023 -003
TOTAL CKTS					22			36	24	18	36	12	24	12	36	16	18	12	12	4	24	36	16	4	12	24		12	6	12
SPARE CKTS					0			0	0	0	0	0	0	2	0	0	0	2	0	0	0	0	0	0	0	0	0	0	0	0
CIRCUIT 1					12			1	1	1	1	2	10	9	7	7	8	8	6	6	6	4	4	5	5	5	3	3	10	5
2					12			1	1	1	2	2	8	9	7	7	8	8	6	6	6	4	4	5	5	3		3	10	5
3					12			1	1	1	2	2	8	9	7	7	8	8	6	6	6	4	4	5	5	3		3	10	5
4					12			1	1	1	2	2	8	3	7	7	8	8	6	6	6	4	4	3	5	3		3	10	5
5					12			1	1	2	2	2	8	6	7	7	8	8	6	X	6	4	4	X	5	3		3	10	5
6					12			1	1	2	2	2	8	11	7	7	8	8	6		6	4	4		5	3		3	10	5
7					12			1	2	2	2	11	8	11	7	7	8	8	11		6	4	4		5	3		3	X	5
8					12			1	2	2	2	11	8	3	7	7	8	8	3		4	4	4		5	3		3		5
9					12			1	2	2	2	11	8	3	7	7	6	6	3		4	4	4		3	3		3		10
10					12			1	2	2	2	11	8	3	7	7	6	6	3		4	4	4		3	12		5		10
11					12			1	2	2	2	8	8	12	7	7	6	12	3		4	4	4		12	3		5		6
12					12			1	2	2	2	11	8	12	7	7	6	12	3		4	4	4		12	6		5		6
13					12			1	2	2	2	X	8	X	7	7	3	X	X		4	4	4		X	12		X		X
14					12			1	9	2	2		8		7	7	3				4	4	4			9				
15					12			1	9	2	2		8		7	7	5				4	4	4			11				
16					12			1	9	2	9		8		7	7	3				4	4	4			3				
17					12			1	9	9	9		8		8	X	3				4	5	X			3				
18					12			1	9	9	9		10		8		3				4	5				6				
19					12			1	9	X	9		10		8		X				4	3				6				
20					12			1	11		9		10		8						4	3				6				
21					12			1	11		9		10		8						4	3				3				
22					12			1	11		9		10		8						4	3				3				
23								1	11		11		10		8						4	3				3				
24								1	11		11		10		8						11	3				3				
25								1	X		11		X		6						X	3				X				
26								1			11				6							3								
27								1			11				6							3								
28								1			11				6							3								
29								1			6				6							3								
30								1			6				6							3								
31								1			6				6							3								
32								1			6				6							3								
33								1			10				6							3								
34								1			11				6							5								
35								1			11				6							5								
36								12			11				6							5					3			
					4	9							1		1							2					7		3	

B

	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
CARD TYPE	JK-SC	3-[illegible]	HEX. INV.	2-NAND	4-NAND	CABLE ASSY		JK-CC	OSC.																					
CARD No	900024 -003	900030 -003	900029 -003	100078 -003	900020 -003	144-100293		900023 -003	083289 -000																					
TOTAL CKTS	12	18	36	24	12			12	1																					
SPARE CKTS	4	17	22	7	10			0	0																					
CIRCUIT 1	13	12	13					13	13																					
2	13		13					13	X																					
3	13		13					13																						
4	13		13		9			13																						
5	13		13		13			13																						
6	13		13					13																						
7								13																						
8								13																						
9								13																						
10	11							13																						
11	11			11				13																						
12				11				13																						
13	X			11	X			X																						
14				9																										
15				9																										
16				9																										
17			11	9																										
18			11																											
19		X	11																											
20			9																											
21			9																											
22			9																											
23			11																											
24			13																											
25				X																										
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27																														
28																														
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31																														
32																														
33																														
34																														
35																														
36																														
	8					5		8	6																					

NOTES
1-ADD FOR TRANSMIT
2-ADD FOR RECEIVE
3-ADD FOR PARITY
4-ADD FOR BTC1
5-ADD FOR AUTODIAL
6-ADD FOR EXT. CLK.
7-ADD FOR RECEIVE OR PARITY
8-ADD FOR EXT. CLK. OR AUTODIAL
IF BTC1, AUTODIAL & EXT. CLK. ARE NOT USED, ROW B IS NOT USED
9-SUBSTITUTE 144-100295 IN 24A AND 25A WHEN CURRENT MODE OPTION (-200) IS REQIERED

SIZE	130-100659-000	
D		
REV.	DESCRIPTION	DATE APPD

ITEM	DWG. OR PART NO.	DESCRIPTION

Systems Engineering Laboratories
6901 West Sunrise Blvd., Fort Lauderdale, Florida 33310

DR Schmandt	5-4-71	LOGIC DIAGRAM CIRCUIT COMPLEMENT SYNC MODEM
CHK		
ENGR	8/4/71	
PROJ	8/2/71	
APPD		
NEXT ASSY 554102(704004)		

CODE IDENT NO.	SIZE	
20886	D	130-100659-000

SHEET 15 REV.

NOTES:
1. UNLESS OTHERWISE SPECIFIED RESISTORS ARE ±5%, 1/4 W.
2. FOR WIRING DIAGRAM SEE D53280.

SIZE	53159	REV. A*
REV.	DESCRIPTION	DATE	APPD
A	69-222; 1.2K WAS 2.2K; 1.2K WAS 3.9K; 2N3947(3) WERE SS677; 2N3727 WAS SS677; 2N3251 WAS SS678. RKM 3-	3/11/69	

TBI-1
TBI-2
TBI-3
9 VAC IN
CR1 MR1120
CR3 MR1120
CR2 MR1120
CR4 MR1120
F1
10 AMP FOR 5 AMP OPER.
15 AMP FOR 10 AMP OPER.
SCR1 2N4168
+ C1 1300μf 15V
+ C2 1300μf 15V
R1 .1Ω 5W
13
4
1
2
150μf 30V
1N4004
1N4004
1.2K
510Ω
1N749A 4.3V
TP2
1K
1N914
2N3251
OTP1
15
1K
2N3947
14
R2 .2Ω 5W
R3 .2Ω 5W
R4 .2Ω 5W
10 AMP ONLY
IN754A 6.8V
6
27Ω
12
2N3725
10
11
Q1 2N5036
Q2 2N3772 - FOR 5 AMP OPER.
2N3771 - FOR 10 AMP OPER.
150μf 30V
1K
IN752A 5.6V
1K
2N3947
2N3947
.033μf 50V MYLAR
1K
TP3
10K
.1μf 10V
180Ω
10Ω
1.2K
680Ω
470Ω 1/2W
1μf 25V
1K
.1μf 10V
2500μf 10V
5
GRD.
TP4
3
680Ω 1/2W
160-083184
TBI-4

ITEM	DWG. OR PART NO.	DESCRIPTION

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Systems Engineering Laboratories
6901 West Sunrise Blvd., Fort Lauderdale, Florida 33310

DR	Tim Tipton	25AUG67
CHK	RKM	8-30-67
ENGR		
PROJ	R. Pinkerton	4-4-68
APPD		
NEXT ASSY	15929	

SCHEMATIC
240 SERIES
LOW VOLTAGE VARIABLE POWER SUPPLY

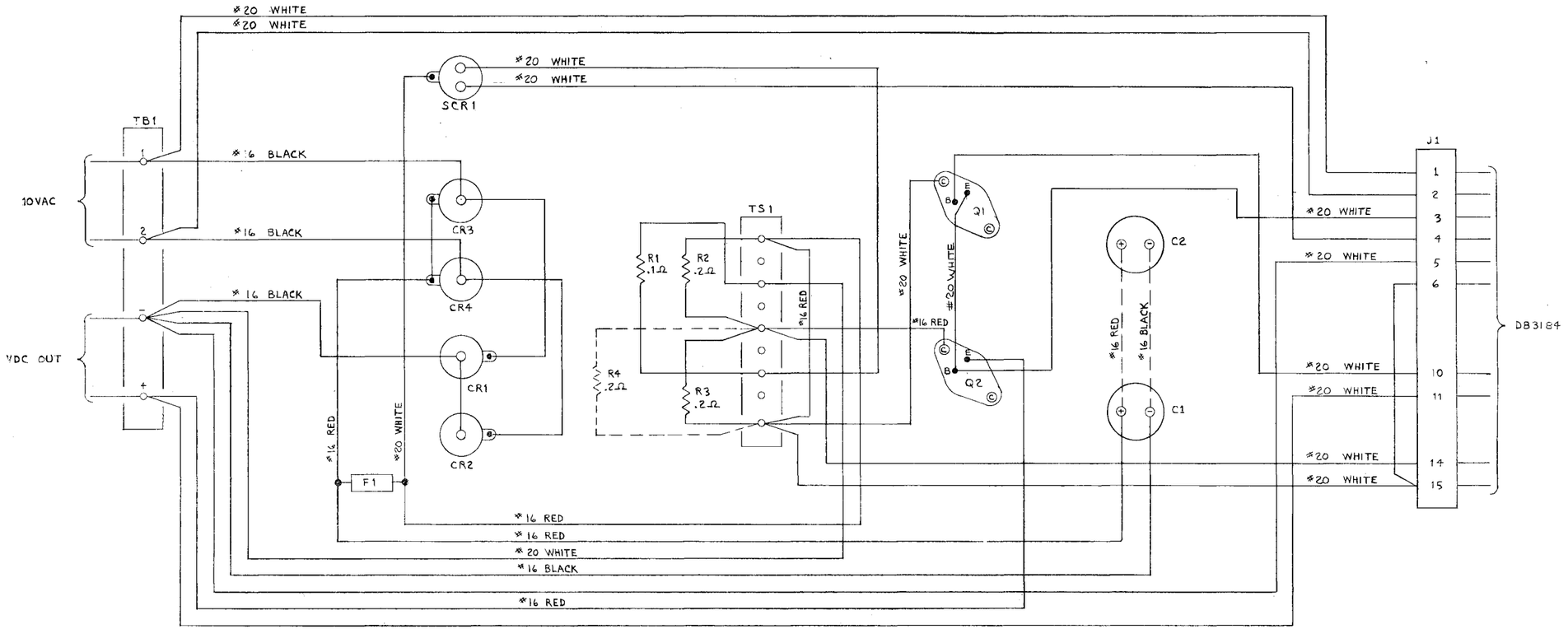
CODE IDENT NO.	SIZE		REV.
20886	D	53159	A

SHEET 1 OF 1

D 53159 A

NOTES:
1. DOTTED WIRING DESIGNATES 240-000-04
2. COMPONENT DESIGNATION ON CHASSIS TO BE DETERMINED BY MANUFACTURING.
3. FOR LOW VOLTAGE SCHEMATIC, SEE D53159
4. ALL WIRES ARE MIL-W-16878-TYPE C, 105°C, 600 V.

SIZE	53280	REV.
REV.	DESCRIPTION	DATE / APPD



ITEM	DWG. OR PART NO.	DESCRIPTION

Systems Engineering Laboratories
6901 West Sunrise Blvd., Fort Lauderdale, Florida 33310

DR M. LLOYD	3-1-68	WIRING DIAGRAM
CHK C. Wasti	4-4-68	240 SERIES
ENGR		LOW VOLTAGE VARIABLE PWR. SUPP.
PROJ R. Bollinger	4-4-68	240-000-01
APPD		
NEXT ASSY 15929		CODE IDENT NO. 20886 / SIZE D / 53280 / REV.

SHEET 1 OF 1