# TeleVideo Remote Workstation Processor Technical Reference 

## PREFACE

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## 1. INTRODUCTION

## GENERAL

The TeleVideo Remote Workstation Processor (RWP) consists of a case with power supply and four backplane slots. The RWP supports up to four TS 800R Remote Workstations. Each TS 800R Remote Workstation consists of an intelligent processor board, located in the remote workstation processor, and remotely-located TeleVideo 950 terminals. The terminals communicate with the RWP through modems. A diagram of a typical system configuration is shown in Figure l-l.

The remote workstation processor gives processing capability to a 950 terminal, through the intelligent processor board, and through access to a TeleVideo service processor, such as the TS $806 / 20$ or TS 816/40. The link between the 950 terminal and the remote workstation processor is RS-232C serial I/O, while the link between the remote workstation processor and the service processor is RS-422, TeleVideo Systems Service Processor Protocol.

The intelligent processor board contains a Z80A microprocessor, memory, and serial $1 / O$ devices. Standard main memory is 64 kilobytes, expandable to 128 kilobytes.


Figure 1-1. Remote Workstation Processor System Diagram

A BIZCOMP model lol2TV modem, manufactured by the Business Computer Corporation, may be purchased separately and mounted piggyback to the intelligent processor board. Due to power supply limitations, the BIZCOMP modem cannot be mounted inside the 950 terminal case. This modem is not supported by TeleVideo. Other modems, such as the Microbaud \#80512, may be used external to the remote workstation processor or 950 terminal case. These modems are also purchased separately and are not supported by TeleVideo.

## REFERENCES

The following publications contain information on the remote workstation processor.

* Remote Workstation Processor User's Manual (TeleVideo)
* TeleVideo Model 950 CRT Terminal Installation and User's Guide (TeleVideo)
* TeleVideo 950 Terminal Maintenance Manual (TeleVideo)
* Zilog Data Book (Zilog)


## 2. FUNCTIONAL DESCRIPTION

## GENERAL

The RWP contains up to four intelligent processor boards. Figure 2-l shows a block diagram of the RWP, with connectors to the intelligent processor board.

## INTELLIGENT PROCESSOR BOARD

Each intelligent processor board contains a zilog z80A microprocessor, associated Z80A peripherals, RS-422 and RS-232C serial I/O channels, and up to two optional additional RS-232C serial I/O channels.

Central processor functions are carried out by a $\quad 80 A$ microprocessor. The CPU communicates with the system using a l6bit address bus, and an 8-bit data bus. System interrupts are daisy chained with the CPU in the following priority order:

| (highest) | I | Z80A DMA |  |
| :--- | :--- | :--- | :--- |
|  | 2 | Z80A SIO | (RS-422 Port) |
|  | 3 | Z80A SIO | (RS-232C Port) |
|  | 4 | Z80A CTC | (Channel A) (optional) |
|  | 5 | Z80A DART | (Channel B) (optional) |

A Z 80A DMA direct memory access controller device operates in burst mode to transfer data between memory locations, memory and the board serial I/O ports, and between serial I/O ports.

Main memory is configured in $64 \mathrm{~K} x \mathrm{l}$ dynamic RAM devices. Standard main memory is 64 kilobytes, expandable to 128 kilobytes. Standard read-only memory is a single $4 \mathrm{~K} x 8$ type 2732A EPROM device. This memory may be expanded to 8 , 16 , or 32 K by using an additional EPROM socket and alternate devices, as shown in Table 2-1.

Table 2-1. Read-Only Memory Expansion

| Device | SEL A | SEL B | Read-Only <br> Memory Size | Address 1 | Address 2 |
| :--- | :---: | :---: | :---: | :---: | :--- |
| One 2732A | 1 | 1 | $4 \mathrm{~K} \times 8$ | 81000 | N/A |
| Two 2732A | 1 | 1 | $8 \mathrm{~K} \times 8$ | 81000 | 82000 |
| One or Two 2764 | 0 | 1 | $16 \mathrm{~K} \times 8$ | 82000 | 84000 |
| One or Two 27128* | 0 | 0 | $32 \mathrm{~K} \times 8$ | 84000 | 88000 |

*Also cut trace A-B (W7), connect jumper C-D (W4)


Figure 2-1. Remote Workstation Processor Block Diagram

The SEL A and SEL B lines referred to in Table 2-1 are traces adjacent to the memory control signals decoder. These lines must be cut or jumpered to produce the logic levels shown in the table. When 27128 EPROM devices are installed, the trace cuts and connections footnoted to the table allow decoding of address line ABl3.

Main memory can be configured into one of four memory maps, as shown in Figure 2-2. The configuration is software selectable using the -PROM and -BANK 1 lines from the diagnostic LED decoder. When the -PROM line is active low, read-only memory is selected. When -BANK 1 is active low, bank l of memory is selected. The bank 2 memory, when selected by -BANK l high, occupies 56 K of the CPU address space. When using bank 2 , the 8 K space from 56 K through 64 K remains in bank 1 to allow future implementation of the operating system.

Standard memory is shown in Figure 2-2A. Address 1 and Address 2 refer to the boundaries of installed read-only memory as listed in Table 2-1. If standard read-only memory is installed, it occupies the address space between 0 and 4 K . The area between 4 K and 8 K is accessable only when a second 2732A is installed. For the 2764 and 27128 EPROM devices, the boundaries for each device are as shown in Table 2-1. Figure 2-2B shows the memory map with read-only memory de-selected, allowing the CPU to addresses all 64 K of main memory.

Figure 2-2C shows the memory map with bank 2 and EPROM both selected. The CPU now addresses bank 2 of main memory, except for the upper 8 K of space from $\%$ EOOO through $\%$ FFFF which remains in bank l. The boundaries for read-only memory are as shown in Table 2-1 for each type of EPROM device. Figure 2-2D shows the memory map with bank 2 selected and EPROM de-selected. Again, the upper 8 K of space remains in bank l. The remainder of the address space is in bank 2 of main memory.

I/O port enables are decoded in a $32 \times 8$ ROM decoder addressed from lines AB2 through AB7. Table 2-2 contains a summary of the I/O port address scheme for the intelligent processor board. Refer to the system User's Manual for detailed instructions on using these ports.

A single $Z 80$ SIO device contains both the service processor interface and the user station interface. Channel A of the SIO contains the RS-422 synchronous SDLC link to the service processor. This channel operates according to the TeleVideo Systems Service Processor Protocol. Data is transmitted and received over this link at 800 kilobaud. Channel B of the SIO contains the RS-232C link to the user station. This channel is configured as a DTE unit for a modem. The modem outputs are


Figure 2-2. Memory Maps for Remote Workstation Processor

Table 2-2. I/O Port Addresses


Table 2-3. Interval Timer Settings for Baud Rates

| Baud <br> Rate | l6x <br> Rate | Divisor |
| :--- | :--- | :--- |$|$| 50 | 800 | 6144 |
| :--- | :--- | :--- |
| 75 | 1200 | 4096 |
| 110 | 1760 | 2793 |
| 135 | 2152 | 2284 |
| 150 | 2400 | 10244 |
| 300 | 4800 | 512 |
| 600 | 9600 | 256 |
| 1200 | 19200 | 171 |
| 1800 | 28800 | 154 |
| 2000 | 32000 | 128 |
| 2400 | 38400 | 85 |
| 3600 | 57600 | 64 |
| 7800 | 76800 | 43 |
| 9600 | 115200 | 32 |
| 19200 | 153600 | 16 |

available internally on connector P6, or externally on connector P5. Circuits $A, B, C A, C B, C F, D B$, and $D D$ are implemented to all full modem controls in either synchronous or asynchronous transmission modes. Baud rate for this channel is programmable to any standard data rate. Table 2-3 contains the CTC interval timer settings for each baud rate.

Two optional RS-232C serial I/O ports may be added to the board with the installation of a single 280 DART device. These ports are asynchronous. Baud rates are programmable to standard rates as listed in Table 2-3. These channels are configured DCE, and are reserved for future use.

An 8-element DIP switch is included on the board for default configuration. This switch is read by the CPU as an I/O port through the status switch buffer. Settings for the DIP switch are given in the system User's Manual.

## 3. CIRCUIT DESCRIPTION

## GENERAL

This section contains circuit descriptions of the major functional blocks on the intelligent processor board. A block diagram of the intelligent processor board is shown in Figure 3-1.

## CLOCR GENERATOR

The major components of the clock generator are:

| Y1 | l6 MHz Crystal-Controlled Oscillator |
| :--- | :--- |
| A59 | Oscillator Divider |
| Q1 | System Clock Driver |
| A61 | Timer Clock Divider |
| A63 | RS-422 Baud Rate Divider |

The 16 MHz oscillator provides the source frequency, which is divided by the oscillator divider to a $-2 \emptyset$ signal of 8 MHz , and a system clock signal of 4 MHz . The system clock signal is current amplified by the clock driver to become $\varnothing$ and $\varnothing$ BF.

The 8 MHz signal is divided in the timer clock divider to produce the clock triggers for the counter-timer device. Another divider uses $-2 \emptyset$ to produce BAUD RATE 422.

## CENTRAL PROCESSOR UNIT

The major components of the central processor unit are:

| A5 | Zilog Z80A Microprocessor |
| :--- | :--- |
| Al7,A18 | Address Buffers |
| A25,A39 | Type 2732A Read-Only Memory |
| A4 | Zilog 280A DMA Direct Memory Access |
| Al | Zilog 280A CTC Counter-Timer |

The central processor unit is based on the $Z 80 A$ microprocessor. This device produces addresses on lines A0 through Al5, which are buffered to become ABO through AB15. Data is carried on data bus lines D0 through D7.

A $280 A$ DMA device handles direct memory access transfer of data between memory locations and the RS-422 serial I/0 port. This device is operated in the burst mode through interrupts to the microprocessor. After the interrupt is acknowledged the DMA requests the bus. When the bus is granted, the transfer is accomplished and the DMA releases the bus. This transfer does not interfere with memory refresh.


Figure 3-1. Intelligent Processor Board Block Diagram

Counter-timer functions, including a time-of-day clock interrupt and programmable baud rates, are carried out in a Z80ACTC device under microprocessor control.

## MAIN MEMORY

The major components of main memory are:
A20 Memory Control Signals Decoder
A45,A54 Control Signals State Machine
A3,Al0,Al6, Bank 1 Main Memory
A24,A32,A38
A4 4 , A5 0
A2,A9,Al5, Bank 2 Main Memory (optional)
A23,A31,A37,
A43,A50
A52,A53 Memory Address Multiplexer
The memory control signals decoder is addressed on lines Al2 through Al5, and on lines -PROM and -BANKl. The decoder selects between the two banks of memory using the row address signals -RAS1 and -RAS2, and between the two read-only memory devices on lines -PROMICE and -PROM2CE, to produce the memory maps described in section 2. An additional decoder signal, -WAIT, is produced automatically with each read-only memory access.

For a memory access, the control signals state machine is held preset by MREQBF not true. When MREQBF is raised, it releases the preset state. The combination of the $Q$ output of the third flip-flop, plus MREQBF and the bank select signal, produces -RAS. The next clocks produce the SEL CLM and -CAS signals by successively clocking through the not true state of RFSH BF. When MREQBF is released, the state machine returns to its preset state.

For memory refresh, the RFSH BF signal goes high to hold the state machine preset, while the inverted refresh signal locks out the bank select signals. With both bank select signals, plus the third flip-flop signal held high, MREQBF high activates -RAS for both banks to accomplish the refresh.

To select read-only memory, the -PROM signal is set high to enable ROM selection, and the -BANK signal selects the device. With MREQBF high, the addressed device is enabled.

Main memory consists of type 8264 memory devices, each device containing 64 kilobits of storage. Standard memory is contained in a single bank of 64 kilobytes, which may be optionally expanded to 128 kilobytes. The memory control logic signals, and the multiplexed address, produce the read or write memory access on data lines D0 through D7.

## DECODERS

The major decoder components are:

| Al4 | I/O Port Decoder |
| :--- | :--- |
| A36 | Diagnostic LED Decoder |
| A8 | Status Switch Buffer |
| Sl | Status Switch Pack |

The I/O port decoder decodes lines AB2 through AB7 to produce I/O device enables. The port addresses for this decoder are listed in Table 2-2.

The diagnostic LED decoder is enabled as a port address of the I/O port decoder, and is written to using the -IOWR signal of the CPU. The diagnostic LED decoder uses lines AO and Al, and DO and Dl to activate the diagnostic LED devices as listed in Table 2-2. In addition, this decoder produces the -ASYNC signal to change the RS-232C modem signal clock source to support synchronous or asynchronous modes, the -LED5 signal to software activate the front panel CARRIER DETECT indicator, and the two memory control signals, -PROM and -BANKl.

The status switch buffer enables the settings of the 8-section status switch pack onto data bus lines D0 through D7. The buffer is an output port of the $I / O$ port decoder and is read with the CPU control signal, -IORD. Settings for the switch pack are given in the system User's Manual.

## SERIAL I/O

The standard intelligent processor board contains a single serial I/O device with two channels: one for RS-422 communication with the service processor, and one for RS-232C communication with a terminal or modem. An additional serial I/O device may be optionally installed to provide two RS-232C channels for a printer or general purpose.

The major serial I/O components are:

| A35 | Z80A SIO Serial I/O Device |
| :--- | :--- |
| A28 | Differential Line Receiver |
| A34 | Differential Line Transmitter |
| A46 | Modem Data Line Receiver |
| A55 | Modem Clock Line Receiver |
| A47 | Modem Baud Rate Selector |
| A42 | Modem Line Driver |
| A57 | Remote Reset Counter |
| A45 | Remote Reset Latch |

An RS-422 serial $1 / 0$ port is contained in channel A of a $Z 80 A$ SIO. This channel is set up for synchronous communication using SDLC protocol at initialization. Transfer of data between this port and main memory is interrupt-driven through Z80A DMA device
direct memory access. Differential data transmission through the SIO is supported by a differential line receiver and a differential line transmitter.

Channel $B$ of the SIO is configured as an RS-232C serial I/O channel for DTE operation with a modem. This channel contains provisions for connecting to a back-panel connector, or to a piggyback modem board. The piggyback modem is not supported by TeleVideo.

Separate line receivers are used for incoming data and clock signals. The output of the clock line receiver is applied to a modem baud rate selector, which allows either the modem signal in synchronous operation, or the programmable baud rate clock in asynchronous operation, to clock the SIO device. The SIO output is passed through a line driver to the modem.

The modem baud rate selector also interacts with the remote reset circuit. When in asynchronous mode, with the CTC supplying the baud rate clock, the occurrence of two successive twelve character period breaks without CPU intervention causes a general reset of the board.

The character periods are counted in the remote reset counter. As long as data is coming into the SIO, the counter is held cleared. When data stops, and there is carrier activity, the counter begins counting. If data does not return during the counting period to clear the counter, the clock pin of the remote reset latch is set low. Return of data clears both sections of the counter, and clocks the latch. If the CPU does not reset the latch by writing to the -CLR BREAK I/O port line, the second break of twelve characters generates a reset through a NAND function of the set latch and the inverted twelve count signal. This reset is passed through the modem baud rate selector to activate the -REMOTE RESET line and reset the board.

## OPTIONAL SERIAL I/O CHANNELS

The major components of the optional serial I/O channels are:

| A13 | Z80A DART Dual Asynchronous Receiver-Transmitter |
| :--- | :--- |
| A7,A29 | Line Receivers |
| A12,A22 | Line Drivers |

Two channels of RS-232C serial I/O may be added to the intelligent processor board by installation of an additional SIO device. These channels are configured as DCE ports in asynchronous-only operation. Each channel is programmed with separate baud rate lines from the CTC. Separate line receivers and line drivers are provided for each channel.

## 4. SYSTEM MAINTENANCE

## GENERAL

The intelligent processor board contains self test diagnostics that are automatically run during system initialization at powerup. These diagnostics light LED indicators on the board and on the RWP front panel. When the test are completed successfully, the board loads the operating system. The diagnostic LED indicators are not visible with the RWP case closed.

A special set of diagnostics for the system is available from TeleVideo. These diagnostics provide a more detailed check of the system, with error messages that closely isolate a malfunction.

## INITIALIZATION AND SELP-TEST DIAGNOSTICS

At power-on, the intelligent processor board begins executing its self-test diagnostics. First, interrupts are turned off and the remote reset latch is cleared. All diagnostic indicators are turned off. The processor then jumps to a data line and modified march test on both banks of memory. During this test diagnostic LED 1 and the front panel indicator are both lit.

The data line test loads a data byte into main memory starting at location 84000 and continuing through to 8 FFFF. The byte is then read back and compared for error. If there is no error, the byte is incremented and compared again until each bit of the memory location byte has been checked.

The march test fills memory from locations \% 4000 through 8 FFFF with a test pattern, then verifies the pattern, complements it, and verifies the pattern again. When completed for the first bank, the second bank is checked, if installed. During the second bank memory tests, indicators 1 and 2 are both lit, and the front panel indicator is off.

Failure of the memory test halts the diagnostics, and blinks the front panel indicator. For bank l, indicator l remains lit to specify the failed test; for bank 2, indicators land 2 remain lit. When the tests are successfully completed for all installed memory, the bank $l$ is switched in, the indicators go out, and the processor moves to the next test.

Start of the DMA test is signalled when diagnostic LED 3 and the front panel indicator both light. This test performs a memory-to-memory move with the DMA programmed to interrupt on end of block. The size and locations of the source and destination blocks are programmed into the DMA device, the DMA is
initialized, and the move is started. After the move, the processor compares both blocks of memory by checking each location in turn. Failure of the DMA test is indicated when the test halts, indicator 3 remains lit, and the front panel indicator blinks. Successful completion is signalled when both indicator 3 and the front panel indicator go out and the processor moves to the next test.

The SIO test is run on channel B (RS-232C, modem) of the SIO. This test writes and verifies an interrupt vector to the device. The test is signalled when diagnostic LEDs 1 and 2 and the front panel indicator all light. First, SIO register lis written with a data pattern to prevent it from affecting the test. Next, the interrupt vector is loaded to status register 2. This register is now read back, and if there is an error, the CPU halts, indicators 1 and 2 remain lit, and the front panel indicator blinks. If no error, the SIO is reset, and the processor moves on to the next test.

The final test uses channel l of the CTC to perform a CPU interrupt. This test is signalled when diagnostic LED 4 and the front panel indicator both light. Channels 0 and $l$ of the CTC are initially reset, and the interrupt vector address is programmed into the CTC. Channel lis given a command word and time constant, and the CPU performs a delay routine. After the delay, channel 1 is reset, and the CPU checks its interrupt flag. If there is no interrupt, the test halts, indicator 4 remains lit, and the front panel indicator blinks. Successful completion is signalled when both indicator 4 and the front panel indicator go out. The processor now blinks all diagnostic indicators and the front panel indicator once, and goes to the bootstrap routine.

In the bootstrap routine, the DMA and SIO devices are initialized, and the board is set up for SDLC protocol. The board sends a request block for booting the operating system to the service processor, and if successful, completes the operating system boot routine. Errors during this routine cause a reset of the DMA, SIO READY line, and SIO status register error flags. The SIO is shut down and the CPU loops on the subroutine that caused the error.

## A:CONNECTOR PIN ASSIGNMENTS

## CONNECTOR PI (POWER SUPPLY)

| PIN | SIGNAL | SIGNAL |
| :---: | :---: | :---: |
| NUMBER | DESIGNATOR | DESCRIPTION |
| 1 | -12V | -12 Volts |
| 2 |  | not used |
| 3 | GND | Ground |
| 4 | +5V | +5 Volts |
| 5 | +12V | +12 Volts |
|  | $\begin{gathered} \text { CONNE } \\ \text { (RS-422 } \end{gathered}$ |  |
| PIN | RS-422 | RS-422 |
| NUMBER | DESIGNATOR | DESCRIPTION |
| 1 | GND | Chassis Ground |
| 2 | TxD | Transmit Data + |
| 3 | RxD | Receive Data + |
| 4 | RTS | Request to Send+ |
| 5 | CTS | Clear to Send + |
| 6 | -TxC | Transmit Clock - |
| 7 | -RxC | Receive Clock - |
| 8 | GND | Signal Ground |
| 9 | -TxD | Transmit Data - |
| 10 | -RxD | Receive Data - |
| 11 | -RTS | Request to Send - |
| 12 | -CTS | Clear to Send - |
| 13 | TxD | Transmit Clock + |
| 14 | RxC | Receive Clock + |
| 15 | TEST | Test |

CONNECTOR P3

| PIN | SIGNAL | SIGNAL |
| :---: | :---: | :---: |
| NUMBER | DESIGNATOR | DESCRIPTION |
| 1 | --- | not used |
| 2 | --- | not used |
| 3 | RING | Ring |
| 4 | TIP | Tip |
| 5 | --- | not used |
| 6 | --- | not used |
|  | CONNECTOR P4 (INTERNAL MODEM PHONE | LINE) |
| PIN | SIGNAL. | SIGNAL |
| NUMBER | DESIGNATOR | DESCRIPTION |
| ]. | RING | Ring |
| 2 | TIP | Tip |

CONNECTORS P5, P8, P9
(RS-232C SERIAL I/O)

| PIN | RS-232C | RS-232C | P5 | P8, P9 |
| :---: | :---: | :---: | :---: | :---: |
| NUMBER | DESIGNATOR | DESCRIPTION |  |  |
| 1 | AA | Protective Ground | GND | GND |
| 2 | BA | Transmitted Data | TXD | RXD |
| 3 | BB | Received Data | RXD | TXD |
| 4 | CA | Request to Send | RTS | RT'S |
| 5 | CB | Clear to Send | CTS | CTS |
| 6 | CC | Data Set Ready |  | DSR |
| 7 | BA | Signal Ground | GND | GND |
| 8 | CF | Data Carrier Detect | DCD | DCD |
| 15 | DB | Transmit Clock | TxC |  |
| 17 | DD | Receive Clock | RxC |  |
| 20 | CD | Data Terminal Ready | DTR |  |

CONNECTOR P6
(INTERNAL MODEM)


## B:SYSTEM REPAIR PRICE AND SPARE PARTS PRICE LISTS

This section contains the Repair Price List for Computers and the Systems Spare Parts Price List in effect at the printing date of this manual. Use these lists for estimating repairs: prices are subject to change without prior notice.

# Repairs Price List for Computers 

March 1, 1983
DESCRIPTIONLogic Board TS 800 (Obsolete).\$ 135.00
Logic Board TS 800A, 802, 802H ..... 150.00
Logic Board TS 801 (Obsolete). ..... 175.00
Logic Board TS 806, 806/20 ..... 250.00
Logic Board TS 816, 816/40. ..... 350.00
Logic Board TS 1602G, 1602GH ..... 400.00
Graphics Board TS 1602G, 1602GH ..... 175.00
Floppy Controller (Daughter Board) TS 802, 802H ..... 50.00
Winchester Disk Controller (5" Drive \& 40MB 8" Drive). ..... 175.00
Tape Controller TS 806C. ..... 95.00
Interface Board TS 816 U ..... 50.00
Keyboard TS 800, 800A, 802, 802H. ..... 50.00
Keyboard TS 1602G, 1602GH. ..... 50.00
Fower Supply Module TS 800, 800A ..... 50.00
Power Supply TS 802, 802H, 806, 806H, 816, 1602G ..... 110.00
Video Module TS 800, 800A, 802, 802H, 1602G, 1602GH ..... 50.00
Floppy Disk Drive 5" ..... 160.00
Winchester Disk Drive 5" ..... 160.00
Winchester Disk Drive 8" ..... 450.00
Tape Drive ..... 300.00
Picture Tube Broken P31 ..... 214.00
Picture Tube Broken P39 ..... 230.00
Top Case Broken TS 802, 800A, 1602G ..... 80.00
Bottom Case Broken TS 802, 800A, 1602G ..... 100.00
Top or Bottom Case Broken Computer Boxes TS 806, 816 ..... 80.00
Front or Rear Panel Broken. ..... 60.00
Basic Repair charge (This additional amount charged when an entire system is returned for repair) ..... 70.00

TeleVideo will bill per above price schedule when no trouble is found in the module returned for repair.

## Out of Warranty

Customer to return defective replaceable module freight prepaid to the factory, 1170 Morse Avenue, Sunnyvale, CA 94086. TeleVideo will send replacement repaired module, billing per above price schedule plus return freight.
Prices subject to change without notice.

# \&.TeleVideo Systems, Inc. 

## 1170 Morse Avenue • Sunnyvale, CA 94086

Eastern Region - (212) 308-0705 • Northeast Region - (617) 369-9370 • Midwest Region - (312) 969-0112
South Central Region - (214) 258-6776 • Southwest Region - (714) 752-9488 • Northwest Region - (408) 745-7760 Southeast Region - (404) 447-1231 • European Sales - (31) 075-28-7461 TLX:844-19122 U.K./Scandinavian Sales -(44) 0908-668778 TLX:851-825151

## Systems Spare Parts Price List

05-10-83

PART PRICE DESCRIPTION
NUMBER


## MANUALS [class A]

| 2004200 | 20.00 | Guide, | Installation | \& User's TS | 800A |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 2003700 | 20.00 | Guide, | Installation | \& User's TS | 802 |
| 2003900 | 20.00 | Guide, | Installation | \& User's TS | 802H |
| 2248100 | 20.00 | Guide, | Installation | \& User's TS | 803 |
| 2133700 | 20.00 | Guide, | Installation | \& User's TS | 1602G |
| 2133800 | 20.00 | Guide, | Installation | \& User's TS | 1602GH |
| 2248600 | 20.00 | Guide, | Installation | \& User's TS | 1603 |
| 2003000 | 10.00 | Guide, | Installation | \& User's TS | 806 |
| 2226500 | 20.00 | Guide, | Installation | \& User's TS | 806/20 |
| 2004700 | 10.00 | Guide, | Installation | \& User's TS | 806C |
| 2002300 | 10.00 | Guide, | Installation | \& User's TS | 806H |
| 2232000 | 20.00 | Guide, | Installation | \& User's TS | 806H/20 |
| 2004100 | 10.00 | Guide, | Installation | \& User's TS | 816 |
| 2226400 | 20.00 | Guide, | Installation | \& User's TS | 816/40 |
| 2150300 | 50.00 | Guide, | User's TELEPL | LAN |  |
| 2200200 | 20.00 | Manual. | Operator's Te | ele3780 |  |
| 2219700 | 40.00 | Manual. | TeleDBMS |  |  |
| 2003200 | 25.00 | Manual. | Mmmost |  |  |
| 2003400 | 50.00 | Manual. | CP/M |  |  |
| 2162400 | 50.00 | Manual. | CPM/86 |  |  |
| 2150400 | 40.00 | Manual | TeleVideo - C | COBOL |  |
| 2133900 | 50.00 | Manual. | Maintenance T | TS 800A, 802 | 802H |
| 2230700 | 50.00 | Manual. | Maintenance T | TS 806/20, 80 | 6, 806C |
| 2131400 | 50.00 | Manual. | Maintenance T | TS 816 |  |
| 2259000 | 50.00 | Manual. | Maintenance T | TS 1602G/GH |  |
| 2291000 | 50.00 | Manual. | Maintenance T | TS 803 |  |

KITS [class B]
2000700
300.12 Kit, Spare Parts, Logic Board 8 Bit Systems *

2252100 703.50 Kit, Spare Parts, Logic Board 16 Bit Systems *
2202900 244.80 Kit, Spare Parts, Logic Board WDC *
2203000 199.59 Kit, Spare Parts, Logic Board FDC *
2252000 401.40 Kit, Spare Parts, Graphics Board TS 1602G *
2280700
2202800
2228400
2270800
153.28 Kit, Spare Parts, Video Mod ts 800A * 90.88 Kit, Spare Parts, Mechanical TS 802/800A* 235.72 Kit, Spare Parts, Data Cables TS 816's* 223.08 Kit, Spare Parts, Data Cbls TS 806 \& User Stat *

* Contents of Kits at end of List


Full Height Half Height Half Height

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PART PRICE DESCRIPTION
NUMBER

MISC. MAJOR PARTS [class D]
2049300 179.00 Picture Tube Black/Green 12" P3l
2173800 192.00 Picture Tube Black/Green 12" P39 Graphics (1602G)
2218700 192.00 Picture Tube Black/Green $1^{\prime \prime}$ P31P
2090200 175.00 Detachable Keyboard TS 800A/802 *
2183701210.00 Detachable Keyboard TS 1602G *
2183700210.00 Detachable Keyboard TS 803/1603 *

2099800 70.20 Case Bottom TS 806/806-20/RWP
2099900 70.20 Case Top TS 806/806-20/RWP
2100600
2100700
2100800
2141700
2141800
2141900
2103100
2103200
2188300
2188500
2188600 110.00 Case Top TS 802/1602G 85.00 Case Bottom TS 802/1602G 40.00 Bezel TS 802/1602G 70.20 Case Bottom TS 800A 97.80 Case Top TS 800A 20.00 Bezel TS 800A 70.00 Case Top TS 816/816-40
180.00 Case Bottom TS 816/816-40 16.32 Case Back Cover Crt TS 803/1603
71.16 Case Main Elect. TS 803/1603

2188800 66.00 Case CRT

TS 803/1603
2189100 15.48 Bezel
10.68 Case Arm Top

TS 803/1603
2189200
2218800
2291100 1.44 Thumb Wheel Adj TS 803/1603

TS 803/1603
. 12 Case Arm Bottom TS 803/1603 26.10 Power Cord TS 803/1603

* ORDER APPROPRIATE LABELS FROM LABELS/LOGO'S (PAGE 7)

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PART PRICE DESCRIPTION
NUMBER

FIRMWARE
8000002 16.92 IC 2332 Char Gen Upper Character Cell 800000316.92 IC 2332 Char Gen Lower Character Cell 800000923.28 IC 8048 With Program ROM for Keyboard TS 800A/802 $8000016 \quad 15.0$ IC charicter Gen. for Graphics Systems $8000018 \quad 34.50$ IC 2716 System Program EPROM Kybd TS 800A/802
$8000045 \quad 37.50$ IC System Program EPROM Z80 Portion TS 800A/802
$8000046 \quad 37.50$ IC System Program EPROM Lower Terminal Firmware
8000047 37.50 IC System Program EPROM Higher Terminal Firmware
$8000050 \quad 37.50$ IC System Program EPROM Z80 Portion TS 802 H
800002455.80 IC System Program EPROM 450ns TS 806
$8000053 \quad 30.90$ IC System Program EPROM 450ns TS 816
$8000106 \quad 30.90$ IC System Program EPROM 450ns TS 816/40
800005430.90 IC System Program EPROM 450ns TS 806C
800009324.00 IC System Program EPROM 450ns TS 1602G/GH
$8000080 \quad 5.40$ IC Memory Decode TS 1602G
8000079 5.40 IC I/O Decode TS 1602G
800002755.80 IC Diagnostic EPROM TS 806
800005255.80 IC Diagnostic EPROM TS 806C
800009655.80 IC Diagnostic EPROM TS 816
800010755.80 IC Diagnostic EPROM TS 816/40
$8000035 \quad 23.70$ IC L2-7 System Program ROM WDC ( 74 S 472512 X 8)
8000036 23.70 IC MX-7 System Program ROM WDC ( 74 S 472512 X 8)
8000037 23.70 IC FX-7 System Program ROM WDC (74S472 5l2 X 8)
8100024100.00 Listing System Program TS 806 *

8100045 100.00 Listing 800A, 802, [Z80 Portion] *
8100046500.00 Listing 800A, 802, 802H [6502 Portion] * 8100050 100.00 Listing TS 802H [Z80 Portion] * 8100053 100.00 Listing System Program EPROM TS 816 W/Code * 8100054 100.00 Listing System Program EPROM TS 806C * 8100093100.00 Listing System Program EPROM TS 1602G/GH *

* Require non-disclosure agreements and letter of intended use.


## CABLES/CONNECTORS/WIRE ASSEMBLIES

2005700
2006800
2006900
2007001
2007300
2006100
2006901
2007000
2006801
2006501
2006600
2006400
25.44 Cbl Asy, Keyboard TS 800A/802
14.22 Cbl Asy, 20 Pin 12" TS 802H WDC To Winchester
18.60 Cbl Asy, 34 Pin $15^{\prime \prime}$ TS 802H Daughter Bd/Floppy WDC/Winch
32.28 Cbl Asy, 40 Pin $16^{\prime \prime}$ TS 802H Daughter Bd To WDC
29.16 Cbl Asy, 34 Pin $14^{\prime \prime}$ TS 802 Daughter Bd To Floppy
11.88 Cbl Asy, 40 Pin $2^{\prime \prime}$ TS $802 / \mathrm{H}$ Logic to Daughter Bd 18.96 Cbl Asy, 34 Pin TS 806 Logic To Floppy/WDC To Winch 20.28 Cbl Asy, 40 Pin $13^{\prime \prime}$ TS 806 Logic To WDC 14.52 Cbl Asy, 20 Pin 15" TS 806-816/40 WDC To Winchester 11.34 Cbl Asy, 16 Pin $8^{\prime \prime}$ TS 806 RS 422 To Logic 36.00 Cbl Asy, 34 Pin 7" TS 806 Parallel Printer 24.12 Cbl Asy, 50 Pin $16^{\prime \prime}$ TS 816 WDC To Winchester

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PART
PRICE
DESCRIPTION
NUMBER

2006201
2006601
2006500
2007100
2007101
2007800
2128500
2006300
2007600
2007700
2135700
2007002
2006204
2006200
2006404
2224300
2235400
2160700
2235500
2160800
2161000
2235600
2008600
2007900
2136500
2008000
2008101
2008201
2176200
2008800
2008900
2136702
2192901
2008400
2008401
2008700
2097900
2141200
2208400
2098000
2163100
2097800
2165300
2098100
2216400
2098103
2098104
2098106
2098107
2098108


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## PART <br> PRICE <br> DESCRIPTION

 NUMBER2174401
2098300
2098703
2098800 2098801 2098802 2098700 2001200 2109000
8.10 Connector 50 Pin Header - Angle
1.80 Connector 2 Position Jumper
1.74 Connector 2 Pin Right Angle Molex
. 72 Connector 2 Pin Straight Wafer
3.72 Connector 3 Pin Straight Wafer
. 72 Connector 5 Pin Straight Wafer
1.02 Plug 5 Pin Molex Right Angle Wafer
11.34 Jack Socket Connector Kit
19.87 Power Cord 3 Conductor 3 Prong 6 FT

CRYSTALS

2098602
2216500
2098603
2098605
2048800
2042800 2098604 2035200 2099700

2099000 2141500 2245800 2245700

2142000
2142100
2142200
2105401
2105500
2105600
2100102
2100500
2219800
2100300
2105700


FANS
35.28 Fan 115V/230V AC 36-47 CFM (AIR OVER)
52.50 Fan Box 230 V AC TS $802 / 802 \mathrm{H}$
56.28 Fan Box ll5V AC TS 1602G/GH
67.20 Fan Box 230V AC TS 1602G/GH

BEZEL'S/CASE ASSEMBLIES

| 40.00 | Panel Front | TS 806 |
| :--- | :--- | :--- |
| 40.00 | Panel Front | TS 806C |
| 40.00 | Panel Front | TS 806H |
| 40.00 | Panel Back | TS 806 |
| 40.00 | Panel Back | TS 816 |
| 40.00 | Panel Front | TS 816 |
| 10.00 | Shroud Connector | TS 800A |
| 10.00 | Shroud Connector | TS 802/1602G |
| 5.00 | Card Guide | TS 802 |
| 15.00 | Cover Fan | TS 816 |
| 28.80 | Panel Floppy Cover TS 802H (Plastic) |  |

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PART PRICE DESCRIPTION
NUMBER


## MISCELLANEOUS SPARES

2101600
2101900
2103500
2152800
2150100
2001300
2101900
2204900
2225200
64.80 Chassis Mounting TS 806/806H
5.88 Panel Cover Hard Disk TS 806
19.98 Cover Top Power Supply TS 802
6.72 Speaker (8 ohm) With Connector
41.70 Filter A.C. Line SAE HP2-2
2.88 Bail Mount Enclosure
5.88 Panel Shield Winchester Disk TS 806
2.89 Shield Board TS 816
31.80 Bracket TS 816/40 WDC

LABELS/LOGO'S
2105000
2191300
2105104
2105105
2105106
2208500
2208600
2105300
2105301
2154402
2142900
2142901
1.50 Label Logo Plastic "TeleVideo" Systems
2.40 Label Logo Plastic "TeleVideo" Printer
.72 Label Keyboard TS 800A
. 72 Label Keyboard TS 802
. 72 Label Keyboard TS 802H
. 72 Label Keyboard TS 1602G
. 72 Label Keyboard TS 1602GH
. 96 Label Back Panel "RS 232" TS 806-806/20
. 96 Label Back Panel "Terminal" TS 806-806/20
1.50 Label Back of Unit TS 800A
. 90 Label Sl TS 800A
. 90 Label S2 TS 800A

BOXES/PACKING MATERIAL

2208800
2143600
2143700
2208900
2143800
2209000
2185700
2208200
2214401
2237300
25.00 Carton Inner
16.86 Carton Outer 20.52 Carton Inner 31.98 Carton Outer 26.22 Carton Inner
31.98 Carton Outer
3.18 Corner Blocks 16.00 Carton 12.00 Formed Foam 10.00 Formed Foam

Shipping TS 802/TS 1602G Shipping TS 802/TS 1602G Shipping TS 806 Shipping TS 806 Shipping TS 816 Shipping TS 816 Shipping Carton Shipping Hard Disk TS 806 TS 800A

ALL PRICES SUBJECT TO CHANGE WITHOUT NOTICE
MINIMUM ORDER $\$ 500.00$
2280700 Kit, Spare Parts, Power - Video Module TS 800A $\$ 153.28$
2042200 2N3906 Vertical Amplifier
2046500 2N3904 Vertical Drive
2200000 2N4401 Horizontal Drive
2047100 2N555l Reference Amplifier
2046700 KTCl627A 75Volt Regulator
2201400 DS135D/IN391
2047500 IN914
2200800 Yoke Deflection With Connector
2201200 Transformer Horizontal Drive
2200900 Linearity Coil 5.40uh
2201300 Transformer Flyback (High Voltage)
2201000 Inductor 27 uh
2126900 Voltage Regulator LAS 16CB 2A/13.8Volts
2186200 Resistor CF 390 Ohms 1/2Watt 5\%
2201600 IN759A Zener Diode
2199300 Capacitor 220 uf l6Volt Electrolytic
2197300 Capacitor .luf 600Volt Mylar
2047300 2SC2233 MJE13006
2280800 Diode 30S2 I.R. 3 Amp
2126600 Voltage Regulator LAS Ll 4053 Amp 5 Volt
2000700 Kit, Spare Parts, Logic Bd 8 Bit Systems $\mathbf{3 0 0 . 1 2}$
2042600 26LS32 RS422 interface
2042400 26LS3l RS422 interface
2050600 SIO/2 serial communications chip
2050800 CTC counter timer chip
2051000 CPU Z80A central processor unit
2051200 DMA direct memory access chip
205160064 K dynamic RAM (4 each)
2029200 75188N
202940075189 N
2228400 Kit Data Cables TS 816's $\quad$ 235.72
2006201 Logic to Tape/Logic to 816U
2006400 Logic to Winchester 816
2006801 816/40 WDC To Winchester
2006601816 Parallel Printer to Logic
2007002 816/40 logic to WDC
2006204 816/40 Logic to Tape/Logic to 816U
2006200 816/40 Logic to WDC
2006404 816/40 WDC to Winchester
2224300 816/40 Parallel Printer
2203000 Kit, Spare Parts Logic bd FDC $\quad$ 199.59
2040200
2040400
2040600
WD2143-01 four phase clock logic
WDl691 floppy support logic
FDl793-02 (93816 fair amd) floppy controller


2270800 Kit Data Cables User Stations and TS 806's \$ 223.08 2006800 802H WDC To Winchester 2007001802 H Daughter Board To WDC 2007300802 Daughter Board To Floppy 2006100802 Logic to Daughter Board 2135700 l602G Logic to Graphics Board 2006900 802H Daughter Board To Floppy/ WDC To Winchester 2006501806 RS422 to Logic 2006901806 .Logic To Floppy/ WDC To Winchester 2007000806 Logic To WDC 2006801806 WDC To Winchester 2006600806 Parallel Printer

| 2202800 | Kit, Spare Parts, Mechanical TS802/800A | \$ 90.88 |
| :---: | :--- | :--- |
| 2005700 | cord for keyboard |  |
| 2223700 | 3 amp l25V fuse (25 each) |  |
| 2199400 | keyswitch |  |
| 2096800 | lo position side dip switch |  |
| 2223300 | lamp 250V fuse ( 25 each) |  |
| 2182100 | RS232 connector |  |
| 2097900 | RJ-1l connector |  |
| 2098000 | RS422 connector |  |
| 2100500 | connector shroud |  |

2202900 Kit, Spare Parts Logic bd WDC \$ 244.80 2056200 parallel converter 2056400 MFM converter 2056600 AM detector 2056800 CRC generator/checker 2057000 parallel to serial converter 2057200 delay line

| 2252000 Kit, Graphics Board | S 401.40 |  |
| :---: | :--- | :--- | :--- |
| 2057400 | IC Gate Array Graphics/l603 |  |
| 2139800 | IC 7220 Graphic Display Controller |  |
| 2139200 | IC Dynamic RAM 4116 16K x l (l20ns) [4 each] |  |

2252100 Kit, Spare Parts, Logic Board 16 Bit Systems $\$ 703.50$ 205160064 K dynamic RAM (. 4 each)
2029200 75188N
202940075189 N
2042600 26LS32 RS422 interface
2042400 26LS3l RS422 interface
2054000 IC 8284A Clock Generator
2054200 IC 8288 Bus Controller
2054400 IC P8088 CPU IAPX 88/10
2054600 IC 8274 USART
2054800 IC 8254 Program Interval Timer
2055000 IC 8259A Priorty Interrupt Controller
2055200 IC 8089 IOP

## C:DRAWINGS

This section contains board assembly drawings and logic diagrams. When ordering parts, use the component type or value shown in the diagrams to refer to the TeleVideo part number listed in the Appendix B Spare Parts Price List. The prices listed in the Spare Parts Price list are for estimating only.








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